# 电子系统设计第二次作业

PB21511897 李霄奕

1.

module unit (

input wire cs\_n,

input wire en,

input wire [3:0] D,

output reg [3:0] Q

);

always @(\*) begin

if ({en,cs\_n}==2’b10) begin

Q <= D;

end

else begin

Q <= Q;

end

end

endmodule

2.

module decoder3\_8 (

input wire [2:0] sel,

input wire [3:0] data\_in,

input wire en,

output wire [3:0] data\_out\_0,

output wire [3:0] data\_out\_1,

output wire [3:0] data\_out\_2,

output wire [3:0] data\_out\_3,

output wire [3:0] data\_out\_4,

output wire [3:0] data\_out\_5,

output wire [3:0] data\_out\_6,

output wire [3:0] data\_out\_7

);

reg [7:0] decoder\_out;

wire cs\_0 = decoder\_out[0];

wire cs\_1 = decoder\_out[1];

wire cs\_2 = decoder\_out[2];

wire cs\_3 = decoder\_out[3];

wire cs\_4 = decoder\_out[4];

wire cs\_5 = decoder\_out[5];

wire cs\_6 = decoder\_out[6];

wire cs\_7 = decoder\_out[7];

always @(\*) begin

case (sel)

3'b000:decoder\_out = ~8'b00000001;

3'b001:decoder\_out = ~8'b00000010;

3'b010:decoder\_out = ~8'b00000100;

3'b011:decoder\_out = ~8'b00001000;

3'b100:decoder\_out = ~8'b00010000;

3'b101:decoder\_out = ~8'b00100000;

3'b110:decoder\_out = ~8'b01000000;

3'b111:decoder\_out = ~8'b10000000;

endcase

end

unit U0( cs\_0,en,data\_in,data\_out\_0);

unit U1( cs\_1,en,data\_in,data\_out\_1);

unit U2( cs\_2,en,data\_in,data\_out\_2);

unit U3( cs\_3,en,data\_in,data\_out\_3);

unit U4( cs\_4,en,data\_in,data\_out\_4);

unit U5( cs\_5,en,data\_in,data\_out\_5);

unit U6( cs\_6,en,data\_in,data\_out\_6);

unit U7( cs\_7,en,data\_in,data\_out\_7);

endmodule

3.

`timescale 10ms/1ms

module decoder3\_8\_tb();

reg [2:0] sel;

reg [3:0] data\_in;

reg en;

wire [3:0] data\_out\_0;

wire [3:0] data\_out\_1;

wire [3:0] data\_out\_2;

wire [3:0] data\_out\_3;

wire [3:0] data\_out\_4;

wire [3:0] data\_out\_5;

wire [3:0] data\_out\_6;

wire [3:0] data\_out\_7;

decoder3\_8 U0(

sel,

data\_in,

en,

data\_out\_0,

data\_out\_1,

data\_out\_2,

data\_out\_3,

data\_out\_4,

data\_out\_5,

data\_out\_6,

data\_out\_7

);

initial begin

//以下证明en对data\_in和sel起控制作用

#0 en=1; #0 data\_in=0; #0 sel=0;//设置初始状态

#1 en=0;

#2 data\_in=1;

#3 en=1;

#4 en=0;

#5 sel=1;

#6 en=1;

//以下证明data\_in的作用

#7 data\_in=2;

#8 data\_in=3;

//以下证明sel的作用

#9 sel=2;

#10 sel=3;

end

endmodule