数字部分 实验二 逻辑综合与等价性检查

思考题

(1) 将2.5节中打开阅读的时序库文件对应的PVT信息填入表格中。

|  |  |  |  |
| --- | --- | --- | --- |
| 时序库文件名 | 工艺角 | 电源电压 (V) | 温度 (℃) |
| **fast\_vdd1v0\_basicCells.lib** |  |  |  |
| **slow\_vdd1v0\_basicCells.lib** |  |  |  |

(2) 将2.5节中逻辑综合各阶段得到的电路基本信息填入表格中。

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 综合阶段 | **elaborate** | **syn\_generic** | **syn\_map** | **syn\_opt** |
| #Leaf Cells |  |  |  |  |
| #Terms |  |  |  |  |
| #Nets |  |  |  |  |
| #StdCells |  |  |  |  |
| 电路单元名称 |  |  |  |  |

(3) 从2.6节生成的报告中，找出以下数据并填入表格中。

**report\_timing命令运行结果中的部分数据**

|  |  |
| --- | --- |
| **Critical Path** | **Value** |
| **Group** |  |
| **Start Point** |  |
| **End Point** |  |
| **Clock Edge (ps)** |  |
| **Output Delay (ps)** |  |
| **Require Time (ps)** |  |
| **Data Path Delay (ps)** |  |
| **Slack (ps)** |  |

**report\_power命令运行结果中的部分数据**

|  |  |
| --- | --- |
| **Item** | **Value** |
| **Instance** |  |
| **Cells** |  |
| **Leakage Power (nW)** |  |
| **Dynamic Power (nW)** |  |
| **Total Power (nW)** |  |

**report\_qor命令运行结果中的部分数据**

|  |  |
| --- | --- |
| **Item** | **Value** |
| **Clock Period (ps)** |  |
| **Critical Path Slack (ps)** |  |
| **Total Negative Slack (TNS) (ps)** |  |
| **Sequential Instance Count** |  |
| **Combinational Instance Count** |  |
| **Total Area (um2)** |  |
| **Max Fanout** |  |
| **Min Fanout** |  |
| **Average Fanout** |  |

(4) 从5.4节生成的报告中，找出以下数据并填入表格中。

**set system mode lec命令运行结果**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Mapped points: SYSTEM class** | | | | |
| **Mapped points** | **PI** | **PO** | **DFF** | **Total** |
| **Golden** |  |  |  |  |
| **Revised** |  |  |  |  |

**compare**命令运行结果

|  |  |  |  |
| --- | --- | --- | --- |
| **Compared points** | **PO** | **DFF** | **Total** |
|  |  |  |  |

**report verification**命令运行结果

|  |  |
| --- | --- |
| **Verification Report** | |
| **Category** | **Count** |
| **1.** **Non-standard modeling options used:** |  |
| **2.** **Incomplete verification:** |  |
| **3.** **User modification to design:** |  |
| **4.** **Conformal Constraint Designer clock domain crossing checks recommended:** |  |
| **5.** **Design ambiguity:** |  |
| **6.** **Compare Results:** |  |

要求：思考题解答以电子版形式发给数字设计助教老师，文件名为：学号+姓名。