COVER

Revision	Description	Date	Drawn	Checked
V10A	Initial	2016-10-27	xxxlzjxxx	
V10B	1、修复BUG	2018-03-27	xxxlzjxxx	

Schematics Index:

Schematics Block:

BUG

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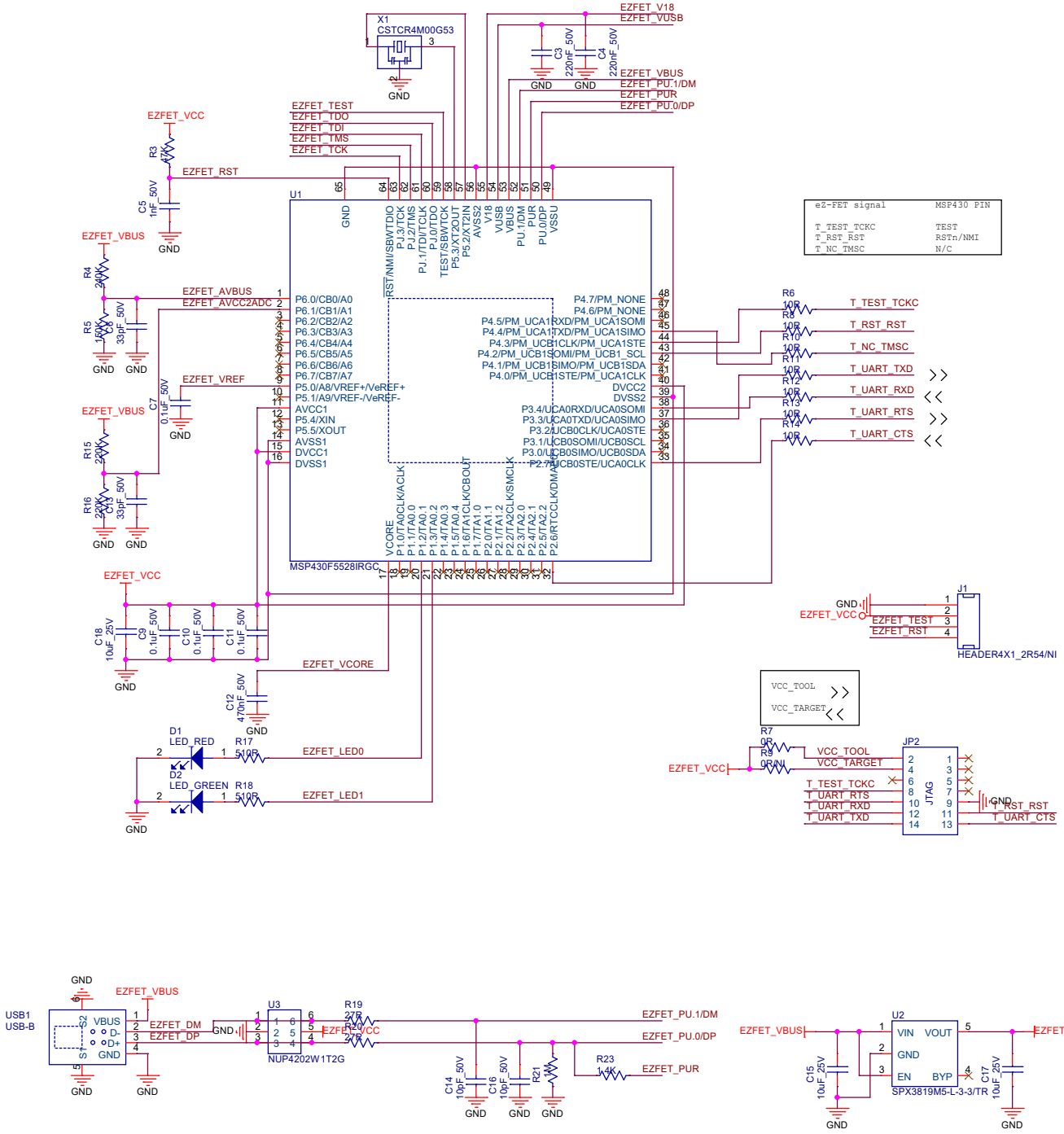
SICHUAN HUIYUAN OPTICAL COMMUNICATIONS CO.,LTD

Title: EZFET_V10A		
Size: A3	Document: 01 COVER	Rev: V10A
Date: Tuesday, March 27, 2018	Sheet 1 of 3	
Designed by: xxxlzjxxx	Checked by: ?	Approved by: ?



5.6.5.1 *JTAG Target Connector*

Figure 12 shows the pinout of the MSP-FET JTAG connector.

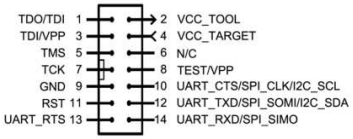


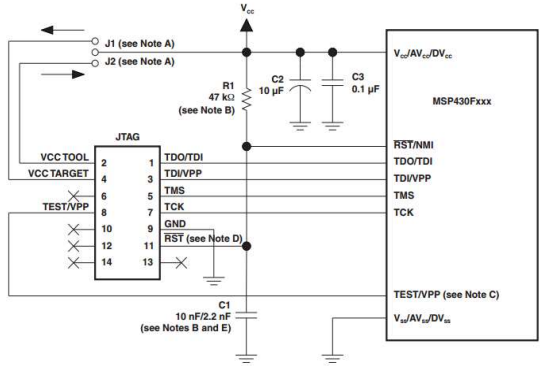
Figure 12. MSP-FET 14-Pin JTAG Connector

5.6.5.2 *MSP-FET Pin States After Power Up*

Table 6 describes the electrical state of every JTAG pin after debug probe power up.

Table 6. MSP-FET Pin States

Pin	Name	After Power up	When JTAG Protocol is Active	When Spy-Bi-Wire Protocol is Active
1	TDO/TDI	Hi-Z, pulled up to 3.3 V	In, TDO	In and Out, SBWTDIO (RST pin)
2	VCC_TOOL	3.3 V	Target V_{CC}	Target V_{CC}
3	TDI/VPP	Hi-Z, pulled up to 3.3 V	Out, TDI	Hi-Z, pulled up to V_{CC}
4	VCC_TARGET	In, external V_{CC} sense	In, external V_{CC} sense	In, external V_{CC} sense
5	TMS	Hi-Z, pulled up to 3.3 V	Out, TMS	Hi-Z, pulled up to V_{CC}
6	N/C	N/C	N/C	N/C
7	TCK	Hi-Z, pulled up to 3.3 V	Out, TCK	Out, SBWTCK
8	TEST/VPP	Out, Ground	Out, TEST	Hi-Z, pulled up to V_{CC}
9	GND	Ground	Ground	Ground
10	UART_CTS/SPI_CLK/I2C_SCL	Hi-Z, pulled up to 3.3 V	Out, Target UART Clear-To-Send Handshake input	Out, Target UART Clear-To-Send Handshake input
11	RST	Out, V_{CC}	Out, RST	Ground
12	UART_TXD/SPI_SOMI/I2C_SDA	Hi-Z, pulled up to 3.3 V	In, Target UART TXD output	In, Target UART TXD output
13	UART_RTS	Hi-Z, pulled up to 3.3 V	In, Target UART Ready-to-Send Handshake output	In, Target UART Ready-to-Send Handshake output
14	UART_RXD/SPI_SIMO	Hi-Z, pulled up to 3.3 V	Out, Target UART RXD input	Out, Target UART RXD input



A 如果使用一个本地目标电源，那么连接 J1。 如果使用调试或编程适配器供电，那么连接 J2。

B 针对RST/NMI 引脚的 R1 和 C1 的配置取决于器件系列。 推荐配置请参阅 MSP430 系列产品用户指南。

C TEST 引脚只在带有复用 JTAG 引脚的 MSP430 系列产品成员上提供。 参见专用器件数据表以确定这个引脚是否可用。

D 当使用只支持 4 线制 JTAG 通信模式的器件并且对器件编程和调试没有要求的时候，到 JTAG 连接器 RST 引脚的连接是可选的。 然而，当在 4 线制 JTAG 模式中使用支持 2 线制 JTAG 通信模式时，此连接是必需的。

E 当在 4 线制 JTAG 模式中使用支持 2 线制 JTAG 通信模式时，C1 的上限不应超过 2.2nF。 这适用于全部两个 TI FET 接口模块 (LPT 和 USB FET)。

图 2-1. 针对 4 线制 JTAG 通信的信号连接

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