Lecture 06 (Instruction Fetch and Dispatch)

1 Instruction Compression

1. Maintain a dictionary for the frequently used sequence of instructions
2. Reduces code size

2 Issue

1. Need to rename registers used by each instruction
2. Different ISAs have different number of physical registers (architectural registers)
3. No separate architectural register file is maintained
4. They map to exactly one physical register at any time

2.1 Rename Stage

1. Register Alias Table (RAT)
2. Free list
3. Rename Table - entry, available bit

2.1.1 RAT

1. Value is updated when write happens to a register
2. 4 instructions are updated in one go
3. Dependency is resolved using a multiplexer

We'll finish the course by minors since "itna samay hai"

3 Dispatch

1. Renamed instructions are sent to instruction window
2. Instruction are made up of
    - valid
    - opcode
    - src tag 1 (imm1)

- ready bit 1 (comes from available bit of rename table initially)
- src tag 2 (imm2)
- ready bit 2
- dest tag

3. Instructions are chosen based on usability and resources available
4. Ready bit is 1 if register is free or can be forwarded
5. After selecting, the register files are read and the they are sent to execute unit

3.1 Wakeup

1. Once producer finishes executing, it broadcasts the tag of destination physical register
2. Each entry in IW marks its source operand as ready if the tag matches

Reminder: Physical registers are write-once, read multiple times