Lecture 28 ()

1 PLSC and Coherence

1. If accesses to a single location preserve program order, then we have no issues
2. However, we might have non-atomic writes because of other addresses
3. Accesses for a single address are atomic

2 Ordering between Accesses to same Variable

(observer is at the core)

1. Read → Read: no difference
2. Write → Read: this may be global since writes might reach later for other cores (since atomicity need not exist)
3. Write → Write: needs to be global
4. Read → Write: this becomes global since writes are ordered

3 Axioms of Coherence

1. Write Serialization: Writes to the same location are globally ordered
2. Write Propagation: A write is eventually seen by all the threads

4 `fence`

1. Store instruction completes when all threads can read the new value
2. Instruction that ensures that all instructions prior to it complete execution
3. It is a memory barrier

5 Execution Witness

1. Parallel Execution → Execution Witness → Sequential Execution
2. If we can create SE that obeys the memory model, then the execution is valid
3. EW is a graph with nodes as instructions

4. Edges can be local and global
5. These edges are happens-before edges (hb)