Lecture 16 (SRAM and CAM)

1 SRAM Array

1.1 SRAM Cell

1. Cross-coupled inverter pair
2. Can be implemented in CMOS as well

1.2 Array

1. Have row address and column address
2. Column is chosen using a mux
3. Row address is used to enable the word line for the entire row

1.2.1 Two Lines

1. We have two outputs BL and BL' for each cell
2. Instead of waiting for the capacitor to charge up, we measure the difference
3. *similar to tarazu - we are that old!*
4. Also helps eliminate noise

1.2.2 Precharging Trick

We precharge both lines to 0.5V

2 CAM Array

2.1 CAM Cell

1. SRAM Cell on top
2. Surrounded by A' and A lines
3. Match line is below SRAM cell
4. T1, T2 in series on left; T3, T4 in series on right
5. When $Q = A$, match line has > 0 voltage

2.2 Array

1. All WLs are set to 1
2. A_i's are set to the tag address
3. Match is set to a non-zero value for all match lines
4. In case of match, a priority encoder will have the correct index

3 CACTI

1. Finds optimal number of banks to have minimal access time, area, power
2. Cuts array into sub-arrays (= bank)

3.1 P-Complete

Given $O(n)$ processors, solve problem in $O(poly(log(n))$

1. DFS
2. Given a circuit, give its output
3. Linear programming