Lecture 20 (On Chip Network)

1 Layout of Memory Chip

1. Checkerboard - core and cache bank alternate
2. Rim layout - cache inside, core outside

2 Router

1. Each node has a router that communicates on its behalf
2. Has a data buffer to send information

2.1 Connection between Routers

1. $D = kl^2$, l is length of wire
2. Delay increases a lot as length increases

2.1.1 Buffered Wires

1. Add buffers to reduce delay
2. For optimal number of buffers, we get minimum delay as $D = 2\sqrt{kdl} - d$, where d is delay of buffer

3 Multi Layer Interconnects

Alternates between horizontal and vertical between different vertical layers

4 Interconnect in Silicon Chips

1. Bus approach - fails trivially
2. Tiling - Network on Chip

4.1 NoC

1. Arrange a set of nodes as tile

2. Router sends and receives all messages for its tile
3. Router also performs forwarding

5 Parameters

5.1 Bisection Bandwidth

1. Number of links that need to be snapped to divide NoC into two equal parts
2. Gives idea of *path diversity*

5.2 Diameter

Maximum optimal distance between any two pair of nodes

Note: Sir knows Delhi roads quite well

6 Topologies

1. Chain
2. Ring
3. Fat tree
4. Mesh
5. Torus
6. Folded torus
7. Hypercube
8. Clos Network

6.1 Hybercube

1. Recursive structure
2. If it has N nodes,
   - diameter = $\sqrt{N}$
   - bisection bandwidth = $N/2$

6.2 Clos Network

1. nr inputs and outputs
2. Inner layer has a $(m \times m)r$ switches
3. Performs a permutation
4. If $m \geq n$, we can reconnect unused input to unused output by rearranging
5. If $m \geq 2n - 1$, we can reconnect without rearrangement

6.2.1 Butterfly Network

Uses only 2×2 switches and $\log(n)$ layers

7 Message Transmission - Hierarchy of Messages Sent

1. Message
2. Packet - head flit, body flits, tail flit
3. Flit - flow control digit (typically 8 or 16 bytes)
4. Phit - physical digit

8 Flow Control

1. We can't drop flits unlike in network transmission
2. Sender needs to have idea about free space at receiver's end

8.1 Credit Based Flow Control

1. Sender (A) maintains an estimate of number of free buffers at receiver (B)
2. If A thinks B has enough free space, only then it sends

8.1.1 Assumptions

1. Routers are clock synchronized
2. Time is measured in number of cycles
3. We first receive a message, process it and add it to buffer
4. Status messages are 1 phit each

8.1.2 Formulation

$$t_D = t_{ph} + t_f + 2t_{pr}$$

$$t_{ph} = \text{ time taken for receiving status message (credit) - phit}$$

$$t_f = \text{ time to send flit}$$

$$t_{pr} = \text{ processing time}$$