Air University
(Final-Term Examination: Spring 2024)

Subject:	**Digital Logic Design**	Total Marks:	**100**
Course Code:	**EE-123**	Date:	**8th June, 2024**
Class:	**BS-CYS**	Time:	**13:30-16:30**
Semester:	**II**	Duration:	**2 Hours**
Section:	**A & B**	FM Name:	**Dr. Bahman R. Alyaei**

HoD Signatures:_____ FM Signatures:_____

Note:

- **This is closed book exam, All questions must be attempted.**
- **This examination carries 45% weight towards the final grade.**
- **Calculators are not allowed**

	Q. No. 1 (CLO 3)	**25 Marks**
a	For the following Boolean expressions **Draw** the logic circuit diagram using appropriate logic gates: 1) $X = A(BC)$. 2) $Y = (A + B)C$.	10
b	Apply the rules of Boolean Algebra to **Evaluate** the standard POS expression for the following digital system. $Z = (A + B + \bar{C})(A + C)$	5
c	**Apply** the method of **Numerical Expansion** to generate the Standard SOP form of the following Boolen Expression. $M = \bar{A} + A\bar{B} + ABC$	5
d	Using rules of Boolean Algebra, **Express** the equation of the following digital system in minimum form. $N = A + AB + \overline{(A + AB)}C$	5
	Q. No. 2 (CLO 3)	**30 Marks**
a	For the truth table shown, **Evaluate** the following: **(i)** The standard SOP expression of the output variable. **(ii)** The standard POS expression of the output variable. **(iii)** The simplified SOP expression of the output variable using K-Map.	5+5+10
b	For the non-standard Boolean expression given below, **Generate** the truth table. $X = \bar{A} + AB$	10

Inputs			**Output**
A	***B***	***C***	***X***
0	0	0	1
0	0	1	x
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	x
1	1	0	0
1	1	1	1

	Q. No. 3 (CLO 4)	25 Marks
a	Using the method of Truth Table and word comparison **(not bit by bit method)**, **Design** the two bit word comparator that produces the following output: 1) Equal. 2) Greater than or equal. 3) Less than or equal. **Note: Strict greater and less is not required.**	5+10+10
	Q. No. 4 (CLO 4)	**10 Marks**
a	**Design** the following digital systems using block level design method. 1) Four bit adder using the blocks Full-Adder. 2) Four bit Multiplier using blocks of 4-bit adders and necessary logic gates.	5+5
	Q. No. 5 (CLO 4)	**10 Marks**
a	**Design** the following digital systems using appropriate MUX blocks. 1) Using appropriate Multiplexer (MUX) block, design the following digital system. $Y = \overline{A_2}A_1A_0 + A_2\overline{A_1}A_0 + A_2A_1\overline{A_0}$ 2) Using 8×1 MUX with Enable (EN) input and necessary logic gates, implement 16×1 MUX.	5+5

********** End of Question Paper **********