# Air University
## Final Term Examination: Fall, 2022

Student ID: 211132
Marks: 100
Max. Time Allowed (03 Hrs)
Date: 4th Jan, 2023
Time: 13:00-16:00

Subject: Digital Logic Design
Course Code: EE223
Class: BSCYS-F-21-A
Semester: Fall 22
FM: Maria Tahir

FM Signature:

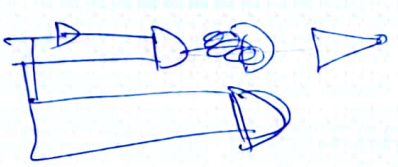
*The Question Paper Needs To Be Returned With the Answer Sheet*

**Key instructions for Students:**

1. This is a **closed book/closed notes** examination.
2. Calculators **are allowed.**
3. Solve each question with **proper logic and explanation.** You will **not get any credits** for directly written answers.
4. **Draw properly** labeled graphs/schematics and block diagrams, where necessary.
5. In case of any confusion, **employ appropriate assumptions** and solve the question. Justify assumptions, if any.
6. **Be legible and logical.**

**Course Learning Outcomes**

| CLO# | Statement | PLOs | Learning Domain & Level |
|---|---|---|---|
| CLO1 | **Understand** the fundamental concepts of digital logic design including basic and universal gates, number systems, and binary coded systems, basic components of combinational and sequential circuits. | PLO1 | C2 |
| CLO2 | **Explain** the basic techniques of digital electronic circuits design including Boolean algebra and multi-variable Karnaugh map. | PLO2 | C2 |
| CLO3 | **Illustrate** the working of small-scale combinational and sequential digital circuits. | PLO2 | C3 |
| CLO4 | **Interpret real-world problems** and solve those using small-scale combinational and synchronous sequential digital circuits. | PLO3 | C1 |



## Question 01

CLO3: 10+05+10 = 25

A digital circuit is designed using AND-OR logic having four input variables (A-MSB, B, C, and D-LSB). The circuit operates so that it passes HIGH output only when any of the two or three inputs are HIGH, LOW otherwise. Your task is to:

a. ***Analyze*** the truth table showing the respective output to each input combination.
b. Find out the Standard Boolean Expression and minimize it using K-map.
c. Draw the logic circuit reflecting the minimized expression obtained in part 'b'.

## Question 02

CLO4: 05+05+10+10 = 30

A data acquisition system is used to collect the data from three motion sensors, which are installed in a room. While sending the data, all three sensors coordinate so that every time a sensor detects a motion, it sends a HIGH signal and the other two sensors transmit LOW even if they do not sense any motion simultaneously. Sometimes two or maybe all three detect the motions simultaneously and transmit a HIGH signal toward three input lines of the data acquisition card. The data acquisition system has to decode the data into eight different outputs to detect a specific combination of sensor's transmission. Keeping this logic in mind:

a. ***Design*** a 3-to-8-line basic decoder logic, which is responsible to decode the data in each possible input combination from sensors.
b. What would be each decoder output ($D_0$-$D_7$) if the input combinations are as shown in *Table 1*?
c. Design the logic Circuitry for The Full adder. Illustrate the difference between the Ripple carry adder and the Look ahead carry adder.
d. A user wants to control the device that bombards by using a specific range of frequencies by comparing the Inputs. Design the Combinational logic circuit.

*Table 1 (do not give your answer here)*

| *Sensor 1* | *Sensor 2* | *Sensor 3* | *$D_0$-$D_7$* |
|---|---|---|---|
| 1 | 0 | 0 | ? |
| 0 | 1 | 1 | ? |
| 0 | 1 | 0 | ? |
| 1 | 1 | 1 | ? |
| 0 | 0 | 1 | ? |

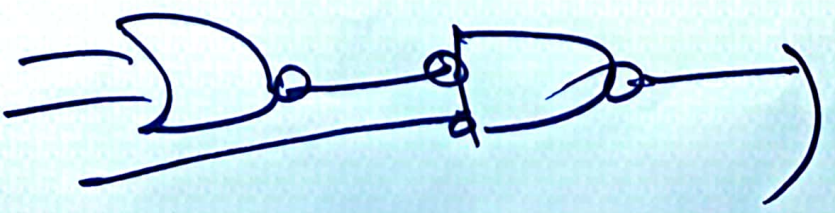
## Question 03

CLO2: 05+05+05 = 15

For the NOR logic shown below:

$$\overline{\overline{A+B+C}+\overline{D+E+F}}$$

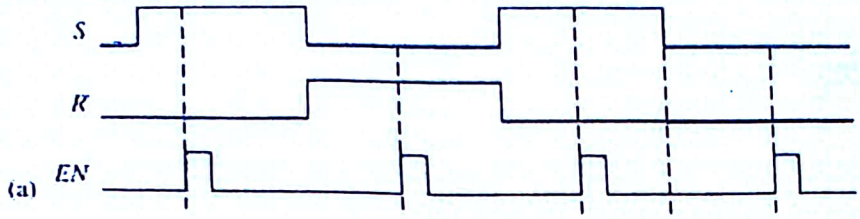
a. ***Transform*** the Boolean equation given above into a logic diagram having NOR gates only.
b. Using appropriate dual symbols, redraw the logic diagram drawn in part 'a' and develop the output expression.
c. Prove that the output of the NOR circuit in part 'a' is the same as for the circuit in part 'b'.



**Question N0: 04** CLO4: 10+5+10+5 = 30

a) Design the Three modes of Basic Set Reset Latch operations.

b) Determine the Q output waveform if the inputs shown in Figure are applied to a gated S-R latch that is initially RESET.




c) Differentiate Edge triggered S-R Flip-Flop and J-K Flip-Flop (Draw Sequential Circuits and Truth Table).

d) Construct positive Edge Triggered D Flip-Flops

END OF EXAM.