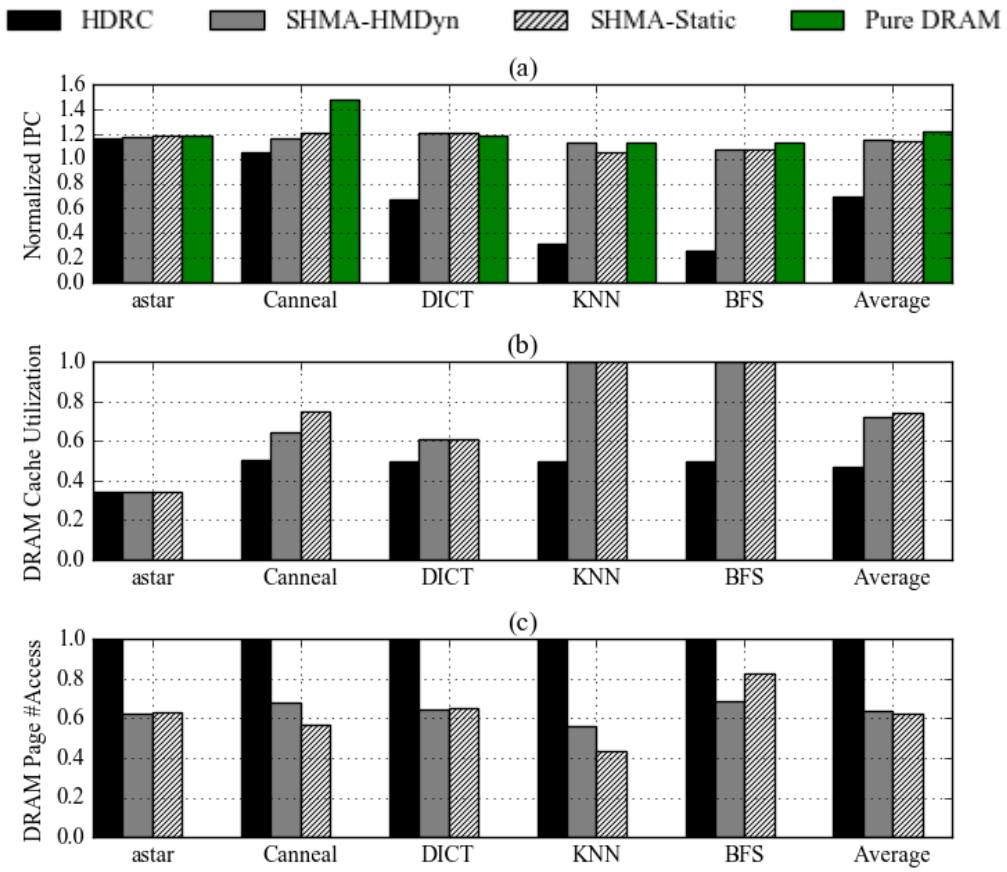

Fig. 1: (a) Instruction per cycle normalized to a system with 32GB PCM, without DRAM cache, (b) DRAM Cache Utilization and (c) average access frequency of every DRAM cache page, normalized to HDRC

app	4GHz, 4 cores configuration (Normalized IPC)			2GHz, 32 cores configuration (Normalized IPC)		
	HDRC	SHMA-HMDyn	SHMA-Static	HDRC	SHMA-HMDyn	SHMA-Static
astar	1.30	1.30	1.33	1.17	1.18	1.18
Canneal	0.96	1.27	1.34	1.05	1.16	1.20
DICT	0.58	1.34	1.34	0.67	1.21	1.21
KNN	0.23	1.23	1.08	0.31	1.13	1.05
BFS	0.22	1.34	1.36	0.25	1.07	1.08

We repeat part of the experiment with 2GHz, 32 cores configuration. Experimental results are shown in Figure 1. Figure 1(a) depicts the nomalized performance of HDRC, SHMA-HMDyn, SHMA-Static and a system with 32GB DRAM only, a system with 32GB PCM is the baseline. For all these applications, HDRC only reaches 69.1% performance of the baseline, SHMA-HMDyn, SHMA-Static and a system with 32GB DRAM(the performance upper bound) achieve 15.0%, 14.7% and 22.3% performance improvement on average. Compared to HDRC, SHMA-Static and SHM-HMDyn exhibit 45.9% and 45.6% performance

improvement respectively. Just selecting part of workloads has resulted in lower performance improvement that isn’t as remarkable as our thesis.