

KF70 Steve Haynal

#### SofterHardware

Sheet: /Power and FPGA/

File: Power.sch

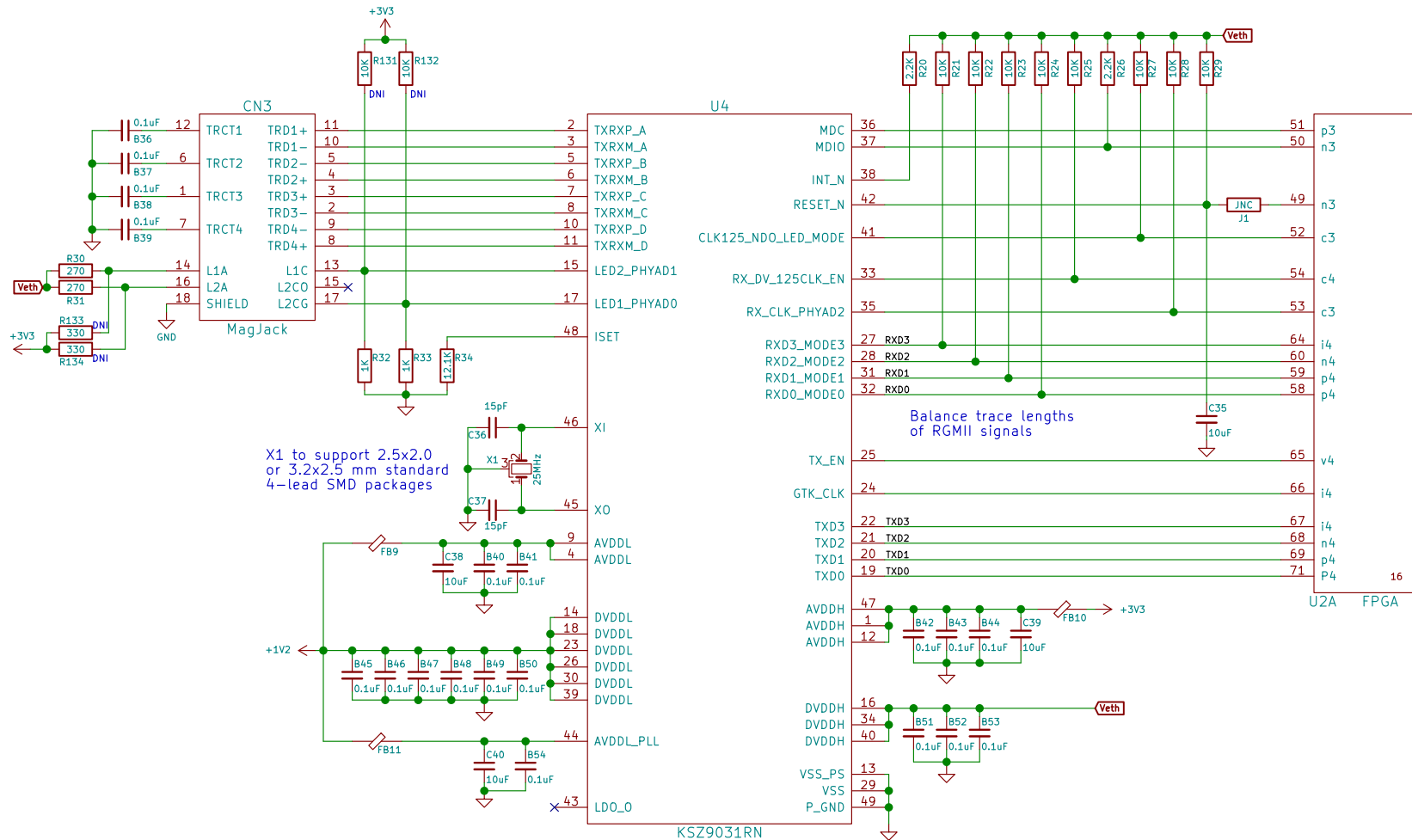
#### Title: Power

Size: USLetter Date: 2017-06-18

KiCad E.D.A. kicad 4.0.6

Rev: 2.0-beta3

Id: 2/7



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Sheet: /Ethernet/

File: Ethernet.sch

**Title: Ethernet**

Size: USLetter Date: 2017-06-18

KiCad E.D.A. kicad 4.0.6

Rev: 2.0-beta3

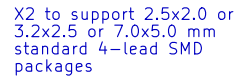
Id: 3/7

Default Versa with oscillator: Include FB12,C41,B56,B57,X2, Include R36,R38 if required by oscillator. Exclude B55,R35,R37,U5,J3,J4,C42.  
Versa with VCO: Include FB12,C41,B56,B57,X2,U5,R35,R37,B55. Exclude R36,R38,J4,J3,C42.  
Versa with crystal: Include X2 as crystal, B57,J4,J3 as jumper, C42,R38 as 15pF. Exclude FB12,C41,B56,U5,R35,R36,R37,B55.

No Versa but oscillator to AD9866: Exclude all Versa components, build for oscillator, connect WJ3 to WJ1.

No Versa but external clock to AD9866: Exclude all Versa components and oscillator components. Wire from WJ2 to WJ1.

See RF Frontend sheet for additional AD9866 clock options



Synchronized radio external clock:

Include CL1,B58,R39.

Exclude J23,J25.

Synchronized radio recovered clock:

Include J23,J5.

Adjust R39,R40.  
Optional: C14,R50



Output for synchronized radio: Include R45,CL2.

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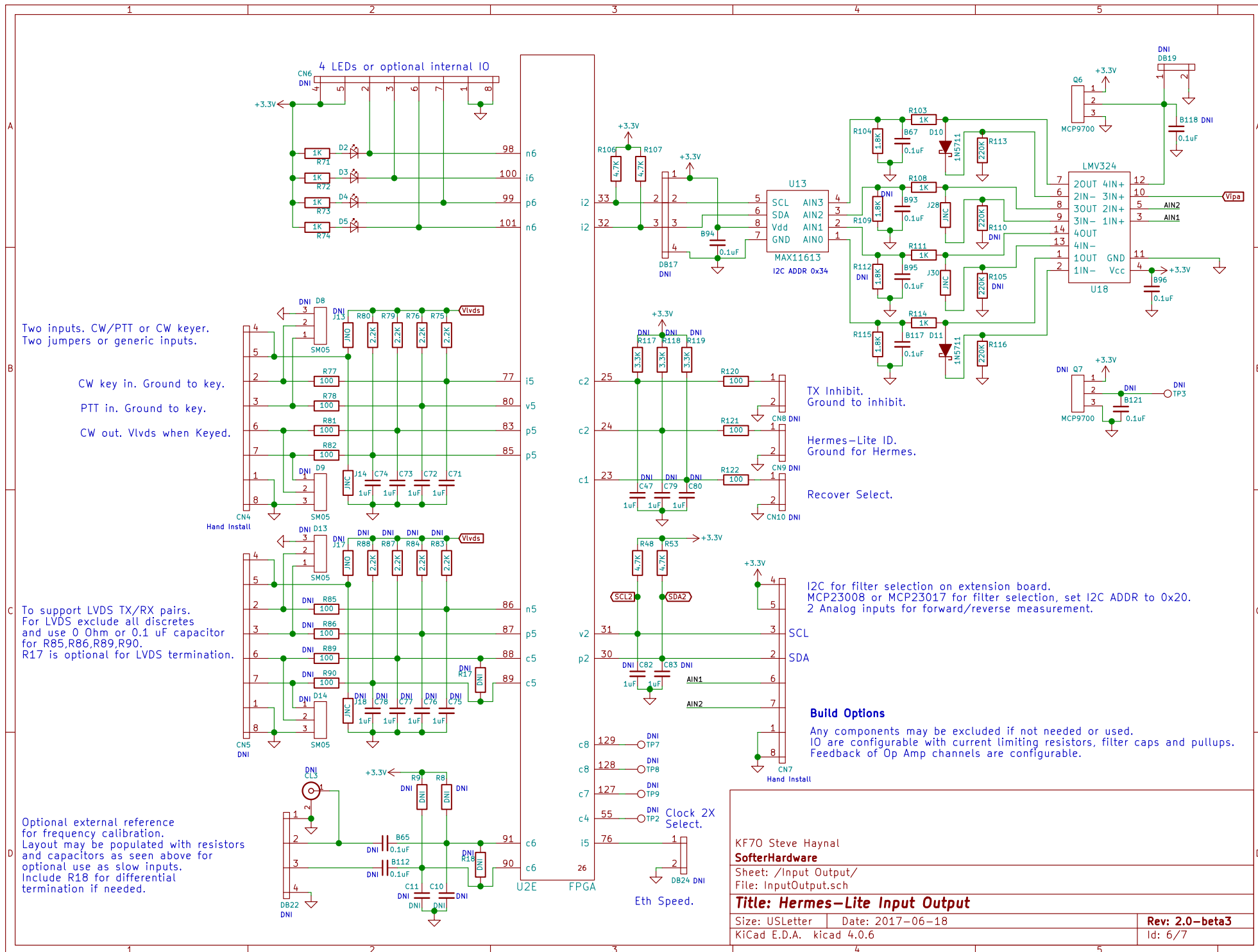
File: Clock.sch

**Title:** Clock

Size: 352x64	Date: 1/1/2025
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Id: 4/7





All values are first-cut place holders. To be refined with simulation and experimentation.

#### Build Options

Any or all components may be excluded if PA is unused.

SOT-89 or TO-220 LDMOS supported on main circuit board.  
TO-220 mounts to side of enclosure.  
SOT-89 dissipates heat to PCB and side of enclosure.

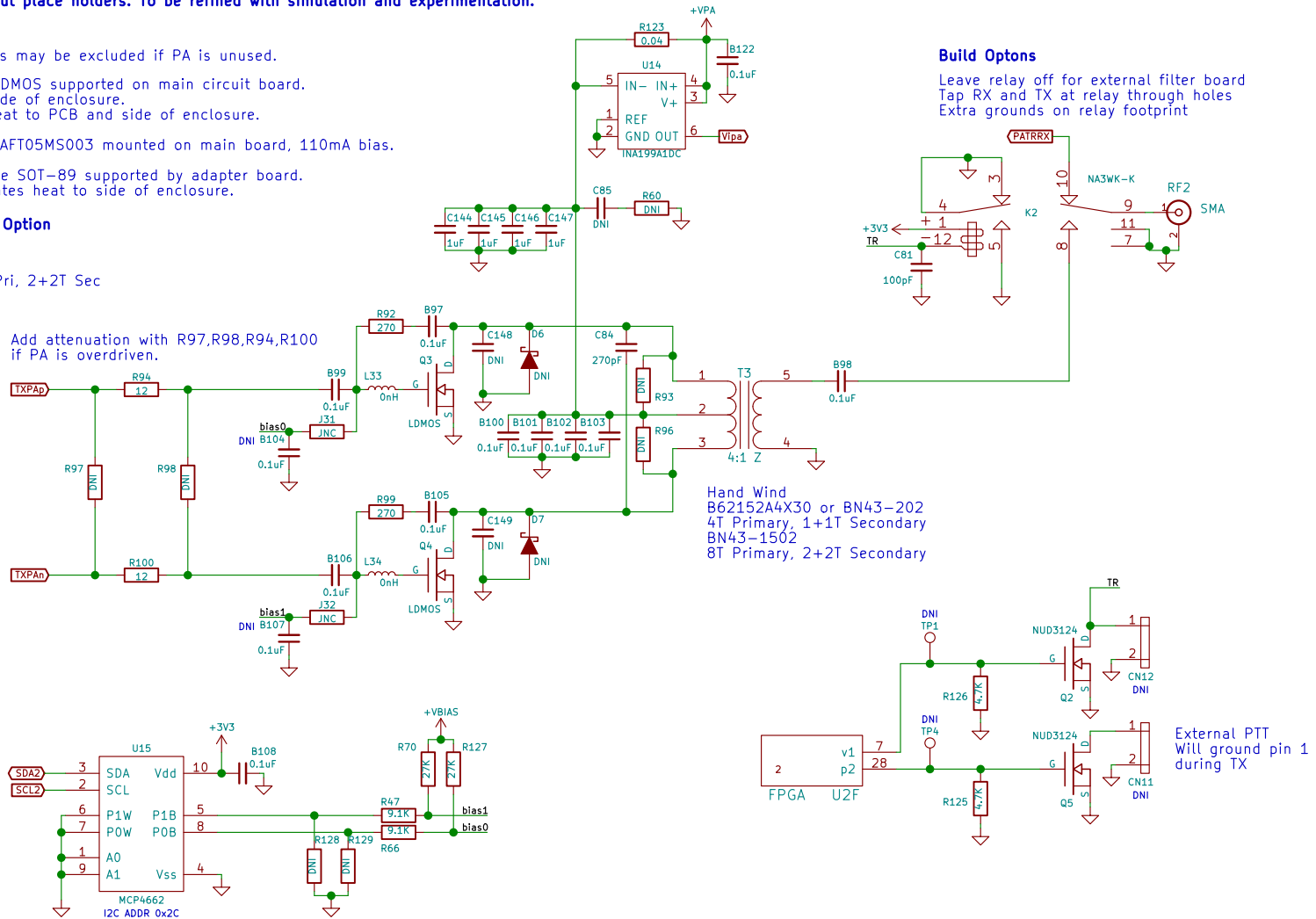
Deafault build uses 2 AFT05MS003 mounted on main board, 110mA bias.

PLD-1.5 and alternate SOT-89 supported by adapter board.  
Adapter board dissipates heat to side of enclosure.

#### RD15HVF1 Test Build Option

L33,L34 = 4.7 Ohm  
R92,R99 = 500 Ohm  
T3 = BN61-202 4T Pri, 2+2T Sec  
200 mA bias

Add attenuation with R97,R98,R94,R100  
if PA is overdriven.



R101,R95,R47,R66 set for AFT05MS003. Bias voltage ranges from 2.5 to 3.5V.  
Set R101,R95 to 7.5K, R47,R66 to 3.3K for bias voltage range from 3.1 to 5.3V.

Design based on work by Claudio IN30TD/DK1CG, John W9JSW, and other LDMOS/MOSFET QRP PA designs

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Sheet: /PA/

File: PA.sch

**Title: Hermes-Lite V2 5W Power Amplifier**

Size: USLetter Date: 2017-06-18

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Rev: 2.0-beta3

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