Power and FPGA

Power.sch

Ethernet

Ethernet.sch

Clock

Clock.sch

RF Frontend

RFFrontend.sch

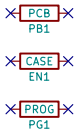
Input Output

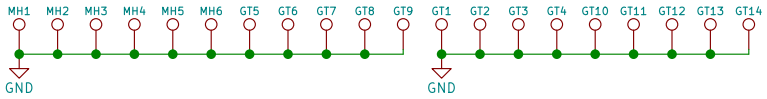
InputOutput.sch

PA

PA.sch

Do Not Include (DNI) any components
on this page fo assembly





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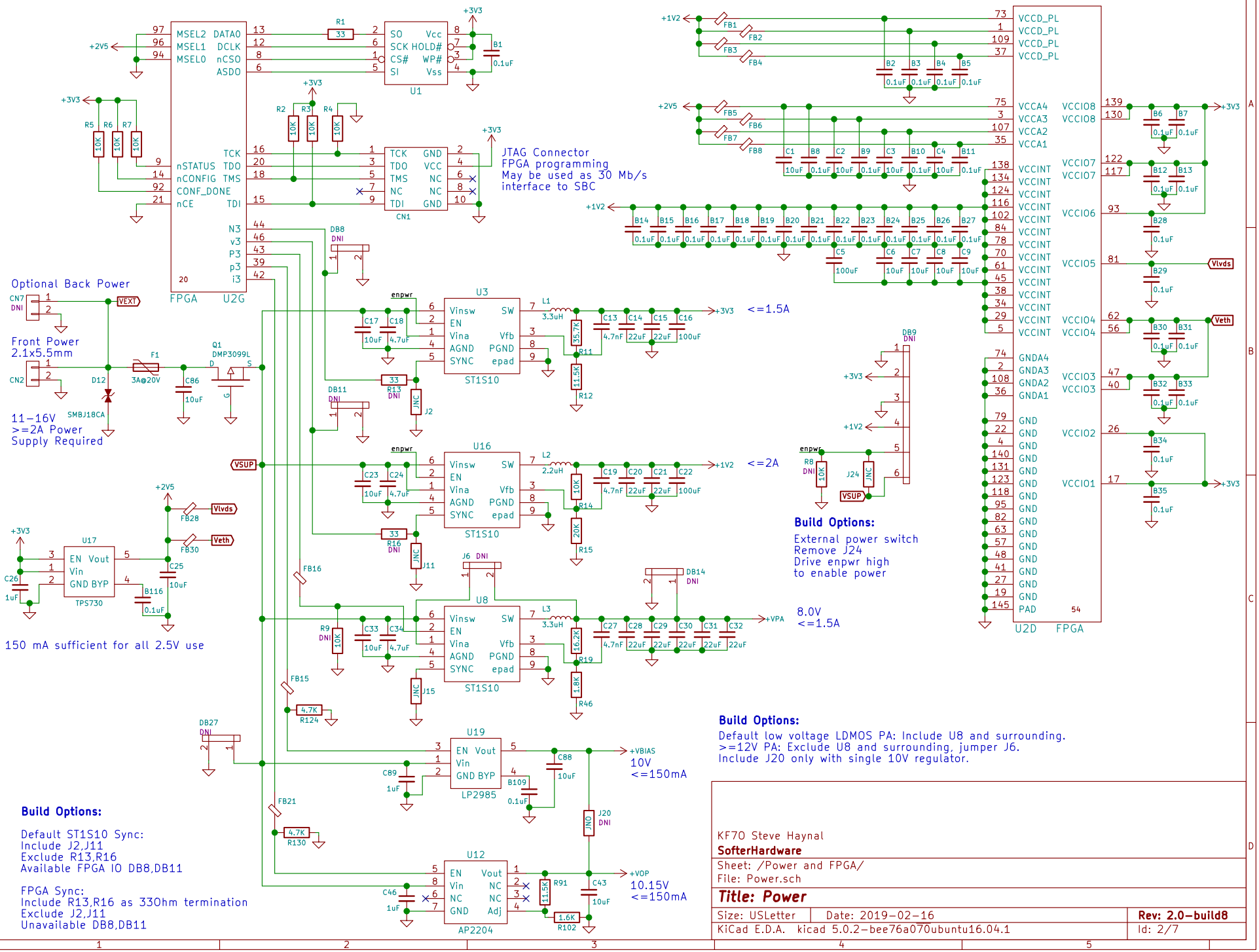
Sheet: /
File: hermeslite.sch

Title: Hermes-Lite

Size: USLetter	Date: 2019-02-16	**Rev: 2.0-build8**
KiCad E.D.A. kicad 5.0.2-bee76a070ubuntu16.04.1		Id: 1/7


JTAG Connector
FPGA programming
May be used as 30 Mb/s
interface to SBC
Optional Back Power
Front Power
2.1x5.5mm
11–16V
>=2A Power
Supply Required
<=1.5A
<=2A
8.0V
<=1.5A
Build Options:
External power switch
Remove J24
Drive enpwr high
to enable power
150 mA sufficient for all 2.5V use
Build Options:
Default low voltage LDMOS PA: Include U8 and surrounding.
>=12V PA: Exclude U8 and surrounding, jumper J6.
Include J20 only with single 10V regulator.
Build Options:
Default ST1S10 Sync:
Include J2,J11
Exclude R13,R16
Available FPGA IO DB8,DB11
FPGA Sync:
Include R13,R16 as 33Ohm termination
Exclude J2,J11
Unavailable DB8,DB11
+VBIAS
10V
<=150mA
+VOP
10.15V
<=150mA
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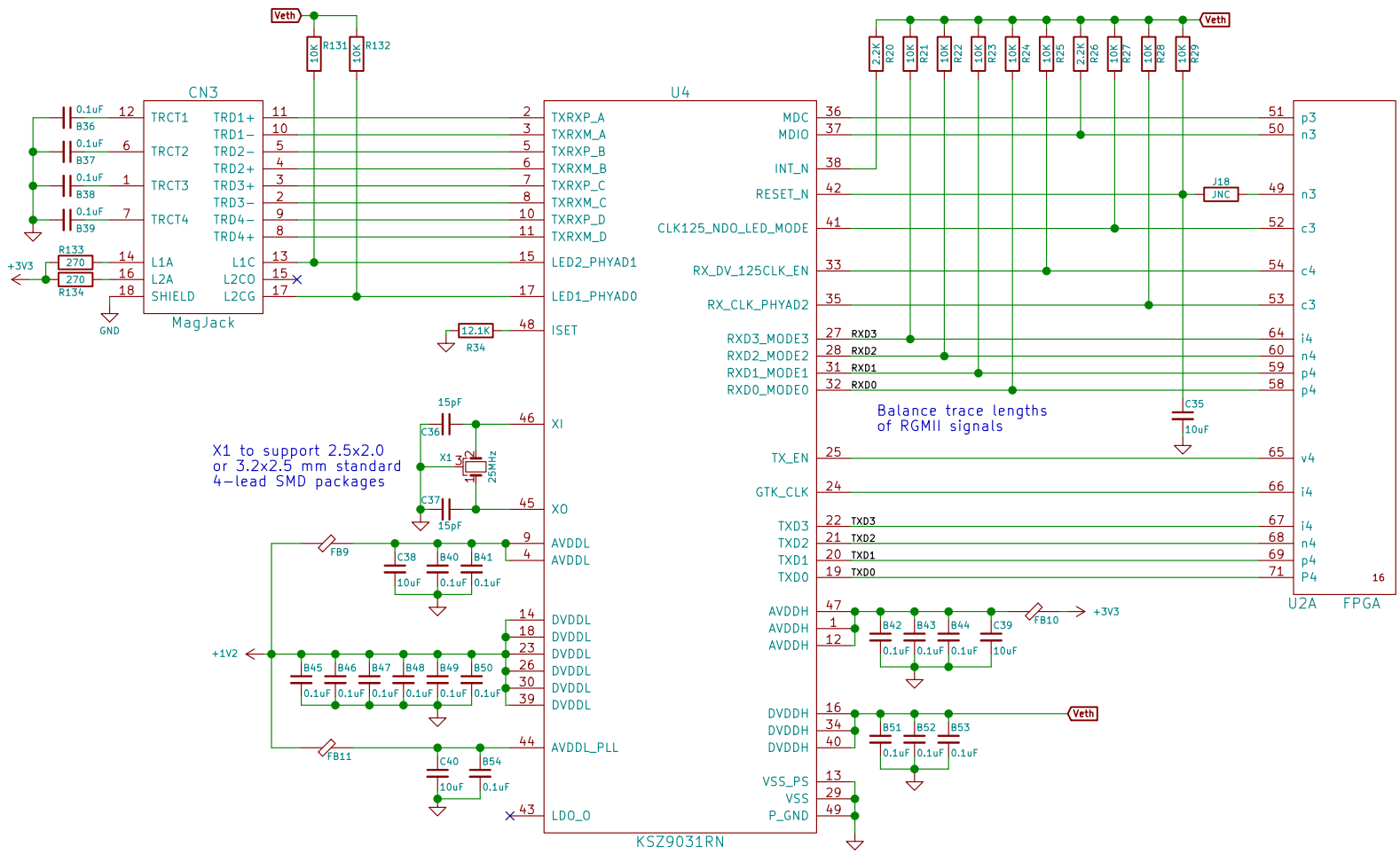
Sheet: /Power and FPGA/
File: Power.sch
Title: Power
Size: USLetter
Date: 2019-02-16
Rev: 2.0-build8
KiCad E.D.A. kicad 5.0.2-bee76a070ubuntu16.04.1
Id: 2/7



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Sheet: /Ethernet/	
File: Ethernet.sch	
Title: Ethernet	
Size: USLetter | Date: 2019-02-16	**Rev: 2.0-build8**
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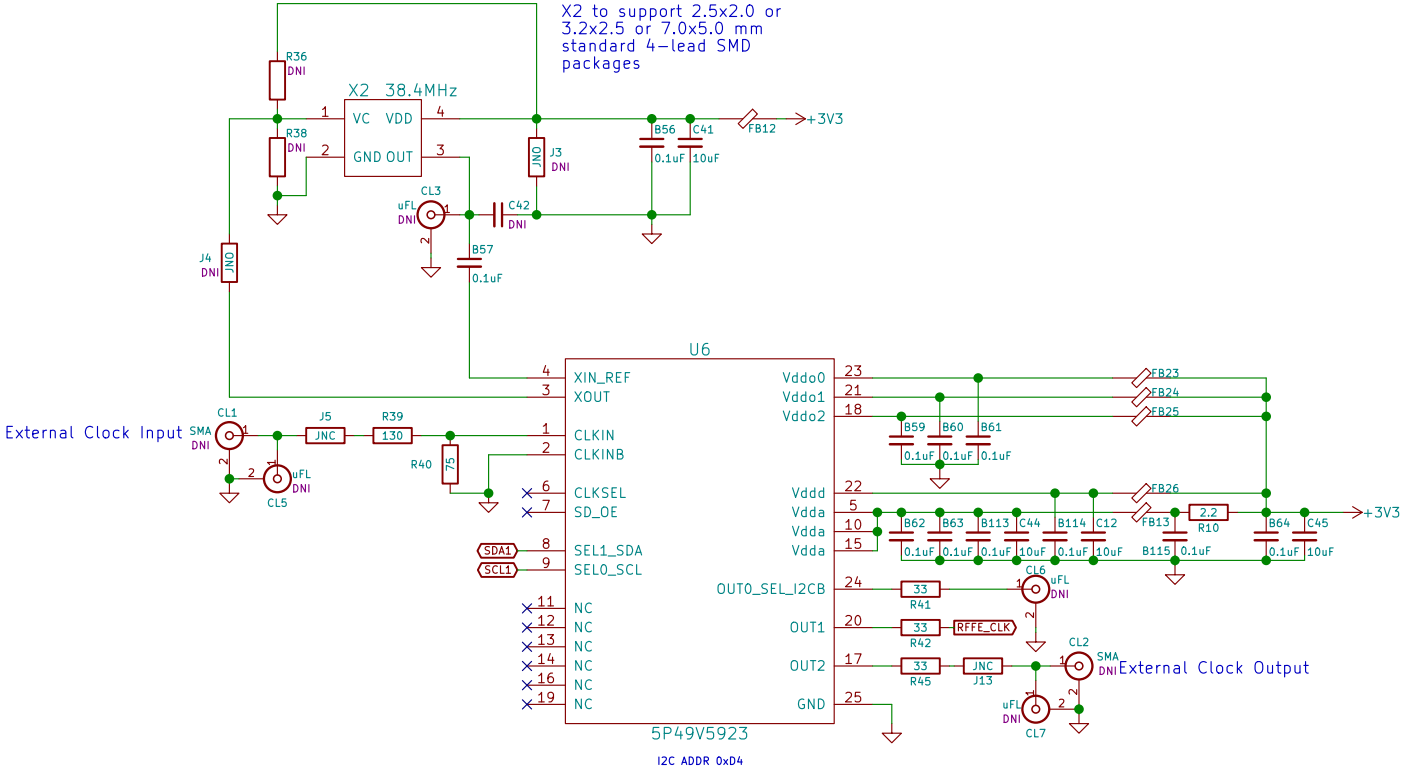
Build Options:

Default Versa with oscillator: Include FB12,C41,B56,B57,X2. Include R36,R38 if required by oscillator. Exclude J3,J4,C42.
Versa with crystal: Include X2 as crystal, B57,J4,J3 as jumper, C42,R38 as 15pF. Exclude FB12,C41,B56,R36.
External clock: Configure U6 for CLKIN input and correct ratio, drive CL1 or CL5 with external clock.
Other experimental options possible with uFL connectors. See RF Frontend sheet for additional AD9866 clock options.



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Sheet: /Clock/
File: Clock.sch

Title: Clock

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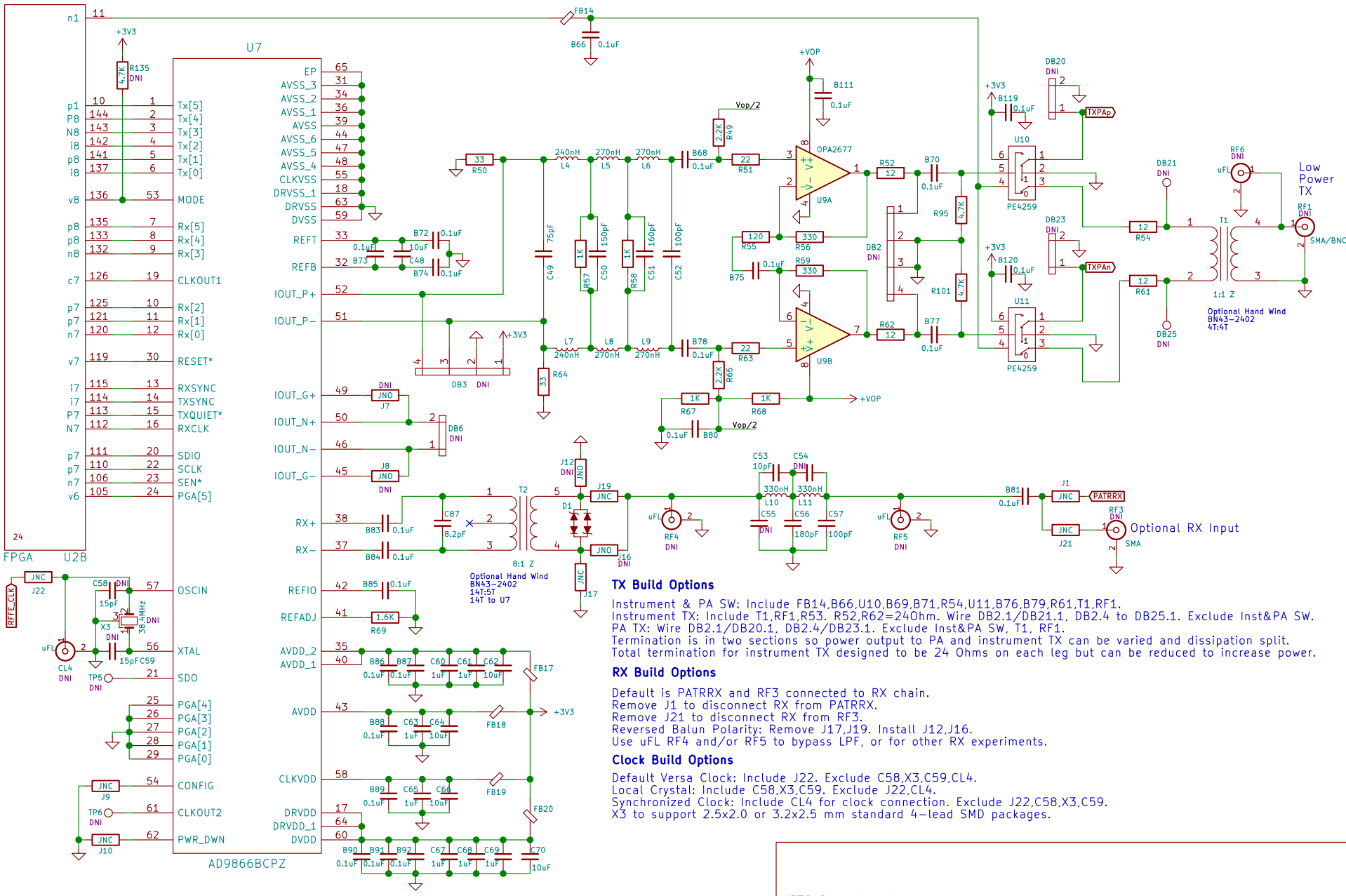

TX Build Options

Instrument & PA SW: Include FB14,B66,U10,B69,B71,R54,U11,B76,B79,R61,T1,RF1.
Instrument TX: Include T1,RF1,R53. R52,R62=240hm. Wire DB2.1/DB21.1, DB2.4 to DB25.1. Exclude Inst&PA SW.
PA TX: Wire DB2.1/DB20.1, DB2.4/DB23.1. Exclude Inst&PA SW, T1, RF1.
Termination is in two sections so power output to PA and instrument TX can be varied and dissipation split.
Total termination for instrument TX designed to be 24 Ohms on each leg but can be reduced to increase power.

RX Build Options

Default is PATRRX and RF3 connected to RX chain.
Remove J1 to disconnect RX from PATRRX.
Remove J21 to disconnect RX from RF3.
Reversed Balun Polarity: Remove J17,J19. Install J12,J16.
Use uFL RF4 and/or RF5 to bypass LPF, or for other RX experiments.

Clock Build Options

Default Versa Clock: Include J22. Exclude C58,X3,C59,CL4.
Local Crystal: Include C58,X3,C59. Exclude J22,CL4.
Synchronized Clock: Include CL4 for clock connection. Exclude J22,C58,X3,C59.
X3 to support 2.5x2.0 or 3.2x2.5 mm standard 4-lead SMD packages.

Expected User Install for Standard Build

Only if no companion card and desired by user:
RF1 RF3

Op Amp Design by Jim N2ADR
TX Filter Design by Claudio IN3OTD/DK1CG
RX Filter Design by Andrew G4XZL

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Sheet: /RF Frontend/
File: RFFrontend.sch

Title: RF Frontend

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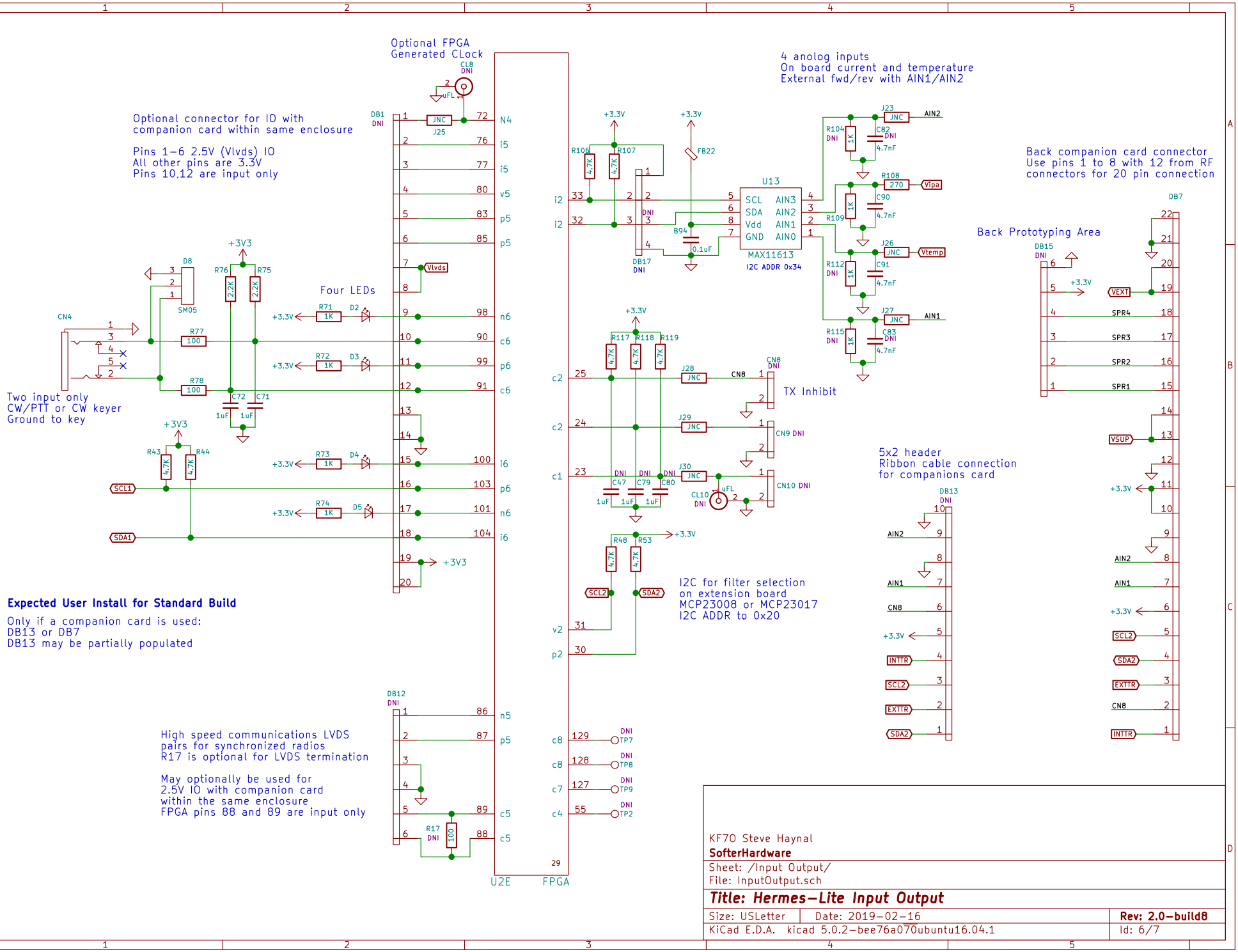
Optional FPGA
Generated CLock
CL8
DNI
uFL
Optional connector for IO with
companion card within same enclosure
Pins 1-6 2.5V (Vlvds) IO
All other pins are 3.3V
Pins 10,12 are input only
DB1
DNI
JNC
J25
Four LEDs
+3V3
D8
SM05
CN4
R76
R75
2.2K
R77
100
R78
100
C72
C71
1uF
R71
R72
R73
R74
1K
D2
D3
D4
D5
R43
R44
4.7K
SCL1
SDA1
Vlvds
Two input only
CW/PTT or CW keyer
Ground to key
Expected User Install for Standard Build
Only if a companion card is used:
DB13 or DB7
DB13 may be partially populated
High speed communications LVDS
pairs for synchronized radios
R17 is optional for LVDS termination
May optionally be used for
2.5V IO with companion card
within the same enclosure
FPGA pins 88 and 89 are input only
DB12
R17
100
U2E
FPGA
4 anolog inputs
On board current and temperature
External fwd/rev with AIN1/AIN2
R106
R107
FB22
U13
SCL
SDA
Vdd
GND
AIN3
AIN2
AIN1
AIN0
MAX11613
I2C ADDR 0x34
B94
0.1uF
DB17
R104
R109
R112
R115
C82
C90
C91
C83
4.7nF
R108
270
Vipa
Vtemp
AIN2
AIN1
J23
J26
J27
TX Inhibit
R117
R118
R119
J28
J29
J30
CN8
CN9 DNI
CN10 DNI
C47
C79
C80
CL10
R48
R53
SCL2
SDA2
I2C for filter selection
on extension board
MCP23008 or MCP23017
I2C ADDR to 0x20
TP7
TP8
TP9
TP2
Back companion card connector
Use pins 1 to 8 with 12 from RF
connectors for 20 pin connection
Back Prototyping Area
DB15
DB7
VEXT
VSUP
SPR4
SPR3
SPR2
SPR1
5x2 header
Ribbon cable connection
for companions card
DB13
INTTR
EXTTR
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Sheet: /Input Output/
File: InputOutput.sch
Title: Hermes-Lite Input Output
Size: USLetter
Date: 2019-02-16
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Build Optons

Any or all components may be excluded if PA is unused.

SOT-89 or TO-220 LDMOS supported on main circuit board
TO-220 mounts to side of enclosure
SOT-89 dissipates heat to PCB and side of enclosure

Deafult build uses 2 AFT05MS003 mounted on main board, 110mA bias

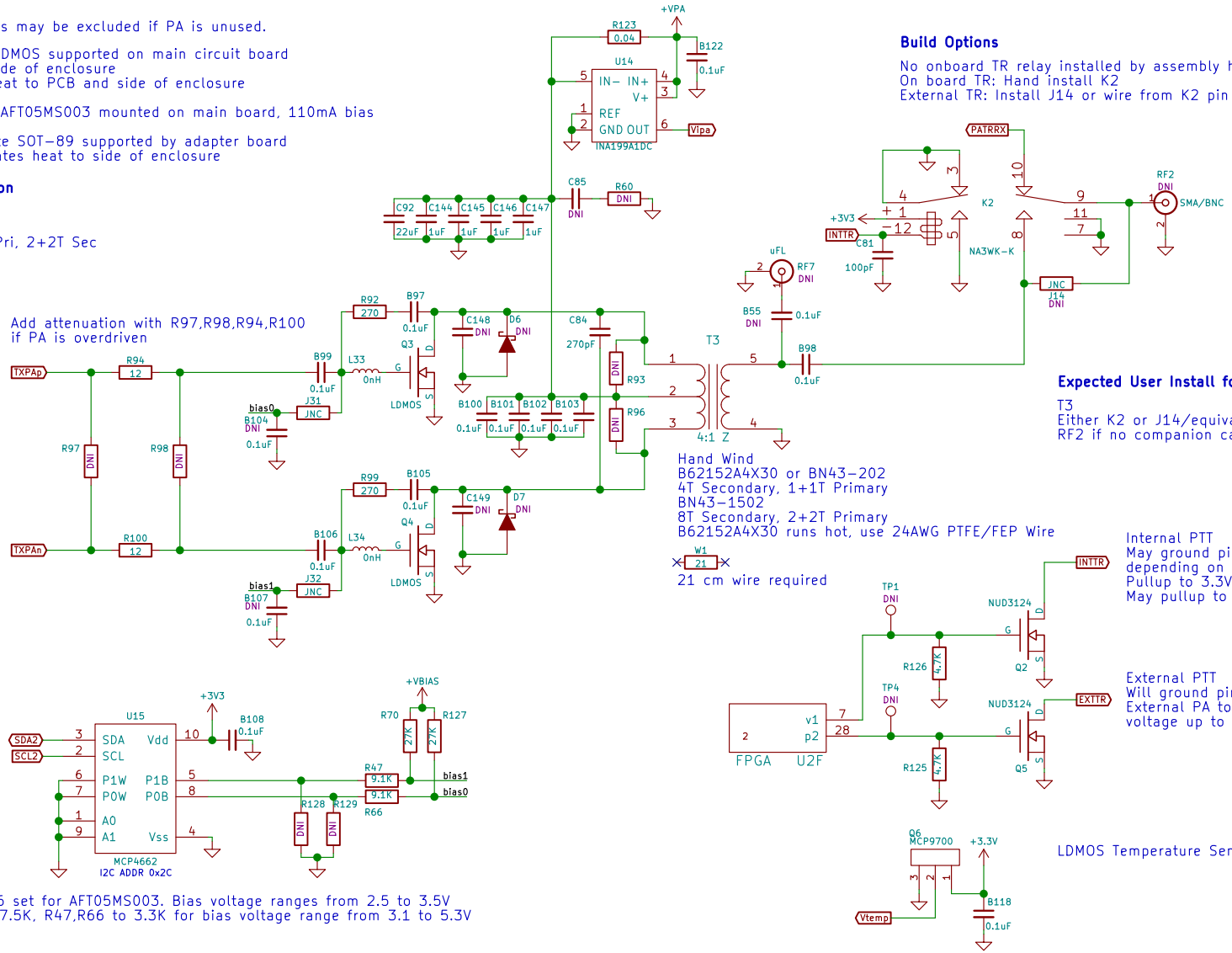
PLD-1.5 and alternate SOT-89 supported by adapter board
Adapter board dissipates heat to side of enclosure

RD15HVF1 Build Option

L33,L34 = 4.7 Ohm
R92,R99 = 500 Ohm
T3 = BN61-202 4T Pri, 2+2T Sec
200 mA bias

Build Options

No onboard TR relay installed by assembly house
On board TR: Hand install K2
External TR: Install J14 or wire from K2 pin 8 to pin 9



R127,R70,R47,R66 set for AFT05MS003. Bias voltage ranges from 2.5 to 3.5V
Set R127,R70 to 7.5K, R47,R66 to 3.3K for bias voltage range from 3.1 to 5.3V

Design based on work by Claudio IN3OTD/DK1CG, John W9JSW, and other LDMOS/MOSFET QRP PA designs

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Sheet: /PA/
File: PA.sch

Title: Hermes-Lite V2 5W Power Amplifier

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