Power and FPGA

Power.sch

Ethernet

Ethernet.sch

Clock

Clock.sch

RF Frontend

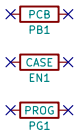
RFFrontend.sch

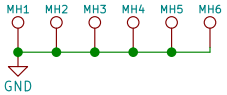
Input Output

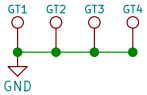
InputOutput.sch

PA

PA.sch







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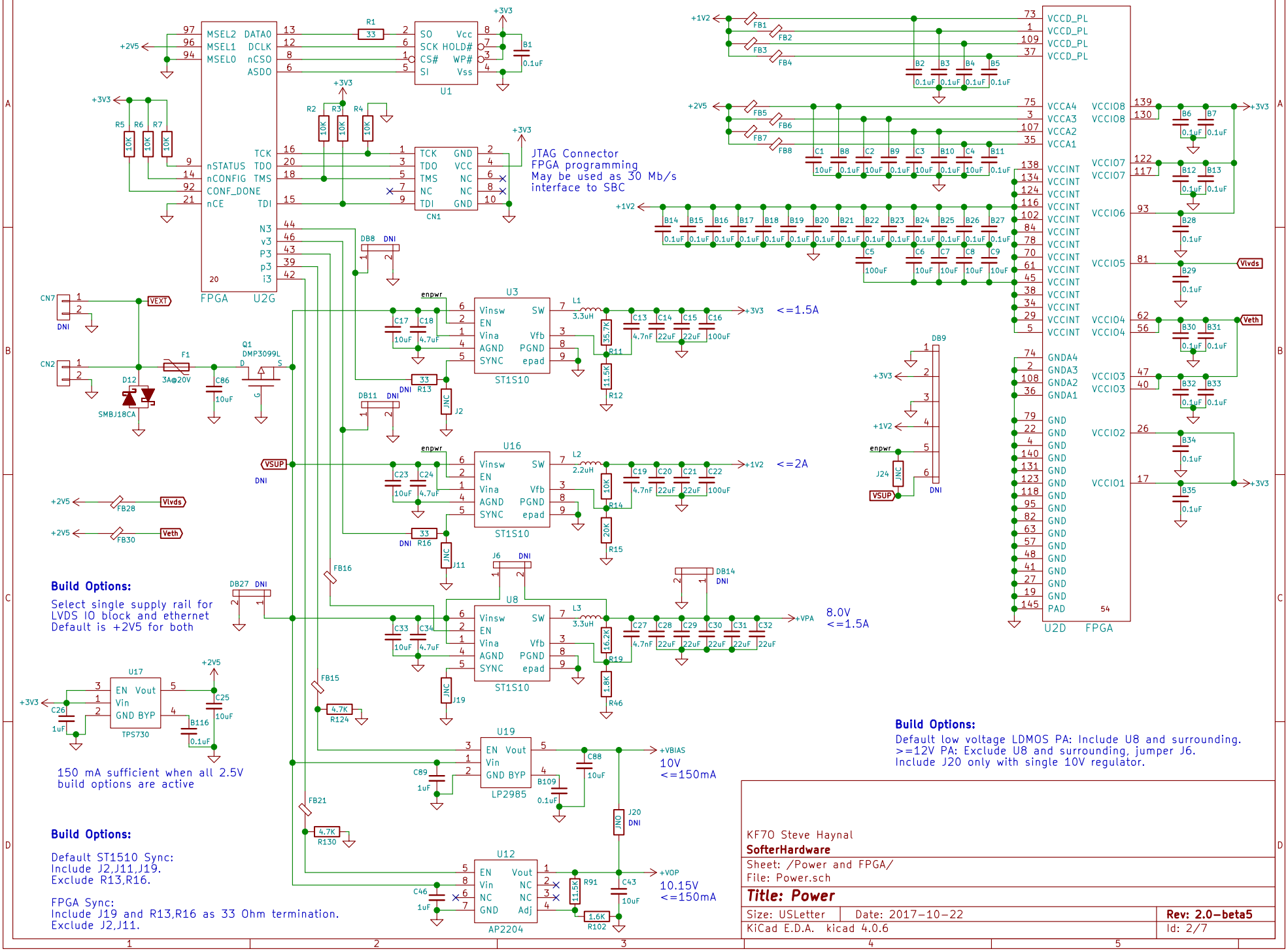
Sheet: /
File: hermeslite.sch

Title: Hermes-Lite

Size: USLetter	Date: 2017-10-22	**Rev: 2.0-beta5**
KiCad E.D.A. kicad 4.0.6		Id: 1/7


JTAG Connector
FPGA programming
May be used as 30 Mb/s
interface to SBC
<=1.5A
<=2A
8.0V
<=1.5A
10V
<=150mA
10.15V
<=150mA
150 mA sufficient when all 2.5V
build options are active
Build Options:
Select single supply rail for
LVDS IO block and ethernet
Default is +2V5 for both
Build Options:
Default ST1510 Sync:
Include J2,J11,J19.
Exclude R13,R16.
FPGA Sync:
Include J19 and R13,R16 as 33 Ohm termination.
Exclude J2,J11.
Build Options:
Default low voltage LDMOS PA: Include U8 and surrounding.
>=12V PA: Exclude U8 and surrounding, jumper J6.
Include J20 only with single 10V regulator.
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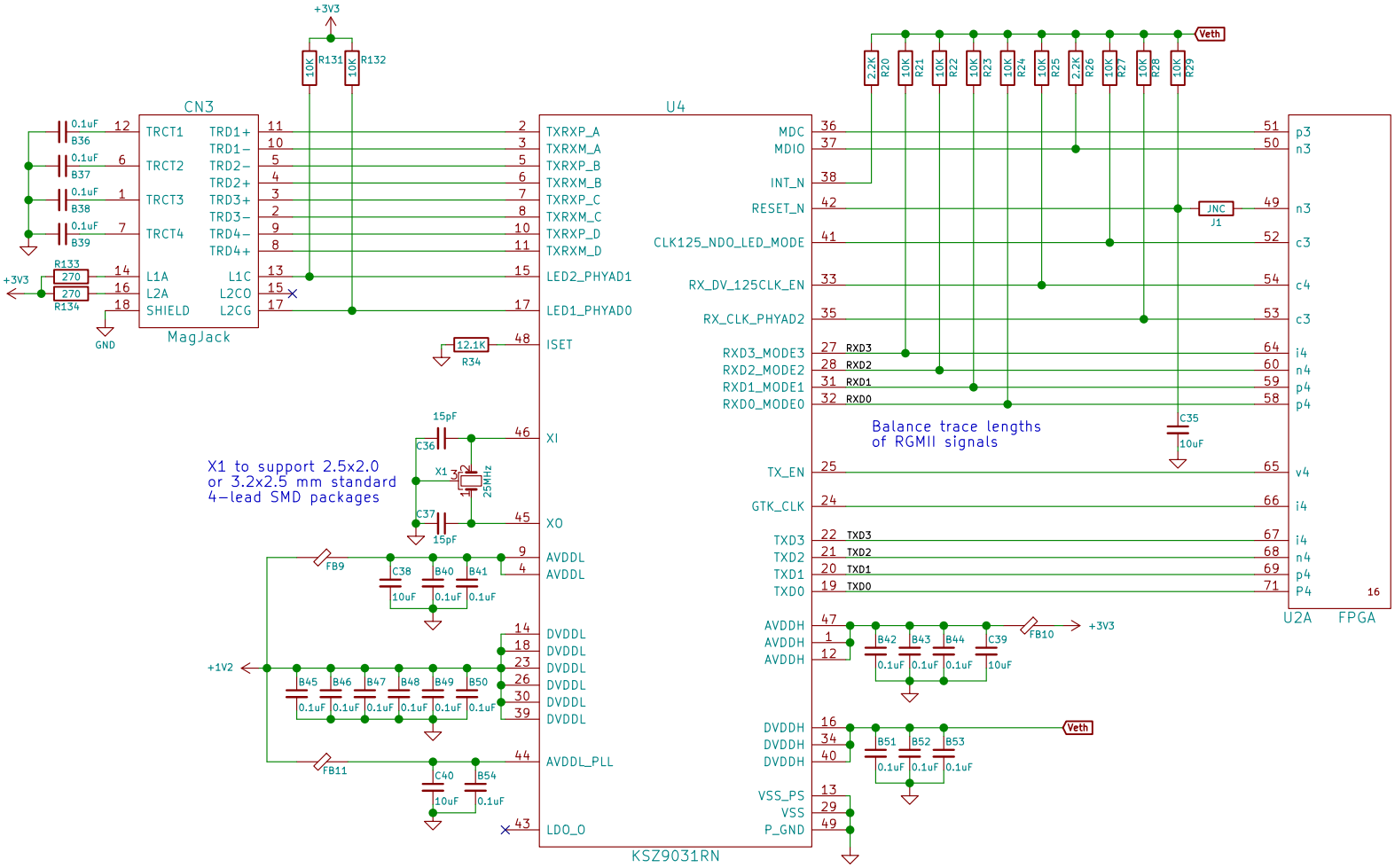
Sheet: /Power and FPGA/
File: Power.sch
Title: Power
Size: USLetter
Date: 2017-10-22
Rev: 2.0-beta5
KiCad E.D.A. kicad 4.0.6
Id: 2/7



Build Options:
None

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Sheet: /Ethernet/	
File: Ethernet.sch	
Title: Ethernet	
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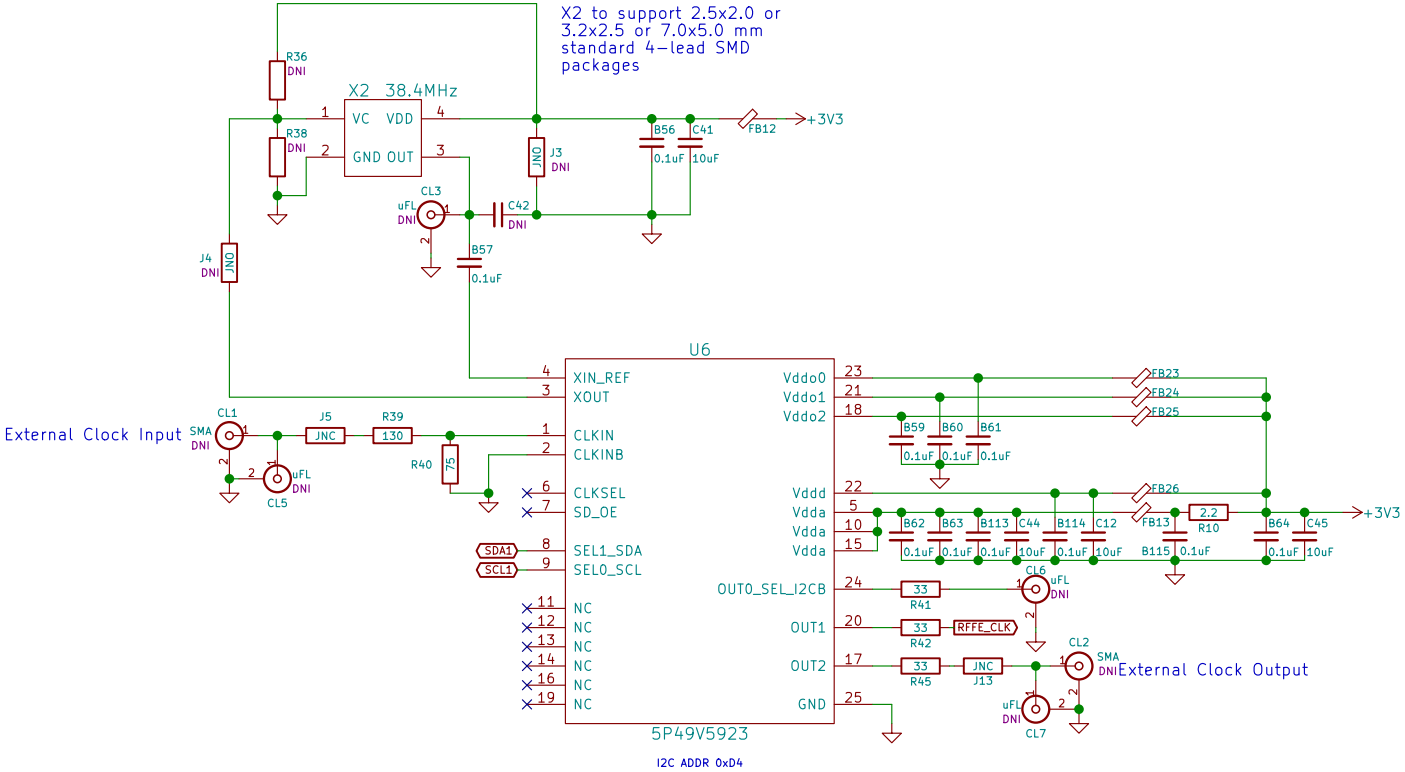
Build Options:

Default Versa with oscillator: Include FB12,C41,B56,B57,X2. Include R36,R38 if required by oscillator. Exclude J3,J4,C42.
Versa with crystal: Include X2 as crystal, B57,J4,J3 as jumper, C42,R38 as 15pF. Exclude FB12,C41,B56,R36.
External clock: Configure U6 for CLKIN input and correct ratio, drive CL1 or CL5 with external clock.
Other experimental options possible with uFL connectors. See RF Frontend sheet for additional AD9866 clock options.



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Sheet: /Clock/
File: Clock.sch

Title: Clock

Size: USLetter	Date: 2017-10-22	**Rev: 2.0-beta5**
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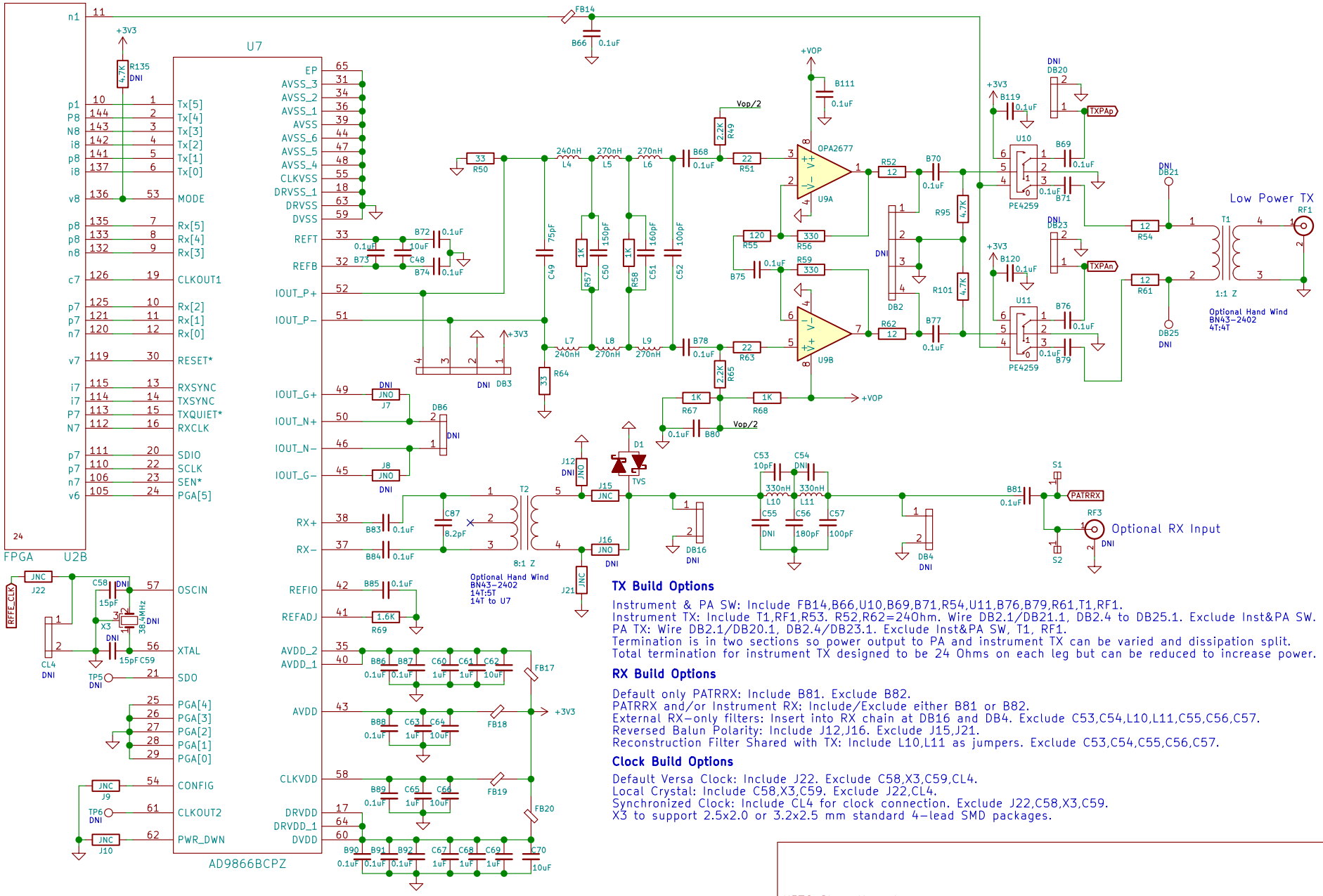

TX Build Options

Instrument & PA SW: Include FB14,B66,U10,B69,B71,R54,U11,B76,B79,R61,T1,RF1.
Instrument TX: Include T1,RF1,R53. R52,R62=240hm. Wire DB2.1/DB21.1, DB2.4 to DB25.1. Exclude Inst&PA SW.
PA TX: Wire DB2.1/DB20.1, DB2.4/DB23.1. Exclude Inst&PA SW, T1, RF1.
Termination is in two sections so power output to PA and instrument TX can be varied and dissipation split.
Total termination for instrument TX designed to be 24 Ohms on each leg but can be reduced to increase power.

RX Build Options

Default only PATRRX: Include B81. Exclude B82.
PATRRX and/or Instrument RX: Include/Exclude either B81 or B82.
External RX-only filters: Insert into RX chain at DB16 and DB4. Exclude C53,C54,L10,L11,C55,C56,C57.
Reversed Balun Polarity: Include J12,J16. Exclude J15,J21.
Reconstruction Filter Shared with TX: Include L10,L11 as jumpers. Exclude C53,C54,C55,C56,C57.

Clock Build Options

Default Versa Clock: Include J22. Exclude C58,X3,C59,CL4.
Local Crystal: Include C58,X3,C59. Exclude J22,CL4.
Synchronized Clock: Include CL4 for clock connection. Exclude J22,C58,X3,C59.
X3 to support 2.5x2.0 or 3.2x2.5 mm standard 4-lead SMD packages.

Op Amp Design by Jim N2ADR
TX Filter Design by Claudio IN3OTD/DK1CG
RX Filter Design by Andrew G4XZL

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Sheet: /RF Frontend/
File: RFFrontend.sch

Title: RF Frontend

Size: USLetter	Date: 2017-10-22	**Rev: 2.0-beta5**
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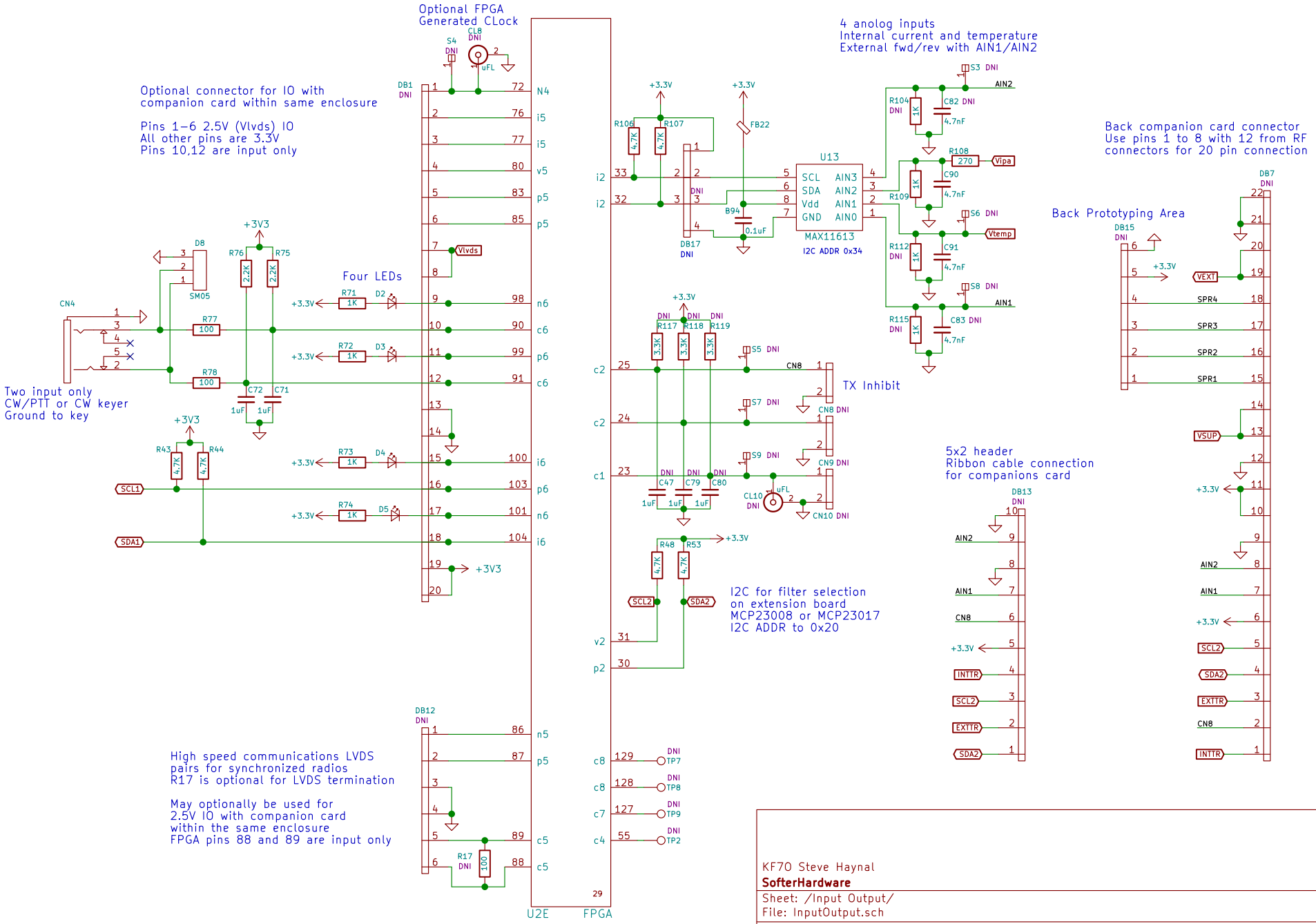
Optional FPGA
Generated CLock
Optional connector for IO with
companion card within same enclosure
Pins 1-6 2.5V (Vlvds) IO
All other pins are 3.3V
Pins 10,12 are input only
Four LEDs
Two input only
CW/PTT or CW keyer
Ground to key
4 anolog inputs
Internal current and temperature
External fwd/rev with AIN1/AIN2
MAX11613
I2C ADDR 0x34
TX Inhibit
I2C for filter selection
on extension board
MCP23008 or MCP23017
I2C ADDR to 0x20
Back companion card connector
Use pins 1 to 8 with 12 from RF
connectors for 20 pin connection
Back Prototyping Area
5x2 header
Ribbon cable connection
for companions card
High speed communications LVDS
pairs for synchronized radios
R17 is optional for LVDS termination
May optionally be used for
2.5V IO with companion card
within the same enclosure
FPGA pins 88 and 89 are input only
U2E
FPGA
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Sheet: /Input Output/
File: InputOutput.sch
Title: Hermes-Lite Input Output
Size: USLetter
Date: 2017-10-22
Rev: 2.0-beta5
KiCad E.D.A. kicad 4.0.6
Id: 6/7

All values are first-cut place holders. To be refined with simulation and experimentation.

Build Optons

Any or all components may be excluded if PA is unused.

SOT-89 or TO-220 LDMOS supported on main circuit board.
TO-220 mounts to side of enclosure.
SOT-89 dissipates heat to PCB and side of enclosure.

Deafult build uses 2 AFT05MS003 mounted on main board, 110mA bias.

PLD-1.5 and alternate SOT-89 supported by adapter board.
Adapter board dissipates heat to side of enclosure.

RD15HVF1 Test Build Option

L33,L34 = 4.7 Ohm
R92,R99 = 500 Ohm
T3 = BN61-202 4T Pri, 2+2T Sec
200 mA bias

Build Optons

Leave relay off for external filter board
Tap RX and TX at relay through holes
Extra grounds on relay footprint

Add attenuation with R97,R98,R94,R100
if PA is overdriven.

Hand Wind
B62152A4X30 or BN43-202
4T Primary, 1+1T Secondary
BN43-1502
8T Primary, 2+2T Secondary
B62152A4X30 runs hot, use 24AWG PTFE/FEP Wire

External PTT
Will ground pin 1
during TX

LDMOS Temperature Sensor

R101,R95,R47,R66 set for AFT05MS003. Bias voltage ranges from 2.5 to 3.5V.
Set R101,R95 to 7.5K, R47,R66 to 3.3K for bias voltage range from 3.1 to 5.3V.

Design based on work by Claudio IN3OTD/DK1CG, John W9JSW, and other LDMOS/MOSFET QRP PA designs

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Sheet: /PA/
File: PA.sch

Title: Hermes-Lite V2 5W Power Amplifier

Size: USLetter	Date: 2017-10-22	**Rev: 2.0-beta5**
KiCad E.D.A. kicad 4.0.6		Id: 7/7