

Power and FPGA

Power.sch

Ethernet

Ethernet.sch

Clock

Clock.sch

RF Frontend

RFFrontend.sch

Input Output

InputOutput.sch

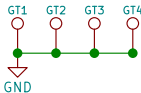
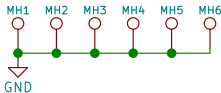
PA

PA.sch

PCB  
PB1

CASE  
EN1

PROG  
PG1



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Sheet: /

File: hermeslite.sch

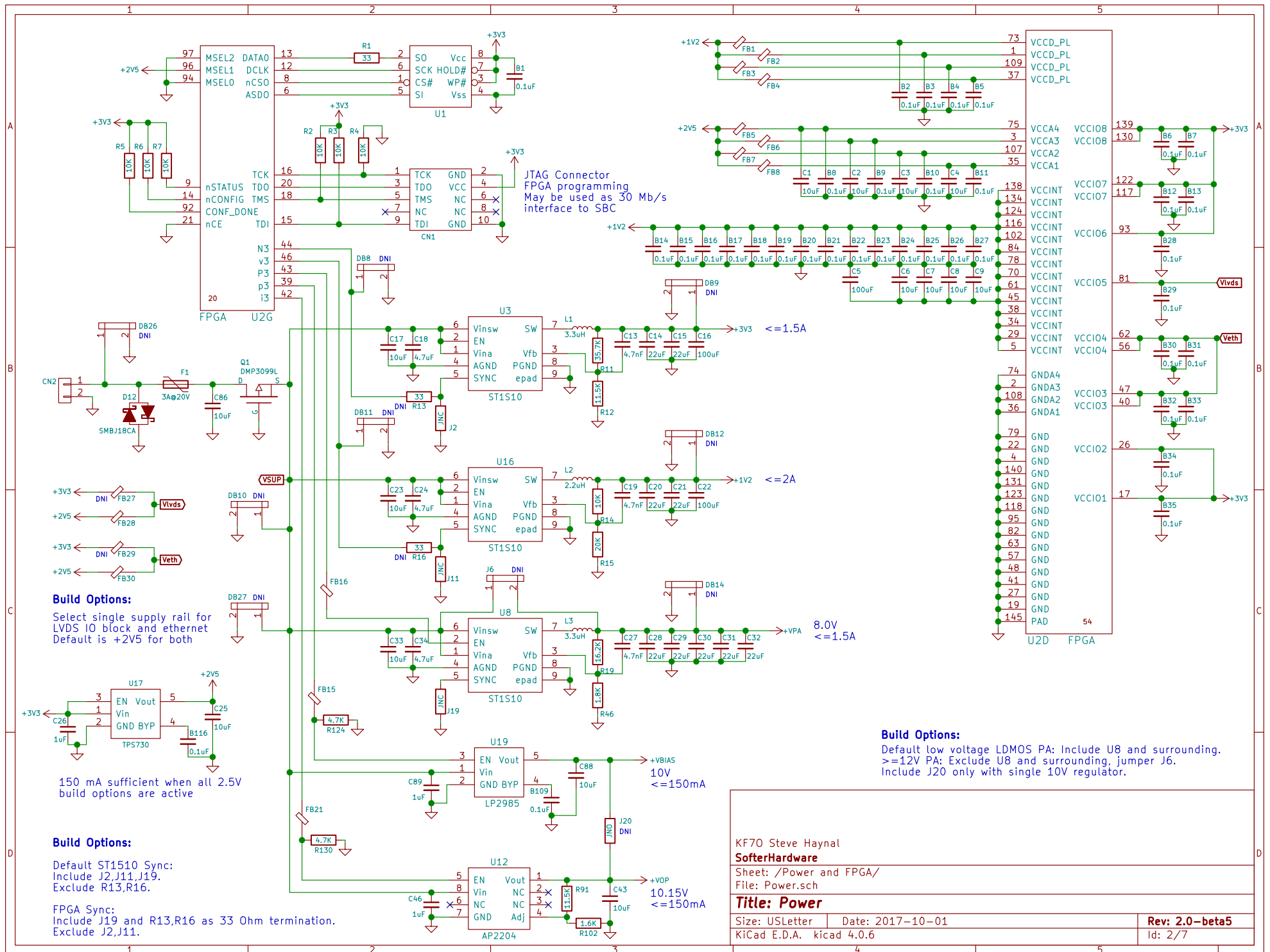
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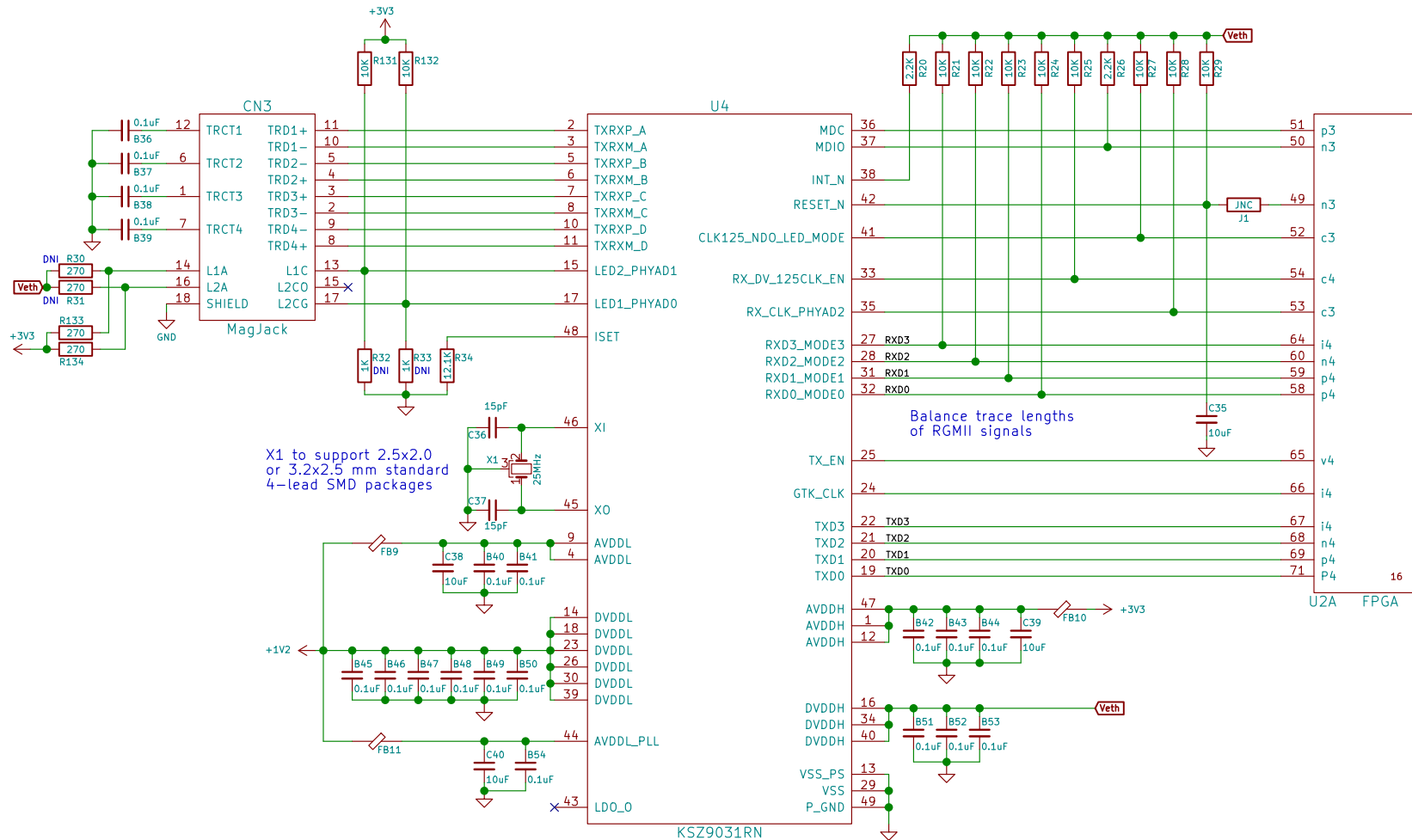
Size: USLetter Date: 2017-10-01

KiCad E.D.A. kicad 4.0.6

Rev: 2.0-beta5

Id: 1/7





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Sheet: /Ethernet/

File: Ethernet.sch

**Title: Ethernet**

Size: USLetter Date: 2017-10-01

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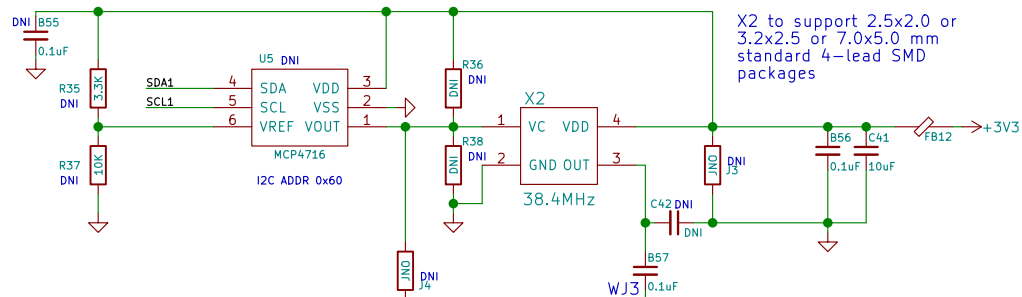
Rev: 2.0-beta5

Id: 3/7

### Build Options:

Default Versa with oscillator: Include FB12,C41,B56,B57,X2. Include R36,R38 if required by oscillator. Exclude B55,R35,R37,U5,J3,J4,C42.  
Versa with VCO: Include FB12,C41,B56,B57,X2,U5,R35,R37,B55. Exclude R36,R38,J4,J3,C42.  
Versa with crystal: Include X2 as crystal, B57,J4,J3 as jumper, C42,R38 as 15pF. Exclude FB12,C41,B56,U5,R35,R36,R37,B55.

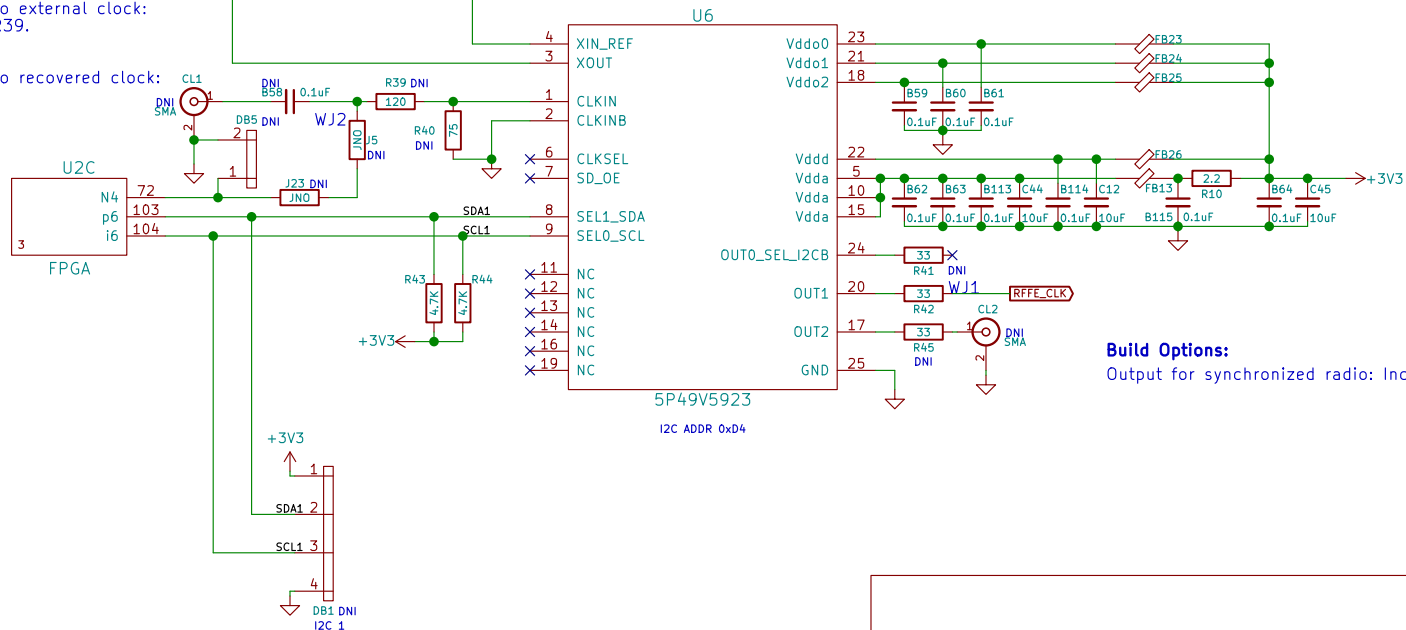
No Versa but oscillator to AD9866: Exclude all Versa components, build for oscillator, connect WJ3 to WJ1.  
No Versa but external clock to AD9866: Exclude all Versa components and oscillator components. Wire from WJ2 to WJ1.  
See RF Frontend sheet for additional AD9866 clock options



### Build Options:

Synchronized radio external clock:  
Include CL1,B58,R39.  
Exclude J23,J25.

Synchronized radio recovered clock:  
Include J23,J5.  
Adjust R39,R40.  
Optional CL1,B58.



### Build Options:

Output for synchronized radio: Include R45,CL2.

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Sheet: /Clock/

File: Clock.sch

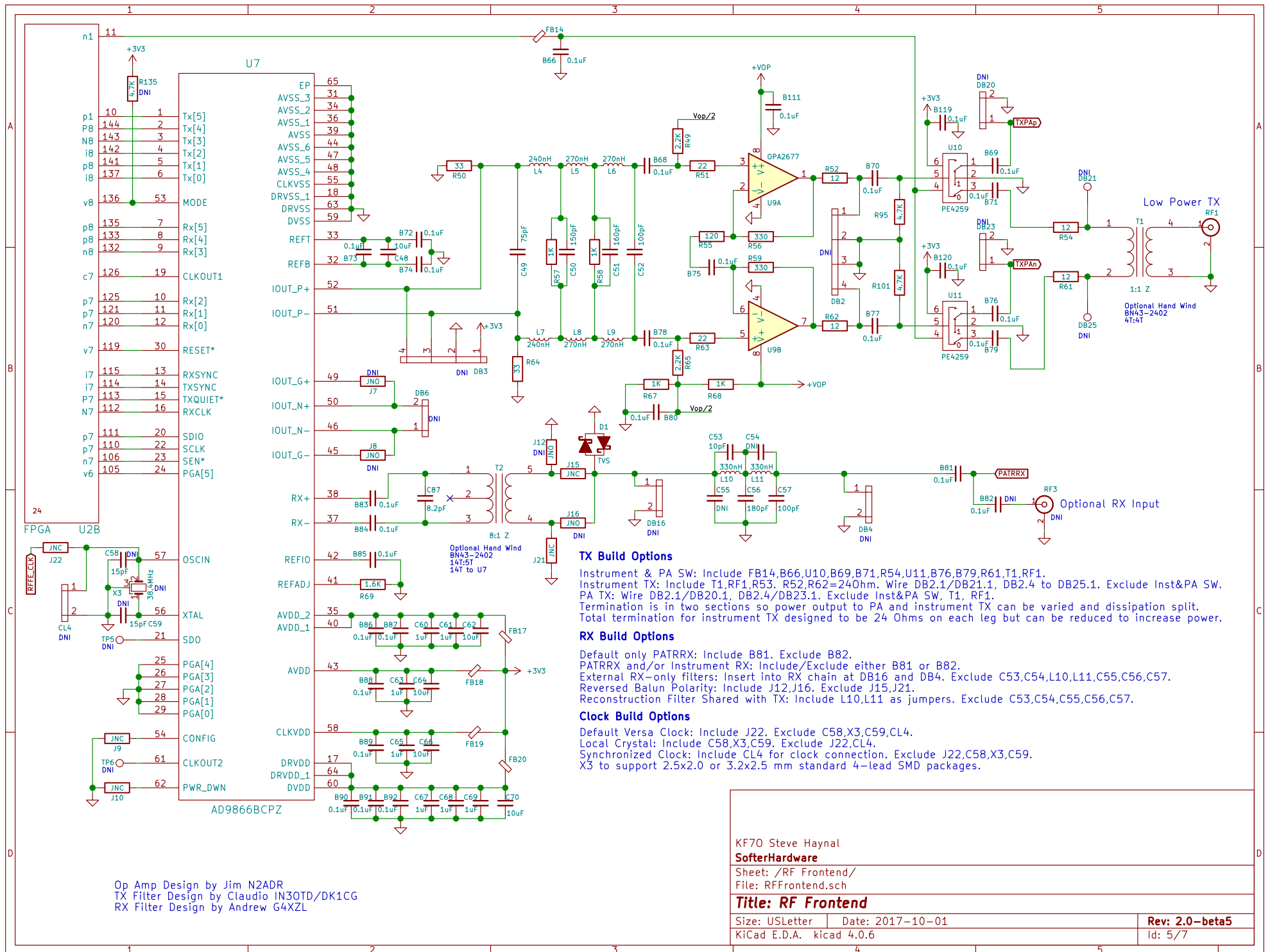
Title: Clock

Size: USLetter Date: 2017-10-01

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Id: 4/7





Id: 7/7