Power and FPGA

Power.sch

Ethernet

Ethernet.sch

Clock

Clock.sch

RF Frontend

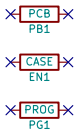
RFFrontend.sch

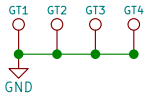
Input Output

InputOutput.sch

PA

PA.sch





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Sheet: /
File: hermeslite.sch

Title: Hermes-Lite

Size: USLetter	Date: 2016-11-13	**Rev: 2.0-beta2**
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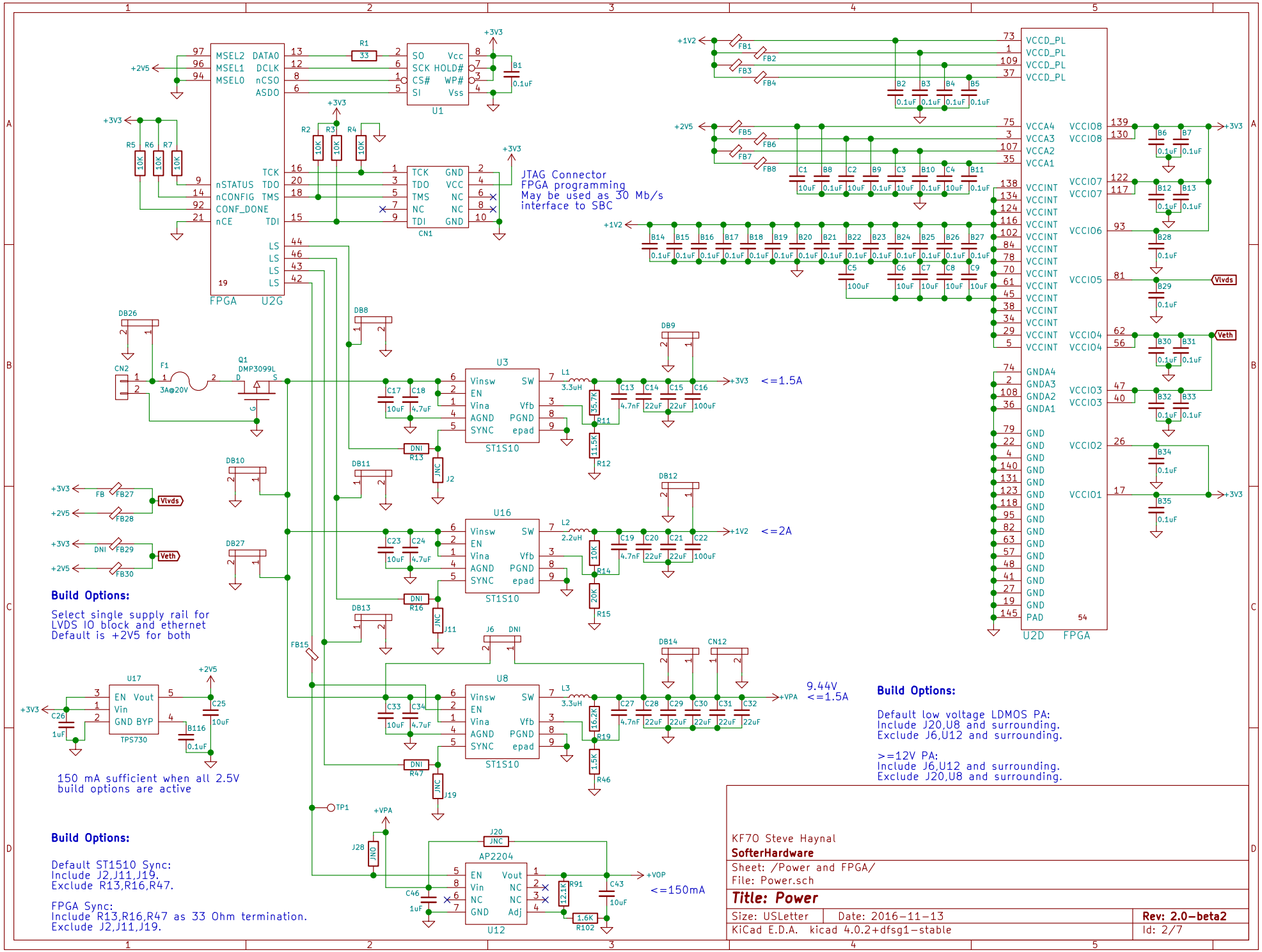
FPGA U2G
JTAG Connector
FPGA programming
May be used as 30 Mb/s
interface to SBC
U1
CN1
U3
ST1S10
U16
U8
U17
TPS730
U12
AP2204
U2D FPGA
<=1.5A
<=2A
9.44V
<=1.5A
<=150mA
Build Options:
Select single supply rail for
LVDS IO block and ethernet
Default is +2V5 for both
150 mA sufficient when all 2.5V
build options are active
Build Options:
Default ST1510 Sync:
Include J2,J11,J19.
Exclude R13,R16,R47.
FPGA Sync:
Include R13,R16,R47 as 33 Ohm termination.
Exclude J2,J11,J19.
Build Options:
Default low voltage LDMOS PA:
Include J20,U8 and surrounding.
Exclude J6,U12 and surrounding.
>=12V PA:
Include J6,U12 and surrounding.
Exclude J20,U8 and surrounding.
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Sheet: /Power and FPGA/
File: Power.sch
Title: Power
Size: USLetter
Date: 2016-11-13
Rev: 2.0-beta2
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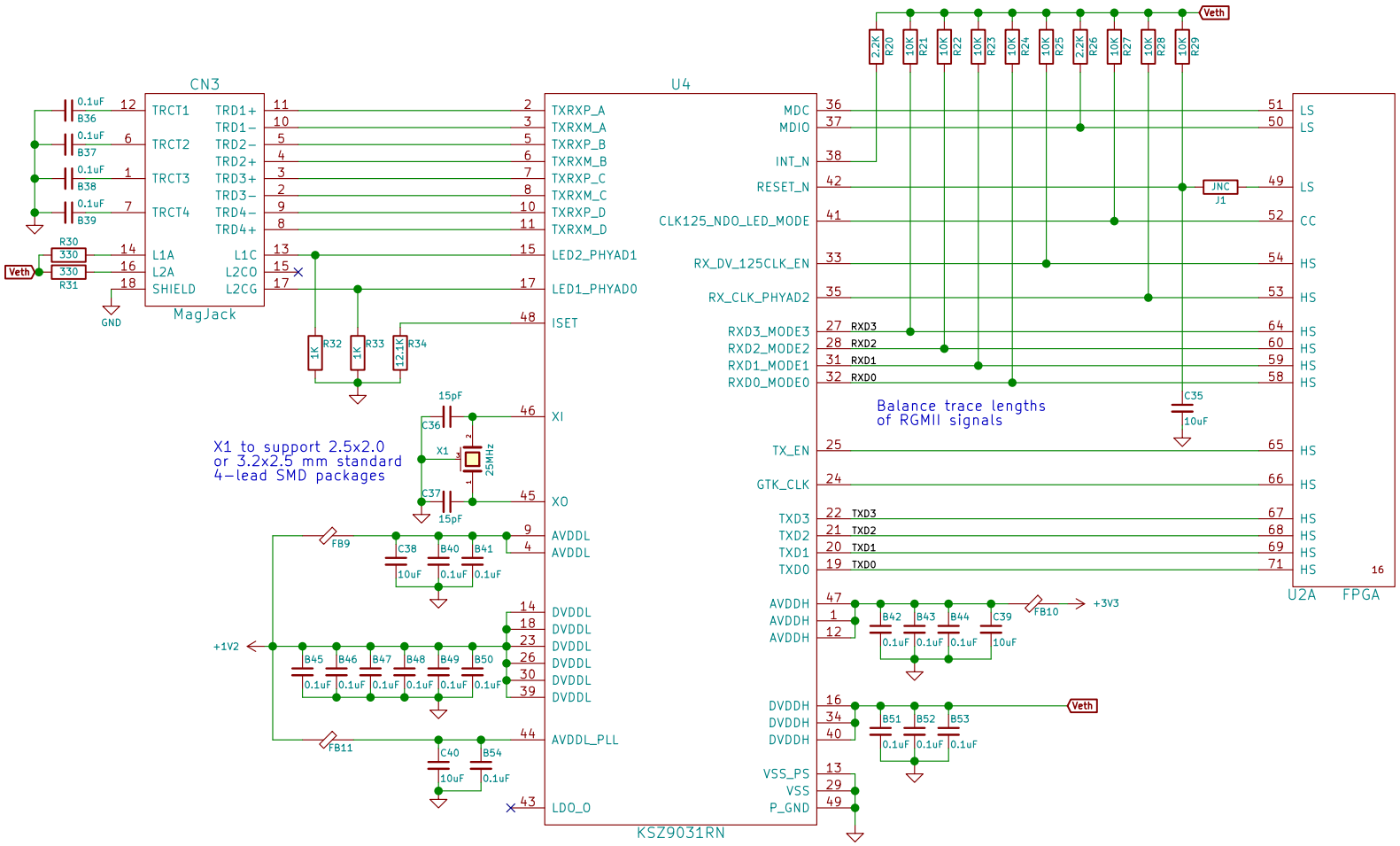
Id: 2/7



Build Options:
None

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Sheet: /Ethernet/	
File: Ethernet.sch	
Title: Ethernet	
Size: USLetter | Date: 2016-11-13	**Rev: 2.0-beta2**
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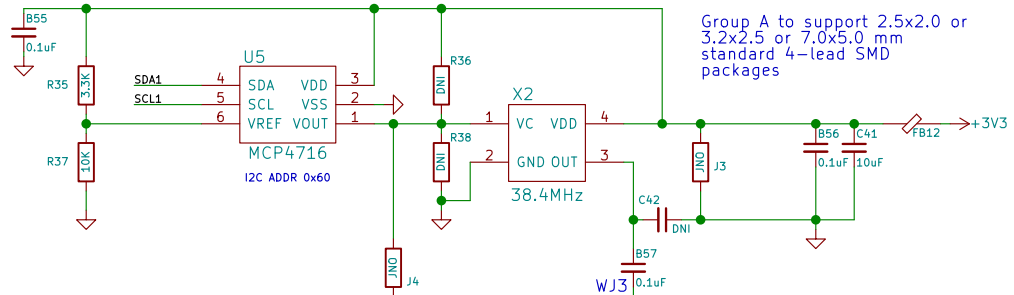
Build Options:

Default Versa with oscillator: Include FB12,C41,B56,B57,X2. Include R36,R38 if required by oscillator. Exclude B55,R35,R37,U5,J3,J4,C42.
Versa with VCO: Include FB12,C41,B56,B57,X2,U5,R35,R37,B55. Exclude R36,R38,J4,J3,C42.
Versa with crystal: Include X2 as crystal, B57 as jumper, J4,J3,C42, R38 as 15pF. Exclude FB12,C41,B56,U5,R35,R36,R37,B55.

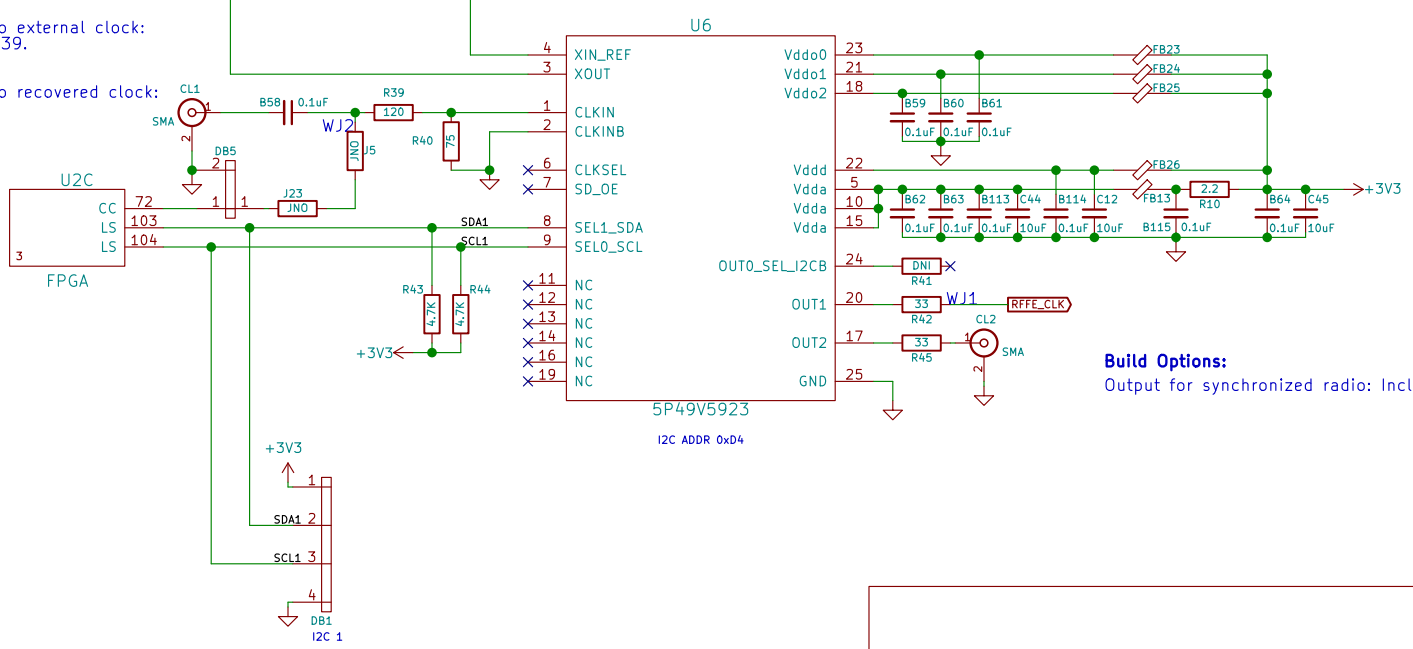
No Versa but oscillator to AD9866: Exclude all Versa components, build for oscillator, connect WJ3 to WJ1.
No Versa but external clock to AD9866: Exclude all Versa components and oscillator components. Wire from WJ2 to WJ1.
See RF Frontend sheet for additional AD9866 clock options



Build Options:

Synchronized radio external clock:
Include CL1,B58,R39.
Exclude J23,J25.

Synchronized radio recovered clock:
Include J23,J5.
Adjust R39,R40.
Optional CL1,B58.



Build Options:
Output for synchronized radio: Include R45,CL2.

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Sheet: /Clock/
File: Clock.sch

Title: Clock

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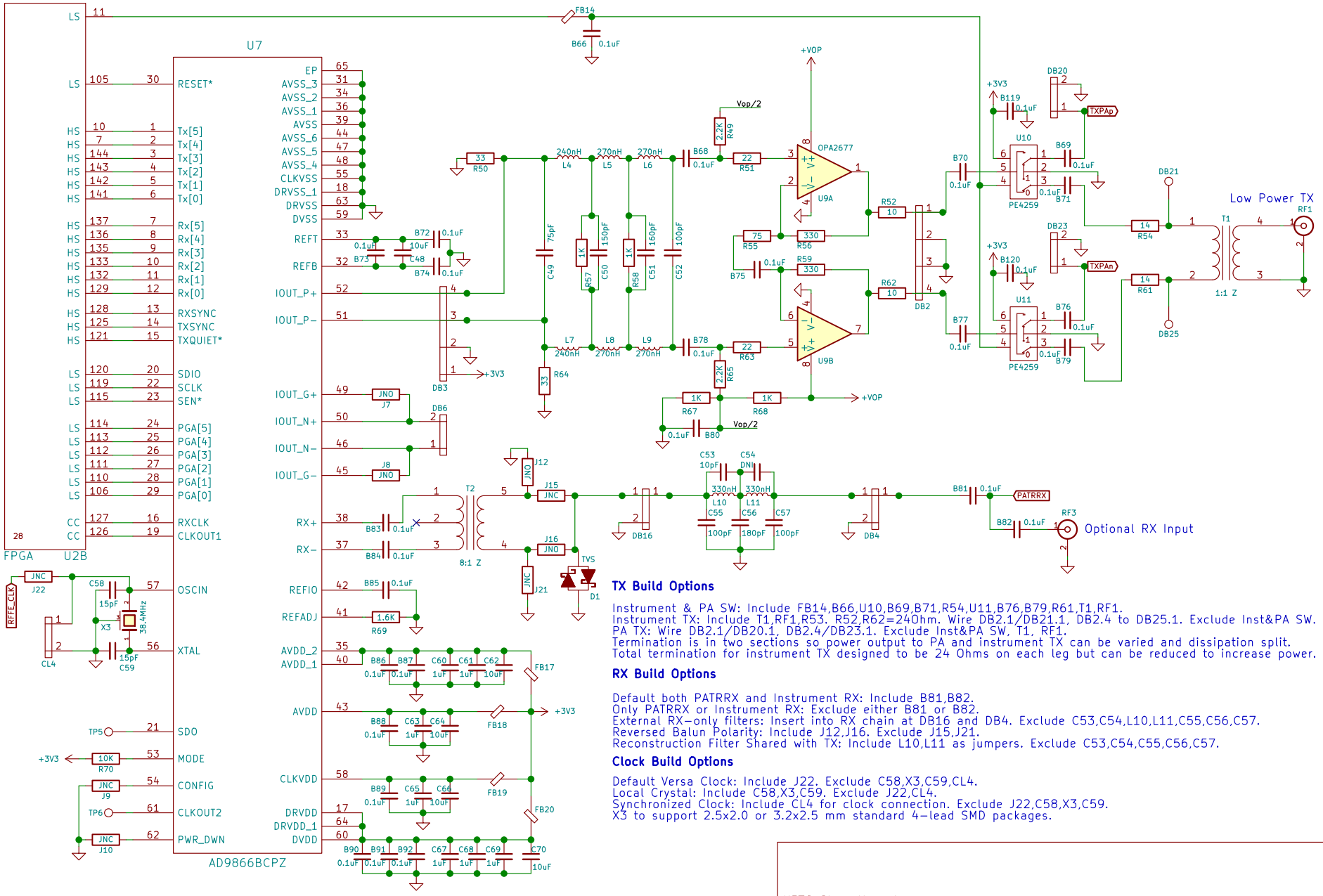

TX Build Options

Instrument & PA SW: Include FB14,B66,U10,B69,B71,R54,U11,B76,B79,R61,T1,RF1.
Instrument TX: Include T1,RF1,R53. R52,R62=24Ohm. Wire DB2.1/DB21.1, DB2.4 to DB25.1. Exclude Inst&PA SW.
PA TX: Wire DB2.1/DB20.1, DB2.4/DB23.1. Exclude Inst&PA SW, T1, RF1.
Termination is in two sections so power output to PA and instrument TX can be varied and dissipation split.
Total termination for instrument TX designed to be 24 Ohms on each leg but can be reduced to increase power.

RX Build Options

Default both PATRRX and Instrument RX: Include B81,B82.
Only PATRRX or Instrument RX: Exclude either B81 or B82.
External RX-only filters: Insert into RX chain at DB16 and DB4. Exclude C53,C54,L10,L11,C55,C56,C57.
Reversed Balun Polarity: Include J12,J16. Exclude J15,J21.
Reconstruction Filter Shared with TX: Include L10,L11 as jumpers. Exclude C53,C54,C55,C56,C57.

Clock Build Options

Default Versa Clock: Include J22. Exclude C58,X3,C59,CL4.
Local Crystal: Include C58,X3,C59. Exclude J22,CL4.
Synchronized Clock: Include CL4 for clock connection. Exclude J22,C58,X3,C59.
X3 to support 2.5x2.0 or 3.2x2.5 mm standard 4-lead SMD packages.

Op Amp Design by Jim N2ADR
TX Filter Design by Claudio IN3OTD/DK1CG
RX Filter Design by Andrew G4XZL

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Sheet: /RF Frontend/
File: RFFrontend.sch

Title: RF Frontend

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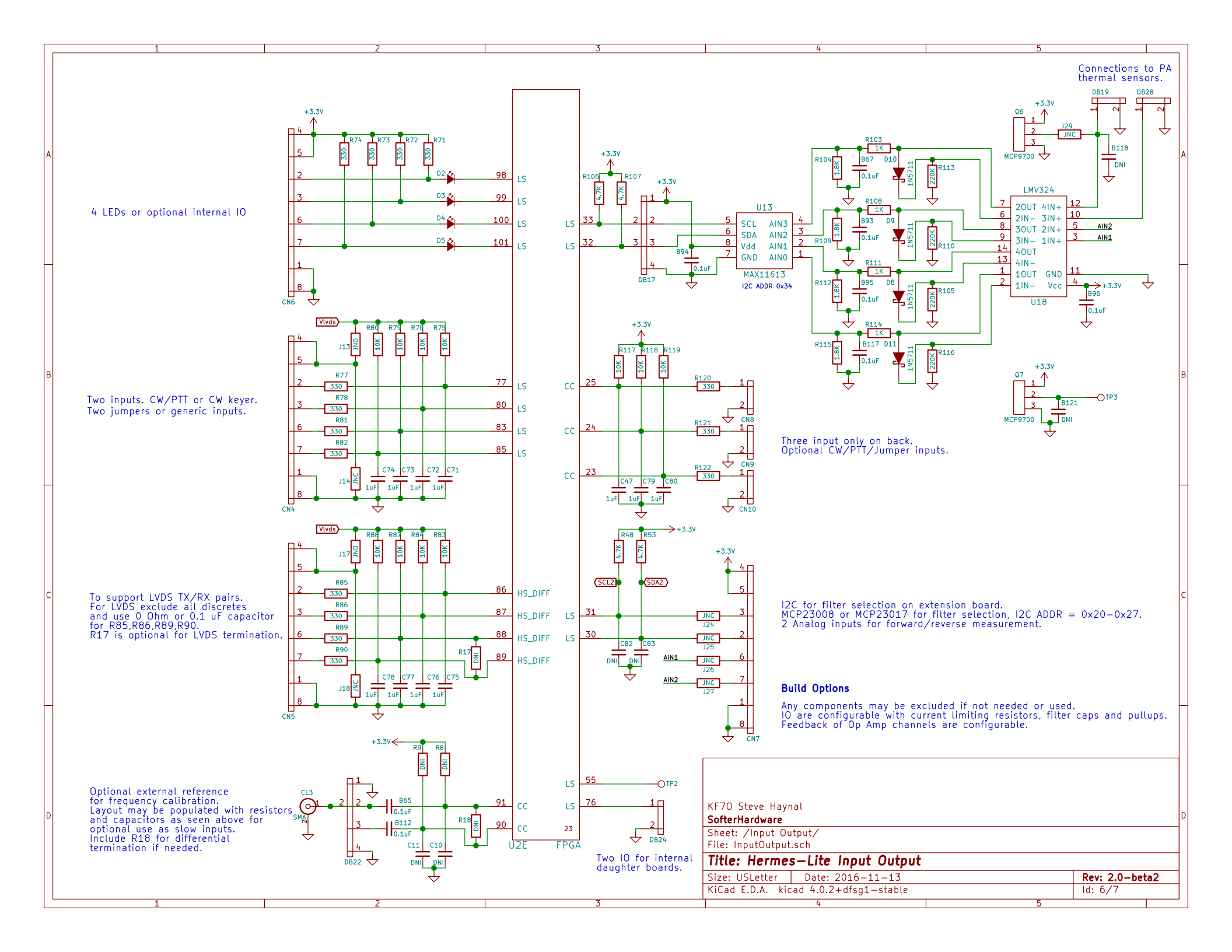
4 LEDs or optional internal IO
Two inputs. CW/PTT or CW keyer.
Two jumpers or generic inputs.
To support LVDS TX/RX pairs.
For LVDS exclude all discretes
and use 0 Ohm or 0.1 uF capacitor
for R85,R86,R89,R90.
R17 is optional for LVDS termination.
Optional external reference
for frequency calibration.
Layout may be populated with resistors
and capacitors as seen above for
optional use as slow inputs.
Include R18 for differential
termination if needed.
Two IO for internal
daughter boards.
Connections to PA
thermal sensors.
Three input only on back.
Optional CW/PTT/Jumper inputs.
I2C for filter selection on extension board.
MCP23008 or MCP23017 for filter selection, I2C ADDR = 0x20-0x27.
2 Analog inputs for forward/reverse measurement.
Build Options
Any components may be excluded if not needed or used.
IO are configurable with current limiting resistors, filter caps and pullups.
Feedback of Op Amp channels are configurable.
MAX11613
I2C ADDR 0x34
LMV324
FPGA
U2E
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Sheet: /Input Output/
File: InputOutput.sch
Title: Hermes-Lite Input Output
Size: USLetter
Date: 2016-11-13
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All values are first-cut place holders. To be refined with simulation and experimentation.

Build Optons

Any or all components may be excluded if PA is unused.

SOT-89 or TO-220 LDMOS supported on main circuit board.
TO-220 mounts to side of enclosure.
SOT-89 dissipates heat to PCB and side of enclosure.

Deafult build uses 2 AFT05MS003 mounted on main board, 110mA bias.

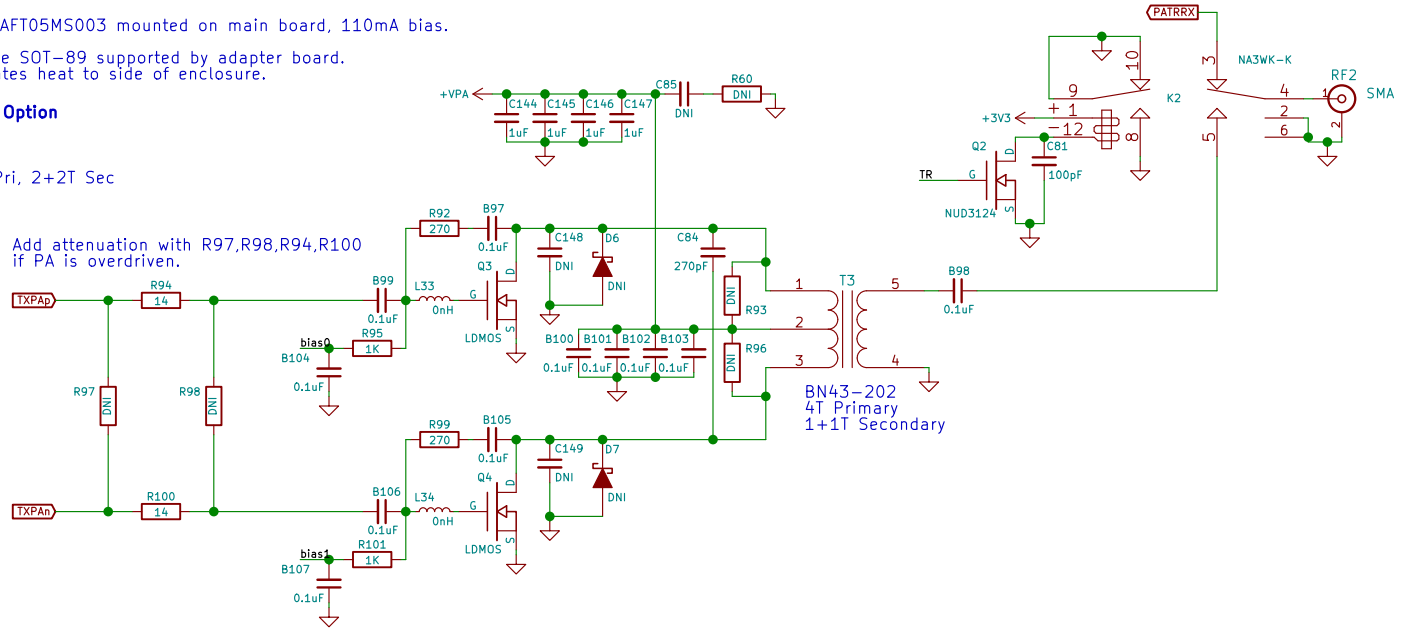
PLD-1.5 and alternate SOT-89 supported by adapter board.
Adapter board dissipates heat to side of enclosure.

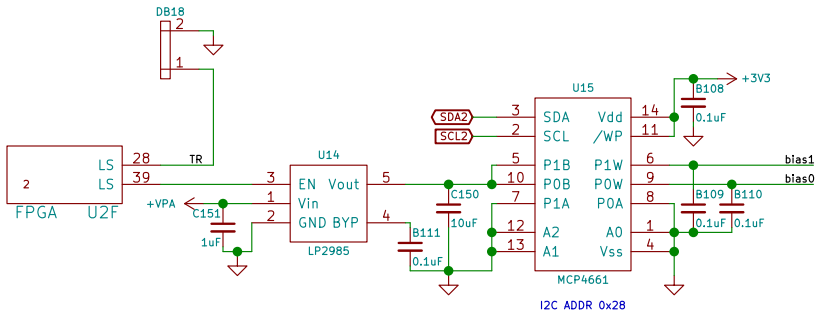
RD15HVF1 Test Build Option

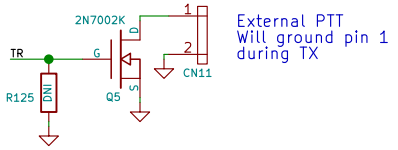
L33,L34 = 4.7 Ohm
R92,R99 = 500 Ohm
T3 = BN61-202 4T Pri, 2+2T Sec
200 mA bias

Build Optons

Leave relay off for external filter board
Tap RX and TX at relay through holes
Extra grounds on relay footprint







Design based on work by Claudio IN3OTD/DK1CG, John W9JSW, and other LDMOS/MOSFET QRP PA designs

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Sheet: /PA/
File: PA.sch

Title: Hermes-Lite V2 5W Power Amplifier

Size: USLetter	Date: 2016-11-13	**Rev: 2.0-beta2**
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