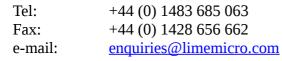
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# **Stream protocol**

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# **Revision History**

#### Version 01r00

Released: 23 Nov, 2015

Initial version.

#### Version 02r00

Released: 13 Jan, 2016

Updated FPGA registers map. Fixed bits indexes in samples data structures.

#### Version 03r00

Released: 28 Jan, 2016

Changed packet header byte indexes.

#### Version 04r00

Released: 17 Feb, 2016

Added timestamp reseting, timestamp synchronization individually for each packet.

#### Version 05r00

Released: 9 May, 2016

Updated FPGA registers map.

# 1

# **Packet structure**

Total packet size is 4096 bytes. It consists of two main parts: header and payload as described in Table 1. Header contains receiver and transmitter status flags and packet timestamp. Timestamp is a 64 bit samples counter used to synchronize received and transmitted signals. The counter is being incremented with each sample after Receiver is enabled. Timestamp can be reset to 0, by using SMPL\_NR\_CLR bit, packets streaming should be disabled when reseting timestamp. Payload contains RF samples data, the data format and ordering depends on number of active channels and each sample bit count.

Table 1 Packet structure

Byte index Bits Description			
Header			
0	15-2	Reserved	
	4	Disable timestamp synchronization for this packet. Gets OR'ed with SPI SYNCH_DIS	
		0 – synchronize packet transmitting with timestamp <b>(For transmitting only)</b>	
		1– ignore timestamp, transmit as soon as possible. Prior synchronized packets existing in	
		FIFO can delay transmitting of unsynchronized packet.	
	3	Tx packet dropped:	
		0 - Tx is working normally	
		1 - Tx received packet with obsolete timestamp	
	2-0	FPGA Rx FIFO fill status:	
		0– from 0% to 12.5%	
		1 – from 12.5% to 25%	
		2 – from 25% to 37.5%	
		3 – from 37.5% to 50%	
		4 – from 50% to 62.5%	
		5 – from 62.5% to 75%	
		6 – from 75% to 87.5%	
		7 – from 87.5% to 100%	
1-7	15-0	Reserved	
8-15	15-0	Timestamp:	
		64 bit samples counter, stored in Big endian format	
		When Receiving: timestamp when the first sample in payload was received	
		When Transmitting: timestamp when the first sample in payload should be transmitted	
Payload			
16-4095	15-0	RF samples data:	

# 1.1.1 Streaming configuration

Streaming configuration should be set before initiating data streaming. Protocol configuration is set by writing to board SPI registers. DNU - Do not use (register bit unsuported in device)

Table 2 Configuration registers

Address	Def. value	Bits	Name	Description	LimeSRD-USB 1v2
0x0000		15-0	Board ID		000E
0x0001		15-0	GW function		1
0x0002	Ì	15-0	GW revision		
		15-8	Reserved		
0x0003	00F0	7-4	GW_TEST_RES	Read only, returns inverted bits from GW_TEST	
		3-0	GW_TEST	Value to test GW SPI	
0x0004	0000	15-0	PHASE_REG_SEL	Value for phase shift in direct clocking mode	
0x0005	0000	15-0	DRCT_CLK_EN	Each bit enables clock to be direct clock source: 1 - enabled, 0 - disabled [n] - nth clock	
				[1] - Second clock	RX clk
				[0] - First clock	TX clk
		15-11	Reserved		
0x0006	0000	10	LOAD_PH_REG	"1" - loads phase shift value from PHASE_REG_SEL, to phase shift module	
		9-5	CNT_IND	Clock counter selection	
		4-0	CLK_IND	Clock selection	0 - TX clk, 1 - RX clk
0x0007	0003	15-0	CH_EN	MIMO Channel enables each bit means: 1- enabled, 0-disabled [n] - nth channel [1] - channel 1 [0] - channel 0	
	0102	15-11	Reserved		
		10	Reserved		DNU
0x0008		9	SYNCH_DIS	Packets synchronization using timestamps:  0 - Enabled  1 - Disabled	
UAUUUU		8	MIMO_INT_EN		
		7-2	Reserved		
		1-0	SMPL_WIDTH	"10"-12bit, "01"-14bit,	
				"00"-16bit	

	0003	15-2	Reserved		
		1	TXPCT_LOSS_CLR	Rising edge clears flag about tx packets dropping	
0x0009		0	SMPL_NR_CLR	Reset_timestamp: Rx and Tx should be stopped when reseting 1 - 0 - Normal operation	
	0000	15-3	Reserved		
0000 4		2	STREAM_LOAD		DNU
0x000A		1	TX_EN		
		0	RX_EN		

#### 1.1.1.1 12 bit compressed samples

When using 12 bit compressed samples configuration the packet payload has the following structure. Bytes are indexed from payload start.

Table 3 Samples data structure

Byte index	Bits	Description
0	7-0	ch0_I0 [7:0]
1	7-4	ch0_Q0[3:0]
	3-0	ch0_I0 [11:8]
2	7-0	ch0_Q0[11:4]
3	7-0	ch1_I1 [7:0]
4	7-4	ch1_Q1[3:0]
	3-0	ch1_I1 [11:8]
5	7-0	ch1_Q1[11:4]

#### 1.1.1.2 16 bit compressed samples

When using 16 bit compressed samples configuration the packet payload has the following structure. Bytes are indexed from payload start.

Table 4 Samples data structure

Byte index	Bits	Description
0	7-0	ch0_I0 [7:0]
1	7-0	ch0_I0 [15:8]
2	7-0	ch0_Q0[7:0]
3	7-0	ch0_Q0[15:0]
4	7-0	ch1_I1[7:0]
5	7-0	ch1_11[15:8]
6	7-0	ch1_Q1[7:0]
7	7-0	ch1_Q1[15:8]