Qualification Report

OpenCellular - Connect1
General Purpose Baseband Computing (GBC)

Revision: 1.0

1. Purpose

The purpose of this document is to capture test data for General Purpose Baseband Computing (GBC) module as part of OpenCellular Base Transceiver Station (BTS). The document provides formal report of measured and validated parameters to qualify GBC module as part of design validation testing to ensure consistent and reliable operation across all supported operating and environmental conditions.

2. Scope

Scope of this document is to qualify different sections as mentioned below:

1. **Power Source section** which includes, PoE, Solar, Lead Acid battery and Li Ion battery
2. **CPU section** which includes Intel Baytrail SoC, PMIC, DDR, Springville, mSATA
3. **TIVA section** with various sensors
4. **Ethernet section** which covers Compliance testing at 100Mbps speed

3. Device-Under-Test (DUT) Details

1. System : OpenCellular Connect -1
2. Sub-system : GBC
3. Hardware version : Life–1 & Life -2

4. Software version :
    a. Ubuntu – 14.04.64 bit
    b. CoreBoot - 4.4-575-gfee24cc-dirty
    c. RTOS- 2_16_00_08
5. Sample Count : 01
6. DUT Sl. No : WZ1630LIFE2GBC0002, WZ1630LIFE2GBC0005 WZ1630LIFE2GBC0010, WZ1630LIFE2GBC0018 & WZ1630LIFE2GBC0021

4. Qualification Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +18V DC

Typical Load – 10.8 – 12.6W

5. Qualification Result Summary


Qualification Result Summary.xlsx

6. Tools and Test Equipment

Tools and Test Equipment	Model and Version Information
Oscilloscope	MSO4034, MSO9404A
DC Power Supply	DP832, E3633A, E3634A
Electronic Load	KMO64
IR Thermometer	Fluke 59
Multimeter	Fluke 17B+
Solar cell array simulator	Agilent E4350B
PoE Injector	PS-201G++

7. Abbreviation

GBC	General Purpose Baseband Computing
PoE	Power over Ethernet
PD	Powered device

PSE	Power Sourcing Equipment
RF-SDR	Radio frequency Software-Defined Radio\
BTS	Base Transceiver Station

9 Qualification Tests Results

9.1 Front Panel:

9.1.1 Solar Supply

9.1.1.1 Test ID / Test Name: FP.1.1 / Voltage accuracy

9.1.1.1.1 Purpose

Solar power input is designed to work in the range of 16 to 22V. The purpose of the test case is to validate the range of solar input voltages for which GBC will be functional.

9.1.1.1.2 Test and Measurement Method

This test is conducted by configuring Solar array simulator E4350B to give a voltage in the range of 16V to 22V by setting it to SAS Mode (Setting Voc, Vmp, Isc and Imp parameters accordingly). Vary the simulator settings for voltages in steps of 2V, measure the input voltage at JTB10A.1, R1304.2, C3M171.1 and C1685.1 and make sure the voltages are in the range of 16V to 22V. Please refer to Section **3.2.1.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.1.1.1.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 16V – 22V
System load – Typical

9.1.1.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – NA

9.1.1.1.5 Test Results

The measured voltages are in range of the set voltages of solar supply output.

9.1.1.1.6 Measurement Logs

NOTE: Pass Criteria: Measured Voltage should be equal to input voltage ±5%

Input Voltage Accuracy for Solar Supply												
Sl. No.	Test case No.	Voc (V)	Vmp(V)	Load current (A)	VPSOLAR (JTB10A.1)	VSLR_OVUVOUT(R1304.2)	VSLRPOE_VOUT (C3M171.1)	VPS_VOUT(C1685.1)	Specification		Margin (%)	PASS / FAIL
									Min	Max		
1	FP 1.1	16	15.6	2.25	15.54	15.53	15.5	15.49	14.82	16.38	-4.52	PASS
2	FP 1.1	18	17.6	2	17.7	17.69	17.67	17.66	16.72	18.48	-4.44	PASS
3	FP 1.1	20	19.6	1.8	19.84	19.83	19.81	19.8	18.62	20.58	-3.79	PASS
4	FP 1.1	22	21.6	1.63	21.96	21.96	21.93	21.92	20.52	22.68	-3.35	PASS

NOTE: The detailed analysis report is embedded in the xls document attached in the end of this section.

9.1.1.2 Test ID / Test Name: FP.1.2 / Input supply range

9.1.1.2.1 Purpose

Solar supply input is designed to work in the range of 16 to 22V. The purpose of the test case is to validate the range of solar voltages for which GBC will be functional.

9.1.1.2.2 Test and Measurement Method

This test is conducted by configuring Solar array simulator E4350B to give a voltage in the range of 16V to 22V by setting it to SAS Mode (Setting Voc, Vmp, Isc and Imp parameters accordingly). Vary the simulator settings for voltages in steps of 2V, measure the input voltage at JTB10A.1, R1304.2, C3M171.1. Make sure the voltages are in the range of 16V to 22V. For every change in input voltage, measure the output voltage of Buck-Boost converter (U88) at R10044.2 and should read 12V. Please refer to Section **3.2.1.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.1.1.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 16V – 22V

System load – Typical

9.1.1.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – NA

9.1.1.2.5 Test Results

By varying the solar input, it is ensured that Buck-Boost output is 12Vwhich in-turn ensures proper functionality of GBC module.

9.1.1.2.6 Measurement Logs

Input Voltage Range for Solar Supply												
Sl. No.	Test case No.	Voc (V)	Vmp (V)	Load current (A)	VPSOLAR (JTB10A.1)	VSLR_OVUVOUT (R1304.2)	VSLRPOE_VOUT (C3M171.1)	12V_IN (R10044.2)	Specification		Margin (%)	PASS / FAIL
									Min	Max		
1	FP 1.2	16	15.6	2.25	15.54	15.53	15.5	12.06	11.76	12.24	-1.47	PASS
2	FP 1.2	18	17.6	2	17.7	17.69	17.67	12.06	11.76	12.24	-1.47	PASS
3	FP 1.2	20	19.6	1.8	19.84	19.83	19.81	12.06	11.76	12.24	-1.47	PASS
4	FP 1.2	22	21.6	1.63	21.96	21.96	21.93	12.06	11.76	12.24	-1.47	PASS

NOTE:

1) Pass Criteria for input voltage range: Measured Voltage should be equal to input voltage ±5%
2) Pass Criteria for Buck-Boost converter: Measured Voltage should be 12V±2%

The detailed analysis report for solar test cases executed is embedded in the xls document attached herewith.

Solar_Supply_Measurement_log.xlsx

9.1.2 AUX Supply

9.1.2.1 Test ID / Test Name: FP.2.1 / Voltage accuracy

9.1.2.1.1 Purpose

AUX power input is designed to work in the range of 16 to 24V. The purpose of the test case is to validate the range of AUX input voltages for which GBC will be functional.

9.1.2.1.2 Test and Measurement Method

This test is conducted by configuring AUX supply to give a voltage in the range of 16V to 24V. Vary the simulator settings for voltages in steps of 2V, measure the input voltage at JTB10A.1, R1304.2, C3M171.1, and C1685.1 and make sure the voltages are in the range of 16V to 24V Please refer to Section **3.2.2.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.1.2.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 16V – 24V

System load – Typical

9.1.2.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – NA

9.1.2.1.5 Test Results

The measured voltages are in range of the set voltages of AUX supply output.

9.1.2.1.6 Measurement Logs

Input Voltage Accuracy for AUX Supply										
Sl. No.	Test case No.	Input Voltage (V)	VPSOLAR (JTB10A.1)	VSLR_OVUVOUT (R1304.2)	VSLRPOE_VOUT(C3M171.1)	VPS_VOUT(C1685.1)	Specification		Margin (%)	PASS / FAIL
							Min	Max		
1	FP 2.1	16	16.04	16.04	16.02	16.01	15.2	16.8	-4.70	PASS
2	FP 2.1	18	18.03	18.03	18	18	17.1	18.9	-4.76	PASS
3	FP 2.1	20	20.02	20.02	20	20	19	21	-4.76	PASS
4	FP 2.1	22	22.02	22.02	21.99	21.99	20.9	23.1	-4.81	PASS
5	FP 2.1	24	24.01	24.01	23.99	23.99	22.8	25.2	-4.80	PASS

NOTE:

1) Pass Criteria: Measured Voltage should be equal to input voltage ±5%
2) The detailed analysis report is embedded in the xls document attached in the end of this section.

9.1.2.2 Test ID / Test Name: FP.2.2 / Input supply range

9.1.2.2.1 Purpose

AUX supply input is designed to work in the range of 16 to 24V. The purpose of the test case is to validate the range of AUX voltages for which GBC will be functional.

9.1.2.2.2 Test and Measurement Method

This test is conducted by AUX power supply to give a voltage in the range of 16V to 24V. Varying the AUX supply settings for voltages in steps of 2V, measure the input voltage at JTB10A.1, R1304.2, and C3M171.1 and make sure the voltages are in the range of 16V to 24V. For every change in input voltage, measure the output voltage of Buck-Boost converter (U88) at R10044.2 and should read 12V. Please refer to Section **3.2.2.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.1.2.2.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 16V – 24V
System load – Typical

9.1.2.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – NA

9.1.2.2.5 Test Results

By varying the AUX input, it is ensured that Buck-Boost output is 12V which in-turn ensures proper functionality of GBC module.

9.1.2.2.6 Measurement Logs

Input Voltage Range for AUX Supply										
Sl. No.	Test case No.	Input Voltage(V)	VPSOLAR (JTB10A.1)	VSLR_OVUVOUT(R1304.2)	VSLR POE_VOUT (C3M171.1)	12V_IN (R10044.2)	Specification		Margin (%)	PASS / FAIL
							Min	Max		

1	FP 2.2	16	16.04	16.04	16.02	12.08	11.76	12.12	-0.33	PASS
2	FP 2.2	18	18.03	18.03	18	12.08	11.76	12.12	-0.33	PASS
3	FP 2.2	20	20.02	20.02	20	12.08	11.76	12.12	-0.33	PASS
4	FP 2.2	22	22.02	22.02	21.99	12.08	11.76	12.12	-0.33	PASS
5	FP 2.2	24	24.01	24.01	23.99	12.08	11.76	12.12	-0.33	PASS

NOTE: Pass Criteria for Buck-Boost converter: Measured Voltage should be 12V±2%

The detailed analysis report with for PoE test cases executed is embedded in the xls document attached herewith.

AUX_IN_FP.2.xlsx

9.1.3 PoE In

9.1.3.1 Test ID / Test Name: FP.3.1 / Voltage Accuracy

9.1.3.1.1 Purpose

The purpose of this test case is to check the voltage accuracy of input side voltage rails when GBC is powered through PoE.

9.1.3.1.2 Test and Measurement Method

This test is conducted by isolating input side of Tiva and Intel microprocessor, by removing R10054 and R10067 respectively. A constant input voltage of 56V is given from PoE injector (PS-201G++) to J1A connector. Measure the output voltages at C3M103.1, C3M171.1, C1685.1 and C3M96.1. Please refer to Section **3.2.3.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.1.3.1.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +56V DC

System load –Typical

9.1.3.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – NA

9.1.3.1.5 Test Results

The input voltage accuracy of GBC when powered through PoE is within the system input voltage range as per design (10.8V to 28V).

9.1.3.1.6 Measurement Logs

PoE In - Voltage Accuracy								
Sl. No.	Test case No.	Voltage Rail	Measuring Points	Measured Voltage(V)	Specification		Design Margin (%)	PASS / FAIL
					Min(V)	Max(V)		
1	FP 3.1	PV18POE	C3M103.1	18.62	10.8	28	-33.50	PASS
2	FP 3.1	VSLRPOE_VOUT	C3M171.1	18.6	10.8	28	-33.57	PASS
3	FP 3.1	VPS_VOUT	C1685.1	18.58	10.8	28	-33.64	PASS
4	FP 3.1	VPOUT_BUCK	C3M96.1	18.53	10.8	28	-33.82	PASS

NOTE: The detailed analysis report is embedded in the xls document attached in the end of this section.

9.1.3.2 Test ID / Test Name: FP.3.2 / Input Voltage Range

9.1.3.2.1 Purpose

PoE input supply range must comply with LTPoE++ standard, i.e. it is designed to work in the range of 53.75V to 56V. The purpose of the test case is to validate the range for LTPoE++ voltage range for which GBC will be functional.

9.1.3.2.2 Test and Measurement Method

This test is conducted by varying PoE injector input voltage from 53.75V to 56V. Varying the injector supply for voltages in steps of 1V, measure the input voltage at C2005.1. Load GBC up to 30W using an external electronic load. For every change in input voltage, measure the output voltage of 48V to 18V isolated converter (U38) at C3M171.1 and should read 18V. Please refer to Section **3.2.3.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.1.3.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 53.75V to 56V

System load – Typical + External electronic load on 12V rail.

9.1.3.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – NA

9.1.3.2.5 Test Results

By varying PoE input voltage; it is ensured that output of 48V to 18V isolated converter (U38) is 18V which in-turn ensures proper functionality of GBC module.

9.1.3.2.6 Measurement Logs

PoE In - Input supply range										
Sl. No.	Test case No.	PoE input voltage (V)	VSLPOE_VOUT (at C3M171) (V)	Load current on 12 V rail(A)	Total system current (A)	Total board power consumption (W)	Specification		Design Margin (%)	PASS / FAIL
							Min(V)	Max(V)		
1	FP 3.2	53.75	18.57	1.82	0.605	32.52	17.1	18.9	-1.75	PASS
2	FP 3.2	55	18.58	1.82	0.597	32.84	17.1	18.9	-1.69	PASS
3	FP 3.2	55.5	18.57	1.82	0.59	32.75	17.1	18.9	-1.75	PASS
4	FP 3.2	56	18.57	1.82	0.587	32.87	17.1	18.9	-1.75	PASS

NOTE: Pass Criteria for input voltage range: Measured Voltage should be equal to output voltage ±5%.

The detailed analysis report for PoE test cases executed is embedded in the xls document attached herewith.

PoE_FP.3.xlsx

9.1.4 PoE – Data

9.1.4.1 Test ID / Test Name: FP.5.1 / Ethernet Compliance

9.1.4.1.1 Purpose

The purpose of this test case is to perform Ethernet Physical Layer Compliance Testing for 100BASE-TX MDI signal.

9.1.4.1.2 Test and Measurement Method

This test is conducted by generating PRBS test pattern from Marvell switch using MDC and MDIO registers and probing signals at both PD port [J1A.1 and J1A.2 (TX pair); J1A.3 and J1A.6 (RX pair)] and PSE port [J1A.13 and J1A.14 (TX pair); J1A.15 and J1A.18 (RX pair)] and perform compliance as per IEEE 802.3 standard which cover these test cases, viz. Template Test, Differential Output Voltage Test, Signal Amplitude Symmetry Test, Rise and Fall Time Test, Waveform Overshoot Test, Jitter Test, Duty Cycle Distortion Test, Return Loss Test, common Mode Rejection. The test procedure and test setup has been performed as per document embed herewith.

Ethernet compliance test procedure and te

Please refer to Section **3.2.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.1.4.1.3 Test Condition

Ambient Temperature - 25˚C
Operating Voltage - +18V DC
System load – Typical

9.1.4.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – NA

9.1.4.1.5 Test Results

Test Report for 100Base-TX

Test	Spec. Range	Measured Value	Result
AOI Template	Fit the template		Fail
Output Voltage (+Vout)	950mV to1050mV	965.4mV	Pass
Output Voltage (-Vout)	-950mV to -1050mV	-961.4mV	Pass
Amplitude Symmetry	0.98 to 1.02	1.004	Pass
Rise Time(+ve)	3ns to 5ns	5.39ns	Fail
Rise Time(-ve)	3ns to 5ns	5.32ns	Fail
Fall Time(+ve)	3ns to 5ns	5.06ns	Fail
Fall Time(-ve)	3ns to 5ns	5.23ns	Fail
Rise/Fall Symmetry(+ve)	<500ps	325ps	Pass
Rise/Fall Symmetry(-ve)	<500ps	425ps	Pass
Overshoot(+ve)	<5%	2.37%	Pass
Overshoot(-ve)	<5%	1.82%	Pass
Transmit Jitter(+ve)	<1.4ns	660ps	Pass
Transmit Jitter(-ve)	<1.4ns	1.32ns	Pass
Distortion (Duty Cycle)	<500ps(±250ps)	300ps	Pass

Transmitter Return Loss:

Frequency	Spec. Value	Measured Value			Result
		85Ohm	100Ohm	115Ohm	
1 MHz	-16.00dB	-17.22dB;	-24.79dB;	-36.20dB	Pass
10 MHz	-16.00dB	-17.74dB;	-24.68dB;	-26.79dB	Pass
20 MHz	-16.00dB	-20.72dB;	-25.24dB;	-20.71dB	Pass
30 MHz	-16.00dB	-25.39dB;	-26.85dB;	-19.26dB	Pass
40 MHz	-13.50dB	-26.57dB;	-28.08dB;	-19.41dB	Pass
50 MHz	-11.56dB	-21.41dB;	-23.05dB;	-18.59dB	Pass
60 MHz	-9.97dB	-11.37dB;	-12.09dB;	-11.73dB	Pass

Receiver Return Loss:

Frequency	Spec. Value	Measured Value			Result
		85Ohm	100Ohm	115Ohm	
1 MHz	-16.00dB	-17.05dB;	-24.32dB;	-35.91dB	Pass
10 MHz	-16.00dB	-17.40dB;	-24.58dB;	-29.64dB	Pass
20 MHz	-16.00dB	-20.33dB;	-27.74dB;	-22.63dB	Pass
30 MHz	-16.00dB	-24.55dB;	-32.09dB;	-20.64dB	Pass
40 MHz	-13.50dB	-21.66dB;	-26.10dB;	-20.36dB	Pass
50 MHz	-11.56dB	-17.62dB;	-20.62dB;	-19.26dB	Pass
60 MHz	-9.97dB	-13.34dB;	-15.30dB;	-15.72dB	Pass

NOTE:

Rise, fall time and AOI template failure are attributed to physical layout of the Ethernet channel on Rev-B design. Channel implementation has been updated in Rev C design, which includes optimized center tap routing and channel length. These optimizations are expected to address the failures and will be validated as part of Rev C product qualification.

9.1.5 Protection

9.1.5.1 Test ID / Test Name: FP.6.1 / Output Voltage Accuracy

Covered in FP.2.1

9.1.5.2 Test ID / Test Name: FP.6.2 / Solar AUX Present Test

9.1.5.2.1 Purpose

The purpose of this test case is to check the presence of Solar or AUX supply.

9.1.5.2.2 Test and Measurement Method

This test is conducted by isolating input side of Tiva and Intel microprocessor by removing R10054 and R10067 respectively. Connect an AUX supply to the input of GBC. Measure the voltage at R9957.2. When AUX or solar supply is present, the voltage on this resistor should measure <0.4V. Please refer to Section **3.2.5.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.1.5.2.3 Test Condition

Ambient Temperature - 25˚C
Operating Voltage - +18V DC
System load – Typical

9.1.5.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – NA

9.1.5.2.5 Test Results

Measuring the voltage at R9957.2 to be < 0.4V, indicates that Solar/ AUX supply is present as the input source to GBC.

9.1.5.2.6 Measurement Logs

Sl. No.	Test case No.	Voltage Rail	Measuring Points	Measured Voltage	Specification		Margin (%)	PASS / FAIL
					Min(V)	Max(V)		
1	FP 6.2	VSLRPOE_VOUT	R988.1	17.98	17.82	18.18	-0.90	PASS
2	FP 6.2	SOLAR_AUX_PRSNT_N	R9957.2	0.185	0	0.4	-53.75	PASS
3	FP 6.2	VPS_VOUT	R1056.1	17.98	17.82	18.18	-0.90	PASS

NOTE:

1) Pass Criteria for Solar_AUX_Present: Measured Voltage at R9957.2 should be < 0.4V (designed value is for <0.4V)
2) The detailed analysis report is embedded in the xls document attached in the end of this section.

9.1.5.3 Test ID / Test Name: FP.6.3 / Protection Limit

9.1.5.3.1 Purpose

The purpose of this test case is to ensure the voltage protection limits are as per the designed value, i.e. input voltage to U91 (LT4256) is ≥11.5V.

9.1.5.3.2 Test and Measurement Method

This test is conducted by isolating input side of Tiva and Intel microprocessor, by removing R10054 and R10067 respectively. Connect an AUX supply to the input of GBC. Vary the input voltage from 10.5V to 11.5V in steps of 0.2V. Measure the voltages at C3M171.1, R1053.2, R1056.1 and R10044.2. Input voltage for U91 should be greater than 11.5V for its proper operation. This test fails if input voltage of U91 (VSLRPOE_VOUT) is less than 11.5V, or if the nodal voltage at R1053 and R1052 junction is greater than 3.96V. Please refer to Section **3.2.5.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.1.5.3.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +10.5V DC to +11.5V DC

System load –Typical

9.1.5.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – NA

9.1.5.3.5 Test Results

Measuring the voltage at R1053.2 < 3.96V and input voltage to U91 greater than 11.5V indicates that U91 protects GBC at under voltages.

9.1.5.3.6 Measurement Logs

Sl. No.	Test case No.	Voltage Rail										PASS / FAIL
		VSLRPOE_VOUT @ C3M171.2	Node voltage at UV pin of U91 @ R1053.2	VPS_VOUT @ R1056.2	Specification		Design Margin (%)	12V_IN @ R10044.3	Specification		Design Margin (%)	
					Min (V)	Max (V)			Min (V)	Max (V)		
1	FP 6.3	10.5	3.672	0	0	0	0.00	0	0	0	0.00	PASS
2	FP 6.3	10.8	3.776	0	0	0	0.00	0	0	0	0.00	PASS
3	FP 6.3	11	3.846	0	0	0	0.00	0	0	0	0.00	PASS
4	FP 6.3	11.2	3.917	0	0	0	0.00	0	0	0	0.00	PASS
5	FP 6.3	11.5	4.021	11.52	11.27	11.73	-1.79	12.08	11.76	12.24	-1.31	PASS

NOTE:

Pass Criteria for Protection Circuit:

1) Voltage measured at VSLRPOE_VOUT should be ≥11.5V (11.5V is the designed value). This implies that the node voltage at R1053.2 should be >3.96V.
2) When the above two criteria are met, voltage at VPS_VOUT should be equal to VSLRPOE_VOUT and 12V_IN should be equal to ±5% of 12V (i.e. between 11.4V and 12.6V)

The detailed analysis report for PoE test cases executed is embedded in the xls document attached herewith.

Protection_FP.6.xlsx

9.2 Power:

9.2.1 PoE

9.2.1.1 Test ID / Test Name: PWR.1.1 / Voltage Accuracy

Same as test case FP.3.1

9.2.1.2 Test ID / Test Name: PWR.1.2 / Ripple Measurement

9.2.1.2.1 Purpose

The purpose of this test case is to check the maximum peak-to-peak ripple voltage of PoE supply.

9.2.1.2.2 Test and Measurement Method

This test is conducted by isolating input side of Tiva and Intel microprocessor, by removing R10054 and R10067 respectively. A constant input voltage of 56V is given from PoE injector (PS-201G++) to J1A connector. An Isolated DC-DC converter in turn converts 56V to 18V. To measure the ripple voltage, operate the oscilloscope in AC coupling mode and measure the ripple voltage across C3M103.1. Please refer to Section **4.2.1.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure

9.2.1.2.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage – PoE injector supply

System load – Idle/Typical

9.2.1.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018
Software versions – NA

9.2.1.2.5 Test Results

The ripple voltage accuracy is within 5% of expected ripple voltage.

9.2.1.2.6 Measurement Logs

PoE In - Ripple Measurement								
Sl. No.	Test case No.	Voltage Rail	Measuring Point	Ripple Voltage(mV)	Specification		Margin (%)	PASS / FAIL
					Min(mV)	Max(mV)		
1	PWR1.2	PV18POE	C3M103.1	13.2	0	900	-98.53	PASS

NOTE:

1) Supporting waveform capture is provided at end of test case id PWR 1.3

2) The detailed analysis report is embedded in the xls document attached in the end of this section.

9.2.1.3 Test ID / Test Name: PWR.1.3 /PoE Present Check

9.2.1.3.1 Purpose

The purpose of this test case is to check the presence of PoE as an input supply source.

9.2.1.3.2 Test and Measurement Method

This test is conducted by isolating input side of Tiva and Intel microprocessor, by removing R10054 and R10067 respectively. A constant input voltage of 56V is given from PoE injector (PS-201G++) to J1A connector. A DC-DC in turn converts 56V to 18V. When PoE supply is present, the voltage on R9953.2 resistor should measure <1.155V. Any voltage less than 1.155V is considered as low signal for Tiva thus indicating the presence of PoE supply. Please refer to Section **4.2.1.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.1.3.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +18V DC

System load – Idle/Typical

9.2.1.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018
Software versions – NA

9.2.1.3.5 Test Results

The voltage at R9953.2 was measured to be 0.192V.

9.2.1.3.6 Measurement Logs

PoE In - Supply Present Check								
Sl. No.	Test case No.	Voltage Rail	Measuring Point	Measured Voltage(V)	Specification		Margin (%)	PASS / FAIL
					Min(mV)	Max(mV)		
1	PWR1.3	POE_PRSNT_N	R9953.2	0.192	0	1.155	-83.38	PASS

The detailed analysis report with waveform captured for PoE test cases executed is embedded in the xls document attached herewith.

PoE.xlsx

9.2.1.4 Test ID / Test Name: PWR.1.4 / Data transfer validation

9.2.1.4.1 Purpose

This test case indicates the data validation between PoE ports A and B.

9.2.1.4.2 Test and Measurement Method

Connect Data In port of PoE injector to CPU1. Connect Port B of GBC to another machine (CPU2). Ping CPU2 from CPU1 and vice versa. Please refer to Section **4.2.1.5** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.1.4.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – AUX supply: + PoE injector supply

System load – Typical

9.2.1.4.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – NA

9.2.1.4.5 Test Results

The number of packets transferred from CPU1 to CPU2 and vice versa should have a loss of 0%, then data validation through PoE is successful.

9.2.1.4.6 Measurement Logs

PoE_Data_Validation_CPU1.JPG

PoE_Data_Validation_CPU2.jpg

9.2.1.5 Test ID / Test Name: PWR.1.5 / Power delivery

9.2.1.5.1 Purpose

The purpose of the test case is to validate the power delivery of PoE.

9.2.1.5.2 Test and Measurement Method

This test is conducted by measuring the voltage at the sense resistor R10044 and calculating the current and power for the output section. PoE Voltage and Current are measured by connecting the injector to DC power supply and measuring the voltage at the input point of injector. The efficiency is calculated as $\eta = 100\% * Pout / Pin$. Please refer to Section **4.2.1.6** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.1.5.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – PoE injector supply

System load – Typical

9.2.1.5.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – NA

9.2.1.5.5 Test Results

The efficiency is calculated to be 61.64%.

9.2.1.5.6 Measurement Logs

PoE Power Delivery										
Section	Probing points	Resistor Value (mΩ)	Voltage (V)	Measured Voltage across sense resistor (mV)	Current (A)	Power (W)	Calculated Efficiency (%)	Specification (%)		Design Margin (%)
								Min	Max	
Input Section	NA	NA	47.97	NA	0.487	23.36139				
Output Section	R10044	10	12	12	1.2	14.4	61.64	60	70	-2.73361

NOTE: PoE Voltage and Current measured by connecting the injector to DC power supply and measuring the voltage at the output point of injector.

NOTE: This test case was carried out for typical load condition. Full load condition will be tested in next version.

The detailed analysis report for power delivery of PoE is embedded in the xls document attached herewith.

PoE_Power_Delivery
.xlsx

9.2.2 Isolated DC-DC Converter

9.2.2.1 Test ID / Test Name: PWR.3.1 / Output Voltage Accuracy

9.2.2.1.1 Purpose

The purpose of this test case is to check the voltage accuracy of output voltage rail of DC – DC converter when PoE input voltage is varied.

9.2.2.1.2 Test and Measurement Method

A varying input PoE voltage from 40V to 48V is varied in steps and fed to J1A connector. Measure the input voltage at J1.A C2005.1 and output voltage of DC-DC converter at C1807.1. Please refer to Section **4.2.2.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.2.1.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +40V to +48V DC

System load –Typical

9.2.2.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – NA

9.2.2.1.5 Test Results

The output voltage accuracy of DC-DC converter when powered through varying PoE input voltage is within 5% of expected voltage.

9.2.2.1.6 Measurement Logs

Isolated DC-DC Converter -Output Voltage Accuracy								
Sl. No.	Test case No.	PoE Input Voltage (V)	VPORTA_P(V)	PV18POE	Specification		Margin (%)	PASS/ FAIL
					Min(V)	Max(V)		
1	PWR 3.1	44.2	44.2	18.58	17.1	18.9	-1.69	PASS
2	PWR 3.1	40.4	40.22	18.63	17.1	18.9	-1.43	PASS
3	PWR 3.1	47.4	47.2	18.57	17.1	18.9	-1.75	PASS

NOTE: The detailed analysis report is embedded in the xls document attached in the end of this section.

9.2.2.2 Test ID / Test Name: PWR.3.2 / Solar AUX and PoE Or'ring circuit

9.2.2.2.1 Purpose

The purpose of this test case is to check the switching between AUX/ Solar supply and PoE supply.

9.2.2.2.2 Test and Measurement Method

This test is conducted by isolating input side of Tiva and Intel microprocessor, by removing R10054 and R10067 respectively. A constant input voltage of 56V is given from PoE injector (PS-201G++) to J1A connector. A DC-DC in turn converts 56V to 18V. AUX/ Solar input supply is also given to JTB10A.1. Measure the output voltage at C3M171.1. As per design, output voltage should follow AUX/ Solar supply if AUX supply is greater than 16.3V; else output voltage will follow PoE. Please refer to Section **4.2.2.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.2.2.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +18V DC from PoE; AUX voltage range +15V DC to +24V DC

System load – Idle/Typical

9.2.2.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018
Software versions – NA

9.2.2.2.5 Test Results

From AUX or solar input voltage equal to 16.27V, the output voltage follows the input.

9.2.2.2.6 Measurement Logs

Isolated DC-DC Converter - Solar AUX and PoE OR'ing Circuit								
Sl. No.	Test case No.	Voltage Rail VSLR_OVUVOUT(V)	Voltage Rail PV18POE (V)	Measured Voltage(V)	Specification		Margin (%)	PASS/ FAIL
					Min(V)	Max(V)		
1	PWR 3.2	15	18.65	18.61	17.7175	19.5405	-4.76	PASS
2	PWR 3.2	15.7	18.65	18.61	17.7175	19.5405	-4.76	PASS
3	PWR 3.2	16.06	18.65	18.58	17.7175	19.509	-4.76	PASS
4	PWR 3.2	16.27	18.65	16.25	15.4565	17.0835	-4.88	PASS
5	PWR 3.2	17	18.65	16.97	16.15	17.85	-4.93	PASS
6	PWR 3.2	18	18.65	17.95	17.1	18.9	-4.97	PASS
7	PWR 3.2	24	18.65	23.91	22.8	25.2	-4.87	PASS
NOTE: When VSLR_OVUVOUT is between 16.12V and 16.17V; then voltage source selection is based on the first available source.								

The detailed analysis report for PoE test cases executed is embedded in the xls document attached herewith.

Isolated - DC-DC_PWR.3.xlsx

9.2.3 Lead Acid battery

9.2.3.1 Test ID / Test Name: PWR.4.1 / Output Voltage Accuracy

9.2.3.1.1 Purpose

The purpose of this test case is to check the output voltage accuracy of battery charger U82 (LTC4015).

9.2.3.1.2 Test and Measurement Method

This test is conducted by isolating input side of Tiva and Intel microprocessor, by removing R10054 and R10067 respectively. Measure the voltages at C1685.1, JTB10B.3, C1741.1, and C1686.1. Please refer to Section **4.2.3.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.3.1.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - Lead Acid battery voltage – 9.5V to 13.8V (12V nominal voltage)

System load – Idle/Typical

9.2.3.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018
Software versions – NA

9.2.3.1.5 Test Results

Measured battery voltage at various input points are within the limits.

9.2.3.1.6 Measurement Logs

Lead Acid Battery - Voltage Accuracy								
Sl. No.	Test case No.	Voltage Rail	Measuring Point	Measured Voltage(V)	Specification		Margin (%)	PASS / FAIL
					Min(V)	Max(V)		
1	PWR 4.1	VPS_VOUT	C1685.1	0	0	0	0	PASS
2	PWR 4.1	LACID_VBAT_P	JTB10B.3	12.77	10.5	13.5	-5.41	PASS
3	PWR 4.1	LT4231_BAT_CHRGR_LACID	C1741.1	12.75	12.610375	12.929625	-1.11	PASS
4	PWR 4.1	VBC_LACID	C1686.1	12.73	12.590625	12.909375	-1.11	PASS

NOTE: The detailed analysis report is embedded in the xls document attached in the end of the test case PWR.4.7.

9.2.3.2 Test ID / Test Name: PWR.4.2 / Charge current measurement

9.2.3.2.1 Purpose

Charge current for lead acid battery is designed for 10.6A.

i.e. $Charge\ current\ = \frac{32mV}{3mohm} = 10.66A$

Charge current read from register Ibat having sub-address 0x3D, must be equal to the programmed charge current (10.66A).

NOTE: Charge current will decrease when charging voltage increases.

9.2.3.2.2 Test and Measurement Method

Connect lead acid battery terminals between to JTB10B.3and JTB10B.4 Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0, lead acid battery charger U82 can be accessed. Program the charge current as 10.66A by writing into Icharge _target register at address 0x1A. Read register Ibat having sub-address 0x3D. This value gives the charging current of the lead acid battery. Repeat the same procedure for different values such as 2A, 4A, 6A and 8A as charge current for verification. Please refer to Section **4.2.3.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.3.2.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +Lead Acid Battery Voltage (12V nominal, 9.5V to 13.8V)

System load –Typical

9.2.3.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0014

Software versions – NA

9.2.3.2.5 Test Results

The register read value must be equal to the current measured across resistor R9959.

The detailed analysis report for lead acid battery charge current test case executed is embedded in the xls document attached herewith.

Lead Acid_Charge_Curren

NOTE: PASS Criteria: IBAT value read from register 0x3D and current measured across R9959 should be equal.

9.2.3.3 Test ID / Test Name: PWR.4.3 / Load current measurement

9.2.3.3.1 Purpose

The purpose of this test case is to measure the current drawn from the battery when system is powered ON by lead acid battery.

9.2.3.3.2 Test and Measurement Method

This test is conducted by isolating input side of Intel microprocessor, by removing R10067. Connect the lead acid battery at JTB10B.3.

Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0, lead acid battery charger U82 can be accessed. Read register IIN having sub-address 0x3E. This value gives the load current of GBC board.

Measure the voltage drop across R9959 (battery sense resistor).

Load current is given by $\frac{[Voltage\ across\ 9960(mV)]}{R9960(mohm)} = \frac{[Voltage\ across\ R9960(mV)]}{2}$. Please refer to Section **4.2.3.5** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.3.3.3 Test Condition

Ambient Temperature - 25˚C (Lab temperature was maintained at 25˚C during testing)
Operating Voltage – Lead Acid battery voltage
System load – Idle/Typical

9.2.3.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018
Software versions – NA

9.2.3.3.5 Test Results

The register read value must be equal to the current measured across resistor R9960.

9.2.3.3.6 Measurement Logs

The detailed analysis report for lead acid battery Load current test case executed is embedded in the xls document attached herewith.

Lead_Acid_load_current.xlsx

NOTE: PASS criteria: IIN value read from register 0x3E and current measured across R9960 should be equal.

9.2.3.4 Test ID / Test Name: PWR.4.4 / LDO Output voltage

9.2.3.4.1 Purpose

The purpose of this test case is to measure the battery charger (U82) internal $INTV_{CC}$ LDO voltage.

9.2.3.4.2 Test and Measurement Method

This test is conducted by isolating input side of Tiva and Intel microprocessor, by removing R10054 and R10067 respectively. Connect the lead acid battery at JTB10B.3. Measure the battery charger internal LDO voltage at C1767.1. Please refer to Section **4.2.3.6** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.3.4.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage – Lead Acid battery voltage

System load – Idle/Typical

9.2.3.4.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018
Software versions – NA

9.2.3.4.5 Test Results

Internal LDO voltage is measured and is within the expected limit (i.e. between 4.3V and 5.5V).

9.2.3.4.6 Measurement Logs

Lead Acid Battery - LDO Output Voltage									
Sl. No.	Test case No.	Voltage Rail	Measuring Point	Measured Voltage (V)	Expected Voltage (V)	Specification		Margin (%)	PASS/FAIL
						Min(V)	Max(V)		
1	PWR 4.4	INT_VCC_LACID	C1767.1	4.87	5	4.3	5.5	-9.09	PASS

NOTE: The detailed analysis report is embedded in the xls document attached in the end of this section.

9.2.3.5 Test ID / Test Name: PWR.4.5 / Temperature Measurement

9.2.3.5.1 Purpose

The purpose of this test case is to measure the temperature of battery charger IC U82 Microcontroller when it's fully operational.

9.2.3.5.2 Test and Measurement Method

Connect lead acid battery. Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0, lead acid battery charger, U82 can be accessed. Read register DIE_TEMPERATURE having sub-address 0x3F. Please refer to Section **4.2.3.7** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.3.5.3 Test Condition

Ambient Temperature - 23˚C

Operating Voltage – Lead Acid battery voltage

System load – Idle/Typical

9.2.3.5.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018

Software versions – NA TIVA RTOS VER.33 lead acid battery charger configuration code

9.2.3.5.5 Test Results

The measured value is well within operating temperature of U82 i.e. -40C to +125C

9.2.3.5.6 Measurement Logs

Sl. No	Register	Register Address	Hex Value	Decimal Value	Parameter	Value	Specification		Margin (%)	PASS / FAIL
							Min (deg C)	Max (deg C)		
1	DIE_TEMP	0x3F	3568	13672	LTC4015 temperature (deg C)	36.447	-40	125	191.12	PASS

The detailed analysis report with waveform captured for lead acid battery die temperature test case executed is embedded in the xls document attached herewith.

Lead Acid_temperature_m

9.2.3.6 Test ID / Test Name: PWR.4.6 / Charge control

9.2.3.6.1 Purpose

This test case indicates the programmed charge current for lead acid battery.

9.2.3.6.2 Test and Measurement Method

Connect lead acid battery at connector JTB10B. Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0, lead acid battery charger U82 can be accessed. Write the desired charge current to register 0x1A, *ICHARGE_TARGET*. Read the register 0x3D (*Ibat*) to measure the charge current. Please refer to Section **4.2.3.8** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.3.6.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – Lead Acid battery and AUX supply: +18V DC

System load – Typical

9.2.3.6.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – TIVA RTOS VER.33 lead acid battery charger configuration code

9.2.3.6.5 Test Results

The read value from register 0x3D and 0x1A should be the same.

9.2.3.6.6 Measurement Logs

Lead Acid_Charge_Contrc

NOTE: PASS criteria: Programmed value of register 0x1A should be equal to the read value from register 0x3D.

9.2.3.7 Test ID / Test Name: PWR.4.7 / Lead Acid and LiON battery or 'ring circuit

9.2.3.7.1 Purpose

The purpose of this test case is to check OR'ing between lead acid battery and lithium ion battery when solar or AUX power supply is absent. Measure the current drawn from the battery when system is powered ON by lithium ion battery.

9.2.3.7.2 Test and Measurement Method

Connect both lead acid battery and lithium ion battery. If lead acid battery measures >10.35V. lead acid battery will be selected as the power supply source. Please refer to Section **4.2.3.9** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.3.7.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage – Lithium ion battery voltage or lead acid battery

System load – Idle/Typical

9.2.3.7.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005
Software versions – NA

9.2.3.7.5 Test Results

When lead acid battery voltage is greater than 10.35V, the power source for GBC will be lead acid and is verified by this test.

9.2.3.7.6 Measurement Logs

Lead Acid and Lithium Ion Battery - OR'ing Circuit								
Sl. No	Test Case ID	VBC_ LION (V) @C3M98.1	VBC_ LACID (V) @C3M97.1	VPOUT_BUCK (V) @ C3M96.1	Specification		Margin (%)	PASS / FAIL
					Min	Max		
1	PWR.4.7	12.37	11.17	11.12	10.35	13.5	-7.44	PASS

NOTE: VPOUT_BUCK = VBC_LACID only if voltage of lead acid battery voltage is >10.35

The detailed analysis report for lead acid battery charger test cases executed is embedded in the xls document attached herewith.

Lead Acid Battery Charger.xlsx

Battery Oring ckt_PWR.4.7.xlsx

9.2.3.8 Test ID / Test Name: PWR.4.8 / Power delivery

9.2.3.8.1 Purpose

The purpose of the test case is to validate the power delivery of Lead Acid battery.

9.2.3.8.2 Test and Measurement Method

This test is conducted by measuring the voltage at the sense resistors R9959 and R10044 and calculating the current and power. The efficiency is calculated as $\eta = 100\% * Pout / Pin$. Please refer to Section **4.2.3.10** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.3.8.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.2.3.8.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – NA

9.2.3.8.5 Test Results

The efficiency is calculated to be 69.39%.

9.2.3.8.6 Measurement Logs

Lead Acid Power Delivery										
Section	Probing points	Resistor Value (mΩ)	Voltage (V)	Measured Voltage across sense resistor (mV)	Current (A)	Power (W)	Calculated Efficiency (%)	Specification (%)		Design Margin (%)
								Min	Max	
Input Section	R9959	5	11.89	0.8	0.16	1.9024				
Output Section	R10044	10	12	1.1	0.11	1.32	69.39	60	70	-0.87709

NOTE: This test case was carried out for typical load condition. Full load condition will be tested in next version.

The detailed analysis report for power delivery of Lead Acid battery is embedded in the xls document attached herewith.

Lead_Acid_Power_Delivery.xlsx

9.2.4 Lithium Ion Battery

9.2.4.1 Test ID / Test Name: PWR.5.1 / Output Voltage Accuracy

9.2.4.1.1 Purpose

The purpose of this test case is to check the output voltage accuracy of battery charger U85 (LTC4015).

9.2.4.1.2 Test and Measurement Method

This test is conducted by isolating input side of Tiva and Intel microprocessor, by removing R10054 and R10067 respectively. Measure the voltages at C1718.1, JTB8.1, C1715.1, and C1718.1. Please refer to Section **4.2.4.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.4.1.3 Test Condition

Ambient Temperature - 25˚C
Operating Voltage - AUX voltage range +16V DC to +24V DC and lithium ion battery (9V to 12.6V)
System load – Idle/Typical

9.2.4.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005
Software versions – NA

9.2.4.1.5 Test Results

Measured battery voltage at various input points are within the specified limits.

9.2.4.1.6 Measurement Logs

Lithium Ion Battery – Output Voltage Accuracy								
Sl. No.	Test case No.	Voltage Rail	Measuring Point	Measured Voltage(V)	Specification		Margin (%)	PASS / FAIL
					Min(V)	Max(V)		
1	PWR 5.1	VPS_VOUT	C1718.1	0	0	0	0	PASS
2	PWR 5.1	LION_VBAT_P	JTB8.1	11.67	11.1	12.6	-5.14	PASS

3	PWR 5.1	VBC_LION	C1715.1	11.68	11.1	12.6	-5.23	PASS

NOTE: The detailed analysis report with waveform captured is embedded in the xls document attached in the end of the test case PWR 5.5.

9.2.4.2 Test ID / Test Name: PWR.5.2 / Charge Current Measurement

9.2.4.2.1 Purpose

Charge current for lithium ion battery is designed for 1.45A.

i.e. Charge current $= \frac{32\text{mV}}{22\text{mohm}} = 1.45\text{A}$

Charge current read from register Ibat having sub-address 0x3D, must be equal to the programmed charge current (1.45A).

NOTE: Charge current will decrease when charging voltage increases.

9.2.4.2.2 Test and Measurement Method

Connect lithium ion battery terminals between to JTB8.1 and JTB8.2. Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0, lithium ion battery charger U85 can be accessed. Read register Ibat having sub-address 0x3D. This value gives the charging current of the lithium ion battery. The read value must be equal to the measured value across R10039. Please refer to Section **4.2.4.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.4.2.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage – Lithium ion battery Voltage (9V to 12.6V)

System load –Typical

9.2.4.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0014

Software versions – TIVA RTOS VER.33 code for lithium ion battery configuration

9.2.4.2.5 Measurement Logs

Lithium_Ion_Battery Logs.xlsx

NOTE: PASS Criteria: Measured value across R10039 and read value from register 0x3D must be equal

9.2.4.3 Test ID / Test Name: PWR.5.3 / Load current measurement

9.2.4.3.1 Purpose

The purpose of this test case is to measure the current drawn from the battery when system is powered ON by lithium ion battery.

9.2.4.3.2 Test and Measurement Method

Connect lead acid battery. Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0, lithium ion battery charger U85 can be accessed. Read register IIN having sub-address 0x3E. IIN register outputs the value of total load current. Please refer to Section **4.2.4.5** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.4.3.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage – Lithium ion battery voltage

System load – Idle/Typical + External electronic load

9.2.4.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005
Software versions – TIVA RTOS VER.33 code for lithium ion battery configuration

9.2.4.3.5 Test Results

Current measured across R9961 must be equal to value read from register 0x3E.

9.2.4.3.6 Measurement Logs

Lithium_Ion_Battery Logs.xlsx

NOTE: PASS Criteria: Measured value across R9961 and read value from register 0x3E must be equal

9.2.4.4 Test ID / Test Name: PWR.5.4 / LDO Output Voltage

9.2.4.4.1 Purpose

The purpose of this test case is to ensure the internal LDO output voltage of Lithium Ion battery charger U85 must be equal to 5V.

9.2.4.4.2 Test and Measurement Method

Connect Lithium Ion battery terminals between to JTB8.1 and JTB8.2. Measure the battery charger U85 internal LDO output voltage at C1765.1. The above measured voltage should be equal to 5V to ensure proper functionality of GBC module. Please refer to Section **4.2.4.6** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.4.4.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage – Lithium ion battery Voltage (9V to 12.6V)

System load –Typical

9.2.4.4.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0014

Software versions – NA

9.2.4.4.5 Test Result

Measured LDO voltage is within the prescribed limit.i.e. between 4.3V and 5.5V

9.2.4.4.6 Measurement Logs

Lithium Ion Battery - LDO Output Voltage									
Sl. No.	Test case No.	Voltage Rail	Measuring Point	Measured Voltage(V)	Expected Voltage(V)	Specification		Margin %	PASS/FAIL
						Min(V)	Max(V)		
1	PWR 5.4	INT_VCC_LION	C1765.1	5.037	5	4.3	5.5	-9.09	PASS

9.2.4.5 Test ID / Test Name: PWR.5.5 / Temperature Measurement

9.2.4.5.1 Purpose

The purpose of this test case is to measure the temperature of battery charger IC U85 when it's fully operational.

9.2.4.5.2 Test and Measurement Method

Connect lithium ion battery terminals between to JTB8.1and JTB8.2 Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0, lithium ion battery charger U85 can be accessed. Read register DIE_TEMPERATURE having sub-address 0x3F. Please refer to Section **4.2.4.7** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.4.5.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage – Lithium ion battery Voltage (9V to 12.6V)

System load –Typical

9.2.4.5.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0014

Software versions – TIVA RTOS VER.33 code for lithium ion battery configuration

9.2.4.5.5 Test Result

Read temperature is within the prescribed limits of the lithium ion battery, U85 IC.

9.2.4.5.6 Measurement Logs

Sl.No	Register	Register Address	Hex Value	Decimal Value	Parameter	Value	Specification		Margin(%)	PASS / FAIL
							Min(deg C)	Max(deg C)		
1	DIE_TEMP	0x3F	35c1	13761	LTC4015 temperature (deg C)	38.399	-40	125	196.00	PASS


Lithium_Ion_battery
_Charger.xlsx


lithium
ion_temperature_me

9.2.4.6 Test ID / Test Name: PWR.5.6 / Charge control (JEITA)

9.2.4.6.1 Purpose

This test case indicates the current at which the lithium ion battery should be charged at a given temperature.

9.2.4.6.2 Test and Measurement Method

Connect lithium ion battery at connector JTB8. Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0 lithium ion battery charger U85 can be accessed. Write to registers from JEITA_T1 (sub- address 0x1F) to JEITA_T6 (sub- address 0x24) with temperature range from 0◦C to 60◦C. Read register *DIE_TEMP* (sub-address 0x3F) to know the temperature. The battery should charge with a current corresponding to the measured temperature. Measure the charging current by measuring voltage across R10039. Charging current can be calculated by $Charging\ Current = \frac{measured\ voltage(mV)}{22}$. Also read the register *IBAT* (sub-address 0x3D). Please refer to Section **4.2.4.8** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.4.6.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – Lithium Ion battery + AUX supply: +18V DC
System load – Typical

9.2.4.6.4 DUT Sample Information

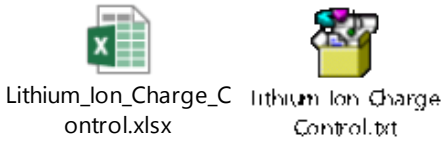
GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – TIVA RTOS VER.33 code for lithium ion battery configuration

9.2.4.6.5 Test Results

The value read by register 0x3D and the measured current across resistor R10039, should be same.

9.2.4.6.6 Measurement Logs



9.2.4.7 Test ID / Test Name: PWR.5.7 / Lion – Lead Acid and LiON battery or ‘ing circuit

9.2.4.7.1 Purpose

The purpose of this test case is to check or ‘ing between lithium ion and lead acid battery when solar or AUX power supply is absent.

9.2.4.7.2 Test and Measurement Method

Connect both lead acid battery and lithium ion battery. If lead acid battery measures <10.35V, lithium ion battery will be selected as the power supply source. Please refer to Section **4.2.4.9** in latest version of “OC_CONNECT_1_GBC_Test_Specification” document for detailed test procedure.

9.2.4.7.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage – Lithium ion battery voltage or lead acid battery

System load – Idle/Typical

9.2.4.7.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005
Software versions – NA

9.2.4.7.5 Test Results

When lead acid battery voltage is greater than 10.35V, the power source for GBC will be from lead acid and is verified by this test.

9.2.4.7.6 Measurement Logs

Lead Acid and Lithium Ion Battery - OR’ing Circuit							
		VBC_LION(V)	**VBC_LACID(V)**		**Specification**		

Sl. No	Test Case ID	@C3M97.1	@C3M98.1	VPOUT_BUCK (V) @ C3M96.1	Min	Max	Margin (%)	PASS / FAIL
1	PWR.5.7	12.38	10.3	12.37	11.1	13.5	-8.37	PASS

NOTE: VPOUT_BUCK = VBC_LION only if voltage of lead acid battery voltage is < 10.35

Battery Oring ckt_PWR.5.7.xlsx

9.2.4.8 Test ID / Test Name: PWR.5.8 / Charge time

9.2.4.8.1 Purpose

This test case indicates the total time for which lithium ion is in charging phase.

9.2.4.8.2 Test and Measurement Method

Connect lithium ion battery at connector JTB8. Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0 lithium ion battery charger U85 can be accessed. Read register *MAX_CHARGE_TIMER* having sub-address 0x30. This register outputs the value of total time (in seconds) the lithium ion battery is in charging state. Please refer to Section **4.2.4.10** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.4.8.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – Lithium Ion battery + AUX supply: +18V DC
System load – Typical

9.2.4.8.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0005

Software versions – TIVA RTOS VER.33 code for lithium ion battery configuration

9.2.4.8.5 Test Results

By reading the register 0x30, it is validated that charge time read equals to the actual time of charging of lithium ion battery. , i.e. 618 seconds (10 min 30 seconds)

9.2.4.8.6 Measurement Logs

9.2.4.9 Test ID / Test Name: PWR.5.9 / Power delivery

9.2.4.9.1 Purpose

The purpose of the test case is to validate the power delivery of Lithium Ion Battery.

9.2.4.9.2 Test and Measurement Method

This test is conducted by measuring the voltage at the sense resistors R10039 and R10044 and calculating the current and power. The efficiency is calculated as η = 100% * Pout / Pin. Please refer to Section **4.2.4.11** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.4.9.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.2.4.9.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – NA

9.2.4.9.5 Test Results

The efficiency is calculated to be 64.64%.

9.2.4.9.6 Measurement Logs

Lithium Ion Power Delivery										
Section	Probing points	Resistor Value (mΩ)	Voltage (V)	Measured Voltage across sense	Current (A)	Power (W)	Calculated Efficiency (%)	Specification (%)		Design Margin (%)
								Min	Max	

				resistor (mV)						
Input Section	R10039	22	12.48	3.6	0.164	2.042				
Output Section	R10044	10	12	1.1	0.110	1.320	64.64	60	70	-7.66178

NOTE: This test case was carried out for typical load condition. Full load condition will be tested in next version.

The detailed analysis report for power delivery of Lithium Ion battery is embedded in the xls document attached herewith.

Lithium Ion_Power_Delivery.:

9.2.5 Buck-Boost

9.2.5.1 Test ID / Test Name: PWR.6.1 / Line regulation

9.2.5.1.1 Purpose

The purpose of this test case is to check the ability of the Buck-Boost converter to maintain its specified output voltage over changes in the input line voltage.

9.2.5.1.2 Test and Measurement Method

This test is conducted by isolating input side of buck-boost converter (U88) by removing R10071 resistor and connecting and external DC power supply. Isolate input side of Tiva and Intel microprocessor, by removing R10054 and R10067 respectively. The input voltage is then varied in steps and output voltage is measured at R10044.2. Validate the output voltage accuracy at each step. Please refer to Section **4.2.5.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.5.1.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +9V DC to 22V DC

System load – Idle/Typical

9.2.5.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018

Software versions – NA

9.2.5.1.5 Test Results

The output voltage accuracy of buck boost converter is within 2% of expected voltage under various supply input and load conditions.

9.2.5.1.6 Measurement Logs

Line regulation without electronic load (Probed at C1800)						
Supply Voltage (V)	Output Current (A)	Output Voltage (V)	Specification		Margin (%)	Pass/Fail
			Min(V)	Max(V)		
9	0.04	11.92	11.76	12.24	-1.36	PASS
11.1	0.04	11.93	11.76	12.24	-1.45	PASS
12.6	0.04	11.94	11.76	12.24	-1.53	PASS
16	0.04	12.01	11.76	12.24	-1.88	PASS
18	0.04	12.03	11.76	12.24	-1.72	PASS
20	0.04	12.03	11.76	12.24	-1.72	PASS
22	0.04	12.04	11.76	12.24	-1.63	PASS

Line regulation with electronic load (Probed at C1800)							
Supply Voltage (V)	Load Current (A)	Output Current (A)	Output Voltage (V)	Specification		Margin (%)	Pass/Fail
				Min(V)	Max(V)		
9	0.5	0.68	11.98	11.76	12.24	-1.87	PASS
9	1	1.35	11.99	11.76	12.24	-1.96	PASS
9	1.5	2.05	11.98	11.76	12.24	-1.87	PASS
11.1	0.5	0.59	11.99	11.76	12.24	-1.96	PASS
11.1	1	1.12	12	11.76	12.24	-1.96	PASS
11.1	1.5	1.67	11.99	11.76	12.24	-1.96	PASS
12.6	0.5	0.51	11.99	11.76	12.24	-1.96	PASS
12.6	1	0.98	11.99	11.76	12.24	-1.96	PASS
12.6	1.5	1.47	12	11.76	12.24	-1.96	PASS
16	0.5	0.39	11.99	11.76	12.24	-1.96	PASS
16	1	0.78	11.96	11.76	12.24	-1.70	PASS
16	1.5	1.16	12.05	11.76	12.24	-1.55	PASS
18	0.5	0.36	12.02	11.76	12.24	-1.80	PASS
18	1	0.69	12.03	11.76	12.24	-1.72	PASS
18	1.5	1.04	12.06	11.76	12.24	-1.47	PASS
20	0.5	0.33	12.04	11.76	12.24	-1.63	PASS

20	1	0.64	12.05	11.76	12.24	-1.55	PASS
20	1.5	0.94	12.1	11.76	12.24	-1.14	PASS
22	0.5	0.3	12.01	11.76	12.24	-1.88	PASS
22	1	0.58	12.04	11.76	12.24	-1.63	PASS
22	1.5	0.86	12.06	11.76	12.24	-1.47	PASS

The detailed analysis report with waveform captured for Buck-Boost Line Regulation test case executed is embedded in the xls document attached herewith.

Buck-Boost_line_regulation.xlsx

9.2.5.2 Test ID / Test Name: PWR.6.2 / Load regulation

9.2.5.2.1 Purpose

The purpose of this test case is to check the capability of Buck-Boost converter to maintain a constant output voltage over changes in the load.

9.2.5.2.2 Test and Measurement Method

This test is conducted by isolating input side of buck-boost converter (U88) by removing R10071 resistor and connecting and external DC power supply. Isolate input side of Tiva and Intel microprocessor, by removing R10054 and R10067 respectively. The input voltage is then varied in steps and output voltage is measured at R10044.2. Connect an external load at R10063.1 and vary in steps of 0.5A. Please refer to Section **4.2.5.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.5.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Idle/Typical

9.2.5.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018

Software versions – NA

9.2.5.2.5 Test Results

The output voltage accuracy of buck boost converter is within 2% of expected voltage under various load conditions.

9.2.5.2.6 Measurement Logs

Load Regulation (Input Voltage - 18V)						
Load Current (A)	Output Current (A)	Output Voltage (V) (avg)	Specification		Margin (%)	Pass/Fail
			Min(V)	Max(V)		
0.5	0.39	11.88	11.76	12.24	-1.02	PASS
1	0.73	11.87	11.76	12.24	-0.94	PASS
1.5	1.07	11.89	11.76	12.24	-1.11	PASS

The detailed analysis report with waveform captured for Buck-Boost Load Regulation test case executed is embedded in the xls document attached herewith.

Buck-Boost_load_regulation.xlsx

9.2.5.3 Test ID / Test Name: PWR.6.3 / Ripple measurement

9.2.5.3.1 Purpose

The purpose of this test case is to check the maximum peak-to-peak ripple voltage of Buck-Boost converter output under different load conditions and input voltage.

9.2.5.3.2 Test and Measurement Method

This test is conducted by isolating input side of buck-boost converter (U88) by removing R10071 resistor and connecting and external DC power supply. Isolate input side of Tiva and Intel microprocessor, by removing R10054 and R10067 respectively. The input voltage is then varied in steps and output voltage is measured at R10044.2. Connect an external load at R10063.1 and vary in steps of 0.5A. Setting oscilloscope in AC coupling mode, measure the ripple voltage across C1800. Please refer to Section **4.2.5.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.5.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Idle/Typical/Full

9.2.5.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018

Software versions – NA

9.2.5.3.5 Test Results

The maximum peak-to-peak ripple voltage measured is found to be less than 5% of the input voltage.

9.2.5.3.6 Measurement Logs

Ripple Measurement for line regulation						
Supply Voltage (V)	Load Current (A)	Ripple Voltage (mV)	Specification		Design Margin (%)	Pass/Fail
			Min(mV)	Max(mV)		
9	0.5	52	0	450	-88.44	PASS
9	1	62	0	450	-86.22	PASS
9	1.5	64	0	450	-85.78	PASS
11.1	0.5	44	0	555	-92.07	PASS
11.1	1	58	0	555	-89.55	PASS
11.1	1.5	56	0	555	-89.91	PASS
12.6	0.5	44	0	630	-93.02	PASS
12.6	1	50	0	630	-92.06	PASS
12.6	1.5	52	0	630	-91.75	PASS
16	0.5	24	0	800	-97.00	PASS
16	1	24	0	800	-97.00	PASS
16	1.5	25	0	800	-96.88	PASS
18	0.5	29	0	900	-96.78	PASS
18	1	28	0	900	-96.89	PASS
18	1.5	29	0	900	-96.78	PASS
20	0.5	31	0	1000	-96.90	PASS
20	1	30	0	1000	-97.00	PASS
20	1.5	30	0	1000	-97.00	PASS
22	0.5	33	0	1100	-97.00	PASS
22	1	34	0	1100	-96.91	PASS
22	1.5	34	0	1100	-96.91	PASS

The detailed analysis report with waveform captured for Buck-Boost Ripple measurement test case executed is embedded in the xls document attached herewith.

Buck-Boost_Ripple_ measurement.xlsx

9.2.5.4 Test ID / Test Name: PWR.6.4 / Load Current Measurement

9.2.5.4.1 Purpose

The purpose of this test case is to measure the current drawn by Buck-Boost Converter when it is fully operational.

9.2.5.4.2 Test and Measurement Method

This test is conducted by measuring voltage across sense resistor R10044 (0.01ohm). The measured value is then used to derive current drawn by the system. Please refer to Section **4.2.5.5** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.5.4.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Idle/Typical

9.2.5.4.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – NA

9.2.5.4.5 Test Results

The current drawn by the Buck-Boost is close to typical current consumption of Intel (600mA), TIVA (120mA) and miscellaneous IC's.

9.2.5.4.6 Measurement Logs

Buck-Boost converter - Load Current measurement					
		Current (A)	Specification		Pass/Fail

Voltage across sense resistor R10044	Resistance (ohm)		Min	Max	Design Margin (%)	
7.638 mV	0.01	0.7638	0.4	0.8	-4.53	PASS

The detailed analysis report with waveform captured for Buck-Boost Load Current Measurement test case executed is embedded in the xls document attached herewith.

PWR.6.4_BuckBoost _LoadCurrent.xls

9.2.5.5 Test ID / Test Name: PWR.6.5 / Temperature Measurement

9.2.5.5.1 Purpose

The purpose of this test case is to measure the operating junction temperature of Buck Boost converter when it's fully operational under ambient temperature.

9.2.5.5.2 Test and Measurement Method

This test is conducted by measuring the case temperature via using Fluke 59 Mini IR Thermometer measured on U88.And then calculating junction operating temperature using the below formula:

$$T_j = T_c + R_{th(j-c)} \times P$$

Tc : Case temperature*
Rth(j-c) : Thermal resistance between Junction - Case
P : Current consumption **

The derived operating junction temperature value is well within operating temperature range of the device. Please refer to Section **4.2.5.6** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.5.5.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.2.5.5.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018

Software versions – NA

9.2.5.5.5 Test Results

The temperature measured at the Buck Boost converter is well within the designed spec.

9.2.5.5.6 Measurement Logs

Temperature Measurement						
Measuring point	Case Temperature (degree Celsius)	Calculated operating junction temperature (degree Celsius)	Specification (degree Celsius)		Design Margin (%)	Pass/Fail
			Min	Max		
U88	45.17	53.05	-40	125	232.63	PASS

The detailed analysis report with waveform captured for each of the Buck Boost temperature measurement test cases executed is embedded in the xls document attached herewith.

Buck-Boost_temp_measurement.xlsx

9.2.6 TIVA Power Supply

9.2.6.1 Test ID / Test Name: PWR.7.3 / Ripple measurement

9.2.6.1.1 Purpose

The purpose of this test case is to check the maximum peak-to-peak ripple voltage of DC-DC converter output under different load conditions and input voltage.

9.2.6.1.2 Test and Measurement Method

This test is conducted by isolating both input and output side of DC-DC converter (U70) by removing relevant resistors. The load connected is varied for different currents along with input voltage. Please refer to Section **4.2.6.2** in latest version of “OC_CONNECT_1_GBC_Test_Specification” document for detailed test procedure.

9.2.6.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Idle/Typical/Full

9.2.6.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – NA

9.2.6.1.5 Test Results

The maximum peak-to-peak ripple voltage measured is found to be less than 10mVp-p of the output voltage.

9.2.6.1.6 Measurement Logs

Ripple Measurement for TIVA power supply						
		Ripple Voltage (mV)	Specification		Design Margin (%)	Pass/Fail
Supply Voltage (V)	Measuring Point		Min(mV)	Max(mV)		
18	C502	6.3	0	10	-37	PASS

NOTE: The detailed analysis report with waveform captured is embedded in the xls document attached in the end of this section.

9.2.6.2 Test ID / Test Name: PWR.7.4 / Load Current Measurement

9.2.6.2.1 Purpose

The purpose of this test case is to measure the current drawn by TIVA microcontroller when it's fully operational.

9.2.6.2.2 Test and Measurement Method

This test is conducted by measuring voltage across shunt resistor R10054 (0.002ohm). The measured value is 0.26mV. So the current drawn by the device is 130mA. The same has been validated by reading through I2C. Please refer to Section **4.2.6.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.6.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.2.6.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – NA

9.2.6.2.5 Test Results

The current drawn by the TIVA controller is within the designed spec.

9.2.6.2.6 Measurement Logs

Load current Measurement for Tiva power supply								
Voltage across shunt (mV)	Measuring Point	Resistance (Ohm)	Current (mA)	Read Value through I2C (mA)	Specification (mA)		Design Margin (%)	Pass/Fail
					Min	Max		
0.26	R10054	0.002	130	137	120	140	-5.11	PASS

NOTE:

1) PASS criteria – Calculated value must be equal to read value through I2C.
2) The detailed analysis report with waveform captured is embedded in the xls document attached in the end of this section.

9.2.6.3 Test ID / Test Name: PWR.7.5 / Temperature Measurement

9.2.6.3.1 Purpose

The purpose of this test case is to measure the operating junction temperature of TIVA microcontroller when it's fully operational and under ambient temperature.

9.2.6.3.2 Test and Measurement Method

This test is conducted by measuring the temperature via using Fluke 59 Mini IR Thermometer measured on U72. And then calculating junction operating temperature using the below formula:

$$T_j = T_c + R_{th(j-c)} \times P$$

Tc : Case temperature*
Rth(j-c) : Thermal resistance between Junction - Case
P : Current consumption **

The derived operating junction temperature value is well within operating temperature of the device. Please refer to Section **4.2.6.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.6.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.2.6.3.4 DUT Sample Information

GBC Board Serial Number – PT11605002

Software versions – NA

9.2.6.3.5 Test Results

The temperature measured at the TIVA controller is well within the designed spec.

9.2.6.3.6 Measurement Logs

Temperature Measurement						
Case Temperature (degree Celsius)	Measuring Point	Calculated operating junction temperature (degree Celsius)	Specification (degree Celsius)		Design Margin (%)	Pass/Fail
			Min	Max		
41	U72	46.05	-40	85	215.13	PASS

The detailed analysis report with waveform captured for each of the TIVA power supply test case executed is embedded in the xls document attached herewith.

TIVA power supply Measurement Logs \

9.2.7 FET Switch

9.2.7.1 Test ID / Test Name: PWR.9.3 / Ripple Measurement

9.2.7.1.1 Purpose

The purpose of this test case is to check the maximum peak-to-peak ripple voltage of FET switch.

9.2.7.1.2 Test and Measurement Method

To measure the ripple voltage, coupling mode is changed to AC and Bandwidth to 20M in oscilloscope. Ripple voltage is measured across the capacitor C1A4. Please refer to Section **4.2.7.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.7.1.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +18V DC

System load – Idle/Typical

9.2.7.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – NA

9.2.7.1.5 Test Results

The ripple voltage accuracy is within 5% of expected ripple voltage.

9.2.7.1.6 Measurement Logs

FET switch - Ripple Measurement						
Voltage Rail	Measuring Point	Ripple Voltage(mV)	Specification		Design Margin (%)	Pass/Fail
			Min (mV)	Max (mV)		
V12_A	C1A4	27	0	600	-95.5	PASS

The detailed analysis report with waveform captured for FET switch Ripple Measurement test case executed is embedded in the xls document attached herewith.

PWR.9.3 FETswitch_RippleMe

9.2.7.2 Test ID / Test Name: PWR.9.4 / Load Current Measurement

9.2.7.2.1 Purpose

The purpose of this test case is to measure the current drawn by FET switch when it is fully operational.

9.2.7.2.2 Test and Measurement Method

This test is conducted by measuring voltage across shunt resistor R10067 (0.002ohm). The measured value is then used to derive current drawn by the system. The same has been validated by reading through I2C. Please refer to Section **4.2.7.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.7.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.2.7.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – NA

9.2.7.2.5 Test Results

The current drawn by the FET switch is within the designed spec.

9.2.7.2.6 Measurement Logs

FET switch - Load Current Measurement								
Voltage across shunt resistor R10067	Measurement Point	Resistance (ohm)	Current (A)	Read Through I2C	Specification		Design Margin (%)	Pass/Fail
					Min	Max		
1.230 mV	R10067	0.002	0.615	0.556 A	0.605	0.625	10.61	FAIL

NOTE:

1) Resolution for failure - Changed the TIVA configuration settings. The read current readings is now matching with the actual drawn current
2) PASS criteria – Calculated value must be equal to read value through I2C.

The detailed analysis report with waveform captured for FET switch Load Current Measurement test case executed is embedded in the xls document attached herewith.

PWR.9.4_FETswitch_
LoadCurrent.xls

9.2.7.3 Test ID / Test Name: PWR.9.5/ Temperature Measurement

9.2.7.3.1 Purpose

The purpose of this test case is to measure the operating junction temperature of FET switch U248 when it is fully operational.

9.2.7.3.2 Test and Measurement Method

This test is conducted by measuring the temperature via using Fluke 59 Mini IR Thermometer measured on U248. And then calculating junction operating temperature using the below formula:

$$T_j = T_c + R_{th(j-c)} \times P$$

Tc : Case temperature*
Rth(j-c) : Thermal resistance between Junction - Case
P : Current consumption **

The derived operating junction temperature value is well within range of operating temperature of the device. Please refer to Section **4.2.7.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.7.3.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage –18V

System load – Idle/Typical

9.2.7.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021
Software versions – NA

9.2.7.3.5 Test Results

The measured value is well within operating temperature of the device.

9.2.7.3.6 Measurement logs

Temperature Measurement of FET Switch						
Case Temperature (degree Celsius)	Measurement Point	Calculated operating junction temperature (degree Celsius)	Specification (degree Celsius)		Design Margin (%)	Pass/Fail
			Min	Max		
44.2	U248	49	-40	125	222.50	PASS

The detailed analysis report with waveform captured for FET switch Temperature Measurement test case executed is embedded in the xls document attached herewith.

FET_Switch_tempera
ture_measurement_lc

9.2.8 PMIC

9.2.8.1 Test ID / Test Name: PWR.10.2 / Voltage accuracy of all output voltages

9.2.8.1.1 Purpose

The purpose of the test case is to measure the output voltage rails of PMIC and to ensure that these voltages are in specified limits for the proper operation of Intel SoC.

9.2.8.1.2 Test and Measurement Method

This test is conducted by probing at appropriate locations to measure the voltage rails as depicted in the below table. The measured values are in-line to Intel SoC requirement and should match with the pre-programmed voltages as per IDT9145-I0 specification. Please refer to Section **4.2.8.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.8.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.2.8.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – NA

9.2.8.1.5 Test Results

The measured values match with the pre-programmed voltages as per IDT9145-I0 specification.

9.2.8.1.6 Measurement Logs

PMIC Output Supply Accuracy						
Voltage Rail	Measuring Points	Output Voltage (V)	Specification		Margin (%)	Pass/Fail
			Min(V)	Max(V)		
V1P8_A	C3M17	1.792	1.764	1.836	-1.59	PASS
VDDQ	C4M10	1.345	1.323	1.377	-1.66	PASS
V5_A	C3M24	5.08	4.9	5.1	-0.39	PASS
V1P5_S	C3M8	1.495	1.47	1.53	-1.70	PASS
VSFR_SX	C3M30	1.345	1.323	1.377	-1.66	PASS
V1P35_S	C3M22	1.342	1.323	1.377	-1.44	PASS
V1P2_A	C2N9	1.245	1.225	1.275	-1.63	PASS
V1P2_S	C2N11	1.244	1.225	1.275	-1.55	PASS
VTT_DDR	C4P17	0.664	0.62775	0.72225	-5.77	PASS
V1P8_IFSUP	C1B7	1.793	1.764	1.836	-1.64	PASS
VUSBPHY	C3M10	3.283	3.234	3.366	-1.52	PASS
V3P3_A	C3M11	3.293	3.234	3.366	-1.82	PASS
VCC_S	C2B34	0.91	0.98	1.02	7.14	FAIL
VNN_S	C2B1	0.948	0.931	0.969	-1.83	PASS
VDDQ	C1B4	1.343	1.323	1.377	-1.51	PASS
V1P05_S	C3M180	1.057	1.029	1.071	-1.31	PASS
V1P0_A	C3M19	1	0.98	1.02	-1.96	PASS
V12_A	C3L18	12.09	11.76	12.24	-1.23	PASS

NOTE: Failure is attributed to IDT9145 PMIC and is addressed with IDT9180 PMIC. Rev C design now uses IDT9180 PMIC.

The detailed analysis report with waveform captured for PMIC voltage accuracy Measurement test case executed is embedded in the xls document attached herewith.

PMIC.xlsx

9.2.8.2 Test ID / Test Name: PWR.10.3/ Secondary supplies enable functionality

9.2.8.2.1 Purpose

The purpose of the test case is to validate secondary supply rails of PMIC by checking status of dependency rails with respect to change in status (high or low).

9.2.8.2.2 Test and Measurement Method

Impact of High level status of PMIC_SLP_S0IX is verified by measuring dependency power rails VSFRX and V1P0SX_EN at appropriate locations as mentioned in the below table and ensuring those are enabled. Upon which remove R1B22 to make PMIC_SLP_S0IX low and ensure dependency power rails VSFRX and V1P0SX_EN are disabled. Please refer to Section **4.2.8.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.8.2.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.2.8.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – NA

9.2.8.2.5 Test Results

This test case verifies the impact of Secondary power supplies on dependency power rails as per the IDT9145 specification.

9.2.8.2.6 Measurement Logs

Secondary supplies enable functionality							
Power rail	Power rail Status	Dependency rails	Measuring Points	Dependency rail status	Specification	Design Margin (%)	Pass/Fail
					Expected rail status		
PMIC_SLP_S0IX	High	VSFRX	C3M30	Enable	Enable	NA	PASS
		V1P0SX_EN	C3B21	Enable	Enable		PASS
	Low	VSFRX	C3M30	Disable	Disable		PASS
		V1P0SX_EN	C3B21	Disable	Disable		PASS
PMIC_SLP_S3	High	V1P05_S	c3M180	Enable	Enable		PASS
		V1P02_S	C2N11	Enable	Enable		PASS
		V1P5_S	C3M8	Enable	Enable		PASS
		V1P35_S	C3M22	Enable	Enable		PASS

	Low	V1P05_S	c3M180	Disable	Disable		PASS
		V1P02_S	C2N11	Disable	Disable		PASS
		V1P5_S	C3M8	Disable	Disable		PASS
		V1P35_S	C3M22	Disable	Disable		PASS

9.2.8.3 Test ID / Test Name: PWR.10.5/ PMIC debug circuit functionality

9.2.8.3.1 Purpose

The purpose of the test case is to validate debug circuit of PMIC.

9.2.8.3.2 Test and Measurement Method

This test case is conducted by probing dependency power rails of PMIC_SLP_S0IX and PMIC_SLP_S3 at appropriate locations as depicted in below table. High level status of PMIC_THERMTRIP is checked in debug circuit by removing R4M16 to isolate PMIC_THERMTRIP from Intel SOC and ensure all the power rails are turned on. Please refer to Section **4.2.8.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.8.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.2.8.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – NA

9.2.8.3.5 Test Results

The debug circuit functionality is verified and validated

9.2.8.3.6 Measurement Logs

PMIC debug circuit functionality							
Power rail		Dependency rails	Measuring Points	Dependency rail status	Specification		Pass/Fail

	Power rail Status				Expected rail status	Design Margin (%)	
PMIC_SLP_S0IX	High	VSFRX	C3M30	Enable	Enable		PASS
		V1P0SX_EN	C3B21	Enable	Enable		PASS
	Low	VSFRX	C3M30	Disable	Disable		PASS
		V1P0SX_EN	C3B21	Disable	Disable		PASS
PMIC_SLP_S3	High	V1P05_S	C3M180	Enable	Enable		PASS
		V1P02_S	C2N11	Enable	Enable		PASS
		V1P5_S	C3M8	Enable	Enable		PASS
		V1P35_S	C3M22	Enable	Enable	NA	PASS
	Low	V1P05_S	C3M180	Disable	Disable		PASS
		V1P02_S	C2N11	Disable	Disable		PASS
		V1P5_S	C3M8	Disable	Disable		PASS
		V1P35_S	C3M22	Disable	Disable		PASS
PMIC_THERMTRIP	High	All Power rails		Enable	Enable		PASS
	Low	All Power rails		Disable	Disable		PASS

9.2.9 System Power sequence

9.2.9.1 Test ID / Test Name: PWR.11.1 / Power-up

9.2.9.1.1 Purpose

The purpose of the test case is to validate the Power-up sequence of the system including GBC and RF-SDR board.

9.2.9.1.2 Test and Measurement Method

This test is conducted by probing the signals “ATOM_12V_ONOFF” (Intel atom) and “TRXFE_12V_ONOFF” (RF-SDR) at R10753 and R10580 respectively. The power sequence is measured while powering on the system. Please refer to Section **4.2.9.2** in latest version of “OC_CONNECT_1_GBC_Test_Specification” document for detailed test procedure.

9.2.9.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.2.9.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0010

Debug board Serial Number - WZ1628LIFE2DEBUG0018

Software versions – TIVA RTOS code

9.2.9.1.5 Test Results

Power up sequence is verified and is in the following order.

1. Intel atom
2. RF-SDR

9.2.9.1.6 Measurement Logs

Sl.No	Measuring Point	Measured sequence	Specification	Design Margin (%)	Result
			Expected sequence		
System power-up sequence					
1	R10753	ATOM_12V_ONOFF	ATOM_12V_ONOFF	NA	PASS
2	R10580	TRXFE_12V_ONOFF	TRXFE_12V_ONOFF		

NOTE: There is no time delay requirement for the power up sequence.

The detailed analysis report with waveform captured for system power up sequence is embedded in the xls document attached herewith.

System_Power-up_Sequence.xlsx

9.2.9.2 Test ID / Test Name: PWR.11.2 / Power-down

9.2.9.2.1 Purpose

The purpose of the test case is to validate the Power-down sequence of the system including GBC and RF-SDR board.

9.2.9.2.2 Test and Measurement Method

This test is conducted by probing the signals “ATOM_12V_ONOFF” (Intel atom) and “TRXFE_12V_ONOFF” (RF-SDR) at R10753 and R10580 respectively. The power sequence is measured

while powering off the system. Please refer to Section **4.2.9.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.9.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.2.9.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0010

Debug board Serial Number - WZ1628LIFE2DEBUG0018

Software versions – TIVA RTOS code

9.2.9.2.5 Test Results

Power down sequence is verified and is in the following order.

1. RF-SDR
2. Intel atom

9.2.9.2.6 Measurement Logs

Sl.No	Measuring Point	Measured sequence	Specification	Design Margin (%)	Result
			Expected sequence		
System power-down sequence					
1	R10580	TRXFE_12V_ONOFF	TRXFE_12V_ONOFF	NA	PASS
2	R10753	ATOM_12V_ONOFF	ATOM_12V_ONOFF		

NOTE: There is no time delay requirement for the power down sequence.

The detailed analysis report with waveform captured for system power down sequence is embedded in the xls document attached herewith.

System_Power-down_Sequence.xlsx

9.2.9.3 Test ID / Test Name: PWR.11.3 / Soft Reset

9.2.9.3.1 Purpose

The purpose of the test case is to validate the soft reset for the system.

9.2.9.3.2 Test and Measurement Method

This test is conducted by connecting debug board to GBC board and restarting the system after it boots up. The system is restarted either by giving the command "sudo reboot" in the terminal or by clicking the restart button. Please refer to Section **4.2.9.5** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.9.3.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.2.9.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002
Debug board Serial Number - WZ1628LIFE2DEBUG0018
Software versions – Linux 14.4.4

9.2.9.3.5 Test Results

Soft Reset for the system is verified.

9.2.9.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Soft Reset							
NA							

The snapshots of Soft Reset for the system are attached herewith.


Soft_Reset_1.jpg


Soft_Reset_2.jpg

9.2.9.4 Test ID / Test Name: PWR.11.4 / Hard Reset

9.2.9.4.1 Purpose

The purpose of the test case is to validate the hard reset of the system.

9.2.9.4.2 Test and Measurement Method

This test is conducted by connecting debug board to GBC board and restarting the system after it boots up. The system is restarted by pressing switch (S2). Please refer to Section **4.2.9.6** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.2.9.4.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.2.9.4.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Debug board Serial Number - WZ1628LIFE2DEBUG0018

Software versions – Linux 14.4.4

9.2.9.4.5 Test Results

Hard Reset for the system is verified.

9.2.9.4.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Hard Reset							
NA							

The snapshots of Hard Reset for the system are attached herewith.


Hard_Reset.jpg

9.3 CPU

9.3.1 Intel Atom

9.3.1.1 Test ID / Test Name: CPU.1.1/ Boot configuration

9.3.1.1.1 Purpose

The purpose of the test case is to validate SPI NOR Flash memory by accessing the device and loading the CoreBoot image

9.3.1.1.2 Test and Measurement Method

This test is conducted by programming SPI NOR FLASH device using SF100 ISP IC programmer. Please refer to Section **5.2.1.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.1.1.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.3.1.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0016

Software versions – NA

9.3.1.1.5 Test Results

This test case verifies successfully programming and configuring the SPI NOR FLASH.

9.3.1.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		

Boot configuration
NA

Snapshot of SF100 programmer GUI and its programming execution is embed in the image below.

BOOT configuration.PNG

9.3.1.2 Test ID / Test Name: CPU.1.2/ Power-on sequence

9.3.1.2.1 Purpose

The purpose of the test case is to validate sequence of PMIC power rails while powering on the system.

9.3.1.2.2 Test and Measurement Method

This test is conducted by probing at appropriate locations using logic analyzer to check the sequence of power rails as depicted in the below table and the trigger is set to 550mV. The measured sequence should be as per the IDT9145-I0 specification. Please refer to Section **5.2.1.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.1.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.1.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – NA

9.3.1.2.5 Test Results

This test case verifies the Cold Boot Sequence (Power on sequence) of Intel SOC.

9.3.1.2.6 Measurement Logs

Power-on sequence

Sl. No	Logic analyzer bits	Measurement Points	Measured sequence	Specification	Design Margin (%)	Result
				Expected sequence		
1	D5	R2B40.1	PWRBTNIN	PWRBTNIN	NA	PASS
2	D0	C1B7.1	VUSBPHY	V1P8_IFSUP		
3	D1	C3M10	V1P0_A	VUSBPHY		
4	D2	C3M19.1	V1P2_A	V1P0_A		
5	D3	C2N9.2	V1P8_A	V1P2_A		
6	D4	C3M17.1	VDDQ	V1P8_A		
7	D6	C4M10.2	V1P8_IFSUP*	VDDQ		
8	D7	C2B34.1	VCC	VCC		
9	D8	C3M8.1	V1P5_S	V1P5_S		
10	D9	C3M22.1	V1P35_S	V1P35_S		
11	D10	C3B33.1	COREPWROK	COREPWROK		

NOTE:

1. *Even though V1P8_IFSUP is not in sequence we can consider this test case as PASS. Because V1P8_IFSUP is not used for Intel SOC.

2. PMIC IC has been changed in next version from 9145 to 9180. IDT team has tested power on and power down sequence and the reports for the same are attached below.

The detailed analysis report with waveform captured for power on sequence test case is embed in the excel document attached herewith.

Power_on_sequence.xlsx

Validation report for Facebook_Aricer

9.3.1.3 Test ID / Test Name: CPU.1.3/ Power-down sequence

9.3.1.4.1 Purpose

The purpose of the test case is to validate sequence of PMIC power rails while powering off the system.

9.3.1.4.2 Test and Measurement Method

This test is conducted by probing at appropriate locations using logic analyzer to check the sequence of power rails while powering off the device as depicted in the below table and the trigger is set to 550mV.

The measured sequence should be as per the IDT9145 specification. Please refer to Section **5.2.1.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.1.4.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load –Typical

9.3.1.4.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – NA

9.3.1.4.5 Test Results

This test case fails to verify the Cold Off Sequence (Power down sequence) of Intel SOC.

9.3.1.4.6 Measurement Logs

Power-down sequence						
Sl.No	Logic analyzer bits	Measurement Points	Measured sequence	Specification Expected sequence	Design Margin (%)	Result
1	D11	R2B13.1	PLTRST_B	PLTRST_B	NA	FAIL
2	D10	C3B33.1	COREPWROK	COREPWROK		
3	D12	C2B22.1	VDDQ_VTT	VDDQ_VTT		
4	D7	C2B34.1	VCC	VCC		
5	D13	C3A12.1	VNN	V3P3S		
6	D15	C2B1.1	V1P2_A	VNN		
7	D3	C2N9.2	V1P0_A	V1P2_A		
8	D4	C3M17.1	V1P8_A	V1P8_A		
9	D2	C3M19.1	V3P3S	V1P0_A		

NOTE: Failure resolution: Issue is attributed to IDT9145 PMIC and is addressed with IDT9180 PMIC. Rev C design now uses IDT9180 PMIC.

The detailed analysis report with waveform captured for power down sequence test case is embed in the excel document attached herewith.

Power_down_sequence.xlsx

9.3.2 PMIC (IDTP9145) - I2C

9.3.2.1 Test ID / Test Name: CPU.2.1 / Electrical validation

9.3.2.1.1 Purpose

The purpose of the test case is to validate the electrical characteristics of I2C interface between Intel Atom processor and PMIC.

9.3.2.1.2 Test and Measurement Method

This test is conducted by probing the I2C signal at R1B14.2 (SCL), R1B8.2 (SDA) after running the script "./soc_i2c0_pmic_read_kernel_4.4.0.31.sh" in the terminal. The measured values are well with-in the limit as specified in the IDT9145 PMIC datasheet specification. Please refer to Section **5.2.2.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.2.1.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.3.2.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – Linux 14.4.4 with PMIC I2C code

9.3.2.1.5 Test Results

The electrical characteristics of I2C interface between Intel Atom processor and PMIC is within the designed spec.

9.3.2.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
PMIC - U2B3							
SOC_I2C_SCL	R1B14.2	VLOW (max) (V)	0.08	-0.5	0.54	116.00	PASS
		VHIGH (min) (V)	1.8	1.26	2.3	-21.74	PASS
		Rise time (ns)	163.8	0	300	-45.40	PASS
		Fall time (ns)	152.9	0	300	-49.03	PASS
		Frequency (kHz)	384.6	0	400	-3.85	PASS
SOC_I2C_SDA	R1B8.2	VLOW (max) (V)	0.08	-0.5	0.54	116.00	PASS
		VHIGH (min) (V)	1.8	1.26	2.3	-21.74	PASS
		Rise time (ns)	284.8	0	300	-5.07	PASS
		Fall time (ns)	163.8	0	300	-45.40	PASS

The detailed analysis report with waveform captured for PMIC I2C - Electrical validation is embedded in the xls document attached herewith.

PMIC I2C Electrical validation.xlsx

9.3.2.2 Test ID / Test Name: CPU.2.2/ Signal integrity

9.3.2.2.1 Purpose

The purpose of the test case is to validate the signal integrity of I2C interface between Intel Atom processor and PMIC.

9.3.2.2.2 Test and Measurement Method

This test is conducted by probing the I2C signal at R1B14.2 (SCL), R1B8.2 (SDA) after running the script "./soc_i2c0_pmic_read_kernel_4.4.0.31.sh" in the terminal. The measured values are well with-in the limit as specified in the IDT9145 PMIC datasheet specification. Please refer to Section **5.2.2.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.2.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.2.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – Linux 14.4.4 with PMIC I2C code

9.3.2.2.5 Test Results

The signal integrity of I2C interface between Intel Atom processor and PMIC is not within the designed spec.

9.3.2.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
PMIC - U2B3							
SOC_I2C_SCL	R1B14.2	Positive Over-shoot (%)	11.63	0	10	16.3	FAIL
		Negative Over-shoot (%)	20.93	0	10	109.3	FAIL
SOC_I2C_SDA	R1B8.2	Positive Over-shoot (%)	9.3	0	10	-7	PASS
		Negative Over-shoot (%)	9.3	0	10	-7	PASS
		Data set-up time (ns)	1450	100	2500	-42	PASS
		Data hold time (ns)	990	300	2500	-60.40	PASS

NOTE: Failure Resolution: Series termination changed to 33 Ohms in Rev C.

The detailed analysis report with waveform captured for PMIC I2C - Signal integrity is embedded in the xls document attached herewith.

PMIC I2C - Signal integrity.xlsx

9.3.2.3 Test ID / Test Name: CPU.2.3/ Functional validation

9.3.2.3.1 Purpose

The purpose of the test case is to validate the I2C interface of PMIC IC.

9.3.2.3.2 Test and Measurement Method

This test is conducted by accessing I2C0 bus and reading chip revision register value 0x05 from address 0x01. Please refer to Section **5.2.2.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.2.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.2.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – Linux 14.4.4 with PMIC I2C code

9.3.2.3.5 Test Results

INTEL atom processor able to read chip revision register of PMIC and the same has been validated.

9.3.2.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
PMIC							
NA							

The snapshot of functional validation of PMIC I2C is attached herewith.

pmic_i2c_FV.png

9.3.3 DDR (TS512MSK64W6H-I) - SMBus

9.3.3.1 Test ID / Test Name: CPU.5.1/ Electrical validation

9.3.3.1.1 Purpose

The purpose of the test case is to validate the electrical characteristics of SMBus interface between Intel Atom processor and DDR Memory.

9.3.3.1.2 Test and Measurement Method

This test is conducted by probing the SMBus signal at U4D1.6 (SDA) and U4D1.7 (CLK) after running the script "./pcu_smb_ddr3spd_read.sh" in the terminal. The measured values are well with-in the limit as specified in the DDR datasheet specification. Please refer to Section **5.2.3.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.3.1.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.3.3.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – Linux 14.4.4 with DDR3 SMB code

9.3.3.1.5 Test Results

The electrical characteristics of SMBus interface between Intel Atom processor and DDR Memory is within the designed spec.

9.3.3.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
DDR-SMB (Before Level Shifter)							

PCU_SMB_CLK	U4D1.2	VLOW (max) (V)	0	-0.5	0.54	100.00	PASS
		VHIGH (min) (V)	1.8	1.26	5.5	-42.86	PASS
		Rise time (ns)	710	0	1000	-29.00	PASS
		Fall time (ns)	8	0	300	-97.33	PASS
		Frequency (kHz)	100	0	100	0.00	PASS
PCU_SMB_DAT	U4D1.3	VLOW (max) (V)	0	-0.5	0.54	100.00	PASS
		VHIGH (min) (V)	1.8	1.26	5.5	-42.86	PASS
		Rise time (ns)	740	0	1000	-26.00	PASS
		Fall time (ns)	10	0	300	-96.67	PASS
DDR-SMB (After Level Shifter)							
SMB_DDR3_CLK	U4D1.7	VLOW (max) (V)	0.4	-0.5	0.99	180.00	PASS
		VHIGH (min) (V)	2.8	2.31	3.8	-21.21	PASS
		Rise time (ns)	860	0	1000	-14.00	PASS
		Fall time (ns)	52	0	300	-82.67	PASS
		Frequency (kHz)	83.3	0	100	-16.70	PASS
SMB_DDR3_DAT	U4D1.6	VLOW (max) (V)	0.4	-0.5	0.99	180.00	PASS
		VHIGH (min) (V)	2.8	2.31	3.8	-21.21	PASS
		Rise time (ns)	980	0	1000	2.00	PASS
		Fall time (ns)	56	0	300	-81.33	PASS

The detailed analysis report with waveform captured for DDR SMBus - Electrical validation is embedded in the xls document attached herewith.

DDR SMB Electrical validation.xlsx

9.3.3.2 Test ID / Test Name: CPU.5.2 / Signal integrity

9.3.3.2.1 Purpose

The purpose of the test case is to validate the signal integrity of SMBus interface between Intel Atom processor and DDR Memory.

9.3.3.2.2 Test and Measurement Method

This test is conducted by probing the SMBus signal at U4D1.6 (SDA) and U4D1.7 (CLK) after running the script "./pcu_smb_ddr3spd_read.sh" in the terminal. The measured values are well with-in the limit as specified in the DDR datasheet specification. Please refer to Section **5.2.3.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.3.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.3.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – Linux 14.4.4 with DDR3 SMB code

9.3.3.2.5 Test Results

The Signal integrity characteristics of SMBus interface between Intel Atom processor and DDR Memory is not within the designed spec.

9.3.3.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
DDR-SMB (Before Level Shifter)							
PCU_SMB_CLK	U4D1.2	Positive Over-shoot (V)	0	0	0.18	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.18	-100.00	PASS
PCU_SMB_DAT	U4D1.3	data set-up time (ns)	3000	250	10000	-70.00	PASS
		data hold time (ns)	1680	300	10000	-83.20	PASS
		Positive Over-shoot (V)	0	0	0.18	-100.00	PASS
		Negative Over-shoot (V)	0.34	0	0.18	88.89	FAIL
DDR-SMB (After Level Shifter)							
SMB_DDR3_CLK	U4D1.7	Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.32	0	0.33	-3.03	PASS
SMB_DDR3_DAT	U4D1.6	data set-up time (ns)	3000	250	10000	-70.00	PASS
		data hold time (ns)	1660	300	10000	-83.40	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.36	0	0.33	9.09	FAIL

NOTE: Failure Resolution: Series termination changed to 10 Ohms in Rev C.

The detailed analysis report with waveform captured for DDR SMBus - Signal integrity is embedded in the xls document attached herewith.


DDR SMB Signal integrity.xlsx

9.3.3.3 Test ID / Test Name: CPU.5.3 / Functional validation

9.3.3.3.1 Purpose

The purpose of the test case is to validate the SMBus interface of DDR Memory.

9.3.3.3.2 Test and Measurement Method

This test is conducted by reading I2C9 bus at address 50H by reading device register address from 128 to 145. . Please refer to Section **5.2.3.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.3.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.3.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – Linux 14.4.4 with DDR3 SMB code

9.3.3.3.5 Test Results

INTEL atom processor able to read DDR registers and the same has been validated.

9.3.3.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
DDR-SMB							
NA							

The snapshots of functional validation of DDR SMBus are attached herewith.


DDR3_SMBus_FV_1.png


DDR3_SMBus_FV_2.png

9.3.4 PCU (ADT7481) - SMBus

9.3.4.1 Test ID / Test Name: CPU.6.1/ Electrical validation

9.3.4.1.1 Purpose

The purpose of the test case is to validate the electrical characteristics of SMBus interface between Intel Atom processor and temperature sensor.

9.3.4.1.2 Test and Measurement Method

This test is conducted by probing the I2C signal at U3A1.10 (SCL), U3A1.9 (SDA) after running the script "./pcu_smb_tsensor_read.sh" in the terminal. The measured values are well with-in the limit as specified in the Temperature Sensor datasheet specification. Please refer to Section **5.2.4.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.4.1.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.3.4.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – Linux 14.4.4 with Temp sensor SMB code

9.3.4.1.5 Test Results

The electrical characteristics of SMBus interface between Intel Atom processor and temperature sensor is within the designed spec.

9.3.4.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
PCU - SMB (Before Level Shifter)							
PCU3_SMB_CLK	U2A1.2	VLOW (max) (V)	0	-0.5	0.54	100.00	PASS
		VHIGH (min) (V)	1.8	1.26	5.5	-42.86	PASS
		Rise time (ns)	700	0	1000	-30.00	PASS
		Fall time (ns)	8.4	0	300	-97.20	PASS
		Frequency (kHz)	92.592	0	100	-7.41	PASS
PCU3_SMB_DAT	U2A1.3	VLOW (max) (V)	0	-0.5	0.54	100.00	PASS
		VHIGH (min) (V)	1.8	1.26	5.5	-42.86	PASS
		Rise time (ns)	750	0	1000	-25.00	PASS
		Fall time (ns)	11.6	0	300	-96.13	PASS
PCU-SMB (After Level Shifter)							
SMB_3P3_CLK	U3A1.10	VLOW (max) (V)	0.4	-0.5	0.8	180.00	PASS
		VHIGH (min) (V)	2.8	2.1	3.8	-26.32	PASS
		Rise time (ns)	630	0	1000	-37.00	PASS
		Fall time (ns)	62	0	300	-79.33	PASS
		Frequency (kHz)	98.039	0	100	-1.96	PASS
SMB_3P3_DAT	U3A1.9	VLOW (max) (V)	0.4	-0.5	0.8	180.00	PASS
		VHIGH (min) (V)	2.8	2.1	3.8	-26.32	PASS
		Rise time (ns)	650	0	1000	-35.00	PASS
		Fall time (ns)	60	0	300	-80.00	PASS

The detailed analysis report with waveform captured for PCU SMBus - Electrical validation is embedded in the xls document attached herewith.

PCU SMB Electrical validation.xlsx

9.3.4.2 Test ID / Test Name: CPU.6.2 / Signal Integrity

9.3.4.2.1 Purpose

The purpose of the test case is to validate the Signal Integrity of SMBus interface between Intel Atom processor and temperature sensor.

9.3.4.2.2 Test and Measurement Method

This test is conducted by probing the I2C signal at U3A1.10 (SCL), U3A1.9 (SDA) after running the script "./pcu_smb_tsensor_read.sh" in the terminal. The measured values are well with-in the limit as specified in the Temperature Sensor datasheet specification. Please refer to Section

5.2.4.3 in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.4.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.4.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – Linux 14.4.4 with Temp sensor SMB code

9.3.4.2.5 Test Results

The Signal Integrity characteristics of SMBus interface between Intel Atom processor and temperature sensor is not within the designed spec.

9.3.4.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
PCU-SMB (Before Level Shifter)							
PCU3_SMB_CLK	U2A1.2	Positive Over-shoot (V)	0	0	0.18	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.18	-100.00	PASS
PCU3_SMB_DAT	U2A1.3	data set-up time (ns)	3720	250	10000	-62.80	PASS
		data hold time (ns)	1690	300	10000	-83.10	PASS
		Positive Over-shoot (V)	0	0	0.18	-100.00	PASS
		Negative Over-shoot (V)	0.2516	0	0.18	39.78	FAIL
PCU-SMB (After Level Shifter)							
SMB_3P3_CLK	U3A1.10	Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.23	0	0.33	-30.30	PASS
SMB_3P3_DAT	U3A1.9	data set-up time (ns)	3040	250	10000	-69.60	PASS
		data hold time (ns)	1620	300	10000	-83.80	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.28	0	0.33	-15.15	PASS

NOTE: Failure Resolution: Series termination changed to 10 Ohms in Rev C.

The detailed analysis report with waveform captured for PCU SMBus - Signal Integrity is embedded in the xls document attached herewith.

PCU SMB Signal Integrityxlsx

9.3.4.3 Test ID / Test Name: CPU.6.3 / Functional validation

9.3.4.3.1 Purpose

The purpose of the test case is to validate the SMBus interface of temperature sensor.

9.3.4.3.2 Test and Measurement Method

This test is conducted by reading I2C9 bus at address 3DH and 3EH for respective device ID and manufacture ID and read values 81H and 41H respectively. Please refer to Section **5.2.4.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.4.3.3 Test Condition

Ambient Temperature25˚C

Operating Voltage – 18V

System load – Typical

9.3.4.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – Linux 14.4.4 with Temp sensor SMB code

9.3.4.3.5 Test Results

INTEL atom processor able to read Device and Manufacture ID of temperature sensor and the same has been validated.

9.3.4.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
PCU - SMB							
NA							

The snapshot of functional validation of PCU SMBus is attached herewith.

Temp_sensor_SMBus_FV.png

9.3.5 Springville 1 - MDI

9.3.5.1 Test ID / Test Name: CPU.7.1/ Signal characteristics

9.3.5.1.1 Purpose

The purpose of this test case is to verify MDI (interface between Marvell Switch (88E6071) to Springville (WGI210AT)) signal characteristics.

9.3.5.1.2 Test and Measurement Method

This test is conducted by connecting a Linux PC to port A of GBC board and starting communication between them by pinging each other. The MDI transmitting signals (from Springville to Switch) are measured at R962 (MDI0P) and R963 (MDI0N) and MDI receiving signals (from Switch to Springville) are measured at L1M2.6 (MDI1P) and L1M2.8 (MDI1N). Please refer to Section **5.2.5.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.5.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.5.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – Linux 14.4.4

9.3.5.1.5 Test Results

The signal characteristics of MDI signals are as per the specification and the data rate is 100Mbps.

9.3.5.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Springville 1 - MDI							
MDI0P, MDI0N	R962.2, R963.2	Vp-p (V)	1.012	0.950	1.05	-3.62	PASS
		Overshoot (%)	0.86	0	5	-82.80	PASS
		Undershoot (%)	2.01	0	5	-59.80	PASS
		Data rate (Mbps)	100	NA	100	0.00	PASS
MDI1P, MDI1N	L1M2.6, L1M2.8	Vp-p (V)	1.012	0.950	1.05	-3.62	PASS
		Overshoot (%)	0.86	0	5	-82.80	PASS
		Undershoot (%)	2.01	0	5	-59.80	PASS
		Data rate (Mbps)	100	NA	100	0.00	PASS

The detailed analysis report with waveform captured for signal characteristics of Springville MDI test case is embedded in the xls document attached herewith.

MDI_switch_to_springville.xlsx

9.3.5.2 Test ID / Test Name: CPU.7.2/ Functional validation

9.3.5.2.1 Purpose

The purpose of the test case is to validate the function of springville1-MDI.

9.3.5.2.2 Test and Measurement Method

This test is conducted by connecting a Linux PC to port A of GBC board and starting communication between them by giving command “ping IPaddress (IP address of Linux PC)” in the terminal of GBC system and “ping IPaddress (IP address of GBC system)” in Linux PC. Please refer to Section **5.2.5.3** in latest version of “OC_CONNECT_1_GBC_Test_Specification” document for detailed test procedure.

9.3.5.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.5.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – Linux 14.4.4

9.3.5.2.5 Test Results

Communication is established between Springville and Marvell switch through MDI interface over 100Mbps data rate.

The snapshot of functional validation of Springville MDI is attached herewith.


Springville1_MDI_GBC_FV.png


Springville1_MDI_LinuxPC_FV.png


Springville1_MDI_DataRate.png

9.3.6 TIVA - UART

9.3.6.1 Test ID / Test Name: CPU.8.1 / Electrical validation

9.3.6.1.1 Purpose

The purpose of the test case is to validate the electrical characteristics of UART interface between Tiva controller and Intel Atom processor.

9.3.6.1.2 Test and Measurement Method

This test is conducted by probing the UART TX signal at R10550 and UART RX signal at R10472 respectively. UART TX is measured by sending data from TIVA to SOC. UART RX is measured by sending data from SOC to TIVA. Please refer to Section **5.2.6.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.6.1.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.3.6.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Debug board Serial Number - WZ1628LIFE2DEBUG0018

Software versions – Linux 14.4.4

9.3.6.1.5 Test Results

The electrical characteristics of UART interface between Tiva controller and Intel Atom processor fails.

9.3.6.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
UART TX							
ISO_TIVA_SOC_UART3_TX	R10550	VLOW (V)	0	-0.378	0.63	100.00	PASS
		VHIGH (V)	1.8	1.17	2.232	-19.35	PASS
		Positive Overshoot (V)	0.17	0	0.18	-5.56	PASS
		Negative Overshoot (V)	0.22	0	0.18	22.22	FAIL
UART RX							
TIVA_SOC_UART3_RX	R10472	VLOW (V)	-0.18	0	1.155	-115.58	FAIL
		VHIGH (V)	3.16	2.145	4	-21.00	PASS
		Positive Overshoot (V)	0.9	0	0.33	172.73	FAIL
		Negative Overshoot (V)	0.96	0	0.33	190.91	FAIL

NOTE: Failure Resolution: Series termination changed to 49.9 Ohms in Rev C.

The detailed analysis report with waveform captured for Electrical validation of TIVA – UART test case is embedded in the xls document attached herewith.

TIVA- UART_EV.xlsx

9.3.6.2 Test ID / Test Name: CPU.8.2 / Functional validation

9.3.6.2.1 Purpose

The purpose of the test case is to validate the function of UART interface between Tiva controller and Intel Atom processor.

9.3.6.2.2 Test and Measurement Method

The function of UART is validated by sending message from SOC to TIVA to request the Intel temperature reading and getting the response from TIVA. Please refer to Section **5.2.6.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.6.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.6.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Debug board Serial Number - WZ1628LIFE2DEBUG0018

Software versions – Linux 14.4.4

9.3.6.2.5 Test Results

The UART interface between Tiva controller and Intel Atom processor is validated.

9.3.6.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
TIVA- UART							
NA							

The snapshots of Functional validation of UART interface between Tiva controller and Intel Atom processor are attached herewith.

UART_RX_SOC.png UART_RX_TIVA.png UART_TX_SOC.jpg UART_TX_SOC_TIVA.jpg UART_TX_TIVA.jpg

9.3.7 Memory - DDR

9.3.7.1 Test ID / Test Name: CPU.9.1 / Reference voltage measurement

9.3.7.1.1 Purpose

The purpose of the test case is to measure the reference voltages of DDR (DDR_VREF and DDR_VTT).

9.3.7.1.2 Test and Measurement Method

This test is conducted by probing the voltage at R2P7.1/R3P12.1 and C4P17.1 for DDR_VREF and DDR_VTT respectively. The measured reference values have to be in the range 0.64 - 0.725V. The VDDQ voltage has also been measured at C3P14.1 to validate the reference voltage (VREF = VDDQ/2, VDDQ = 1.35V). Please refer to Section **5.2.7.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.7.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.7.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – NA

9.3.7.1.5 Test Results

The voltage measured at DDR_VREF and DDR_VTT are in the range 0.64 - 0.725V.

9.3.7.1.6 Measurement Logs

Memory - DDR Reference voltage measurement							
Test	Probing Point	Measured Voltage (V)	Expected Voltage(V)	Specification		Design Margin (%)	Result
				Min(V)	Max(V)		
VDDQ	C3P14.1	1.33	1.35	1.28	1.45	-3.90625	PASS
VREF/DQ	R2P7.1	0.671	0.675	0.64	0.725	-4.84375	PASS
VREFCA	R3P12.1	0.671	0.675	0.64	0.725	-4.84375	PASS

VTT_DDR	C4P17.1	0.657	0.675	0.64	0.725	-2.65625	PASS

The detailed analysis report with waveform captured for Reference voltage measurement test case is embedded in the xls document attached herewith.

Memory - DDR_Vref.xlsx

9.3.7.2 Test ID / Test Name: CPU.9.2 / VREF Schmoo test

9.3.7.2.1 Purpose

The purpose of the test case is to validate the DDR module by varying VREF voltage within the limits at different temperatures.

9.3.7.2.2 Test and Measurement Method

This test is conducted by executing 'memtester' utility on SoC for different voltages of DDR_VREF at different temperatures. DDR_VREF can be varied by changing the voltage divide resistors, R2P11, R2P7, R3P6 and R3P12 such that there can be three co-ordinates within the specified range of DDR module. In each co-ordinate, memtester utility is executed at six different temperatures to validate VREF Schmoo. Please refer to Section **5.2.7.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.7.2.3 Test Condition

Temperature – -20˚C to +70˚C
Operating Voltage – 18V
System load – Typical

9.3.7.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002
Software versions – Linux 14.4.4 with memtester utility

9.3.7.2.5 Test Results

The 'memtester' utility passes for various DDR_VREF voltages under different temperature conditions.

9.3.7.2.6 Measurement Logs

1. Memory - DDR VREF measurement

Memory - DDR VREF measurement										
Sl. No.	Probing Point	Temperature Condition (°C)	Resistor Value (kΩ) - R2P7/R3P12	Resistor Value (kΩ) - R2P11/R3P6	Measured Voltage (V)	Expected Voltage (V)	Specification		Design Margin (%)	Pass/Fail
							Min (V)	Max (V)		
1	R2P7	-20	4.42	4.7	0.616	0.654	0.64	0.725	3.75	FAIL
2		0	4.42	4.7	0.631	0.654	0.64	0.725	1.41	FAIL
3		20	4.42	4.7	0.626	0.654	0.64	0.725	2.19	FAIL
4		25	4.42	4.75	0.662	0.651	0.64	0.725	-3.44	PASS
5		40	4.42	4.7	0.611	0.654	0.64	0.725	4.53	FAIL
6		70	4.42	4.7	0.614	0.654	0.64	0.725	4.06	FAIL
7		-20	4.99	4.7	0.671	0.695	0.64	0.725	-4.84	PASS
8		0	4.99	4.7	0.659	0.695	0.64	0.725	-2.97	PASS
9		20	4.99	4.7	0.663	0.695	0.64	0.725	-3.59	PASS
10		25	4.99	4.7	0.708	0.695	0.64	0.725	-2.34	PASS
11		40	4.99	4.7	0.66	0.695	0.64	0.725	-3.13	PASS
12		70	4.99	4.7	0.66	0.695	0.64	0.725	-3.13	PASS
13		-20	5.11	4.42	0.693	0.724	0.64	0.725	-4.41	PASS
14		0	5.11	4.42	0.686	0.724	0.64	0.725	-5.38	PASS
15		20	5.11	4.42	0.681	0.724	0.64	0.725	-6.07	PASS
16		25	5.11	4.42	0.718	0.724	0.64	0.725	-0.97	PASS
17		40	5.11	4.42	0.679	0.724	0.64	0.725	-6.09	PASS
18		70	5.11	4.42	0.689	0.724	0.64	0.725	-4.97	PASS

NOTE: Reason for failure - Measurements have been taken placing the board in thermal chamber and the length of the wire soldered to the measuring points were very long which caused the drop and hence the failures.

2. Memory - DDR VDDQ measurement

Memory - DDR VDDQ measurement										
Sl. No.	Probing Point	Temperature Condition (°C)	Resistor Value (kΩ) - R2P7/R3P12	Resistor Value (kΩ) - R2P11/R3P6	Measured Voltage (V)	Expected Voltage (V)	Specification		Design Margin (%)	Pass/Fail
							Min (V)	Max (V)		
1	C3P14	-20	4.42	4.7	1.289	1.35	1.28	1.45	-0.70	PASS
2		0	4.42	4.7	1.319	1.35	1.28	1.45	-3.05	PASS
3		20	4.42	4.7	1.316	1.35	1.28	1.45	-2.81	PASS

4		25	4.42	4.75	1.379	1.35	1.28	1.45	-4.90	PASS
5		40	4.42	4.7	1.288	1.35	1.28	1.45	-0.63	PASS
6		70	4.42	4.7	1.323	1.35	1.28	1.45	-3.36	PASS
7		-20	4.99	4.7	1.33	1.35	1.28	1.45	-3.91	PASS
8		0	4.99	4.7	1.323	1.35	1.28	1.45	-3.36	PASS
9		20	4.99	4.7	1.323	1.35	1.28	1.45	-3.36	PASS
10		25	4.99	4.7	1.368	1.35	1.28	1.45	-5.66	PASS
11		40	4.99	4.7	1.317	1.35	1.28	1.45	-2.89	PASS
12		70	4.99	4.7	1.329	1.35	1.28	1.45	-3.83	PASS
13		-20	5.11	4.42	1.329	1.35	1.28	1.45	-3.83	PASS
14		0	5.11	4.42	1.321	1.35	1.28	1.45	-3.20	PASS
15		20	5.11	4.42	1.322	1.35	1.28	1.45	-3.28	PASS
16		25	5.11	4.42	1.364	1.35	1.28	1.45	-5.93	PASS
17		40	5.11	4.42	1.321	1.35	1.28	1.45	-3.20	PASS
18		70	5.11	4.42	1.316	1.35	1.28	1.45	-2.81	PASS

The snapshot of execution of 'memtester' utility for VREF Schmoo test is attached herewith.

DDR_memtest_3072M.png

The detailed analysis report with waveform captured for VREF Schmoo test is embedded in the xls document attached herewith.

Memory - DDR_Schmoo_Test.x

9.3.7.3 Test ID / Test Name: CPU.9.3 / Functional validation

9.3.7.3.1 Purpose

The purpose of the test case is to validate the entire DDR memory using memtest option at boot stage.

9.3.7.3.2 Test and Measurement Method

This test is conducted by executing memtest function during boot stage. The results of memtest are captured to check for any errors. Please refer to Section **5.2.7.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.7.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.7.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – CoreBoot with memtest option

9.3.7.3.5 Test Results

The memtest test is executed with zero errors.

9.3.7.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Memory - DDR							
NA							

The snapshot of execution of memtest option for functional validation of DDR memory is attached herewith.

DDR_Memtest_FV.jpg

9.3.7.4 Test ID / Test Name: CPU.9.4 / Throughput measurement

9.3.7.4.1 Purpose

The purpose of the test case is to validate the DDR memory for its latency and bandwidth.

9.3.7.4.2 Test and Measurement Method

This test is conducted by running “make results see”.exe after unpacking the downloaded source code (lmbench 3.0). The results will be saved in lmbench directory. Read / Write throughputs which are read in Mbps data speed present in the last result columns. Please refer to Section **5.2.7.5** in latest version of “OC_CONNECT_1_GBC_Test_Specification” document for detailed test procedure.

9.3.7.4.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.7.4.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – Linux 14.4.4 with lmbench 3.0

9.3.7.4.5 Test Results

The read / write throughputs are measured in Mbps. The throughput of Mem read and Mem write is 4414 MB/s and 2758 MB/s respectively.

9.3.7.4.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Memory – DDR ; Throughput measurement							
NA							

The log of throughput measurement for DDR memory is attached herewith.

lmbench output.txt

9.3.8 Memory SPI NOR Flash

9.3.8.1 Test ID / Test Name: CPU.10.1 / Electrical validation

9.3.8.1.1 Purpose

The purpose of the test case is to validate the electrical characteristics of SPI interface of SPI NOR Flash.

9.3.8.1.2 Test and Measurement Method

This test is conducted by probing the SPI signal at R10762.2 (CLK), R1M11.2 (MISO) while system booting. The measured values should follow pass criteria, as specified in the below table. Please refer to Section **5.2.8.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.8.1.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.3.8.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018

Software versions – Core boot

9.3.8.1.5 Test Results

The Electrical characteristics of SPI interface of SPI NOR Flash is within the designed spec.

9.3.8.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
SPI_NOR_Flash							
SOC_FLASH_CLK	R10762	VLOW (max) (V)	-4.47e-13	-0.5	0.54	100.00	PASS
		VHIGH (min) (V)	1.64	1.26	2.2	-25.45	PASS
		Rise time (V/ns)	0.1906	0.1	3	-90.60	PASS

		Fall time (V/ns)	0.1682	0.1	3	-68.20	PASS
		Frequency (MHz)	33.33	0	50	-33.34	PASS
SOC_FLASH_MISO	R10764	VLOW (max) (V)	0.02	-0.5	0.54	104.00	PASS
		VHIGH (min) (V)	1.82	1.26	2.2	-17.27	PASS
		Rise time (V/ns)	0.2028	0.1	3	-93.24	PASS
		Fall time (V/ns)	0.2025	0.1	3	-93.25	PASS

The detailed analysis report with waveform captured for SPI NOR Flash electrical validation test case is embed in the excel document attached herewith.

SPI_NOR_FLASH_EV.xlsx

9.3.8.2 Test ID / Test Name: CPU.10.2 / Signal Integrity

9.3.8.3.1 Purpose

The purpose of the test case is to validate the signal integrity of SPI interface of SPI NOR Flash.

9.3.8.3.2 Test and Measurement Method

This test is conducted by probing the SPI signal at R10762.2 (CLK), R1M11.2 (MISO) while system booting. The measured values should follow pass criteria, as specified in the below table. Please refer to Section **5.2.8.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.8.3.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.3.8.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018

Software versions – Core boot

9.3.8.3.5 Test Results

The Signal integrity characteristics of SPI interface of SPI NOR Flash is within the designed spec.

9.3.8.3.6 Measurement Logs

SPI_NOR_Flash							
Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test Result
				Min	Max		
SOC_FLASH_CLK	R10762	Positive Over-shoot (V)	0.074	0	0.18	-58.8889	PASS
		Negative Over-shoot (V)	0.074	0	0.18	-58.8889	PASS
SOC_SPI_MISO	R1M11.2	Positive Over-shoot (V)	0.102	0	0.18	-43.3333	PASS
		Negative Over-shoot (V)	0.122	0	0.18	-32.2222	PASS
		data set-up time (ns)	13.7	2	100	-86.3	PASS
		data hold time (ns)	33	0	100	-67	PASS

NOTE: Re-measurement taken by changing R1M11 from 22 Ohm to 49.9 Ohm to decrease Overshoot and Undershoot of MISO signal.

The detailed analysis report with waveform captured for SPI NOR Flash electrical validation test case is embed in the excel document attached herewith.


SPI_NOR_FLASH_SI.xlsx

9.3.9 Storage - mSATA

9.3.9.1 Test ID / Test Name: CPU.11.1 / Signal Integrity

9.3.9.1.1 Purpose

The purpose of the test case is to validate the signal integrity of mSATA signals by plotting the eye diagram.

9.3.9.1.2 Test and Measurement Method

This test is conducted by plotting eye diagram of TX lines (SATA_TXP0/N0) and RX lines (SATA_RXN0/P0) and analyzing the eye characteristics as per mSATA standard. The TX lines are probed at C1833.1 and C1834.1. The RX lines are probed at C1835.2 and C1836.2. Please refer to

Section **5.2.9.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.9.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.9.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – Linux 14.4.4

9.3.9.1.5 Test Results

The eye height fails for both mSATA TX and RX lines. All other parameters of mSATA TX and RX lines are within the specified limits.

9.3.9.1.6 Measurement Logs

Storage - mSATA Signal integrity -MSATA Transmit						
Probing points	Parameters	Measured Value	Specification		Design Margin (%)	Result
			Min	Max		
C1833.1 and C1834.1	Eye jit RMS (ps)	4.3	NA	100	-95.70	PASS
	Eye Width (ps)	304.858	166.66	NA	-82.92	PASS
	Eye Height (mV)	520.1	695.2	NA	25.19	FAIL
	Data TIE (ps)	0.088	-11	11	100.80	PASS
	Data Rate (Gb/s)	3	NA	3	0.00	PASS
	Voltage peak to peak (mV)	949.46	800	NA	-18.68	PASS

Storage - mSATA Signal integrity -MSATA Receive						
Probing points	Parameters	Measured Value	Specification		Design Margin (%)	Result
			Min	Max		
C1835.2 and C1836.2	Eye jit RMS (ps)	11.436	NA	100	-88.56	PASS
	Eye Width (ps)	279.435	166.66	NA	-67.67	PASS
	Eye Height (mV)	304.2	695.2	NA	56.24	FAIL
	Data TIE (ps)	0.512	-11	11	104.65	PASS
	Data Rate (Gb/s)	3.06	NA	3	2.00	PASS
	Voltage peak to peak (mV)	1210.13	800	NA	-51.27	PASS

NOTE: Failure Resolution: New mSATA drives are being planned for Rev C and SATA characteristics will be revalidated in Rev C.

The detailed analysis report with waveform captured for Signal Integrity of mSATA memory is embedded in the xls document attached herewith.

mSATA Signal integrity.xlsx

9.3.9.2 Test ID / Test Name: CPU.11.2 / IO Stress

9.3.9.2.1 Purpose

The purpose of the test case is to validate mSATA memory access when mSATA lines are under stress.

9.3.9.2.2 Test and Measurement Method

This test is conducted by using FIO utility, which will stress the mSATA lines to their maximum performance. While they are under stress, mSATA memory should be accessible with no errors. Please refer to Section **5.2.9.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.9.2.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.3.9.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Software versions – Linux 14.4.4 with FIO utility configured

9.3.9.2.5 Test Results

FIO utility results show that there are no errors in accessing mSATA memory.

9.3.9.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Storage – mSATA							
NA							

The snapshots of execution of FIO utility for validating IO Stress of mSATA memory is attached herewith.


mSATA_FIO_1.png


mSATA_FIO_2.png

9.3.10 SpringVille1 – PCIe

9.3.10.1 Test ID / Test Name: CPU.13.1 and CPU.13.2 / Electrical Validation, Eye – plotting

9.3.10.1.1 Purpose

The purpose of this test case is to check and validate the electrical parameters and signal integrity of PCIe interface between Intel processor (U3) and Springville1 (U2M1).

9.3.10.1.2 Test and Measurement Method

- Transmitter Tests:
  1. Remove Springville1 IC (U2M1). Terminate the Tx lane1 lines from Intel processor by mounting a 50-ohm resistor on pin no 23 and 24 of U2M1. By doing so, PCIe compliance pattern as per section *4.2.8* of PCIe base specification ver. *2.1* is generated.
  2. Probe PCIE1_TXP_LAN and PCIE1_TXN_LAN at C2B30.1 and C2B29.1 respectively.
  3. Run the test utility N5393D in the iminium oscilloscope. To configure the test suite, select PCIe version as 2.0, Transmitter tests, Device1, Lane1, and speed as 2.5GT/s. In select tests option in utility, select transmitter tests and run all the selected test cases.
  4. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin.
- Receiver Tests:

1. Mount back Springville1 IC (U2M1). Terminate the Rx lane1 lines from Springville1 (U2M1) by lifting capacitor side C2M4.1 and C2M6.1 and terminating the line by mounting a 50-ohm resistor. By doing so, PCIe compliance pattern as per section *4.2.8* of PCIe base specification ver. *2.1* is generated.
2. Probe PCIE1_RXP_LAN and PCIE1_RXN_LAN at C2M4.1 and C2M6.1 respectively.
3. Run the test utility N5393D in the infiniium oscilloscope. To configure the test suite, select PCIe version as 2.0, Receiver tests, Device1, Lane1, and speed as 2.5GT/s. In select tests option in utility, select receiver tests and run all the selected test cases.
4. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin.

   Please refer to Section **5.2.10** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.10.1.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +18V DC

System load –Typical

9.3.10.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018

Software version – NA

9.3.10.1.5 Test Results

The test result generated by the test utility should be within the mentioned range in the PCIe Ver.*2.1* base specification.

9.3.10.1.6 Measurement Logs

- Transmitter:

PCIe - Springville1 _Transmitter Test						
Sl. No	**Test Name**	**Measured Value**	**Pass Margin**		**% Pass Margin**	**PASS / FAIL**
			Min	**Max**		
1	Unit Interval Test (UI) (ps)	400.025	399.88	400.12	39.6	PASS

2	Template Test	-	-	-	100	PASS
3	Median-to-Max jitter(ps)	17.03		50	65.9	PASS
4	Eye Width(mUI)	891	750		18.8	PASS
5	Peak Differential Output Voltage(Transition) (mV)	923.5	800	1200	30.9	PASS
6	Peak Differential Output Voltage (Non - Transition) (mV)	682.7	504	1200	25.7	PASS
7	Rise/Fall time (ps)	78.13	50		56.3	PASS
8	De-emphasized voltage ratio (dB)	-2.6	-4.5	-2.5	5	PASS
9	RMS AC peak common mode voltage (mV)	19.8		20	1	PASS
10	Avg DC common mode voltage (mV)	2.3	0	3600	0.1	PASS
11	Avg DC common mode voltage output variation (mV)	72.3		100	27.7	PASS
12	Avg DC common mode line delta (mV)	4.653		25	81.4	PASS

The detailed analysis report for PCIe – springville1 transmitter test case executed is attached herewith.

Transmitter_Springville1.html

- Receiver:

PCIe - Springville1 _Receiver Test						
Sl. No	**Test Name**	**Measured Value**	**Pass Margin**		**% Pass Margin**	**PASS / FAIL**
			Min	**Max**		
1	Unit Interval Test (UI) (ps)	400.028	399.88	400.12	38.3	PASS
2	Template Test	-	-	-	100	PASS
3	Median-to-Max jitter(ps)	18.7		120	84.4	PASS
4	Eye Width(mUI)	893	400		123.3	PASS
5	Peak Differential Output Voltage (mV)	225.2	175	1200	4.9	PASS
6	RMS AC peak common mode input voltage (mV)	57.3		150	61.8	PASS

The detailed analysis report for PCIe – springville1 receiver test case executed is attached herewith.

Receiver_Springville1.html

9.3.11 SpringVille2 – PCIe

9.3.11.1 Test ID / Test Name: CPU.14.1 and CPU14.2 / Electrical Validation, Eye – plotting

9.3.11.1.1 Purpose

The purpose of this test case is to check and validate the electrical parameters and signal integrity of PCIe interface between Intel processor (U3) and Springville2 (U2M2).

9.3.11.1.2 Test and Measurement Method

- Transmitter Tests:

  1. Remove Springville2 IC (U2M2). Terminate the Tx lane2 lines from Intel processor by mounting a 50-ohm resistor on pin no 23 and 24 of U2M2. By doing so, PCIe compliance pattern as per section *4.2.8* of PCIe base specification ver. *2.1* is generated.
  2. Probe PCIE2_TXP_LAN and PCIE2_TXN_LAN at C2B32.1 and C2B31.1 respectively.
  3. Run the test utility N5393D in the infiniium oscilloscope. To configure the test suite, select PCIe version as 2.0, Transmitter tests, Device1, Lane2, and speed as 2.5GT/s. In select tests option in utility, select transmitter tests and run all the selected test cases.
  4. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin.

- Receiver Tests:

  1. Mount back Springville2 IC (U2M2). Terminate the Rx lane2 lines from Springville2 (U2M2) by lifting capacitor side C2M22.1 and C2M21.1 and terminating the line by mounting a 50-ohm resistor. By doing so, PCIe compliance pattern as per section *4.2.8* of PCIe base specification ver. *2.1* is generated.
  2. Probe PCIE2_RXP_LAN and PCIE2_RXN_LAN at C2M22.1 and C2M21.1 respectively.
  3. Run the test utility N5393D in the infiniium oscilloscope. To configure the test suite, select PCIe version as 2.0, Receiver tests, Device1, Lane2, and speed as 2.5GT/s. In select tests option in utility, select receiver tests and run all the selected test cases.
  4. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin.

     Please refer to Section **5.2.11** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.11.1.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +18V DC

System load –Typical

9.3.11.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018

Software version – NA

9.3.11.1.5 Test Results

The test result generated by the test utility should be within the mentioned range in the PCIe Ver.*2.1* base specification.

9.3.11.1.6 Measurement Logs

- Transmitter:

PCIe - Springville2 _Transmitter Test						
Sl. No	**Test Name**	**Measured Value**	**Pass Margin**		**% Pass / Fail Margin**	**PASS / FAIL**
			Min	**Max**		
1	Unit Interval Test (UI) (ps)	400.025	399.88	400.12	39.6	PASS
2	Template Test	-	-	-	-100	FAIL
3	Median-to-Max jitter(ps)	16.28		50	64.7	PASS
4	Eye Width(mUI)	899	750		19.9	PASS
5	Peak Differential Output Voltage(Transition) (mV)	861.8	800	1200	15.5	PASS
6	Peak Differential Output Voltage (Non - Transition) (mV)	639.6	504	1200	19.5	PASS
7	Rise/Fall time (ps)	60.31	50		20.6	PASS
8	De-emphasized voltage ratio (dB)	-2.6	-4.5	-2.5	5	PASS
9	RMS AC peak common mode voltage (mV)	13.7		20	13.5	PASS
10	Avg DC common mode voltage (mV)	4.5	0	3600	0.1	PASS

11	Avg DC common mode voltage output variation (mV)	62.7		100	37.3	PASS
12	Avg DC common mode line delta (mV)	4.867		25	80.5	PASS

NOTE: This test will be re-performed in RevC by varying the de-emphasis settings.

The detailed analysis report for PCIe – springville2 transmitter test case executed is attached herewith.

Transmitter_Spring Ville2.zip

- Receiver:

PCIe - Springville2 _Receiver Test						
Sl. No	**Test Name**	**Measured Value**	**Pass Margin**		**% Pass Margin**	**PASS / FAIL**
			Min	**Max**		
1	Unit Interval Test (UI) (ps)	400.026	399.88	400.12	39.2	PASS
2	Template Test	-	-	-	100	PASS
3	Median-to-Max jitter(ps)	20.52		120	82.9	PASS
4	Eye Width(mUI)	799	400		99.8	PASS
5	Peak Differential Output Voltage (mV)	515.8	175	1200	33.2	PASS

The detailed analysis report for PCIe – springville2 receiver test case executed is attached herewith.

Receiver_SpringVill e2.zip

9.3.12 TRXFE – GPIO

NOTE: CPU 15.1 cannot be done because the GPIO line is connected to Test points in RF-SDR board.

9.3.12.1 Test ID / Test Name: CPU.15.2 / Control outputs functional validation

9.3.12.1.1 Purpose

The purpose of the test case is to execute the control outputs functional validation of TRXFE- GPIO signals.

9.3.12.1.2 Test and Measurement Method

This test is conducted by toggling the GPIO lines by using GPIO Sysfs Interface in Linux. Please refer to Section **5.2.12.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.12.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.12.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0010

Software versions – Linux 14.4.4

9.3.12.1.5 Test Results

The toggling of TRXFE- GPIO signals is verified.

9.3.12.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
TRXFE – GPIO: Control outputs							
NA							

The snapshots of execution of Control outputs functional validation of TRXFE- GPIO are attached herewith.


TRXFE_GPIO1_340.png


TRXFE_GPIO2_341.png


TRXFE_GPIO3_342.png


TRXFE_GPIO4_343.png

9.3.12.2 Test ID / Test Name: CPU.15.3 / Signaling characteristics

9.3.12.2.1 Purpose

The purpose of the test case is to validate the signal characteristics of TRXFE- GPIO signals.

9.3.12.2.2 Test and Measurement Method

This test is conducted by probing the TRXFE - GPIO lines before level shifter at R10546, R10547, R10548 and R10549 and after level shifter at R10542, R10543, R10528 and R10529 respectively and verifying the signal characteristics. The GPIO lines are toggled using GPIO Sysfs Interface in Linux. Please refer to Section **5.2.12.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.12.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.12.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0010

Software versions – Linux 14.4.4

9.3.12.2.5 Test Results

The signal characteristic of TRXFE- GPIO signals is within the requirement limits.

9.3.12.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification	Test result

				Min(V)	Max(V)	Design Margin (%)	
TRXFE - GPIO (Before Level Shifter)							
SOC_TRXFE_GPIO1	R10546	V_{LOW} (V)	0	0	0.63	-100.00	PASS
		V_{HIGH} (V)	1.8	1.17	1.8	0.00	PASS
		Positive Over-shoot (V)	0	0	0.18	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.18	-100.00	PASS
SOC_TRXFE_GPIO2	R10547	V_{LOW} (V)	0	0	0.63	-100.00	PASS
		V_{HIGH} (V)	1.8	1.17	1.8	0.00	PASS
		Positive Over-shoot (V)	0	0	0.18	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.18	-100.00	PASS
SOC_TRXFE_GPIO3	R10548	V_{LOW} (V)	0	0	0.63	-100.00	PASS
		V_{HIGH} (V)	1.8	1.17	1.8	0.00	PASS
		Positive Over-shoot (V)	0	0	0.18	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.18	-100.00	PASS
SOC_TRXFE_GPIO4	R10549	V_{LOW} (V)	0	0	0.63	-100.00	PASS
		V_{HIGH} (V)	1.8	1.17	1.8	0.00	PASS
		Positive Over-shoot (V)	0	0	0.18	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.18	-100.00	PASS
TRXFE - GPIO (After Level Shifter)							
ISO_SOC_TRXFE_GPIO1	R10542	V_{LOW} (V)	0	-0.3	0.8	100.00	PASS
		V_{HIGH} (V)	3.3	2	3.6	-8.33	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.33	-100.00	PASS
ISO_SOC_TRXFE_GPIO2	R10543	V_{LOW} (V)	0	-0.3	0.8	100.00	PASS
		V_{HIGH} (V)	3.3	2	3.6	-8.33	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.33	-100.00	PASS
ISO_SOC_TRXFE_GPIO3	R10528	V_{LOW} (V)	0	-0.3	0.8	100.00	PASS
		V_{HIGH} (V)	3.3	2	3.6	-8.33	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.33	-100.00	PASS
ISO_SOC_TRXFE_GPIO4	R10529	V_{LOW} (V)	0	-0.3	0.8	100.00	PASS
		V_{HIGH} (V)	3.3	2	3.6	-8.33	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.33	-100.00	PASS

The detailed analysis report with waveform captured for Signaling characteristics of TRXFE- GPIO is embedded in the xls document attached herewith.

TRXFE_GPIO.xlsx

9.3.13 TIVA –GPIO

9.3.13.1 Test ID / Test Name: CPU.17.1 / Control inputs functional validation

9.3.13.1.1 Purpose

The purpose of the test case is to execute the control inputs functional validation of TIVA-GPIO signals.

9.3.13.1.2 Test and Measurement Method

This test is conducted by toggling the GPIO lines from TIVA controller using CCS software and checking the status of the GPIO lines in SOC by using GPIO Sysfs Interface in Linux. Please refer to Section **5.2.13.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.13.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.13.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0010

Software versions – Linux 14.4.4

9.3.13.1.5 Test Results

The toggling of TIVA- GPIO signals is verified.

9.3.13.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
TIVA - GPIO: Control inputs							

NA

The snapshots of execution of control inputs functional validation of TIVA- GPIO is attached herewith.


GPIO2_FV_TIVA.png


GPIO2_FV_SOC.png

9.3.13.2 Test ID / Test Name: CPU.17.2 / Control outputs functional validation

9.3.13.2.1 Purpose

The purpose of the test case is to execute the control outputs functional validation of TIVA-GPIO signals.

9.3.13.2.2 Test and Measurement Method

This test is conducted by toggling the GPIO lines by using GPIO Sysfs Interface in Linux. Please refer to Section **5.2.13.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.13.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.13.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0010

Software versions – Linux 14.4.4

9.3.13.2.5 Test Results

The toggling of TIVA- GPIO signals is verified and TIVA_SOC_GPIO1 fails.

9.3.13.2.6 Measurement Logs

Test			Observation	Specification		

	Measuring Point	Measuring Criteria		Min	Max	Design Margin (%)	Test result
TIVA - GPIO: Control outputs							
NA							

The snapshots of execution of Control outputs functional validation of TIVA- GPIO is attached herewith.


tiva_soc_gpio1_gpio468.png


tiva_soc_gpio2_gpio469.png

9.3.13.3 Test ID / Test Name: CPU.17.3 / Signaling characteristics

9.3.13.3.1 Purpose

The purpose of the test case is to validate the signal characteristics of TIVA- GPIO signals.

9.3.13.3.2 Test and Measurement Method

This test is conducted by probing the GPIO2 signal at R10514 before level shifter and at R10516 after level shifter and verifying the signal characteristics. The GPIO line is toggled using GPIO Sysfs Interface in Linux. Please refer to Section **5.2.13.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.13.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.13.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0010

Software versions – Linux 14.4.4

9.3.13.3.5 Test Results

The signal characteristic of TIVA- GPIO signals is within the requirement limits.

9.3.13.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min(V)	Max(V)		
TIVA_GPIO (Before Level Shifter)							
ISO_TIVA_SOC_GPIO2	R10514	V_{LOW} (V)	0	0.00	0.63	-100.00	PASS
		V_{HIGH} (V)	1.8	1.17	1.80	0.00	PASS
		Positive Over-shoot (V)	0	0.00	0.18	-100.00	PASS
		Negative Over-shoot (V)	0	0.00	0.18	-100.00	PASS
TIVA_GPIO (After Level Shifter)							
TIVA_SOC_GPIO2	R10516	V_{LOW} (V)	0	0.00	1.16	-100.00	PASS
		V_{HIGH} (V)	3.3	2.15	4.00	-17.50	PASS
		Positive Over-shoot (V)	0.3	0.00	0.33	-9.09	PASS
		Negative Over-shoot (V)	0.1	0.00	0.33	-69.70	PASS

The detailed analysis report with waveform captured for signaling characteristics of TIVA-GPIO is embedded in the xls document attached herewith.

TIVA_GPIO.xlsx

9.3.14 TRXFE- FX3 - USB 2.0

9.3.14.1 Test ID / Test Name: CPU.19.1 / Electrical validation

9.3.14.1.1 Purpose

The purpose of the test case is to validate the electrical characteristics of USB2.0 interface between GBC and RF-SDR.

9.3.14.1.2 Test and Measurement Method

This test is conducted by probing the USB2.0 signal at R206.2 (USB_DP0), R208.2 (USB_DN0).Capture one frame of data (USB 2.0 signals) and save as .csv format. Then input this file to USBET20 tool. This will produces the familiar .html results files of the analysis. Please refer to Section **5.2.14.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.14.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.14.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021
Debug board Serial Number - WZ1628LIFE2DEBUG0018

RF-SDR Board Serial Number - WZ1630LIFE2SDR0006

Software versions – Linux 14.4.4

9.3.14.1.5 Test Results

The electrical characteristics of USB2.0 interface between GBC and RF-SDR is verified.

9.3.14.1.6 Measurement Logs

The detailed analysis report generated by "USBET20" tool for FX3-USB2.0 - Electrical validation is attached herewith.

FX3_USB2.0.zip

9.3.14.2 Test ID / Test Name: CPU.19.2 / Throughput measurement

9.3.14.2.1 Purpose

The purpose of the test case is to validate USB 2.0 throughput.

9.3.14.2.2 Test and Measurement Method

This test is conducted by Installing the FX3 Utility and running the installation script. (./install.sh). The cyusb_linux application is run. The process is started under the Data Transfers tab. Please refer to Section **5.2.14.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.14.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.14.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – Linux 14.4.4 with cyusb_linux application

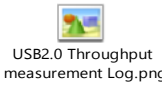
9.3.14.2.5 Test Results

The throughput of USB2.0 is 22.588 MB/s.

9.3.14.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
USB 2.0 - Throughput measurement							
NA							

The log of throughput measurement for USB 2.0 is attached herewith.


USB2.0 Throughput measurement Log.png

9.3.14.3 Test ID / Test Name: CPU.19.3 / Functional validation

9.3.14.3.1 Purpose

The purpose of the test case is to validate USB 2.0 interface between GBC and RF-SDR board.

9.3.14.3.2 Test and Measurement Method

This test is conducted by connecting debug board and RF-SDR board to GBC board and giving the command "**sudo uhd_usrp_probe**" in the terminal. Please refer to Section **5.2.14.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.14.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.14.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Debug board Serial Number - WZ1628LIFE2DEBUG0018

RF-SDR Board Serial Number - WZ1630LIFE2SDR0006

Software versions – Linux 14.4.4

9.3.14.3.5 Test Results

The functional validation of USB 2.0 interface between GBC and RF-SDR board is verified.

9.3.14.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
TRXFE- FX3 - USB 2.0							
NA							

The snapshot of functional validation of USB 2.0 interface between GBC and RF-SDR board is attached herewith.

TRXFE- FX3 - USB 2.0.png

9.3.15 TRXFE- FX3 - USB 3.0

9.3.15.1 Test ID / Test Name: CPU.20.2 / Throughput measurement

9.3.15.1.1 Purpose

The purpose of the test case is to validate USB 3.0 throughput.

9.3.15.1.2 Test and Measurement Method

This test is conducted by Installing the FX3 Utility and running the installation script. (./install.sh). The cyusb_linux application is run. The process is started under the Data Transfers tab after selecting streamer. Please refer to Section **5.2.15.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.15.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.15.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – Linux 14.4.4 with cyusb_linux application

9.3.15.1.5 Test Results

The throughput of USB3.0 is 240.007 MB/s.

9.3.15.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
USB 3.0 - Throughput measurement							
NA							

The log of throughput measurement for USB 3.0 is attached herewith.

USB3.0 Throughput measurement Log.p

9.3.15.2 Test ID / Test Name: CPU.20.3 / Functional validation

9.3.15.2.1 Purpose

The purpose of the test case is to validate USB 3.0 interface between GBC and RF-SDR board.

9.3.15.2.2 Test and Measurement Method

This test is conducted by connecting debug board and RF-SDR board to GBC board and giving the command "**sudo uhd_usrp_probe**" in the terminal. Please refer to Section **5.2.15.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.15.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.15.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Debug board Serial Number - WZ1628LIFE2DEBUG0018

RF-SDR Board Serial Number - WZ1630LIFE2SDR0006

Software versions – Linux 14.4.4

9.3.15.2.5 Test Results

The functional validation of USB 3.0 interface between GBC and RF-SDR board is verified.

9.3.15.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
TRXFE- FX3 - USB 3.0							
NA							

The snapshot of functional validation of USB 3.0 interface between GBC and RF-SDR is attached herewith.

TRXFE- FX3 - USB 3.0.png

9.3.16 Debug USB 2.0

9.3.16.1 Test ID / Test Name: CPU.21.1 / Functional validation

9.3.16.1.1 Purpose

The purpose of the test case is to validate USB 2.0 in debug board.

9.3.16.1.2 Test and Measurement Method

This test is conducted by connecting debug board to GBC board and connecting a USB 2.0 in debug board and giving the command "**lsusb –t**"/" **lsusb -v**" in the terminal. Please refer to Section **5.2.16** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.16.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.16.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Debug board Serial Number - WZ1628LIFE2DEBUG001

Software versions – Linux 14.4.4

9.3.16.1.5 Test Results

The functional validation of USB 2.0 in debug board is verified.

9.3.16.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Debug USB 2.0							
NA							

The snapshots of functional validation of USB 2.0 in debug board are attached herewith.


USB2.0_FV_1.png


USB2.0_FV_2.png

9.3.17 Debug USB 3.0

9.3.17.1 Test ID / Test Name: CPU.22.1 / Functional validation

9.3.17.1.1 Purpose

The purpose of the test case is to validate USB 3.0 in debug board.

9.3.17.1.2 Test and Measurement Method

This test is conducted by connecting debug board to GBC board. Board is turned on with CoreBoot loaded. Once Linux comes up, the USB3.0 signals at USB switch (U48) is routed to debug connector by toggling operation mode select pin of Mux/Demux switch (U48) using GPIO Sysfs Interface in Linux. A USB3.0 pen drive/HDD is connected to debug port and "lsusb –t" command is given in the terminal which shows the device is listed under USB3.0 Bus/Hub. This confirms that the USB3.0 enumeration is happening at GBC. Please refer to Section **5.2.17** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.17.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.17.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Debug board Serial Number - WZ1628LIFE2DEBUG0018

Software versions – Linux 14.4.4

9.3.17.1.5 Test Results

The functional validation of USB 3.0 in debug board is verified.

9.3.17.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Debug USB 3.0							
NA							

The snapshots of functional validation of USB 3.0 in debug board are attached herewith.

USB3.0_FV.jpg

9.3.18 Debug - Ethernet

9.3.18.1 Test ID / Test Name: CPU.23.1 / Functional validation

9.3.18.1.1 Purpose

The purpose of the test case is to validate Ethernet port in debug board.

9.3.18.1.2 Test and Measurement Method

This test is conducted by connecting debug board to GBC board and connecting a PC to the Ethernet port of debug board. The connection between GBC system and the external PC is verified using "ping" command. Please refer to Section **5.2.18** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.18.1.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.3.18.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002
Debug board Serial Number - WZ1628LIFE2DEBUG0018
Software versions – Linux 14.4.4

9.3.18.1.5 Test Results

The functional validation of Ethernet port in debug board is verified.

9.3.18.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Debug - Ethernet							
NA							

The snapshots of functional validation of Ethernet port in debug board are attached herewith.


Debug_Ethernet_FV
_Complete_Setup.jpg


Debug_Ethernet_FV
_GBC.png


Debug_Ethernet_FV
_PC.png

9.3.19 Display-HDMI

9.3.19.1 Test ID / Test Name: CPU.24.1 / Functional validation with debug port

9.3.19.1.1 Purpose

The purpose of the test case is to validate HDMI port in debug board.

9.3.19.1.2 Test and Measurement Method

This test is conducted by connecting debug board to GBC board and connecting a monitor to the HDMI port of debug board. Please refer to Section **5.2.19** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.19.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.19.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Debug board Serial Number - WZ1628LIFE2DEBUG0018

Software versions – Linux 14.4.4

9.3.19.1.5 Test Results

The functional validation of HDMI port in debug board is verified.

9.3.19.1.6 Measurement Logs

Test			Observation	Specification		

	Measuring Point	Measuring Criteria		Min	Max	Design Margin (%)	Test result
Display-HDMI							
NA							

The snapshots of functional validation of HDMI port in debug board are attached herewith.


Display_HDMI_FV_1.jpg


Display_HDMI_FV_2.jpg

9.3.20 Debug - UART

9.3.20.1 Test ID / Test Name: CPU.25.1 / Functional validation

9.3.20.1.1 Purpose

The purpose of the test case is to validate UART interface in debug board.

9.3.20.1.2 Test and Measurement Method

This test is conducted by connecting debug board to GBC board and connecting a PC (with Docklight software) to the USB port (J1N4) of debug board. The Docklight software will be running in the PC. The Intel Atom processor sends boot log through the USB port to the PC during board power up. The data sent can be verified in the application software. Please refer to Section **5.2.20** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.20.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.3.20.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0002

Debug board Serial Number - WZ1628LIFE2DEBUG0018

Software versions – Linux 14.4.4

9.3.20.1.5 Test Results

The functional validation of UART interface in debug board is verified.

9.3.20.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Debug-UART							
NA							

The log of functional validation of UART interface in debug board is attached herewith.

Boot log.txt

9.3.21 RFSDR – PCIe

9.3.21.1 Test ID / Test Name: CPU.26.1 and CPU26.2 / RFSDR-PCIe0

9.3.21.1.1 Purpose

The purpose of this test case is to check and validate the electrical parameters and signal integrity of PCIe interface at 5GT/s between Intel processor (U3) and RFSDR board.

9.3.21.1.2 Test and Measurement Method

- Transmitter Tests:

1. Terminate PCIe transmitter lane 0 lines with a 50-ohm resistor. By doing so, PCIe compliance pattern as per section *4.2.8* of PCIe base specification ver. *2.1* is generated.
2. For low power mode: voltage swing of PCIE signals from 600mV to 800V), modify bit 9:7 of "LCTL2_LSTS2" register with offset 70h to 010b
3. From AWG (arbitrary waveform generator), generate bursts a 100MHz signal for 1ms duration. Connect the output of AWG to *PCIE0_RXP*. This ensures the PCIe Tx lines to be transmitting data at 5GT/s speed.
4. Probe PCIE0_TXP PCIE0_TXN at C2000.1 and C1999.1 respectively.

5. Run the test utility N5393D in the infiniium oscilloscope. To configure the test suite, select PCIe version as 2.0, Transmitter tests, Device1, Lan01, and speed as 5GT/s. In select tests option in utility, select transmitter tests and run all the selected test cases.
6. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin.

   Please refer to Section **5.2.21** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.3.21.1.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +18V DC

System load –Typical

9.3.21.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software version – NA

9.3.21.1.5 Test Results

The test result generated by the test utility should be within the mentioned range in the PCIe Ver.*2.1* base specification.

9.3.21.1.6 Measurement Logs

PCIe0 - 5GT/s_ -6dB Full power level - Writing to register 70h						
Sl. No	**Test Name**	**Measured Value**	**Pass Margin**		**% Pass Margin**	**PASS / FAIL**
			Min	**Max**		
1	Unit Interval Test (UI) (ps)	200.013	199.94	200.06	39.2	PASS
2	Rise/Fall time (ps)	50.63	30	>30	68.8	PASS
3	Tmin - Pulse(mUI)	938	900	>900	4.2	PASS
4	Deemphasized Voltage Ratio - 3.5dB (dB)	-2.8	-4.5	-2.5	15	PASS
5	Deterministic Jitter > 1.5 MHz (mUI)	32	<150	150	78.7	PASS
6	Random Jitter < 1.5 MHz(ps)	1.72	<3	3	42.7	PASS
7	Template Test	-	-	-	100	PASS

8	Eye Width(mUI)	846	750	>750	12.8	PASS
9	Peak Differential Output Voltage(Transition) (mV)	722.9	400	1200	40.4	PASS
10	Peak Differential Output Voltage (Non -Transition) (mV)	523.4		1200	29.7	PASS

The detailed analysis report for PCIe 0 – RFSDR transmitter test case executed for the above case is attached herewith.

PCIE_low swing.zip

9.4 TIVA

9.4.1 TIVA Access

9.4.1.1 Test ID / Test Name: TIV.1.1 / Configuration

9.4.1.1.1 Purpose

The purpose of this test case is to access TIVA through JTAG and configuring with the help of CCS debug software.

9.4.1.1.2 Test and Measurement Method

Connect debug board to a GBC board. To access CCS debug software, connect USB cable from host PC to connector J1N2 on debug board. Configure the debugger in CCS, and load the program onto TIVA (U72). Please refer to Section **6.2.1.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.1.1.3 Test Condition

Ambient Temperature - 25˚C

Operating Voltage - +18V DC

System load –Typical

9.4.1.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0021

Software versions – TIVA RTOS code

9.4.1.1.5 Test Results

Program is successfully loaded into TIVA through CCS debug software.

9.4.1.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
TIVA Configuration							
NA							


CCS_configuration.JPG


Tiva_Configuration.PNG

9.4.1.2 Test ID / Test Name: TIV.1.2 / System Reset sequence

9.4.1.2.1 Purpose

The purpose of the test case is to validate TIVA system reset sequence.

9.4.1.2.2 Test and Measurement Method

This test is conducted by probing the signals “TIVA_RESET_TO_PROC”, “TIVA_ETHSW_RESET”, “TIVA_TRXFE_RESET”, “TIVA_SYNC_RESET” at R10523, R10438, 0165 and R10519 respectively. The TIVA system reset sequence.is measured while resetting the system from TIVA controller. Please refer to Section **6.2.1.3** in latest version of “OC_CONNECT_1_GBC_Test_Specification” document for detailed test procedure.

9.4.1.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.1.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0004

Debug board Serial Number - WZ1628LIFE2DEBUG0018

Software versions – TIVA RTOS code

9.4.1.2.5 Test Results

TIVA system reset sequence is verified and is in the following order.

1. TIVA_RESET_TO_PROC
2. TIVA_ETHSW_RESET
3. TIVA_TRXFE_RESET
4. TIVA_SYNC_RESET

9.4.1.2.6 Measurement Logs

Sl.No	Measurement Points	Measured sequence	Specification	Design Margin (%)	Result
			Expected sequence		
TIVA system reset sequence					
1	R10523	TIVA_RESET_TO_PROC	TIVA_RESET_TO_PROC	NA	PASS
2	R10438	TIVA_ETHSW_RESET	TIVA_ETHSW_RESET		
3	R10165	TIVA_TRXFE_RESET	TIVA_TRXFE_RESET		
4	R10519	TIVA_SYNC_RESET	TIVA_SYNC_RESET		

NOTE: There is no time delay requirement for the System reset sequence.

The detailed analysis report with waveform captured for TIVA system reset sequence is embedded in the xls document attached herewith.

TIVA_System_Reset_Sequence.xlsx

9.4.2 PSE – I2C (LTC4274AIUHF)

9.4.2.1 Test ID / Test Name: TIV.2.1 / Electrical validation

9.4.2.1.1 Purpose

The purpose of the test case is to validate the electrical characteristics of I2C interface of PSE controller.

9.4.2.1.2 Test and Measurement Method

This test is conducted by probing the I2C signal at U206.2 (TIVA_PSE_I2C8_SDA) and U206.3 (TIVA_PSE_I2C8_SCLK) before isolator, U206.7 (PSE_I2CSDA) and U206.6 (PSE_I2CSCL) after isolator on the GBC board. The measured values are well with-in the limit as specified in the I2C isolator and PSE datasheet specification. Please refer to Section **6.2.2.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure

9.4.2.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.2.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.2.1.5 Test Results

The electrical characteristics of I2C interface with PSE is within the designed spec.

9.4.2.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
PSE (Before Isolator)							
TIVA_PSE_I2C8_SCLK	U206.3	VLOW (max) (V)	0	0	0.5	-100.00	PASS
		VHIGH (min) (V)	3.3	2.31	3.3	0.00	PASS
		Rise time (ns)	964	0	1000	-3.60	PASS
		Fall time (ns)	32.8	0	300	-89.07	PASS
		Frequency (kHz)	96.15	0	100	-3.85	PASS
TIVA_PSE_I2C8_SDA	U206.2	VLOW (max) (V)	0.26	0	0.5	-48.00	PASS
		VHIGH (min) (V)	3	2.31	3.3	-9.09	PASS
		Rise time (ns)	240	0	1000	-76.00	PASS
		Fall time (ns)	36.4	0	300	-87.87	PASS
PSE (After Isolator)							
PSE_I2CSCL	U206.6	VLOW (max) (V)	-0.08	-0.5	0.8	84.00	PASS
		VHIGH (min) (V)	3.06	2.2	3.8	-19.47	PASS
		Rise time (ns)	492	0	1000	-50.80	PASS
		Fall time (ns)	49	0	300	-83.67	PASS
		Frequency (kHz)	96.9	0	100	-3.10	PASS

PSE_I2CSDA	U206.7	VLOW (max) (V)	-0.1	-0.5	0.8	80.00	PASS
		VHIGH (min) (V)	2.8	2.2	3.8	-26.32	PASS
		Rise time (ns)	488	0	1000	-51.20	PASS
		Fall time (ns)	47	0	300	-84.33	PASS

The detailed analysis report with waveform captured for PSE I2C - Electrical validation is embedded in the xls document attached herewith.

PSE I2C Electrical Validation.xlsx

9.4.2.2 Test ID / Test Name: TIV.2.2 / Signal Integrity

9.4.2.2.1 Purpose

The purpose of the test case is to validate the signal integrity of I2C interface of PSE controller.

9.4.2.2.2 Test and Measurement Method

This test is conducted by probing the I2C signal at U206.2 (TIVA_PSE_I2C8_SDA) and U206.3 (TIVA_PSE_I2C8_SCLK) before isolator, U206.7 (PSE_I2CSDA) and U206.6 (PSE_I2CSCL) after isolator on the GBC board. The measured values are well with-in the limit as specified in the I2C isolator and PSE datasheet specification. Please refer to Section **6.2.2.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.2.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.2.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.2.2.5 Test Results

The Signal integrity characteristics of I2C interface with PSE is within the designed spec.

9.4.2.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
PSE (Before Isolator)							
TIVA_PSE_I2C8_SCLK	U206.3	Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.33	-100.00	PASS
TIVA_PSE_I2C8_SDA	U206.2	data set-up time (ns)	1750	240	10000	-82.50	PASS
		data hold time (ns)	2980	240	10000	-70.20	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.33	-100.00	PASS
PSE (After Isolator)							
PSE_I2CSCL	U206.6	Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.16	0	0.33	-51.52	PASS
PSE_I2CSDA	U206.7	data set-up time (ns)	2500	240	10000	-75.00	PASS
		data hold time (ns)	2980	240	10000	-70.20	PASS
		Positive Over-shoot (V)	0.18	0	0.33	-45.45	PASS
		Negative Over-shoot (V)	0.24	0	0.33	-27.27	PASS

The detailed analysis report with waveform captured for PSE I2C - Signal Integrity is embedded in the xls document attached herewith.

TIVA PSE I2C Signal Integrity.xlsx

9.4.2.3 Test ID / Test Name: TIV.2.3 / Functional validation

9.4.2.3.1 Purpose

The purpose of the test case is to validate the I2C interface of PSE controller.

9.4.2.3.2 Test and Measurement Method

This test is conducted by reading I2C8 bus at address 2FH and read back the device ID 70H. Please refer to Section **6.2.2.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.2.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.2.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.2.3.5 Test Results

TIVA is able to read device ID from PSE device.

9.4.2.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
PSE							
NA							

The snapshot of functional validation of PSE I2C is attached herewith.

PSE I2C Validation.png

9.4.3 Power Monitor (INA226) – I2C

9.4.3.1 Test ID / Test Name: TIV.3.1 / Electrical validation

9.4.3.1.1 Purpose

The purpose of the test case is to validate the electrical characteristics of I2C interface of Power monitor IC.

9.4.3.1.2 Test and Measurement Method

This test is conducted by probing the I2C signal at U182.5 (SCL), U182.4 (SDA). The measured values are well with-in the limit as specified in the INA226 power monitor datasheet specification. Please refer to Section **6.2.3.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.3.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.3.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.3.1.5 Test Results

The electrical characteristics of I2C interface of power monitor is within the designed spec.

9.4.3.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Power Monitor (INA226) - U185							
TIVA_PWRMNTR_I2C6_SCLK	U185.5	VLOW (max) (V)	0	-0.5	0.99	100.00	PASS
		VHIGH (min) (V)	3.3	2.31	6	-42.86	PASS
		Rise time (ns)	720	0	1000	-28.00	PASS
		Fall time (ns)	19.6	0	300	-93.47	PASS
		Frequency (kHz)	96.52	0	100	-3.48	PASS
TIVA_PWRMNTR_I2C6_SDA	U185.4	VLOW (max) (V)	0	-0.5	0.99	100.00	PASS
		VHIGH (min) (V)	3.4	2.31	6	-43.33	PASS
		Rise time (ns)	704	0	1000	-29.60	PASS
		Fall time (ns)	52	0	300	-82.67	PASS

NOTE:

1) Rise time and fall time passes for t70%-30%. Values are taken for t10%-90%.
2) Re-measurement taken by changing the pull-up value from 10K to 4.75K and Rise time and Fall time passes.

The detailed analysis report with waveform captured for Power Monitor I2C - Electrical validation is embedded in the xls document attached herewith.

Power Monitor I2C Electrical validation.

9.4.3.2 Test ID / Test Name: TIV.3.2 / Signal Integrity

9.4.3.2.1 Purpose

The purpose of the test case is to validate the signal integrity of I2C interface of Power monitor IC.

9.4.3.2.2 Test and Measurement Method

This test is conducted by probing the I2C signal at U182.5 (SCL), U182.4 (SDA). The measured values are well with-in the limit as specified in the I2C specification standard, please refer to Section **6.2.3.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.3.2.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.4.3.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.3.2.5 Test Results

The Signal integrity characteristics of I2C interface with Current and Power monitor IC is within the designed spec.

9.4.3.2.6 Measurement Logs

Test		Measuring Criteria	Observation	Specification		

	Measuring Point			Min	Max	Design Margin (%)	Test result
Power Monitor (INA226) - U185							
TIVA_PWRMNTR_I2C6_SCLK	U185.5	Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.3	0	0.33	-9.09	PASS
TIVA_PWRMNTR_I2C6_SDA	U185.4	data set-up time (ns)	1700	250	10000	-83.00	PASS
		data hold time (ns)	3000	300	10000	-70.00	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.12	0	0.33	-63.64	PASS

The detailed analysis report with waveform captured for Power Monitor I2C - Signal Integrity is embedded in the xls document attached herewith.

Power Monitor I2C Signal Integrity.xlsx

9.4.3.3 Test ID / Test Name: TIV.3.3 / Functional validation

9.4.3.3.1 Purpose

The purpose of the test case is to validate the I2C interface of Power monitor IC.

9.4.3.3.2 Test and Measurement Method

This test is conducted by reading I2C6 bus at address 40H and Manufacture ID, 5449 is read from Address FEh. Please refer to Section **6.2.3.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.3.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.3.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.3.3.5 Test Results

TIVA is able to access the power monitor through I2C bus and read Manufacture ID from the device.

9.4.3.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Power Monitor							
NA							

The snapshots of functional validation of Power Monitor are attached herewith.


Power_Monitor_I2C_FV_1.png


Power_Monitor_I2C_FV_1.png

9.4.4 RF-SDR board – I2C (PCA9557PW,118)

9.4.4.1 Test ID / Test Name: TIV.4.1 / Electrical validation

9.4.4.1.1 Purpose

The purpose of the test case is to validate the electrical characteristics of I2C interface of IO expander in RF-SDR board.

9.4.4.1.2 Test and Measurement Method

This test is conducted by probing the I2C signal at R1089.2 and R2034 (SCL), R1088.2 and R2033 (SDA) at RF SDR Board while it's integrated with GBC board. The measured values are well with-in the limit as specified in the PCA9557 IO expander datasheet specification. Please refer to Section **6.2.4.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure

9.4.4.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.4.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.4.1.5 Test Results

The electrical characteristics of I2C interface with IO expander is within the designed spec.

9.4.4.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
RF-SDR IO Exp- I2C (Before Level Shifter)							
TIVA_TRXFECONN_I2C2_SCLK	R1089.2	VLOW (max) (V)	0	-0.5	0.99	100.00	PASS
		VHIGH (min) (V)	3.3	2.31	5.5	-40.00	PASS
		Rise time (ns)	216	0	300	-28.00	PASS
		Fall time (ns)	2.3	0	300	-99.23	PASS
		Frequency (kHz)	357.1	0	400	-10.73	PASS
TIVA_TRXFECONN_I2C2_SDA	R1088.2	VLOW (max) (V)	0	-0.5	0.99	100.00	PASS
		VHIGH (min) (V)	3.3	2.31	5.5	-40.00	PASS
		Rise time (ns)	244	0	300	-18.67	PASS
		Fall time (ns)	2.8	0	300	-99.07	PASS
RF-SDR IO Exp- I2C (After Level Shifter)							
SYS_I2C_2_SCL	R2034	VLOW (max) (V)	0.4	-0.5	0.99	180.00	PASS
		VHIGH (min) (V)	2.8	2.31	5.5	-21.21	PASS
		Rise time (ns)	56	0	300	-81.33	PASS
		Fall time (ns)	35	0	300	-88.33	PASS
		Frequency (kHz)	357.1	0	400	-10.73	PASS
SYS_I2C_2_SDA	R2033	VLOW (max) (V)	0.4	-0.5	0.99	180.00	PASS
		VHIGH (min) (V)	2.8	2.31	5.5	-21.21	PASS
		Rise time (ns)	64	0	300	-78.67	PASS
		Fall time (ns)	42	0	300	-86.00	PASS

The detailed analysis report with waveform captured for RF SDR IO Expander I2C - Electrical validation is embedded in the xls document attached herewith.

RF SDR IO Exp I2C Electrical validation.

9.4.4.2 Test ID / Test Name: TIV.4.2 / Signal Integrity

9.4.4.2.1 Purpose

The purpose of the test case is to validate the signal integrity of I2C interface of IO expander in RF-SDR board.

9.4.4.2.2 Test and Measurement Method

This test is conducted by probing the I2C signal at R1089.2 and R2034 (SCL), R1088.2 and R2033 (SDA) at RF SDR Board. The measured values are well with-in the limit as specified in the PCA9557 IO expander datasheet specification. Please refer to Section **6.2.4.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.4.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.4.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.4.2.5 Test Results

The Signal integrity characteristics of I2C interface with IO expander is within the designed spec.

9.4.4.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
RF-SDR IO Exp (Before Level Shifter)							
TIVA_TRXFECONN_I2C2_SCLK	R1089.2	Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.33	-100.00	PASS

TIVA_TRXFECONN_I2C2_SDA	R1088.2	data set-up time (ns)	456	100	2500	-81.76	PASS
		data hold time (ns)	548	300	2500	-78.08	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.1088	0	0.33	-67.03	PASS
RF-SDR IO Exp (After Level Shifter)							
SYS_I2C_2_SCL	R2034	Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.22	0	0.33	-33.33	PASS
SYS_I2C_2_SDA	R2033	data set-up time (ns)	664	100	2500	-73.44	PASS
		data hold time (ns)	330	300	2500	-10.00	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.22	0	0.33	-33.33	PASS

The detailed analysis report with waveform captured for RF SDR IO Expander I2C - Signal Integrity is embedded in the xls document attached herewith.

RF SDR IO Exp I2C Signal Integrity.xlsx

9.4.4.3 Test ID / Test Name: TIV.4.3 / Functional validation

9.4.4.3.1 Purpose

The purpose of the test case is to validate the I2C interface of IO expander in RF-SDR board.

9.4.4.3.2 Test and Measurement Method

This test is conducted by reading I2C2 bus and writing data in input register. Register 0x3 is written with value 0xfe (slave address 0x1b) and Register 0x1 is written with value 0xaa (slave address 0x1e). Please refer to Section 6.2.4.4 in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.4.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.4.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.4.3.5 Test Results

TIVA is able to write data in input register of IO expander.

9.4.4.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
RF SDR IO Exp							
NA							

The snapshot of functional validation of IO Expander in RF-SDR Board is attached herewith.

RF-SDR_board_I2C.png

9.4.5 Temp Sensor (SE98ATP, 547) – I2C

9.4.5.1 Test ID / Test Name: TIV.5.1 / Electrical validation

9.4.5.1.1 Purpose

The purpose of the test case is to validate the electrical characteristics of I2C interface of temperature sensor.

9.4.5.1.2 Test and Measurement Method

This test is conducted by probing the I2C signal at R10255.2/ R10221.2 (SCL), R10256.2/ R10222.2 (SDA). The measured values are well with-in the limit as specified in the SE98ATP, 547 Temp sensor datasheet specification. Please refer to Section **6.2.5.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.5.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.5.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.5.1.5 Test Results

The electrical characteristics of I2C interface of temperature sensor is within the designed spec.

9.4.5.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Temp Sensor - U215 (Near Tiva)							
TIVA_TEMPSEN_I2C1_SCLK	R10255.2	VLOW (max) (V)	0	-0.5	0.99	100.00	PASS
		VHIGH (min) (V)	3.4	2.31	4.3	-20.93	PASS
		Rise time (ns)	570	0	1000	-43.00	PASS
		Fall time (ns)	16	0	300	-94.67	PASS
		Frequency (kHz)	94.34	0	100	-5.66	PASS
TIVA_TEMPSEN_I2C1_SDA	R10256.2	VLOW (max) (V)	0	-0.5	0.99	100.00	PASS
		VHIGH (min) (V)	3.4	2.31	4.3	-20.93	PASS
		Rise time (ns)	600	0	1000	-40.00	PASS
		Fall time (ns)	16	0	300	-94.67	PASS
Temp Sensor - U210 (Far from Tiva)							
TIVA_TEMPSEN_I2C1_SCLK	R10221.2	VLOW (max) (V)	0	-0.5	0.99	100.00	PASS
		VHIGH (min) (V)	3.3	2.31	4.3	-23.26	PASS
		Rise time (ns)	570	0	1000	-43.00	PASS
		Fall time (ns)	18	0	300	-94.00	PASS
		Frequency (kHz)	94.34	0	100	-5.66	PASS
TIVA_TEMPSEN_I2C1_SDA	R10222.2	VLOW (max) (V)	0	-0.5	0.99	100.00	PASS
		VHIGH (min) (V)	3.3	2.31	4.3	-23.26	PASS
		Rise time (ns)	600	0	1000	-40.00	PASS
		Fall time (ns)	36	0	300	-88.00	PASS

The detailed analysis report with waveform captured for Temp Sensor I2C - Electrical validation is embedded in the xls document attached herewith.

Temp Sensor I2C Electrical validation.

9.4.5.2 Test ID / Test Name: TIV.5.2 / Signal Integrity

9.4.5.2.1 Purpose

The purpose of the test case is to validate the signal integrity of I2C interface of temperature sensor.

9.4.5.2.2 Test and Measurement Method

This test is conducted by probing the I2C signal at R10255.2/ R10221.2 (SCL), R10256.2/ R10222.2 (SDA). The measured values are well with-in the limit as specified in the I2C specification standard, but need tweaking the layout design for better HOLD time. Please refer to Section **6.2.5.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.5.2.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.4.5.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.5.2.5 Test Results

The Signal integrity characteristics of I2C interface with temperature sensor is within the designed spec except the Hold time which needs tweaking in layout design in next version.

9.4.5.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Temp Sensor - U215 (Near Tiva)							
TIVA_TEMPSEN_I2C1_SCLK	R10255.2	Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.2	0	0.33	-39.39	PASS
TIVA_TEMPSEN_I2C1_SDA	R10256.2	data set-up time (ns)	2460	250	10000	-75.40	PASS
		data hold time (ns)	3000	200	3450	-13.04	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.3	0	0.33	-9.09	PASS
Temp Sensor - U210 (Far from Tiva)							
TIVA_TEMPSEN_I2C1_SCLK	R10221.2	Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.3	0	0.33	-9.09	PASS
TIVA_TEMPSEN_I2C1_SDA	R10222.2	data set-up time (ns)	2460	250	10000	-75.40	PASS
		data hold time (ns)	3000	200	3450	-13.04	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.2	0	0.33	-39.39	PASS

The detailed analysis report with waveform captured for Temp Sensor I2C - Signal Integrity is embedded in the xls document attached herewith.

Temp Sensor I2C Signal Integrity.xlsx

9.4.5.3 Test ID / Test Name: TIV.5.3 / Functional validation

9.4.5.3.1 Purpose

The purpose of the test case is to validate the I2C interface of temperature sensor.

9.4.5.3.2 Test and Measurement Method

This test is conducted by reading I2C1 bus at address 18H, 19F, 1AH, 1CH, 1DH and 1FH. The Device ID is read from register 0x6 with value 0x1131. The Manufacture ID is read from register 0x7 with value 0xa102. Please refer to Section **6.2.5.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.5.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.5.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.5.3.5 Test Results

TIVA is able to access the temperature sensor through I2C bus and read manufacture ID from the device.

9.4.5.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Temp Sensor							
NA							

The snapshots of functional validation of temperature sensor are attached herewith.


Temp_Sesnor_I2C_FV_1.png


Temp_Sesnor_I2C_FV_2.png

9.4.6 Sync Board I2C (PCA9557PW,118)

9.4.6.1 Test ID / Test Name: TIV.6.1 / Electrical Validation

9.4.6.1.1 Purpose

The purpose of the test case is to validate the electrical characteristics of I2C interface of GPIO Expander in sync board.

9.4.6.1.2 Test and Measurement Method

This test is conducted by probing the I2C signal at U1.1-SCL (Near Via), U1.2-SDA (Near Via). The measured values are well with-in the limit as specified in the PCA9557PW,118 GPIO Expander datasheet specification. Please refer to Section **6.2.6.2** of 'SYNC Board' Test specifications (Rev 0.1) for detailed test procedure.

9.4.6.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.6.1.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0006

SYNC Board Serial Number- WZ1627LIFE1SYNC0011

Software versions – TIVA RTOS code

9.4.6.1.5 Test Results

The electrical characteristics of I2C interface with GPIO Expander is within the designed specification.

9.4.6.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Sync board – I2C (PCA9557PW,118)							
TIVA_SYNCCONN_I2C7_SCLK	U1.1	VLOW (max) (V)	-0.2	-0.5	0.99	60.00	PASS
		VHIGH (min) (V)	3.2	2.31	5.5	-38.53	PASS
		Rise time (ns)	450	0	1000	-55.00	PASS
		Fall time (ns)	5.6	0	300	-98.13	PASS
		Frequency (kHz)	90.9	0	100	-9.10	PASS
TIVA_SYNCCONN_I2C7_SDA	U1.2	VLOW (max) (V)	0	-0.5	0.99	100.00	PASS
		VHIGH (min) (V)	3.3	2.31	5.5	-40.00	PASS
		Rise time (ns)	450	0	1000	-55.00	PASS
		Fall time (ns)	39	0	300	-87.00	PASS

The detailed analysis report with waveform captured for Sync board I2C - Electrical validation is embedded in the xls document attached herewith.

Sync board I2C
Electrical validation.

9.4.6.2 Test ID / Test Name: TIV.6.2 / Signal Integrity

9.4.6.2.1 Purpose

The purpose of the test case is to validate the electrical characteristics of I2C interface of GPIO Expander in sync board.

9.4.6.2.2 Test and Measurement Method

This test is conducted by probing the I2C signal at U1.1-SCL (Near Via), U1.2-SDA (Near Via). The measured values are well with-in the limit as specified in the PCA9557PW,118 GPIO Expander datasheet specification. Please refer to Section **6.2.6.3** of 'SYNC Board' Test specifications (Rev 0.1) for detailed test procedure.

9.4.6.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.6.2.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0006

SYNC Board Serial Number- WZ1627LIFE1SYNC0011

Software versions – TIVA RTOS code

9.4.6.2.5 Test Results

The Signal Integrity characteristics of I2C interface with GPIO Expander is within the designed specification.

9.4.6.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Sync board – I2C (PCA9557PW,118)							
TIVA_SYNCCONN_I2C7_SCLK	U1.1	Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.33	-100.00	PASS

TIVA_SYNCCONN_I2C7_SDA	U1.2	data set-up time (ns)	2520	250	10000	-74.80	PASS
		data hold time (ns)	296	0	10000	-97.04	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.33	-100.00	PASS

The detailed analysis report with waveform captured for Sync board I2C - Signal Integrity is embedded in the xls document attached herewith.

Sync board I2C Signal Integrity.xlsx

9.4.6.3 Test ID / Test Name: TIV.6.3 / Functional Validation

9.4.6.3.1 Purpose

The purpose of the test case is to validate the I2C interface of GPIO expander in sync board.

9.4.6.3.2 Test and Measurement Method

This test is conducted by reading I2C7 bus at address 1FH. Input register data, 0x3 is written with value 0x1f. Please refer to Section **6.2.6.4** of 'SYNC Board' Test specifications (Rev 0.1) for detailed test procedure.

9.4.6.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.6.3.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0006

SYNC Board Serial Number- WZ1627LIFE1SYNC0011

Software versions – TIVA RTOS code

9.4.6.3.5 Test Results

TIVA is able to write data in input register of GPIO Expander in Sync board.

9.4.6.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
Sync board							
NA							

The snapshot of functional validation of GPIO Expander in SYNC Board is attached herewith.


Sync_board_I2C_FV.png

9.4.7 LED board – I2C (SX1509BIULTRT)

9.4.7.1 Test ID / Test Name: TIV.7.1 / Electrical validation

9.4.7.1.1 Purpose

The purpose of the test case is to validate the electrical characteristics of I2C interface of GPIO Expander in LED board.

9.4.7.1.2 Test and Measurement Method

This test is conducted by probing the I2C signal at R24.2 (SCL), R23.2 (SDA) at LED board while it's integrated with GBC board. The measured values are well with-in the limit as specified in the SX1509BIULTRT GPIO Expander datasheet specification. Please refer to Section **6.2.7.2** of 'LED Board' Test specifications (Rev 0.1) for detailed test procedure.

9.4.7.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.7.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0006

Software versions – TIVA RTOS code

9.4.7.1.5 Test Results

The electrical characteristics of I2C interface with GPIO Expander is within the designed spec.

9.4.7.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
LED board – I2C (SX1509BIULTRT)							
LED_I2C_SCL	U1.25	VLOW (max) (V)	0	-0.4	0.99	100.00	PASS
		VHIGH (min) (V)	3.3	2.31	3.3	0.00	PASS
		Rise time (ns)	630	0	1000	-37.00	PASS
		Fall time (ns)	30.4	0	300	-89.87	PASS
		Frequency (kHz)	83.33	0	100	-16.67	PASS
LED_I2C_SDA	U1.24	VLOW (max) (V)	0.2	-0.4	0.99	150.00	PASS
		VHIGH (min) (V)	3	2.31	3.3	-9.09	PASS
		Rise time (ns)	760	0	1000	-24.00	PASS
		Fall time (ns)	60	0	300	-80.00	PASS

The detailed analysis report with waveform captured for LED board I2C - Electrical validation is embedded in the xls document attached herewith.

LED board I2C Electrical validation.

9.4.7.2 Test ID / Test Name: TIV.7.2 / Signal Integrity

9.4.7.2.1 Purpose

The purpose of the test case is to validate the Signal characteristics of I2C interface of GPIO Expander in LED board.

9.4.7.2.2 Test and Measurement Method

This test is conducted by probing the I2C signal at R24.2 (SCL), R23.2 (SDA). The measured values are well with-in the limit as specified in the SX1509BIULTRT GPIO Expander

datasheet specification. Please refer to Section **6.2.7.3** of 'LED Board' Test specifications (Rev 0.1) for detailed test procedure.

9.4.7.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.7.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0006

Software versions – TIVA RTOS code

9.4.7.2.5 Test Results

The Signal Integrity characteristics of I2C interface with GPIO Expander is within the designed spec.

9.4.7.2.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
LED board – I2C (SX1509BIULTRT)							
LED_I2C_SCL	U1.25	Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0	0	0.33	-100.00	PASS
LED_I2C_SDA	U1.24	data set-up time (ns)	2760	250	10000	-72.40	PASS
		data hold time (ns)	3600	300	10000	-64.00	PASS
		Positive Over-shoot (V)	0	0	0.33	-100.00	PASS
		Negative Over-shoot (V)	0.3	0	0.33	-9.09	PASS

The detailed analysis report with waveform captured for LED board I2C - Signal Integrity is embedded in the xls document attached herewith.

LED board I2C Signal Integrity.xlsx

9.4.7.3 Test ID / Test Name: TIV.7.3 / Functional validation

9.4.7.3.1 Purpose

The purpose of the test case is to validate the I2C interface of GPIO Expander in LED board.

9.4.7.3.2 Test and Measurement Method

This test is conducted by reading I2C8 bus at address 3EH. Register REG_CLOCK is read with 0x0 and REG_MISC is read with 0x24. Please refer to Section **6.2.7.3** of 'LED Board' Test specifications (Rev 0.1) for detailed test procedure.

9.4.7.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.7.3.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0006

Software versions – TIVA RTOS code

9.4.7.3.5 Test Results

TIVA is able to registers of GPIO expander in LED board.

9.4.7.3.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
LED board							
NA							

The snapshot of functional validation of GPIO Expander in LED Board is attached herewith.

LED_board_I2C_FV.png

9.4.8 TIVA GPIO

9.4.8.1 Test ID / Test Name: TIV.10.1 / Control inputs functional validation

9.4.8.1.1 Purpose

The purpose of the test case is to execute the control inputs functional validation of TIVA-GPIO signals.

9.4.8.1.2 Test and Measurement Method

This test is conducted by toggling the GPIO lines which are input to TIVA through hardware.

Please refer to Section **6.2.8** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.8.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.8.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018

Software versions – NA

9.4.8.1.5 Test Results

Some TIVA- GPIO signals are toggling and some are not toggling.

NOTE: Resolution for failure – This is due to the design issue and this will be updated in the next version.

9.4.8.1.6 Measurement Logs

The list of result of control inputs functional validation of TIVA- GPIO is attached herewith.

TIVA GPIO_Input.xlsx

9.4.9 TIVA GPIO

9.4.9.1 Test ID / Test Name: TIV.11.1 / Control outputs functional validation

9.4.9.1.1 Purpose

The purpose of the test case is to execute the control outputs functional validation of TIVA-GPIO signals.

9.4.9.1.2 Test and Measurement Method

This test is conducted by toggling the GPIO lines which are output from TIVA by software control using CCS. Please refer to Section **6.2.9** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.9.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.4.9.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0018

Software versions – TIVA RTOS code

9.4.9.1.5 Test Results

Some TIVA- GPIO signals are toggling and some are not toggling.

NOTE: Resolution for failure – This is due to the design issue and this will be updated in the next version.

9.4.9.1.6 Measurement Logs

The list of result of Control outputs functional validation of TIVA- GPIO is attached herewith.

TIVA GPIO_Output.xlsx

9.4.10 ETH SW MGMT Interface

9.4.10.1 Test ID / Test Name: TIV.12.1 / Functional validation

9.4.10.1.1 Purpose

The purpose of the test case is to validate the TIVA in order to control and configure the Marvell switch.

9.4.10.1.2 Test and Measurement Method

This test is conducted by accessing two GPIOs (PC6- MDC, PC7-MDIO) of TIVA which are connected to Marvell switch(88E6071)'s MDC/MDIO and read back the device ID 0141H. Please refer to Section **6.2.10** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.4.10.1.3 Test Condition

Ambient Temperature – 25˚C
Operating Voltage – 18V
System load – Typical

9.4.10.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0001

Software versions – TIVA RTOS code

9.4.10.1.5 Test Results

TIVA is able to read device ID from Marvell device.

9.4.10.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
ETH SW MGMT Interface							
NA							

The snapshot of functional validation of Marvell switch is attached herewith.

9.5 Ethernet:

9.5.1 PoE (PD) - MDI

9.5.1.1 Test ID / Test Name: ETH.1.1/ Electrical Validation

9.5.1.1.1 Purpose

The purpose of this test case is to verify MDI (interface between Marvell Switch (88E6071) to POE (PD port)) signal characteristics.

9.5.1.1.2 Test and Measurement Method

This test is conducted by connecting a Linux PC to port A (PD port) of GBC board and starting communication between them by pinging each other. The MDI transmitting signals (from Port to Switch) are measured at J1A.1 (TXP) and J1A.2 (TXN) and MDI receiving signals (from Switch to Port) are measured at J1A.3 (RXP) and J1A.6 (RXN). Please refer to Section **7.2.1.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.5.1.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.5.1.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0007

Software versions – Linux 14.4.4

9.5.1.1.5 Test Results

The signal characteristics of MDI signals are as per the specification and the data rate is 100Mbps.

9.5.1.1.6 Measurement Logs

Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		

PoE(PD) - MDI							
LANSW_ETHSW_P1_TXP, LANSW_ETHSW_P1_TXN	J1A.1, J1A.2	Vp-p (V)	2.45	1.9	2.63	-6.84	PASS
		Overshoot (%)	3.05	0	10	-69.50	PASS
		Undershoot (%)	3.025	0	10	-69.75	PASS
		Data rate (Mbps)	100	NA	100	0.00	PASS
ETHSW_LANSW_P1_RXP, ETHSW_LANSW_P1_RXN	J1A.3, J1A.6	Vp-p (V)	2.1	1.9	2.63	-10.53	PASS
		Overshoot (%)	1.247	0	10	-87.53	PASS
		Undershoot (%)	1.217	0	10	-87.83	PASS
		Data rate (Mbps)	100	NA	100	0.00	PASS

The detailed analysis report with waveform captured for signal characteristics of PoE (PD) MDI test case is embedded in the xls document attached herewith.

POE(PD)_MDI.xlsx

9.5.1.2 Test ID / Test Name: ETH.1.2/ Functional validation

9.5.1.2.1 Purpose

The purpose of the test case is to validate the function of PoE (PD) - MDI.

9.5.1.2.2 Test and Measurement Method

This test is conducted by connecting a Linux PC to port A of GBC board and starting communication between them by giving command “ping IPaddress (IP address of Linux PC)” in the terminal of GBC system and “ping IPaddress (IP address of GBC system)” in Linux PC. Please refer to Section **7.2.1.3** in latest version of “OC_CONNECT_1_GBC_Test_Specification” document for detailed test procedure.

9.5.1.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.5.1.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0007

Software versions – Linux 14.4.4

9.5.1.2.5 Test Results

Communication is established between Port and Marvell switch through MDI interface over 100Mbps data rate.

The snapshot of functional validation of Springville MDI is attached herewith.


PoE(PD) - MDI_GBC_FV.png


PoE(PD) - MDI_LinuxPC_FV.pn


POE(PD)_MDI_datarate.PNG

9.5.2 TIVA Ethernet

9.5.2.1 Test ID / Test Name: ETH.3.1/ Electrical Validation

9.5.2.1.1 Purpose

The purpose of this test case is to verify the electrical parameters between Marvell Switch (88E6071) to TIVA.

9.5.2.1.2 Test and Measurement Method

This test is conducted by connecting a debug board to GBC. Ethernet cable from PC to port A (PD port) of GBC board. Flash the relevant code to TIVA so that signals between Port 0 of marvell switch and TIVA are initiated. The transmitting signals (from Port to Switch) are measured at T10.16 (TXP) and T10.14 (TXN) and receiving signals (from TIVA to Switch) are measured at T10.11 and (RXP) and T10.9 (RXN). Please refer to Section **7.2.2.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.5.2.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.5.2.1.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0007

9.5.2.1.5 Test Results

The electrical characteristics of Port0 Ethernet signals are as per the specification.

9.5.2.1.6 Measurement Logs

TIVA - Ethernet							
Test	Measuring Point	Measuring Criteria	Observation	Specification		Design Margin (%)	Test result
				Min	Max		
ETHSW_TIVA_P0_TXP, ETHSW_TIVA_P0_TXN	T10.16, T10.14	Vp-p (V)	2.24	1.9	2.63	-14.83	PASS
		Overshoot (%)	1.69	0	10	-83.10	PASS
		Undershoot (%)	1.61	0	10	-83.90	PASS
ETHSW_TIVA_P0_RXP, ETHSW_TIVA_P0_RXN	T10.11, T10.9	Vp-p (V)	2.2	1.9	2.63	-15.79	PASS
		Overshoot (%)	1.03	0	10	-89.70	PASS
		Undershoot (%)	0.099	0	10	-99.01	PASS

The detailed analysis report with waveform captured for electrical characteristics for TIVA – Port0 of marvel switch MDI test case is embedded in the xls document attached herewith.

TIVA-Ethernet.xlsx

9.5.2.2 Test ID / Test Name: ETH.3.2/ Functional validation

9.5.2.2.1 Purpose

The purpose of the test case is to validate the function of TIVA – Marvell Switch (Port 0)

9.5.2.2.2 Test and Measurement Method

This test is conducted by connecting a debug board to GBC. Ethernet cable from PC to port A (PD port) of GBC board. Flash the relevant code to TIVA so that signals between Port 0 of marvell switch and TIVA are initiated. Once IP address is assigned to TIVA, initiate the communication by pinging from PC using the TCPSendRecieve executable. Please refer to Section **7.2.2.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.5.2.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.5.2.2.4 DUT Sample Information

GBC Board Serial Number – WZ1630LIFE2GBC0007

9.5.2.2.5 Test Results

Communication is established between TIVA and Port 0 of Marvell switch at 100Mbps data rate.

The snapshot of functional validation of TIVA –Ethernet interface is attached herewith.

TIVA_Ethernet_Functional_Validation.PN

9.6 Clocks

9.6.1 Clock Sources

9.6.1.1 Test ID / Test Name: CLK.1.1 / Frequency Accuracy

9.6.1.1.1 Purpose

The purpose of this test case is to validate the frequency accuracy of crystal sources for 25MHz and 32.768 kHz.

9.6.1.1.2 Test and Measurement Method

1) This test is conducted for the following 25MHz crystals:
   i) Y3B2 at C3B22.1.
   ii) Y2M3 at C2M26.2.
   iii) Y2M1 at C2M2.2.
   iv) X1 at C475.1.
   v) X5 at C521.1
2) This test is also conducted for the following 32.768kHz crystal:
   i) Y2M2 at C2N1.2

The values are captured by a frequency counter. For frequency accuracy and stability measured value (Hz) is converted to ppb by following the below procedure:

i) The difference between the ideal clock frequency and maximum frequency value is calculated (df).

ii) Ppb is calculated by the equation: $ppb = \frac{df(Hz)*10^6*1000}{f(Hz)}$

Please refer to Section **8.2.1.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.6.1.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.6.1.1.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0005

Software versions – NA

9.6.1.1.5 Test Results

The frequency read at frequency counter is within the prescribed limit for Y3B2 and Y2M2 crystal.

9.6.1.1.6 Measurement Logs

Y3B2 Clock - Frequency Accuracy									
Sl. No	Test Case ID	Ideal Clock Frequency (MHz)	Measured Frequency(MHz)	Deviation(MHz)	Frequency tolerance (ppb)	Specification		Margin (%)	PASS / FAIL
						Min(ppb)	Max(ppb)		
1	CLK1.1	25	24.9981645	0.002	73420	-100000	100000	-26.58	PASS
2	CLK1.1		24.99816027						
3	CLK1.1		24.99815864						
4	CLK1.1		24.99815792						

Y2B3 Clock - Frequency Accuracy									
Sl. No	Test Case ID	Ideal Clock Frequency(MHz)	Measured Frequency (MHz)	Deviation(M Hz)	Frequen cy toleranc e (ppb)	Margin		Margi n (%)	PASS / FAIL
						Min(p pb)	Max(p pb)		
1	CLK1.1	25	24.99851	0.001487	59485.2	-30000	30000	98.284	FAIL
2	CLK1.1		24.99851						
3	CLK1.1		24.99851						
4	CLK1.1		24.99851						
5	CLK1.1		24.99851						
6	CLK1.1		24.99851						

Y2M1 Clock - Frequency Accuracy									
Sl.No	Test Case ID	Ideal Clock Frequency(MHz)	Measured Frequency(M Hz)	Deviation(M Hz)	Frequen cy toleranc e (ppb)	Specification		Margi n (%)	PASS / FAIL
						Min (ppb)	Max (ppb)		
1	CLK1.1	25	24.99847	0.001529	61165.2	-30000	30000	103.88 4	FAIL
2	CLK1.1		24.99847						
3	CLK1.1		24.99847						
4	CLK1.1		24.99847						
5	CLK1.1		24.99847						

Y2M2 Clock - Frequency Accuracy									
Sl. No	Test Case ID	Ideal Clock Frequ ency(kH z)	Measured Frequency(k Hz)	Deviation(kHz)	Frequenc y tolerance (ppb)	Specification		Margin (%)	PASS / FAIL
						Min(pp b)	Max(p pb)		
1	CLK1.1	32.768	32.76694167	0.0010583 3	32297.668 46	-50000	50000	- 35.4046 6	PASS
2	CLK1.1		32.76693846						
3	CLK1.1		32.76693775						

X1 Clock - Frequency Accuracy									
Sl.N o	Test Case ID	Ideal Clock Frequen cy (MHz)	Measured Frequncy (MHz)	Deviation (MHz)	Frequenc y tolerance (ppb)	Specification		Margin (%)	PASS / FAIL
						Min (ppb)	Max (ppb)		
1	CLK1.1	25	24.99805495	0.0019450 5	77802	40000	50000	55.604	FAIL
2	CLK1.1		24.99805339						

3	CLK1.1		24.99805276						
4	CLK1.1		24.99805273						
5	CLK1.1		24.99805229						

X5 Clock - Frequency Accuracy									
Sl. No	**Test Case ID**	**Ideal Clock Frequency(MHz)**	**Measured Frequncy(MHz)**	**Deviation(MHz)**	**Frequency tolerance (ppb)**	**Specification**		**Margin (%)**	**PASS / FAIL**
						Min (ppb)	**Max (ppb)**		
1	CLK1.1	25	24.99764676	0.00235324	94129.6	-50000	50000	88.2592	FAIL
2	CLK1.1		24.99764478						
3	CLK1.1		24.99764371						
4	CLK1.1		24.99764137						

NOTE: Resolution for failure – TBD. This test case will be re-measured in Life-3.

The detailed analysis report for Clock sources test case executed is attached herewith.

Clock Sources_CLK1.1.xlsx

9.6.1.2 Test ID / Test Name: CLK.1.2 / Timing Jitter

9.6.1.2.1 Purpose

The purpose of this test case is to validate the timing jitter of crystal clock sources.

9.6.1.2.2 Test and Measurement Method

3) This test is conducted for the following 25MHz crystals:

i) Y3B2 at C3B22.1.

ii) Y2M3 at C2M26.2.

iii) Y2M1 at C2M2.2.

iv) X1 at C475.1.

v) X5 at C521.1

The jitter values are captured by an oscilloscope.

Please refer to Section **8.2.1.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.6.1.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.6.1.2.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0002

Software versions – NA

9.6.1.2.5 Test Results

The timing jitter of Y3B2 crystal is within the specified limit.

9.6.1.2.6 Measurement Logs

Clock - Timing Jitter							
Sl.No	Test Case ID	Ideal Crystal Frequency	Cycle-to-cycle Jitter(ps)	Specification		Margin (%)	PASS / FAIL
				Min(ps)	Max(ps)		
1	CLK1.2	Y3B2 - 25MHz	145.24	0	300	-51.59	PASS
2	CLK1.2	X5 - 25MHz	59.014	0	50	18.03	FAIL
3	CLK1.2	X1 - 25MHz	533.82	0	300	77.94	FAIL

Clock - Timing Jitter							
Sl.No	Test Case ID	Ideal Crystal Frequency	RMS Jitter(ps)	Specification		Margin (%)	PASS / FAIL
				Min(ps)	Max(ps)		
1	CLK1.2	Y2M3 - 25MHz	9.8884	0	1.5	559.23	FAIL
2	CLK1.2	Y2M1 - 25MHz	8.16	0	1.5	444.00	FAIL
3	CLK1.2	X1 - 25MHz	11.589	0	1.5	672.60	FAIL

The detailed analysis report for clock sources jitter test case executed is attached herewith.


Clock_Timing Jitter.xlsx


Timing jitter.zip

NOTE: Resolution for failure – TBD. This test case will be re-measured in Life-3.

9.6.2 PCIe - GBE clock

9.6.2.1 Test ID / Test Name: CLK.2.1 / Frequency Accuracy

9.6.2.1.1 Purpose

The purpose of this test case is to validate the frequency accuracy of 100MHz PCIe reference clock: PCIE0_GBE_CLKP.

9.6.2.1.2 Test and Measurement Method

This test is conducted by probing 100MHz clock at R10647.1. The value is captured by a frequency counter for 6 iterations. For frequency accuracy and stability measured value (Hz) is converted to ppm by following the below procedure:

iii) The difference between the ideal clock frequency and maximum frequency value is calculated (df).

iv) Ppb is calculated by the equation: $ppb = \frac{df(Hz)*10^6*1000}{f(Hz)}$

Please refer to Section **8.2.2.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.6.2.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.6.2.1.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0021

Software versions – NA

9.6.2.1.5 Test Results

The frequency read at frequency counter is within the prescribed limit of 100MHz clock.

9.6.2.1.6 Measurement Log

Clock - PCIe -GBE Clock - Frequency Accuracy									
Sl. No	Test Case ID	Ideal Clock Frequency (MHz) - PCIE0_GBE_CLKP	Measured Frequency(MHz)	Deviation	Frequency tolerance (ppb)	Specification		Margin (%)	PASS / FAIL
						Min (ppb)	Max (ppb)		
1	CLK2.1	100	99.994329	0.005671	56710	-300000	300000	118.9033	PASS
2	CLK2.1		99.994326						
3	CLK2.1		99.994288						
4	CLK2.1		99.994235						
5	CLK2.1		99.994226						
6	CLK2.1		99.99422						

NOTE: The detailed analysis report with waveform captured is embedded in the xls document attached in the end of this section.

9.6.2.2 Test ID / Test Name: CLK.2.2 / Signal Integrity

9.6.2.2.1 Purpose

The purpose of the test case is to validate the electrical characteristics of 100 MHz PCIe clock.

9.6.2.2.2 Test and Measurement Method

This test is conducted by probing 100MHz clock at R10647.1. The value is captured on an oscilloscope and is within the prescribed limit by Intel microcontroller. Please refer to Section **8.2.2.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.6.2.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.6.2.2.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0021

Software versions – NA

9.6.2.2.5 Test Results

The electrical characteristics of 100 MHz PCIe Clock is within the designed spec.

9.6.2.2.6 Measurement Log

PCIe - GBE clock - signal Integrity									
Sl. No	Test Case ID	Measuring Rail	Measurement location	Measured Parameter	Measured Value (V)	Specification		Margin (%)	PASS/ FAIL
						Min(V)	Max(V)		
1	CLK2.2	PCIE0_GBE_CLKP	R10647.1	Positive Over-shoot	0.12	0	0.18	-33.33	PASS
2	CLK2.2	PCIE0_GBE_CLKN	R10648.1	Negative Over-shoot	0.12	0	0.18	-33.33	PASS

NOTE: The detailed analysis report with waveform captured is embedded in the xls document attached in the end of this section.

9.6.2.3 Test ID / Test Name: CLK.2.3 / Timing Jitter

9.6.2.3.1 Purpose

The purpose of the test case is to validate the Timing Jitter of 100 MHz PCIe Clock.

9.6.2.3.2 Test and Measurement Method

This test is conducted by terminating PCIE0_GBE_CLKP and with a 2.2pF capacitor at R10647.1 and R10648.1. Probe at R10647.1 and R10648.1. Run the test utility N5393D in the infiniium oscilloscope. To configure the test suite, select PCIe version as 2.0, Refclk tests, Device1, Lan0. In select tests option in utility, select common clock tests and run all the selected test cases. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin. Please refer to Section **8.2.2.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.6.2.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.6.2.3.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0021

Software versions – NA

9.6.2.3.5 Test Results

The timing jitter for 100Mhz clock is checked and validated.

9.6.2.3.6 Measurement Log

PCIe - GBE clock_Timing Jitter									
Sl. No	**Test Case ID**	**Measuring Rail**	**Measurement location**	**Measured Parameter**	**Measured Value (ps)**	**Specification**		**Margin (%)**	**PASS / FAIL**
						Min(V)	**Max(V)**		
1	CLK2.3	PCIE0_GBE_CLKP	R10647.1	RMS Jitter	12.95	NA	NA	NA	NA
				Peak-to-peak jitter	96.348	0	150	-35.77	PASS

The detailed analysis report with waveform captured for each of the 100MHz PCIe clock test case executed is embedded in the xls document attached herewith.

report.html

PCIE_100MHz_CLK.xlsx

9.6.3 40 MHz GPSDO Clock

9.6.3.1 Test ID / Test Name: CLK.3.1 / Frequency Accuracy

9.6.3.1.1 Purpose

The purpose of this test case is to validate the frequency accuracy of 40MHz reference clock for GPSDO. Please refer to Section **8.2.3.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.6.3.1.2 Test and Measurement Method

This test is conducted by probing 40MHz clock at R19.2. The value is captured by a frequency counter.

9.6.3.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.6.3.1.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0002

SYNC Board Serial Number- WZ1627LIFE1SYNC0011

Software versions – NA

9.6.3.1.5 Test Results

The frequency read at frequency counter is within the prescribed limit of 40MHz clock.

9.6.3.1.6 Measurement Log

Clock - GPSDO_40MHz_ Clock - Frequency Accuracy									
Sl. No	Test Case ID	Ideal Clock Frequency (MHz)	Measured Frequency (MHz)	Deviation (MHz)	Frequency tolerance (ppb)	Specification		Margin %	PASS / FAIL
						Min (ppb)	Max (ppb)		
1	CLK3.1	40	40.00008109	8.11E-05	2027.25	-50	50	100.00016	FAIL
2	CLK3.1		40.0000812						
3	CLK3.1		40.00008119						
4	CLK3.1		40.00008128						

NOTE: Resolution for failure – TBD. This test case will be re-measured in Life-3.

The detailed analysis report with waveform captured is embedded in the xls document attached in the end of this section.

9.6.3.2 Test ID / Test Name: CLK.3.2 / Signal Integrity

9.6.3.2.1 Purpose

The purpose of the test case is to validate the electrical characteristics of 40 MHz GPSDO Clock.

9.6.3.2.2 Test and Measurement Method

This test is conducted by probing the GPSDO Clock signal at R19.2 (Near Via). The measured values are well with-in the limit as specified in the LTE-Lite Module datasheet specification. Please refer to Section **8.2.3.3** of 'SYNC Board' Test specifications (Rev 0.1) for detailed test procedure.

9.6.3.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.6.3.2.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0002

SYNC Board Serial Number- WZ1627LIFE1SYNC0011

Software versions – NA

9.6.3.2.5 Test Results

The electrical characteristics of 40 MHz GPSDO Clock is within the designed spec. 40MHz clock is coming out from the GPSDO Module.

9.6.3.2.6 Measurement Log

Clock - GPSDO_40MHz_ Clock - Signal Integrity									
Sl. No	Test Case ID	Measuring Rail	Measurement location	Measured Parameter	Measured Value (V)	Specification		Margin (%)	PASS/ FAIL
						Min(V)	Max(V)		
1	CLK3.2	LTE_REF_OUT_40MHz	R19.2	VLOW	0.125	0	0.4	-68.75	PASS
				VHIGH	3.125	0.8	3.3	-5.30	PASS

NOTE: The detailed analysis report with waveform captured is embedded in the xls document attached in the end of this section.

9.6.3.3 Test ID / Test Name: CLK.3.3 / Timing Jitter

9.6.3.3.1 Purpose

The purpose of the test case is to validate the Timing Jitter of 40 MHz GPSDO Clock.

9.6.3.3.2 Test and Measurement Method

This test is conducted by probing the GPSDO Clock Signal Timing Jitter at R19.2 (Near Via). The measurement data will be compared with the measured data that will be made available by Jacksons Lab. Steps to measure RMS jitter through signal analyzer:

i) Connect Sync board to GBC board.

ii) Configure DC power supply to give a voltage of 18V.

iii) Set the central frequency to 40MHz in MXA signal Analyzer.

iv) Carrier frequency will be automatically detected.

v) Go to Mode option, Select Phase Noise.

vi) Go to Measure option and select Log Plot.

vii) In Span option set start and stop offset values to 8kHz and 22MHz respectively

viii) Select marker go to Integrated RMS Noise then select Jitter option.

ix) Go to Band adjust set the left band (10 KHz) and right band (22MHz).

x) Measure the Jitter on the analyzer in pico second.

xi) Select auto tune in frequency option at the end of each step.

Please refer to Section **8.2.3.4** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.6.3.3.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.6.3.3.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0002

SYNC Board Serial Number- WZ1627LIFE1SYNC0011

Software versions – NA

9.6.3.3.5 Test Results

The timing Jitter of 40 MHz GPSDO Clock is measured.

9.6.3.3.6 Measurement Log

Clock - GPSDO_40MHz_ Clock - Timing Jitter								
Sl. No	**Test Case ID**	**Measuring Rail**	**Measurement location**	**Measured Parameter**	**Measured Value (ps)**	**Margin**		**PASS/ FAIL**
						Min(V)	**Max(V)**	
				RMS Jitter	47.75	NA	NA	NA
1	CLK3.3	LTE_REF_OUT_40MHz	R10647.1	Peak-to-peak jitter	355.26	NA	NA	NA

The detailed analysis report with waveform captured for each of the SYNC Board Clock test case executed is embedded in the xls document attached herewith.

NOTE:

For 40MHz clock jitter requirement, ADI indicates that the only requirement is of phase noise of Reference input. There is no requirement for jitter as there is internal PLL in ADI that cleans the clock. Therefore, measurement was done to capture the baseline performance, and was not against any specification.

9.6.4 HDMI clock

9.6.4.1 Test ID / Test Name: CLK.4.1 / Frequency Accuracy

9.6.4.1.1 Purpose

The purpose of this test case is to validate the frequency accuracy of HDMI clock.

9.6.4.1.2 Test and Measurement Method

Connect debug board to GBC. Probe HDMI_CLK_DP and HDMI_CLK_DN at C4N2.2 and C4N1.2 respectively. Measure the frequency value using oscilloscope. Please refer to Section **8.2.4.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.6.4.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.6.4.1.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0002

Software versions – NA

9.6.4.1.5 Test Results

The frequency read at frequency counter is within the prescribed limit of 100MHz HDMI clock.

9.6.4.1.6 Measurement Log

Clock - 100MHz_ Clock - Frequency Accuracy								
						Specification		

Sl. No	Test Case ID	Ideal Clock Frequency (MHz)	Measured Frequency (MHz)	Deviation (Hz)	Frequency tolerance (ppb)	Min(ppb)	Max(ppb)	Margin (%)	PASS / FAIL
1	CLK4.1	100	107.9	7.9	79	-1000000	1000000	100.01	PASS

NOTE: The detailed analysis report with waveform captured is embedded in the xls document attached in the end of this section.

9.6.4.2 Test ID / Test Name: CLK .4.2 / Signal Integrity

9.6.4.2.1 Purpose

The purpose of the test case is to validate the electrical characteristics of 100 MHz HDMI Clock.

9.6.4.2.2 Test and Measurement Method

Connect debug board to GBC. Probe HDMI_CLK_DP and HDMI_CLK_DN at C4N2.2 and C4N1.2 respectively. Measure the overshoot and undershoot parameters for HDMI clock using oscilloscope. Please refer to Section **8.2.4.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.6.4.2.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.6.4.2.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0002

Software versions – NA

9.6.4.2.5 Test Results

The electrical characteristics of 100 MHz HDMI Clock is within the designed spec.

9.6.4.2.6 Measurement Log

Clock - 100MHz_ Clock - Frequency Accuracy								
						Specification		

Sl. No	Test Case ID	Measuring Rail	Measurement location	Measured Parameter	Measured Value (V)	Min(V)	Max(V)	Margin (%)	PASS/ FAIL
1	CLK4.2	HDMI_CLK_DP and HDMI_CLK_DN	C4N2.2 and C4N1.2	Positive Over-shoot	0.16	0	0.78	-79.49	PASS
				Negative Over-shoot	0.2	0	0.2	0.00	PASS

The detailed analysis report with waveform captured for each of the 100MHz PCIe clock test case executed is embedded in the xls document attached herewith.

HDMI_100MHz.xlsx

9.6.5 GPS 1pps clock

9.6.5.1 Test ID / Test Name: CLK.5.1 / Frequency Accuracy

9.6.5.1.1 Purpose

The purpose of this test case is to validate the 1pps clock.

9.6.5.1.2 Test and Measurement Method

Connect Sync board to GBC board. Probe R48.1 on sync board in order to check 1pps clock. Measure the frequency using frequency counter. Please refer to Section **8.2.5.2** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.6.5.1.3 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.6.5.1.4 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0005

SYNC Board Serial Number- WZ1627LIFE1SYNC0011

Software versions – NA

9.6.5.1.5 Test Results

The frequency read at frequency counter is 1Hz and is within the prescribed limit.

9.6.5.1.6 Measurement Logs

Clock - SYNC_1pps_ Clock - Frequency Accuracy								
Sl. No	Test Case ID	Ideal Clock Frequency(Hz)	Measured Frequency(Hz)	Deviation(Hz)	Frequency tolerance (ppb)	Margin		PASS / FAIL
						Min(ppb)	Max(ppb)	
1	CLK.5.1	1	1.000002022	2.0215E-06	2021.5	NA	NA	NA
2	CLK.5.1		1.000002018					
3	CLK.5.1		1.000002198					
4	CLK.5.1		1.000002037					
5	CLK.5.1		1.000002021					

NOTE: The detailed analysis report with waveform captured is embedded in the xls document attached in the end of this section.

9.5.2.1 Test ID / Test Name: CLK.5.2 / Signal Integrity

9.6.5.1.7 Purpose

The purpose of the test case is to validate the electrical characteristics of 1pps clock.

9.6.5.1.8 Test and Measurement Method

Connect Sync board to GBC board. This test is conducted by probing 1pps clock at R48.1 on the sync board. The value is captured on an oscilloscope. Please refer to Section **8.2.5.3** in latest version of "OC_CONNECT_1_GBC_Test_Specification" document for detailed test procedure.

9.6.5.1.9 Test Condition

Ambient Temperature – 25˚C

Operating Voltage – 18V

System load – Typical

9.6.5.1.10 DUT Sample Information

GBC Board Serial Number- WZ1630LIFE2GBC0005

SYNC Board Serial Number- WZ1627LIFE1SYNC0011

Software versions – NA

9.6.5.1.11 Test Results

9.6.5.1.12 Measurement Log

Sync Board - 1Hz Signal Integrity								
Sl. No	**Test Case ID**	**Measuring Rail**	**Measurement location**	**Measured Parameter**	**Measured Value**	**Margin**		**PASS/ FAIL**
						Min(V)	**Max(V)**	
1	CLK.5.2	R_LTE_1_PPS_OUT	R48.1	Frequency	1 Hz	NA	NA	NA
2				Voltage Peak to Peak	3.690 V	NA	NA	NA
3				Overshoot	160 mV	NA	NA	NA
4				Undershoot	140 mV	NA	NA	NA

The detailed analysis report with waveform captured for each of the 1Hz clock test case executed is embedded in the xls document attached herewith.

1PPS clock.xlsx

10. Revision History

SL.no	Date	Version	Author	Comments
1	February 9th, 2017	1.0	OpenCellular Team	First Release