1. Description

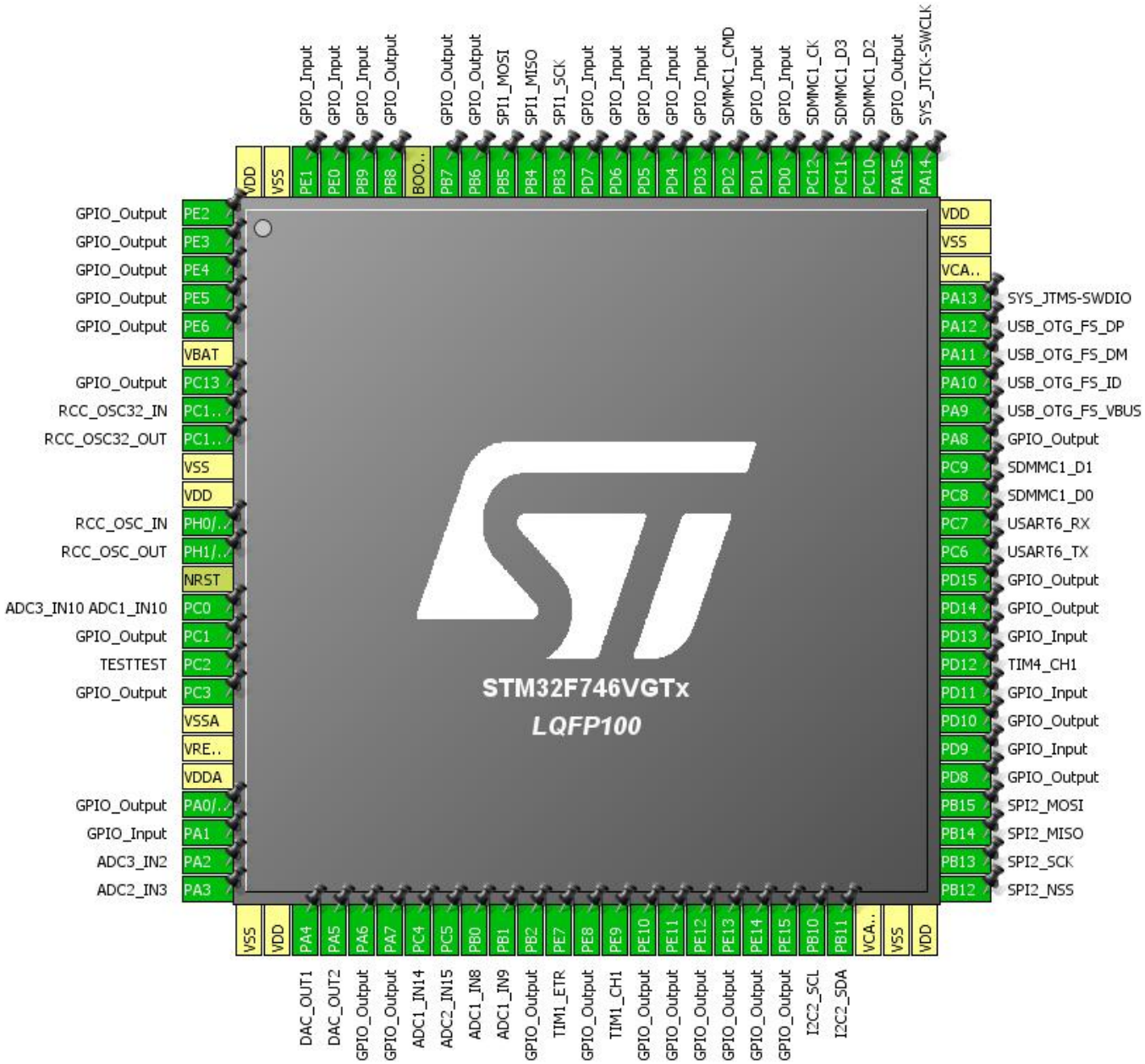
1.1. Project

Project Name	PSDR
Board Name	custom
Generated with:	STM32CubeMX 4.27.0
Date	10/29/2018

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746VGTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



3. Pins Configuration

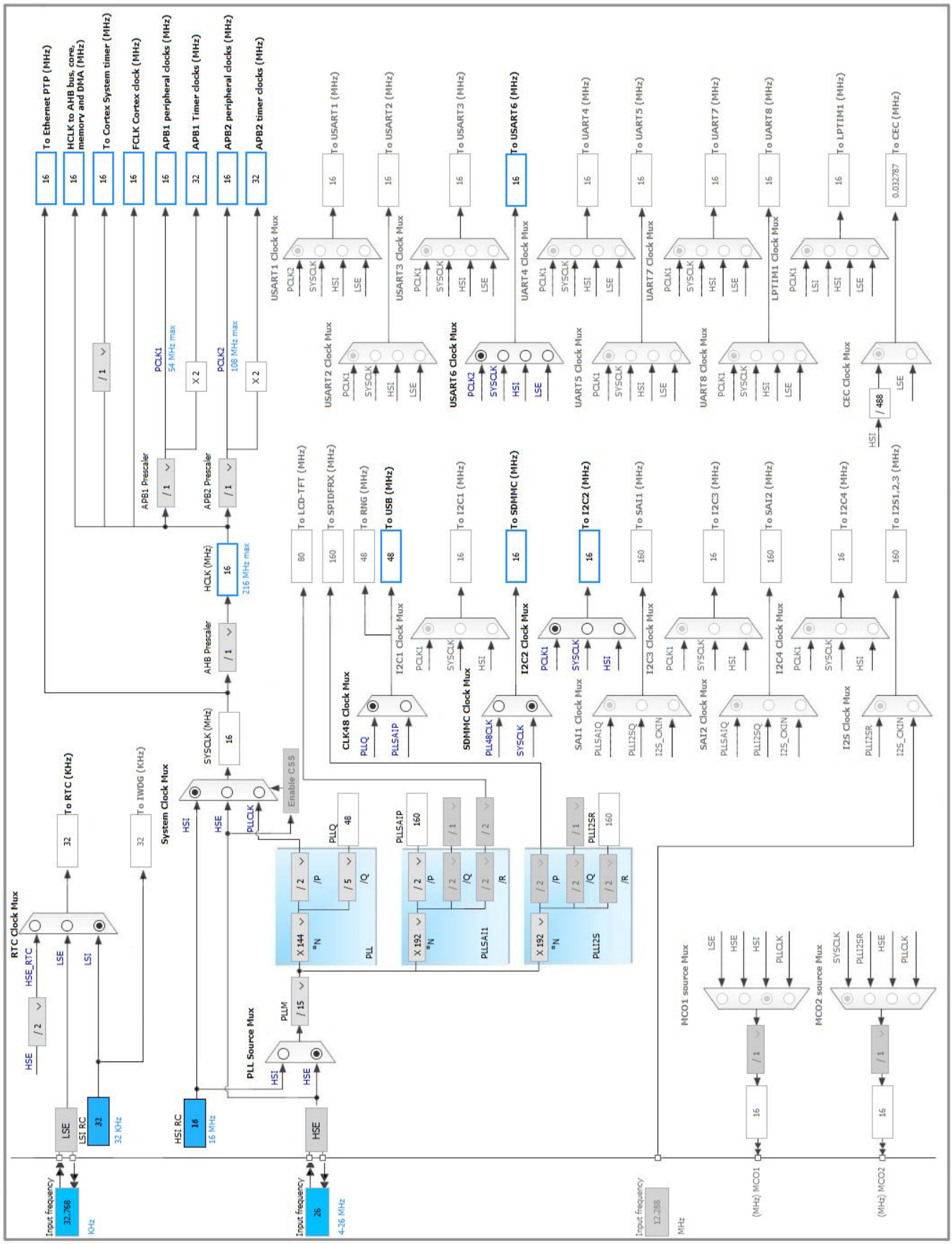
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	
2	PE3 *	I/O	GPIO_Output	
3	PE4 *	I/O	GPIO_Output	
4	PE5 *	I/O	GPIO_Output	
5	PE6 *	I/O	GPIO_Output	
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Output	
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0/OSC_IN	I/O	RCC_OSC_IN	
13	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	ADC3_IN10, ADC1_IN10	
16	PC1 *	I/O	GPIO_Output	
17	PC2 *	I/O	GPIO_Output	TESTTEST
18	PC3 *	I/O	GPIO_Output	
19	VSSA	Power		
20	VREF+	Power		
21	VDDA	Power		
22	PA0/WKUP *	I/O	GPIO_Output	
23	PA1 *	I/O	GPIO_Input	
24	PA2	I/O	ADC3_IN2	
25	PA3	I/O	ADC2_IN3	
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	DAC_OUT1	
29	PA5	I/O	DAC_OUT2	
30	PA6 *	I/O	GPIO_Output	
31	PA7 *	I/O	GPIO_Output	
32	PC4	I/O	ADC1_IN14	
33	PC5	I/O	ADC2_IN15	
34	PB0	I/O	ADC1_IN8	
35	PB1	I/O	ADC1_IN9	
36	PB2 *	I/O	GPIO_Output	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
37	PE7	I/O	TIM1_ETR	
38	PE8 *	I/O	GPIO_Output	
39	PE9	I/O	TIM1_CH1	
40	PE10 *	I/O	GPIO_Output	
41	PE11 *	I/O	GPIO_Output	
42	PE12 *	I/O	GPIO_Output	
43	PE13 *	I/O	GPIO_Output	
44	PE14 *	I/O	GPIO_Output	
45	PE15 *	I/O	GPIO_Output	
46	PB10	I/O	I2C2_SCL	
47	PB11	I/O	I2C2_SDA	
48	VCAP_1	Power		
49	VSS	Power		
50	VDD	Power		
51	PB12	I/O	SPI2_NSS	
52	PB13	I/O	SPI2_SCK	
53	PB14	I/O	SPI2_MISO	
54	PB15	I/O	SPI2_MOSI	
55	PD8 *	I/O	GPIO_Output	
56	PD9 *	I/O	GPIO_Input	
57	PD10 *	I/O	GPIO_Output	
58	PD11 *	I/O	GPIO_Input	
59	PD12	I/O	TIM4_CH1	
60	PD13 *	I/O	GPIO_Input	
61	PD14 *	I/O	GPIO_Output	
62	PD15 *	I/O	GPIO_Output	
63	PC6	I/O	USART6_TX	
64	PC7	I/O	USART6_RX	
65	PC8	I/O	SDMMC1_D0	
66	PC9	I/O	SDMMC1_D1	
67	PA8 *	I/O	GPIO_Output	
68	PA9	I/O	USB_OTG_FS_VBUS	
69	PA10	I/O	USB_OTG_FS_ID	
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15 *	I/O	GPIO_Output	
78	PC10	I/O	SDMMC1_D2	
79	PC11	I/O	SDMMC1_D3	
80	PC12	I/O	SDMMC1_CK	
81	PD0 *	I/O	GPIO_Input	
82	PD1 *	I/O	GPIO_Input	
83	PD2	I/O	SDMMC1_CMD	
84	PD3 *	I/O	GPIO_Input	
85	PD4 *	I/O	GPIO_Input	
86	PD5 *	I/O	GPIO_Input	
87	PD6 *	I/O	GPIO_Input	
88	PD7 *	I/O	GPIO_Input	
89	PB3	I/O	SPI1_SCK	
90	PB4	I/O	SPI1_MISO	
91	PB5	I/O	SPI1_MOSI	
92	PB6 *	I/O	GPIO_Output	
93	PB7 *	I/O	GPIO_Output	
94	BOOT0	Boot		
95	PB8 *	I/O	GPIO_Output	
96	PB9 *	I/O	GPIO_Input	
97	PE0 *	I/O	GPIO_Input	
98	PE1 *	I/O	GPIO_Input	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN8

mode: IN9

mode: IN10

mode: IN14

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 10 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN3

mode: IN15

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 15 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. ADC3

mode: IN2

mode: IN10

5.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 10 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.4. DAC

mode: OUT1 Configuration

mode: OUT2 Configuration

5.4.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None

5.5. I2C2

I2C: I2C

5.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.7. RTC

mode: Activate Clock Source

5.7.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

5.8. SDMMC1

Mode: MMC 4 bits Wide bus

5.8.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock divider bypass	Disable
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMCCLK clock divide factor	0

5.9. SPI1

Mode: Full-Duplex Master

5.9.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**54.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.10. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

5.10.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**27.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware

5.11. SYS

Debug: Serial Wire

Timebase Source: TIM2

5.12. TIM1

Slave Mode: External Clock Mode 1

Trigger Source: ETR1

Channel1: Input Capture direct mode

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable
Slave Mode Controller	ETR mode 1

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Trigger:

Trigger Polarity	non inverted
Trigger Prescaler	Prescaler not used
Trigger Filter (4 bits value)	0

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct

Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.13. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

5.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.14. USART6

Mode: Asynchronous

5.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.15. USB_OTG_FS

Mode: OTG/Dual_Role_Device

mode: Activate_VBUS

5.16. FREERTOS

mode: Enabled

5.16.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.16.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled

xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA3	ADC2_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC2_IN15	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PC0	ADC3_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC3_IN2	Analog mode	No pull-up and no pull-down	n/a	
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI2	PB12	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE7	TIM1_ETR	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
USB_OTG_FS	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	
	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TESTTEST
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA0/WKUP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_TX	DMA2_Stream3	Memory To Peripheral	**High ***
ADC1	DMA2_Stream0	Peripheral To Memory	**Very High ***

SPI1_TX: DMA2_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM2 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	5	0
DMA2 stream3 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM4 global interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
SDMMC1 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
USART6 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746VGTx
Datasheet	027590_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	PSDR
Project Folder	C:\Users\micha\workspace\PSDR\TestingMakeFile\PSDR
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F7 V1.12.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report