# Security of BIOS/UEFI System Firmware from Attacker and Defender Perspectives

Section 4. Common Attack Vectors against System Firmware

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# Section 4. Common Attack Vectors Against BIOS and UEFI Firmware

### So What is System Firmware?

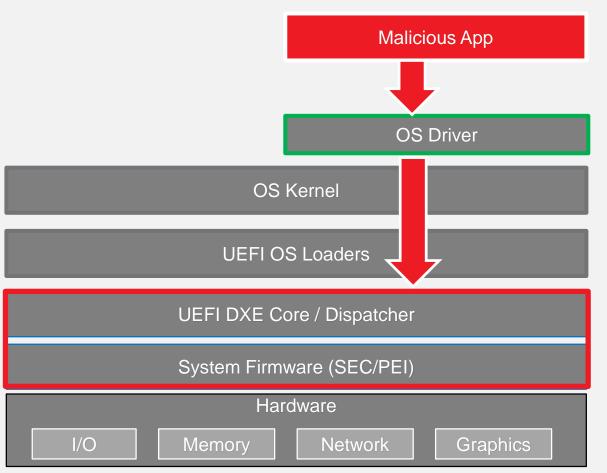
**Operating System** Runtime **System** App App **Firmware** (UEFI RT, Kernel + Drivers SMM) **System Firmware** (BIOS, UEFI firmware, Coreboot...) **Hardware** Graphics Memory CPU I/O Network

Privilege

#### **How Can System Firmware Be Attacked?**

- 1. Inadequate hardware write protections of firmware "ROM"
- 2. Firmware update implementation
- 3. Persistent Configuration (UEFI Variables, CMOS settings)
- 4. Inadequate hardware protections of runtime firmware (System Management Interrupt Handlers)
- 5. Runtime firmware (SMI handlers)
- 6. Resume from sleep states
- 7. Network stack implementation in firmware
- 8. Other interfaces with OS/software, network, devices...

#### Do BIOS Attacks Require Kernel Privileges?



A matter of finding legitimate signed kernel driver which can be used on behalf of user-mode exploit as a *confused deputy*.

**RWEverything** driver signed for Windows 64bit versions (co-discovered with researchers from MITRE)

### 4.1 Attacking UEFI Secure Boot

# 4.1 (1) Attacking Secure Boot via Corruption of Firmware Root Signing Certificate (Platform Key)

#### **HW protection of FW in ROM**

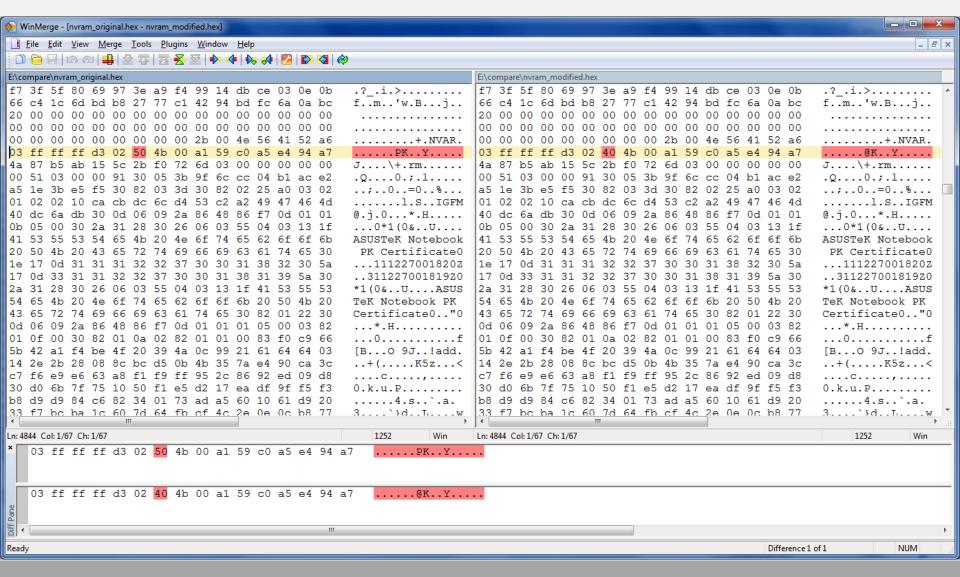
[\*] Module path: C:\chipsec\1.1.4\source\tool\chipsec\modules\common\bios\_wp.py
[x][ ------

[\*] running module: chipsec.modules.common.bios wp

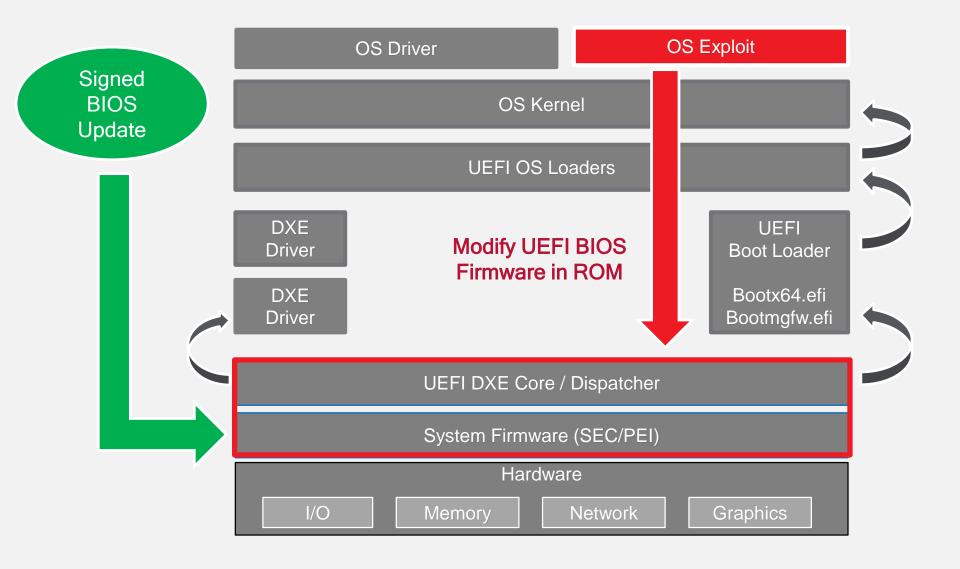
# chipsec main.py --module common.bios wp

```
[x] [ Module: BIOS Region Write Protection
[*] BIOS Control = 0x08
   [05] SMM BWP = 0 (SMM BIOS Write Protection)
   [04] TSS = 0 (Top Swap Status)
  [01] BLE = 0 (BIOS Lock Enable)
   [00] BIOSWE = 0 (BIOS Write Enable)
[-] BIOS region write protection is disabled!
[*] BIOS Region: Base = 0x00200000, Limit = 0x007FFFFF
SPI Protected Ranges
PRx (offset) | Value | Base | Limit | WP? | RP?
PRO (74) | 00000000 | 00000000 | 00000000 | 0 | 0
PR1 (78) | 00000000 | 00000000 | 00000000 | 0 | 0
PR2 (7C) | 00000000 | 00000000 | 00000000 | 0 | 0
PR3 (80) | 00000000 | 00000000 | 0 | 0
PR4 (84) | 00000000 | 00000000 | 00000000 | 0 | 0
[!] None of the SPI protected ranges write-protect BIOS region
[!] BIOS should enable all available SMM based write protection mechanisms or configure SPI protected ranges to protect the entire BIOS region
[-] FAILED: BIOS is NOT protected completely
```

# Platform Key certificate is stored in the NVRAM potion of SPI flash memory



#### Modify PK in SPI if Writes are Allowed



#### **Modifying Platform Key in NVRAM**

#### Corrupt Platform Key EFI variable in NVRAM

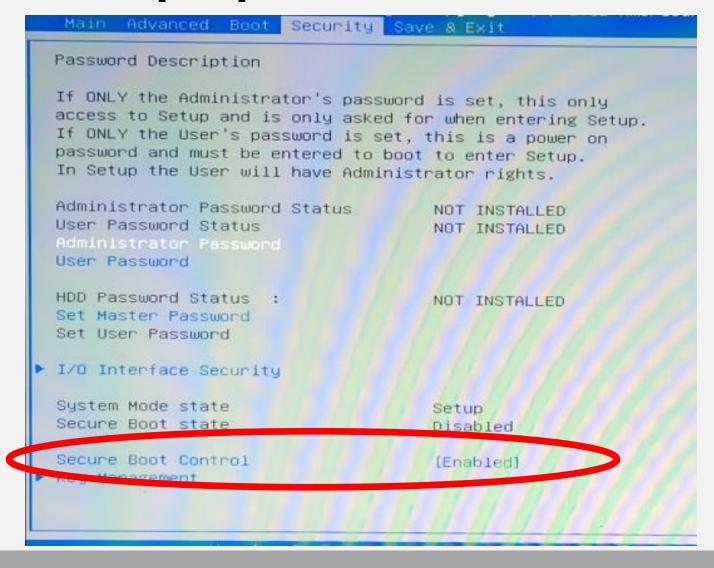
- Name ("PK") or Vendor GUID {8BE4DF61-93CA-11D2-AA0D-00E098032B8C}
- AuthenticatedVariableService DXE driver enters Secure Boot SETUP\_MODE when correct "PK" EFI variable cannot be located in EFI NVRAM
- Main volatile SecureBoot variable is then set to DISABLE
- DXE ImageVerificationLib then assumes Secure Boot is off and skips Secure Boot checks
- Generic exploit, independent of the platform/vendor
- 1 bit modification!

×

- [+] loaded exploits.secureboot.pk
- [+] imported chipsec.modules.exploits.secureboot.pk
- [\*] BIOS Region: Base = 0x00200000, Limit = 0x007FFFFF
- [\*] Reading EFI NVRAM (0x40000 bytes of BIOS region) from ROM..
- [\*] Done reading EFI NVRAM from ROM
- [\*] Searching for Platform Key (PK) EFI variables..
- [\*] Found PK EFI variable in NVRAM at offset 0x12E9B
- [+] Found 1 PK EFI variables in NVRAM
- [\*] Checking protection of UEFI BIOS region in ROM..
- [spi] UEFI BIOS write protection enabled but not locked. Disabling..
- [!] UEFI BIOS write protection is disabled
- [\*] Modifying Secure Boot persistent configuration..
- [\*]  $0 \text{ PK FLA} = 0 \times 212 \text{ EA6}$  (offset in NVRAM buffer =  $0 \times 12 \text{ EA6}$ )
- [\*] Modifying PK EFI variable in ROM at FLA = 0x212EA6..
- [+] Modified all Platform Keys (PK) in UEFI BIOS ROM
- [!] \*\*\* Secure Boot has been disabled \*\*\*
- \* Installing UEFI Bootkit..
- [!] \*\*\* UEFI Bootkit has been installed \*\*\*
- [\*] Press any key to reboot..

4.1 (2) Attacking Secure Boot via Setup UEFI Variable (On/Off, Verification Policies, CSM Enabled, "Clear Keys" control)

# Secure Boot Can Be Turned On/Off in BIOS Setup Options



#### Looking for Enable Policy in SPI Dump...



chipsec\_util.py spi dump spi.bin

#### Extracting Runtime UEFI Variables...

#### Secure Boot On

#### Secure Boot Off

```
Name
                                                                                               NetworkStackVar B2CB8C2B-D719-3D
                              MemCeil. D26F6F65-4599-1A11-B8}
db 99D26F6F-1145-B81A-49B9-1F}MonotonicCounter D26F6F65-4599}
                                                               db 99D26F6F-1145-B81A-49B9-1F85}NvRamSpdMap 963D3AD7-A345-DABC-D
dbx 99D26F6F-1145-B81A-49B9-1}MrcS3Resume BCA34596-D0DA-670E
                                                               dbx 99D26F6F-1145-B81A-49B9-1F8}PchInit 0ED0DABC-6567-6F6F-D299-
KEK D26F6F65-4599-1A11-B849-B}NetworkStackVar B2CB8C2B-D719-}
                                                               KEK D26F6F65-4599-1A11-B849-B91}PK D26F6F65-4599-1A11-B849-B91F8
PK D26F6F65-4599-1A11-B849-B9}NvRamSpdMap 963D3AD7-A345-DABC}
                                                              PK D26F6F65-4599-1A11-B849-B91F}PlatformLang D26F6F65-4599-1A11-
                                                              AcpiGlobalVariable 8C2B0398-B2C}PlatformLastLang D0DABCA3-670E-6
AcpiGlobalVariable 8C2B0398-B}PchInit 0ED0DABC-6567-6F6F-D29
AEDID 3D3AD719-4596-BCA3-DAD0}PK D26F6F65-4599-1A11-B849-B91
                                                               AEDID 3D3AD719-4596-BCA3-DAD0-0}PlatformLastLangCodes D0DABCA3-6
Boot0000 D26F6F65-4599-1A11-B}PlatformLang D26F6F65-4599-1A1
                                                               Boot0000 D26F6F65-4599-1A11-B84\rd 0398E000-8C2B-B2CB-19D7-3A3D9
BootOrder D26F6F65-4599-1A11-}PlatformLastLang D0DABCA3-670E
                                                               BootOrder D26F6F65-4599-1A11-B8}SaPegData 45963D3A-BCA3-D0DA-0E6
ConIn D26F6F65-4599-1A11-B849}PlatformLastLangCodes D0DABCA3}
                                                               ConIn D26F6F65-4599-1A11-B849-B}Save1MBuffer 2B0398E0-CB8C-19B2-
                                                               ConOut_D26F6F65-4599-1A11-B840 }ScramblerBaseSeed_BCA34596-มขบล
ConOut D26F6F65-4599-1A11-B84}rd 0398E000-8C2B-B2CB-19D7-3A3}
                                                              ConOutChild1 D26F6F65-459-1A11}Setup D0DABCA3-670E-6F65-6FD2-99
ConOutChild1 D26F6F65-4599-1A}RevocationList 98E0000D-2B03-C
                                                               ConOutChildNumber D26F6F65 4599}SetupDptfFeatures D0DABCA3-670E-
ConOutChildNumber D26F6F65-45}SaPegData 45963D3A-BCA3-D0DA-0
copy 0398E000-8C2B-B2CB-19D7-}Save1MBuffer 2B0398E0-CB8C-19B}
                                                               copy 0398E000-8C2B-B2CB-19D7-3A}SetupSnprpmreatures popabCA3-670
cr 0398E000-8C2B-B2CB-19D7-3A}ScramblerBaseSeed BCA34596-D0D
                                                              cr 0398E000-8C2B-B2CB-19D7-3A3D}StdDefaults 4599D26F-1A11-49B8-B
CurrentPolicy 98E0000D-2B03-C}Setup D0DABCA3-670E-6F65-6FD2-
                                                               db 99D26F6F-1145-B81A-49B9-1F85}TcgInternalSyncFlag DABCA345-0ED
db 99D26F6F-1145-B81A-49B9-1F}SetupDptfFeatures D0DABCA3-670
                                                               dbx 99D26F6F-1145-B81A-49B9-1F8}TdtAdvancedSetupDataVar 3AD719B2
dbx 99D26F6F-1145-B81A-49B9-1}SetupSnbPpmFeatures D0DABCA3-6
                                                               DefaultBootOrder D719B2CB-3D3A-}Timeout D26F6F65-4599-1A11-B849-
DefaultBootOrder D719B2CB-3D3}StdDefaults 4599D26F-1A11-49B8
                                                               DefaultConOutChild D26F6F65-459}UsbSupport D0DABCA3-670E-6F65-6F
DefaultConOutChild D26F6F65-4}TcgInternalSyncFlag DABCA345-0}
                                                               del 0398E000-8C2B-B2CB-19D7-3A3}WdtPersistentData 670ED0DA-6F65-
del 0398E000-8C2B-B2CB-19D7-3}TdtAdvancedSetupDataVar 3AD719
                                                               dir 0398E000-8C2B-B2CB-19D7-3A3}
dir 0398E000-8C2B-B2CB-19D7-3}Timeout D26F6F65-4599-1A11-B84}
                                                              FastEfiBootOption CB8C2B03-19B2}
FastEfiBootOption CB8C2B03-19}UsbSupport D0DABCA3-670E-6F65-
                                                               FPDT Variable D26F6F65-4599-1A1}
FPDT Variable D26F6F65-4599-1}WdtPersistentData 670ED0DA-6F6
                                                               GnvsAreaVar A345963D-DABC-0ED0-}
GnvsAreaVar A345963D-DABC-0ED}
                                                               HobRomImage 6F65670E-D26F-4599-}
HobRomImage 6F65670E-D26F-459}
                                                               IccAdvancedSetupDataVar 19B2CB8}
IccAdvancedSetupDataVar 19B2C}
                                                               KEK D26F6F65-4599-1A11-B849-B91}
KEK D26F6F65-4599-1A11-B849-B}
                                                               Lang D26F6F65-4599-1A11-B849-B9}
Kernel CopyOfUSN 98E0000D-2B0
                                                               LastBoot CB8C2B03-19B2-3AD7-3D9}
Kernel USN 98E0000D-2B03-CB8C
                                                               md 0398E000-8C2B-B2CB-19D7-3A3D}
Lang D26F6F65-4599-1A11-B849-}
                                                               MemCeil. D26F6F65-4599-1A11-B84}
LastBoot CB8C2B03-19B2-3AD7-3}
                                                               MonotonicCounter D26F6F65-4599-
md 0398E000-8C2B-B2CB-19D7-3A}
                                                               MrcS3Resume BCA34596-D0DA-670E-3
                   944 bytes in 7 files
                                                                                    725 bytes in 3 files
-D26F-9945-111AB849B91F_NV+BS+RT_0.bin
                                                              670E-6F65-6FD2-9945111AB849 NV+BS+RT 0.bin
                                            1 03/02/14 23:00
                                                                                                             713 03/02/14 22:55
                 17,925 bytes in 52 files =
                                                                                  17,706 bytes in 48 files
```

#### Secure Boot On/Off is Stored in "Setup"

#### Secure Boot On

#### Secure Boot Off

```
EFI Variable (offset = 0x4bb4):
                                                     Variable (offset = 0x4bb4):
                                                          : Setup
Guid
       : DODABCA3-670E-6F65-6FD2-9945111AB849
                                                  Guid
                                                          : DODABCA3-670E-6F65-6FD2-9945111AB849
Attributes: 0x7 ( NV+BS+RT )
                                                  Attributes: 0x7 ( NV+BS+RT )
Data:
                                                  00 01 20 00 00 00 00 02 00 00 01 00 00 01 00 01
8c 16 32 00 00 01 00 01 01 00 00 00 01
                                                             00 00 01 01 00 00 00 01
                                                  01 01 01 01 00 01 00 00 01 01 00 00 01
01 01 01 01 00 01 00 00 01 01 00 00
                                                  00 00 00 00 00 01 01 01 01 01 00 00 00
                                                  01 00 01 00 01 01 00 01 00 00 01 01
04 04 00 00 00 00 00 00 00 00 00 00 00
                                                  00 00 00 00 00 00 00 00 00 00 00 00 00
                                                  00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 01 01 01 01 01 02 02 01 00 01
                                                  00 00 00 01 01 01 01 01 02 02 01 00 01
00 00 00 20 00 00 00 00 01 00 03 00 37 00 44 00
                                                  00 00 00 20 00 00 00 01 00 03 00 37 00 44 00
1c 19 00 2d 00 38 00 1c 10 01 41 00 51 00 1c 1a
                                                  1c 19 00 2d 00 38 00 1c 10 01 41 00 51 00 1c 1a
```

#### Verification Policies are Stored in "Setup"



- Read 'Setup' UEFI variable and look for sequences
- 04 04 04, 00 04 04, 05 05 05, 00 05 05
- We looked near Secure Boot On/Off Byte!
- Modify bytes corresponding to policies to 00
   (ALWAYS EXECUTE) then write modified 'Setup' variable

#### Patching Image Verification Policies...

```
[CHIPSEC] Reading EFI variable Name='Setup' GUID={EC87D643-EBA4-4BB5-A1E5-
  3F3E36B20DA9} from 'Setup orig.bin' via Variable API..
EFI variable:
         : Setup
Name
GUID
         : EC87D643-EBA4-4BB5-A1E5-3F3E36B20DA9
                                               OptionRomPolicy
Data
                                               FixedMediaPolicy
                                               RemovableMediaPolicy
00 00 00 00 00 00 01 01 00 00 00 04 04
[CHIPSEC] (uefi) time elapsed 0.000
[CHIPSEC] Writing EFI variable Name='Setup' GUID={EC87D643-EBA4-4BB5-A1E5-
  3F3E36B20DA9} from 'Setup policy exploit.bin' via Variable API..
Writing EFI variable:
Name
         : Setup
         : EC87D643-EBA4-4BB5-A1E5-3F3E36B20DA9
GUID
Data
00 00 00 00 00 00 01 01 00 00 04 00 00
[CHIPSEC] (uefi) time elapsed 0.203
```

#### **CSM Enabled With Secure Boot**

- CSM allows legacy OS to boot on top of UEFI firmware without any Secure Boot checks
- Some systems have CSM enabled by default with Secure Boot enabled and fallback to boot from MBR when UEFI signature verification fails

Mitigations: Never load CSM when Secure Boot is enabled

# Other Critical Secure Boot Config Stored in Unprotected Setup UEFI Variable

- CSM Enable policy: allows malware to enable CSM with Secure Boot and boot from MBR
- "Clear Secure Boot Keys" control: allows malware to clear all keys including PK thus disabling Secure Boot
- "Restore Default Secure Boot Keys" control: allows malware to revert all keys and blacklist to potentially insecure "default" values

**Mitigations**: UEFI firmware must never store setting critical for Secure Boot in unprotected UEFI variables (such as Setup)

# 4.1 (3) Attacking Secure Boot via PE/TE Header Vulnerability

### Does firmware allow unsigned TE executables?

SecureBoot EFI variable doesn't exist or equals to SECURE\_BOOT\_MODE\_DISABLE? EFI\_SUCCESS

File is not valid PE/COFF image? EFI\_ACCESS\_DENIED

SecureBootEnable NV EFI variable doesn't exist or equals to SECURE\_BOOT\_DISABLE? **EFI\_SUCCESS** 

SetupMode NV EFI variable doesn't exist or equals to SETUP\_MODE? EFI\_SUCCESS

### PE/TE Header Handling by the BIOS

Decoded UEFI BIOS image from SPI Flash

```
C:\chipsec>chipsec_util.py decode spi_flash.bin nvar
[+] imported common configuration: chipsec.cfg.common
[CHIPSEC] Executing command 'decode' with args ['spi_flash.bin', 'nvar']
[CHIPSEC] Decoding SPI ROM image from a file 'spi_flash.bin'
[CHIPSEC] Found SPI Flash descriptor at offset 0x0 in the binary 'spi_flash.bin'
[CHIPSEC] (decode) time elapsed 18.003
C:\chipsec>
    {C:\chipsec\spi_flash.bin.dir\1_200000-7FFFFF_BIOS.bin.dir\FV\01_8C8CE578-8A3D-4F1C-9935-896185C32DD3.dir\5AE3F37E-4E...
    Size
                                                                                                                       Size
                           Name
                                                                                         Name
                                                                                                                         Up
    00 8C8CE578-8A3D-4F1C-9935-896185C32}Folder
                                                                  00 S COMPRESSION
                                                                                                                      1331 K
    01 8C8CE578-8A3D-4F1C-9935-896185C32}Folder
                                                                   00 S COMPRESSION.gz
                                                                                                                      148477
    02 8C8CE578-8A3D-4F1C-9935-896185C32}Folder
                                                                   01 S FREEFORM SUBTYPE GUID
                                                                                                                          794
     00 8C8CE578-8A3D-4F1C-9935-896185C32}131072
                                                                   02 S USER INTERFACE
    01 8C8CE578-8A3D-4F1C-9935-896185C32}5008 K
                                                                   CORE DXE.efi
                                                                                                                      1330 k
     02 8C8CE578-8A3D-4F1C-9935-896185C32}638976
```

#### PE/TE Header Confusion Issue

- TE format doesn't support signatures so BIOS has to deny loading such image
- In practice, BIOS implementations may differ...
- ExecuteSecurityHandler calls GetFileBuffer to read an executable image
- Which reads the image, checks if it has a valid PE/COFF header and returns EFI\_LOAD\_ERROR if not
- In case of an image load error,
  ExecuteSecurityHandler returns EFI SUCCESS (0)
- Signature Checks are Skipped!

#### PE/TE Header Confusion Attack

- Convert malicious PE/COFF EFI executable (bootkit.efi) to TE by replacing the image header
- Replace OS boot loaders with resulting TE EFI executable
- Vulnerable BIOS skips signature check for this executable
- Malicious bootkit.efi loads & patches original OS boot loader

#### Exercise 4.1

Bypassing UEFI Secure Boot (PE/TE)



### 4.2 Attacking SPI Flash Protections

#### **BIOS** Range is Not Protected in SPI

- BIOS Write Protections often still not properly enabled on many systems
- SMM based write protection of entire BIOS region is often not used:
   BIOS\_CONTROL[SMM\_BWP]
- If SPI Protected Ranges (mode agnostic) are used (defined by PR0-PR4 in SPI MMIO), they often don't cover entire BIOS & NVRAM
- Some platforms use SPI device specific write protection but only for boot block/startup code or SPI Flash descriptor region

#### Mitigations:

- Set BIOS\_CONTROL[SMM\_BWP] 1
- Program SPI flash protected ranges (PRx) to cover BIOS range

References: Persistent BIOS Infection (used <u>flashrom</u> on legacy BIOS), <u>Evil Maid Just Got Angrier</u>, <u>BIOS Chronomancy</u>, <u>A Tale Of One Software Bypass Of Windows 8 Secure Boot</u>

### Checking with common bios wp

# chipsec main.py --module common.bios wp

```
[*] running module: chipsec.modules.common.bios wp
[x] [ Module: BIOS Region Write Protection
[*] BIOS Control = 0x02
   [05] SMM BWP = 0 (SMM BIOS Write Protection)
   [04] TSS = 0 (Top Swap Status)
   [01] BLE = 1 (BIOS Lock Enable)
   [00] BIOSWE = 0 (BIOS Write Enable)
[!] Enhanced SMM BIOS region write protection has not been enabled (SMM BWP is not used)
[*] BIOS Region: Base = 0x00500000, Limit = 0x007FFFFF
SPI Protected Ranges
PRx (offset) | Value | Base | Limit | WP? | RP?
PRO (74) | 87FF0780 | 00780000 | 007FF000 | 1 | 0
PR1 (78) | 00000000 | 00000000 | 00000000 | 0 | 0
PR2 (7C) | 00000000 | 00000000 | 0 00000000 | 0
PR3 (80) | 00000000 | 00000000 | 0 | 0
PR4 (84) | 00000000 | 00000000 | 00000000 | 0 | 0
[!] SPI protected ranges write-protect parts of BIOS region (other parts of BIOS can be
modified)
[!] BIOS should enable all available SMM based write protection mechanisms or configure
```

- [-] FAILED: BIOS is NOT protected completely

SPI protected ranges to protect the entire BIOS region

# SMI Suppression Attack (If SMM Based BIOS WP is Not Used)

- Some systems write-protect BIOS by disabling BIOS Write-Enable (BIOSWE) and setting BIOS Lock Enable (BLE) but don't use SMM based write-protection BIOS\_CONTROL[SMM\_BWP]
- SMI event is generated when Update SW writes BIOSWE=1
- Possible attack against this configuration is to block SMI events
- E.g. disable all chipset sources of SMI: clear SMI\_EN[GBL\_SMI\_EN]
  if BIOS didn't set GBL\_SMI\_LOCK: Setup for Failure: Defeating
  SecureBoot
- Another variant is to disable specific TCO SMI source used for BIOSWE/BLE (clear TCO\_EN in SMI\_EN if BIOS didn't set TCO\_LCK)

#### Mitigations:

 Set BIOS\_CONTROL[SMM\_BWP] ← 1 and lock SMI configuration (set GBL SMI LCK, TCO LCK)

### Checking with common.bios\_smi

# chipsec\_main.py --module common.bios\_smi

```
[*] running module: chipsec.modules.common.bios smi
[x] [ Module: SMI Events Configuration
[-] SMM BIOS region write protection has not been enabled (SMM BWP is not used)
[*] PMBASE (ACPI I/O Base) = 0 \times 0400
[*] SMI EN (SMI Control and Enable) register [I/O port 0x430] = 0x00002033
   [13] TCO EN (TCO Enable) = 1
   [00] GBL SMI EN (Global SMI Enable) = 1
[+] All required SMI events are enabled
[*] TCOBASE (TCO I/O Base) = 0 \times 0460
[*] TCO1 CNT (TCO1 Control) register [I/O port 0x468] = 0x1800
   [12] TCO LOCK = 1
[+] TCO SMI configuration is locked
[*] GEN PMCON 1 (General PM Config 1) register [BDF 0:31:0 + 0xA0] = 0x0A14
   [04] SMI LOCK = 1
[+] SMI events global configuration is locked
[+] PASSED: All required SMI sources seem to be enabled and locked!
```

### Unlocked SPI Flash Config. / PRx

- Some BIOS rely on SPI Protected Ranges (PR0-PR4 registers in SPI MMIO) to provide write protection of regions of SPI Flash
- SPI Flash Controller configuration including PRx has to be locked down by BIOS via Flash Lockdown
- If BIOS doesn't lock SPI Controller configuration (by setting FLOCKDN bit in HSFS SPI MMIO register), malware can disable SPI protected ranges re-enabling write access to SPI Flash

#### Mitigations:

• Set HSFS [FLOCKDN] 1

### Checking with common.spi\_lock

[+] PASSED: SPI Flash Controller configuration is locked

# Insecure Access Permissions in SPI Flash Descriptor

- SPI flash memory is operating in descriptor mode, i.e. when valid flash descriptor is present in SPI flash
- In descriptor mode, flash descriptor defines access permissions to various regions in SPI flash by different SPI bus masters, e.g. by CPU host software such as BIOS or OS
- FD itself is a region and is access permission to FD allows writes from BIOS/OS after manufacturing then any code at BIOS/OS level can modify it

Master Read/Write Acces	s	to Flash	Regions	
Region		CPU/BIOS	ME	GBe
0 Flash Descriptor 1 BIOS		R RW	R 	

Access permissions to SPI flash descriptor

# Checking with common.spi\_desc

# chipsec\_main.py --module common.spi\_desc

[\*] running module: chipsec.modules.common.spi desc

[+] PASSED: SPI flash permissions prevent SW from writing to flash descriptor

# Exercise 4.2 BIOS/SPI Flash Protections

# 4.3 Attacking BIOS Update

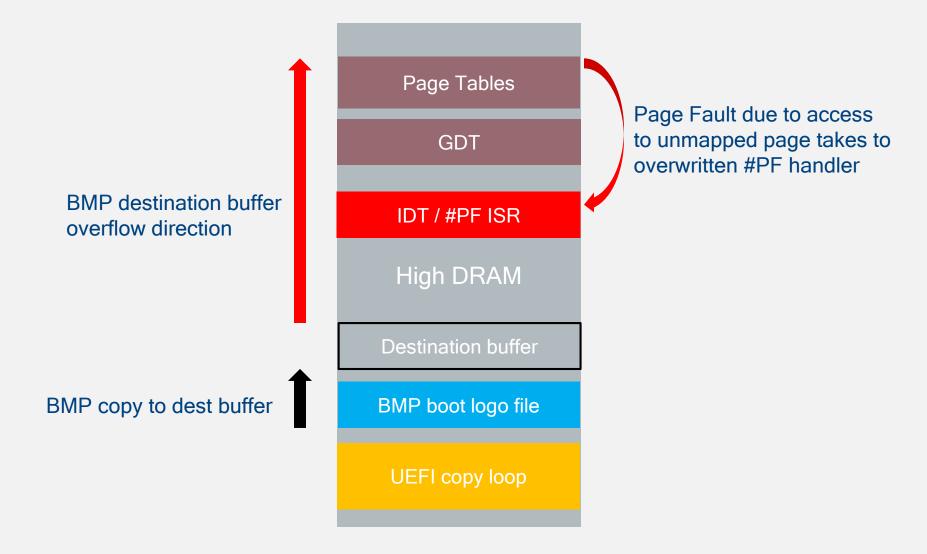
# **Exploiting Unsigned BMP Image File**

- Unsigned sections within BIOS update (e.g. boot splash logo BMP image)
- BIOS displayed the logo before SPI Flash write-protection was enabled
- EDK ConvertBmpToGopBlt() integer overflow followed by memory corruption during DXE while parsing BMP image
- Copy loop overwrote #PF handler and triggered #PF

#### References:

**Attacking Intel BIOS** 

# **UEFI Exploit via .BMP Logo File**



Source: Attacking Intel BIOS by Rafal Wojtczuk & Alexander Tereshkin

# **RBU Packet Parsing Vulnerability**

- Legacy BIOS with signed BIOS update
- OS schedules BIOS update placing new BIOS image in DRAM split into RBU packets
- Upon reboot, BIOS Update SMI Handler reconstructs BIOS image from RBU packets in SMRAM and verifies signature
- Buffer overflow (memcpy with controlled size/dest/src)
  when copying RBU packet to a buffer with reconstructed
  BIOS image

#### References:

BIOS Chronomancy: Fixing the Core Root of Trust for Measurement Defeating Signed BIOS Enforcement

## **EDK2 Capsule BOF Vulnerabilities**

- Attacker sets up a capsule in memory, and when capsule update is called, BIOS parses the data provided by the attacker
- Capsule Coalescing when the blocks of a capsule are made contiguous, an integer overflow allowed attackers to control a memory copy operation.
- Capsule Envelop when blocks of the capsule are parsed, an integer overflow allowed attackers to cause a small allocation and large memory copy operation.

#### References:

Extreme Privilege Escalation on Windows 8/UEFI Systems

# 4.4 Attacking SMRAM

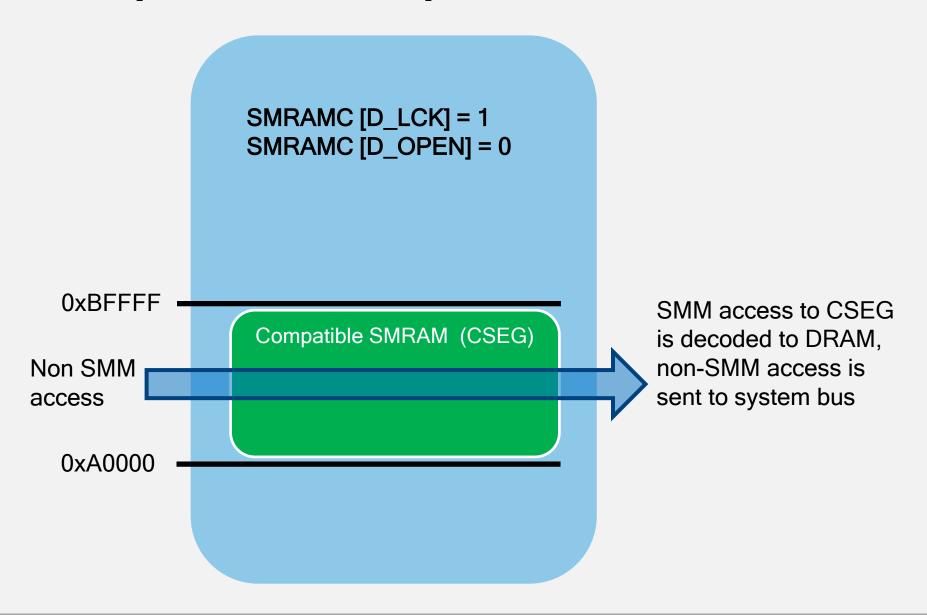
# Unlocked Compatible/Legacy SMRAM

- D\_LCK bit in SMRAMC register locks down configuration of Compatible SMM range (a.k.a. CSEG)
- SMRAMC [D\_OPEN] = 0 forces access to legacy SMM space decode to system bus rather than to DRAM where SMI handlers are when CPU is not in System Management Mode (SMM)
- When D\_LCK is not set by BIOS, SMM space decode can be changed to open access to CSEG if CPU is not in SMM

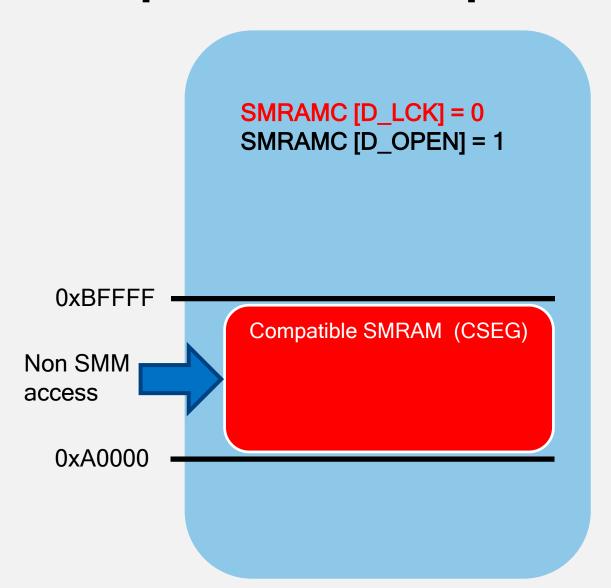
#### References:

<u>Using CPU SMM to Circumvent OS Security Functions</u> <u>Using SMM For Other Purposes</u>

#### **Compatible SMM Space: Normal Decode**



## **Compatible SMM Space: Unlocked**



Non-SMM access to CSEG is decoded to DRAM where SMI handlers can be modified

## Detecting with common.smm

# **SMRAM** "Cache Poisoning" Attack

- CPU executes from cache if memory type is cacheable
- Ring0 exploit can make SMRAM cacheable (variable MTRR)
- Ring0 exploit can then populate cache-lines at SMBASE with SMI exploit code (ex. modify SMBASE) and trigger SMI
- CPU upon entering SMM will execute SMI exploit from cache

Mitigations: CPU System Management Range Registers (SMRR) forcing UC and blocking access to SMRAM when CPU is not in SMM. BIOS has to enable SMRR

#### References:

Attacking SMM Memory via Intel Cache Poisoning Getting Into the SMRAM: SMM Reloaded

# Checking with common.smrr

```
[*] running module: chipsec.modules.common.smrr
[x] [ Module: CPU SMM Cache Poisoning / SMM Range Registers (SMRR)
[+] OK. SMRR are supported in IA32 MTRRCAP MSR
[*] Checking SMRR Base programming..
BASE = 0xBD000000
   MEMTYPE = 6
[+] SMRR Memtype is WB
[+] OK so far. SMRR Base is programmed
[*] Checking SMRR Mask programming..
[*] IA32 SMRR MASK MSR = 0 \times 000000000 FF800800
   MASK = 0 \times FF800000
   VLD = 1
[+] OK so far. SMRR are enabled in SMRR MASK MSR
[*] Verifying that SMRR BASE/MASK have the same values on all logical CPUs..
[CPU0] SMRR BASE = 00000000BD000006, SMRR MASK = 00000000FF800800
[CPU1] SMRR BASE = 00000000BD000006, SMRR MASK = 00000000FF800800
[CPU2] SMRR BASE = 00000000BD000006, SMRR MASK = 00000000FF800800
[CPU3] SMRR BASE = 00000000BD000006, SMRR MASK = 00000000FF800800
[+] OK so far. SMRR MSRs match on all CPUs
```

[+] PASSED: SMRR protection against cache attack seems properly configured

# **SMRAM Memory Remapping Attack**

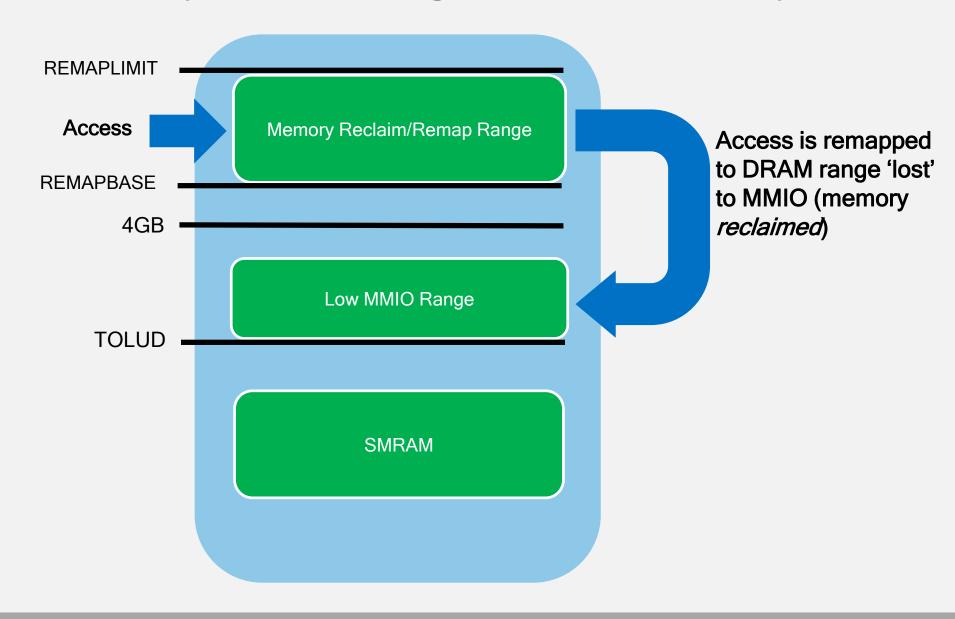
- Remap Window is used to reclaim DRAM range below 4Gb "lost" for Low MMIO
- Defined by REMAPBASE/REMAPLIMIT registers in Memory Controller PCIe configuration space
- MC remaps Reclaim Window access to DRAM below 4GB (above Top Of Low DRAM)
- If not locked, OS malware can reprogram target of reclaim to overlap with SMRAM (or something else)

**Mitigations**: BIOS has to lock down Memory Map registers including **REMAP\***, **TOLUD/TOUUD** 

#### References:

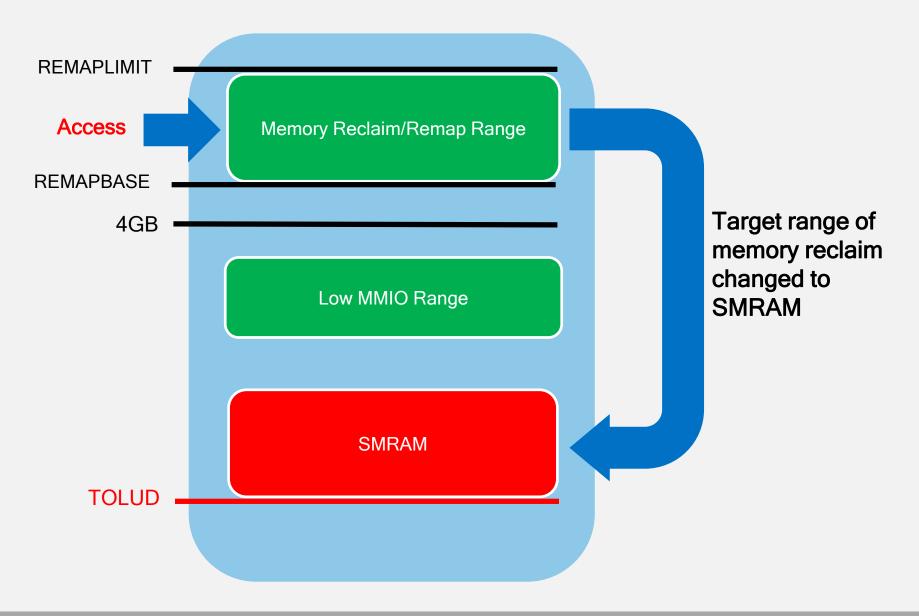
Preventing & Detecting Xen Hypervisor Subversions

### Memory Remapping: Normal Memory Map



Source: <u>Preventing & Detecting Xen Hypervisor Subversions</u>

### **Memory Remapping: Attacking SMRAM**



Source: <u>Preventing & Detecting Xen Hypervisor Subversions</u>

# Checking with remap

# chipsec main.py --module remap [\*] running module: chipsec.modules.remap [x] [ Module: Memory Remapping Configuration [\*] Registers: [ \* ] TOUUD : 0x00000011E600001 [\*] REMAPLIMIT: 0x00000011E500001 [\*] REMAPBASE : 0x000000100000001 [\*] TOLUD : 0xDFA00001 TSEGMB : 0xDD000001 [\*] [\*] Memory Map: [ \* ] Top Of Upper Memory: 0x00000011E600000 [\*] Remap Limit Address: 0x00000011E5FFFFF [\*] Remap Base Address: 0x000000100000000 : 0x000000100000000 [\*] 4GB Top Of Low Memory : 0x0000000DFA00000 TSEG (SMRAM) Base : 0x00000000DD000000 [\*] [\*] checking memory remap configuration.. [\*] Memory Remap is enabled

[+] Remap window configuration is correct: REMAPBASE <= REMAPLIMIT < TOUUD

- [\*] checking if memory remap configuration is locked..
- [+] TOUUD is locked
- [+] TOLUD is locked
- [+] REMAPBASE and REMAPLIMIT are locked

[+] All addresses are 1MB aligned

[+] PASSED: Memory Remap is configured correctly and locked

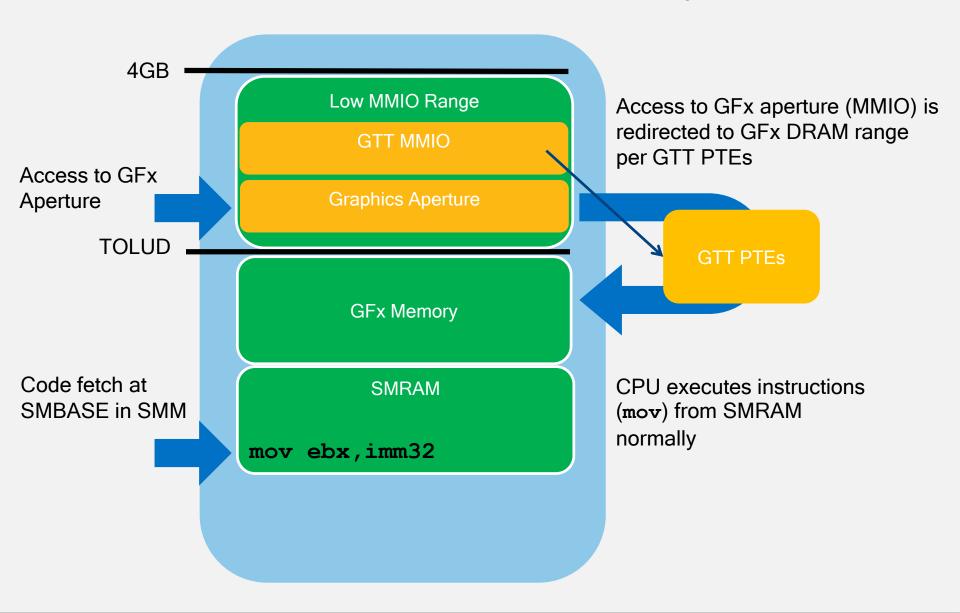
# **SMRAM Redirection via GFx Aperture**

- If BIOS doesn't lock down memory config, boundary separating DRAM and MMIO (TOLUD) can be moved somewhere else. E.g. malware can move it below SMRAM to make SMRAM decode as MMIO
- Graphics Aperture can then be overlapped with SMRAM and used to redirect MMIO access to memory range defined by PTE entries in Graphics Translation Table (GTT)
- When CPU accesses protected SMRAM range to execute SMI handler, access is redirected to unprotected memory range somewhere else in DRAM

**Mitigations:** Similarly to *Remapping Attack*, BIOS has to lock down HW memory configuration (i.e. **TOLUD**) to mitigate this attack

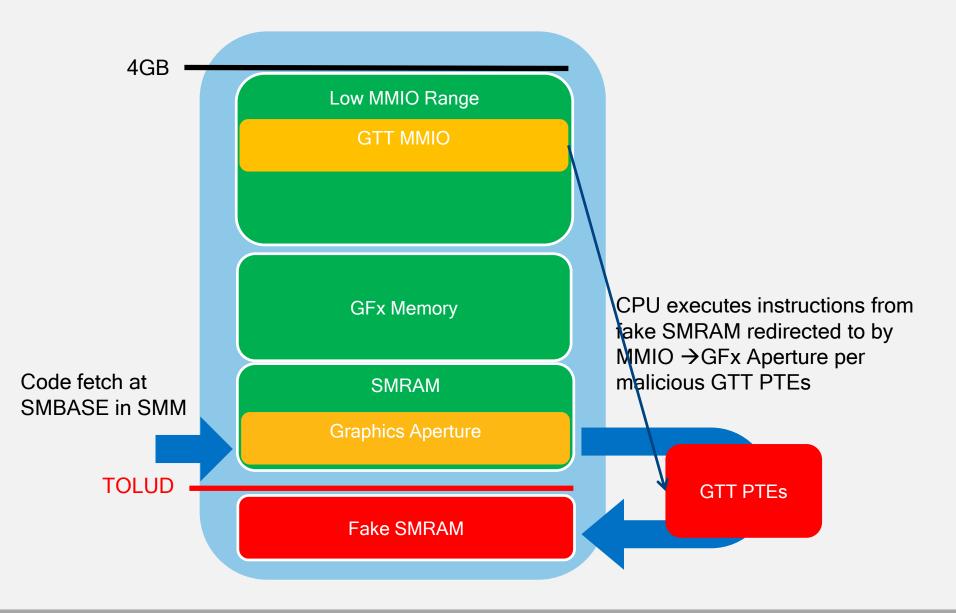
References: System Management Mode Design and Security Issues (GART)

#### **Access in SMM: Normal Memory Map**



Source: System Management Mode Design and Security Issues

#### **Access in SMM: GFx Aperture Redirection**



Source: System Management Mode Design and Security Issues

#### **DMA Attacks on SMRAM**

- Protection from inbound DMA access is guaranteed by programming TSEG range
- If BIOS doesn't lock down TSEG range configuration, malware can move TSEG outside of where actual SMRAM is
- Then program one of DMA capable devices (e.g. GPU device) or Graphics Aperture to access SMRAM

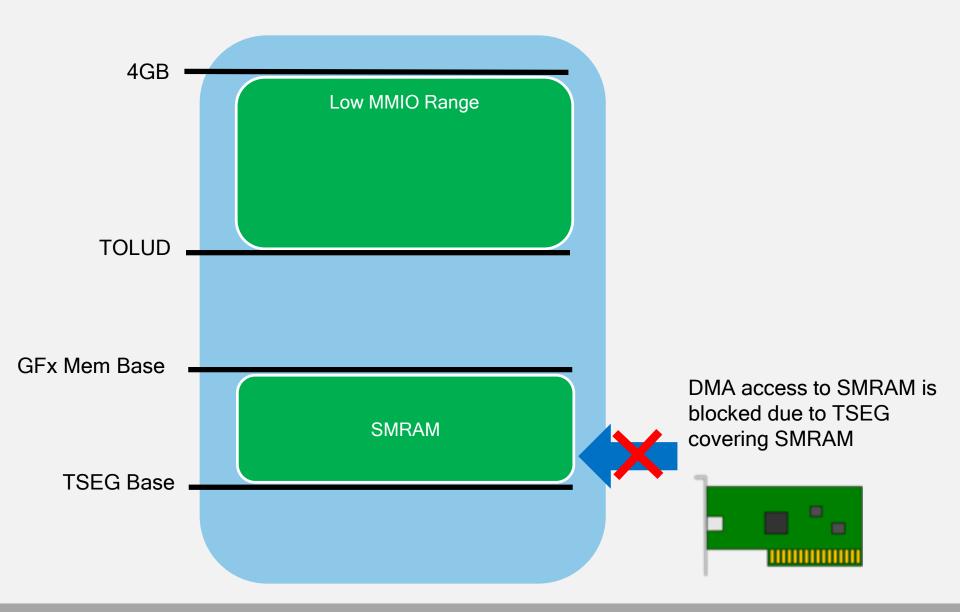
Mitigations: BIOS has to lock down configuration required to define range protecting SMRAM from inbound DMA access (e.g. TSEG range)

#### References:

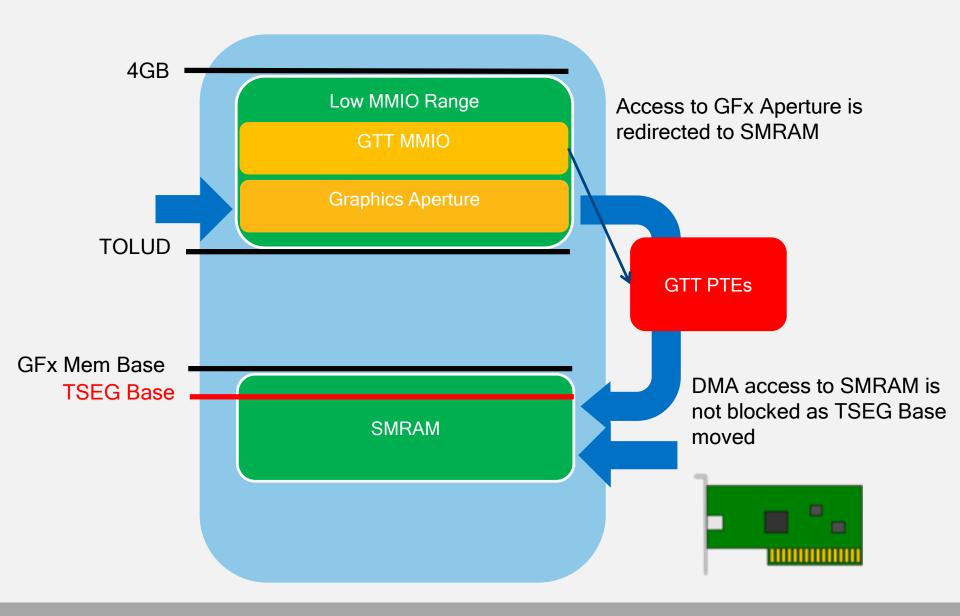
Programmed I/O accesses: a threat to Virtual Machine Monitors?

System Management Mode Design and Security Issues

#### **DMA Access to SMRAM**



#### **DMA Access to SMRAM: DMA Attacks**



# Checking with smm\_dma

# chipsec\_main.py --module smm\_dma

```
[*] running module: chipsec.modules.smm dma
[x] [ Module: SMRAM DMA Protection
[*] Registers:
[*] PCIO.O.O TOLUD = 0xDFA00001 << Top of Low Usable DRAM (b:d.f <math>00:00.0 + 0xBC)
[*] PCIO.O.O BGSM = 0xDD800001 << Base of GTT Stolen Memory (b:d.f 00:00.0 + 0xB4)
[*] PCIO.O.O TSEGMB = 0xDD000001 << TSEG Memory Base (b:d.f 00:00.0 + 0xB8)
[*] IA32 SMRR PHYSBASE = 0 \times DD0000006 << SMRR Base Address MSR (MSR <math>0 \times 1F2)
[*] IA32 SMRR PHYSMASK = 0xFF800800 \ll SMRR Range Mask MSR (MSR 0x1F3)
[*] Memory Map:
[*] Top Of Low Memory : 0xDFA00000
[*] TSEG Range (TSEGMB-BGSM) : [0xDD000000-0xDD7FFFFF]
[*] SMRR Range (size = 0x00800000): [0xDD000000-0xDD7FFFFF]
[*] checking locks..
[+] TSEGMB is locked
[+] BGSM is locked
[*] checking TSEG alignment..
[+]
     TSEGMB is 8MB aligned
[*] checking TSEG covers entire SMRR range..
[+] TSEG covers entire SMRAM
[+] PASSED: TSEG is properly configured. SMRAM is protected from DMA attacks
```

# 4.5 Attacking Hardware Configuration

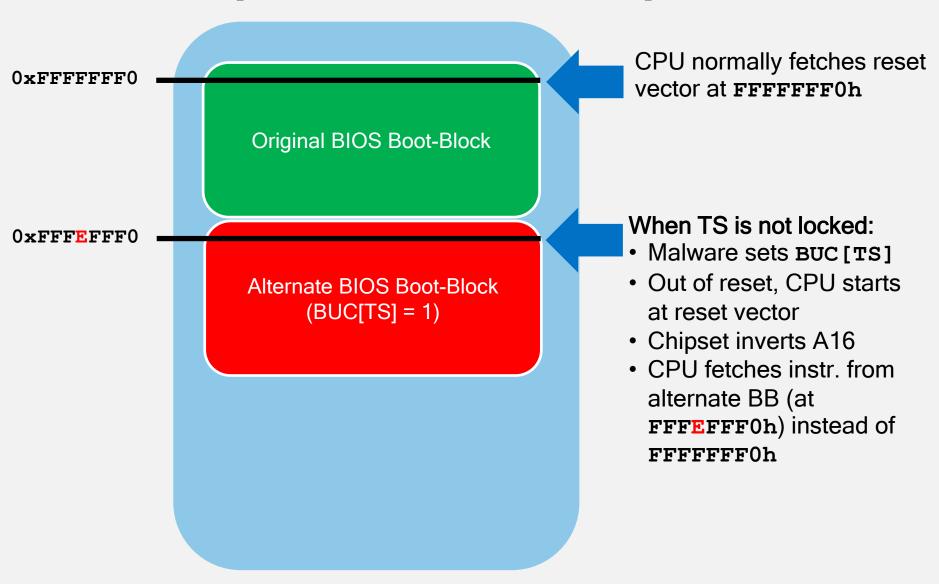
# **BIOS Top Boot-Block Swap Attack**

- Top Swap Mode allows fault-tolerant update of the BIOS boot-block
- Enabled by **BUC[TS]** in Root Complex MMIO range
- Chipset inverts A16 line (A16-A20 depending on the size of bootblock) of the address targeting ROM, e.g. when CPU fetches reset vector on reboot
- Thus CPU executes from 0xfffffff inside "backup" boot-block rather than from 0xfffffff
- Top Swap indicator is not reset on reboot (requires RTC reset)
- When not locked/protected, malware can redirect execution of reset vector to alternate (backup) boot-block

Mitigations: BIOS has to lock down Top Swap configuration (*BIOS Interface Lock* in *General Control & Status* register) & protect swap boot-block range in SPI

References: BIOS Boot Hijacking and VMware Vulnerabilities Digging

# **BIOS Top Boot-Block Swap Attack**



Source: BIOS Boot Hijacking and VMware Vulnerabilities Digging

# Checking with common.bios\_ts

# chipsec\_main.py --module common.bios\_ts

```
[*] running module: chipsec.modules.common.bios ts
[x] [ Module: BIOS Interface Lock and Top Swap Mode
[*] BC = 0x2A << BIOS Control (b:d.f 00:31.0 + 0xDC)
   [00] BIOSWE
                      = 0 << BIOS Write Enable
   [01] BLE = 1 << BIOS Lock Enable
   [02] SRC = 2 \ll SPI Read Configuration
   [04] TSS = 0 \ll Top Swap Status
   [05] SMM BWP = 1 << SMM BIOS Write Protection
[*] BIOS Top Swap mode is disabled
[*] BUC = 0x00000000 << Backed Up Control (RCBA + <math>0x3414)
                      = 0 << Top Swap
   [00] TS
[*] RTC version of TS = 0
[*] GCS = 0 \times 000000021 \ll General Control and Status (RCBA + <math>0 \times 3410)
   [00] BILD = 1 << BIOS Interface Lock Down
                      = 0
   [10] BBS
```

[+] PASSED: BIOS Interface is locked (including Top Swap Mode)

# 4.6 (1) Attacking SMI Handlers: SMI Call-Outs

#### SMI Call-Out Vulnerabilities

- OS level exploit stores payload in F-segment below 1MB (0xF8070 physical address)
- Exploit has to also reprogram PAM to write to F-segment
- Then triggers SW SMI via APMC port (I/O 0xB2)
- SMI handler does CALL 0F000:08070 in SMM

#### References:

- In 2009, SMI call-out vulnerabilities were discovered by Rafal Wojtczuk and Alex Tereshkin in EFI SMI handlers (<a href="Attacking Intel BIOS">Attacking Intel BIOS</a>) and by Filip Wecherowski in legacy SMI (<a href="BIOS SMM Privilege Escalation Vulnerabilities">BIOS SMM Privilege Escalation Vulnerabilities</a>)
- Also discussed by Loic Duflot in <u>System Management Mode Design and Security Issues</u>
- In 2015, researchers from LegbaCore found that many modern systems are still vulnerable to these issues <u>How Many Million BIOS Would You Like To Infect</u> (<u>paper</u>)

#### **Legacy SMI Call-Out Vulnerabilities**

Disassembly of the code of \$SMISS handler, one of SMI handlers in the BIOS firmware in ASUS Eee PC 1000HE system.

0003F073: 50 push ax

0003F074: B4A1 mov ah,0A1

\*\* 0003F076: 9A197D00F0 call 0F000:07D19

0003F07B: 2404 and al,004

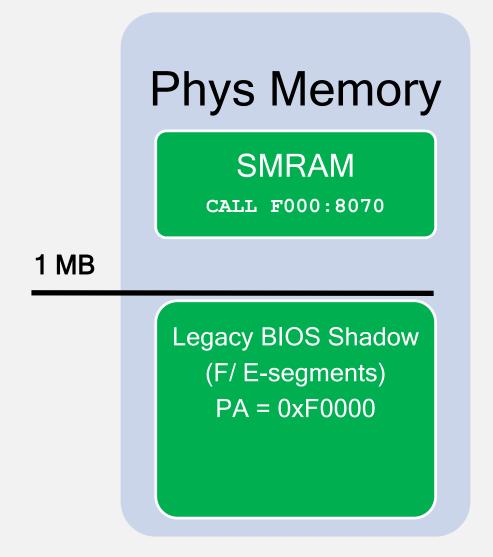
0003F07D: 7414 je 00003F093 0003F07F: B434 mov ah,034

\*\* 0003F081: 9A708000F0 call 0F000:08070

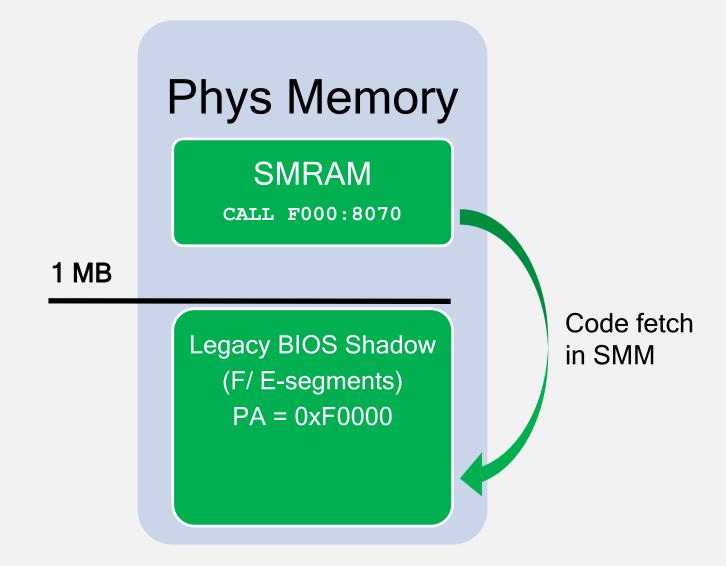
14 call-out vulnerabilities in one SMI handler!

BIOS SMM Privilege Escalation Vulnerabilities

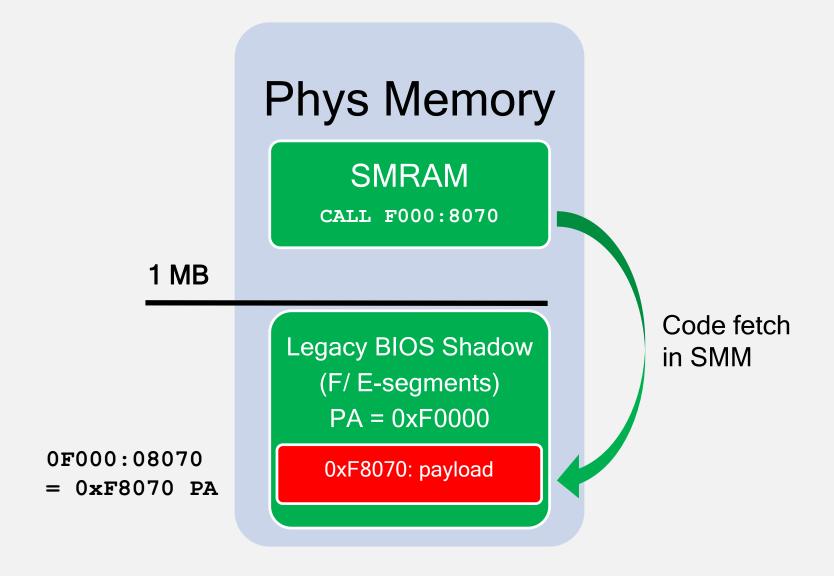
### **Legacy SMI Handlers Calling Out of SMRAM**



### **SMI Handlers Calling Out of SMRAM**



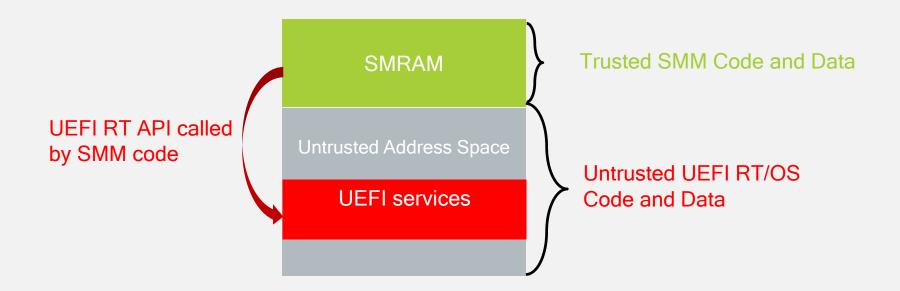
### **SMI Handlers Calling Out of SMRAM**



#### **UEFI SMI Call-Outs**

```
[uefi] EFI System Table:
49 42 49 20 53 59 53 54 1f 00 02 00 78 00 00 00
                                     IBI SYST
33 15 11 86 00 00 00 00 98 33 45 ff ff ff ff ff
                                     3
                                             3E
00 00 00 00 00 00 00 00 18 ae bf ff ff ff ff ff
18 9e bf ff ff ff ff ff
Header:
 Signature : IBI SYST
 Revision : 2.31
 HeaderSize
           : 0x00000078
 CRC32
           : 0x86111533
 Reserved : 0x00000000
EFI System Table:
 FirmwareVendor : 0xFFFFFFFFF453398
 FirmwareRevision : 0x0000000000002270
 ConsoleInHandle : 0x0000000000000000
 ConTn
                : 0x00000000000000000
 ConsoleOutHandle : 0x00000000000000000
 ConOut
                : 0x00000000000000000
 StandardErrorHandle: 0x00000000000000000
 StdEnn
 RuntimeServices : 0xFFFFFFFFFBFAE18
 BootServices
 ConfigurationTable : 0xFFFFFFFFFFBF9E18
[uefi] UEFI appears to be in Runtime mode
```

#### Modern EFI Firmware Also Affected



How Many Million BIOS Would You Like To Infect by LegbaCore

#### Statically analyzing SMI handlers for call-outs

**Legacy SMI handlers** do far calls to BIOS functions in F/E - segments (0xE0000 - 0xFFFFF physical memory) with specific code segment selectors

```
[+] searching for pattern '\x9a..\x88\x00' in file 'BIOS_1b.mod'
offset 0x009914: \x9a\xd8\x71\x88\x00 (call 0x0088 : 0x71d8)
offset 0x00e705: \x9a\x09\x49\x88\x00 (call 0x0088 : 0x4909)
offset 0x00e711: \x9a\x09\x49\x88\x00 (call 0x0088 : 0x4909)
offset 0x00e71b: \x9a\x09\x49\x88\x00 (call 0x0088 : 0x4909)
offset 0x00e723: \x9a\x09\x49\x88\x00 (call 0x0088 : 0x4909)
offset 0x00eda4: \x9a\xd8\x71\x88\x00 (call 0x0088 : 0x71d8)
offset 0x00edb5: \x9a\xd8\x71\x88\x00 (call 0x0088 : 0x71d8)
offset 0x00edcc: \x9a\xd8\x71\x88\x00 (call 0x0088 : 0x71d8)
offset 0x00eddd: \x9a\xd8\x71\x88\x00 (call 0x0088 : 0x71d8)
offset 0x00edf0: \x9a\xd8\x71\x88\x00 (call 0x0088 : 0x71d8)
offset 0x00ee06: \x9a\xd8\x71\x88\x00 (call 0x0088 : 0x71d8)
offset 0x014808: \x9a\x98\x21\x88\x00 (call 0x0088 : 0x2198)
offset 0x014832: \x9a\x0b\x21\x88\x00 (call 0x0088 : 0x210b)
offset 0x014855: \x9a\x98\x21\x88\x00 (call 0x0088 : 0x2198)
offset 0x014872: \x9a\x98\x21\x88\x00 (call 0x0088 : 0x2198)
offset 0x0148a2: \x9a\xf4\x4c\x88\x00 (call 0x0088 : 0x4cf4)
```

#### Statically analyzing SMI handlers for call-outs

Searching where EFI DXE SMM drivers reference/fetch outside of SMRAM range of addresses with IDAPython plugin by LegbaCore:

```
oid __fastcall smi_handler_da0889e8(__int64 a1, __int64 a2)
 __int64 *v2; // rdx@2
 if (*(_{QWORD} *)a2 == 0x90i64)
  switch ( VD8AD8024 + 0x80000000 )
     case 0u:
         AD801C = readmsr_wrapper(vD8AD8018, (__int64)&qword_DA087B78[145]);
      break;
      wrmsr_wrapper(vD8AD8018, vD8AD801C);
```

How Many Million BIOS Would You Like To Infect by LegbaCore

# **Dynamically detecting SMM call-outs**

DXE SMI drivers may call Runtime, Boot or DXE services API

- Find Runtime, Boot and DXE service tables containing UEFI API function pointers in memory (EFI System Table)
- Patch each function with detour code chaining the original function
- Enumerate and invoke all SMI handlers
- If SMI handler calls-out to some UEFI API, patch will get invoked

Difficulties with this approach:

- it needs enumeration of all SMI handlers (with proper interfaces)
- SMI handlers may call functions not in RT/BS/DXE service tables

# Hooking runtime UEFI services...

```
[uefi] EFI Runtime Services Table:
52 55 4e 54 53 45 52 56 1f 00 02 00 88 00 00 00 |
                                                RUNTSERV
6f aa 42 cb 00 00 00 00 2c 2b e0 fe ff ff ff ff |
                                                οВ
bc 2c e0 fe ff ff ff ff 20 2e e0 fe ff ff ff ff
0c 30 e0 fe ff ff ff ff dc 14 65 da 00 00 00 00
00 14 65 da 00 00 00 00 34 0b d6 fe ff ff ff
                                                        4
e0 Oc d6 fe ff ff ff ff 3c 0e d6 fe ff
ec e3 e0 fe ff ff ff ff 60 96 d4 fe ff ff ff ff
f8 fa e0 fe ff ff ff ff 9c fd e0 fe ff ff ff ff
cc 0f d6 fe ff ff ff ff
Header:
 Signature : RUNTSERV
 Revision : 2.31
 HeaderSize : 0x00000088
CRC32 : 0xCB42AA6F
 Reserved : 0x00000000
Runtime Services:
 GetTime
                           0xFFFFFFFFFEE02B2C
 SetTime
                           0xFFFFFFFFEE02CBC
 GetWakeupTime
                           0xFFFFFFFFFEE02E20
 SetWakeupTime
                          : 0xFFFFFFFFEE0300C
 SetVirtualAddressMap : 0x00000000DA6514DC
 ConvertPointer : 0x00000000DA651400
               : 0xFFFFFFFFED60B34
 GetVariable
 GetNextVariableName : 0xFFFFFFFFED60CE0
 SetVariable
                          : 0xFFFFFFFFED60E3C
 GetNextHighMonotonicCount: 0xFFFFFFFFEE0E3EC
 ResetSystem
                          : 0xFFFFFFFFED49660
 UpdateCapsule
                          : 0xFFFFFFFFEE0FAF8
 QueryCapsuleCapabilities : 0xFFFFFFFFEE0FD9C
 QueryVariableInfo
                          : 0xFFFFFFFFED60FCC
```

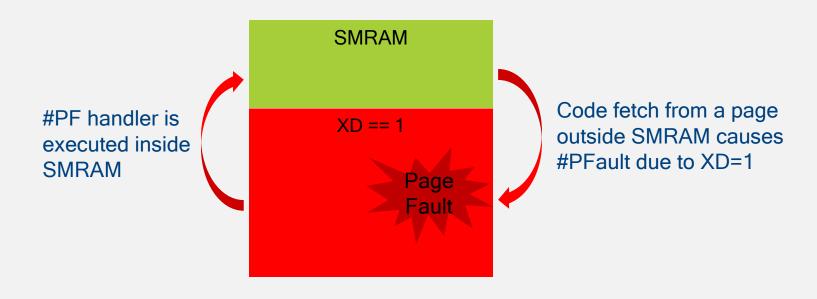
## BIOS developers can easily detect call-outs

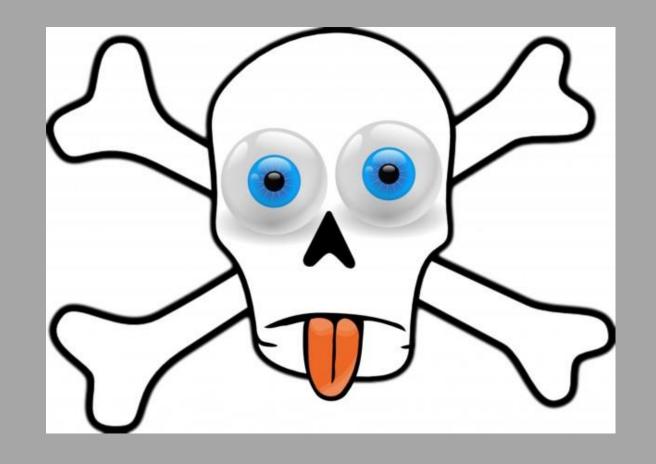
- 1. A "simple" ITP debugger script to step on branches and verify that target address of the branch is within SMRAM
- Enable SMM Code Access Check HW feature on preproduction systems based on newer CPUs to weed out all "intended" code fetches outside of SMRAM from SMI drivers
- 3. NX based soft SMM Code Access Check patches by Phoenix look promising

# Using Paging to detect SMM call-outs

#### NX based soft SMM Code Access Check patches by Phoenix

- SMM paging/NX are enabled when CPU enters SMM
- PTEs outside of SMRAM have XD=1
- #PF is signaled when SMI handler attempts to fetch from any page outside of SMRAM





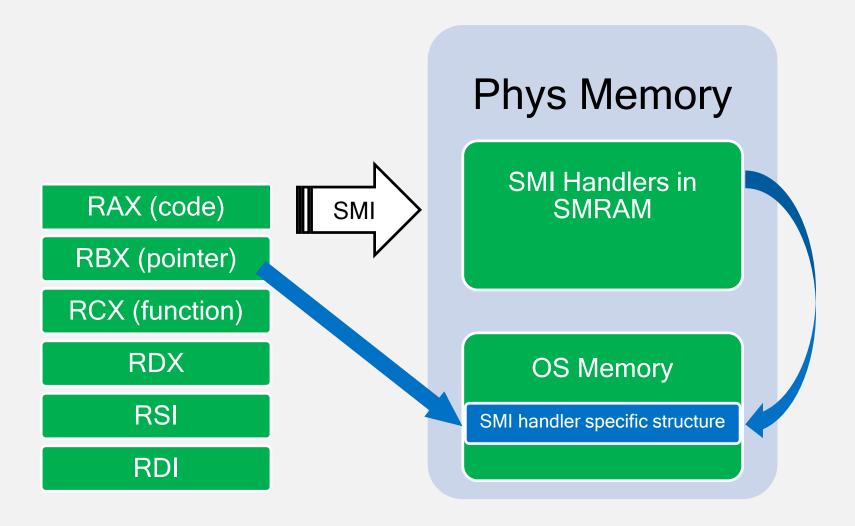
4.6 (2) Attacking SMI Handlers: SMI Input Pointers

# **SMI Input Pointer Vulnerabilities**

- When OS triggers SMI (e.g. SW SMI via I/O port 0xB2) it passes arguments to SMI handler via general purpose registers
- OS may also pass an address (pointer) to a structure through which an SMI handler can read arguments & returns result
- SMI handlers traditionally were not validating that such pointers are outside of SMRAM
- If an exploit passes an address which is inside SMRAM,
   SMI handler may write onto itself on behalf of the exploit

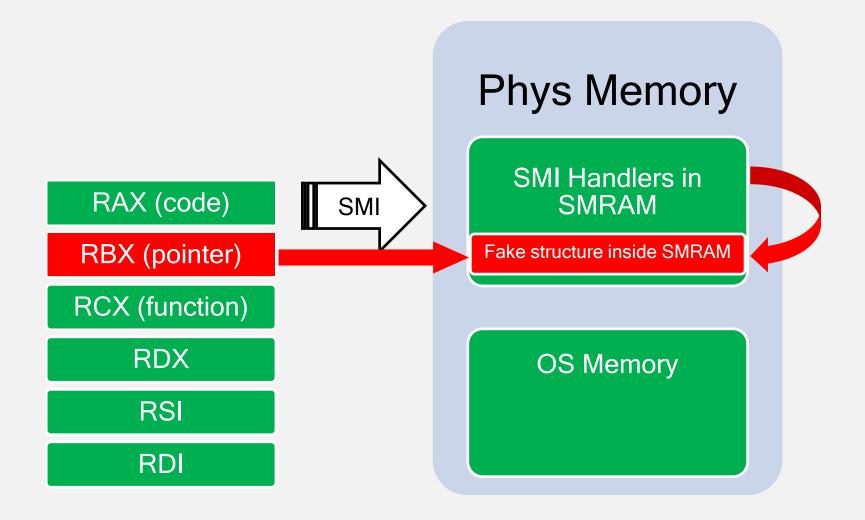
References: A New Class of Vulnerability in SMI Handlers

# Pointer Arguments to SMI Handlers



SMI Handler writes result to a buffer at address passed in RBX...

#### **Pointer Vulnerabilities**



Exploit tricks SMI handler to write to an address inside SMRAM

### What can exploit overwrite in SMRAM?

- Depending on the vulnerability, caller may control address to write, the value written, or both.
- Often the caller controls the address (and knows offset off of the address) but doesn't completely control the values written to the address by the SMI handler
- What can an exploit overwrite in SMRAM without crashing?
  - SMI entry point at SMBASE + 8000h
  - Internal SMI handler's state/flags inside SMRAM
  - Contents of SMM state save area (registers)
- Current value of SMBASE MSR is also saved in SMM state save at SMBASE + FEF8h area by CPU upon SMI
- Saved value of SMBASE is restored upon executing RSM
- Exploit can relocate SMRAM! Overwrite saved SMBASE to relocate SMRAM to unprotected memory location on next SMI

### How does exploit know where to write?

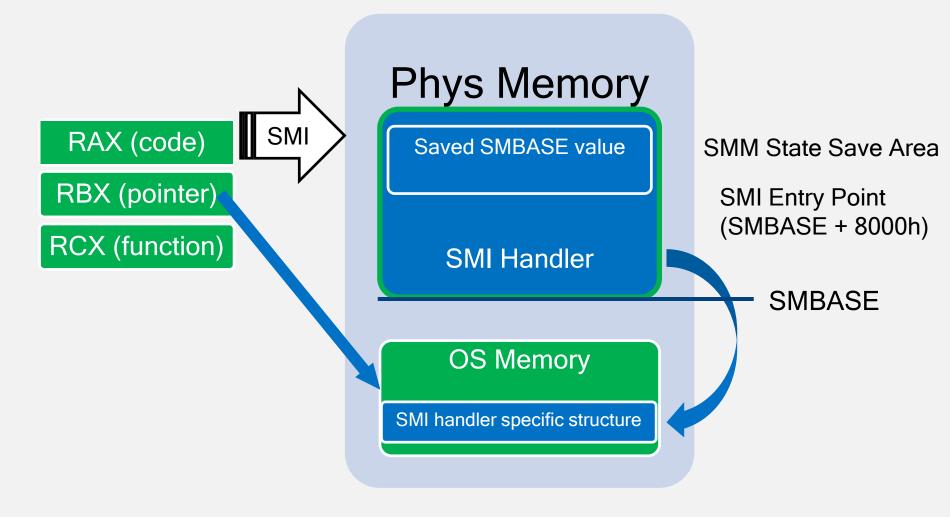
#### Exploit needs to know location of saved SMBASE

#### Dump contents of SMRAM

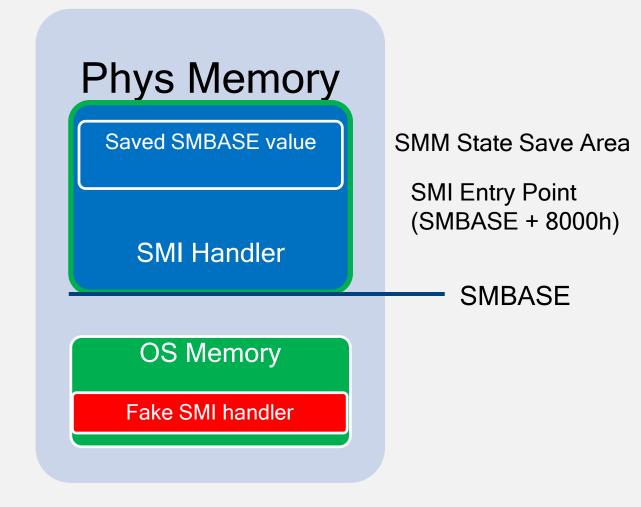
- Use another vulnerability (e.g. S3 boot script) to disable SMRAM protections and use DMA or graphics to read SMRAM
- Dump SPI flash contents, extract DXE SMM binaries and find SMRAM Init there
- Use similar SMI pointer read/write vulnerability
- Use hardware ITP offline

#### 2. Find SMM state save area for each logical CPU

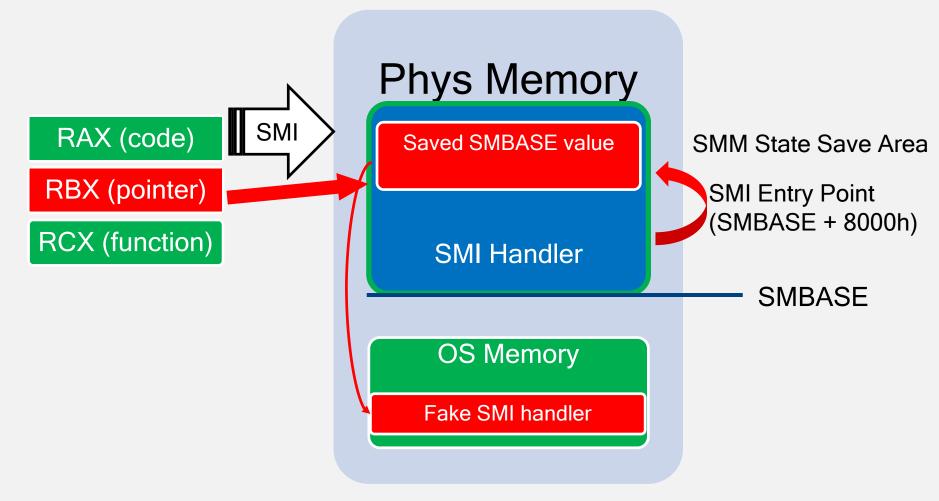
- SMM state save is at SMBASE + FC00h but SMBASE is different per CPU thread and per BIOS and some offset of TSEG/SMRR base
- Find SMI entry point (@ SMBASE + 8000h)
- Exploit can guess several locations of SMBASE (SMRR\_PHYSBASE = SMBASE or SMM entry point, blind iteration through all offsets within SMRAM as potential saved SMBASE value)
- Or exploit can invoke SMI handler with known values in GPRs, then find where they are saved in SMRAM



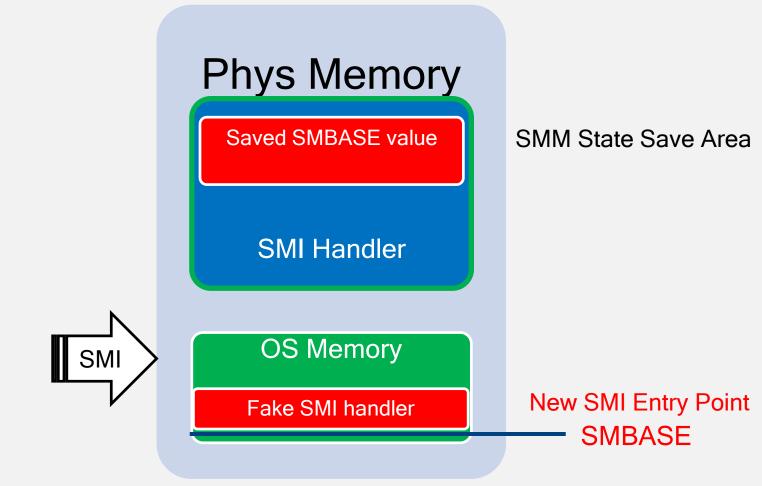
 CPU stores current value of SMBASE in SMM save state area on SMI and restores it on RSM



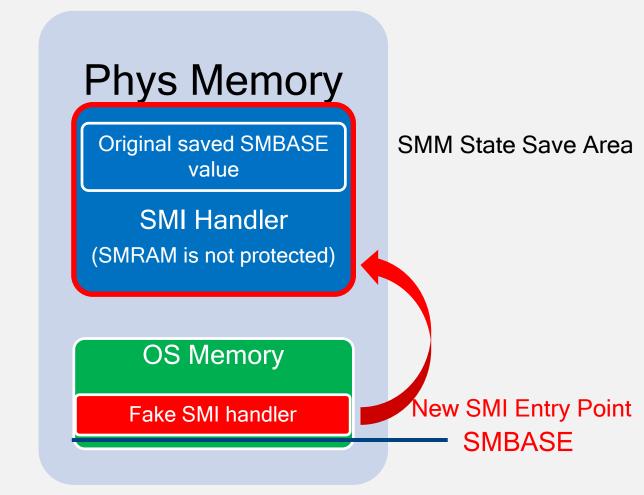
Exploit prepares fake SMRAM with fake SMI handler outside of SMRAM



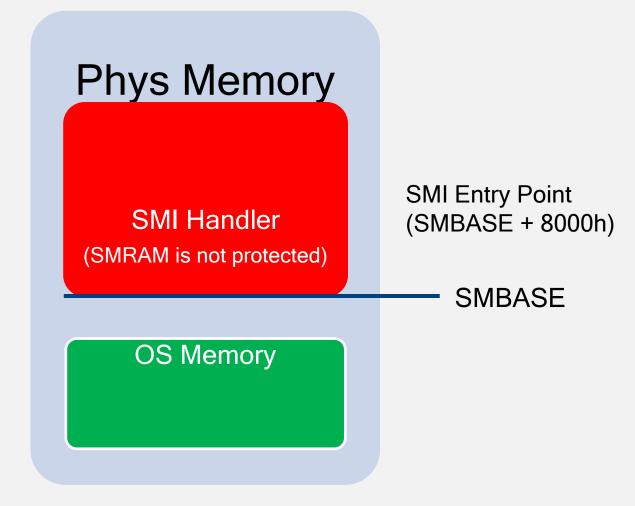
- Exploit triggers SMI w/ RBX pointing to saved SMBASE address in SMRAM
- SMI handler overwrites saved SMBASE on exploit's behalf with address of fake SMI handler outside of SMRAM (e.g. 0 PA)



- Exploit triggers another SMI
- CPU executes fake SMI handler at new entry point outside of original protected SMRAM because SMBASE location changed



- Fake SMI handler disables original SMRAM protection (disables SMRR)
- Then restores original SMBASE values to switch back to original SMRAM



- The SMRAM is restored but not protected by HW anymore
- Any SMI handler may be installed/modified by malware

```
[+] loaded chipsec.modules.poc.smm.smi pointer
[*] running loaded modules ...
[*] running module: chipsec.modules.poc.smm.smi pointer
[*] Module path: C:\chipsec\source\tool\chipsec\modules\poc\smm\smi pointer.pyc
[*] Original SMRAM memory dump:
[*] Bypass SMRAM protection via SMI pointer vulnerability:
   [1] -> Save original OS code/data at future SMBASE
   [2] -> Prepare custom SMI handler at future SMBASE
   [3] -> Trigger SMI with malformed pointer to modify SMBASE field in SMRAM
   [4] -> Trigger SMI to execute custom SMI handler to disable SMRAM protection and restore SMBASE
   [5] -> Restore original OS code/data
[+] Done: SMRAM is open for R/W access from OS kernel
[*] SMRAM memory dump:
DA000000: eb 52 8b ff 00 00 00 00 | be 01 00 00 ba 01 00 00
DA000010: b2 01 00 00 a2 01 00 00
                          be 01 00 00 d3 01 00 00
DA000020: ff ff ff ff 00 00 00 da | 00 00 00 00 d0 1a 02 da
DA000030: 00 00 00 00 00 8c 01 da | 00 00 00 00 00 cc 00 da
[*] Checking SMRAM is writeable..
[*] Modified SMRAM memory dump:
DA000000: Of aa 8b ff 00 00 00 00 | be 01 00 00 ba 01 00 00
                          be 01 00 00 d3 01 00 00
DA000010: b2 01 00 00 a2 01 00 00
DA000020: ff ff ff ff 00 00 00 da | 00 00 00 00 d0 1a 02 da
DA000030: 00 00 00 00 00 8c 01 da | 00 00 00 00 00 cc 00 da
```

# Input Pointers in EDKII: CommBuffer

- CommBuffer is a memory buffer used as a communication protocol between OS runtime and DXE SMI handlers
- Pointer to CommBuffer is stored in "UEFI" ACPI table in ACPI NVS memory accessible to OS
- Contents of CommBuffer are specific to SMI handler. Variable SMI handler read UEFI variable GUID, Name and Data from CommBuffer

Vulnerability	Ref	Affected	Reported by
CommBuffer SMM Overwrite/Exposure (3 issues)	<u>Tianocore</u>	EDK2	Intel ATR
TOCTOU (race condition) Issue with CommBuffer (2 issues)	<u>Tianocore</u>	EDK2	Intel ATR
SMRAM Overwrite in Fault Tolerant Write SMI Handler (2 issues)	<u>Tianocore</u>	EDK2	Intel ATR
SMRAM Overwrite in SmmVariableHandler (2 issues)	<u>Tianocore</u>	EDK2	Intel ATR

## Attacking CommBuffer Pointer

#### SecurityPkg/VariableAuthenticated/RuntimeDxe:

```
SmmVariableHandler (
  SmmVariableFunctionHeader = (SMM VARIABLE COMMUNICATE HEADER *) CommBuffer;
  switch (SmmVariableFunctionHeader->Function) {
    case SMM VARIABLE FUNCTION GET VARIABLE:
      SmmVariableHeader = (SMM VARIABLE COMMUNICATE ACCESS VARIABLE *)
                          SmmVariableFunctionHeader->Data;
      Status = VariableServiceGetVariable (
                 (UINT8 *) SmmVariableHeader->Name + SmmVariableHeader->NameSize
                 );
VariableServiceGetVariable (
          VOID
  OUT
                            *Data
  CopyMem (Data, GetVariableDataPtr (Variable.CurrPtr), VarDataSize);
```

CommBuffer

**SMRAM** 

# Mitigating CommBuffer Attack

- SMI Handlers often have multiple commands, calling a different function for each command and take command specific arguments
- Note the calls to SmmIsBufferOutsideSmmValid. This checks for addresses to overlap with SMRAM range

```
SmiHandler() {
  // check CommBuffer is outside SMRAM
  if (!SmmIsBufferOutsideSmmValid(CommBuffer, Size)) {
    return EFI SUCCESS;
  switch (command)
    case 1: do command1(CommBuffer);
    case 2: do command2(CommBuffer);
```

CommBuffer

**SMRAM** 

### CommBuffer TOCTOU Issues

- SMI handler checks that it won't access outside of CommBuffer
- What if SMI handler reads CommBuffer memory again after the check
- DMA engine (for example GFx) can modify contents of CommBuffer

Time of Check

## Validate input addresses before using them!

- Read pointer issues are also exploitable to expose SMRAM contents
- SMI handlers have to validate each address/pointer (+ offsets) they receive from OS prior to reading from or writing to it including returning status/error codes
  - E.g. use/implement a function which validates address + size for overlap with SMRAM similar to SmmIsBufferOutsideSmmValid in EDKII

### Exercise 4.3

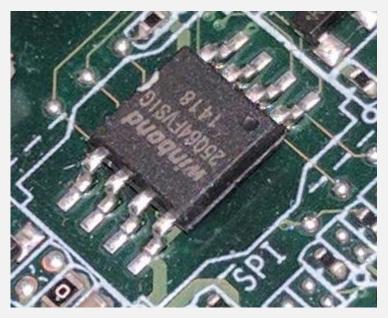
Security of SMI Handler Firmware

### Exercise 4.4

**Attacking SMI Handlers** 

# 4.7 Attacking UEFI Variables

## Where does firmware store its settings?



- UEFI BIOS stores persistent config as "UEFI Variables" in NVRAM part of SPI Flash chip
- UEFI Variables can be Boot-time or Run-time
- Run-time UEFI Variables are accessible by OS via run-time Variable API (via SMI Handler)
- OS exposes UEFI Variable API to [privileged] user-mode applications

SetFirmwareEnvironmentVariable

/sys/firmware/efi/efivars/ Or
/sys/firmware/efi/vars

# Lots of settings..

UsbSupport\_EC87D643-EBA4-4BB5-A1E5-3F3E36B20DA9\_NV+BS+RT\_0

↑ Name	Ext	Size	
AcpiGlobalVariable_C020489E-6DB2-4EF2-9AA5-CA06FC11D36A_NV+BS+RT_1	bin	8	
MITSESetup C811FA38-42C8-4579-A9BB-60E94EDDFB34 NV+BS+RT 0	bin	Q1	
Boot0000_8BE4DF61-93CA-11D2-AA0D-00E098032B8C_NV+BS+RT_0	bin	136	
Boot0001_8BE4DF61-93CA-11D2-AA0D-00E098032B8C_NV+BS+RT_0	bin	300	A 'OLL D' ' LL
BootCurrent_8BE4DF61-93CA-11D2-AA0D-00E098032B8C_BS+RT_0	bin	2	AcpiGlobalVariable
BootOptionSupport 8BE4DF61-93CA-11D2-AA0D-00E098032B8C BS+RT 0	bin	4	
BootOrder_8BE4DF61-93CA-11D2-AA0D-00E098032B8C_NV+BS+RT_0	bin	10	
☐ db_D719B2CB-3D3A-4596-A3BC-DAD00E67656F_NV+BS+RT+TBAWS_0	Lin	3,143	
□ dbx_D719B2CB-3D3A-4596-A3BC-DAD00E67656F_NV+BS+RT+TBAWS_0	bin	70	
DimmSPDdata_A09A3266-0D9D-476A-B8EE-0C226BE16644_NV+BS+RT_0	bin	8	
DmiData_70E56C5E-280C-44B0-A497-09681ABC375E_NV+BS+RT_0	bin	397	D 10 1
FastBootOption_B540A530-6978-4DA7-91CB-7207D764D262_NV+BS+RT_0	bin	284	BootOrder
FlashInfoStructure_82FD6BD8-02CE-419D-BEF0-C47C2F123523_NV+BS+RT_0	bin	7	
Guid1394_F9861214-9260-47E1-BCBB-52AC033E7ED8_NV+BS+RT_0	bin	8	
KEK_8BE4DF61-93CA-11D2-AA0D-00E098032B8C_NV+BS+RT+TBAWS_0	bin	1,560	
LastBoot_B540A530-6978-4DA7-91CB-7207D764D262_NV+BS+RT_0	bin	10	
LegacyDevOrder_A56074D8-65FE-45F7-BD21-2D2BDD8E9652_NV+BS+RT_0	bin	16	Secure Boot
MaintenanceSetup_EC87D643-EBA4-4BB5-A1E5-3F3E36B20DA9_NV+BS+RT_(	) bin	410	Secure Door
MEFWVersion_9B875AAC-36EC-4550-A4AE-86C84E96767E_NV+BS+RT_0	bin	20	certificates
MemorySize_6F20F7C8-E5EF-4F21-8D19-EDC5F0C496AE_NV+BS+RT_0	bin	8	
MemoryTypeInformation_4C19049F-4137-4DD3-9C10-8B97A83FFDFA_NV+BS+F	RT_0 bin	64	(PK, KEK, db, dbx)
MrcS3Resume_87F22DCB-7304-4105-BB7C-317143CCC23B_NV+BS+RT_0	bin	4,052	
NBPlatformData_EC87D643-EBA4-4BB5-A1E5-3F3E36B20DA9_BS+RT_0	bin	14	
OsIndications_8BE4DF61-93CA-11D2-AA0D-00E098032B8C_NV+BS+RT_0	bin	8	
OsIndicationsSupported_8BE4DF61-93CA-11D2-AA0D-00E098032B			
PasswordInfo_6320A8C8-9C93-4A71-B529-9F79C8761B8D_NV+BS			LODG D LDGGGGGGGG MIL DG DT TDLLIG G L' E L
I CHOST CHILLOCK FOR DOOT TOTAL COURT THE DOSTITION			A3BC-DAD00E67656F_NV+BS+RT+TBAWS_0.bin.dir]
			G-A3BC-DAD00E67656F_NV+BS+RT+TBAWS_0.bin.dir
PKDefault_8BE4DF61-93CA-11D2-AA0D-00E098032B8C_NV+BS+R 🗀 [KEK_8]	BBE 4DF61	-93CA-11D	2-AA0D-00E098032B8C_NV+BS+RT+TBAWS_0.bin.dii
SecureBoot_8BE4DF61-93CA-11D2-AA0D-00E098032B8C_BS+RT_ [ [PK_8E	3E4DF61-	93CA-11D2	-AAOD-00E098032B8C_NV+BS+RT+TBAWS_0.bin.dir]
SecurityTokens_6320A8C8-9C93-4A71-B529-9F79C8761B8D_NV+B[SecurityTokens_6320A8C8-9C93-4A71-B529-9F79C8761B8D_NV+B	eBoot 8B	E4DF61-93	CA-11D2-AA0D-00E098032B8C_BS+RT_0.bin.dir]
□ C . CCC7DC43 CD44 4DDC 44CC 3C3C3CD3CD40 NV DC DT C	_		CA-11D2-AA0D-00E098032B8C_BS+RT_0.bin.dir]
SetupDefault_EC87D643-EBA4-4BB5-A1E5-3F3E36B20DA9_NV+BS+n1_0	DILI	410	A 1102 And 00000000000000000000000000000000000
SetupMode_8BE4DF61-93CA-11D2-AA0D-00E098032B8C_BS+RT_0	bin	1	
SetupPlatformData_EC87D643-EBA4-4BB5-A1E5-3F3E36B20DA9_BS+RT_0	bin	16	
SignatureSupport_8BE4DF61-93CA-11D2-AA0D-00E098032B8C_BS+RT_0	bin	80	Setup
TpmDeviceSelectionUpdate_EC87D643-EBA4-4BB5-A1E5-3F3E36B20DA9_NV+	BS bin	1	Octup
TrEEPhysicalPresence_F24643C2-C622-494E-8A0D-4632579C2D5B_NV+BS+R1	T_O bin	12	

32<sub>A...</sub>

bin

## **Dangerous Contents in UEFI Variables**

- Secure Boot configuration settings (see our All Your Boot Are Belong To Us)
- Addresses to structures/buffers which firmware reads from or writes to during boot
- Policies for hardware protections & locks such as BIOS Write Protection, Flash LockDown, BIOS Interface Lock
- Policies disabling security features
- Values of hardware configuration registers which firmware locks down
- Data which firmware really really needs to just boot
- Secrets: BIOS passwords in clear

# This cannot be good...

- Overwrite early firmware code/data if (physical addresses) pointers are stored in unprotected variables
- Bypass UEFI and OS Secure Boot if its configuration or keys are stored in unprotected variables
- Bypass or disable hardware protections if their policies are stored in unprotected variables
- Make the system unable to boot (brick) if setting essential to boot the system are stored in unprotected variables

## Who needs a Setup variable, anyway?

#### VU#758382

- Storing Secure Boot settings in Setup could be bad
- Now user-mode malware can clobber contents of Setup UEFI variable with garbage or delete it
- Malware may also clobber/delete default configuration StdDefaults
- The system may never boot again

The attack has been co-discovered with researchers from LegbaCore (Corey Kallenberg, Xeno Kovah) and MITRE Corporation (Sam Cornwell, John Butterworth).

Source: Setup For Failure

### Variable Attribute Checks in CHIPSEC

# chipsec\_main.py --module common.uefi.access\_uefispec

```
[*] running module: chipsec.modules.common.uefi.access uefispec
[x] [ Module: Access Control of Variables Defined in UEFI Spec
[*] Testing UEFI variables ..
[*] Variable BootOrder
[*] Variable dbx
[*] Variable ConOut
[*] Variable db
[*] Variable PK
[*] Variable BootCurrent
[*] Variable Timeout
[*] Variable KEK
[*] Variable Boot0000
[*] Variable Boot0001
[*] Variable SecureBoot
[*] Variable ConIn
```

[+] PASSED: All checked UEFI spec variables are protected according to spec

### Exercise 4.5

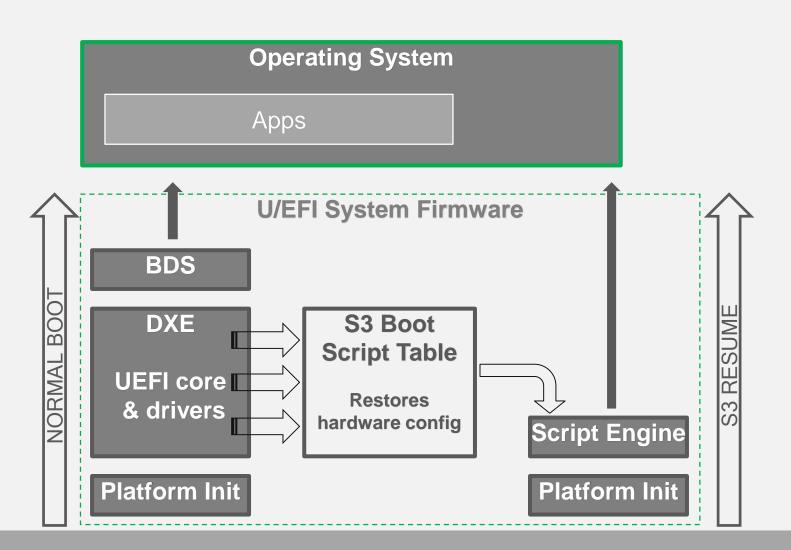
Security of UEFI Variables

# 4.8 Attacking Firmware S3 Resume

# VU# 976132 (CVE-2014-8274)

- Security issues in system firmware due to handling of S3 resume boot script have been independently discovered by other security researchers
- Rafal Wojtczuk of Bromium and Corey Kallenberg
   (@coreykal) of LegbaCore first published <u>Attacks on UEFI</u>
   <u>Security</u> (paper)
- PoC exploit was described and developed by Dmytro Oleksiuk (@d\_olex) in <u>Exploiting UEFI boot script table</u> <u>vulnerability</u>
- Pedro Vilaça (@osxreverser) found related <u>vulnerability</u> in Mac EFI firmware (SPI Flash Configuration HW lock bit FLOCKDN is gone after resuming from S3)

#### Waking the system from S3 "sleep" state



# Searching for ACPI global structure...

AcpiGlobalVariable UEFI variable points to a structure in memory (ACPI VARIABLE SET COMPATIBILITY)

```
[CHIPSEC] Reading EFI variable Name='AcpiGlobalVariable'.. [uefi] EFI variable AF9FFD67-EC10-488A-9DFC-6CBF5EE22C2E:AcpiGlobalVariable:
```

18 be 89 da

# Searching for "S3 Boot Script"...

Pointer AcpiBootScriptTable at offset 0x18 in the structure ACPI\_VARIABLE\_SET\_COMPATIBILITY points to the script table

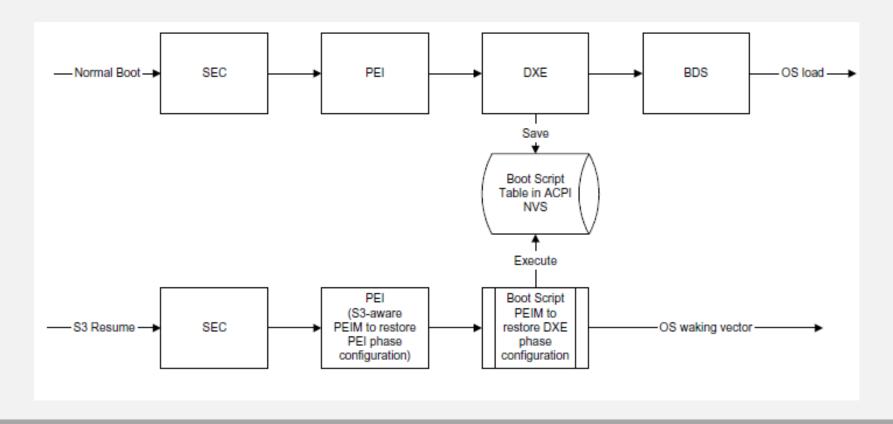
```
typedef struct {
//
// Acpi Related variables
//
EFI_PHYSICAL_ADDRESS AcpiReservedMemoryBase;
UINT32 AcpiReservedMemorySize;
EFI_PHYSICAL_ADDRESS S3ReservedLowMemoryBase;
EFI_PHYSICAL_ADDRESS AcpiBootScriptTable;
...
} ACPI_VARIABLE_SET_COMPATIBILITY;
```

# "S3 Boot Script" table in memory

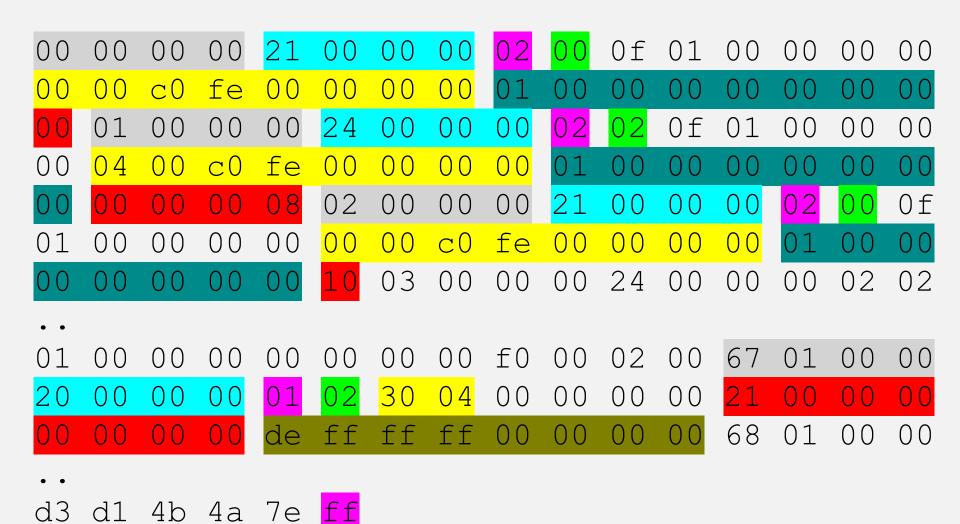
```
[CHIPSEC] Reading: PA = 0x00000000DA88A018, len = 0x100, output:
00 00 00 00 21 00 00 00 02 00 0f 01 00 00 00 00
00 00 c0 fe 00 00 00 00 01 00 00 00 00 00 00
00 01 00 00 00 24 00 00 00 02 02 0f 01 00 00
00 04 00 c0 fe 00 00 00 00 01 00 00 00 00 00
00 00 00 00 08 02 00 00 00 21 00 00 00 02 00 0f
01 00 00 00 00 00 00 c0 fe 00 00 00 00 01 00
  00 00 00 00 10 03 00 00 00 24 00 00 00 02 02
0f 01 00 00 00 00 04 00 c0 fe 00 00 00 00 01 00
     00 00 00 00 00 07 00 00 04 00 00 00 24 00
     02 02 07 07 07 07 07 07 04 f4 d1 fe 00 00
00 00 01 00 00 00 00 00 00 00 80 00 00 00 05 00
00 00 28 00 00 00 03 02 00 00 00 00 00 00 14 90
d1 fe 00 00 00 00 00 00 00 00 00 00 00 00 01 00
     00 00 00 00 06 00 00 00 28 00 00 00 03
00 00 00 00 00 00 04 90 d1 fe 00 00 00 00 01 00
00 00 00 00 00 00 f8 00 00 00 00 00 00 00 07 00
```

# Why "S3 Resume Boot Script"?

To speed up S3 resume, required HW configuration actions are written to an "S3 Resume Boot Script" by DXE drivers instead of running all configuration actions normally performed during boot



# S3 Boot Script is a Sequence of Platform Dependent Opcodes



# **Decoding Opcodes**

```
[000] Entry at offset 0x0000 (length = 0x21):
Data:
02 00 0f 01 00 00 00 00 00 c0 fe 00 00 00
01 00 00 00 00 00 00 00 00
Decoded:
  Opcode: S3 BOOTSCRIPT MEM WRITE (0x02)
 Width: 0x00 (1 bytes)
 Address: 0xFEC00000
 Count : 0x1
 Values: 0 \times 00
. .
[359] Entry at offset 0x2F2C (length = 0x20):
Data:
01 02 30 04 00 00 00 00 21 00 00 00 00 00 00
de ff ff ff 00 00 00 00
Decoded:
  Opcode: S3 BOOTSCRIPT IO READ WRITE (0x01)
 Width: 0x02 (4 bytes)
 Address: 0x00000430
 Value : 0x00000021
 Mask : OxffffffbE
```

# chipsec\_util.py uefi s3bootscript

# **S3 Boot Script Opcodes**

- I/O port write (0x00)
- I/O port read-modify-write (0x01)
- Memory write (0x02)
- Memory read-modify-write (0x03)
- PCIe configuration write (0x04)
- PCIe configuration read-modify-write (0x05)
- SMBus execute (0x06)
- Stall (0x07)
- Dispatch (0x08)
- Dispatch2

## **Processor I/O Port Opcodes**

S3\_BOOTSCRIPT\_IO\_WRITE/READ\_WRITE opcodes in the S3 boot script write or RMW to processor I/O ports

Opcode below sends SW SMI by writing value 0xBD port 0xB2

```
D:\source\tool\s3bootscript.log
[360] Entry at offset 0x2F4C (len = 0x19, header len = 0x8):
Data:
0
lbd
Decoded:
 Opcode: S3_BOOTSCRIPT_IO_WRITE (0x00)
 Width : 0x00 (1 bytes)
 Address: 0x000000B2
 Count: 0x1
 Values : 0xBD
```

## "Dispatch" Opcodes

**S3\_BOOTSCRIPT\_DISPATCH/2** opcodes in the S3 boot script jumps to entry-point defined in the opcode

#### **Opcode Restoring BIOS Write Protection**

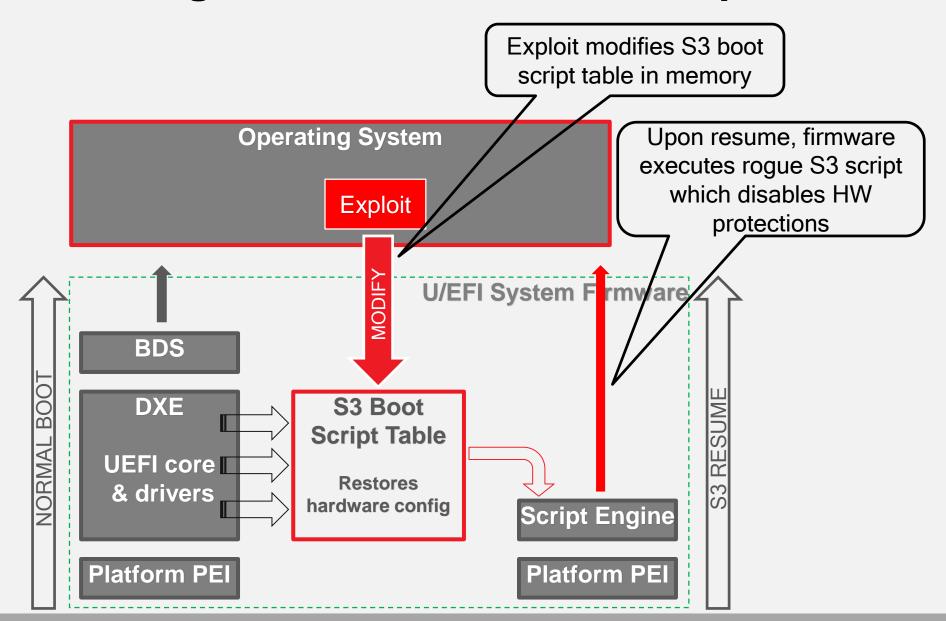
**S3\_BOOTSCRIPT\_PCI\_CONFIG\_WRITE** opcode in the S3 boot script restores BIOS hardware write-protection (value 0x2A means BIOS hardware write protection is ON)

```
edit s3bootscript.log - Far 3.0
D:\source\tool\s3bootscript.log
                                                            28595
[569] Entry at offset 0x4BFB (len = 0x21, header len = 0x8):
Data:
04 00 00 00 00 00 00 00 dc 00 1f 00 00 00 00 00
01 00 00 00 00 00 00 00 08
Decoded:
  Opcode: S3_BOOTSCRIPT_PCI_CONFIG_WRITE (0x04)
  Width: 0x00 (1 bytes)
  Address: 0x001F00DC
  Count : 0x1
  Values : 0x2A
```

# Things that can go wrong

- Address (pointer) to S3 boot script is stored in a runtime UEFI variable (e.g. NV+RT+BS AcpiGlobalTable)
- The S3 boot script itself is stored in unprotected memory (ACPI NVS) accessible to the OS or DMA capable devices
- The PEI executable parsing and interpreting the S3 boot script or any other executable needed for S3 resume is running out of unprotected memory
- S3 boot script contains Dispatch (Dispatch2) opcodes with entry-points in unprotected memory
- EFI firmware "forgets" to store opcodes which restore all required hardware locks and protections in S3 boot script

#### Attacking FW on resume from sleep



# Lucky you! BIOS protection is ON

```
[x][ Module: BIOS Region Write Protection
[*] BC = 0x2A << BIOS Control (b:d.f 00:31.0 + 0xDC)
    [00] BIOSWE
                         = 0 << BIOS Write Enable
    [01] BLE
                         = 1 << BIOS Lock Enable
    [02] SRC
                         = 2 << SPI Read Configuration
    [04] TSS
                       = 0 << Top Swap Status
    [05] SMM BWP
                         = 1 << SMM BIOS Write Protection
[+] BIOS region write protection is enabled (writes restricted to SMM)
[*] BIOS Region: Base = 0x00200000, Limi
                                         PASSED: BIOS is write
SPI Protected Ranges
                                                  protected
PRx (offset) | Value | Base
                                   Limic
                                   0000000
              00000000 00000000
PRØ (74)
                                   000000
PR1 (78)
              00000000 | 00000000
PR2 (7C)
              00000000
                         00000000
                                   00000
PR3 (80)
              00000000
                         00000000
                                   0000
PR4 (84)
                                   00r
              00000000
                         00000000
[!] None of the SPI protected ranges //ite-protect BIOS region
[+] PASSED: BIOS is write protected
```

## Sleep well

```
Found Boot Script in
    Module: S3 Resume Boot-Script Testing
                                                        unprotected memory
[helper] -> NtEnumerateSystemEnvironmentValuesEx( inf
[uefi] searching for EFI variable(s): ['AcpiGlobalVariable/
[uefi] found: 'AcpiGlobalVariable' {AF9FFD67-EC10-488A-9D/
                                                            r5EE22C2E} NV+BS+RT variable
[uefi] Pointer to ACPI Global Data structure: 0x00000000
                                                         ∍BE18
[uefi] Decoding ACPI Global Data structure
[uefi] ACPI Boot-Script table base = 0x00000000DA88A018
[uefi] Found 1 S3 resume boot-scripts
[uefi] 53 resume boot-script at ขxขบบบบบบบคxxAv18
[uefi] Decoding S3 Resume Boot-Script..
                                                      Script Opcode restores
[uefi] S3 Resume Boot-Script size: 0x5776
[*] Looking for 0x4 opcodes in the script at 0x000000
                                                      BIOS Protection == ON
+1 Found opcode at offset 0x4BFB
 Opcode : S3 BOOTSCRIPT PCI CONFIG WRITE (0x04)
 Width: 0x00 (1 bytes)
 Address: 0x001F00DC
 Count: 0x1
                                                             Changing it to OFF
 Values : 0x2A
   Modifying register value at address 0x00000000DA88EC33
   Original value: 0x2A
   Modified value: 0x9
   After sleep/resume, check the value of PCI config register 0x001F00DC is 0x9
   PASSED: The script has been modified. Go to sleep...
```

#### Oh wait...

```
[x][ Module: BIOS Region Write Protection
[*] BC = 0x09 << BIOS Control (b:d.f 00:31.0 + 0xDC)
   [00] BIOSWE
                       = 1 << BIOS Write Enable
   [01] BLE
                       = 0 << BIOS Lock Enable
   [02] SRC = 2 << SPI Read Configuration
   [04] TSS
               = 0 << Top Swap Status
                 = 0 << SMM BIOS Write Protection
   [05] SMM BWP
[-] BIOS region write protection is disabled!
[*] BIOS Region: Base = 0x00200000, Limit =
                                            FAILED: BIOS is NOT
SPI Protected Ranges
                                             protected completely
PRx (offset) | Value
                      Base
                                Limit
             00000000
                        00000000
                                  00000000
PRØ (74)
PR1 (78)
             00000000
                       00000000
                                  00000000
PR2 (7C)
                                  00000000
            00000000
                       00000000
PR3 (80)
             00000000 | 00000000 |
                                  00000000
PR4 (84)
                                  00000000
             00000000
                        00000000
[!] None of the SPI protected ranges write-project BIOS region
[!] BIOS should enable all available SMM based write protection mechanisms or
   FAILED: BIOS is NOT protected completely
```

# Opcode restoring BIOS Write Protection has been modified

S3\_BOOTSCRIPT\_PCI\_CONFIG\_WRITE opcode in the S3 boot script restored BIOS hardware write-protection in OFF state

```
D:\source\tool\s3bootscript_afterS3.log
                                                           28595
[569] Entry at offset 0x4BFB (len = 0x21, header len = 0x8):
Data:
04 00 00 00 00 00 00 00 dc 00 1f 00 00 00 00 00
01 00 00 00 00 00 00 00 09
Decoded:
 Opcode: S3_BOOTSCRIPT_PCI_CONFIG_WRITE (0x04)
 Width: 0x00 (1 bytes)
  Address: 0x001F00DC
 Values : 0x09
```

#### Checking with common.uefi.s3bootscript

# chipsec\_main.py -m common.uefi.s3bootscript

```
[x] [ Module: S3 Resume Boot-Script Protections
[!] Found 1 S3 boot-script(s) in EFI variables
[*] Checking S3 boot-script at 0x0000000DA88A018
[!] S3 boot-script is not in SMRAM
[*] Reading S3 boot-script from memory...
[*] Decoding S3 boot-script opcodes..
[*] Checking entry-points of Dispatch opcodes..
[-] Found Dispatch opcode (offset 0x014E) with Entry-Point:
0x0000000DA5C3260 : UNPROTECTED
[-] Entry-points of Dispatch opcodes in S3 boot-script are
not in protected memory
[-] FAILED: S3 Boot Script and entry-points of Dispatch
opcodes do not appear to be protected
```

#### Exercise 4.6

Security of Firmware S3 Resume

#### 4.9 Other Firmware Issues

# Pre-Boot Passwords Exposed in BIOS Keyboard Buffer

- BIOS and Pre-OS applications store keystrokes in legacy BIOS keyboard buffer in BIOS data area (at physical address 0x41E)
- BIOS, HDD passwords, Full-Disk Encryption PINs etc.
- Some BIOS'es didn't clear keyboard buffer

#### References:

**Bypassing Pre-Boot Authentication Passwords** 

### Checking with common.bios\_kbrd\_buffer

# chipsec\_main.py --module common.bios\_kbrd\_buffer

<sup>\*</sup> Better check from EFI shell as OS/pre-boot app might have cleared the keyboard buffer

# Training materials are available on Github <a href="https://github.com/advanced-threat-research/firmware-security-training">https://github.com/advanced-threat-research/firmware-security-training</a>

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