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Revision History

Revision	Date	Description
A	Dec. 2015	Initial release

Note: There is no Rev. I, O, Q, S, X, or Z per Mil. standards.

内容

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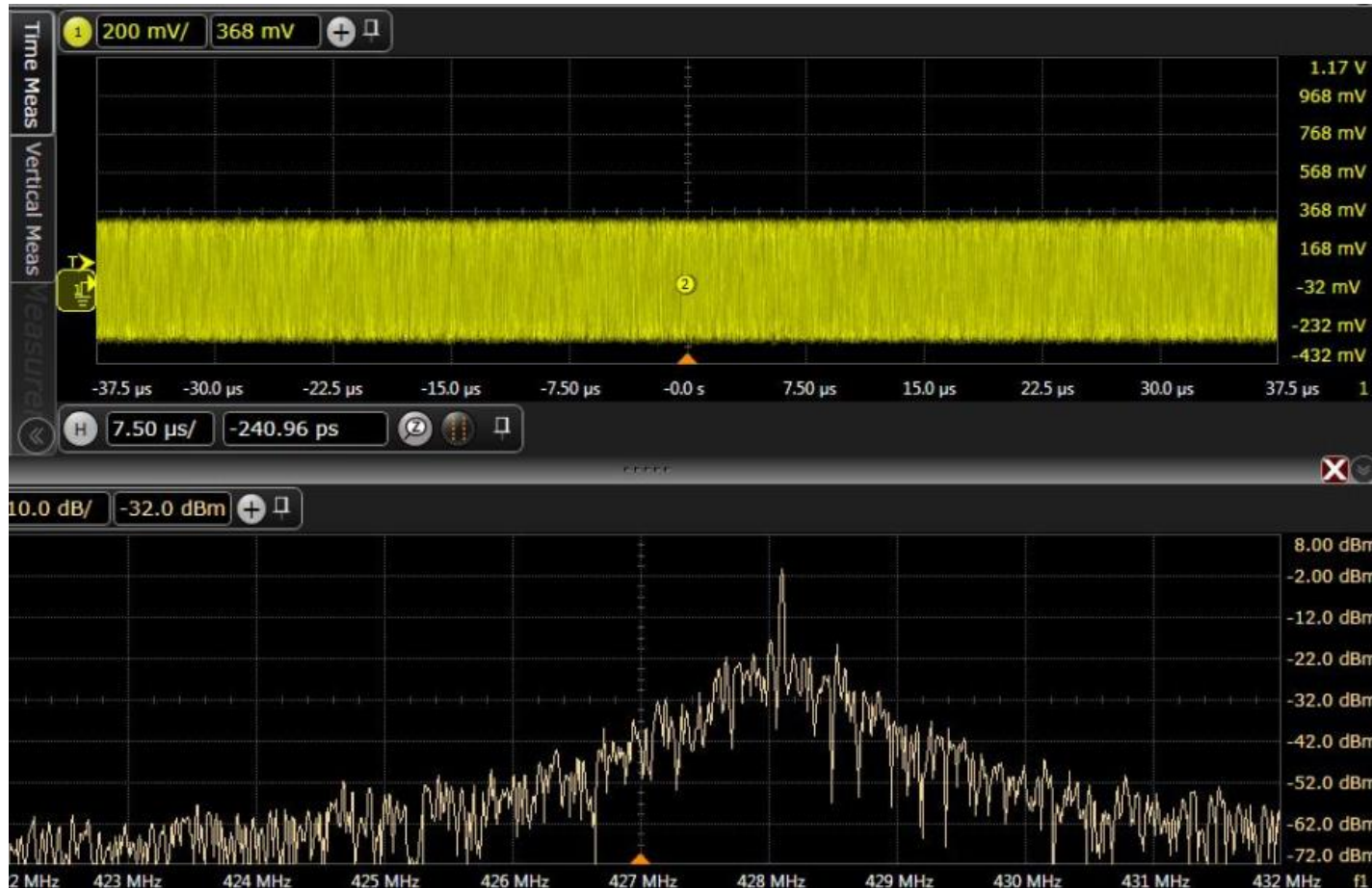
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Display

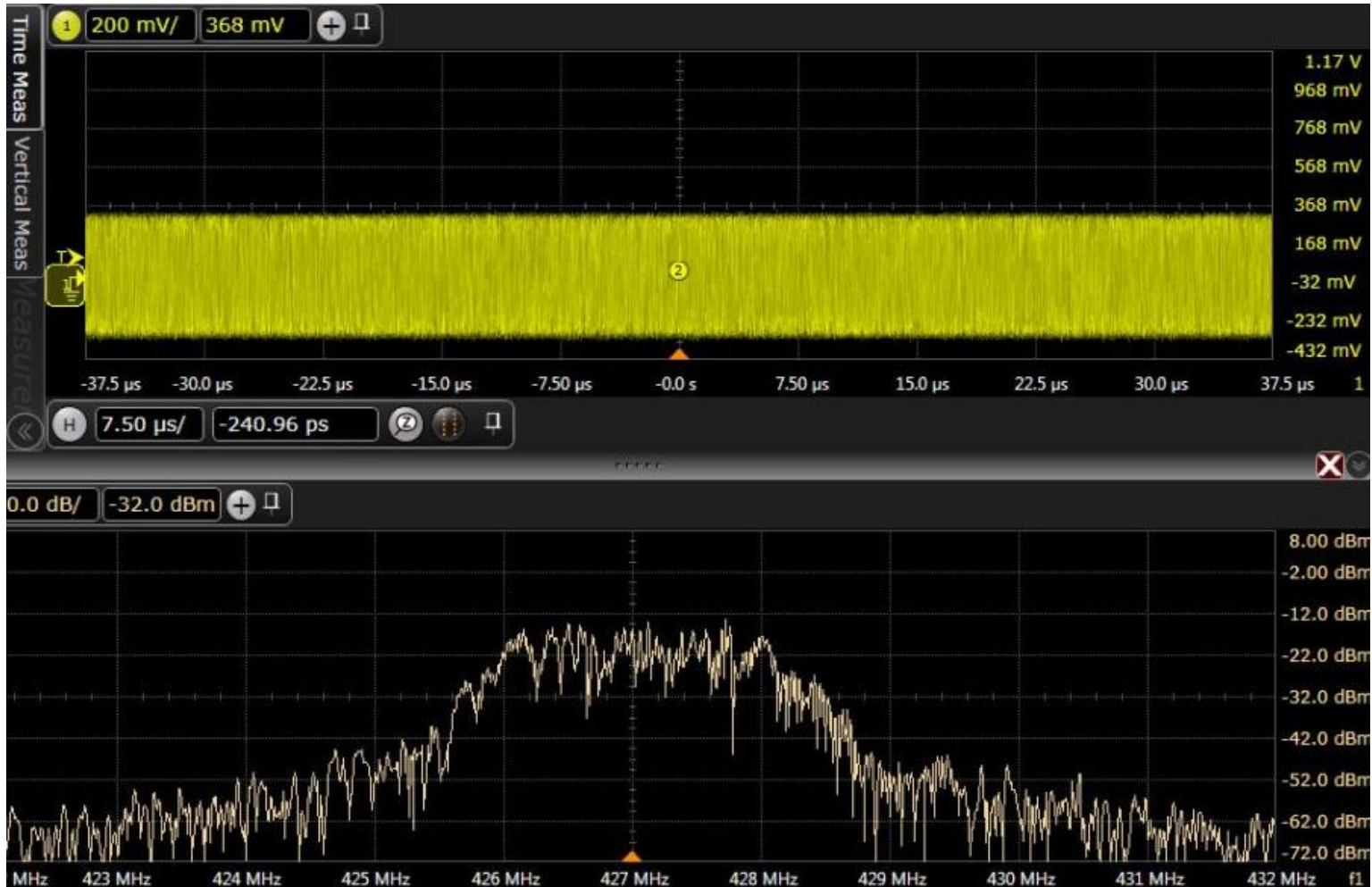
DSI PLL Spread Spectrum Clocking 功能 Overview

- EMI/RF-defense问题从根本上需要从硬件设计上避免，但少数情况下我们需要 enable DSI PLL SSC(Spread Spectrum Clocking), 去减弱EMI问题。
- 如右图所示为 没有使能 SSC的波形：



DSI PLL Spread Spectrum Clocking 功能 Overview – cont1

- 使能DSI PLL SSC后的波形如下：



DSI PLL Spread Spectrum Clocking 在不同Chipset 支持介绍

- SSC Support on
 - 8956/8976
 - 8996

- SSC **Not** Support on
 - 8x10/8x12
 - 8x26/8926/8x28/8928
 - 8974
 - 8909
 - 8916
 - 8936/8939/8929
 - 8952

SSC Feature Support on 8956/8976

- 在 /kernel/Documentation/devicetree/bindings/fb/mdss-pll.txt 中 ,
- qcom,ssc-spread-mode: A string that specifies the supported spread modes of SSC. 1.) "down" 2.) "center".
- 一般只需要在dts 文件中 添加如下改动 :
 - +&mdss_dsi0_pll {
 - + qcom,ssc-enable;
 - + qcom,ssc-frequency-hz = <30000>;
 - + qcom,ssc-ppm = <5000>;
 - + qcom,ssc-spread-mode = "down";
 - +};

SSC Feature Support on 8956/8976 – cont1

- 具体的CAF Link 如下：

1 : clk: qcom: mdss: add support for MDSS PLL Spread Spectrum

- <https://www.codeaurora.org/cgit/quic/la/kernel/msm-3.10/commit/?h=msm-3.10&id=5b2e006ccf98d9dabaf256530687956bca1a6045>

2 : clk: qcom: mdss: fix precision loss in VCO clock rate calculation

- <https://www.codeaurora.org/cgit/quic/la/kernel/msm-3.10/commit/?h=msm-3.10&id=cc12de2f3f84f1862ffd235370dd62e1432df65a>

3 : ARM: dts: msm: enable SSC for DSI PLL for msm8956/8976 v1.1

- <https://www.codeaurora.org/cgit/quic/la/kernel/msm-3.10/commit/?h=msm-3.10&id=69f553667c5975d7aa087dd342a9a88864d84b8b>

SSC Feature Support on 8996

- 在8996上，对于 Spread Spectrum Clocking 功能的支持，首先需要包括下面的link：
- msm: mdss: add support of dsi pll SSC for 8996
 - <https://www.codeaurora.org/cgit/quic/la/kernel/msm-3.18/commit/?h=msm-3.18&id=934b5daad2bf664dd1d496a3ae6d4bb5695f4b00>

SSC Feature Support on 8996 – cont1

- 然后，在msm8996-mdss-pll.dtsi 文件中，添加下面patch：

```
--- a/arch/arm/boot/dts/qcom/msm8996-mdss-pll.dtsi
+++ b/arch/arm/boot/dts/qcom/msm8996-mdss-pll.dtsi
@@ -27,6 +27,8 @@
+
+       clocks = <&clock_mmss clk_mdss_ahb_clk>;
+       clock-names = "iface_clk";
+       clock-rate = <0>;
+       qcom,dsi-pll-ssc-en;
+       qcom,dsi-pll-ssc-mode = "down-spread";
+
+       /* Memory region for passing dynamic refresh pll codes */
+       memory-region = <&dfps_data_mem>;
@@ -63,6 +65,8 @@
+
+       clocks = <&clock_mmss clk_mdss_ahb_clk>;
+       clock-names = "iface_clk";
+       clock-rate = <0>;
+       qcom,dsi-pll-ssc-en;
+       qcom,dsi-pll-ssc-mode = "down-spread";
+
+       qcom,platform-supply-entries {
+               #address-cells = <1>;
```

Questions?

<https://support.cdmatech.com>

