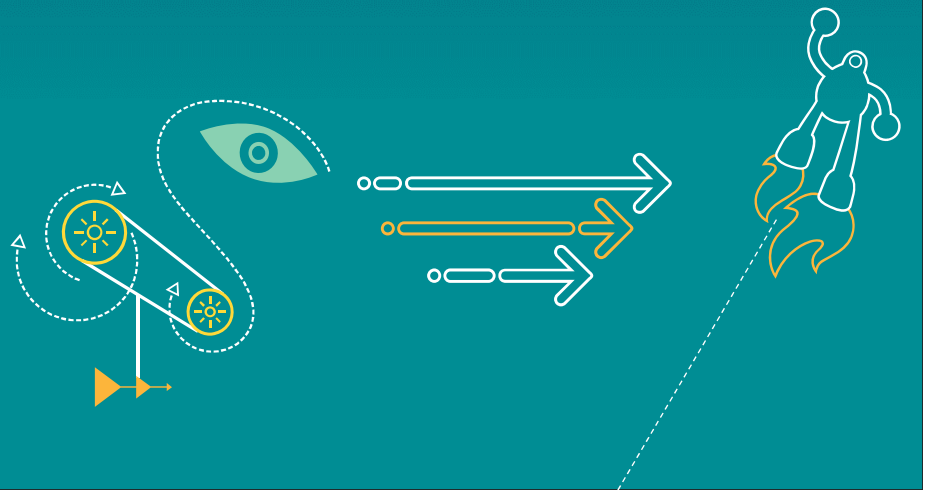
高通硬件基带技术期刊2016-2-4

QUALCOMM®

Qualcomm Technologies, Inc.



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Revision History

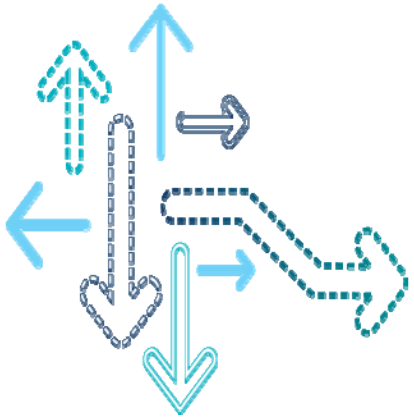
Revision	Date	Description
A	Feb 2016	Initial release

Note: There is no Rev. I, O, Q, S, X, or Z per Mil. standards.

Contents

- Baseband
- audio
- PMIC and SMB

Baseband



MSM8996 RF unused pin handle method update

- 适用平台：MSM8996
- Only four VDD_A2 pin change, no change for other signals

Terminating Unused RF Interface Signals (1 of 2)

I/F	MSM device specification name [1]	Unused pin state
TXDAC0	TX_DAC0_IP/M	Ground
	TX_DAC0_QP/M	Ground
	TX_DAC0_VREF	Ground
	VDD_A2 (pin AE47)	VREG_L15A_1P8
TXDAC1	TX_DAC1_IP/M	Ground
	TX_DAC1_QP/M	Ground
	TX_DAC1_VREF	Ground
	VDD_A2 (pin AB48)	VREG_L15A_1P8
ETDAC0	ET_DAC0_M/P	Ground
	ET_DAC0_VREF	Ground
	VDD_A2 (pin AC47)	VREG_L15A_1P8
ETDAC1	ET_DAC1_M/P	Ground
	ET_DAC1_VREF	Ground
	VDD_A2 (pin V46)	VREG_L15A_1P8

1. The names are from the *MSM8996 Device Specification* (80-NT204-1).

MSM8953 不使用DSI1时连接

- 适用平台： MSM8953
- 推荐：参考80-P2472-5B

Handling Unused Pins (2 of 6)

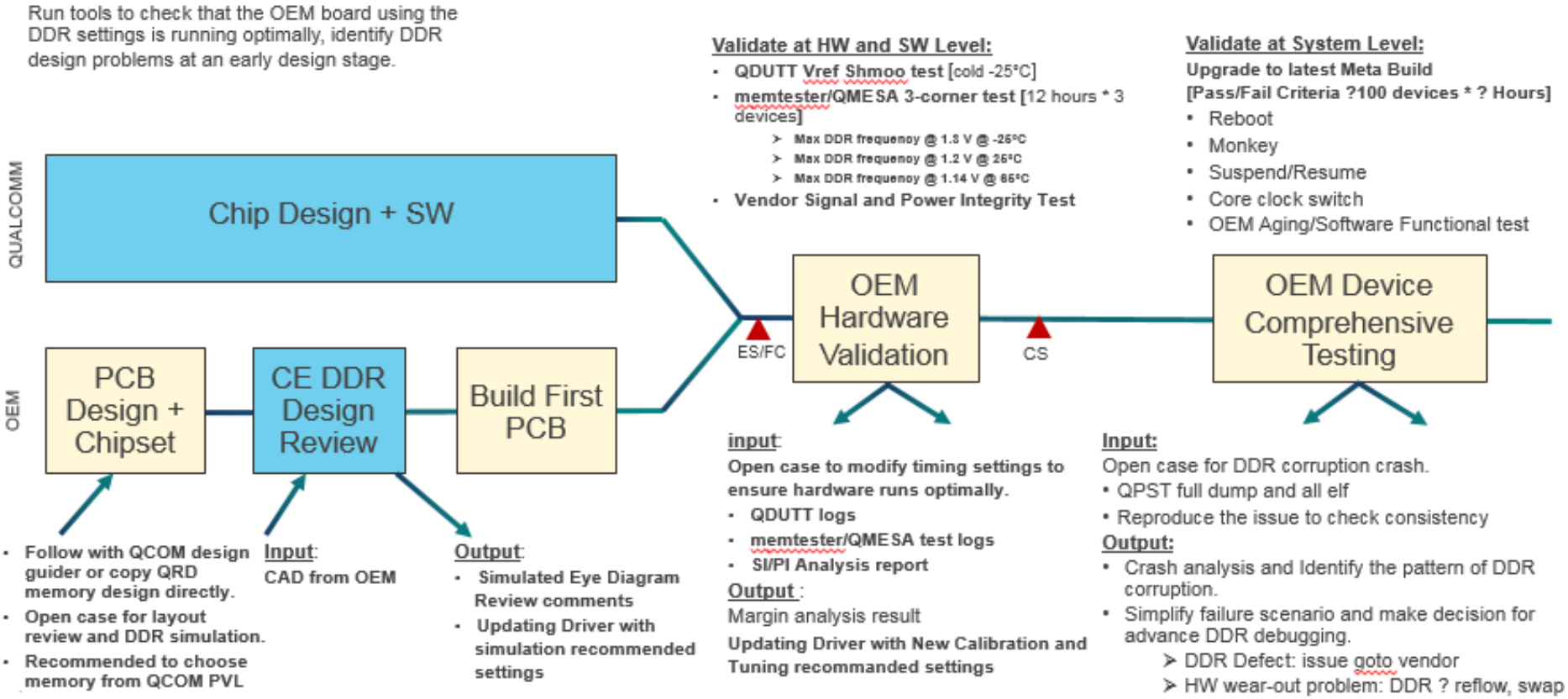
I/F	Signal	Unused pin state	Comments
MIPI DSI1	MIPI_DSI1_CLK_N/P	Float	
	MIPI_DSI1_LANE0_N/P	Float	
	MIPI_DSI1_LANE1_N/P	Float	
	MIPI_DSI1_LANE2_N/P	Float	
	MIPI_DSI1_LANE3_N/P	Float	
	MIPI_DSI1_REXT	Float	
	VDDA_MIPI_DSI1(VDD_DSI_CSI)	VSS (AE11 Pin number only)	
	VDDA_MIPI_DSI1_PLL (VDD_DSI_HV_PLL)	VSS (AE9 Pin number only)	
	VCCA_MIPI_DSI1_PLL (VDD_DSI_LV_PLL)	VSS (AF10 Pin number only)	

- 该改动将会更新到下一个版本参考原理图

DDR 开发流程

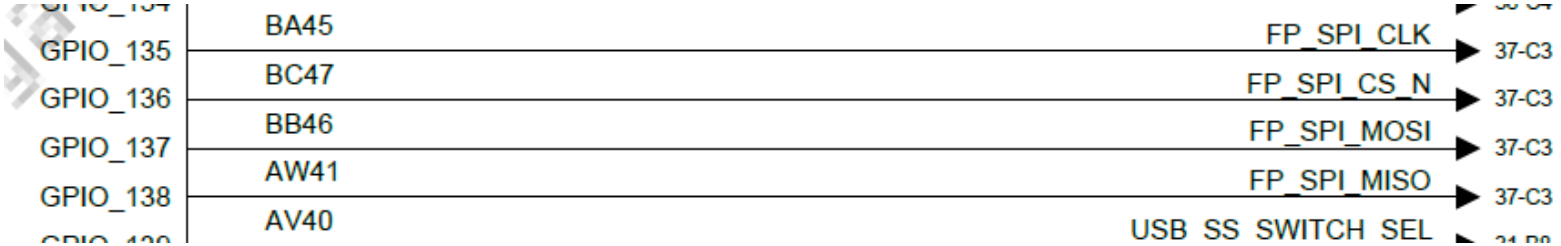
- 适用平台：MSM8909/MSM8952/MSM8937/MSM8953

Proposed OEM DDR Workflow



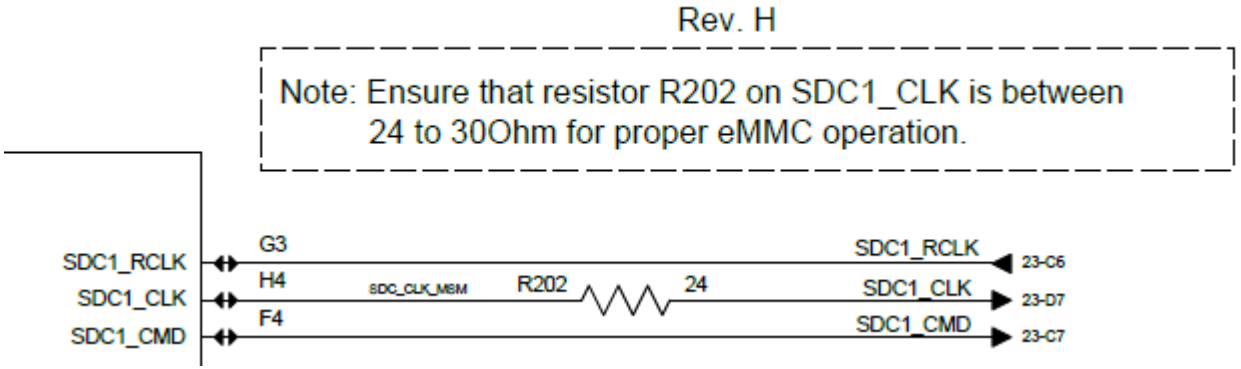
MSM8953 指纹识别SPI

- 适用平台： MSM8953
- 问题描述：请尽量参考高通最新参考设计(rev.B)。高通默认代码使用BLSP7（GPIO135-GPIO138）做为指纹识别SPI， BSLP6（GPIO20-23）预留给ADSP的SPI Sensors。
- 如果想使用其他端口请提软件case进行评估

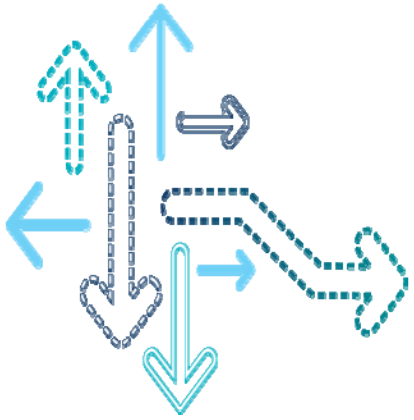


MSM8952 SDC1_CLK串联电阻

- 适用平台： MSM8952
- 问题描述：请尽量参考高通最新参考设计，QCOM eMMC研发部分建议改成24 ohm-30 ohm。 QRD之前的设计是0 ohm，后面也会做相应的更新。
- 如果客户的硬件已经定板，实际测试也没有问题，也可以不改。



Audio



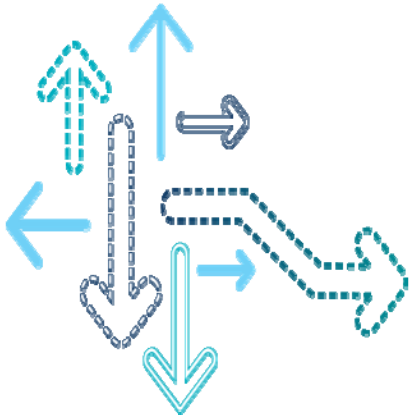
PM8956/PM8952/PM8937/PM8953

- 适用平台：MSM8956/MSM8952/MSM8973/MSM8953

- 对比PM8916，PM8956/PM8952/PM8937/PM8953 mic1增加了差分走线，但是某些版本的寄存器仍然和PM8916一样，在这种情况下，如果客户把上行算法bypass后会发现有TDMA noise。

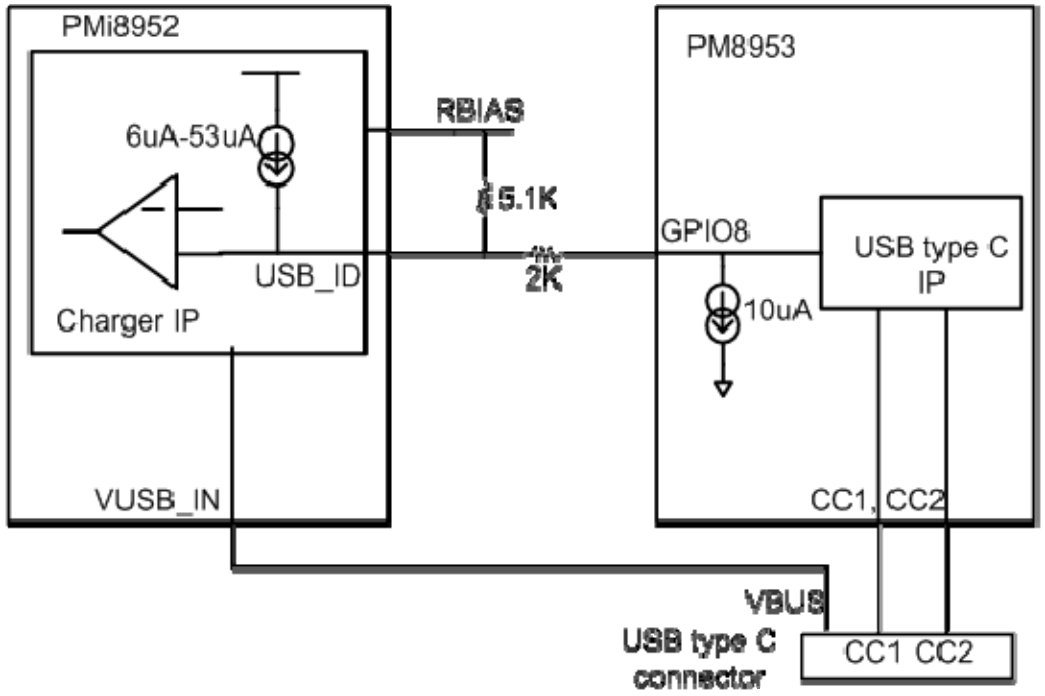
- 将寄存器F145改成0x02 来enable mic1的差分走线，F143改成0x09 将mic1_M连接到TX1_GND上面，这种情况下可以有效的降低noise,次方法主要用来debug， 如果确认问题， 请联系高通软件正式release patch。
- 我们有专门针对与外部micbias和内部micbias的patch。

PMIC



PM8953: Type C SDP/DCP/HVDCP 检测问题

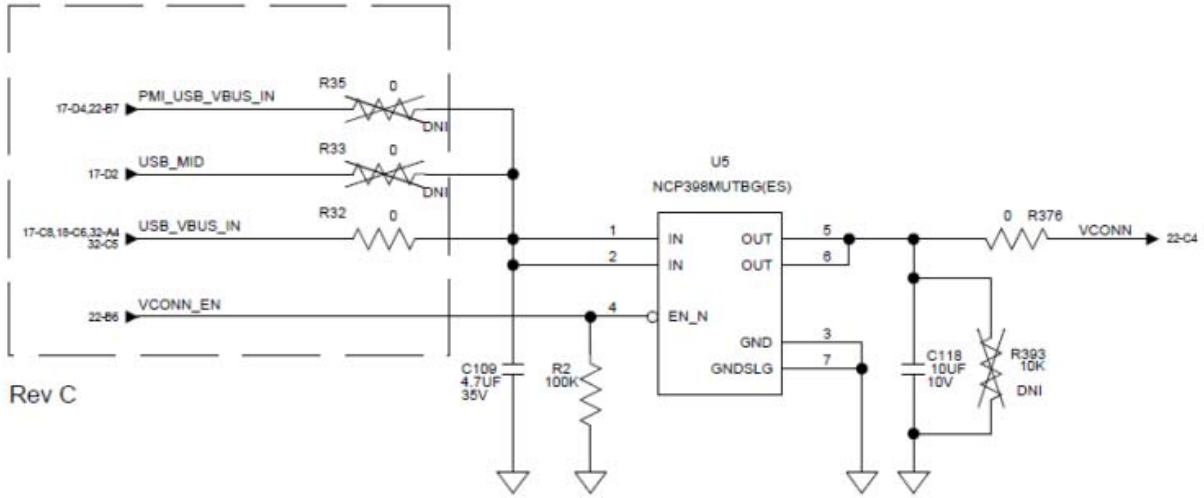
- 适用平台：PM8953
- 问题描述：由于pmi8952 usb_id 里边的RID检测开启时，由于GPIO8 内部默认10uA下拉，会导致USB_ID上电压<1V，导致后续SDP/DCP/HVDCP检测出问题。从而ICL不能被设置成500mA（SDP）或者HVDCP不能被检测到。
- 推荐：usb_id外部加入5.1K上拉到RBIAS，并在GPIO8与usb_id间串联2k电阻



- 该改动将会更新到下一个版本参考原理图

PM8953: Type C VCONN 软启动电流限制不准确

- 适用平台： PM8953
- 问题描述：由于PM8953内部软启动限流模块不准，会导致在插入有源电缆（电缆内电容>4.7uF）时,会导致触发VBUS ocp事件
- 推荐 1）使用Onsemi OVIC NCP398， 适用于10uF以下的有源电缆



Rev C

Note: Mount R33 and DNI R32 if Willsemi part WS3208D56-8/TR is used.

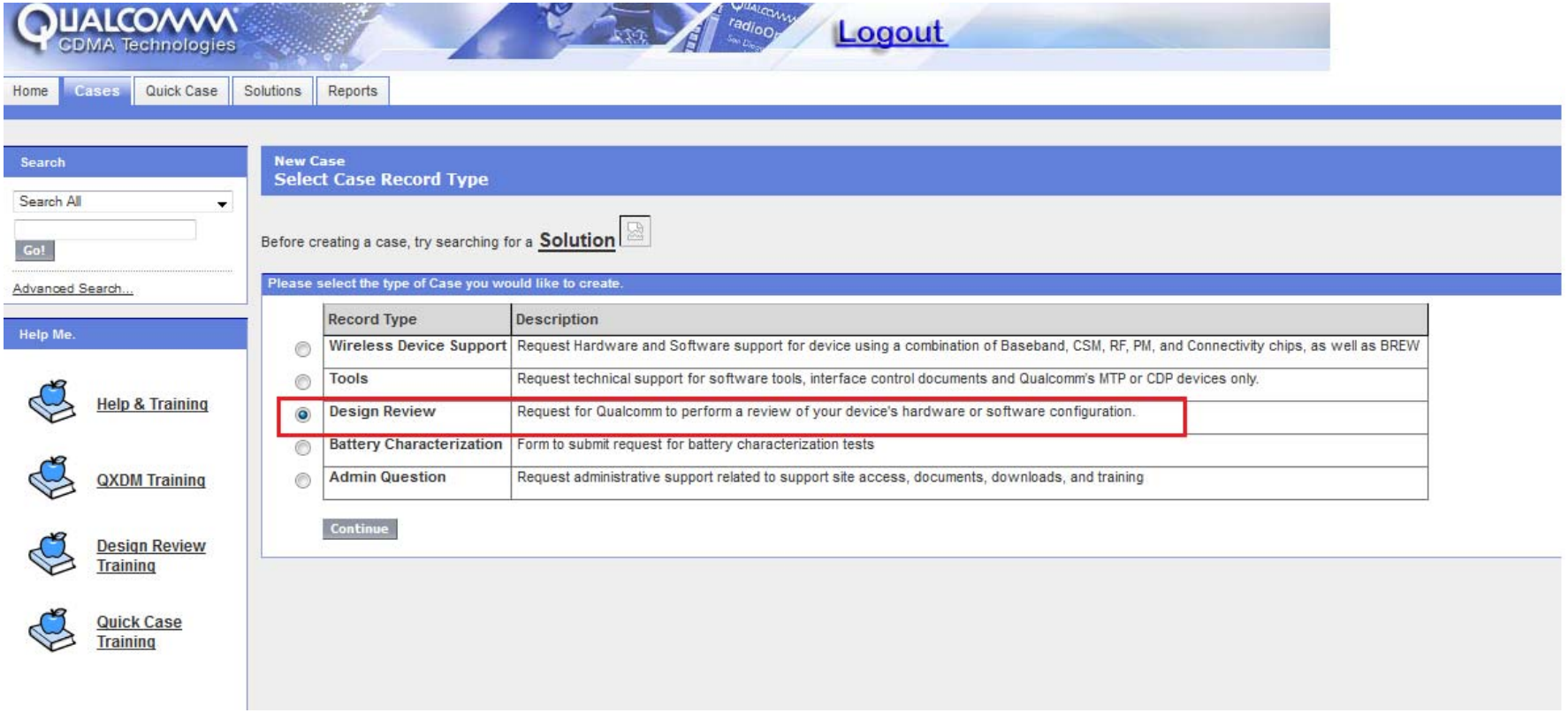
Note: Use Willsemi part WS3208D56-8/TR with no modification, If the active cable capacitance is less than 4.7uF

- 2）使用WS3208D56-8/TR,适用于4.7uF以下的有源电缆

该改动将会更新到下一个版本参考原理图

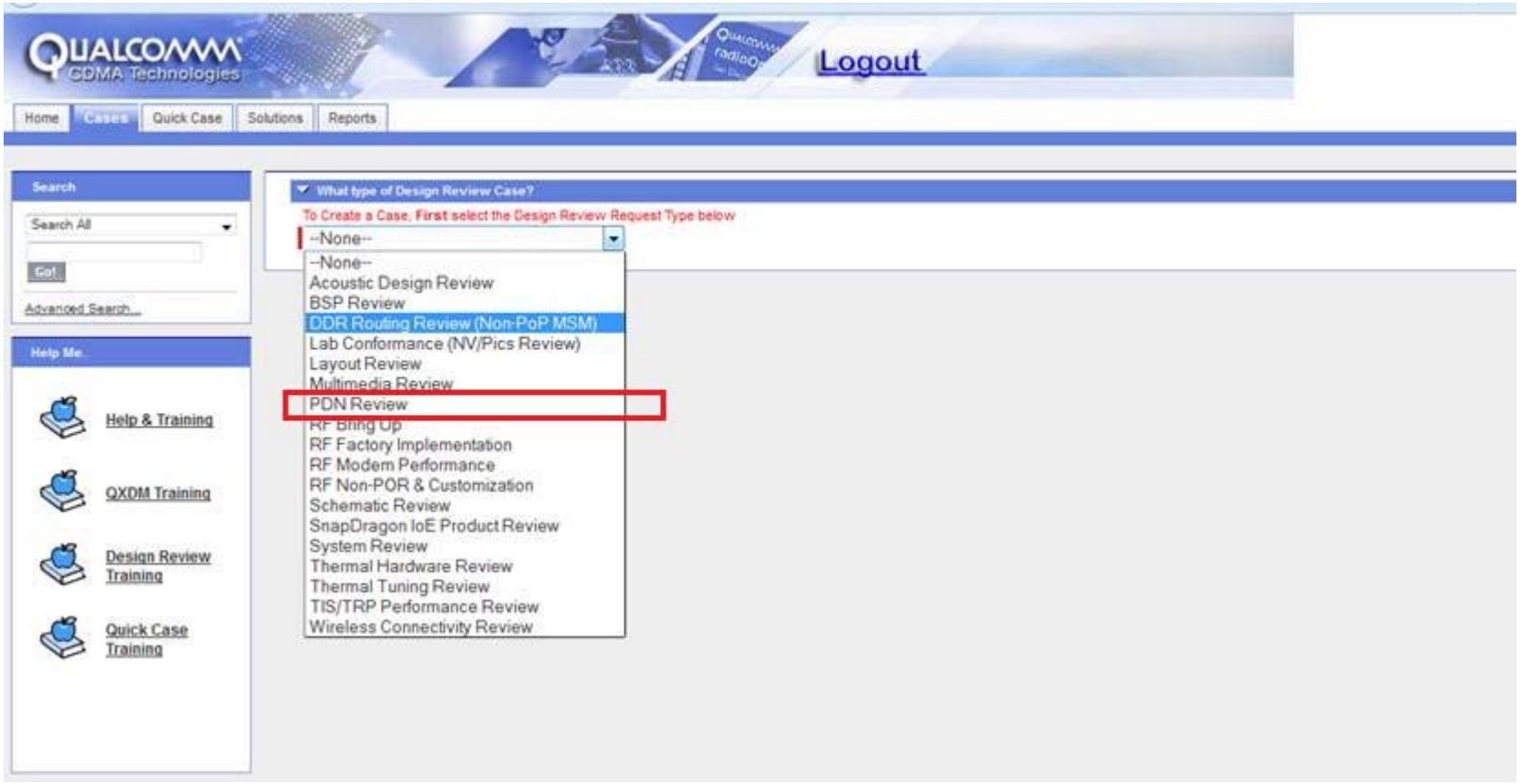
How to open PDN case-step1

- Select **design review** as case type



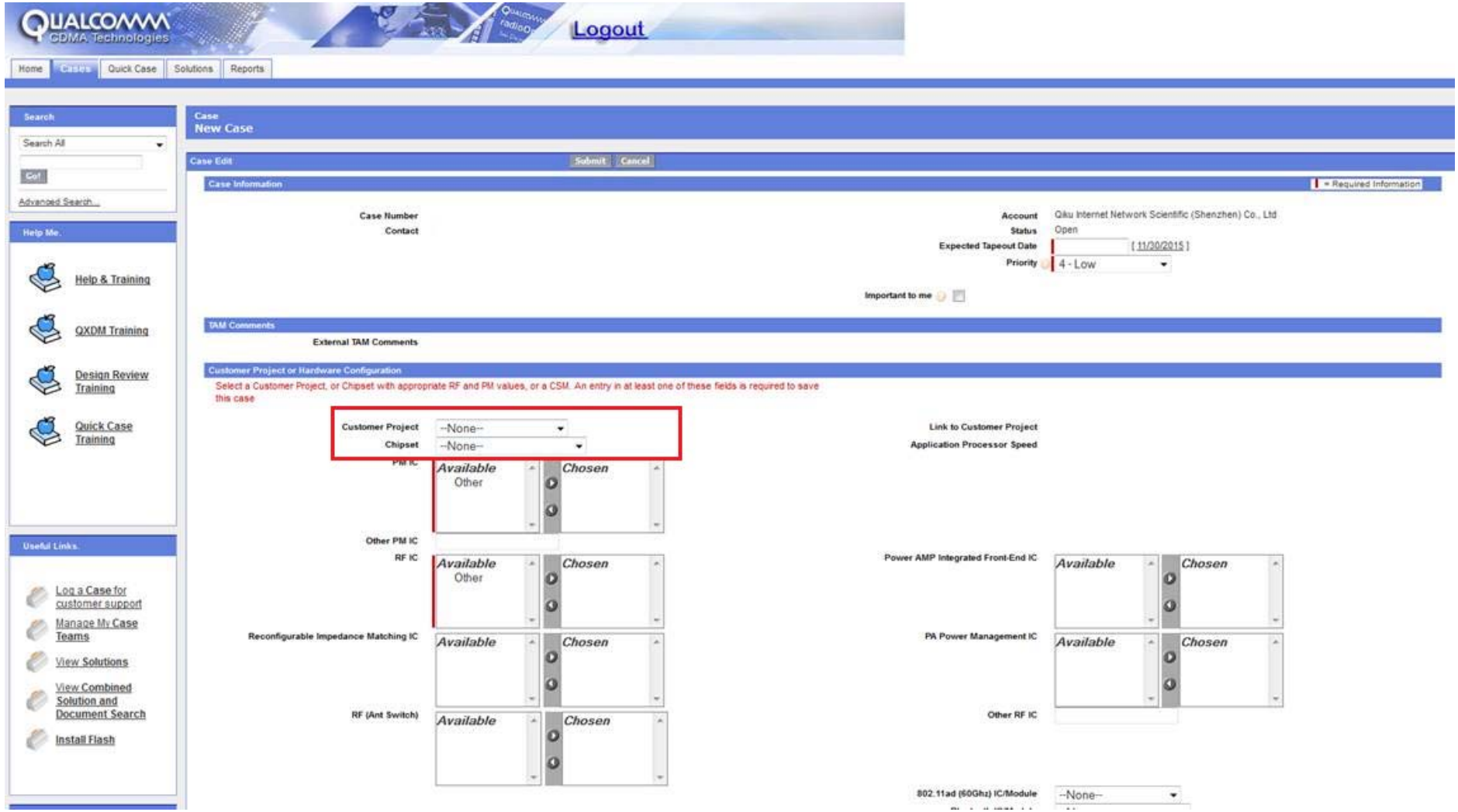
How to open PDN case-step2

- Select **PDN review** as design review type



How to open PDN case-step3

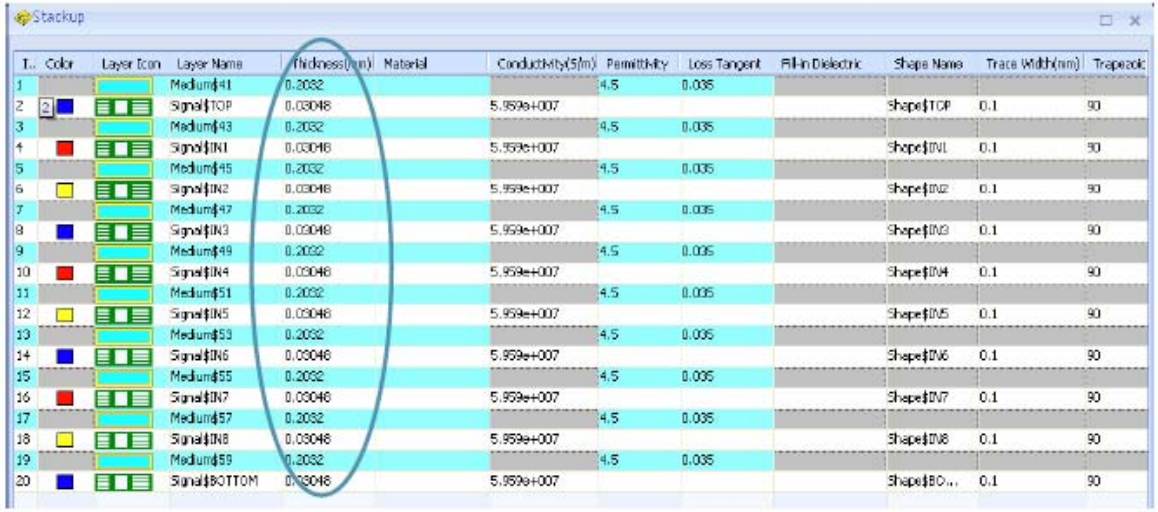
- Please DO select **customer project** before summit case.



How to open PDN case-step4

- Upload files for simulation.

1. Schematic.
2. Stack up file like below, thickness information must be provided.



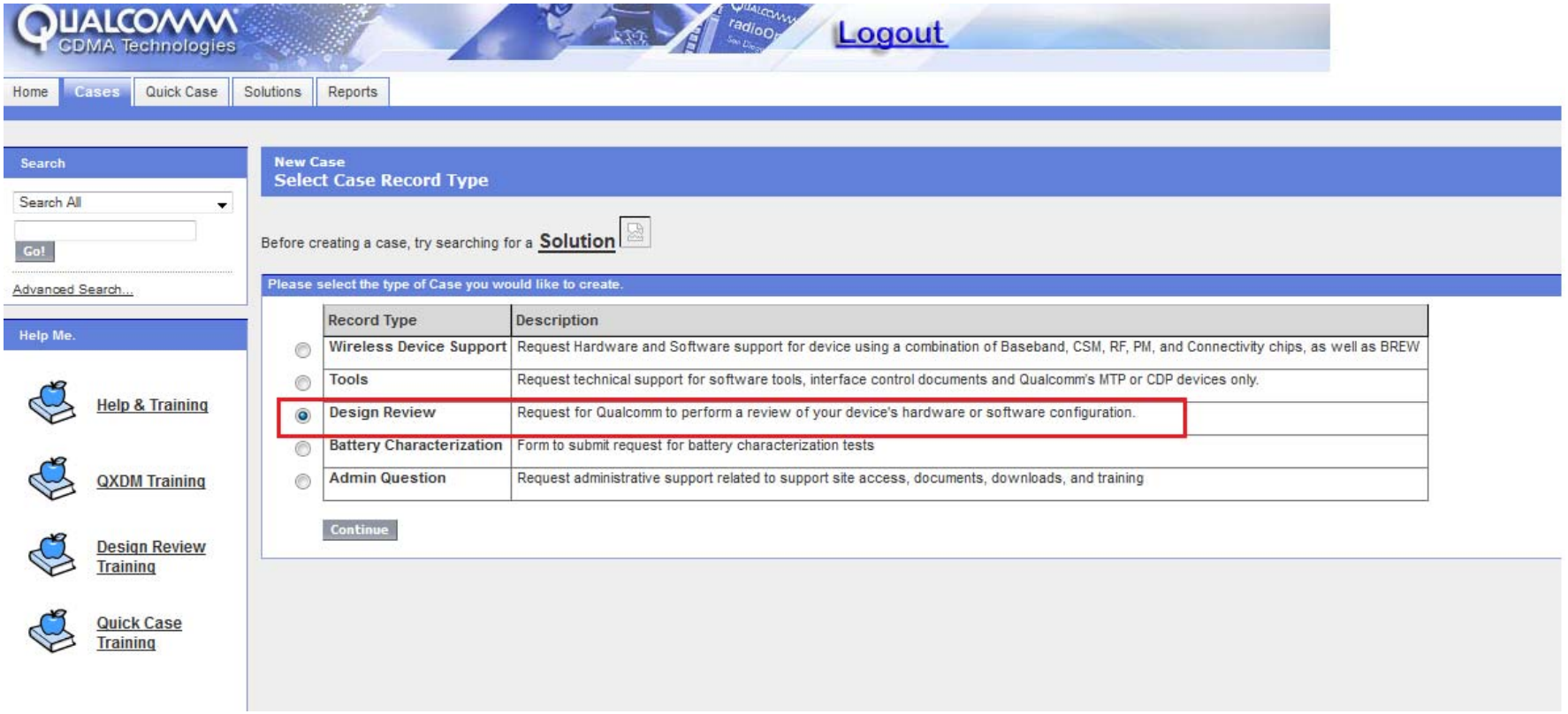
T..	Color	Layer Icon	Layer Name	Thickness(mm)	Material	Conductivity(S/m)	Permittivity	Loss Tangent	Fill-in Dielectric	Shape Name	Trace Width(mm)	Trapezoid
1			Medium$41	0.2032			4.5	0.035				
2			Signal$TOP	0.03048		5.959e+007				Shape$TOP	0.1	90
3			Medium$43	0.2032			4.5	0.035				
4			Signal$IN1	0.03048		5.959e+007				Shape$IN1	0.1	90
5			Medium$45	0.2032			4.5	0.035				
6			Signal$IN2	0.03048		5.959e+007				Shape$IN2	0.1	90
7			Medium$47	0.2032			4.5	0.035				
8			Signal$IN3	0.03048		5.959e+007				Shape$IN3	0.1	90
9			Medium$49	0.2032			4.5	0.035				
10			Signal$IN4	0.03048		5.959e+007				Shape$IN4	0.1	90
11			Medium$51	0.2032			4.5	0.035				
12			Signal$IN5	0.03048		5.959e+007				Shape$IN5	0.1	90
13			Medium$53	0.2032			4.5	0.035				
14			Signal$IN6	0.03048		5.959e+007				Shape$IN6	0.1	90
15			Medium$55	0.2032			4.5	0.035				
16			Signal$IN7	0.03048		5.959e+007				Shape$IN7	0.1	90
17			Medium$57	0.2032			4.5	0.035				
18			Signal$IN8	0.03048		5.959e+007				Shape$IN8	0.1	90
19			Medium$59	0.2032			4.5	0.035				
20			Signal$BOTTOM	0.03048		5.959e+007				Shape$BO...	0.1	90

3. Layout file

- Cadence Allegro →.brd
- OrCAD→.dsn
- Mentor Graphics –PADS →.pcb and .asc
- Mentor Graphics →Board Station →pcb folder
- ODB++ file –Make sure that the signal names are preserved when exported from CAD tools.

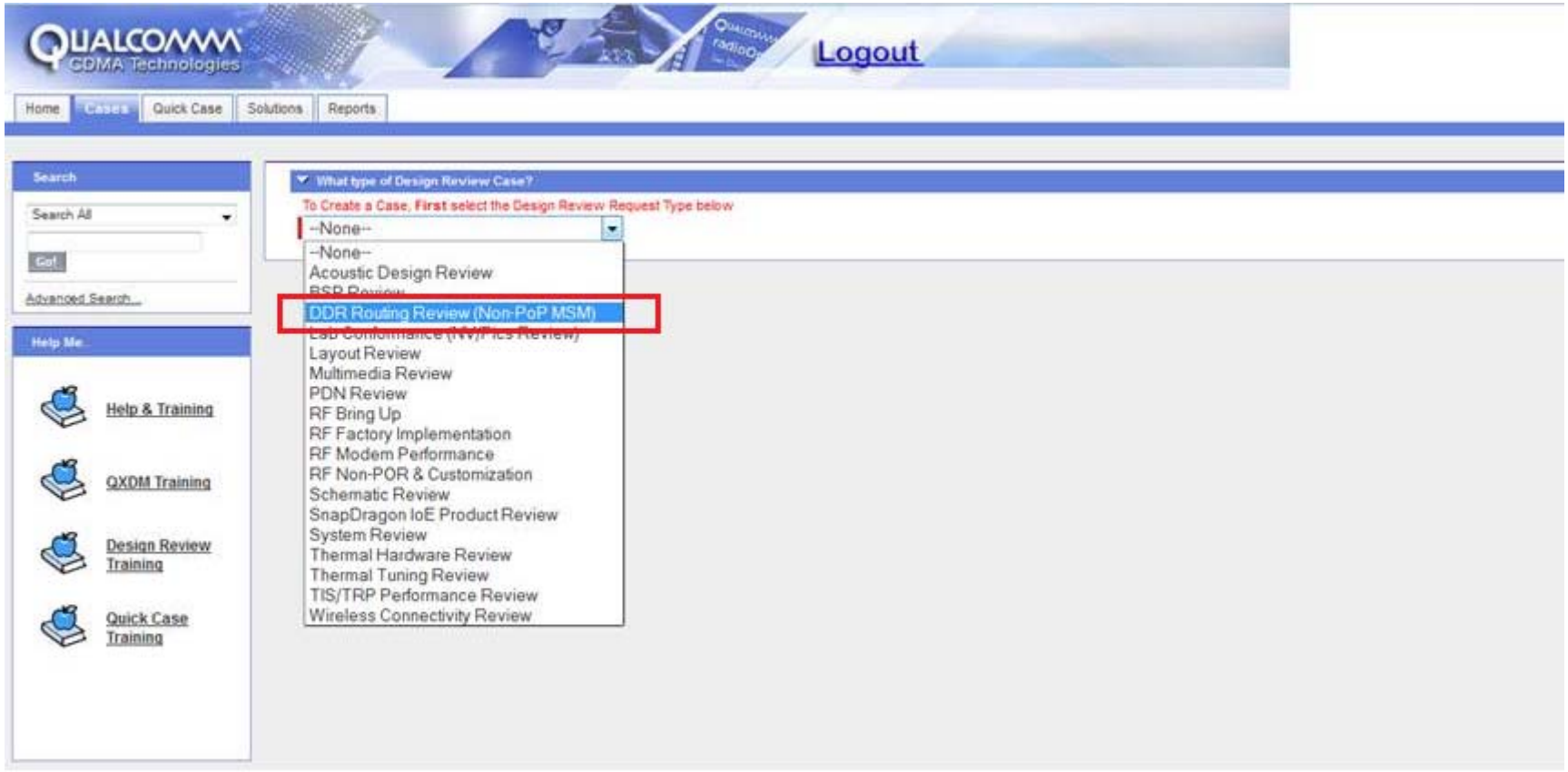
How to open DDR simulation case-step1

- Select **design review** as case type



How to open DDR simulation case-step2

- Select **DDR Routing Review(Non-PoP MSM)** as design review type



How to open DDR simulation case-step3

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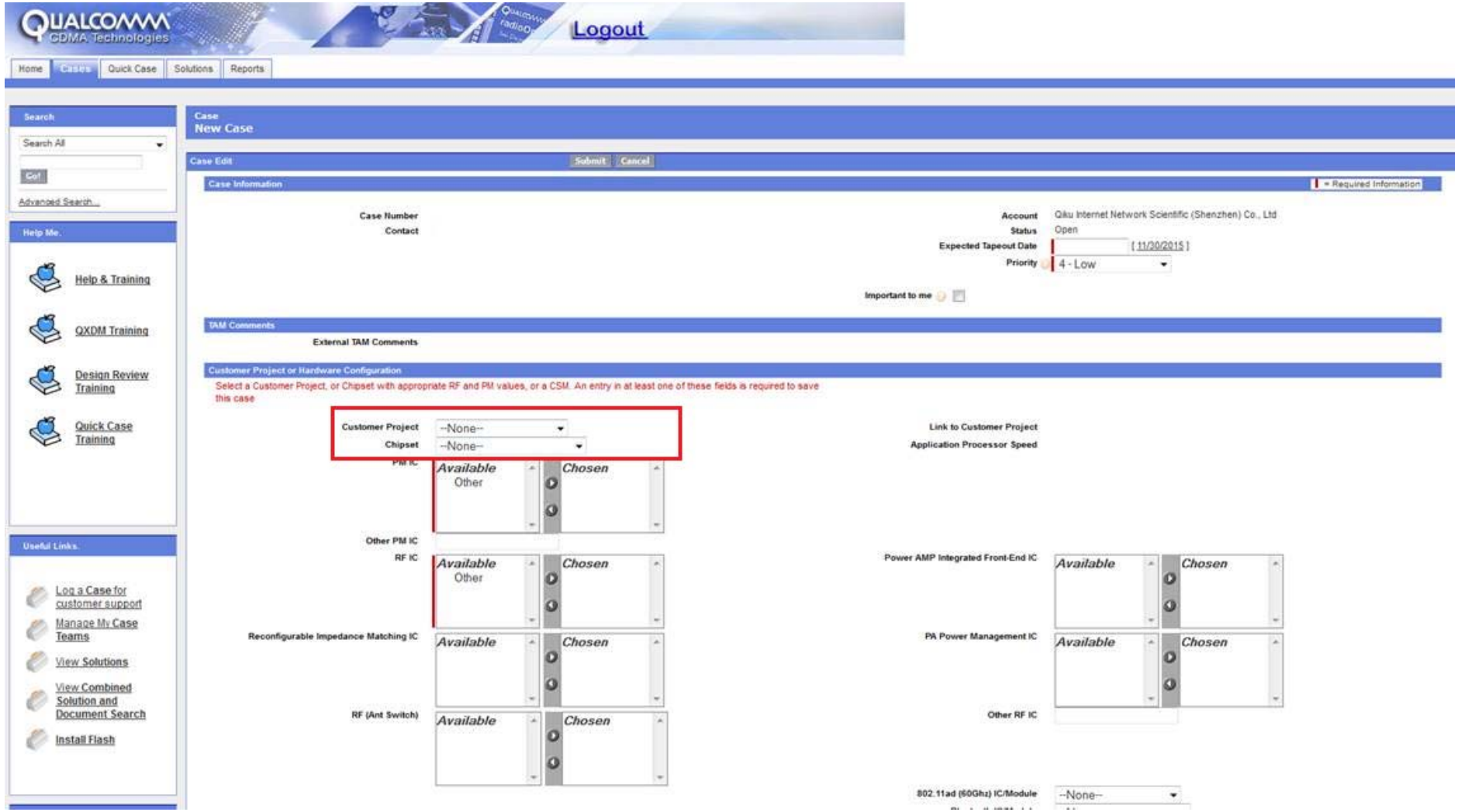

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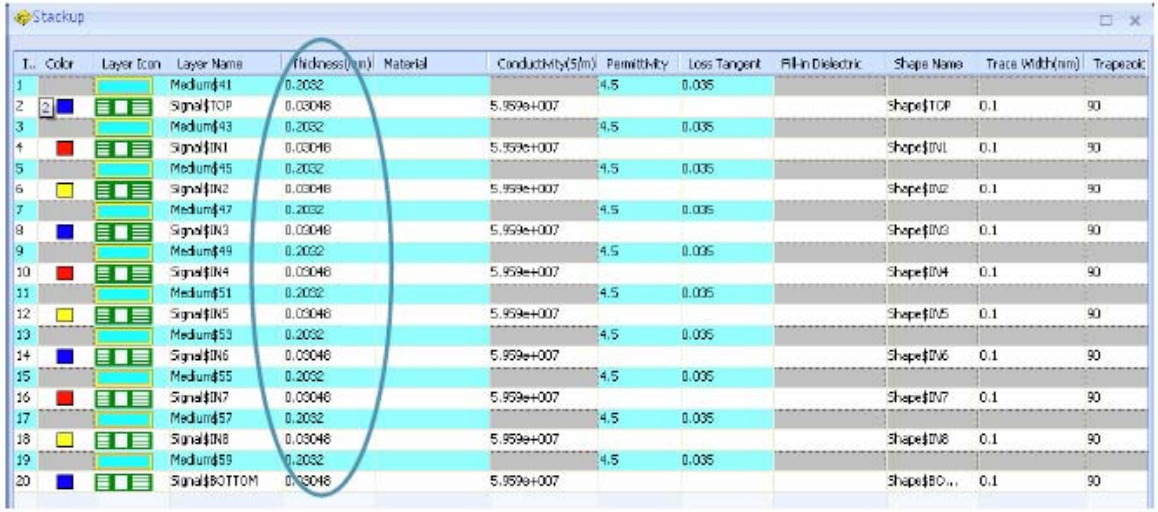

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14			Signal$IN6	0.03048		5.959e+007				Shape$IN6	0.1	90
15			Medium$55	0.2032			4.5	0.035				
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17			Medium$57	0.2032			4.5	0.035				
18			Signal$IN8	0.03048		5.959e+007				Shape$IN8	0.1	90
19			Medium$59	0.2032			4.5	0.035				
20			Signal$BOTTOM	0.03048		5.959e+007				Shape$BO...	0.1	90

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