Pin Information for the Arria™ GX EP1AGX90E Device
Version 1.0

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		VCCD_PLL7			K25			
		VCCA_PLL7			J26			
		GNDA_PLL7			K26			
		GNDA_PLL7			J25			
B2	VREFB2N0	FPLL7CLKp	INPUT		C34			
B2	VREFB2N0	FPLL7CLKn	INPUT		C33			
B2	VREFB2N0	VREFB2N0	VREFB2N0		R30			
B2	VREFB2N0	IO	DIFFIO_TX51p		F30			
B2	VREFB2N0	IO	DIFFIO_TX51n		G31			
B2	VREFB2N0	IO	DIFFIO_RX50p		D33			
B2	VREFB2N0	IO	DIFFIO_RX50n		D32			
B2	VREFB2N0	IO	DIFFIO_TX50p		H29			
B2	VREFB2N0	IO	DIFFIO_TX50n		G30			
B2	VREFB2N0	IO	DIFFIO_RX49p		E32			
B2	VREFB2N0	IO	DIFFIO_RX49n		E31			
B2	VREFB2N0	IO	DIFFIO_TX49p		J28			
B2	VREFB2N0	IO	DIFFIO_TX49n		K27			
B2	VREFB2N1	IO	DIFFIO_RX48p		E34			
B2	VREFB2N1	IO	DIFFIO_RX48n		D34			
B2	VREFB2N1	IO	DIFFIO_TX48p		J30			
B2	VREFB2N1	IO	DIFFIO_TX48n		J29			
B2	VREFB2N1	IO	DIFFIO_RX47p		F32			
B2	VREFB2N1	IO	DIFFIO_RX47n		F31			
B2	VREFB2N1	IO	DIFFIO_TX47p		K30			
B2	VREFB2N1	IO	DIFFIO_TX47n		K29			
B2	VREFB2N1	IO	DIFFIO_RX46p		F34			
B2	VREFB2N1	IO	DIFFIO_RX46n		F33			
B2	VREFB2N1	IO	DIFFIO_TX46p		L26			
B2	VREFB2N1	IO	DIFFIO_TX46n		L25			
B2	VREFB2N1	IO	DIFFIO_RX45p		G33			
B2	VREFB2N1	IO	DIFFIO_RX45n		G32			
B2	VREFB2N1	IO	DIFFIO_TX45p		M26			
B2	VREFB2N1	IO	DIFFIO_TX45n		M25			
B2	VREFB2N1	IO	DIFFIO_RX44p		H32			
B2	VREFB2N1	IO	DIFFIO_RX44n		H31			
B2	VREFB2N1	IO	DIFFIO_TX44p		K28			
B2	VREFB2N1	IO	DIFFIO_TX44n		L28			
B2	VREFB2N1	VREFB2N1	VREFB2N1		M30			
B2	VREFB2N1	IO	DIFFIO_RX43p		G34			
B2	VREFB2N1	IO	DIFFIO_RX43n		H34			
B2	VREFB2N1	IO	DIFFIO_TX43p		L29			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B2	VREFB2N1	IO	DIFFIO_TX43n		M29			
B2	VREFB2N1	IO	DIFFIO_RX42p		J32			
B2	VREFB2N1	IO	DIFFIO_RX42n		J31			
B2	VREFB2N1	IO	DIFFIO_TX42p		M28			
B2	VREFB2N1	IO	DIFFIO_TX42n		M27			
B2	VREFB2N1	IO	DIFFIO_RX41p		J34			
B2	VREFB2N1	IO	DIFFIO_RX41n		J33			
B2	VREFB2N1	IO	DIFFIO_TX41p		N27			
B2	VREFB2N1	IO	DIFFIO_TX41n		N26			
B2	VREFB2N1	IO	DIFFIO_RX40p		K33			
B2	VREFB2N1	IO	DIFFIO_RX40n		K32			
B2	VREFB2N1	IO	DIFFIO_TX40p		N25			
B2	VREFB2N1	IO	DIFFIO_TX40n		N24			
B2	VREFB2N1	IO	DIFFIO_RX39p		L32			
B2	VREFB2N1	IO	DIFFIO_RX39n		L31			
B2	VREFB2N1	IO	DIFFIO_TX39p		N23			
B2	VREFB2N1	IO	DIFFIO_TX39n		P23			
B2	VREFB2N2	IO	DIFFIO_RX38p		L34			
B2	VREFB2N2	IO	DIFFIO_RX38n		K34			
B2	VREFB2N2	IO	DIFFIO_TX38p		N29			
B2	VREFB2N2	IO	DIFFIO_TX38n		N28			
B2	VREFB2N2	IO	DIFFIO_RX37p		M32			
B2	VREFB2N2	IO	DIFFIO_RX37n		M31			
B2	VREFB2N2	IO	DIFFIO_TX37p		P29			
B2	VREFB2N2	IO	DIFFIO_TX37n		P28			
B2	VREFB2N2	IO	DIFFIO_RX36p		M34			
B2	VREFB2N2	IO	DIFFIO_RX36n		M33			
B2	VREFB2N2	IO	DIFFIO_TX36p		R29			
B2	VREFB2N2	IO	DIFFIO_TX36n		R28			
B2	VREFB2N2	IO	DIFFIO_RX35p		N31			
B2	VREFB2N2	IO	DIFFIO_RX35n		N30			
B2	VREFB2N2	IO	DIFFIO_TX35p		R23			
B2	VREFB2N2	IO	DIFFIO_TX35n		T23			
B2	VREFB2N2	IO	DIFFIO_RX34p		N33			
B2	VREFB2N2	IO	DIFFIO_RX34n		N32			
B2	VREFB2N2	IO	DIFFIO_TX34p		T29			
B2	VREFB2N2	IO	DIFFIO_TX34n		T28			
B2	VREFB2N2	VREFB2N2	VREFB2N2		K31			
B2	VREFB2N2	IO	DIFFIO_RX33p		P32			
B2	VREFB2N2	IO	DIFFIO_RX33n		P31			
B2	VREFB2N2	IO	DIFFIO_TX33p		U24			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B2	VREFB2N2	IO	DIFFIO_TX33n		U23			
B2	VREFB2N2	IO	DIFFIO_RX32p		N34			
B2	VREFB2N2	IO	DIFFIO_RX32n		P34			
B2	VREFB2N2	IO	DIFFIO_TX32p		U31			
B2	VREFB2N2	IO	DIFFIO_TX32n		U30			
B2	VREFB2N2	IO	DIFFIO_RX31p		R32			
B2	VREFB2N2	IO	DIFFIO_RX31n		R31			
B2	VREFB2N2	IO	DIFFIO_TX31p		U29			
B2	VREFB2N2	IO	DIFFIO_TX31n		U28			
B2	VREFB2N2	IO	DIFFIO_RX30p		R34			
B2	VREFB2N2	IO	DIFFIO_RX30n		R33			
B2	VREFB2N2	IO	DIFFIO_TX30p		W29			
B2	VREFB2N2	IO	DIFFIO_TX30n		V29			
B2	VREFB2N2	IO	DIFFIO_RX29p		T32			
B2	VREFB2N2	IO	DIFFIO_RX29n		T31			
B2	VREFB2N2	IO	DIFFIO_TX29p		U27			
B2	VREFB2N2	IO	DIFFIO_TX29n		V28			
B2	VREFB2N2	IO	CLK0n/DIFFIO_RX_C0n		T34			
B2	VREFB2N2	IO	CLK0p/DIFFIO_RX_C0p		U34			
B2	VREFB2N2	CLK1n	INPUT		U32			
B2	VREFB2N2	CLK1p	INPUT		U33			
		VCCD_PLL1			R27			
		VCCA_PLL1			T25			
		GNDA_PLL1			T26			
		GNDA_PLL1			R26			
		GNDA_PLL2			W26			
		GNDA_PLL2			V26			
		VCCA_PLL2			V25			
		VCCD_PLL2			W27			
B1	VREFB1N0	IO	CLK2p/DIFFIO_RX_C1p		W34			
B1	VREFB1N0	IO	CLK2n/DIFFIO_RX_C1n		V34			
B1	VREFB1N0	CLK3p	INPUT		V32			
B1	VREFB1N0	CLK3n	INPUT		V31			
B1	VREFB1N0	IO	DIFFIO_RX28p		W31			
B1	VREFB1N0	IO	DIFFIO_RX28n		W30			
B1	VREFB1N0	IO	DIFFIO_TX28p		V23			
B1	VREFB1N0	IO	DIFFIO_TX28n		W23			
B1	VREFB1N0	IO	DIFFIO_RX27p		W33			
B1	VREFB1N0	IO	DIFFIO_RX27n		W32			
B1	VREFB1N0	IO	DIFFIO_TX27p		Y24			
B1	VREFB1N0	IO	DIFFIO_TX27n		Y23			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B1	VREFB1N0	IO	DIFFIO_RX26p		Y32			
B1	VREFB1N0	IO	DIFFIO_RX26n		Y31			
B1	VREFB1N0	IO	DIFFIO_TX26p		W28			
B1	VREFB1N0	IO	DIFFIO_TX26n		Y29			
B1	VREFB1N0	IO	DIFFIO_RX25p		Y34			
B1	VREFB1N0	IO	DIFFIO_RX25n		Y33			
B1	VREFB1N0	IO	DIFFIO_TX25p		Y28			
B1	VREFB1N0	IO	DIFFIO_TX25n		Y27			
B1	VREFB1N0	VREFB1N0	VREFB1N0		AE31			
B1	VREFB1N0	IO	DIFFIO_RX24p		AA32			
B1	VREFB1N0	IO	DIFFIO_RX24n		AA31			
B1	VREFB1N0	IO	DIFFIO_TX24p		AA29			
B1	VREFB1N0	IO	DIFFIO_TX24n		AA28			
B1	VREFB1N0	IO	DIFFIO_RX23p		AB31			
B1	VREFB1N0	IO	DIFFIO_RX23n		AB30			
B1	VREFB1N0	IO	DIFFIO_TX23p		AA23			
B1	VREFB1N0	IO	DIFFIO_TX23n		AB23			
B1	VREFB1N0	IO	DIFFIO_RX22p		AB33			
B1	VREFB1N0	IO	DIFFIO_RX22n		AB32			
B1	VREFB1N0	IO	DIFFIO_TX22p		AA26			
B1	VREFB1N0	IO	DIFFIO_TX22n		AA25			
B1	VREFB1N0	IO	DIFFIO_RX21p		AA34			
B1	VREFB1N0	IO	DIFFIO_RX21n		AB34			
B1	VREFB1N0	IO	DIFFIO_TX21p		AB29			
B1	VREFB1N0	IO	DIFFIO_TX21n		AB28			
B1	VREFB1N0	IO	DIFFIO_RX20p		AC32			
B1	VREFB1N0	IO	DIFFIO_RX20n		AC31			
B1	VREFB1N0	IO	DIFFIO_TX20p		AB24			
B1	VREFB1N0	IO	DIFFIO_TX20n		AC24			
B1	VREFB1N1	IO	DIFFIO_RX19p		AC34			
B1	VREFB1N1	IO	DIFFIO_RX19n		AC33			
B1	VREFB1N1	IO	DIFFIO_TX19p		AB26			
B1	VREFB1N1	IO	DIFFIO_TX19n		AB25			
B1	VREFB1N1	IO	DIFFIO_RX18p		AD32			
B1	VREFB1N1	IO	DIFFIO_RX18n		AD31			
B1	VREFB1N1	IO	DIFFIO_TX18p		AC27			
B1	VREFB1N1	IO	DIFFIO_TX18n		AB27			
B1	VREFB1N1	IO	DIFFIO_RX17p		AE33			
B1	VREFB1N1	IO	DIFFIO_RX17n		AE32			
B1	VREFB1N1	IO	DIFFIO_TX17p		AD26			
B1	VREFB1N1	IO	DIFFIO_TX17n		AD25			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B1	VREFB1N1	IO	DIFFIO_RX16p		AD34			
B1	VREFB1N1	IO	DIFFIO_RX16n		AE34			
B1	VREFB1N1	IO	DIFFIO_TX16p		AC29			
B1	VREFB1N1	IO	DIFFIO_TX16n		AC28			
B1	VREFB1N1	IO	DIFFIO_RX15p		AF32			
B1	VREFB1N1	IO	DIFFIO_RX15n		AF31			
B1	VREFB1N1	IO	DIFFIO_TX15p		AD29			
B1	VREFB1N1	IO	DIFFIO_TX15n		AD28			
B1	VREFB1N1	VREFB1N1	VREFB1N1		AC30			
B1	VREFB1N1	IO	DIFFIO_RX14p		AF34			
B1	VREFB1N1	IO	DIFFIO_RX14n		AF33			
B1	VREFB1N1	IO	DIFFIO_TX14p		AE30			
B1	VREFB1N1	IO	DIFFIO_TX14n		AE29			
B1	VREFB1N1	IO	DIFFIO_RX13p		AG32			
B1	VREFB1N1	IO	DIFFIO_RX13n		AG31			
B1	VREFB1N1	IO	DIFFIO_TX13p		AE28			
B1	VREFB1N1	IO	DIFFIO_TX13n		AE27			
B1	VREFB1N1	IO	DIFFIO_RX12p		AG34			
B1	VREFB1N1	IO	DIFFIO_RX12n		AH34			
B1	VREFB1N1	IO	DIFFIO_TX12p		AF30			
B1	VREFB1N1	IO	DIFFIO_TX12n		AF29			
B1	VREFB1N1	IO	DIFFIO_RX11p		AH33			
B1	VREFB1N1	IO	DIFFIO_RX11n		AH32			
B1	VREFB1N1	IO	DIFFIO_TX11p		AF28			
B1	VREFB1N1	IO	DIFFIO_TX11n		AF27			
B1	VREFB1N1	IO	DIFFIO_RX10p		AJ34			
B1	VREFB1N1	IO	DIFFIO_RX10n		AJ33			
B1	VREFB1N1	IO	DIFFIO_TX10p		AG29			
B1	VREFB1N1	IO	DIFFIO_TX10n		AG28			
B1	VREFB1N2	IO	DIFFIO_RX9p		AJ32			
B1	VREFB1N2	IO	DIFFIO_RX9n		AJ31			
B1	VREFB1N2	IO	DIFFIO_TX9p		AH31			
B1	VREFB1N2	IO	DIFFIO_TX9n		AH30			
B1	VREFB1N2	IO	DIFFIO_RX8p		AL34			
B1	VREFB1N2	IO	DIFFIO_RX8n		AK34			
B1	VREFB1N2	IO	DIFFIO_TX8p		AH29			
B1	VREFB1N2	IO	DIFFIO_TX8n		AH28			
B1	VREFB1N2	IO	DIFFIO_RX7p		AK32			
B1	VREFB1N2	IO	DIFFIO_RX7n		AK31			
B1	VREFB1N2	IO	DIFFIO_TX7p		AJ30			
B1	VREFB1N2	IO	DIFFIO_TX7n		AJ29			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B1	VREFB1N2	IO	DIFFIO_RX6p		AL33			
B1	VREFB1N2	IO	DIFFIO_RX6n		AL32			
B1	VREFB1N2	VREFB1N2	VREFB1N2		Y30			
B1	VREFB1N2	FPLL8CLKn	INPUT		AM33			
B1	VREFB1N2	FPLL8CLKp	INPUT		AM34			
		GNDA_PLL8			AE26			
		GNDA_PLL8			AF25			
		VCCA_PLL8			AF26			
		VCCD_PLL8			AE25			
B8	VREFB8N0	TDI		TDI	AL31			
B8	VREFB8N0	TMS		TMS	AM32			
B8	VREFB8N0	TCK		TCK	AE24			
B8	VREFB8N0	TRST		TRST	AM31			
B8	VREFB8N0	nCONFIG		nCONFIG	AL30			
B8	VREFB8N0	VCCSEL		VCCSEL	AF24			
B8	VREFB8N0	IO		CS	AH27			
B8	VREFB8N0	IO		CLKUSR	AH26			
B8	VREFB8N0	IO		nWS	AG26			
B8	VREFB8N0	IO		nRS	AG25			
B8	VREFB8N0	IO			AC23			
B8	VREFB8N0	IO			AH25			
B8	VREFB8N0	IO			AL29			
B8	VREFB8N0	VREFB8N0	VREFB8N0		AK28			
B8	VREFB8N0	IO			AB22			
B8	VREFB8N0	IO	DQ17B		AM30	DQ8B		
B8	VREFB8N0	IO			AN31	DQ8B	DQ3B	DQ1B
B8	VREFB8N0	IO	DQ17B		AN32	DQ8B	DQ3B	
B8	VREFB8N0	IO	DQ17B		AP32	DQ8B	DQ3B	DQ1B
B8	VREFB8N0	IO	DQ17B		AP30	DQ8B	DQ3B	DQ1B
B8	VREFB8N0	IO	DQS17B		AP31			
B8	VREFB8N0	IO			AG23			
B8	VREFB8N0	IO			AD23			
B8	VREFB8N0	IO	DQ16B		AP29	DQ8B	DQ3B	DQ1B
B8	VREFB8N0	IO			AN29		DQ3B	DQ1B
B8	VREFB8N0	IO	DQ16B		AM29	DQ8B	DQ3B	DQ1B
B8	VREFB8N0	IO	DQ16B		AP28	DQ8B	DQ3B	DQ1B
B8	VREFB8N0	IO	DQ16B		AM28	DQ8B	DQ3B	DQ1B
B8	VREFB8N0	IO	DQS16B		AN28	DQS8B		
B8	VREFB8N0	IO	DQ15B		AJ27	DQ7B	DQ3B	DQ1B
B8	VREFB8N0	IO			AL28	DQ7B		DQ1B
B8	VREFB8N1	IO	DQ15B		AJ28	DQ7B	DQ3B	DQ1B

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B8	VREFB8N1	IO	DQ15B		AM27	DQ7B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQ15B		AP27	DQ7B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQS15B		AL27		DQS3B	
B8	VREFB8N1	IO			AE23			
B8	VREFB8N1	IO	DQ14B		AN26	DQ7B	DQ3B	DQ1B
B8	VREFB8N1	IO			AL26		DQ3B	DQ1B
B8	VREFB8N1	IO	DQ14B		AJ26	DQ7B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQ14B		AK26	DQ7B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQ14B		AP26	DQ7B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQS14B		AM26	DQS7B		
B8	VREFB8N1	IO			AC22			
B8	VREFB8N1	IO			AD22			
B8	VREFB8N1	VREFB8N1	VREFB8N1		AK25			
B8	VREFB8N1	IO			AF22			
B8	VREFB8N1	IO	DQ13B		AJ24	DQ6B		
B8	VREFB8N1	IO			AL25	DQ6B	DQ2B	
B8	VREFB8N1	IO	DQ13B		AJ25	DQ6B	DQ2B	DQ1B
B8	VREFB8N1	IO	DQ13B		AN25	DQ6B	DQ2B	DQ1B
B8	VREFB8N1	IO	DQ13B		AP25	DQ6B	DQ2B	DQ1B
B8	VREFB8N1	IO	DQS13B		AM25			DQS1B
B8	VREFB8N1	IO			AE22			
B8	VREFB8N1	IO	DQ12B		AM24	DQ6B	DQ2B	DQ1B
B8	VREFB8N1	IO			AL24		DQ2B	DQ1B
B8	VREFB8N1	IO	DQ12B		AJ23	DQ6B	DQ2B	DQ1B
B8	VREFB8N1	IO	DQ12B		AK23	DQ6B	DQ2B	DQ1B
B8	VREFB8N1	IO	DQ12B		AP24	DQ6B	DQ2B	DQ1B
B8	VREFB8N1	IO	DQS12B		AL23	DQS6B		
B8	VREFB8N1	IO			AB21			
B8	VREFB8N1	IO			AC21			
B8	VREFB8N2	IO			AB20			
B8	VREFB8N2	IO	DQ11B		AM23	DQ5B	DQ2B	DQ1B
B8	VREFB8N2	IO			AN23	DQ5B		DQ1B
B8	VREFB8N2	IO	DQ11B		AP23	DQ5B	DQ2B	DQ1B
B8	VREFB8N2	IO	DQ11B		AM22	DQ5B	DQ2B	DQ1B
B8	VREFB8N2	IO	DQ11B		AP22	DQ5B	DQ2B	DQ1B
B8	VREFB8N2	IO	DQS11B		AN22		DQS2B	
B8	VREFB8N2	IO			AC20			
B8	VREFB8N2	IO			AH21			
B8	VREFB8N2	IO			AH22			
B8	VREFB8N2	IO			AC19			
B8	VREFB8N2	IO	DQ10B		AJ22	DQ5B	DQ2B	DQ1B

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B8	VREFB8N2	IO			AL22		DQ2B	DQ1B
B8	VREFB8N2	IO	DQ10B		AM21	DQ5B	DQ2B	DQ1B
B8	VREFB8N2	IO	DQ10B		AP21	DQ5B	DQ2B	DQ1B
B8	VREFB8N2	IO	DQ10B		AJ21	DQ5B	DQ2B	DQ1B
B8	VREFB8N2	IO	DQS10B		AL21	DQS5B		
B8	VREFB8N2	VREFB8N2	VREFB8N2		AK22			
B8	VREFB8N2	IO			AC18			
B8	VREFB8N2	IO			AH23			
B8	VREFB8N2	IO		RUnLU	AH18			
B8	VREFB8N2	IO		DEV_OE	AG20			
B8	VREFB8N2	IO		DEV_CLRn	AH20			
B8	VREFB8N2	IO		nCS	AJ18			
B12	VREFB8N2	IO	PLL12_FBn/OUT2n		AJ20			
B12	VREFB8N2	IO	PLL12_FBp/OUT2p		AK20			
B8	VREFB8N2	IO			AB17			
B12	VREFB8N2	IO	PLL12_OUT1n		AL20			
B12	VREFB8N2	IO	PLL12_OUT1p		AM20			
B12	VREFB8N2	IO	PLL12_OUT0n		AN20			
B12	VREFB8N2	IO	PLL12_OUT0p		AP20			
B8	VREFB8N2	IO	CLK5n		AH19			
B8	VREFB8N2	IO	CLK5p		AJ19			
B8	VREFB8N2	IO	CLK4n		AM19			
B8	VREFB8N2	IO	CLK4p		AN19			
B12		VCC_PLL12_OUT			AE20			
		VCCD_PLL12			AF20			
		VCCA_PLL12			AE18			
		GNDA_PLL12			AF18			
		GNDA_PLL12			AF19			
		GNDA_PLL6			AF17			
		VCCA_PLL6			AE16			
		VCCD_PLL6			AF16			
		GNDA_PLL6			AE17			
B10		VCC_PLL6_OUT			AG16			
B7	VREFB7N0	IO	CLK7p		AL19			
B7	VREFB7N0	IO	CLK7n		AK19			
B7	VREFB7N0	IO	CLK6p		AP18			
B7	VREFB7N0	IO	CLK6n		AP19			
B10	VREFB7N0	IO	PLL6_OUT1p		AM18			
B10	VREFB7N0	IO	PLL6_OUT1n		AL18			
B10	VREFB7N0	IO	PLL6_OUT0p		AP17			
B10	VREFB7N0	IO	PLL6_OUT0n		AN17			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B10	VREFB7N0	IO	PLL6_FBp/OUT2p		AM17			
B10	VREFB7N0	IO	PLL6_FBn/OUT2n		AL17			
B7	VREFB7N0	IO			AC17			
B7	VREFB7N0	IO			AC16			
B7	VREFB7N0	IO	DQ9B		AJ16	DQ4B		
B7	VREFB7N0	IO			AL16	DQ4B	DQ1B	DQ0B
B7	VREFB7N0	VREFB7N0	VREFB7N0		AK17			
B7	VREFB7N0	IO	DQ9B		AK16	DQ4B	DQ1B	
B7	VREFB7N0	IO	DQ9B		AN16	DQ4B	DQ1B	DQ0B
B7	VREFB7N0	IO	DQ9B		AP16	DQ4B	DQ1B	DQ0B
B7	VREFB7N0	IO	DQS9B		AM16			
B7	VREFB7N0	IO			AB16			
B7	VREFB7N0	IO			AJ17			
B7	VREFB7N0	IO	DQ8B		AH16	DQ4B	DQ1B	DQ0B
B7	VREFB7N0	IO			AM15		DQ1B	DQ0B
B7	VREFB7N0	IO	DQ8B		AH15	DQ4B	DQ1B	DQ0B
B7	VREFB7N0	IO	DQ8B		AJ15	DQ4B	DQ1B	DQ0B
B7	VREFB7N0	IO	DQ8B		AP15	DQ4B	DQ1B	DQ0B
B7	VREFB7N0	IO	DQS8B		AL15	DQS4B		
B7	VREFB7N0	IO			AC15			
B7	VREFB7N0	IO	DQ7B		AP14	DQ3B	DQ1B	DQ0B
B7	VREFB7N0	IO			AM14	DQ3B		DQ0B
B7	VREFB7N1	IO	DQ7B		AK14	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ7B		AJ14	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ7B		AN14	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQS7B		AL14		DQS1B	
B7	VREFB7N1	IO			AD14			
B7	VREFB7N1	IO	DQ6B		AP13	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO			AM13		DQ1B	DQ0B
B7	VREFB7N1	IO	DQ6B		AH13	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ6B		AJ13	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ6B		AN13	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQS6B		AL13	DQS3B		
B7	VREFB7N1	IO			AE14			
B7	VREFB7N1	IO	DQ5B		AP12	DQ2B		
B7	VREFB7N1	IO			AM12	DQ2B	DQ0B	
B7	VREFB7N1	VREFB7N1	VREFB7N1		AK13			
B7	VREFB7N1	IO	DQ5B		AH11	DQ2B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQ5B		AH12	DQ2B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQ5B		AJ12	DQ2B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQS5B		AL12			DQS0B

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B7	VREFB7N1	IO			AC14			
B7	VREFB7N1	IO	DQ4B		AP11	DQ2B	DQ0B	DQ0B
B7	VREFB7N1	IO			AM11		DQ0B	DQ0B
B7	VREFB7N1	IO	DQ4B		AJ11	DQ2B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQ4B		AK11	DQ2B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQ4B		AN11	DQ2B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQS4B		AL11	DQS2B		
B7	VREFB7N1	IO			AE13			
B7	VREFB7N1	IO	DQ3B		AP10	DQ1B	DQ0B	DQ0B
B7	VREFB7N1	IO			AM10	DQ1B		DQ0B
B7	VREFB7N1	IO	DQ3B		AH10	DQ1B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQ3B		AJ10	DQ1B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQ3B		AN10	DQ1B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQS3B		AL10		DQS0B	
B7	VREFB7N2	IO			AD13			
B7	VREFB7N2	IO			AH14			
B7	VREFB7N2	IO	DQ2B		AP9	DQ1B	DQ0B	DQ0B
B7	VREFB7N2	IO			AM9		DQ0B	DQ0B
B7	VREFB7N2	IO	DQ2B		AH9	DQ1B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQ2B		AH8	DQ1B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQ2B		AJ9	DQ1B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQS2B		AL9	DQS1B		
B7	VREFB7N2	IO			AC13			
B7	VREFB7N2	IO	DQ1B		AP8	DQ0B		
B7	VREFB7N2	IO			AM8	DQ0B		
B7	VREFB7N2	IO	DQ1B		AJ8	DQ0B		
B7	VREFB7N2	IO	DQ1B		AK8	DQ0B		
B7	VREFB7N2	IO	DQ1B		AN8	DQ0B		
B7	VREFB7N2	IO	DQS1B		AL8			
B7	VREFB7N2	VREFB7N2	VREFB7N2		AK10			
B7	VREFB7N2	IO			AG13			
B7	VREFB7N2	IO	DQ0B		AP7	DQ0B		
B7	VREFB7N2	IO			AM7			
B7	VREFB7N2	IO	DQ0B		AG8	DQ0B		
B7	VREFB7N2	IO	DQ0B		AH7	DQ0B		
B7	VREFB7N2	IO	DQ0B		AJ7	DQ0B		
B7	VREFB7N2	IO	DQS0B		AL7	DQS0B		
B7	VREFB7N2	IO			AF11			
B7	VREFB7N2	IO			AG11			
B7	VREFB7N2	IO			AG10			
B7	VREFB7N2	IO	RDN7		AE10			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B7	VREFB7N2	IO	RUP7		AE9			
B7	VREFB7N2	IO			AF10			
B7	VREFB7N2	PORSEL		PORSEL	AE8			
B7	VREFB7N2	nIO_PULLUP		nIO_PULLUP	AE7			
B7	VREFB7N2	PLL_ENA		PLL_ENA	AF8			
B7	VREFB7N2	GND			AF7			
B7	VREFB7N2	nCEO		nCEO	AF9			
B15		GXB_RX11n			AM2			
B15		GXB_RX11p			AM1			
B15		GXB_TX11n			AP5			
B15		GXB_TX11p			AP4			
B15		GXB_RX10n			AK2			
B15		GXB_RX10p			AK1			
B15		GXB_TX10n			AM5			
B15		GXB_TX10p			AM4			
B15		RREFB15			AH4			
B15		REFCLK0_B15n			AK5			
B15		REFCLK0_B15p			AK4			
B15		REFCLK1_B15n			AH2			
B15		REFCLK1_B15p			AH1			
		VCCA			AC11			
		VCCA			AA8			
		VCCA			AC9			
B15		GXB_RX8n			AF2			
B15		GXB_RX8p			AF1			
B15		GXB_TX8n			AF5			
B15		GXB_TX8p			AF4			
B15		GXB_RX9n			AD2			
B15		GXB_RX9p			AD1			
B15		GXB_TX9n			AD5			
B15		GXB_TX9p			AD4			
NC		NC			W7			
NC		NC			W8			
		VCCA			W12			
B14		GXB_RX7n			AB2			
B14		GXB_RX7p			AB1			
B14		GXB_TX7n			AB5			
B14		GXB_TX7p			AB4			
B14		GXB_RX6n			Y2			
B14		GXB_RX6p			Y1			
B14		GXB_TX6n			Y5			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B14		GXB_TX6p			Y4			
B14		RREFB14			V4			
B14		REFCLK0_B14n			V2			
B14		REFCLK0_B14p			V1			
B14		REFCLK1_B14n			U7			
B14		REFCLK1_B14p			U6			
		VCCA			W11			
		VCCA			U8			
		VCCA			W9			
B14		GXB_RX4n			R2			
B14		GXB_RX4p			R1			
B14		GXB_TX4n			R5			
B14		GXB_TX4p			R4			
B14		GXB_RX5n			N2			
B14		GXB_RX5p			N1			
B14		GXB_TX5n			N5			
B14		GXB_TX5p			N4			
B13		GXB_RX3n			L2			
B13		GXB_RX3p			L1			
B13		GXB_TX3n			L5			
B13		GXB_TX3p			L4			
B13		GXB_RX2n			J2			
B13		GXB_RX2p			J1			
B13		GXB_TX2n			J5			
B13		GXB_TX2p			J4			
B13		RREFB13			G4			
B13		REFCLK0_B13n			G2			
B13		REFCLK0_B13p			G1			
B13		REFCLK1_B13n			E5			
B13		REFCLK1_B13p			E4			
		VCCA			R11			
		VCCA			N8			
		VCCA			R9			
B13		GXB_RX0n			E2			
B13		GXB_RX0p			E1			
B13		GXB_TX0n			C5			
B13		GXB_TX0p			C4			
B13		GXB_RX1n			C2			
B13		GXB_RX1p			C1			
B13		GXB_TX1n			A5			
B13		GXB_TX1p			A4			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		TEMPDIODEp			J8			
		TEMPDIODEn			J7			
B4	VREFB4N0	TDO		TDO	H10			
B4	VREFB4N0	MSEL3		MSEL3	H11			
B4	VREFB4N0	MSEL2		MSEL2	J10			
B4	VREFB4N0	MSEL1		MSEL1	J9			
B4	VREFB4N0	MSEL0		MSEL0	K10			
B4	VREFB4N0	IO			M13			
B4	VREFB4N0	IO			L13			
B4	VREFB4N0	IO	RUP4		J11			
B4	VREFB4N0	IO	RDN4		K11			
B4	VREFB4N0	IO			H13			
B4	VREFB4N0	IO			H14			
B4	VREFB4N0	IO	DQS0T		D7	DQS0T		
B4	VREFB4N0	IO	DQ0T		F7	DQ0T		
B4	VREFB4N0	IO	DQ0T		G7	DQ0T		
B4	VREFB4N0	IO	DQ0T		H8	DQ0T		
B4	VREFB4N0	IO			C7			
B4	VREFB4N0	IO	DQ0T		A7	DQ0T		
B4	VREFB4N0	IO			M15			
B4	VREFB4N0	VREFB4N0	VREFB4N0		E10			
B4	VREFB4N0	IO	DQS1T		D8			
B4	VREFB4N0	IO	DQ1T		B8	DQ0T		
B4	VREFB4N0	IO	DQ1T		E8	DQ0T		
B4	VREFB4N0	IO	DQ1T		F8	DQ0T		
B4	VREFB4N0	IO			C8	DQ0T		
B4	VREFB4N0	IO	DQ1T		A8	DQ0T		
B4	VREFB4N0	IO			L14			
B4	VREFB4N0	IO	DQS2T		D9	DQS1T		
B4	VREFB4N0	IO	DQ2T		F9	DQ1T	DQ0T	DQ0T
B4	VREFB4N0	IO	DQ2T		G8	DQ1T	DQ0T	DQ0T
B4	VREFB4N0	IO	DQ2T		G9	DQ1T	DQ0T	DQ0T
B4	VREFB4N0	IO			C9		DQ0T	DQ0T
B4	VREFB4N0	IO	DQ2T		A9	DQ1T	DQ0T	DQ0T
B4	VREFB4N0	IO			J13			
B4	VREFB4N1	IO	DQS3T		D10		DQS0T	
B4	VREFB4N1	IO	DQ3T		B10	DQ1T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ3T		F10	DQ1T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ3T		G10	DQ1T	DQ0T	DQ0T
B4	VREFB4N1	IO			C10	DQ1T		DQ0T
B4	VREFB4N1	IO	DQ3T		A10	DQ1T	DQ0T	DQ0T

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B4	VREFB4N1	IO			N17			
B4	VREFB4N1	IO			M16			
B4	VREFB4N1	IO	DQS4T		D11	DQS2T		
B4	VREFB4N1	IO	DQ4T		B11	DQ2T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ4T		E11	DQ2T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ4T		F11	DQ2T	DQ0T	DQ0T
B4	VREFB4N1	IO			C11		DQ0T	DQ0T
B4	VREFB4N1	IO	DQ4T		A11	DQ2T	DQ0T	DQ0T
B4	VREFB4N1	IO			J14			
B4	VREFB4N1	IO	DQS5T		D12			DQS0T
B4	VREFB4N1	IO	DQ5T		F12	DQ2T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ5T		G12	DQ2T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ5T		G11	DQ2T	DQ0T	DQ0T
B4	VREFB4N1	VREFB4N1	VREFB4N1		E13			
B4	VREFB4N1	IO			C12	DQ2T	DQ0T	
B4	VREFB4N1	IO	DQ5T		A12	DQ2T		
B4	VREFB4N1	IO			N18			
B4	VREFB4N1	IO	DQS6T		D13	DQS3T		
B4	VREFB4N1	IO	DQ6T		B13	DQ3T	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ6T		F13	DQ3T	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ6T		G13	DQ3T	DQ1T	DQ0T
B4	VREFB4N1	IO			C13		DQ1T	DQ0T
B4	VREFB4N1	IO	DQ6T		A13	DQ3T	DQ1T	DQ0T
B4	VREFB4N1	IO			M17			
B4	VREFB4N1	IO			N19			
B4	VREFB4N1	IO	DQS7T		D14		DQS1T	
B4	VREFB4N1	IO	DQ7T		B14	DQ3T	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ7T		F14	DQ3T	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ7T		E14	DQ3T	DQ1T	DQ0T
B4	VREFB4N2	IO			C14	DQ3T		DQ0T
B4	VREFB4N2	IO	DQ7T		A14	DQ3T	DQ1T	DQ0T
B4	VREFB4N2	IO			M19			
B4	VREFB4N2	IO	DQS8T		D15	DQS4T		
B4	VREFB4N2	IO	DQ8T		A15	DQ4T	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ8T		F15	DQ4T	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ8T		G15	DQ4T	DQ1T	DQ0T
B4	VREFB4N2	IO			C15		DQ1T	DQ0T
B4	VREFB4N2	IO	DQ8T		G14	DQ4T	DQ1T	DQ0T
B4	VREFB4N2	IO			F19			
B4	VREFB4N2	IO	DQS9T		C16			
B4	VREFB4N2	IO	DQ9T		A16	DQ4T	DQ1T	DQ0T

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B4	VREFB4N2	IO	DQ9T		B16	DQ4T	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ9T		F16	DQ4T	DQ1T	
B4	VREFB4N2	VREFB4N2	VREFB4N2		E16			
B4	VREFB4N2	IO			D16	DQ4T	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ9T		G16	DQ4T		
B4	VREFB4N2	IO			G18			
B4	VREFB4N2	IO			F18			
B9	VREFB4N2	IO	PLL5_FBn/OUT2n		F17			
B9	VREFB4N2	IO	PLL5_FBp/OUT2p		E17			
B9	VREFB4N2	IO	PLL5_OUT0n		B17			
B9	VREFB4N2	IO	PLL5_OUT0p		A17			
B9	VREFB4N2	IO	PLL5_OUT1n		D17			
B9	VREFB4N2	IO	PLL5_OUT1p		C17			
B4	VREFB4N2	IO	CLK12n		A19			
B4	VREFB4N2	IO	CLK12p		A18			
B4	VREFB4N2	IO	CLK13n		D18			
B4	VREFB4N2	IO	CLK13p		C18			
B9		VCC_PLL5_OUT			H16			
		VCCD_PLL5			H17			
		VCCA_PLL5			K16			
		GNDA_PLL5			J16			
		GNDA_PLL5			J17			
		GNDA_PLL11			J18			
		GNDA_PLL11			K18			
		VCCA_PLL11			K17			
		VCCD_PLL11			J19			
B11		VCC_PLL11_OUT			K20			
B3	VREFB3N0	IO	CLK14p		B19			
B3	VREFB3N0	IO	CLK14n		C19			
B3	VREFB3N0	IO	CLK15p		D19			
B3	VREFB3N0	IO	CLK15n		E19			
B11	VREFB3N0	IO	PLL11_OUT0p		A20			
B11	VREFB3N0	IO	PLL11_OUT0n		B20			
B11	VREFB3N0	IO	PLL11_OUT1p		C20			
B11	VREFB3N0	IO	PLL11_OUT1n		D20			
B11	VREFB3N0	IO	PLL11_FBp/OUT2p		E20			
B11	VREFB3N0	IO	PLL11_FBn/OUT2n		F20			
B3	VREFB3N0	IO		PGM2	G20			
B3	VREFB3N0	IO		PGM1	H20			
B3	VREFB3N0	IO		PGM0	H22			
B3	VREFB3N0	IO		ASDO	N21			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B3	VREFB3N0	IO		nCSO	G21			
B3	VREFB3N0	IO		CRC_ERROR	G22			
B3	VREFB3N0	IO		DATA0	J20			
B3	VREFB3N0	IO		DATA1	J22			
B3	VREFB3N0	VREFB3N0	VREFB3N0		E22			
B3	VREFB3N0	IO	DQS10T		D22	DQS5T		
B3	VREFB3N0	IO	DQ10T		C21	DQ5T	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ10T		A21	DQ5T	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ10T		F21	DQ5T	DQ2T	DQ1T
B3	VREFB3N0	IO			D21		DQ2T	DQ1T
B3	VREFB3N0	IO	DQ10T		F22	DQ5T	DQ2T	DQ1T
B3	VREFB3N0	IO			M21			
B3	VREFB3N0	IO			G23			
B3	VREFB3N0	IO			M22			
B3	VREFB3N0	IO	DQS11T		C22		DQS2T	
B3	VREFB3N0	IO	DQ11T		A22	DQ5T	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ11T		B22	DQ5T	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ11T		F23	DQ5T	DQ2T	DQ1T
B3	VREFB3N0	IO			D23	DQ5T		DQ1T
B3	VREFB3N0	IO	DQ11T		E23	DQ5T	DQ2T	DQ1T
B3	VREFB3N0	IO			L22			
B3	VREFB3N1	IO			G24			
B3	VREFB3N1	IO			K22			
B3	VREFB3N1	IO	DQS12T		C23	DQS6T		
B3	VREFB3N1	IO	DQ12T		B23	DQ6T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ12T		A23	DQ6T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ12T		D24	DQ6T	DQ2T	DQ1T
B3	VREFB3N1	IO			C24		DQ2T	DQ1T
B3	VREFB3N1	IO	DQ12T		F24	DQ6T	DQ2T	DQ1T
B3	VREFB3N1	IO			M23			
B3	VREFB3N1	IO			L23			
B3	VREFB3N1	IO	DQS13T		B25			DQS1T
B3	VREFB3N1	IO	DQ13T		A24	DQ6T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ13T		A25	DQ6T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ13T		F25	DQ6T	DQ2T	DQ1T
B3	VREFB3N1	IO			C25	DQ6T	DQ2T	
B3	VREFB3N1	IO	DQ13T		D25	DQ6T		
B3	VREFB3N1	VREFB3N1	VREFB3N1		E25			
B3	VREFB3N1	IO			H23			
B3	VREFB3N1	IO			K23			
B3	VREFB3N1	IO	DQS14T		C26	DQS7T		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
B3	VREFB3N1	IO	DQ14T		B26	DQ7T	DQ3T	DQ1T
B3	VREFB3N1	IO	DQ14T		E26	DQ7T	DQ3T	DQ1T
B3	VREFB3N1	IO	DQ14T		F26	DQ7T	DQ3T	DQ1T
B3	VREFB3N1	IO			D26		DQ3T	DQ1T
B3	VREFB3N1	IO	DQ14T		A26	DQ7T	DQ3T	DQ1T
B3	VREFB3N1	IO	DQS15T		B28		DQS3T	
B3	VREFB3N1	IO	DQ15T		A27	DQ7T	DQ3T	DQ1T
B3	VREFB3N1	IO	DQ15T		A28	DQ7T	DQ3T	DQ1T
B3	VREFB3N1	IO	DQ15T		C27	DQ7T	DQ3T	DQ1T
B3	VREFB3N2	IO			C28	DQ7T		DQ1T
B3	VREFB3N2	IO	DQ15T		D27	DQ7T	DQ3T	DQ1T
B3	VREFB3N2	IO			F29			
B3	VREFB3N2	IO	DQS16T		C29	DQS8T		
B3	VREFB3N2	IO	DQ16T		A29	DQ8T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ16T		D28	DQ8T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ16T		E29	DQ8T	DQ3T	DQ1T
B3	VREFB3N2	IO			D29		DQ3T	DQ1T
B3	VREFB3N2	IO	DQ16T		B29	DQ8T	DQ3T	DQ1T
B3	VREFB3N2	IO			K24			
B3	VREFB3N2	IO	DQS17T		A31			
B3	VREFB3N2	IO	DQ17T		A30	DQ8T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ17T		A32	DQ8T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ17T		B32	DQ8T	DQ3T	
B3	VREFB3N2	IO			B31	DQ8T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ17T		C30	DQ8T		
B3	VREFB3N2	IO			J27			
B3	VREFB3N2	VREFB3N2	VREFB3N2		E28			
B3	VREFB3N2	IO			G29			
B3	VREFB3N2	IO			H28			
B3	VREFB3N2	IO		DATA2	G25			
B3	VREFB3N2	IO		DATA3	F27			
B3	VREFB3N2	IO		DATA4	H25			
B3	VREFB3N2	IO		DATA5	G27			
B3	VREFB3N2	IO		DATA6	G26			
B3	VREFB3N2	IO		DATA7	H26			
B3	VREFB3N2	IO		RDYnBSY	F28			
B3	VREFB3N2	IO		INIT_DONE	G28			
B3	VREFB3N2	nSTATUS		nSTATUS	D31			
B3	VREFB3N2	nCE		nCE	D30			
B3	VREFB3N2	DCLK		DCLK	C32			
B3	VREFB3N2	CONF_DONE		CONF_DONE	C31			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		VCCIO2			P25			
		VCCIO2			P26			
		VCCIO2			U25			
		VCCIO2			U26			
		VCCIO1			AC25			
		VCCIO1			AC26			
		VCCIO1			Y25			
		VCCIO1			Y26			
		VCCIO8			AE19			
		VCCIO8			AE21			
		VCCIO8			AF21			
		VCCIO8			AG19			
		VCCIO7			AE12			
		VCCIO7			AE15			
		VCCIO7			AF12			
		VCCIO7			AF15			
		VCCT_B15			AA10			
		VCCT_B15			Y10			
		VCCH_B15			AA11			
		VCCH_B15			Y11			
		VCCR			AA9			
		VCCR			Y9			
		VCCA			Y8			
		VCCL_B15			AB8			
		VCCT_B13			M10			
		VCCT_B13			N10			
		VCCH_B13			M11			
		VCCH_B13			N11			
		VCCR			M9			
		VCCR			N9			
		VCCA			M8			
		VCCL_B13			P8			
		VCCT_B14			T10			
		VCCT_B14			U10			
		VCCH_B14			T11			
		VCCH_B14			U11			
		VCCR			T9			
		VCCR			U9			
		VCCA			T8			
		VCCL_B14			V8			
		VCCP			AA12			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		VCCP			Y12			
		VCCP			M12			
		VCCP			N12			
		VCCP			T12			
		VCCP			U12			
		VCCIO4			J12			
		VCCIO4			J15			
		VCCIO4			K12			
		VCCIO4			K15			
		VCCIO3			H19			
		VCCIO3			J21			
		VCCIO3			K19			
		VCCIO3			K21			
		VCCINT			AA14			
		VCCINT			AA16			
		VCCINT			AA18			
		VCCINT			AA20			
		VCCINT			AA22			
		VCCINT			P15			
		VCCINT			P17			
		VCCINT			P19			
		VCCINT			P21			
		VCCINT			R14			
		VCCINT			R16			
		VCCINT			R18			
		VCCINT			R20			
		VCCINT			R22			
		VCCINT			T13			
		VCCINT			T15			
		VCCINT			T17			
		VCCINT			T19			
		VCCINT			T21			
		VCCINT			U14			
		VCCINT			U16			
		VCCINT			U18			
		VCCINT			U20			
		VCCINT			U22			
		VCCINT			V13			
		VCCINT			V15			
		VCCINT			V17			
		VCCINT			V19			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		VCCINT			V21			
		VCCINT			W14			
		VCCINT			W16			
		VCCINT			W18			
		VCCINT			W20			
		VCCINT			W22			
		VCCINT			Y15			
		VCCINT			Y17			
		VCCINT			Y19			
		VCCINT			Y21			
		GND			A33			
		GND			T24			
		GND			T27			
		GND			T30			
		GND			T33			
		GND			V24			
		GND			AA24			
		GND			AA27			
		GND			AA30			
		GND			AA33			
		GND			V27			
		GND			V30			
		GND			V33			
		GND			AB19			
		GND			AC12			
		GND			AD7			
		GND			AD8			
		GND			AD9			
		GND			AD10			
		GND			AD11			
		GND			AD12			
		GND			AD15			
		GND			AD18			
		GND			AD21			
		GND			AD24			
		GND			AD27			
		GND			AD30			
		GND			AD33			
		GND			AG7			
		GND			AG9			
		GND			AG12			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		GND			AG15			
		GND			AG17			
		GND			AG18			
		GND			AG21			
		GND			AG24			
		GND			AG27			
		GND			AG30			
		GND			P33			
		GND			AG33			
		GND			AK7			
		GND			AK9			
		GND			AK12			
		GND			AK15			
		GND			AK18			
		GND			AK21			
		GND			AK24			
		GND			AK27			
		GND			AK30			
		GND			AK33			
		GND			AN7			
		GND			AN9			
		GND			AN12			
		GND			AN15			
		GND			AN18			
		GND			AN21			
		GND			AN24			
		GND			AN27			
		GND			AN30			
		GND			AN33			
		GND			AN34			
		GND			AP33			
		GND			B7			
		GND			B9			
		GND			B12			
		GND			B15			
		GND			B18			
		GND			B21			
		GND			B24			
		GND			B27			
		GND			B30			
		GND			B33			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		GND			B34			
		GND			E7			
		GND			E9			
		GND			E12			
		GND			E15			
		GND			A2			
		GND			A3			
		GND			A6			
		GND			AA1			
		GND			AA2			
		GND			AA3			
		GND			AA4			
		GND			AA5			
		GND			AA6			
		GND			AA7			
		GND			AB3			
		GND			AB6			
		GND			AB7			
		GND			AB9			
		GND			AB10			
		GND			AB11			
		GND			AB12			
		GND			AC1			
		GND			AC2			
		GND			AC3			
		GND			AC4			
		GND			AC5			
		GND			AC6			
		GND			AC7			
		GND			AC8			
		GND			AD3			
		GND			AD6			
		GND			AE1			
		GND			AE2			
		GND			AE3			
		GND			AE4			
		GND			AE5			
		GND			AE6			
		GND			AF3			
		GND			AF6			
		GND			AG1			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		GND			AG2			
		GND			AG3			
		GND			AG4			
		GND			AG5			
		GND			AG6			
		GND			AH3			
		GND			AH5			
		GND			AH6			
		GND			AJ1			
		GND			AJ2			
		GND			AJ3			
		GND			AJ4			
		GND			AJ5			
		GND			AJ6			
		GND			AK3			
		GND			AK6			
		GND			AL1			
		GND			AL2			
		GND			AL3			
		GND			AL4			
		GND			AL5			
		GND			AL6			
		GND			AM3			
		GND			AM6			
		GND			AN1			
		GND			AN2			
		GND			AN3			
		GND			AN4			
		GND			AN5			
		GND			AN6			
		GND			AP2			
		GND			AP3			
		GND			AP6			
		GND			B1			
		GND			B2			
		GND			B3			
		GND			B4			
		GND			B5			
		GND			B6			
		GND			C3			
		GND			C6			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		GND			D1			
		GND			D2			
		GND			D3			
		GND			D4			
		GND			D5			
		GND			D6			
		GND			E3			
		GND			E6			
		GND			F1			
		GND			F2			
		GND			F3			
		GND			F4			
		GND			F5			
		GND			F6			
		GND			G3			
		GND			G5			
		GND			G6			
		GND			H1			
		GND			H2			
		GND			H3			
		GND			H4			
		GND			H5			
		GND			H6			
		GND			J3			
		GND			J6			
		GND			K1			
		GND			K2			
		GND			K3			
		GND			K4			
		GND			K5			
		GND			K6			
		GND			L3			
		GND			L6			
		GND			M1			
		GND			M2			
		GND			M3			
		GND			M4			
		GND			M5			
		GND			M6			
		GND			M7			
		GND			N3			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		GND			N6			
		GND			N7			
		GND			P1			
		GND			P2			
		GND			P3			
		GND			P4			
		GND			P5			
		GND			P6			
		GND			P7			
		GND			P9			
		GND			P10			
		GND			P11			
		GND			P12			
		GND			R3			
		GND			R6			
		GND			R7			
		GND			R8			
		GND			T1			
		GND			T2			
		GND			T3			
		GND			T4			
		GND			T5			
		GND			T6			
		GND			T7			
		GND			U1			
		GND			U2			
		GND			U3			
		GND			U4			
		GND			U5			
		GND			V3			
		GND			V5			
		GND			V6			
		GND			V7			
		GND			V9			
		GND			V10			
		GND			V11			
		GND			V12			
		GND			W1			
		GND			W2			
		GND			W3			
		GND			W4			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		GND			W5			
		GND			W6			
		GND			Y3			
		GND			Y6			
		GND			Y7			
		GND			AC10			
		GND			W10			
		GND			R10			
		GND			E18			
		GND			E21			
		GND			E24			
		GND			E27			
		GND			E30			
		GND			E33			
		GND			G17			
		GND			H7			
		GND			H9			
		GND			H12			
		GND			H15			
		GND			H18			
		GND			H21			
		GND			H24			
		GND			H27			
		GND			H30			
		GND			H33			
		GND			K7			
		GND			K8			
		GND			K9			
		GND			L10			
		GND			L11			
		GND			L12			
		GND			L15			
		GND			L18			
		GND			L21			
		GND			L24			
		GND			L27			
		GND			L30			
		GND			L33			
		GND			N13			
		GND			N14			
		GND			N15			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		GND			N16			
		GND			N20			
		GND			P24			
		GND			P27			
		GND			P30			
		GND			AA13			
		GND			AA15			
		GND			AA17			
		GND			AA19			
		GND			AA21			
		GND			P14			
		GND			P16			
		GND			P18			
		GND			P20			
		GND			R13			
		GND			R15			
		GND			R17			
		GND			R19			
		GND			R21			
		GND			T14			
		GND			T16			
		GND			T18			
		GND			T20			
		GND			T22			
		GND			U13			
		GND			U15			
		GND			U17			
		GND			U19			
		GND			U21			
		GND			V14			
		GND			V16			
		GND			V18			
		GND			V20			
		GND			W13			
		GND			W15			
		GND			W17			
		GND			W19			
		GND			W21			
		GND			Y14			
		GND			Y16			
		GND			Y18			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		GND			Y20			
		GND			Y22			
		GND			AB13			
		GND			AB14			
		GND			AB15			
		GND			P13			
		GND			P22			
		GND			R12			
		GND			V22			
		GND			Y13			
		VCCPD2			R24			
		VCCPD2			R25			
		VCCPD1			W24			
		VCCPD1			W25			
		VCCPD8			AD19			
		VCCPD8			AD20			
		VCCPD7			AD16			
		VCCPD7			AD17			
		VCCPD4			L16			
		VCCPD4			L17			
		VCCPD3			L19			
		VCCPD3			L20			
		NC			L7			
		NC			L8			
		NC			L9			
		NC			AK29			
		NC			AF23			
		NC			AG22			
		NC			AH24			
		NC			AB18			
		NC			AH17			
		NC			AG14			
		NC			AF14			
		NC			AF13			
		NC			AE11			
		NC			M14			
		NC			K13			
		NC			K14			
		NC			M18			
		NC			G19			
		NC			M20			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX90EF1152	x8/x9 Mode	x16/x18 Mode	x32/x36 Mode
						DQ group for DQS mode	DQ group for DQS mode	DQ group for DQS mode
		NC			N22			
		NC			M24			
		NC			J23			
		NC			J24			

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCINT	Power	1.2 V internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, differential HSTL, differential SSTL, HSTL, and SSTL I/O standards.
VCCIO[1..4,7,8]	Power	I/O supply voltage pins for banks 1-4, 7, and 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5 V, 1.8 V, 2.5 V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCPD[1..4,7,8]	Power	Dedicated power pins. This 3.3 V supply is used to power the I/O pre-drivers and the 3.3 V/2.5 V buffers of the configuration input pins and the JTAG pins. VCCPD powers the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS and CLKUSR.
GND	Ground	Device ground pins.
VREFB[1..4,7,8]N[2..0]	Input	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All of the VREF pins within a bank are shorted together. If VREF pins are not used, designers should connect them to either VCC or GND.
VCC_PLL5_OUT	Power	External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p, and PLL5_FBn/OUT2n. This pin should be connected to the voltage level of the target device which PLL5 in bank 9 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCC_PLL6_OUT	Power	External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p, and PLL6_FBn/OUT2n. This pin should be connected to the voltage level of the target device which PLL6 in bank 10 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCC_PLL11_OUT	Power	External clock output VCCIO power for PLL11 clock outputs PLL11_OUT[1..0]p, PLL11_OUT[1..0]n, PLL11_FBp/OUT2p, and PLL11_FBn/OUT2n. This pin should be connected to the voltage level of the target device which PLL11 in bank 11 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCC_PLL12_OUT	Power	External clock output VCCIO power for PLL12 clock outputs PLL12_OUT[1..0]p, PLL12_OUT[1..0]n, PLL12_FBp/OUT2p, and PLL12_FBn/OUT2n. This pin should be connected to the voltage level of the target device which PLL12 in bank 12 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCCA_PLL[1,2,5..8,11,12]	Power	1.2 V analog power for PLLs[1,2,5..8,11,12].
VCCD_PLL[1,2,5..8,11,12]	Power	1.2 V digital power for PLLs[1,2,5..8,11,12].
GNDA_PLL[1,2,5..8,11,12]	Ground	Analog ground for PLLs[1,2,5..8,11,12].
NC	No Connect	Do not drive any signals into this pin.
RUP4	I/O, Input	Reference pin for banks 3 and 4. The external precision resistor Rup must be connected to the designated RUP pin within bank 4. If not required, this pin is a regular I/O pin.
RDN4	I/O, Input	Reference pin for banks 3 and 4. The external precision resistor Rdn must be connected to the designated RDN pin within bank 4. If not required, this pin is a regular I/O pin.
RUP7	I/O, Input	Reference pin for banks 7 and 8. The external precision resistor Rup must be connected to the designated RUP pin within bank 7. If not required, this pin is a regular I/O pin.
RDN7	I/O, Input	Reference pin for banks 7 and 8. The external precision resistor Rdn must be connected to the designated RDN pin within bank 7. If not required, this pin is a regular I/O pin.
	Dedicated Configuration/JTAG Pins	

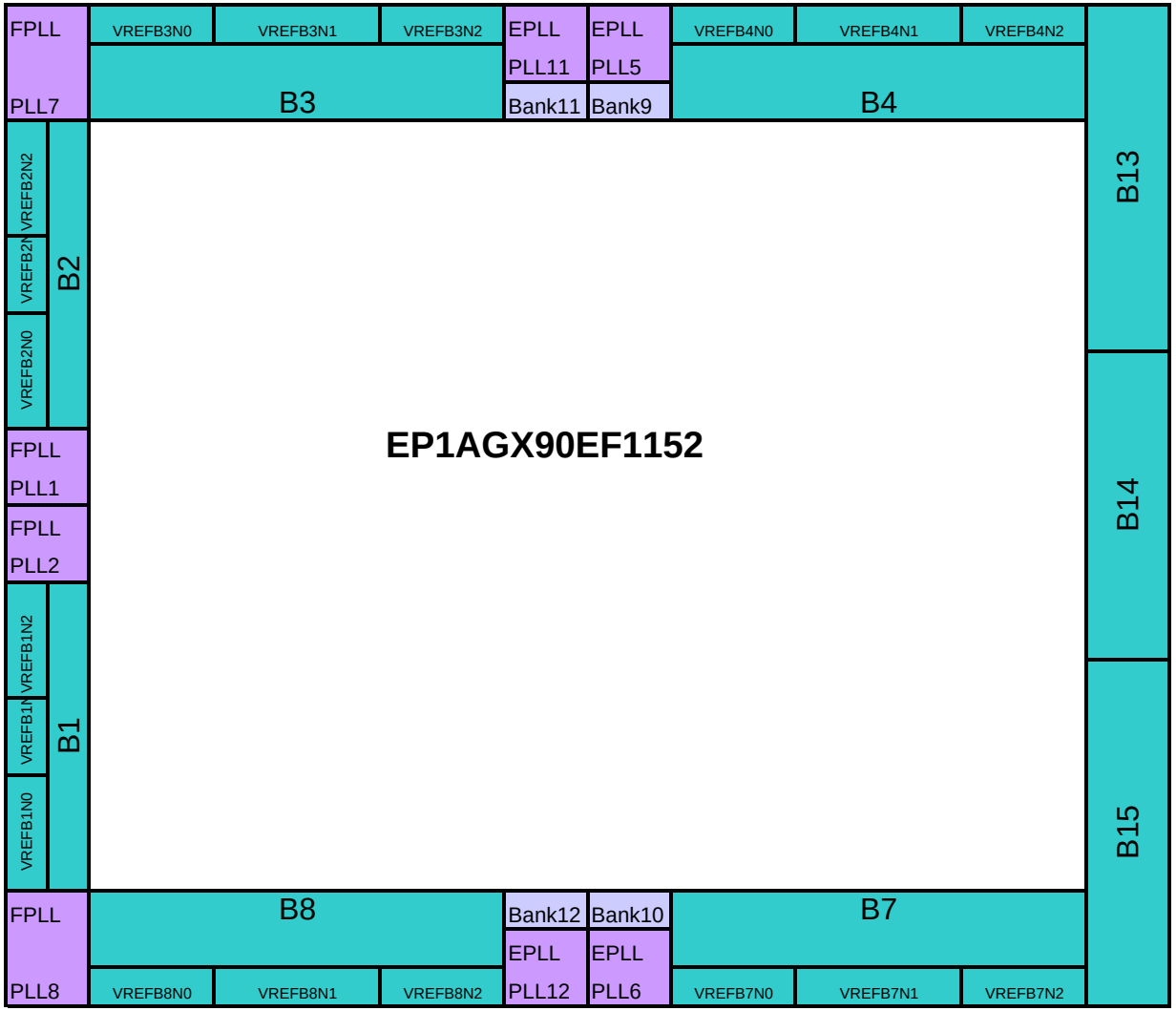
Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns them on.
VCCSEL	Input	Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input), DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8 V/1.5 V input buffer is powered by VCCIO. A logic high (VCCPD) selects the 1.8 V/1.5 V input buffer, while a logic low selects the 3.3 V/2.5 V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX II device/microprocessor with flash memory.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Arria GX device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Arria GX device.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the Arria GX device. In AS mode, DCLK is an output from the Arria GX device that provides timing for the configuration interface.
MSEL[3..0]	Input	Configuration input pins that set the Arria GX device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration Done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects a POR time of about 12 ms and a logic low selects POR time of about 100 ms.
Optional/Dual-Purpose Configuration Pins		
nCSO	I/O Output	Output control signal from the Arria GX FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	I/O Output	Control signal from the Arria GX FPGA to the serial configuration device in AS mode used to read out configuration data.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[6..1]	I/O, Input	Dual-purpose configuration input data pins. The DATA[7..0] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
DATA7	I/O, Bidirectional	In the PPA configuration scheme, the DATA7 pin presents the RDYnBSY signal after the nRS signal has been strobed low.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
nCS, CS	I/O, Input	These are chip-select inputs that enable the Arria GX device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. A low input directs the device to drive the RDYnBSY signal on the DATA7 pin. In non-PPA schemes, it functions as a user I/O during configuration, which means it is tri-stated. This pin can be used as a user I/O pin after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration.
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the memory (either flash or enhanced configuration device) when using a remote system update mode. When not using remote update or local update configuration modes, these pins are user I/O pins.
RUnLU	I/O, Input	Input that selects between remote update and local update. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects remote update and a logic low selects local update. When not using remote update or local update configuration modes, this pin is available as general-purpose user I/O pin.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
Clock and PLL Pins		
CLK[1,3]p	Clock, Input	Dedicated clock input pins 1 and 3 that can also be used for data inputs.
CLK[1,3]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
CLK[2,0]p/DIFFIO_RX_C[1,0]p	I/O, Clock	These pins can be used as I/O pins, clock input pins, or the positive terminal data pins of differential receiver channels.
CLK[2,0]n/DIFFIO_RX_C[1,0]n	I/O, Clock	These pins can be used as I/O pins, the negative clock input pins for differential clock input, or the negative data pins of differential receiver channels.
CLK[4-7,12-15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins.
CLK[4-7,12-15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs.
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs.
FPLL[8..7]CLKp	Clock, Input	Dedicated positive clock inputs for fast PLLs (PLLs 7 and 8) which can also be used for data inputs.
FPLL[8..7]CLKn	Clock, Input	Dedicated negative clock inputs associated with the FPLL[7,8]CLKp pins which can also be used for data inputs.
PLL5_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL5. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL5).
PLL5_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL6_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL6. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL6).
PLL6_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL11_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL11. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL11).
PLL11_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL11. If the clock outputs are single ended, then each pair of pins (i.e., PLL11_OUT0p and PLL11_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL12_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL12. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL12).
PLL12_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL12. If the clock outputs are single ended, then each pair of pins (i.e., PLL12_OUT0p and PLL12_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL[6..5]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, positive external feedback input pins or external clock outputs for PLL[6,5].
PLL[6..5]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative external feedback input PLL[6,5]_FBp or negative terminal clock output pins for differential clock output.
PLL[12..11]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, positive external feedback input pins or positive external clock outputs for PLL[12..11].
PLL[12..11]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative external feedback input PLL[12..11]_FBp or negative external clock output pins for differential clock output.
Dual-Purpose Differential and External Memory Interface Pins		
DIFFIO_RX[50..1]p	IO, Input	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
DIFFIO_RX[50..1]n	IO, Input	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS-compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[51..0]p	IO, Output	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[51..0]n	IO, Output	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS-compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[17..0][T,B]	DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry. The shifted DQS signal can also drive to internal logic.
DQ[17..0][T,B]	DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
Transceiver (I/O Banks) Pins		
VCCP	Power	GX bank [15..13] PCS power. This power is connected to 1.2 V.
VCCR	Power	GX bank [15..13] receiver analog power. This power is connected to 1.2 V.
VCCT_B[15..13]	Power	GX bank [15..13] transmitter analog power. This power is connected to 1.2 V.
VCCA	Power	GX bank [15..13] analog power. This power is connected to 3.3 V.
VCCH_B[15..13]	Power	GX bank [15..13] transmitter driver analog power. This power is connected to 1.2 V or 1.5 V.
VCCL_B[15..13]	Power	GX bank [15..13] VCO analog power. This power is connected to 1.2 V.
GXB_RX[11..0]p	I, Input	High-speed positive differential receiver channels.
GXB_RX[11..0]n	I, Input	High-speed negative differential receiver channels.
GXB_TX[11..0]p	O,Output	High-speed positive differential transmitter channel.
GXB_TX[11..0]n	O,Output	High-speed negative differential transmitter channels.
REFCLK[0,1]_B[15..13]p	I, Input	High-speed differential I/O reference clock positive. This pin is powered by 1.2 V VCCT_B[15..13].
REFCLK[0,1]_B[15..13]n	I, Input	High-speed differential I/O reference clock negative. This pin is powered by 1.2 V VCCT_B[15..13].
RREFB[15..13]	I, Input	Reference resistor for GX side banks.

Note:
1) These descriptions are created based on the largest density of Arria GX (EP1AGX90E) device.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version	Date	Changes Made
1.0	6/22/2007	Initial release.