ChipWhisperer-Lite arm edition
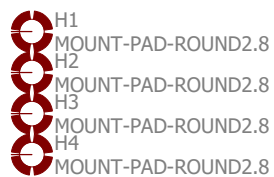
Revision Information

-01 Initial Release (based on -04 cw-lite)
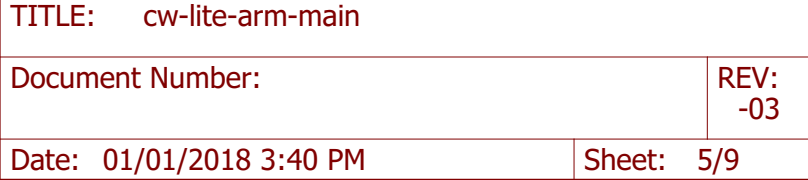
U1

C5 2u2 C8 100n C9 100n C10 100n C11 100n C12 100n
GND
+3V3
C6 4u7 C13 100n C14 100n C15 100n C16 100n C17 100n C18 100n
+3V3
GND

87 VDDCORE_2
83 VDDCORE_3
9 VDDCORE_4
59 VDDCORE_5
34 VDDCORE
53 VDDIN
22 VDDIO_2
36 VDDIO_3
60 VDDIO_4
88 VDDIO
52 VDDOUT
45 VDDBU
1 VDDANA
73 VDDPLL
79 VDDUTMI

PA16/PGMD8 13 — SAM_CS0/7.5F
PA17/PGMD9 14 — TARGET_NRST/7.5G
PA18/PGMD10 17 — TXD0/7.5G
PA19/PGMD11 18 — RXD0/7.5G
PA20/PGMD12 19 — R2 330R — SAM_PDID/8.2L
PA21/PGMD13 20
PA22/PGMD14 5 — TXD2/7.5G
PA23/PGMD15 21 — RXD2/7.5G
PA24 23 — SAM_PDIC/8.2M
PA25 24
PA26 25 — CLK2/7.5H
PA27 96 — USBCK0 — R14 1R — C1 DNM — GND
PA28 84
PA29 85 — PWRON/3.6F
PA30 6 — VBUSDETECT/3.6J
PA31 86

L1 10uH/100mA
+3V3
R15 1R
C4 100n
C3 4u7
GND

42 FWUP
43 ERASE — ERASE/3.1L — GND
44 TST
48 JTAGSEL — GND

51 TDI — TDI/3.2D
56 TCK/SWCLK — TCK/3.2E
57 NRST — NRST/3.2E
54 TDO/TRACESWO — TDO/3.2E

+3V3
C21 100n
GND

2 ADVREF
4 AD12BVREF

PB0 90
PB1 91
PB2 92
PB3 7
PB4 8
PB5 97
PB6 98
PB7 99
PB8 100
PB9 71
PB10 70
PB11 93
PB12 94
PB13 95
PB14 69
PB15 16
PB16 15
PB17 68 — USBSPARE0
PB18 67 — USBSPARE1
PB19 66 — USBRD
PB20 65 — USBCE
PB21 64 — USBALE
PB22 63 — USBSPARE2
PB23 62 — USBWR
PB24 58 — USBCK1 — R1 1R — C2 DNM — GND

USB_AD[0..8]
USB_D[0..7]

26 PA0/PGMNCMD — SAM_CS1/7.5H
27 PA1/PGMRDY — SAM_CS2
28 PA2/PGMNOE — SC_PRESENT
29 PA3/PGMNVALID — SC_RESET/7.5H
30 PA4/PGMM0 — SC_AUX1/7.5H
31 PA5/PGMM1 — SC_AUX2/7.5I
32 PA6/PGMM2
33 PA7/PGMM3
37 PA8/PGMD0 — FPGA_PROGRAM/5.4D
38 PA9/PGMD1 — FPGA_INITB/5.3J
39 PA10/PGMD2 — FPGA_DONE/5.4D
40 PA11/PGMD3
41 PA12/PGMD4
10 PA13/PGMD5 — SAM_MISO/5.3G
11 PA14/PGMD6 — SAM_MOSI/5.6B
12 PA15/PGMD7 — SAM_SCK/5.6B

JP1
+3V3
4
3 RX
2 TX
1
GND

D9 D2
R57 1k R58 1k
GND

3 GNDANA
35 GND_2
46 GNDBU
61 GND_3
72 GNDPLL
82 GNDUTMI
89 GND

47 NRSTB — NRSTB/3.1H
55 TMS/SWDIO — TMS/3.2D
76 DHSDP
77 DHSDM
78 VBG
80 DFSDM — R27 39R
81 DFSDP — R28 39R

D_P/3.8K
D_N/3.8K
GND
R29 6k81 C33 10pF
GNDGND

50 XIN32
49 XOUT32
75 XIN
74 XOUT

+3V3
R62 1R
J7
1 2
3 4
5 6
7 8
SC_RESET/7.5H
CLK2/7.5H
SC_AUX1/7.5I
SC_PRESENT
1k R63 TXD2/7.5G
SC_AUX2/7.5I
+3V3
10k R64
GND

C50 18pF
C51 18pF
Q1
GND

ATSAM3U2CA-AU

VCCIO
U2B3
P4 VCCO_3
P18 VCCO_3
P31 VCCO_3
USB_D6 P35 IO_L1P_3
USB_D7 P34 IO_L1N_VREF_3
USBWR P33 IO_L2P_3
USBSPARE2 P32 IO_L2N_3
USBALE P30 IO_L36P_3
USBCE P29 IO_L36N_3
USBRD P27 IO_L37P_3
USBSPARE1 P26 IO_L37N_3
USBCK1 P24 IO_L41P_GCLK27_3
USBSPARE0 P23 IO_L41N_GCLK26_3
USB_D5 P22 IO_L42P_GCLK25_TRDY2_3
USB_D1 P21 IO_L42N_GCLK24_3
USB_D0 P17 IO_L43P_GCLK23_3
USB_AD4 P16 IO_L43N_GCLK22_IRDY2_3
USB_AD3 P15 IO_L44P_GCLK21_3
USBCK0 P14 IO_L44N_GCLK20_3
USB_AD0 P12 IO_L49P_3
USB_AD1 P11 IO_L49N_3
USB_AD2 P10 IO_L50P_3
P9 IO_L50N_3
USB_D2 P8 IO_L51P_3
USB_D3 P7 IO_L51N_3
USB_D4 P6 IO_L52P_3
USB_AD5 P5 IO_L52N_3
USB_AD6 P2 IO_L83P_3
USB_AD7 P1 IO_L83N_VREF_3
USB_AD8

6SLX9TQG144

TITLE: cw-lite-arm-main
Document Number:
REV: -03
Date: 01/01/2018 3:40 PM
Sheet: 2/9

Switched supplies (required for USB suspend + meeting inrush current limits)

IRLML6402TRPBF

VBUS_SWITCHED/4.7D

To switching reg
for FPGA, ADC, VTarg

C43 100n
C42 10u
GND GND

L4 600R/1A
10n C47
GND

T1
R31 100k

SJ1
JP3
1
2
GND

+5VCLEAN/6.2H

To LNA chip

C41 100n
C40 2u2
GND GND

L5 1k/500mA

R79 1k

C122 DNM
GND

PWRON/2.8E

NOTE: SAM3U defaults to 50k pull-up
on I/O. Need strong pull-down to ensure
system stays off when SAM3U in reset.

T2
IRLML2502

2k R23

GND

+3V3

R17 100k
R18 100k
R19 100k
R20 100k
R21 100k

J3
+3V3

1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20

SAM3 JTAG
SAM-ICE

TDI/2.4G
TMS/2.8L
TCK/2.4G

TDO/2.4G
NRST/2.4G

1k
R16

GND

JP2
1
2
S1

1 3
2 4
RESET

NRSTB/2.8L

GND

VBUS/4.2B

C45 1u
C44 100n
GND GND

L6 600R/1A
C46 10n
GND

R33 47k

VBUSDETECT/2.8E

R34 68k

GND

Erase
JP4
1
2
+3V3

ERASE/2.4F

MICRO-USB-5P-ZX62D-B-5P8-MILLED
J8
1 VCC
2 DM
3 DP
4 ID SHIELD E1*6
5 GND

GND

C48 100n
GND

D_N/2.8L
D_P/2.8L

U6
PRTR5V0U2AX
2 IO1 VCC 4
3 IO2 GND 1

IRLML6402TRPBF

VCCTIO_SWITCHED/8.6K

VCCIO/4.8B

T3

TIOVCC_ON/7.5I

R77 10k

GND

TITLE: cw-lite-arm-main

Document Number:

REV:
-03

Date: 01/01/2018 3:40 PM

Sheet: 3/9

VBUS/3.6H

C39
2u2
GND

U7
IN   OUT
GND
TC1262-3.3VDBTR

+3V3

C38
2u2
GND

GND

LDO Regulator active during USB Suspend

U5
2 RUN1   SW1 4
9 RUN2
3 MODE   VFB1 1
7 VIN
                SW2 8
5 GND
6 GND   VFB2 10
LTC3419EMS
GND

VBUS_SWITCHED/3.7A

C36
22u
GND

L2 3.3uH   +3V3 Switched
R25 6k81
C34
22u
GND

R24
1k5

VCCIO
IO

L3 3.3uH   +1V2 Switched
R30 1k5
C35
22u
GND

R26
1k5
GND

VCCINT
INT

Switching regulator turned off during USB suspend

Shutdown pins not used as require switching +5V
supply anyway for LNA chip, so simply switch off
input to this chip.

H1
MOUNT-PAD-ROUND2.8
H2
MOUNT-PAD-ROUND2.8
H3
MOUNT-PAD-ROUND2.8
H4
MOUNT-PAD-ROUND2.8

TITLE: cw-lite-arm-main

Document Number:

REV:
-03

Date: 01/01/2018 3:40 PM   Sheet: 4/9

CCLK — SAM_SCK/2.3L
DIN — SAM_MOSI/2.3L

BANK3 VCCIO
C52 100n C55 100n C53 100n C61 1u
GND

BANK0 VCCIO
C58 100n C56 100n C59 100n C60 1u
GND

BANK2 VCCIO
C57 100n C54 100n C62 1u
GND

VCCIO R11 10k R12 10k

U2B2
VCCIO
VCCO_2 — P42
VCCO_2 — P63
CMPCS_B_2 — P72
DONE_2 — P71 — FPGA_DONE/2.3K
PROGRAM_B_2 — P37 — FPGA_PROGRAM/2.3J
IO_L1P_CCLK_2 — P70
IO_L1N_M0_CMPMISO_2 — P69 — 1k
IO_L2P_CMPCLK_2 — P67 — GLITCHOUTLP/8.7A M0 DNM R7
IO_L2N_CMPMOSI_2 — P66 — GLITCHOUT/8.7B
IO_L3P_D0_DIN_MISO_MISO1_2 — P65 — R8
IO_L3N_MOSI_CSI_B_MISO0_2 — P64
IO_L12P_D1_MISO2_2 — P62 — VGA_GAIN/6.10J
IO_L12N_D2_MISO3_2 — P61 — VGA_HILOW/6.10I
IO_L13P_M1_2 — P60 — 1k VCCIO
IO_L13N_D10_2 — P59 — ADC_D0 M1 DNM R4
IO_L14P_D11_2 — P58 — ADC_D1
IO_L14N_D12_2 — P57 — ADC_D2
IO_L30P_GCLK1_D13_2 — P56 — ADC_CLK
IO_L30N_GCLK0_USERCCLK_2 — P55
IO_L31P_GCLK31_D14_2 — P51 — SAM_MISO/2.3K
IO_L31N_GCLK30_D15_2 — P50
IO_L48P_D7_2 — P48 — ADC_D3
IO_L48N_RDWR_B_VREF_2 — P47 — ADC_D4
IO_L49P_D3_2 — P46 — ADC_D5
IO_L49N_D4_2 — P45 — ADC_D6
IO_L62P_D5_2 — P44 — ADC_D7
IO_L62N_D6_2 — P43 — ADC_D8
IO_L64P_D8_2 — P41 — ADC_D9
IO_L64N_D9_2 — P40
IO_L65P_INIT_B_2 — P39 — ADC_OR/6.12D
IO_L65N_CSO_B_2 — P38 — FPGA_INITB/2.3K

ADC_D[0..9]

6SLX9TQG144

VCCIO R69 10k R9 10k

R5 1R R6 1R
DNM R71 DNM R70 GND

R22 DNM
C49 100n VCCIO
GND

U9
1 CS   VCC 8
2 MISO HOLD 7
3 WP   SCK 6
4 GND   MOSI 5
SPI_FLASH-X25XXSMD1
GND

U2BVCCAUX VCCIO
VCCAUX — P20
VCCAUX — P36
VCCAUX — P53
VCCAUX — P90
VCCAUX — P129
C20 100n C22 100n C23 100n C24 100n C25 100n C26 2u2
6SLX9TQG144 GND

U2BVCCINT VCCINT
VCCINT — P19
VCCINT — P28
VCCINT — P52
VCCINT — P89
VCCINT — P128
C28 100n C29 100n C30 100n C31 100n C32 100n C27 2u2
6SLX9TQG144 GND

U2BGND
GND — P3
GND — P13
GND — P25
GND — P49
GND — P54
GND — P68
GND — P77
GND — P91
GND — P96
GND — P108
GND — P113
GND — P130
GND — P136
6SLX9TQG144 GND

VCCIO
U2BNA J4
SUSPEND — P73
TCK — P109 — GND 1 +V
TDI — P110 — 2 GND
TDO — P106 — 3 TCK
TMS — P107 — 4 TDO
                5 TDI
                6 TMS
6SLX9TQG144
JTAG Programming/Debug for FPGA
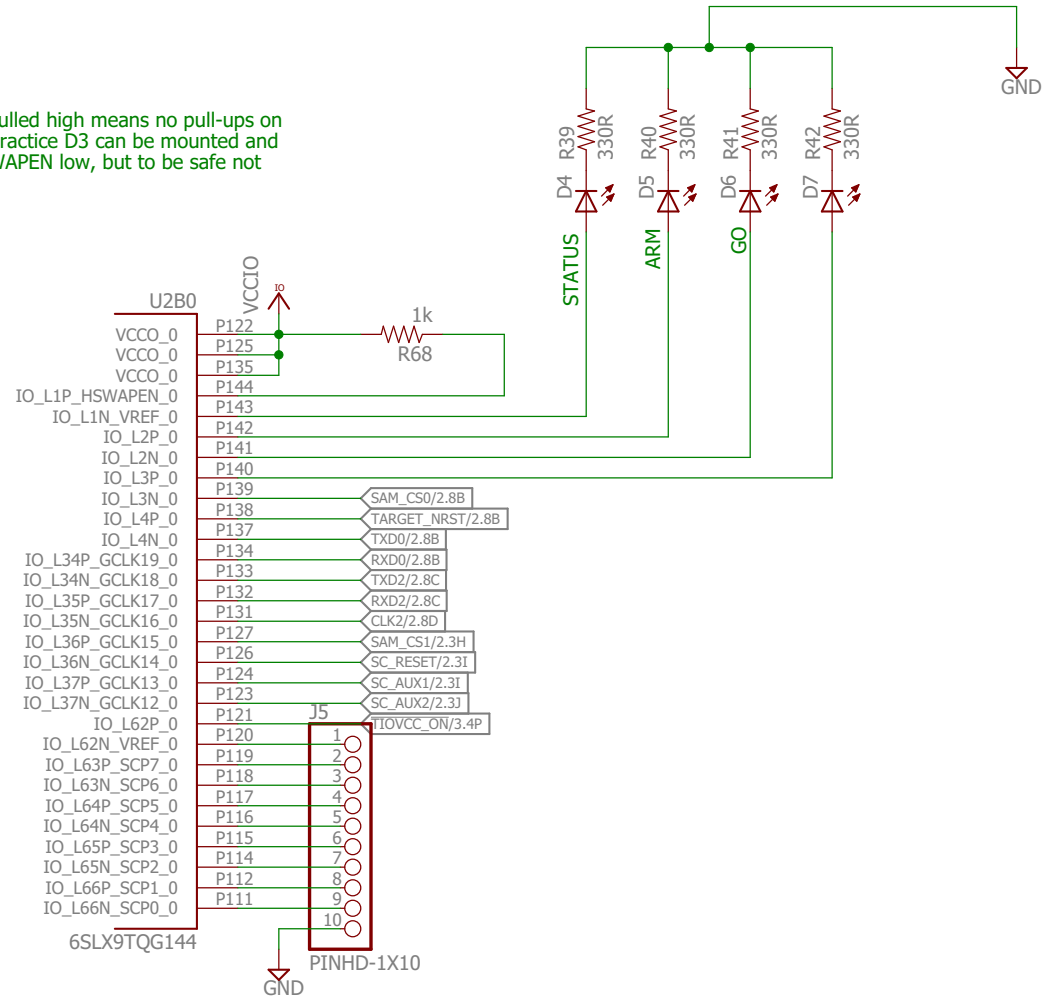
TITLE: cw-lite-arm-main

Document Number:

REV: -03

Date: 01/01/2018 3:40 PM

Sheet: 6/9

HSWAPEN pulled high means no pull-ups on all pins. In practice D3 can be mounted and not pull HSWAPEN low, but to be safe not mounted
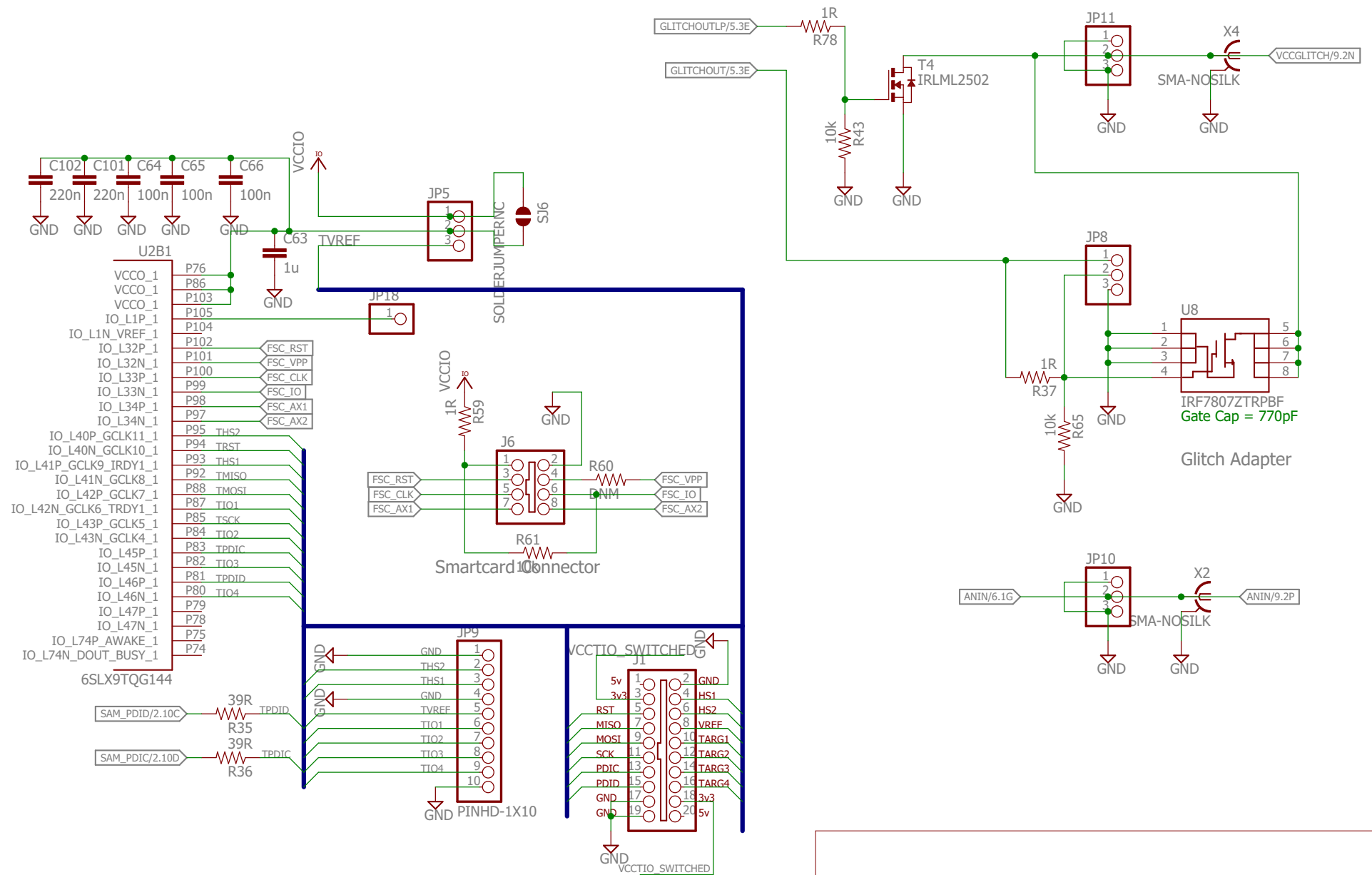
GND

R39 330R
R40 330R
R41 330R
R42 330R

D4
D5
D6
D7

STATUS
ARM
GO

VCCIO
IO

U2B0

VCCO_0	P122	
VCCO_0	P125	
VCCO_0	P135	
IO_L1P_HSWAPEN_0	P144	
IO_L1N_VREF_0	P143	
IO_L2P_0	P142	
IO_L2N_0	P141	
IO_L3P_0	P140	
IO_L3N_0	P139	SAM_CS0/2.8B
IO_L4P_0	P138	TARGET_NRST/2.8B
IO_L4N_0	P137	TXD0/2.8B
IO_L34P_GCLK19_0	P134	RXD0/2.8B
IO_L34N_GCLK18_0	P133	TXD2/2.8C
IO_L35P_GCLK17_0	P132	RXD2/2.8C
IO_L35N_GCLK16_0	P131	CLK2/2.8D
IO_L36P_GCLK15_0	P127	SAM_CS1/2.3H
IO_L36N_GCLK14_0	P126	SC_RESET/2.3I
IO_L37P_GCLK13_0	P124	SC_AUX1/2.3I
IO_L37N_GCLK12_0	P123	SC_AUX2/2.3J
IO_L62P_0	P121	TIOVCC_ON/3.4P
IO_L62N_VREF_0	P120	
IO_L63P_SCP7_0	P119	
IO_L63N_SCP6_0	P118	
IO_L64P_SCP5_0	P117	
IO_L64N_SCP4_0	P116	
IO_L65P_SCP3_0	P115	
IO_L65N_SCP2_0	P114	
IO_L66P_SCP1_0	P112	
IO_L66N_SCP0_0	P111	

6SLX9TQG144

1k
R68

J5
1
2
3
4
5
6
7
8
9
10

PINHD-1X10

GND

SRAM

TITLE: cw-lite-arm-main

Document Number:

REV: -03

Date: 01/01/2018 3:40 PM

Sheet: 7/9

GLITCHOUTLP/5.3E

1R
R78

GLITCHOUT/5.3E

T4
IRLML2502

10k
R43

GND

GND

JP11
1
2
3

GND

X4
SMA-NOSILK

GND

VCCGLITCH/9.2N

VCCIO
IO

C102   C101   C64   C65   C66
220n   220n   100n   100n   100n

GND   GND   GND   GND   GND

C63

GND

1u

TVREF

JP5
1
2
3

SOLDERJUMPERNC

SJ6

U2B1

VCCO_1   P76
VCCO_1   P86
VCCO_1   P103
IO_L1P_1 P105
IO_L1N_VREF_1 P104
IO_L32P_1 P102   FSC_RST
IO_L32N_1 P101   FSC_VPP
IO_L33P_1 P100   FSC_CLK
IO_L33N_1 P99   FSC_IO
IO_L34P_1 P98   FSC_AX1
IO_L34N_1 P97   FSC_AX2
IO_L40P_GCLK11_1 P95   THS2
IO_L40N_GCLK10_1 P94   TRST
IO_L41P_GCLK9_IRDY1_1 P93   THS1
IO_L41N_GCLK8_1 P92   TMISO
IO_L42P_GCLK7_1 P88   TMOSI
IO_L42N_GCLK6_TRDY1_1 P87   TIO1
IO_L43P_GCLK5_1 P85   TSCK
IO_L43N_GCLK4_1 P84   TIO2
IO_L45P_1 P83   TPDIC
IO_L45N_1 P82   TIO3
IO_L46P_1 P81   TPDID
IO_L46N_1 P80   TIO4
IO_L47P_1 P79
IO_L47N_1 P78
IO_L74P_AWAKE_1 P75
IO_L74N_DOUT_BUSY_1 P74

6SLX9TQG144

JP18
1

VCCIO
IO

1R
R59

GND

J6
1   2
3   4
5   6
7   8

FSC_RST
FSC_CLK
FSC_AX1

R60

DNM

R61

Smartcard Connector

FSC_VPP
FSC_IO
FSC_AX2

GND

JP8
1
2
3

U8
1   5
2   6
3   7
4   8

IRF7807ZTRPBF
Gate Cap = 770pF

1R
R37

10k
R65

GND

GND

GND

Glitch Adapter

JP10
1
2
3

X2
SMA-NOSILK

ANIN/6.1G

ANIN/9.2P

GND

GND

SAM_PDID/2.10C

39R
R35

TPDID

SAM_PDIC/2.10D

39R
R36

TPDIC

JP9
GND   1
THS2   2
THS1   3
GND   4
TVREF   5
TIO1   6
TIO2   7
TIO3   8
TIO4   9
10

GND

GND
GND

PINHD-1X10

VCCTIO_SWITCHED

GND

J1
5v   1   2   GND
3v3   3   4   HS1
RST   5   6   HS2
MISO   7   8   VREF
MOSI   9   10   TARG1
SCK   11   12   TARG2
PDIC   13   14   TARG3
PDID   15   16   TARG4
GND   17   18   3v3
GND   19   20   5v

GND

VCCTIO_SWITCHED

TITLE: cw-lite-arm-main

Document Number:

REV:
-03

Date: 01/01/2018 3:40 PM

Sheet: 8/9

Breakaway Section of PCB

TITLE:	cw-lite-arm-main	
Document Number:		REV: -03
Date: 01/01/2018 3:40 PM		Sheet: 9/9