

Schematic

DH electronics GmbH

Project:Avenger

PCB number: 588-100

Date: 14.12.2018

Created: MH

Notes:

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I2C4 Addresses:

PMIC STPMU1A: 0110011 = 0x34

MIPI CSI Bridge: 0010100 = 0x15

HDMI Transmitter: 1111010 = 0x7A

EEPROM (MAC Adress): 1010011 = 0x54



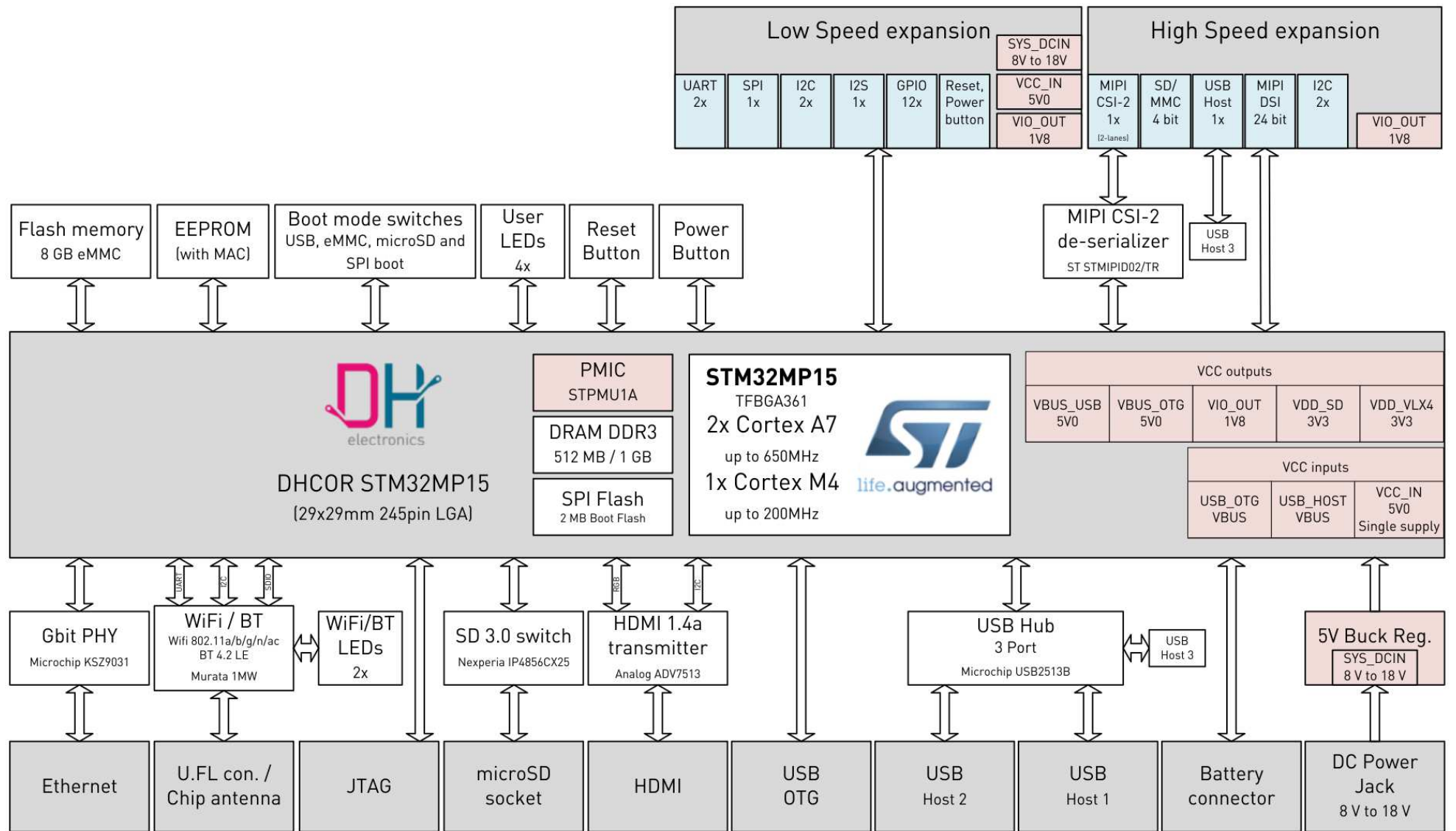
Project: Avenger
Description: Cover sheet

PCB number: 588-100

Revision: R06

Variant: HS00007


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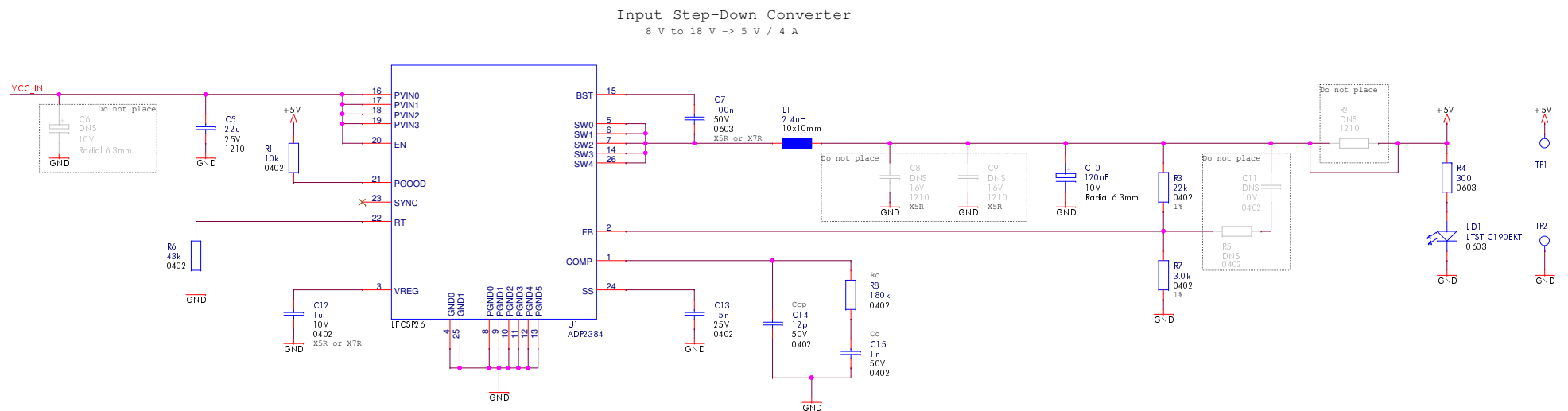
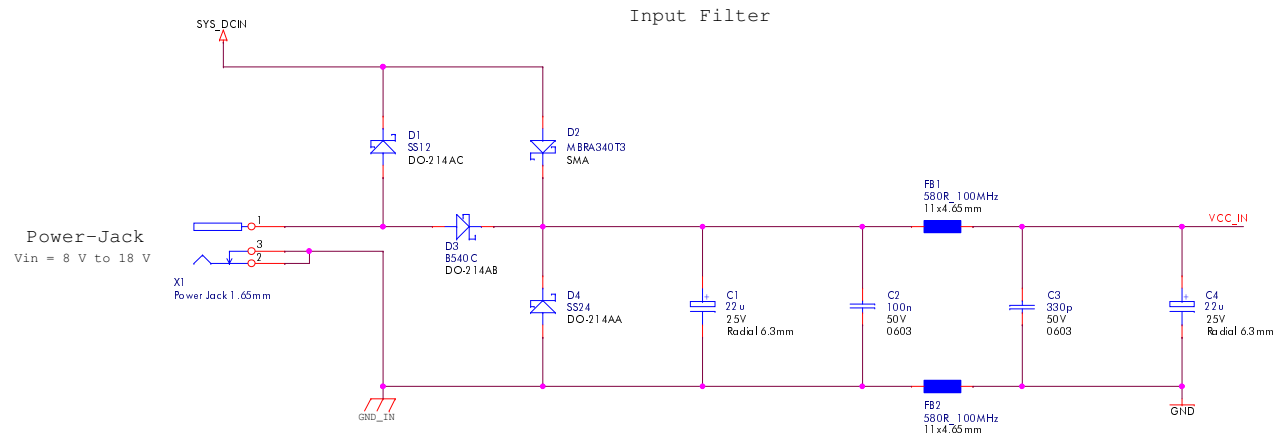


Preliminary Energy Balance

Supply with the DC-Jack Power Connector

Power Source	Component	Voltage [V]	Max. Current [A]	Max. Power [W]	Function
External Power Supply	DC-Jack	8 to 18		26,3001	Σ
DC-Jack	SYS_DCIN-line (Low Speed Connector)	8 to 18		7,0000	-
DC-Jack	Buck Regulator (ADP2384)	8 to 18		19,3001	Σ
Buck Regulator (ADP2384)	+5V-line (Low Speed Connector)	5	1,0000	5,0000	-
Buck Regulator (ADP2384)	USB-Hub (2x USB Host)	5	1,0000	5,0000	-
Buck Regulator (ADP2384)	DHCOR STM32MP15 Power Supply Module	5	0,3000	1,5000	-
Buck Regulator (ADP2384)	HDMI Connector (+5V Pin)	5	0,1500	0,7500	-
Buck Regulator (ADP2384)	DHCOR STM32MP15 - PMIC 3,3V Rail	5		6,1901	Σ
Buck Regulator (ADP2384)	DHCOR STM32MP15 - PMIC 1,8V Rail	5		0,8600	Σ
DHCOR STM32MP15 - PMIC 3,3V Rail	DHCOR STM32MP15 LGA (VDDA)	2,9	0,3500	1,0150	-
DHCOR STM32MP15 - PMIC 3,3V Rail	DHCOR STM32MP15 LGA (VDDA_SD)	2,9	0,3500	1,0150	-
DHCOR STM32MP15 - PMIC 3,3V Rail	DHCOR STM32MP15 LGA (VDD_LDO2)	2,9	0,0000	0,0000	-
DHCOR STM32MP15 - PMIC 3,3V Rail	DHCOR STM32MP15 LGA (VDD_LDO6)	1,8	0,0000	0,0000	-
DHCOR STM32MP15 - PMIC 3,3V Rail	USB-Hub (USB2513B)	3,3	0,0700	0,2310	-
DHCOR STM32MP15 - PMIC 3,3V Rail	Ethernet Phy (KSZ9031)	3,3	0,3288	1,0850	-
DHCOR STM32MP15 - PMIC 3,3V Rail	HDMI transmitter (ADV7513, with LDO for 1.8V)	3,3	0,0788	0,2600	-
DHCOR STM32MP15 - PMIC 3,3V Rail	WiFi / BT (Murata 1MW)	3,3	0,4300	1,4190	-
DHCOR STM32MP15 - PMIC 3,3V Rail	SD 3.0 switch (IP4856CX25)	3,3	0,3030	1,0000	-
DHCOR STM32MP15 - PMIC 3,3V Rail	GoldCap for VBAT	3,3	0,0500	0,1650	-
DHCOR STM32MP15 - PMIC 1,8V Rail	DHCOR STM32MP15 LGA (VDD)	1,8	0,2778	0,5000	-
DHCOR STM32MP15 - PMIC 1,8V Rail	+1,8V-line (Low Speed Connector)	1,8	0,1000	0,1800	-
DHCOR STM32MP15 - PMIC 1,8V Rail	MIPI CSI-2 de-serializer (STMIPID02/TR)	1,8	0,1000	0,1800	-


	Project: Avenger	
	Description: Energy Balance	
	PCB number: 588-100	Revision: R06
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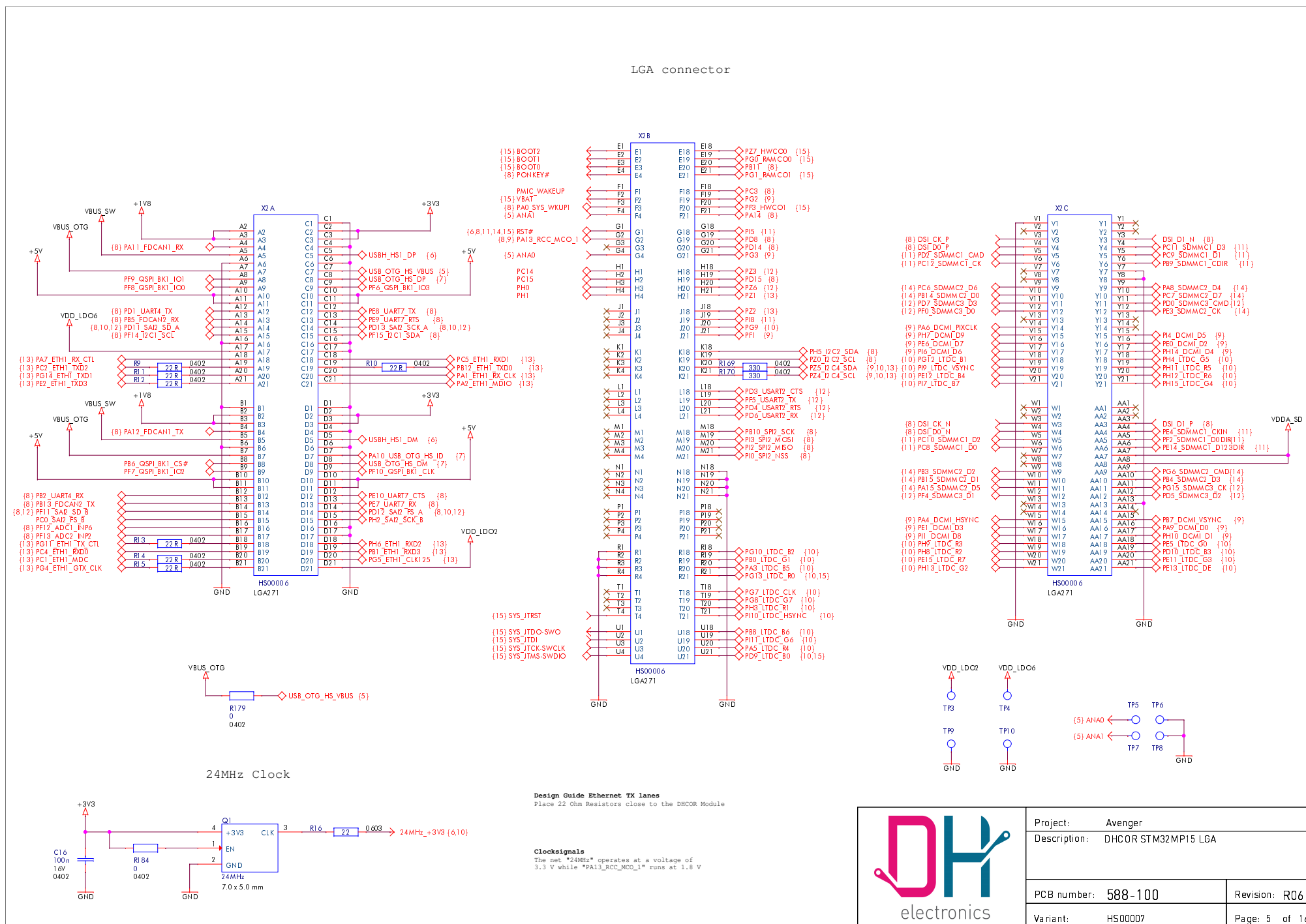


Design Guide:
Layout Recommendations
available in the datasheet

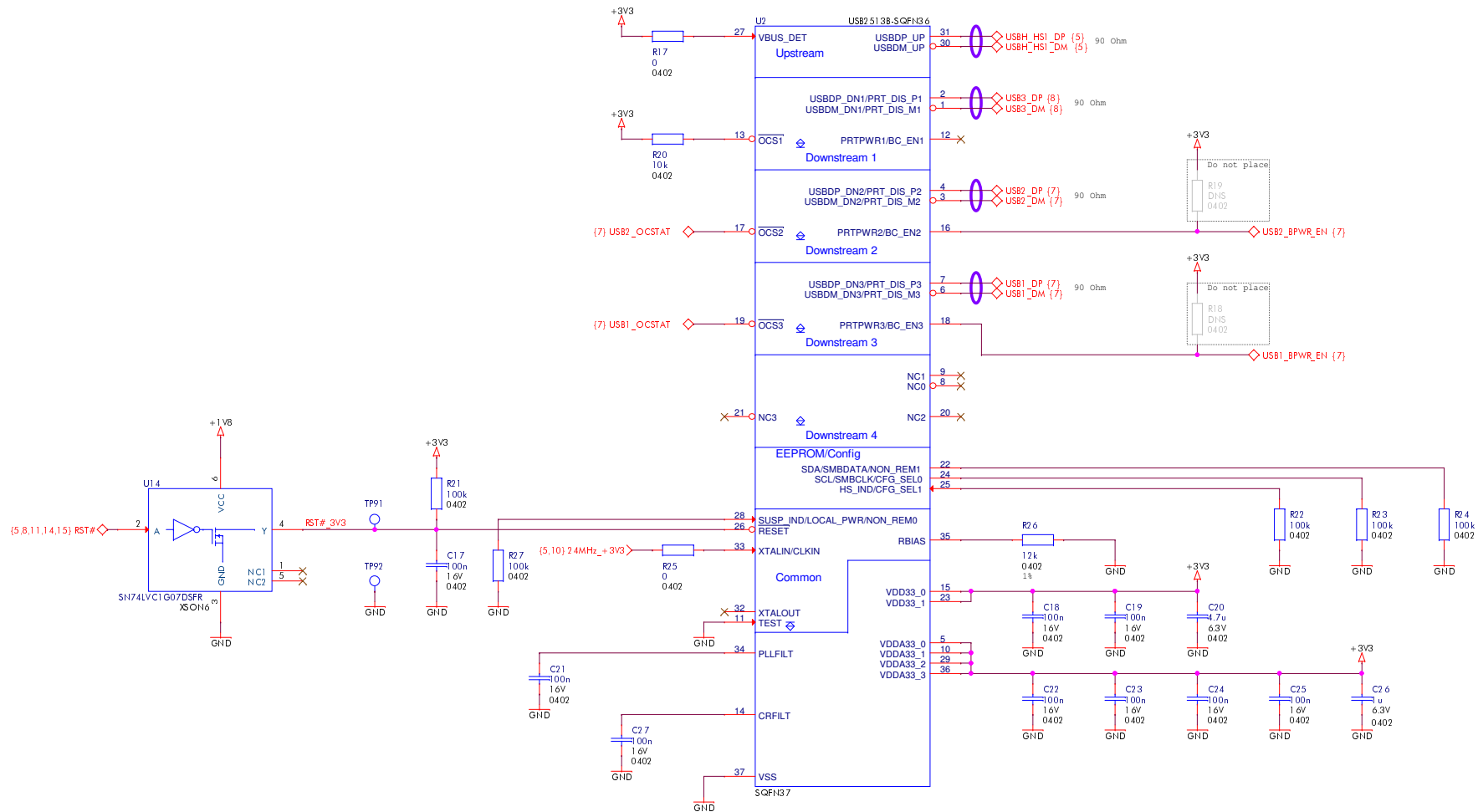
PIN RT:
43k Ohm at RT sets
fsw to 1.192MHz

PIN SS:
Connect a capacitor from SS to GND
to program the soft start time. If
this pin is open, the regulator
uses the internal soft start time.
15nF ~ 3ms soft start time

	Project: Avenger	
	Description: Power Supply	
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USB Hub



Downstream 1

This port is connected to the Expansion Connector with its own +5V supply

VBUS_DET:

For self-powered applications with a permanently attached host, this pin must be connected to a dedicated host control output, or connected to the 3.3 V domain that powers the host (typically VDD33).

CFG_SEL:

CFG_SEL[0] = 0 and CFG_SEL[1] = 0 defines default configuration:
-Strap options enabled
-Self-powered operation enabled
-Individual power switching
-Individual over-current sensing

NON_REM:

NON_REM[0] = 0 and NON_REM[1] = 0 indicates all ports as removable



Project: Avenger
Description: USB Hub

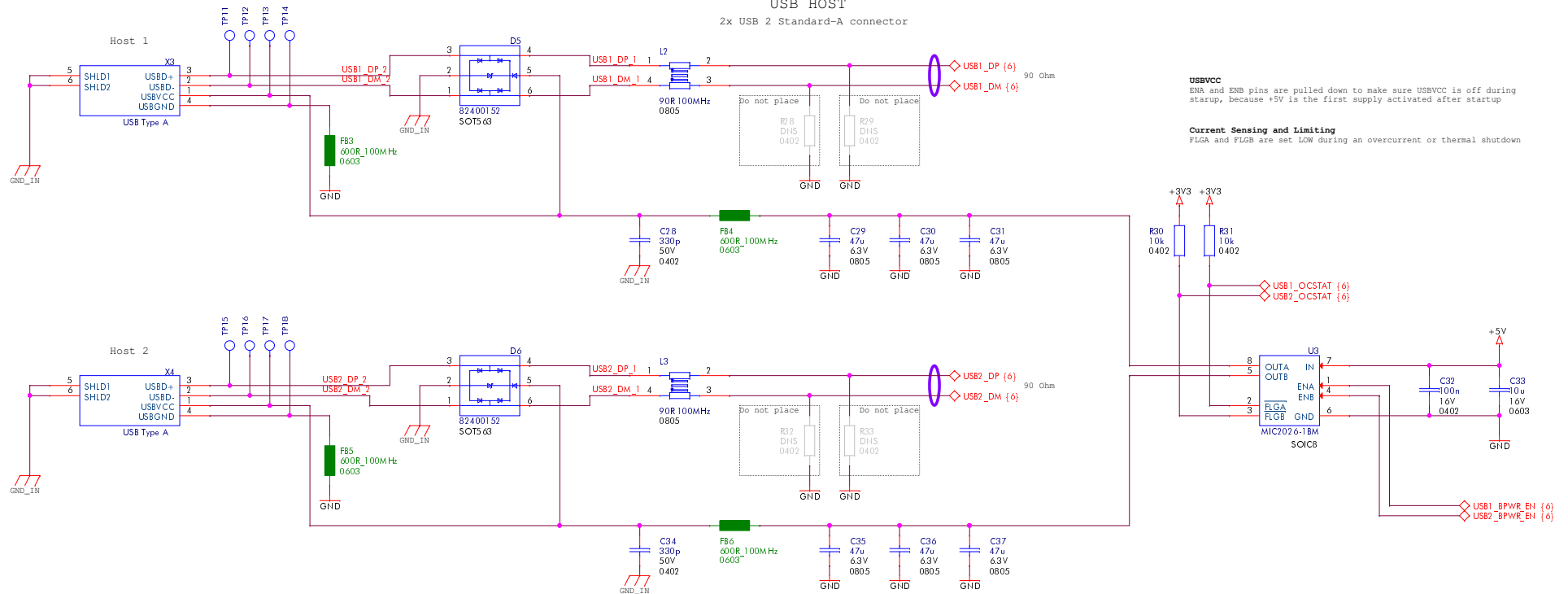
PCB number: 588-100

Revision: R06

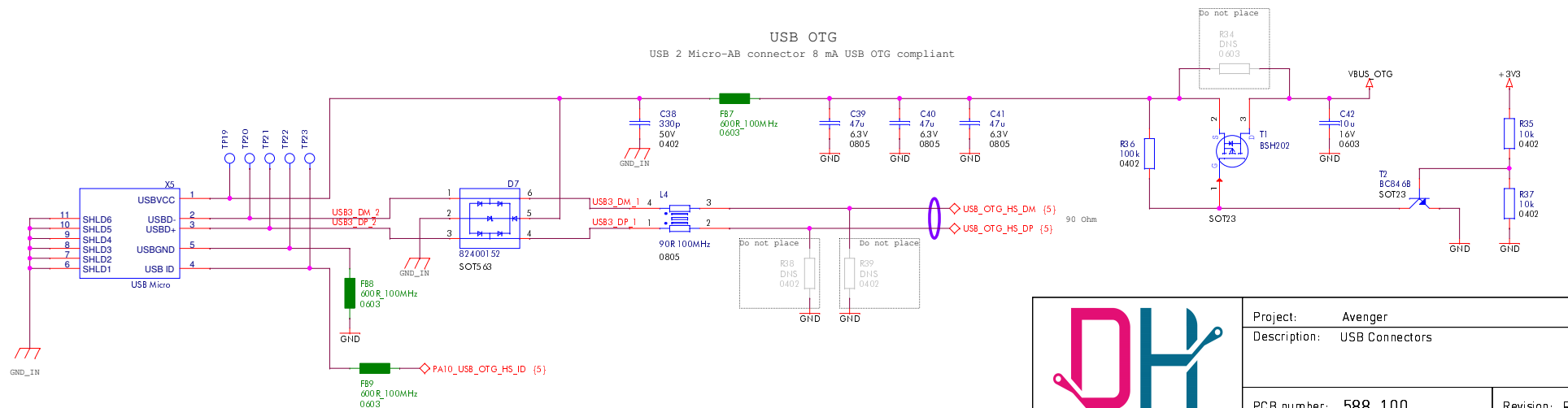
Variant: HS00007


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USB HOST 2x USB 2 Standard-A connector

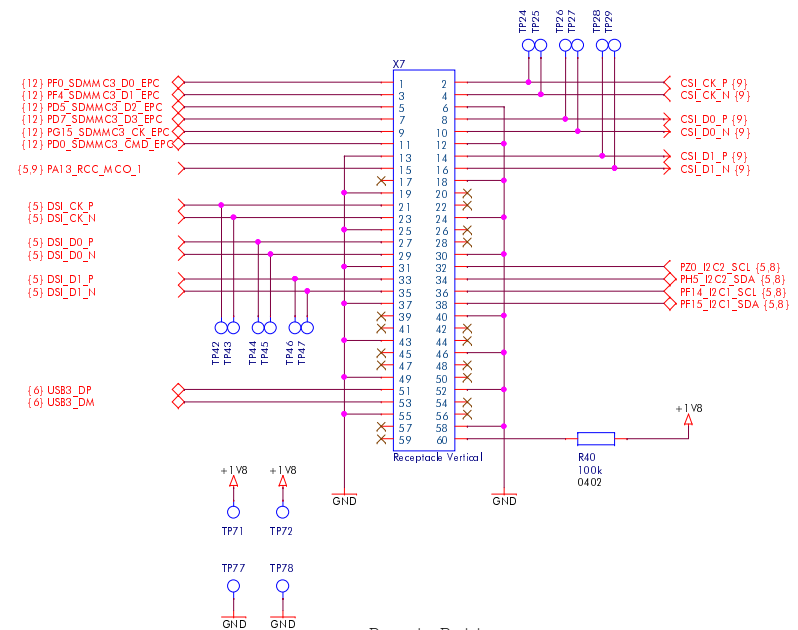


USB OTG USB 2 Micro-AB connector 8 mA USB OTG compliant

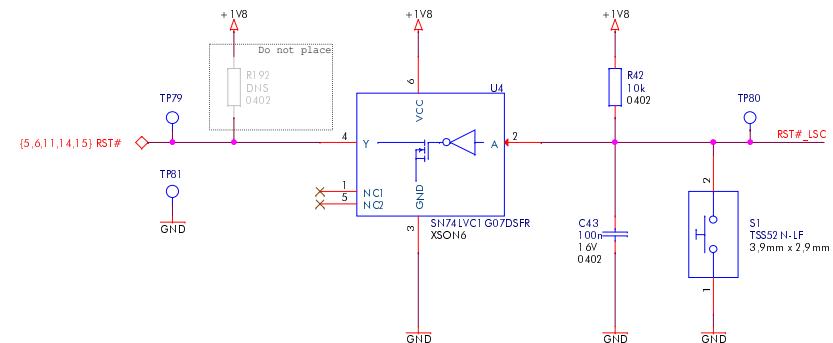



	Project: Avenger	
	Description: USB Connectors	
PCB number: 588-100	Revision: R06	
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High Speed Expansion Connector

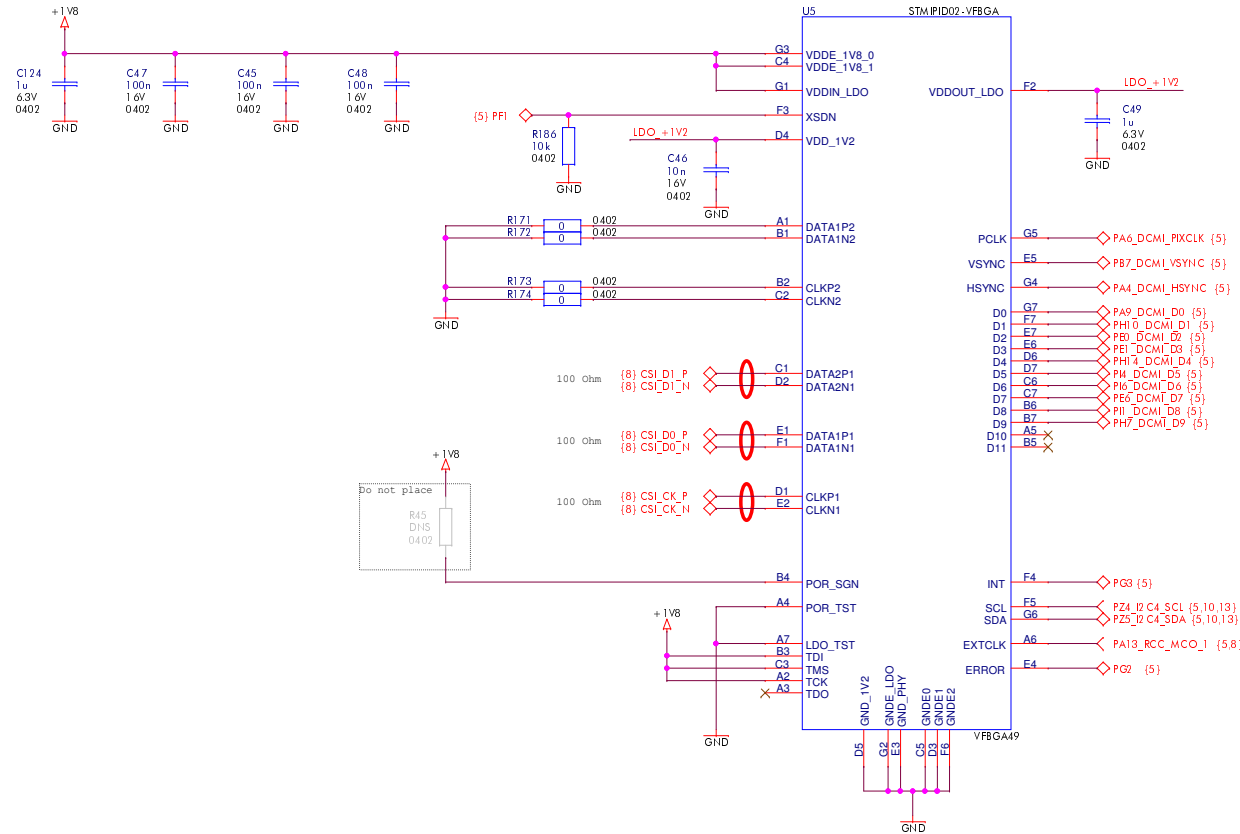


Reset Button



	Project: Avenger	
	Description: Expansion Connectors	
	PCB number: 588-100	Revision: R06
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MIPI CSI Bridge



Design Guide:

The CSI-2 Clock lanes must be in the middle of the 2 data lanes

Design Guide:

The high speed signal pairs (CLKP1, CLKN1), (DATA1P1, DATA1N1) and (DATA2P1, DATA2N1) should be routed as balanced transmission lines with a characteristic differential impedance (Zodiff) of 100ohm and matched in length.

Test Interface (ST internal use)

LDO_TST, TDI, TMS, TCK and TDO are Test interfaces for ST

INT:

This is a status showing reception of short packet in CSI stream which needs to be cleared by user.

ERROR:

This is an accumulated status of all Errors found in the chip. The individual status can be checked via I2C

Design Guide:

The PCLK, HSYNC, VSYNC must be routed in the middle of the output data bus for skew management reasons

I²C4 Address


Address: 0b00101000 = 0x14
Write: 0b00101000 = 0x28
Read: 0b00101001 = 0x29

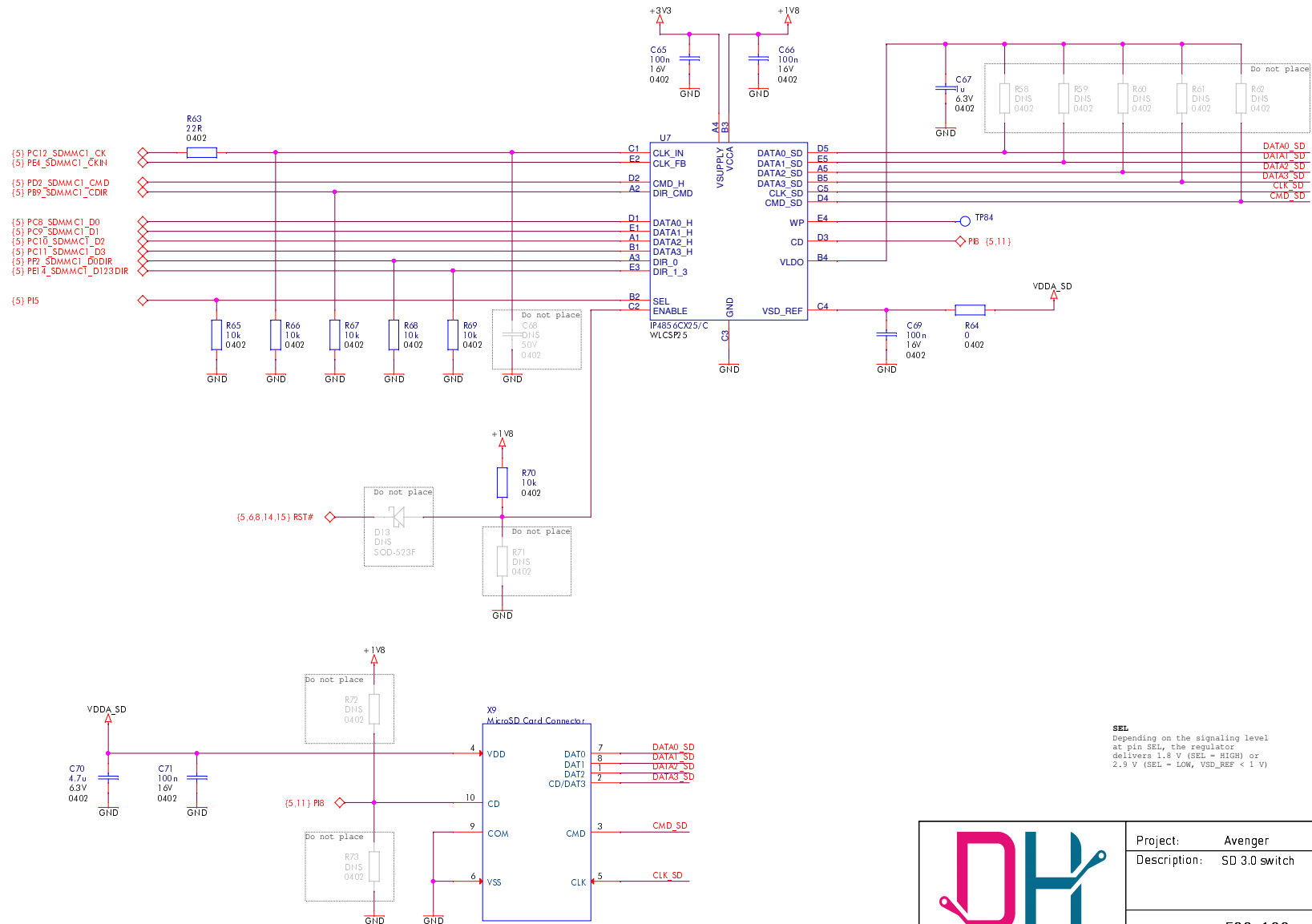
XSDN:


Chip Shutdown is connected GPIO to fit the power-up sequencing requirements

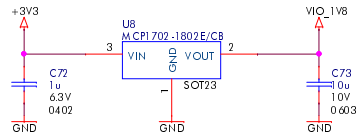
POR_SGN

Power On Reset

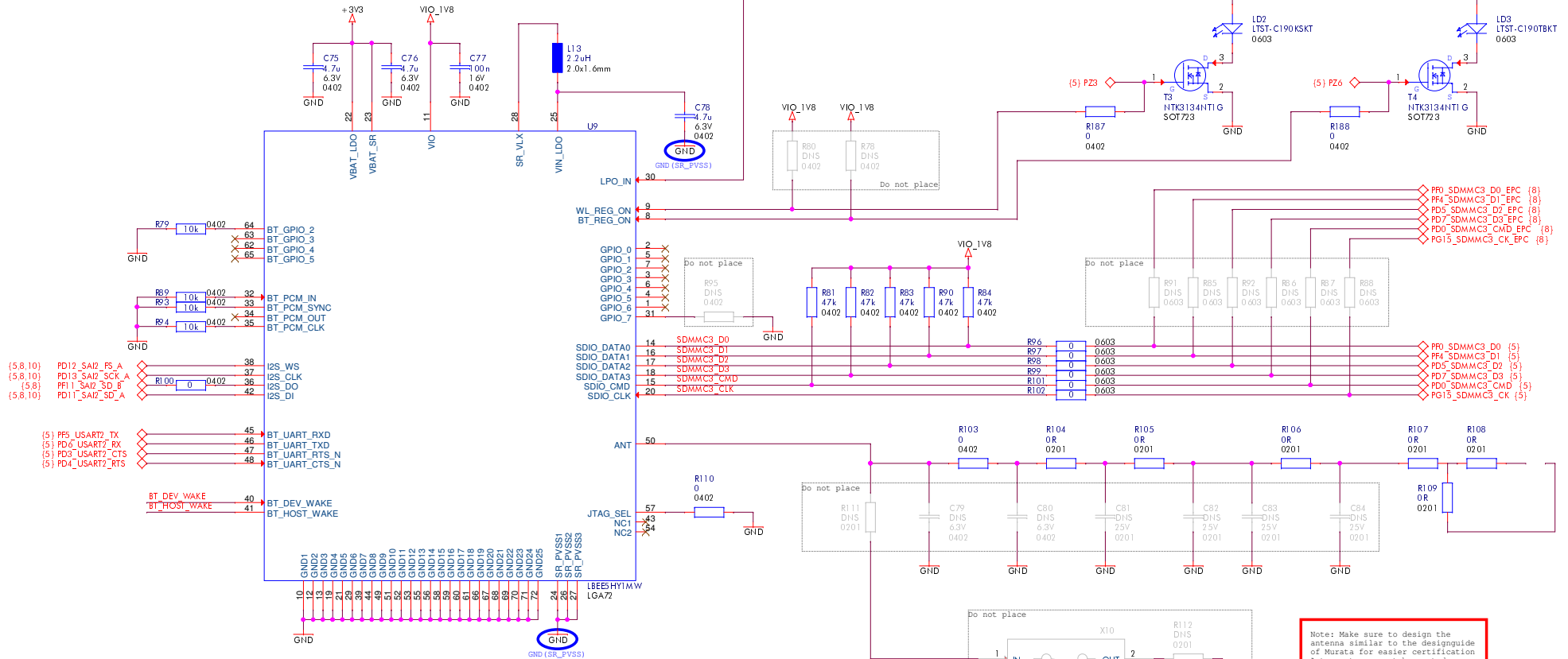
	Project: Avenger	
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	Project: Avenger	
	Description: SD 3.0 switch	
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Design Guide MCP1702
Place thermal vias on GND Pad



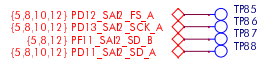
Notes to supply voltage:
VIO = 1V8 or 3V3 (with 1V8 max. 200uA)
VBAT = 3V3 to 4V2 (with 3V3 max 450mA)
VBAT should be up before or at the same time as VIO.
Therefore VIO is provided by a LDO which is driven by the same source as VBAT

Note to GPIO_7:
Strapping option of SDIO interface voltage
Open: SDIO interface voltage=1.8V
10kOhm PD: SDIO interface voltage=3.3V


JTAG_SEL:
JTAG select. This pin must be connected to ground if the JTAG/SWD interface is not used.

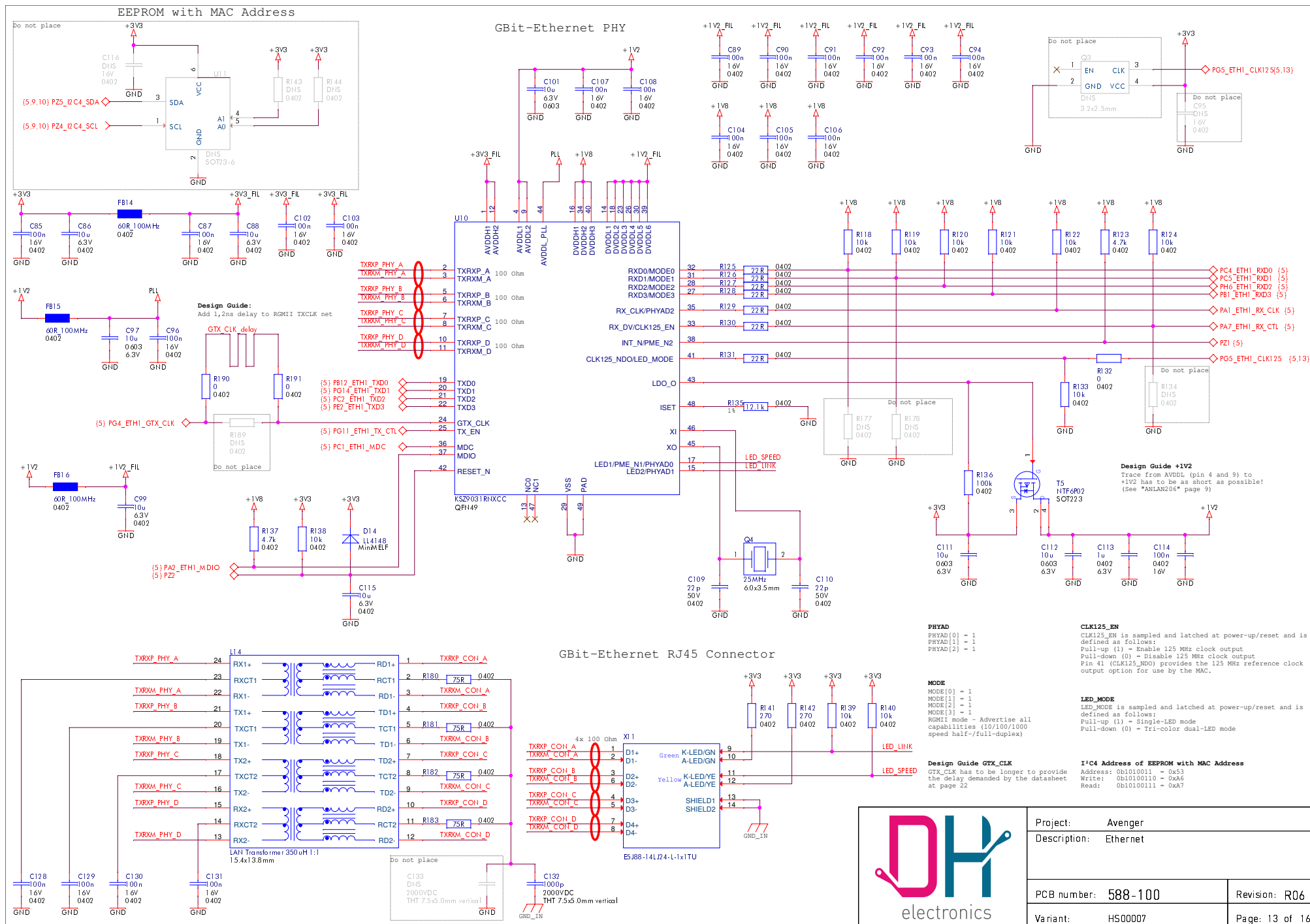
WL_REG_ON and BT_REG_ON:
Used by PMU to power up or power down the internal CYW43455 regulators used by the WiFi/BT section. Also, when deasserted, this pin holds the WiFi/BT section in reset. This pin has an internal 200k ohm pull-down resistor that is enabled by default. It can be disabled through programming.

Note: SR_PVSS GND have to be isolated from typical GND. It's better to separate the GND plane for this area on the top layer and connect it to the main GND thru the via hole on the lower layer.

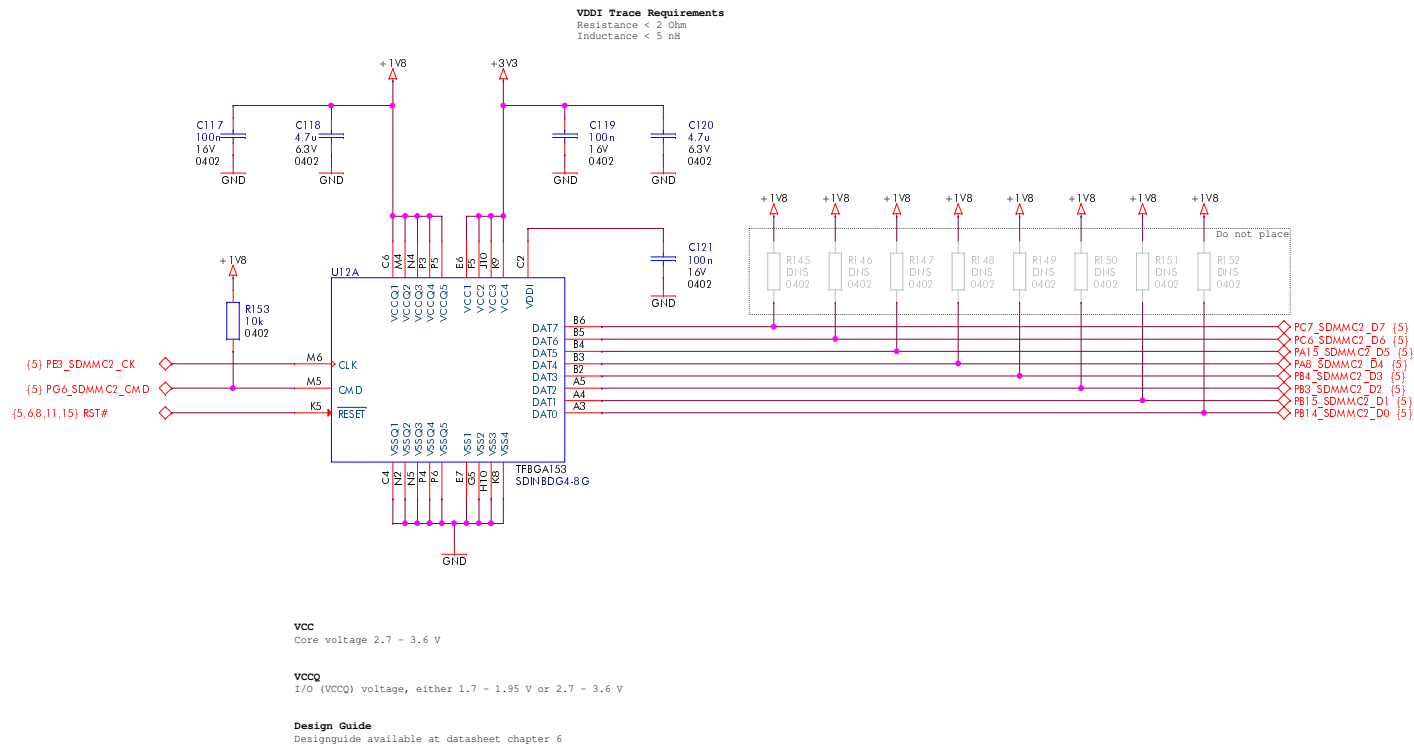


Note: Make sure to design the antenna similar to the design guide of Murata for easier certification. Antenna trace must be routed as 50R coplanar waveguide. The additional coaxial-connector MUST NOT generate any stub lines.

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	Description: WiFi and Bluetooth	
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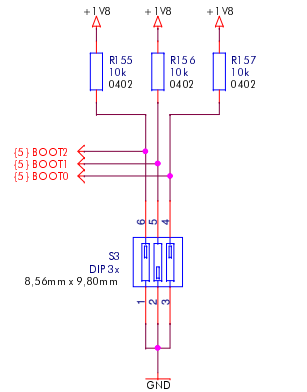


8GB eMMC Flash Drive



UI2B		
A1	NC_A1	NC_IJ2
A2	NC_A2	NC_IJ3
A3	NC_A3	NC_IJ4
A4	NC_A4	NC_IJ5
A5	NC_A5	NC_K1
A6	NC_A6	NC_K2
A7	NC_A7	NC_K3
A8	NC_A8	NC_K4
A9	NC_A9	NC_K5
A10	NC_A10	NC_K6
A11	NC_A11	NC_K7
A12	NC_A12	NC_K8
A13	NC_A13	NC_K9
A14	NC_A14	NC_K10
B1	NC_B1	NC_K11
B2	NC_B2	NC_K12
B3	NC_B3	NC_K13
B4	NC_B4	NC_K14
B5	NC_B5	NC_L1
B6	NC_B6	NC_L2
B7	NC_B7	NC_L3
B8	NC_B8	NC_L4
B9	NC_B9	NC_L5
B10	NC_B10	NC_L6
B11	NC_B11	NC_L7
B12	NC_B12	NC_L8
B13	NC_B13	NC_L9
B14	NC_B14	NC_L10
C1	NC_C1	NC_M1
C2	NC_C2	NC_M2
C3	NC_C3	NC_M3
C4	NC_C4	NC_M4
C5	NC_C5	NC_M5
C6	NC_C6	NC_M6
C7	NC_C7	NC_M7
C8	NC_C8	NC_M8
C9	NC_C9	NC_M9
C10	NC_C10	NC_M10
C11	NC_C11	NC_M11
C12	NC_C12	NC_M12
C13	NC_C13	NC_M13
C14	NC_C14	NC_M14
D1	NC_D1	NC_N1
D2	NC_D2	NC_N2
D3	NC_D3	NC_N3
D4	NC_D4	NC_N4
D5	NC_D5	NC_N5
D6	NC_D6	NC_N6
D7	NC_D7	NC_N7
D8	NC_D8	NC_N8
D9	NC_D9	NC_N9
D10	NC_D10	NC_N10
D11	NC_D11	NC_N11
D12	NC_D12	NC_N12
D13	NC_D13	NC_N13
D14	NC_D14	NC_N14
E1	NC_E1	NC_P1
E2	NC_E2	NC_P2
E3	NC_E3	NC_P3
E4	NC_E4	NC_P4
E5	NC_E5	NC_P5
E6	NC_E6	NC_P6
E7	NC_E7	NC_P7
E8	NC_E8	NC_P8
E9	NC_E9	NC_P9
E10	NC_E10	NC_P10
E11	NC_E11	NC_P11
E12	NC_E12	NC_P12
E13	NC_E13	NC_P13
E14	NC_E14	NC_P14
F1	NC_F1	NC_Q1
F2	NC_F2	NC_Q2
F3	NC_F3	NC_Q3
F4	NC_F4	NC_Q4
F5	NC_F5	NC_Q5
F6	NC_F6	NC_Q6
F7	NC_F7	NC_Q7
F8	NC_F8	NC_Q8
F9	NC_F9	NC_Q9
F10	NC_F10	NC_Q10
F11	NC_F11	NC_Q11
F12	NC_F12	NC_Q12
F13	NC_F13	NC_Q13
F14	NC_F14	NC_Q14
G1	NC_G1	NC_A6
G2	NC_G2	NC_A7
G3	NC_G3	NC_A8
G4	NC_G4	NC_A9
G5	NC_G5	NC_A10
G6	NC_G6	NC_A11
G7	NC_G7	NC_A12
G8	NC_G8	NC_A13
G9	NC_G9	NC_A14
G10	NC_G10	NC_B1
G11	NC_G11	NC_B2
G12	NC_G12	NC_B3
G13	NC_G13	NC_B4
G14	NC_G14	NC_B5
H1	NC_H1	NC_B6
H2	NC_H2	NC_B7
H3	NC_H3	NC_B8
H4	NC_H4	NC_B9
H5	NC_H5	NC_B10
H6	NC_H6	NC_B11
H7	NC_H7	NC_B12
H8	NC_H8	NC_B13
H9	NC_H9	NC_B14
H10	NC_H10	NC_C1
H11	NC_H11	NC_C2
H12	NC_H12	NC_C3
H13	NC_H13	NC_C4
H14	NC_H14	NC_C5
I1	NC_I1	NC_C6
I2	NC_I2	NC_C7
I3	NC_I3	NC_C8
I4	NC_I4	NC_C9
I5	NC_I5	NC_C10
I6	NC_I6	NC_C11
I7	NC_I7	NC_C12
I8	NC_I8	NC_C13
I9	NC_I9	NC_C14
I10	NC_I10	NC_D1
I11	NC_I11	NC_D2
I12	NC_I12	NC_D3
I13	NC_I13	NC_D4
I14	NC_I14	NC_D5
J1	NC_J1	NC_D6
J2	NC_J2	NC_D7
J3	NC_J3	NC_D8
J4	NC_J4	NC_D9
J5	NC_J5	NC_D10
J6	NC_J6	NC_D11
J7	NC_J7	NC_D12
J8	NC_J8	NC_D13
J9	NC_J9	NC_D14
J10	NC_J10	NC_E1
J11	NC_J11	NC_E2
J12	NC_J12	NC_E3
J13	NC_J13	NC_E4
J14	NC_J14	NC_E5
K1	NC_K1	NC_E6
K2	NC_K2	NC_E7
K3	NC_K3	NC_E8
K4	NC_K4	NC_E9
K5	NC_K5	NC_E

Boot Selection

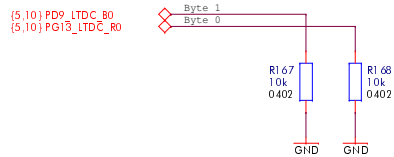


BOOT2 SW3	BOOT1 SW2	BOOT0 SW1 (Number at DIP switch)	
0	0	0	= UART and USB
0	0	1	= NOR-Flash
0	1	0	= eMMC
0	1	1	= NAND-Flash
1	0	0	= Reserved
1	0	1	= SD-Card
1	1	0	= UART and USB
1	1	1	= SD-Card

Switch "ON" means "0"

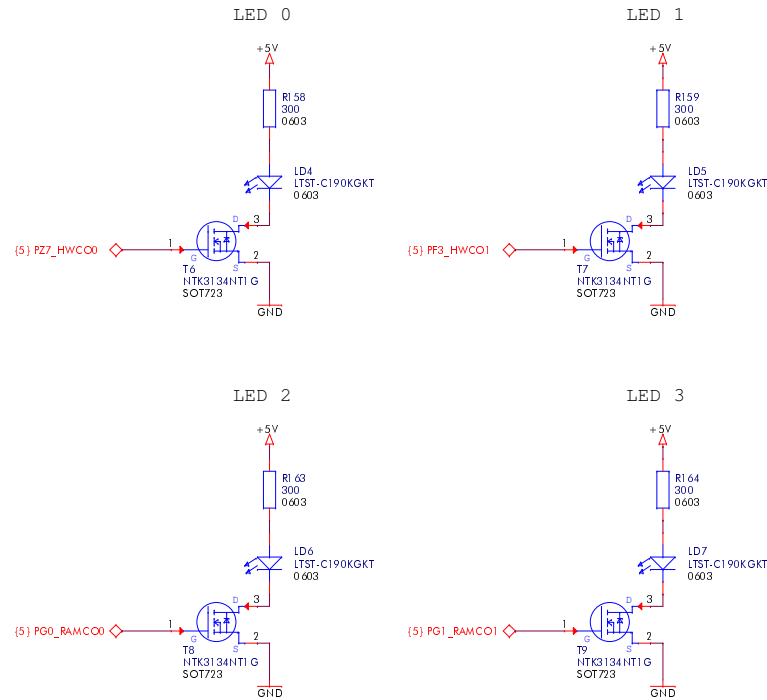
Hardwarecoding

PD9_LTDC_R0 and PG13_LTDC_R0 are used as Hardwarecoding during startup

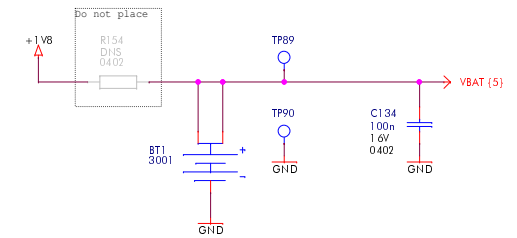


	PD9_LTDC_R0	PG13_LTDC_R0
Hardware version	Byte 1	Byte 0
HW100	0	0
HW200	0	1
HW300	1	0
HW400	1	1

User LEDs

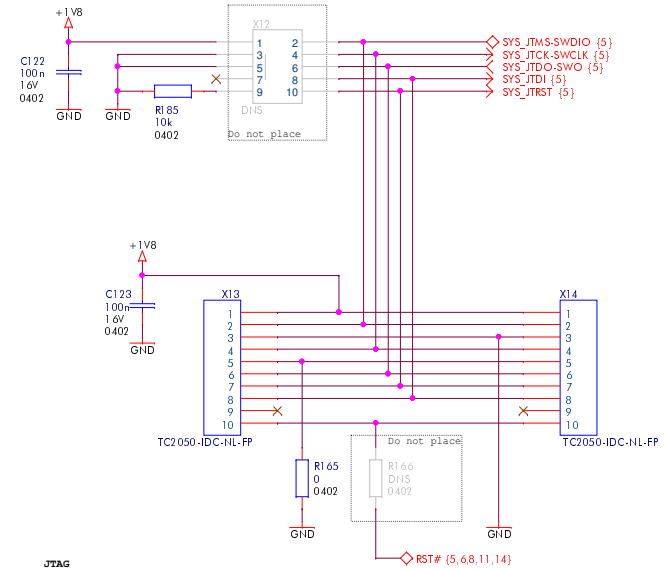


Connector for CR1220 Battery



JTAG

10-Pin connector (Top) and two Tag-Connect connectors on top and bottom of PCB (Bottom)



JTAG

To avoid any uncontrolled I/O levels, the STM32MP15 Series embeds internal pull-up and pull-down resistors on JTAG pins

- JTRST: Internal pull-up
- JTDI: Internal pull-up
- JTCK-SWCLK: Internal pull-up
- JTMS-SWDIO: Internal pull-up
- JTCK-SWCLK: Internal pull-down



Project: Avenger
Description: Miscellaneous

PCB number: 588-100

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Changelog:

588-100 R01 -> R02

- MH/09-08-2018: Included footprint for the DHCOR Module and updated the pin assignment with the current versoin of the DHCOR Module
- MH/21-08-2018: Replaced Goldcap with a CR1220 battery connector
- MH/22-08-2018: Added Testpads for needle adapter and added new capacitor of the ADP2384
- MH/27-08-2018: Connected PA0_SYS_WKUP1 to Expansion Connector
- MH/03-09-2018: Added the changes recommended by the review
- MH/04-09-2018: Added parts to the correct variant in the part manager

588-100 R02 -> R03

- MH/07-09-2018: Changed pinning of HDMI connector in order to achive a smoother layout.
- MH/10-09-2018: Added net-names and indicators for the differential pairs at USB, Changed diode D8 to DNP
- MH/12-09-2018: Added 0-Ohm resistor at Q1 Pin 1
- MH/13-09-2018: Added a 10k-0hm resistor at JTAG Pin 9 to GND. Switched the regular GPIOs on the Low Speed Expansion Connector with the GPIOs which are capable of CAN an ADC to have more functions available to the user. Corrected Project name to "STM32MP15 96Boards"
- SH/17-09-2018: Added R186, R187, R188. Set R78 and R80 on "Do not place"
- SH/19-09-2018: Added C134, R189, R190, R191, R192, U14, TP91, TP92
- MH/24-09-2018: Switched the Port 1 with Port 3 of the USB-Hub to avoid the crossing between them on the layout and inverted some pinnings on the diodes and inductors at the USB connectors.
- MH/25-09-2018: Connected the mechanical pins of the HDMI-connector to GND_IN and corrected the description of the DIP-Switch [Switch "ON" means "0"] and updated symbol of the LAN-Transformer

588-100 R03 -> R04

- MH/01-10-2018: Corrected wrong connection of HDMI-connector and set the battery connector to be placed in the variant HS00007

588-100 R04 -> R05


- MH/15-10-2018: Updated DH-part LD0037 to LD0037-R01 which is the same LED with some additional alternative LEDs reccomended by BMK. In the schematic these LEDs are LD4, LD5, LD6 and LD7. Updated ordering information of U10. Changed C132 and C133 to new type due to PCN of the part used before.

588-100 R05 -> R06

- MH/14-12-2018: R06 is the updated version for the first order [about 200pcs] for the embedded World. Set U11 and its peripherals to DNP because of the wrong connection to 3,3V instead of 1,8V. Changed manufacturer of C1 and C4 to Vishay. Set C6 to DNP and placed C5 instead. Additional C5 has changed to 22uF. Changed Q1 to [DH part nubel] Y-0060. Changed eMMC to commercial type. Updated Q4 from the DH part number Y-0015-R01 to Y-0015-R02. Changed R40 to 100k and set it to be placed as a standard. Set X12 to do not place [Double-checked with linaro, this connector doesn't need to be placed in the series product]. Changed Project name.

588-100 R06 -> R07

xx/xx-xx-20xx:

	Project: Avenger	
	Description: Changelog	
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