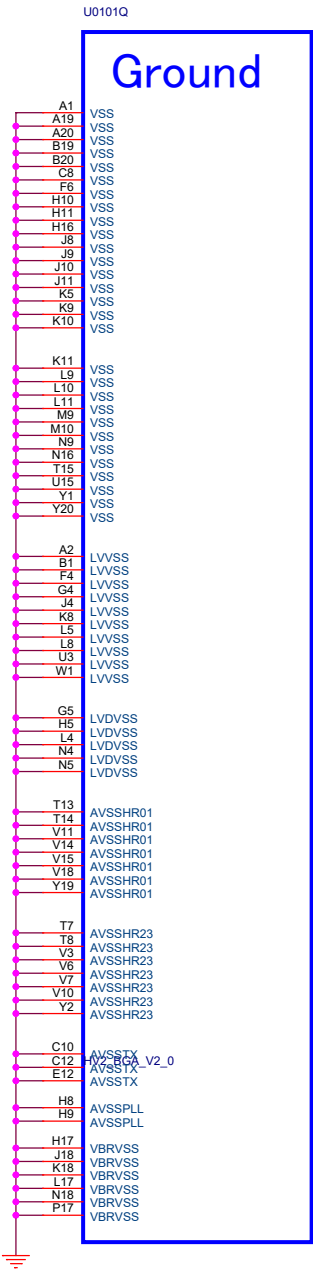
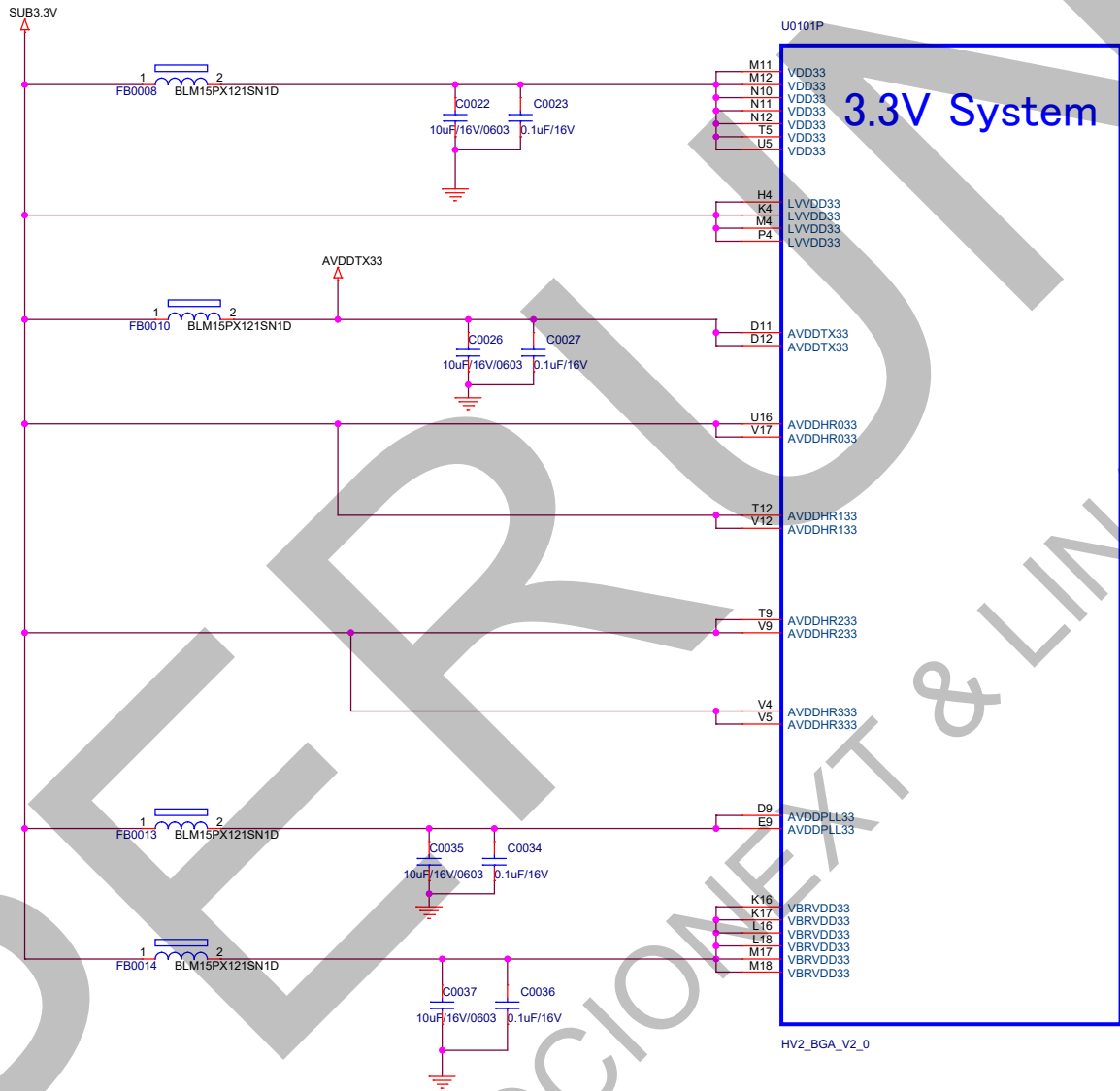
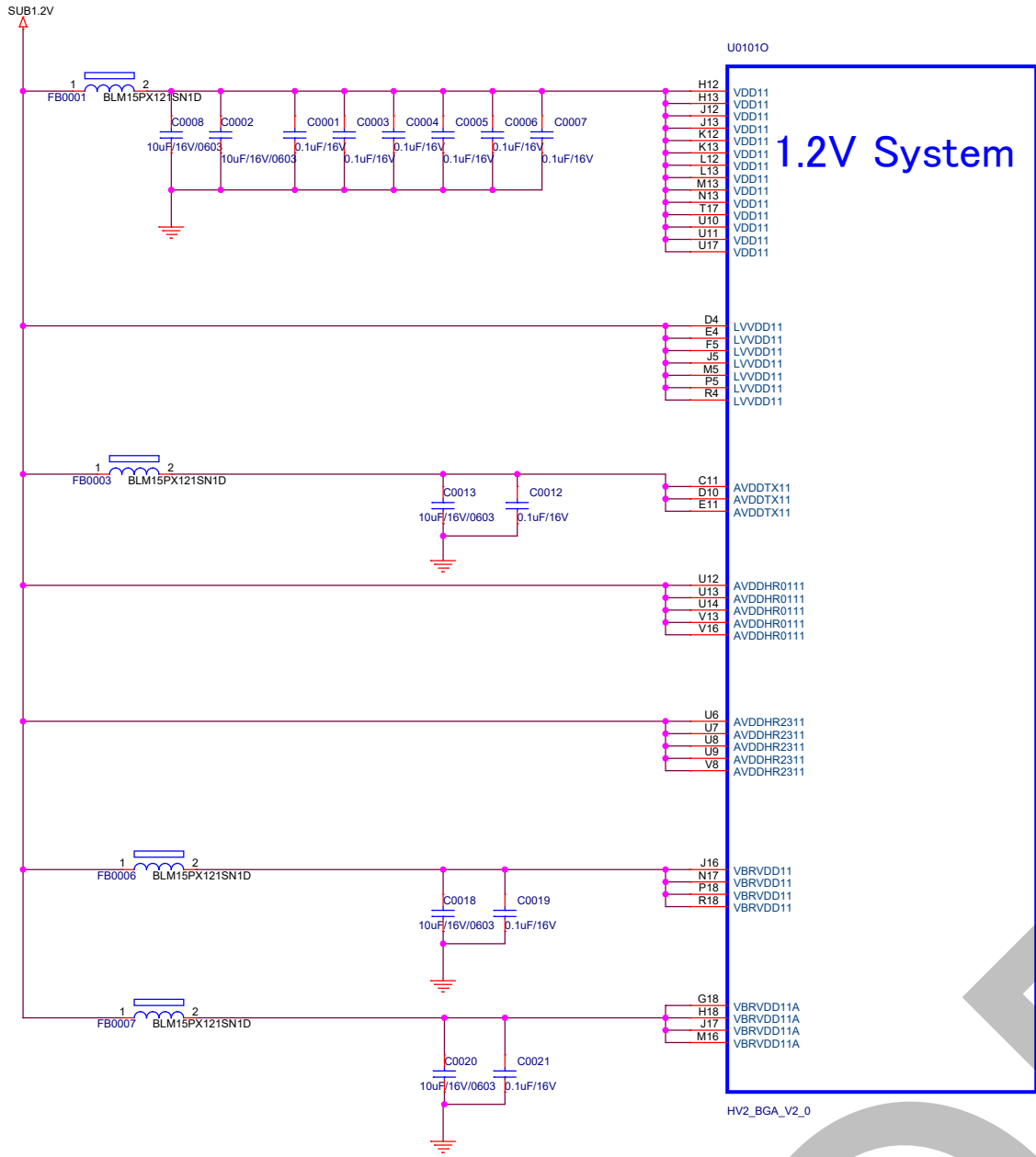


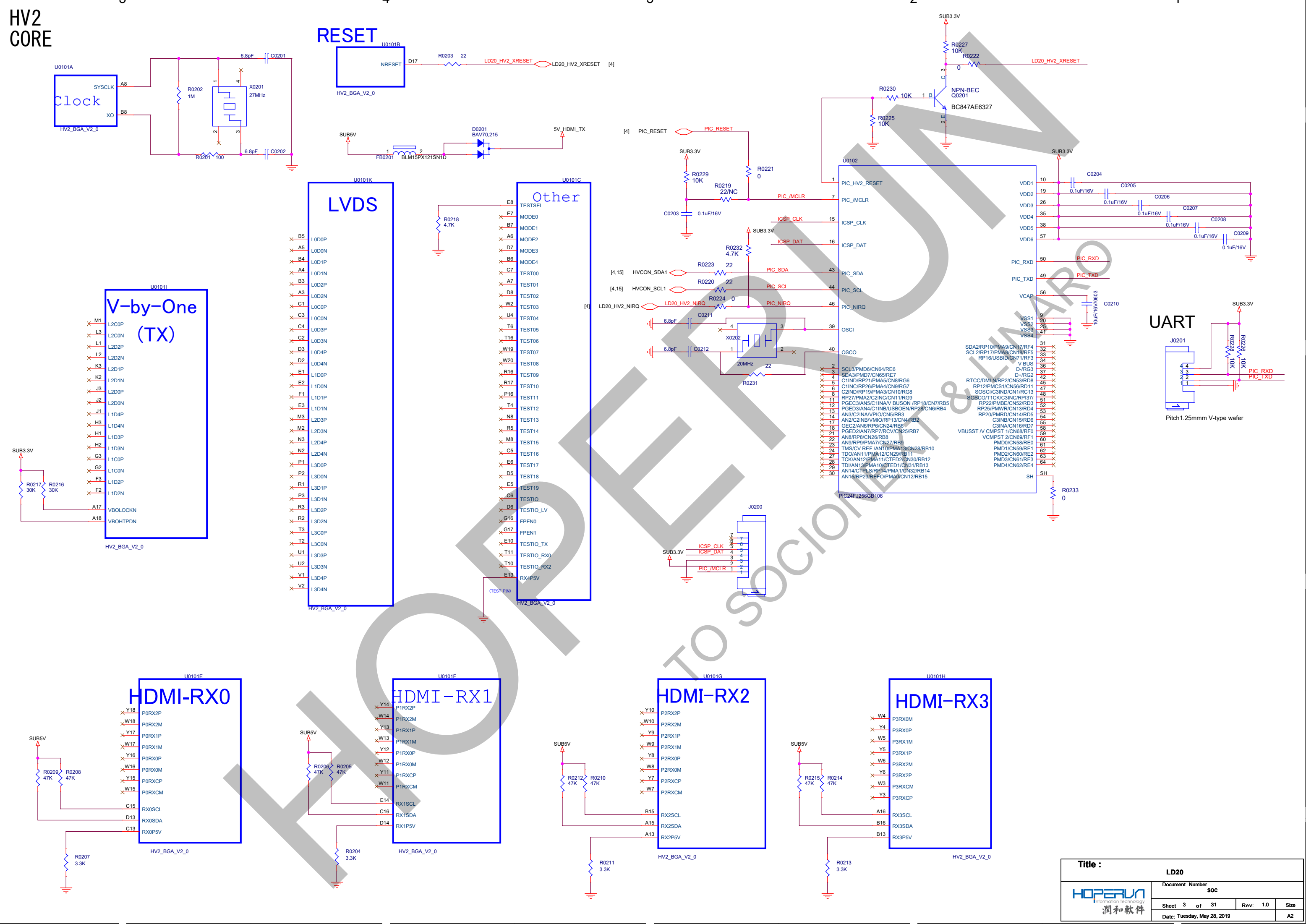
REF LD20 96 BOARD

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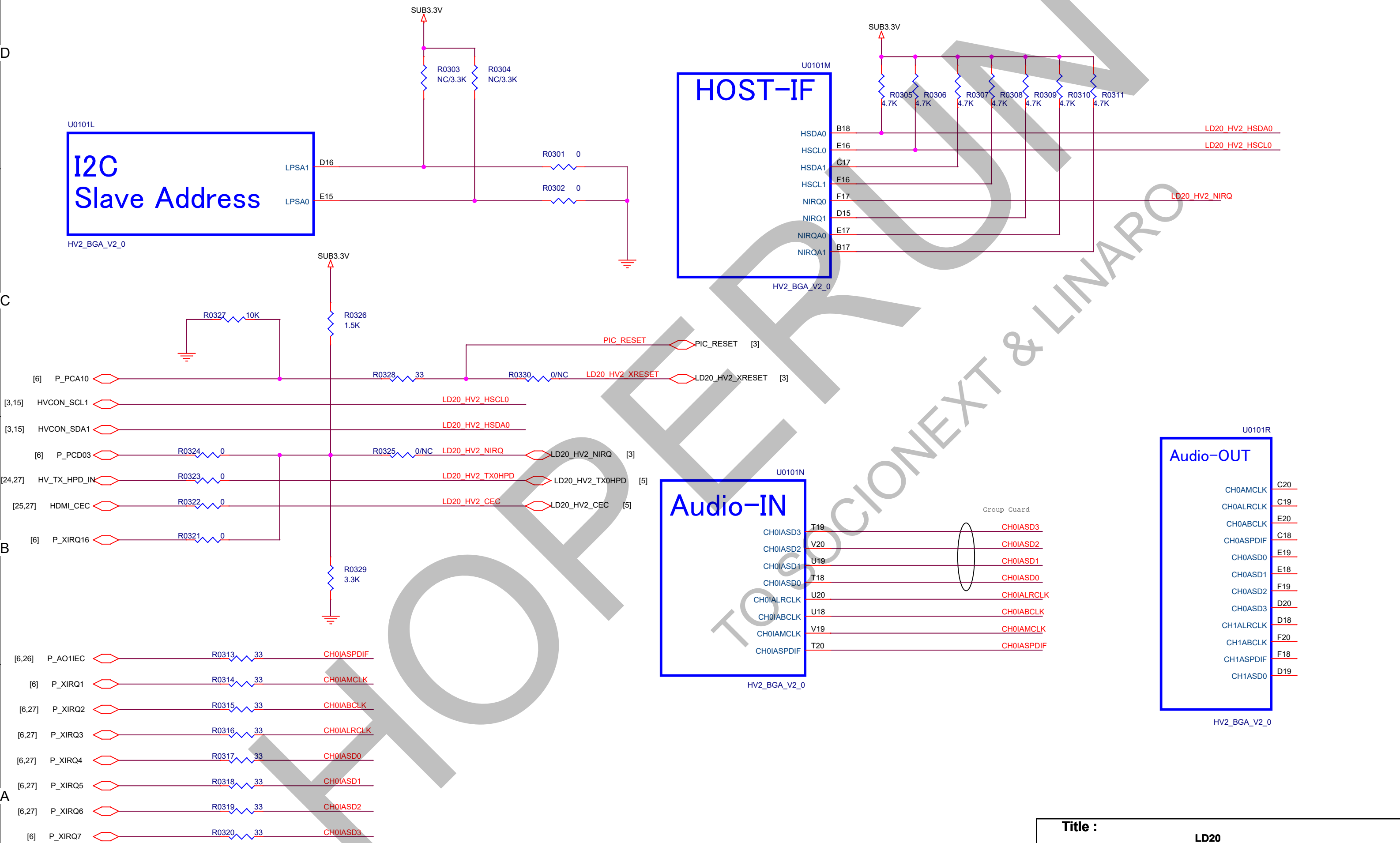
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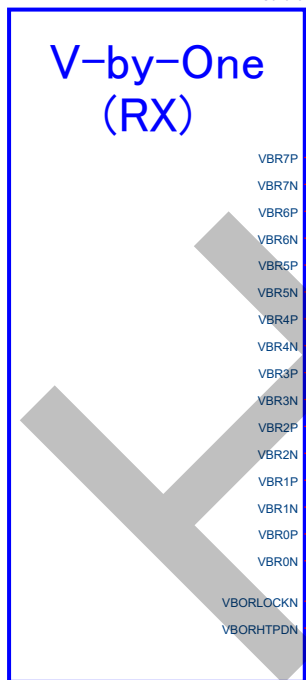
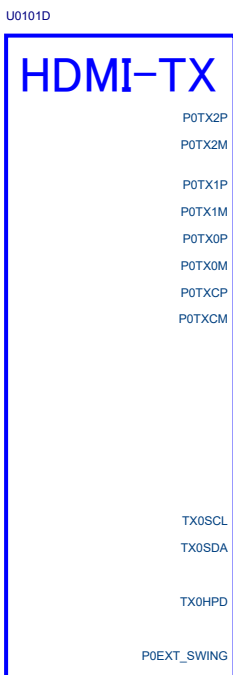
HV2
CORE

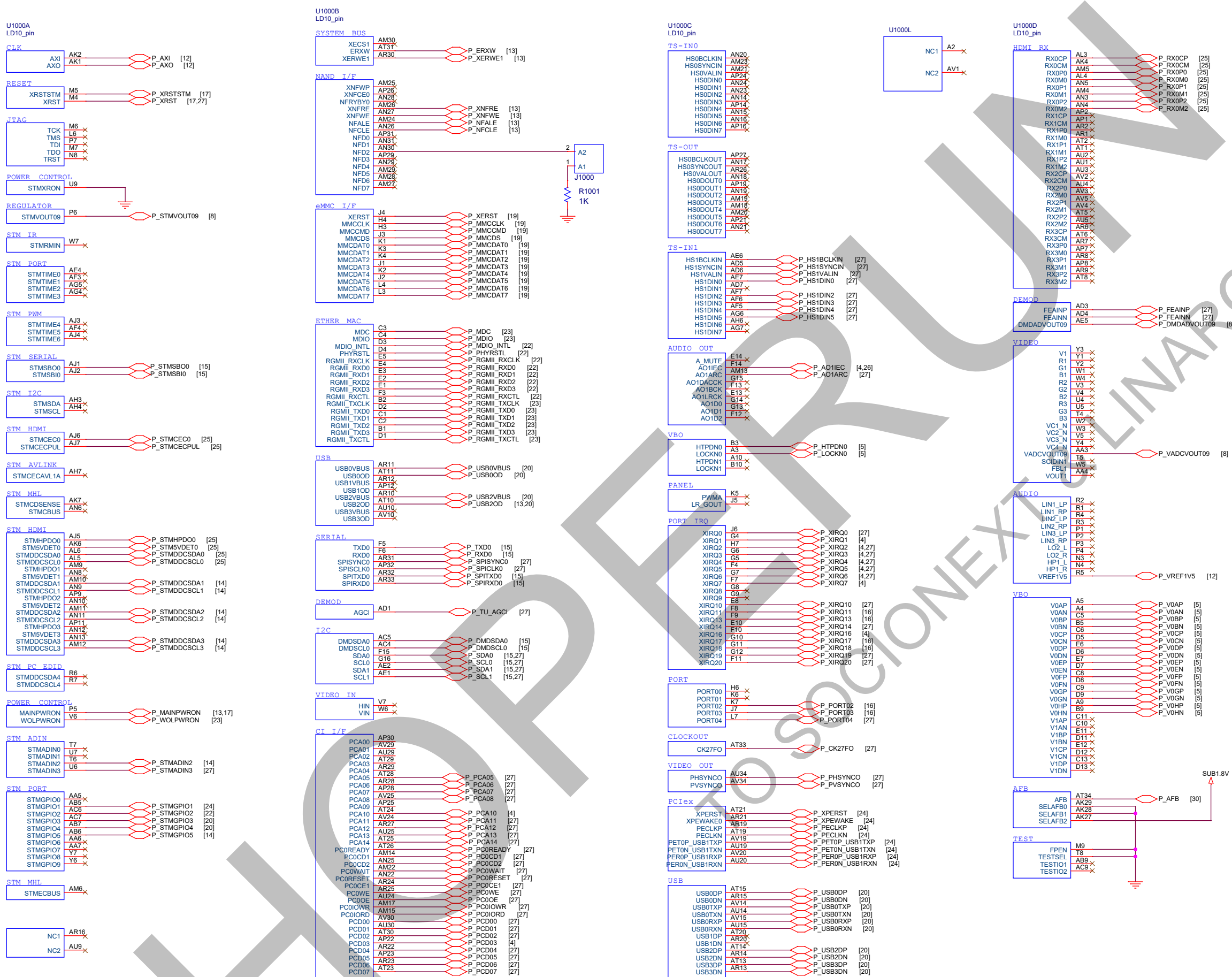


HV2 AUDIO

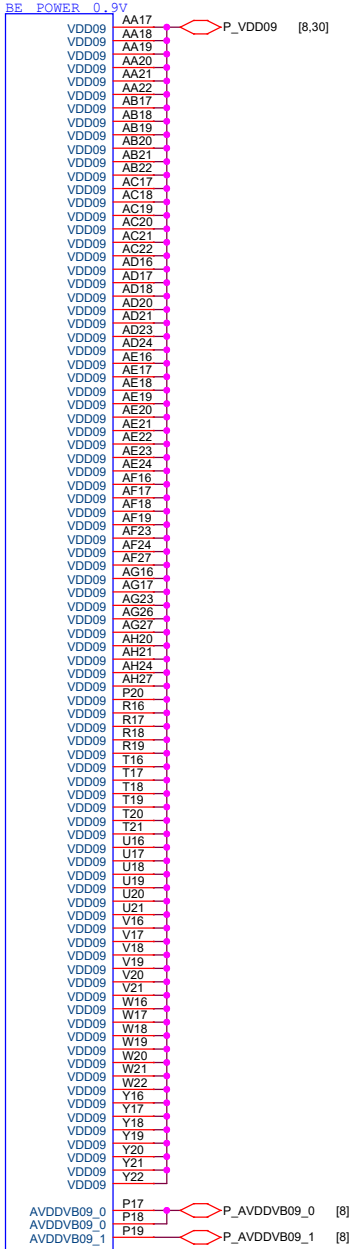


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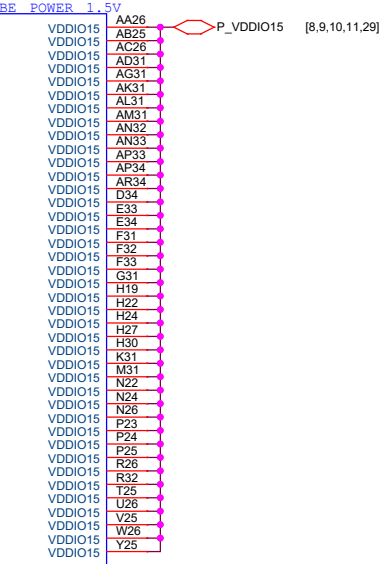




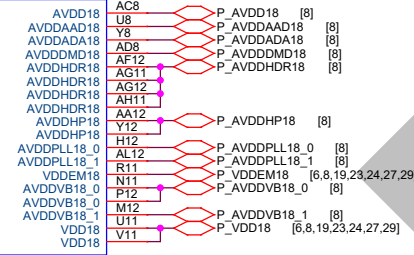
U1000H
LD10_pin



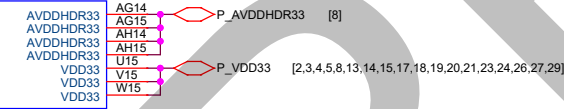
U1000I
LD10_pin



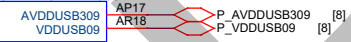
BE_POWER 1.8V



BE_POWER 3.3V



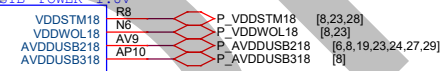
STB_POWER 0.9V



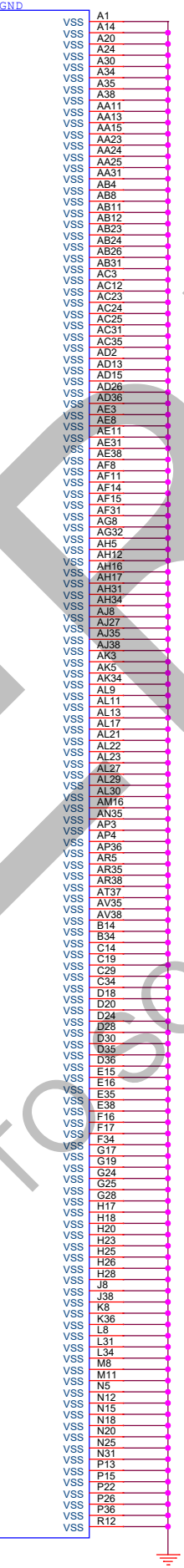
STB_POWER 3.3V



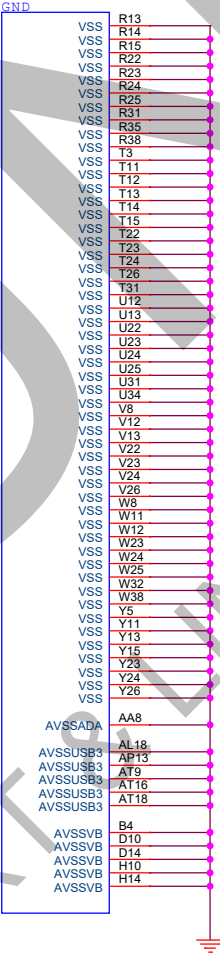
STB_POWER 1.8V



U1000J
LD10_pin



U1000K
LD10_pin



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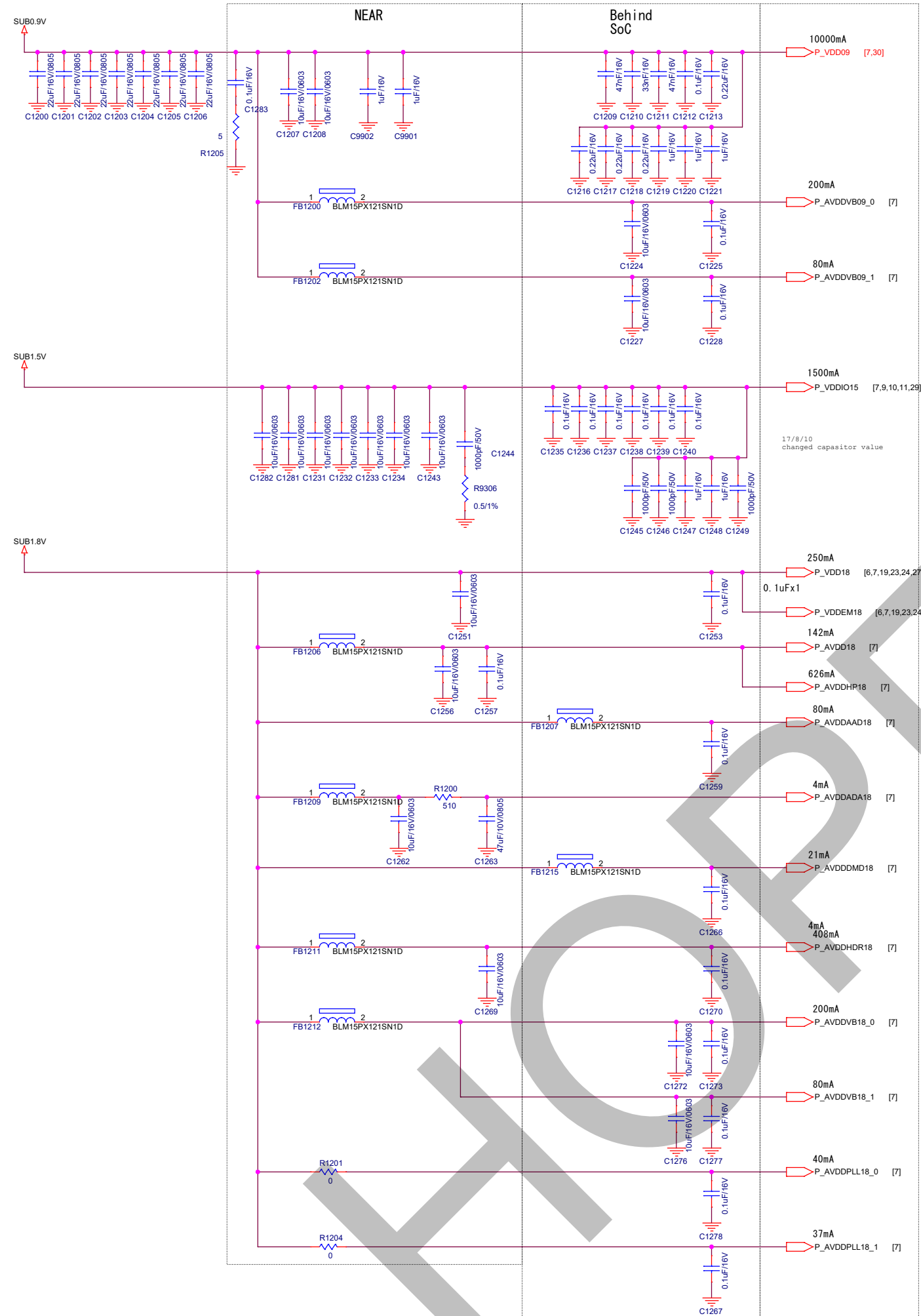
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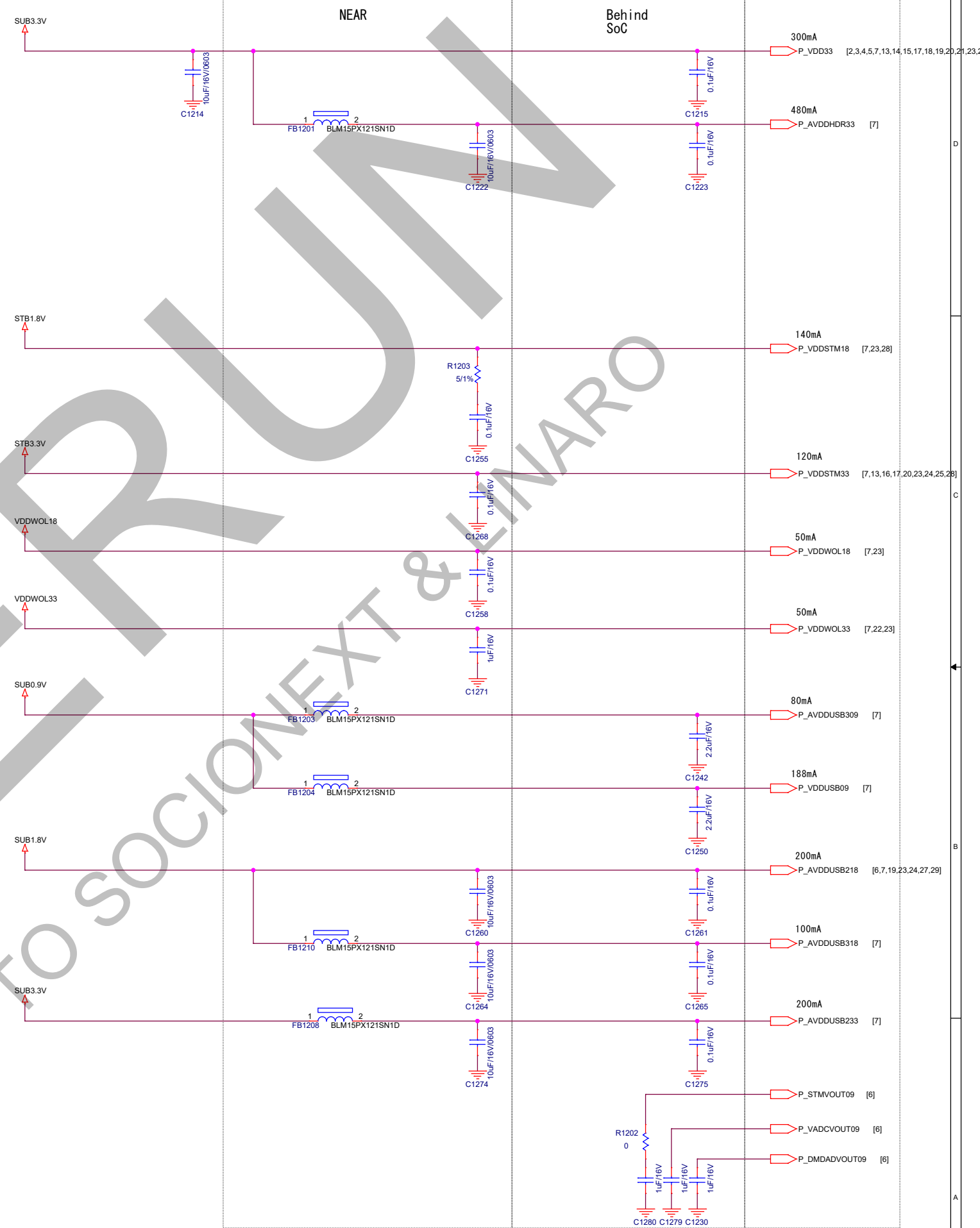
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PWR

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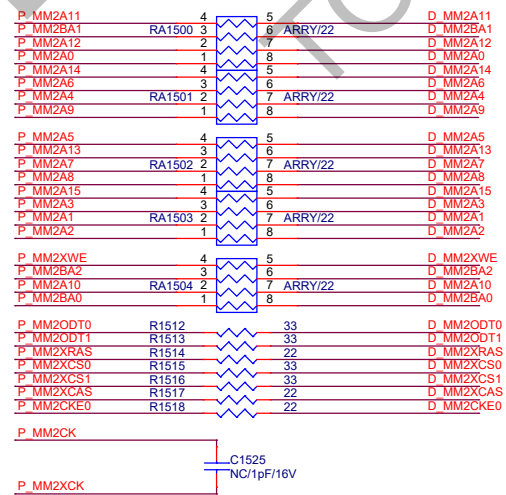
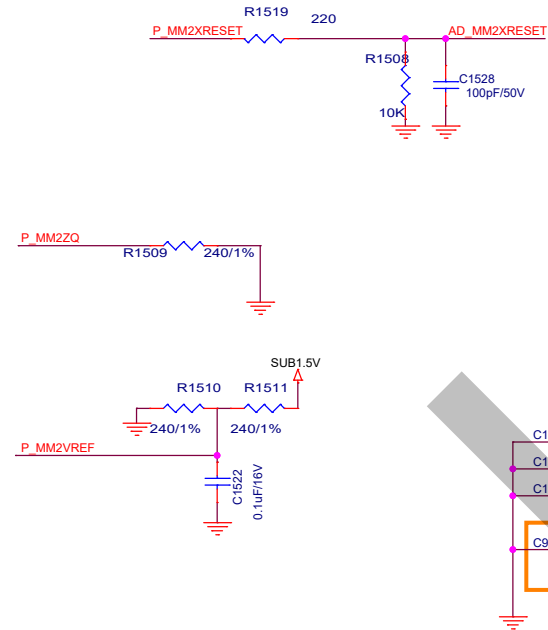
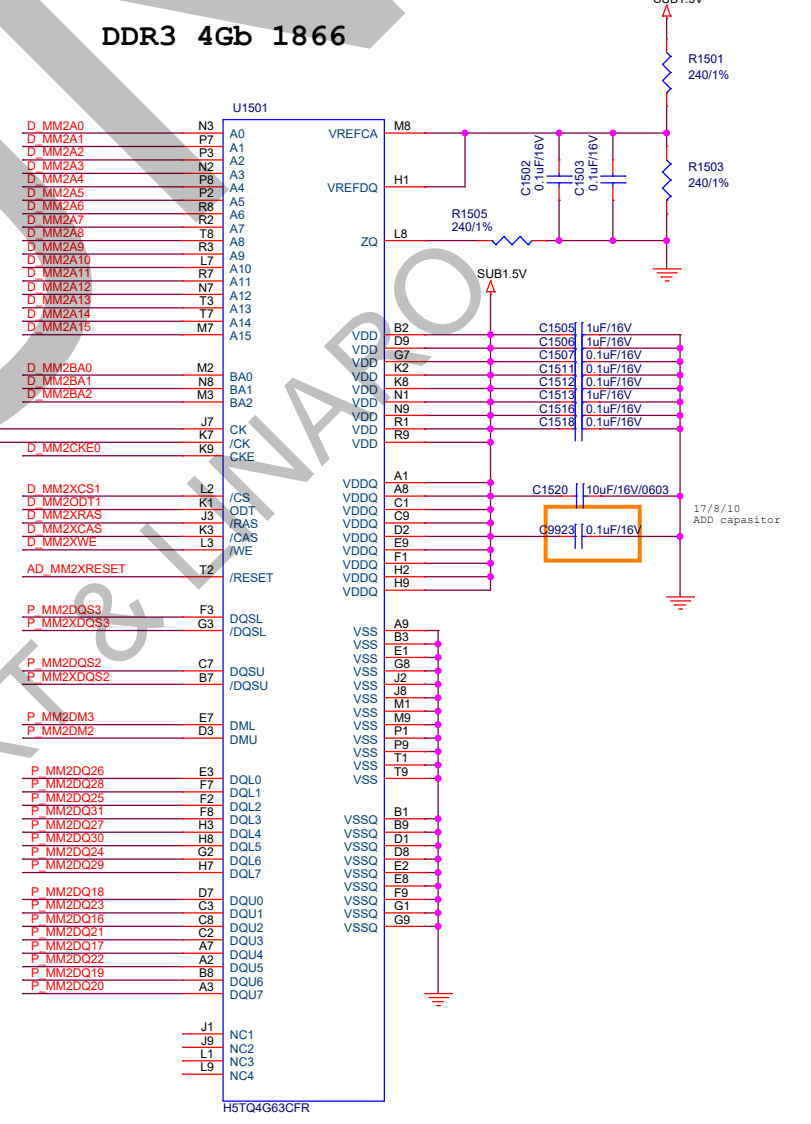
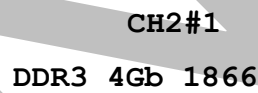
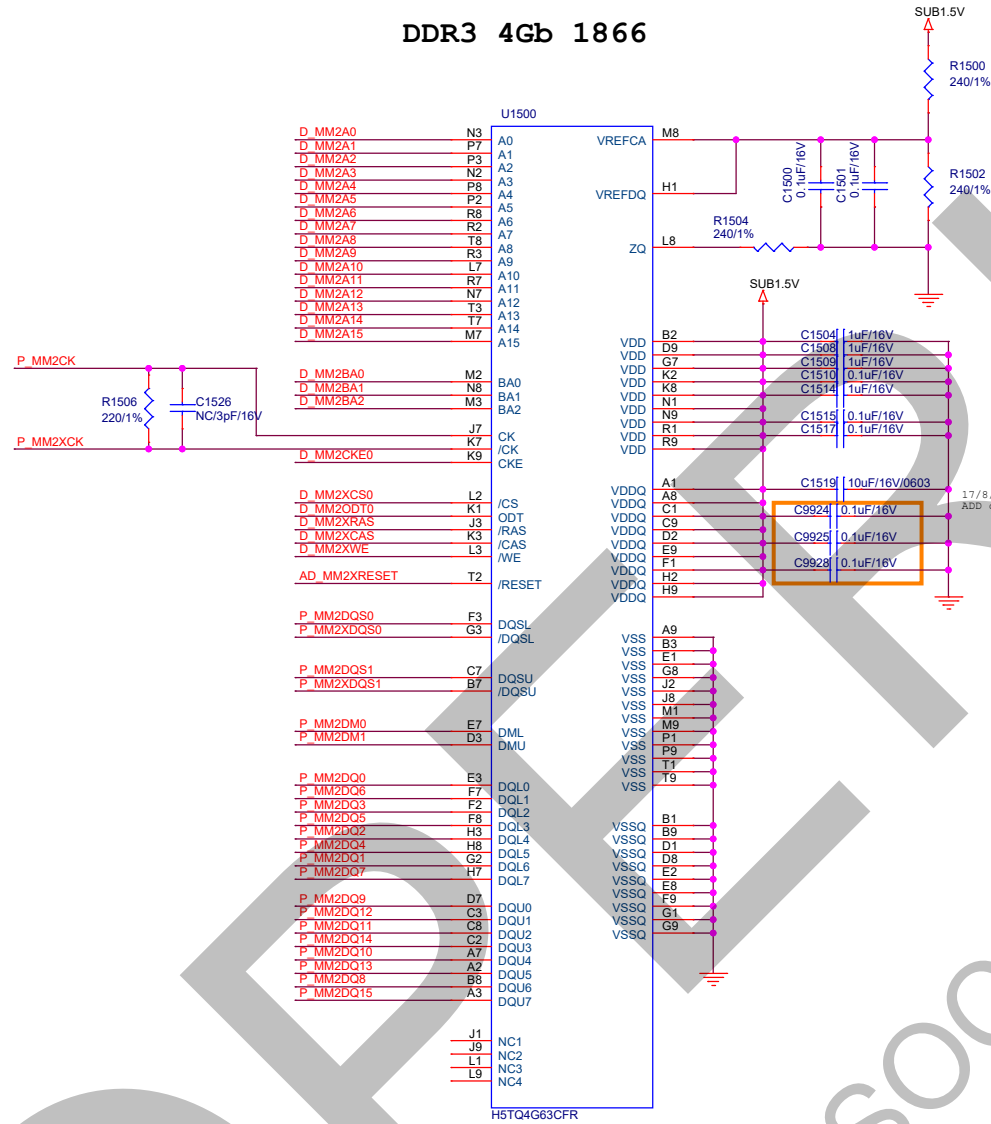
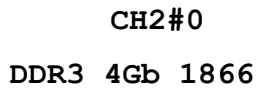
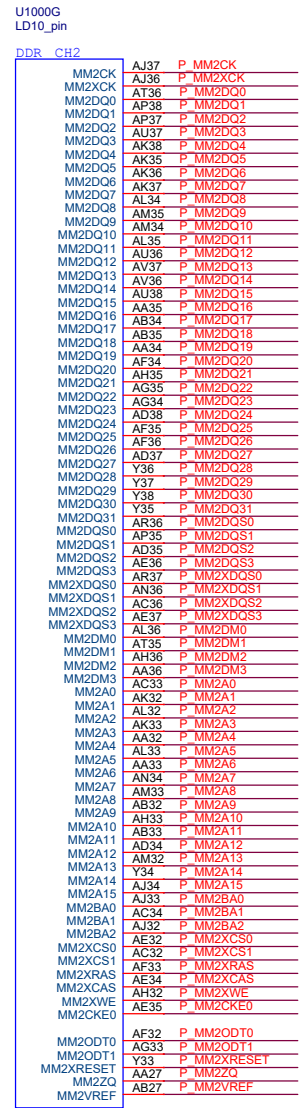
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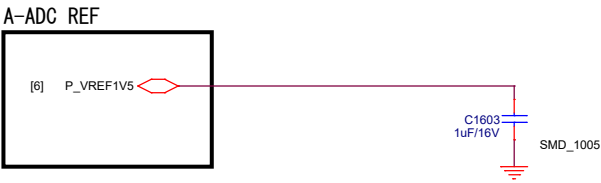
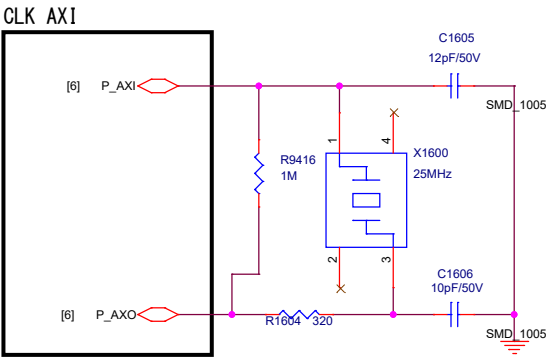
Rev:

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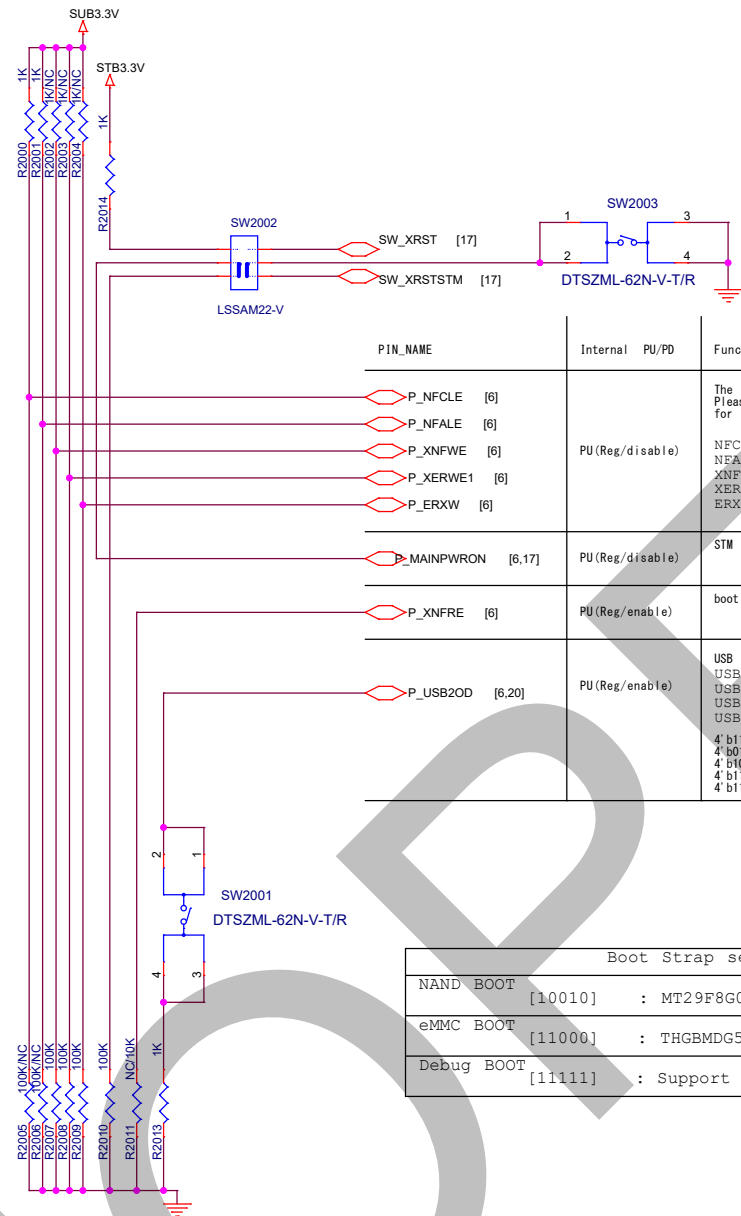
A2

LD20 DDR3
IF





LD20 Initial
SETUP



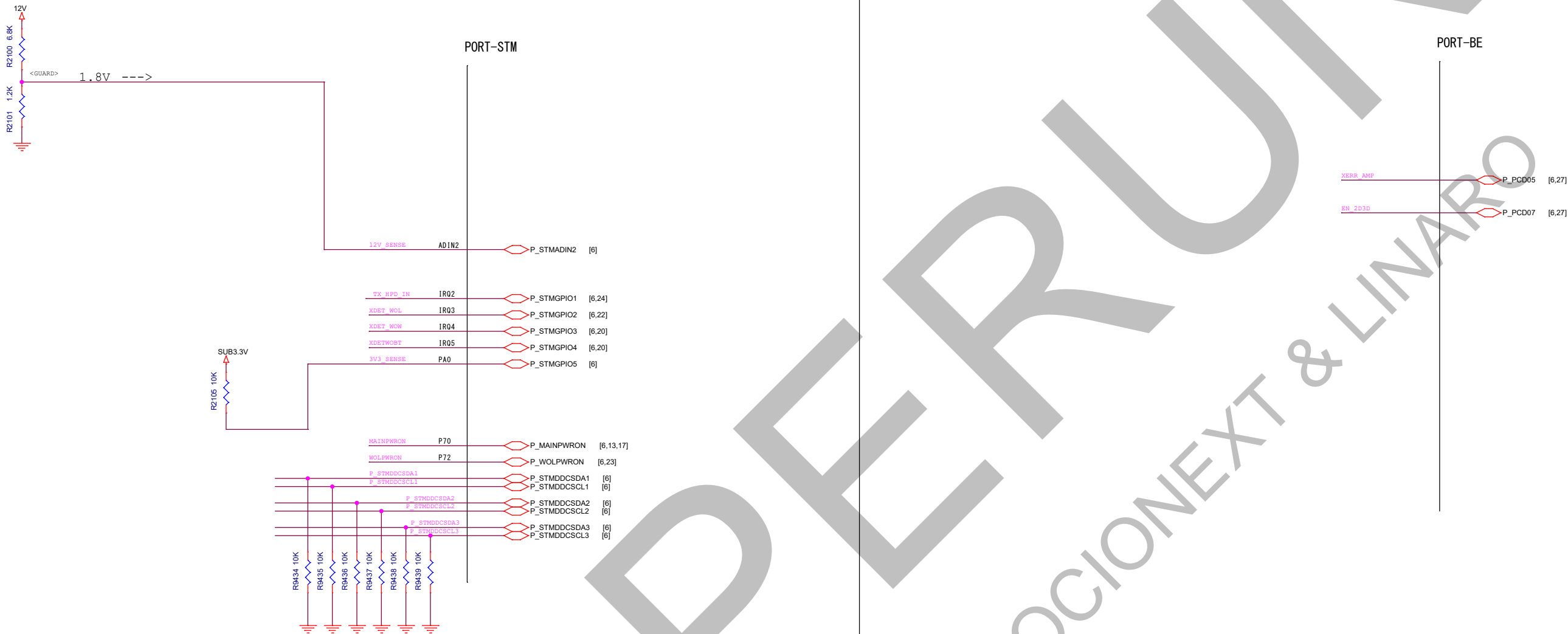
PIN_NAME	Internal	PU/PD	Function
P_NFCLE [6]			The LSI boot mode on the BE side will be changed. Please refer to the sheet of "LDdb boot mode" for the detail specification
P_NFALE [6]			
P_XNFW [6]			
P_XERWE1 [6]			
P_ERXW [6]			
P_MAINPWON [6,17]		PU(Reg/disable)	NFCLE : boot_mode_sel[4] NFALE : boot_mode_sel[3] XNFW : boot_mode_sel[2] XERWE1 : boot_mode_sel[1] ERXW : boot_mode_sel[0]
P_XNFRE [6]		PU(Reg/disable)	STM boot mode select 0 = STM boot 1 = BE boot
P_USB2OD [6,20]		PU(Reg/enable)	boot mode select 0 = debug 1 = default
		PU(Reg/enable)	USB Boot Port Select USB3OD : XUSBBOOT[3] USB2OD : XUSBBOOT[2] USB1OD : XUSBBOOT[1] USB0OD : XUSBBOOT[0] 4'b1111 = Normal 4'b0111 = USB Port3 4'b0111 = USB Port2 4'b1011 = USB Port1 4'b1110 = USB Port0

Boot Strap setting		
NAND BOOT [10010]	:	MT29F8G08ADADAH4 (Micron)
eMMC BOOT [11000]	:	THGBMDG5D1LBAIL (TOSHIBA)
Debug BOOT [11111]	:	Support card

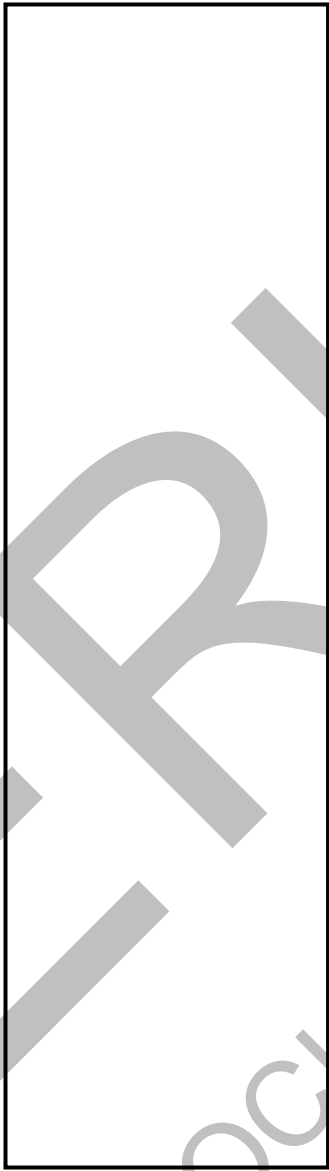
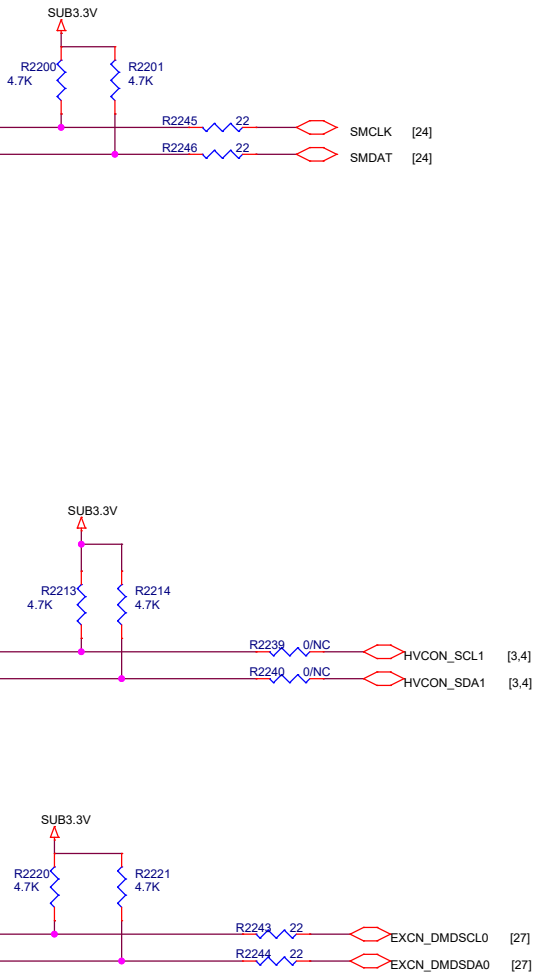
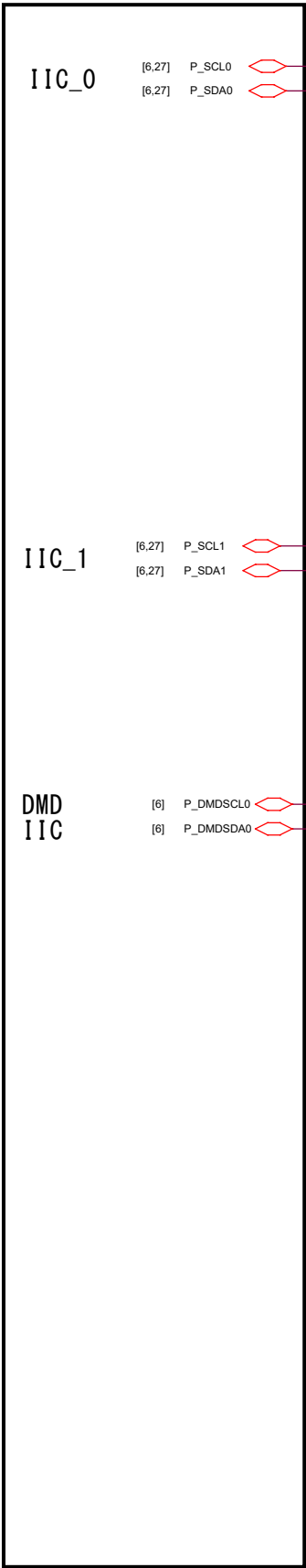
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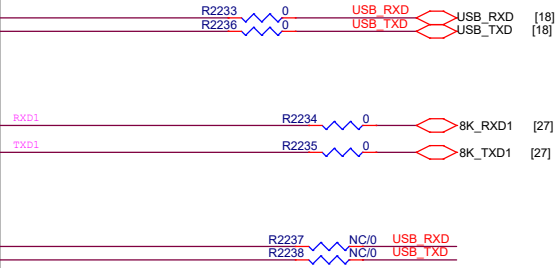
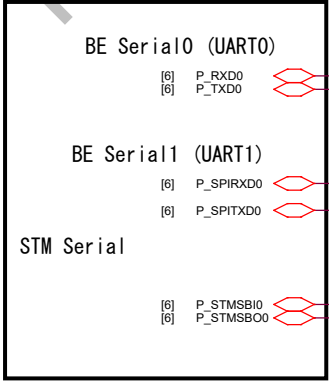
LD20
Port



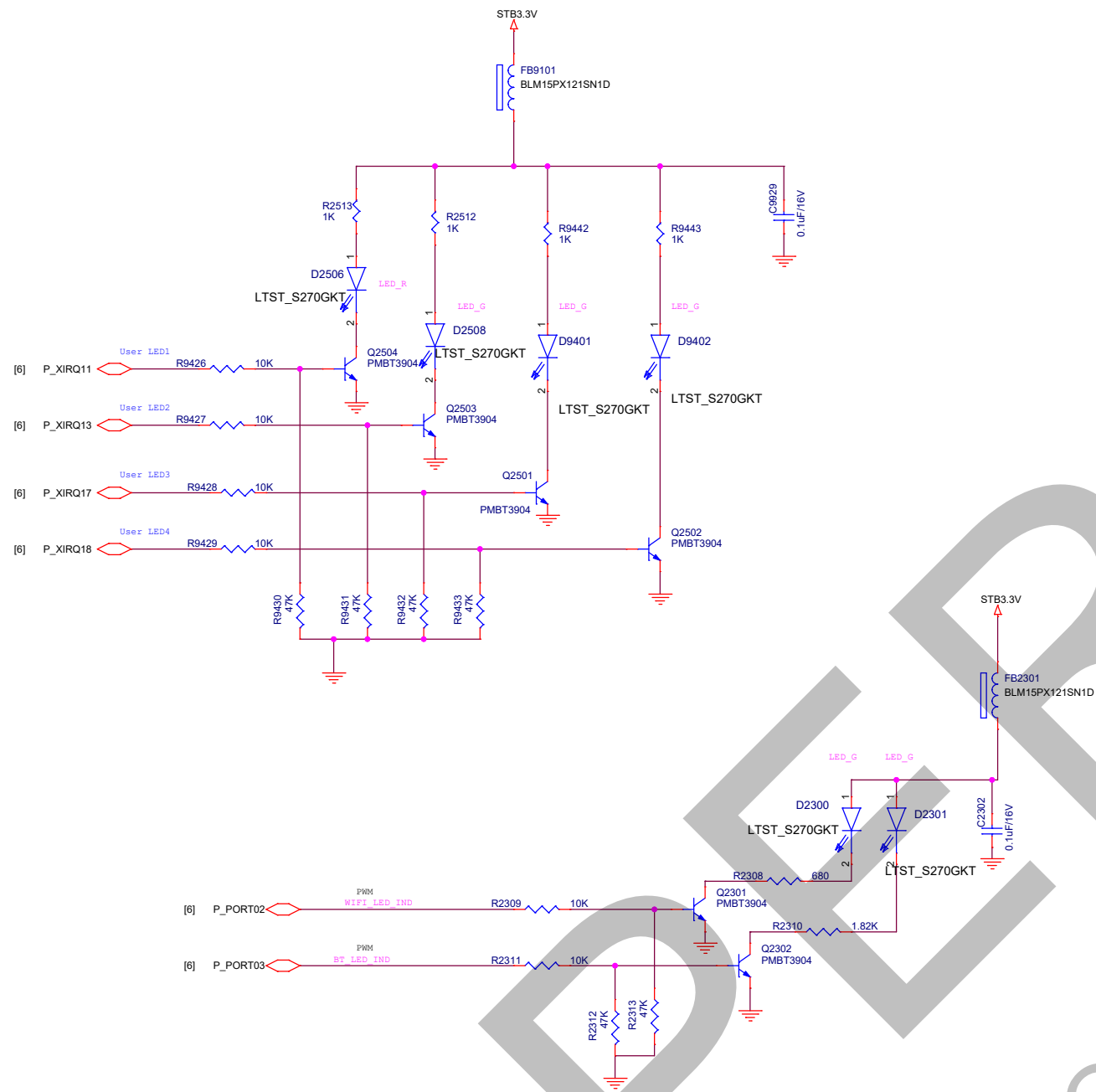
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Serial

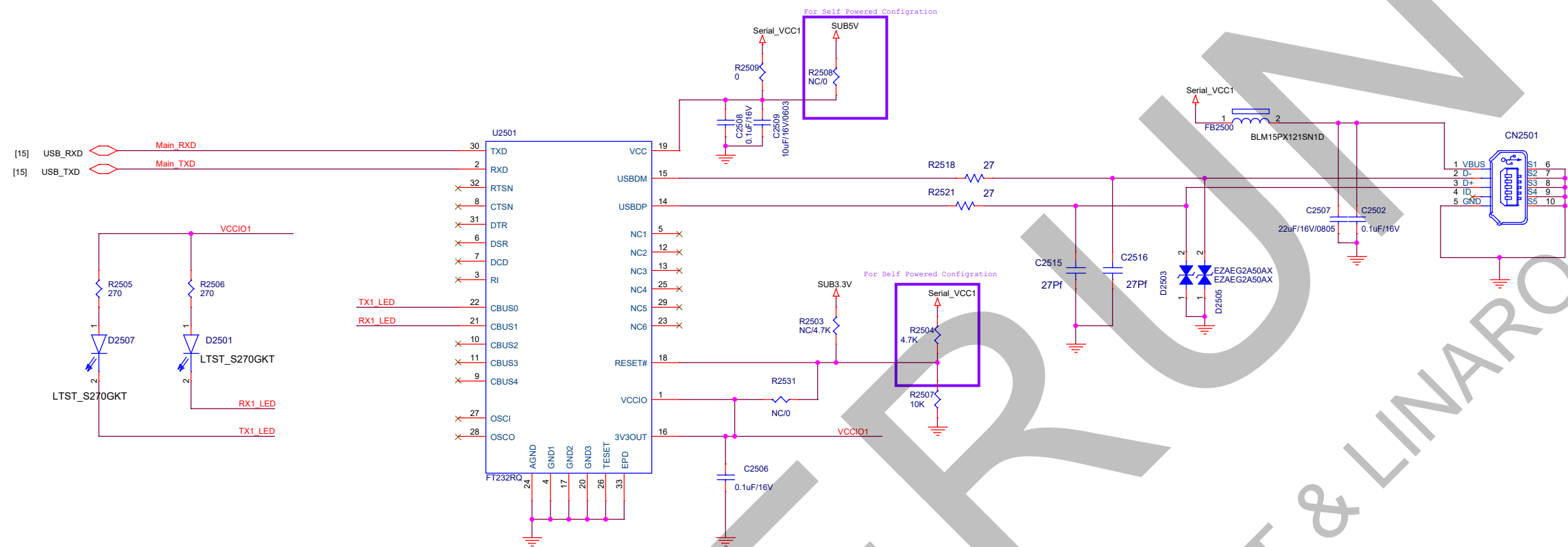


USER LEDS

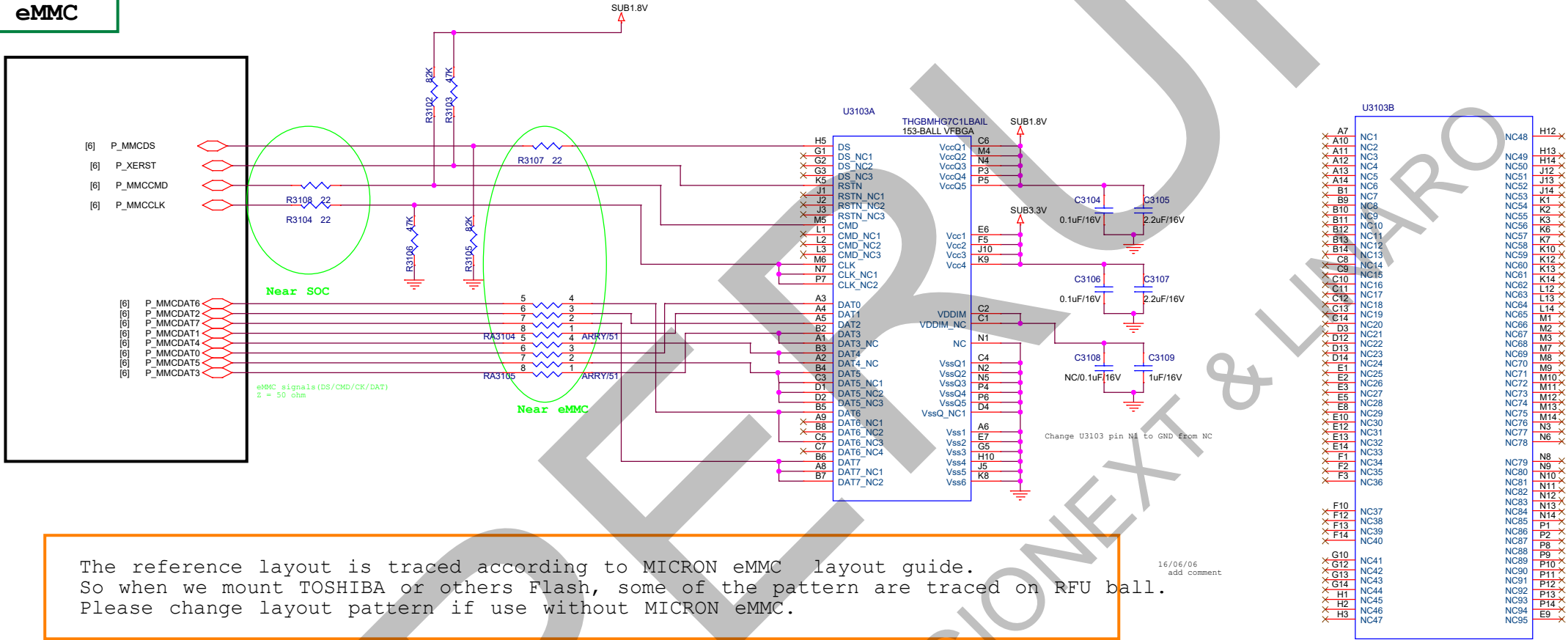


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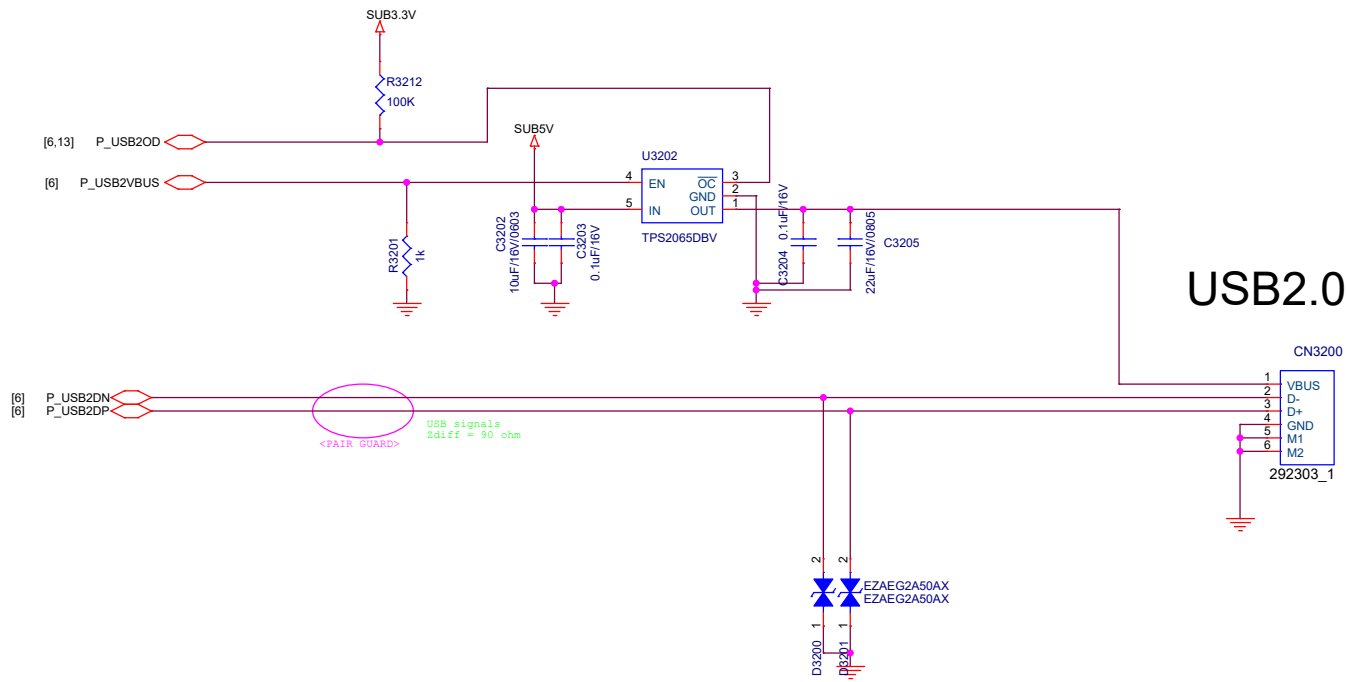


eMMC



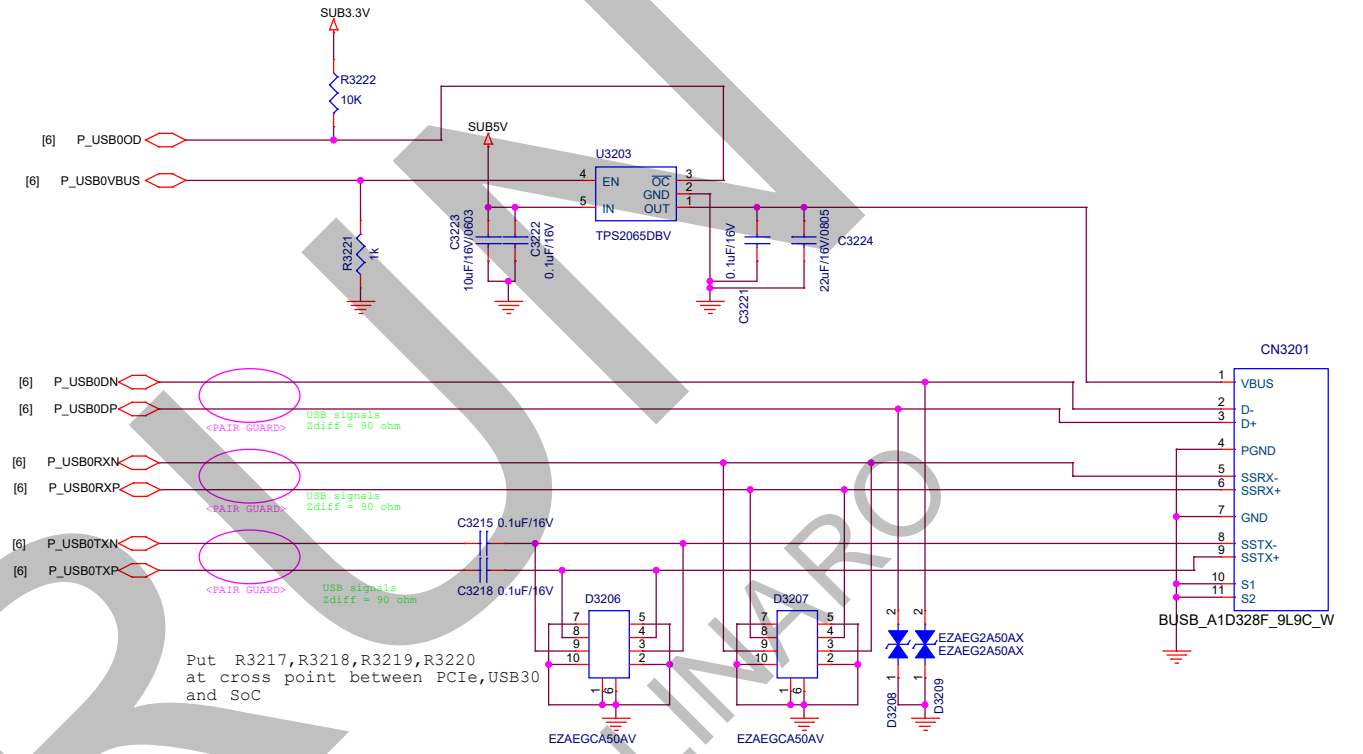
USB

USB 2

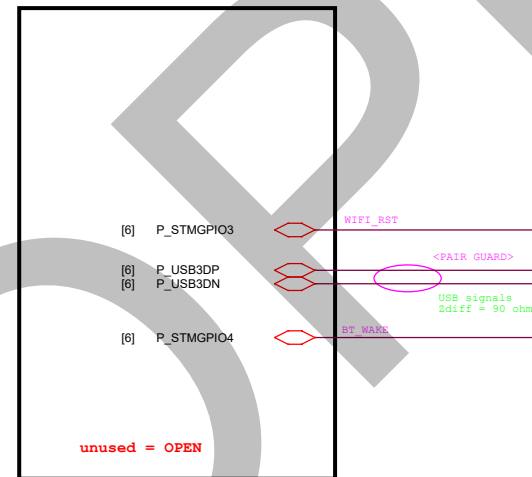


USB2.0

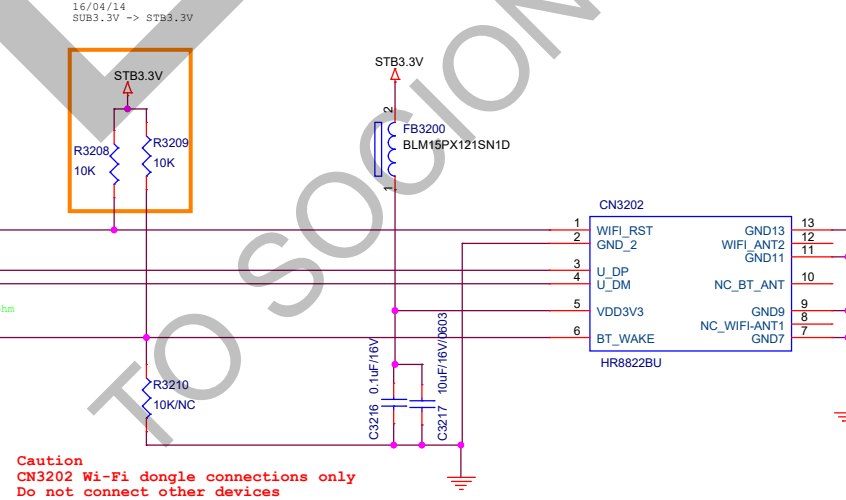
USB0



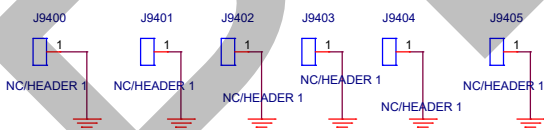
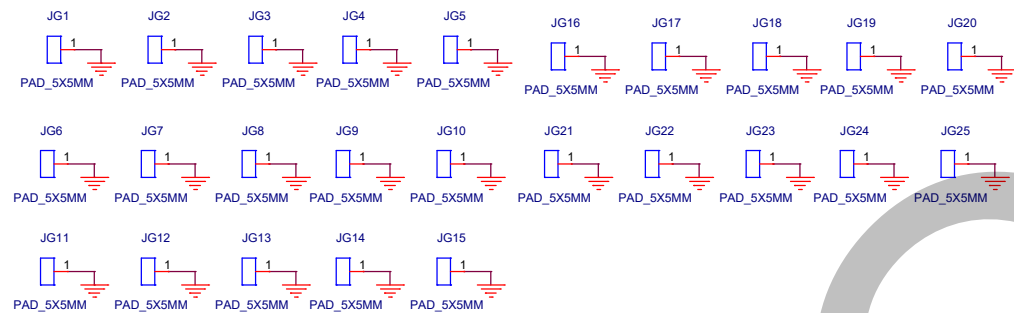
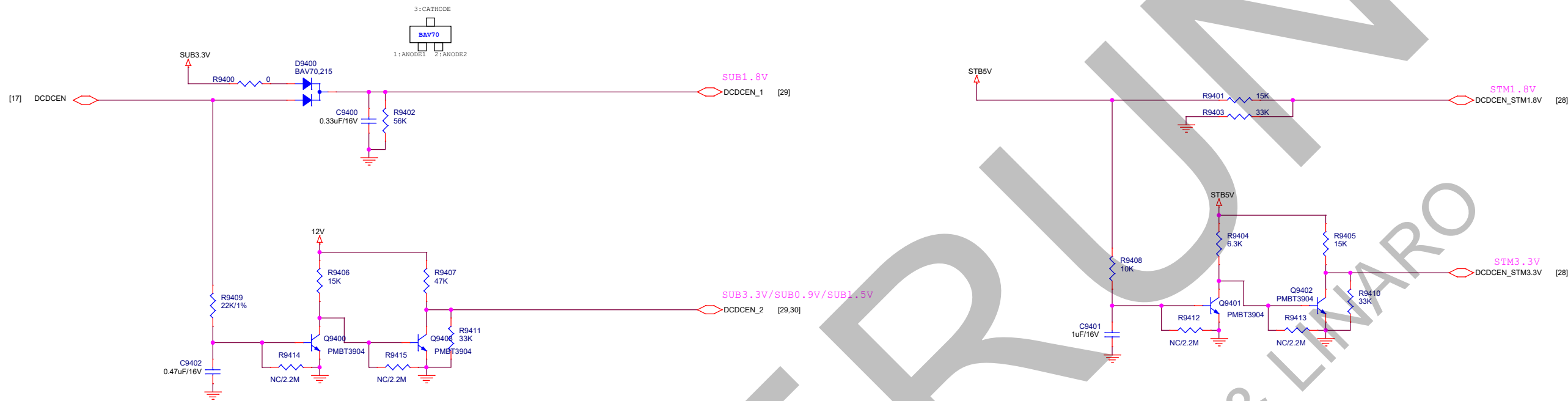
USB3



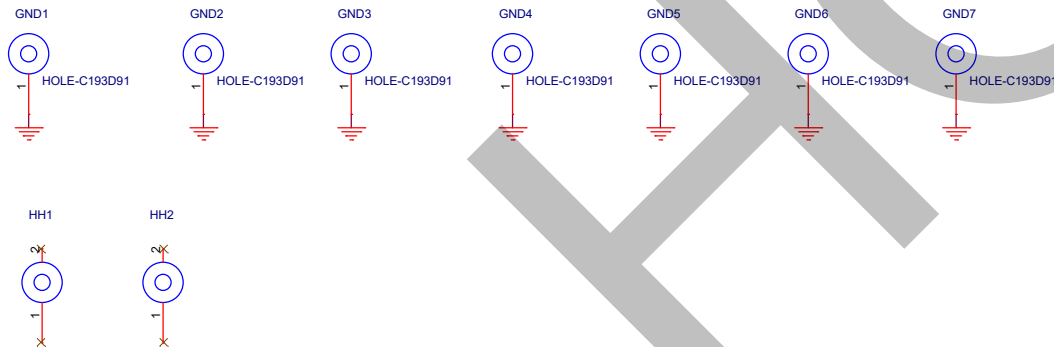
WIFI Module




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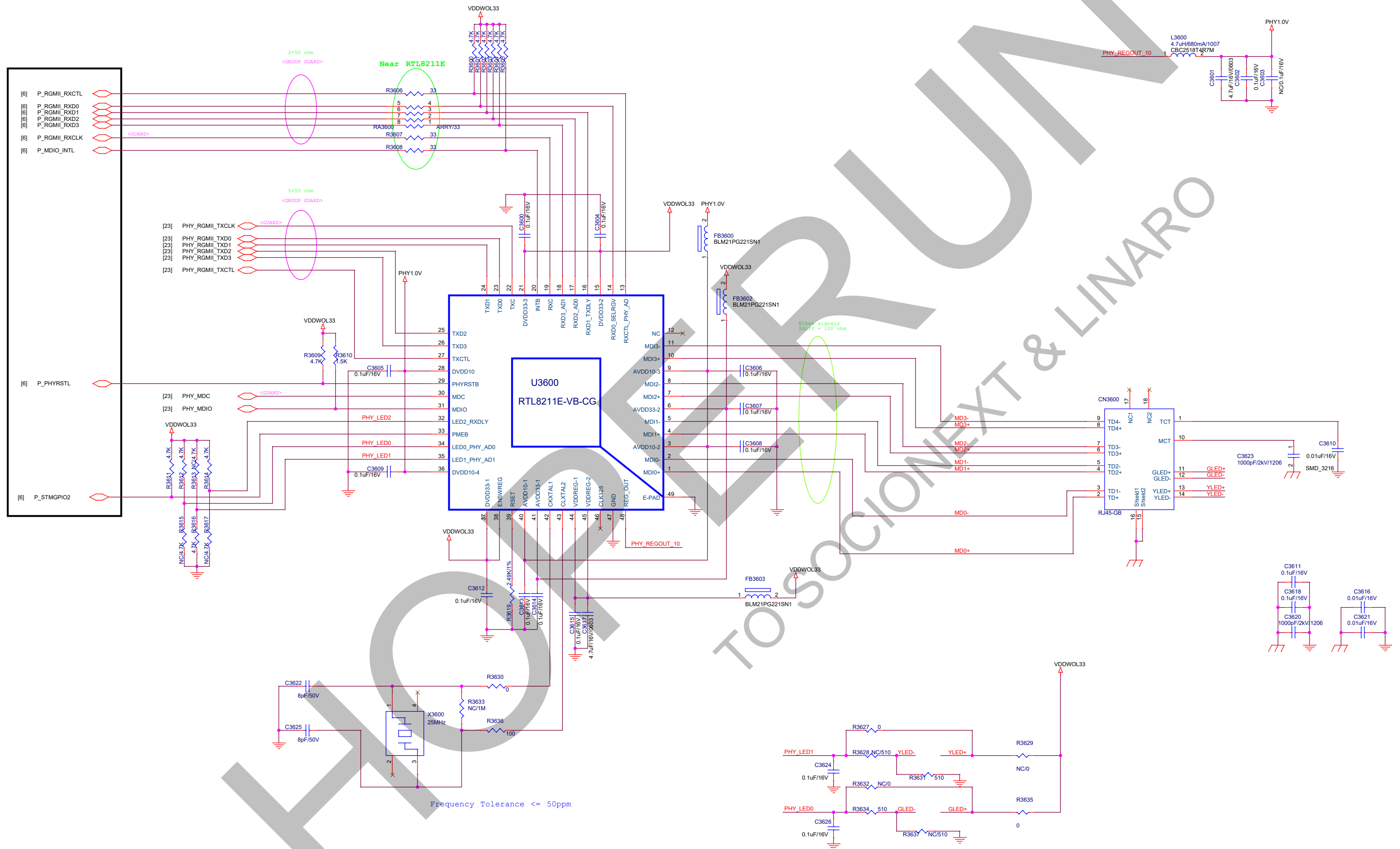
SCREW HOLES




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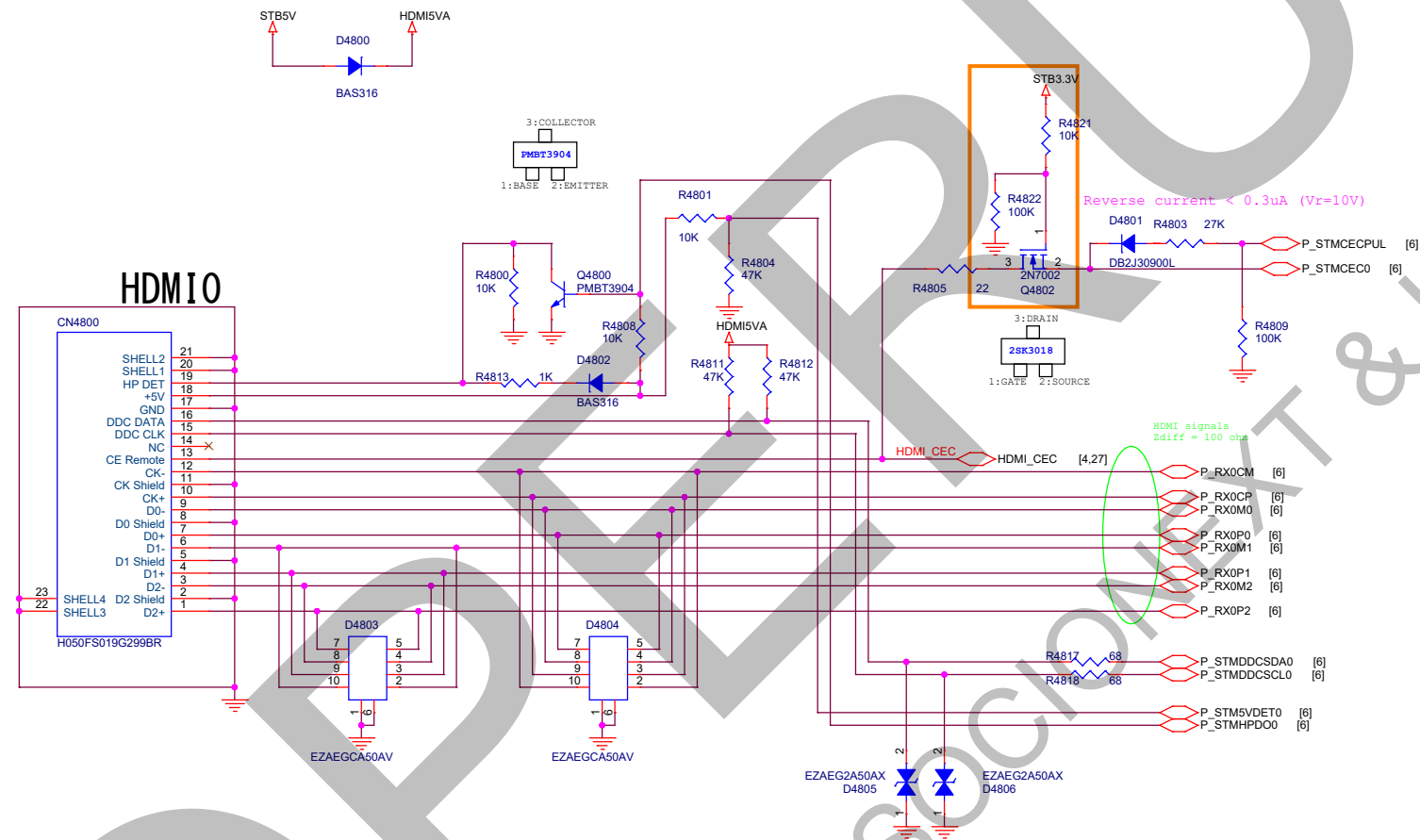
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5
Ether-PHY (RTL8211E-VB)

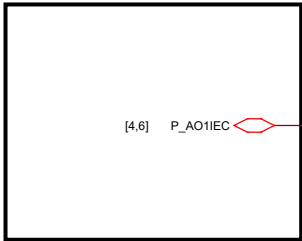


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SPDIF out



[4,6] P_AO1IEC

<GUARD>

R5401

0

SUB3.3V

FB5400
BLM21PG221SN1

R5400
10K

C5400
0.1uF/16V

SMD_1005

CN5400

VCC

VIN

GND

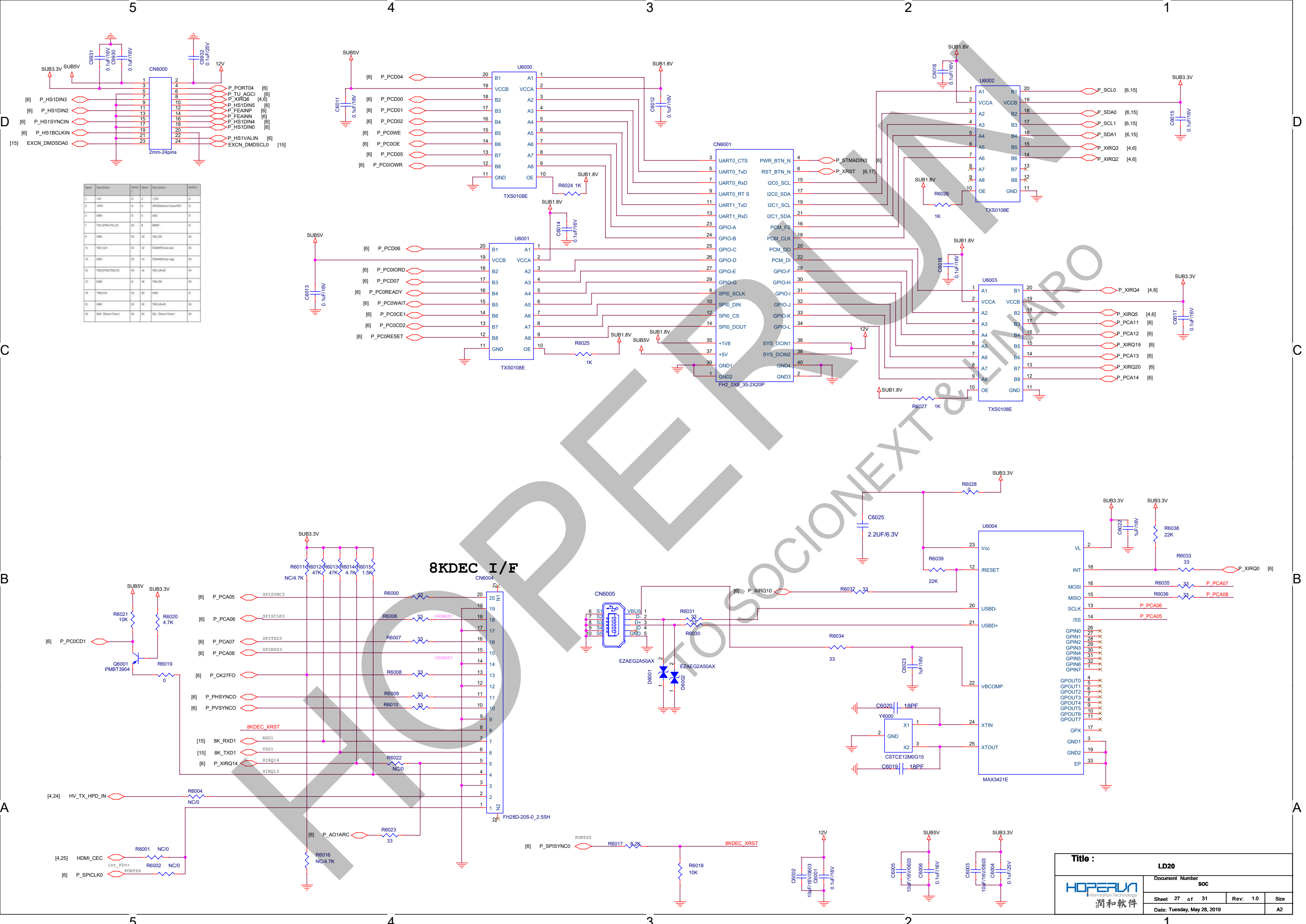
M1

M2

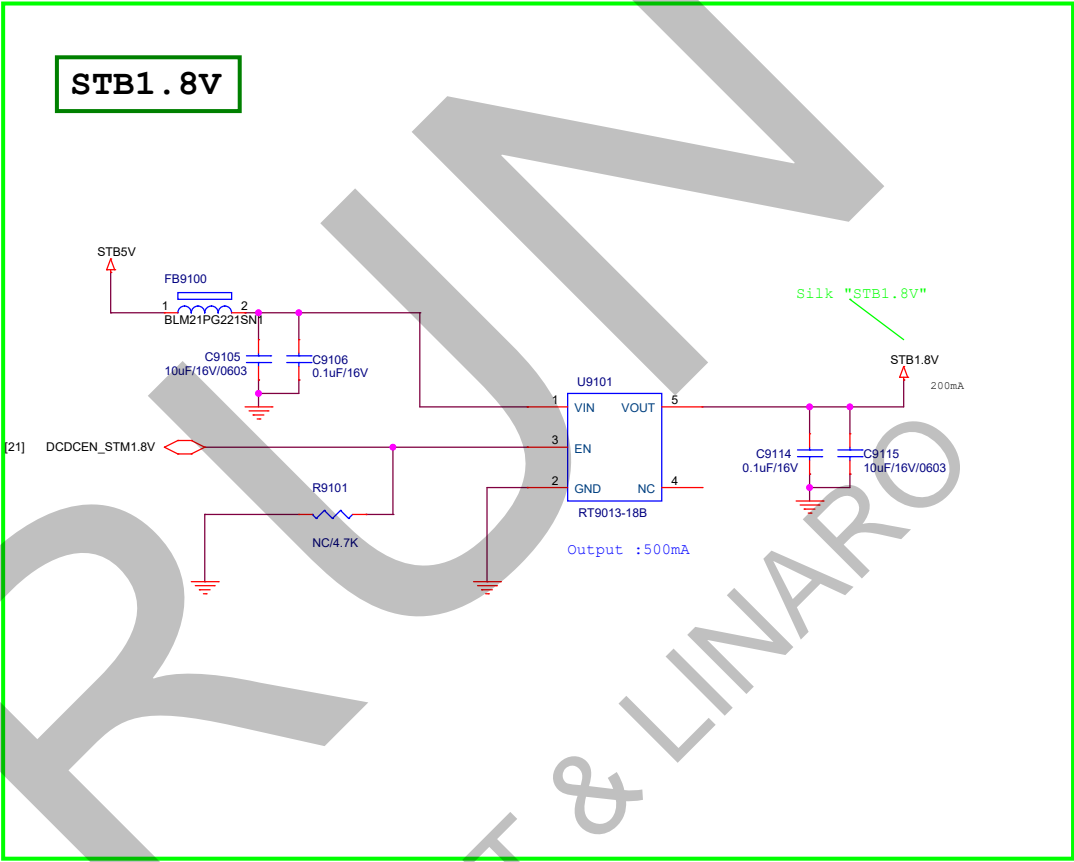
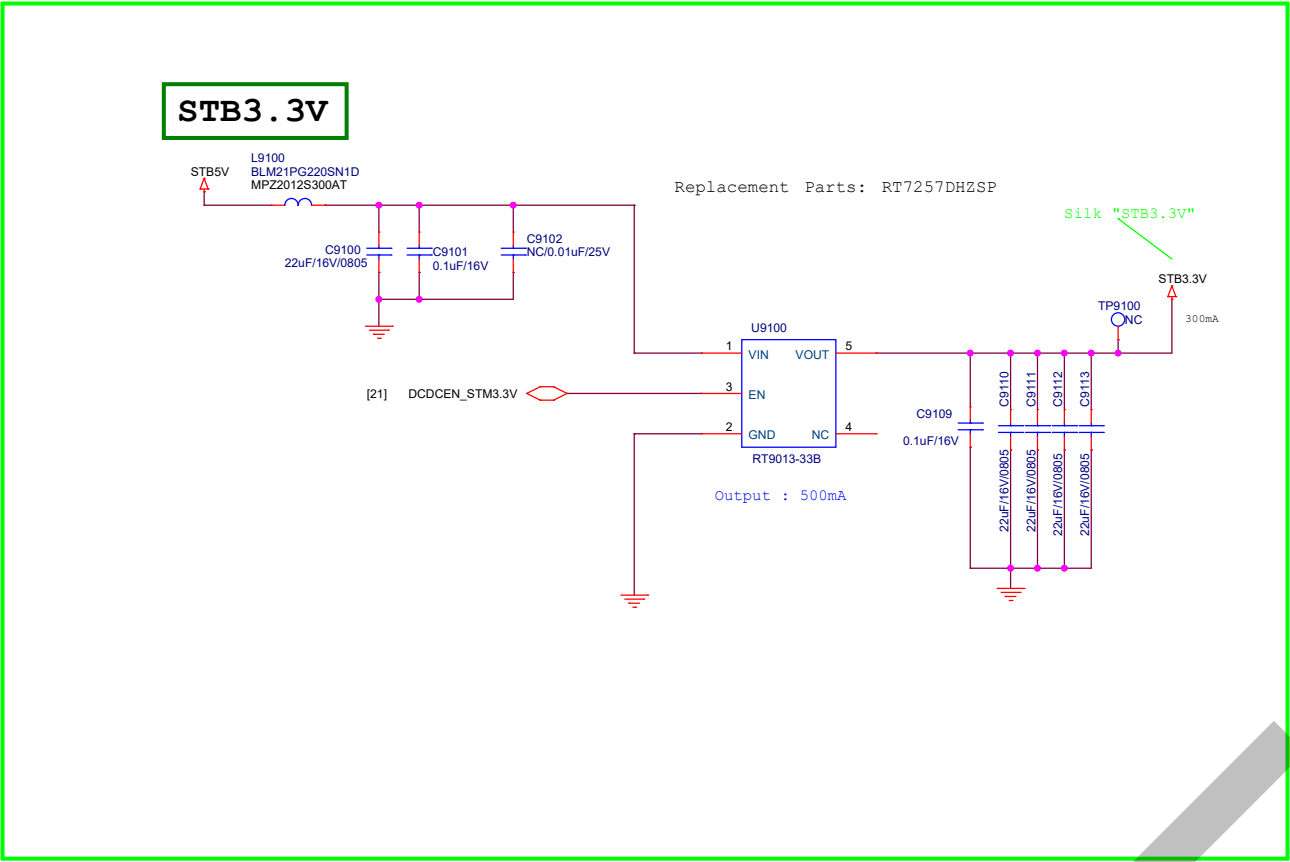
M3

8161103_T0002D_R

SPDIF
OUTPUT



DCDC (STM)

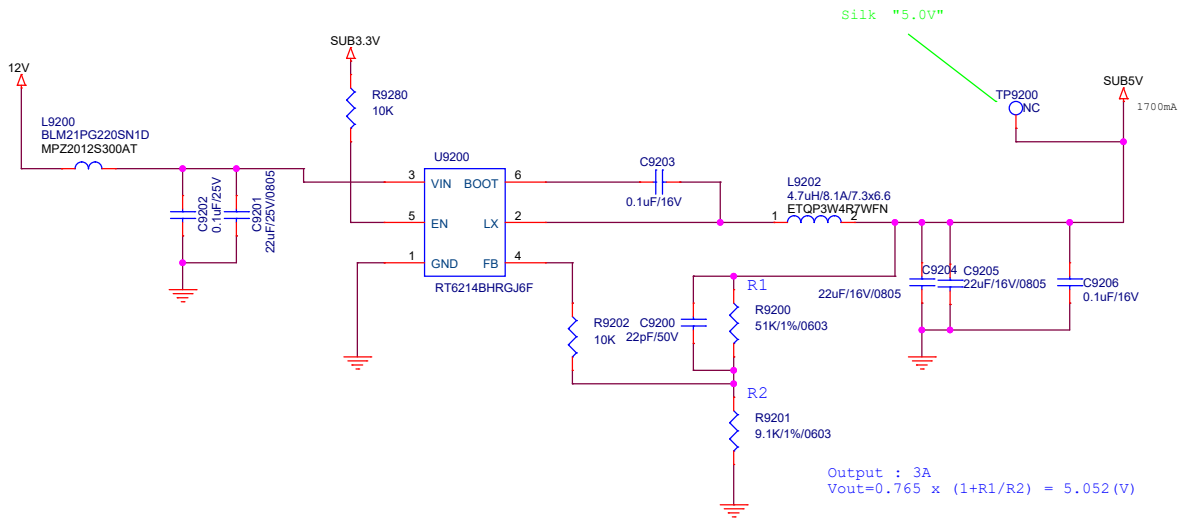


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DCDC (BE1)

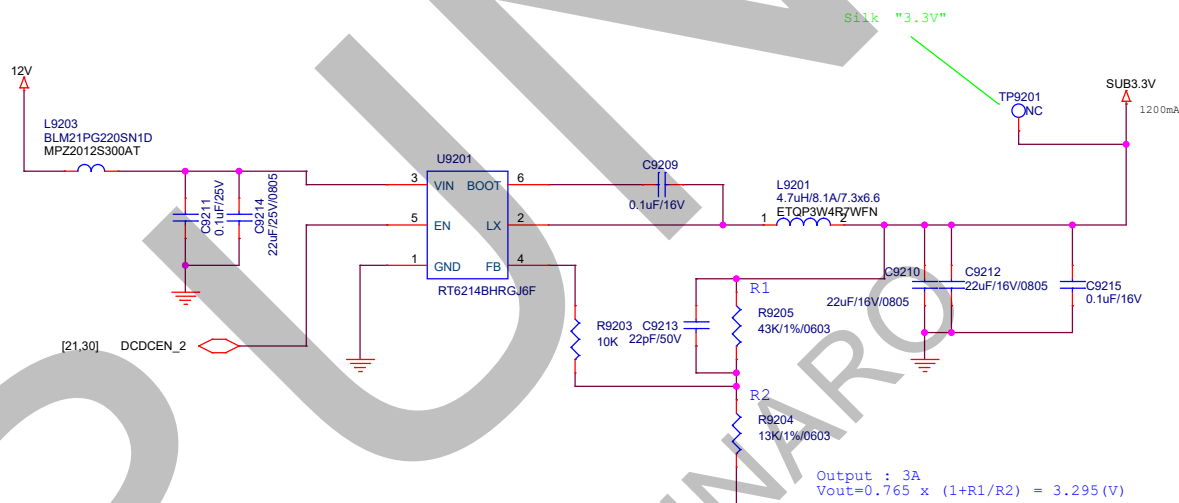
5.0V

R1,R2: Chip size 0603(1608)



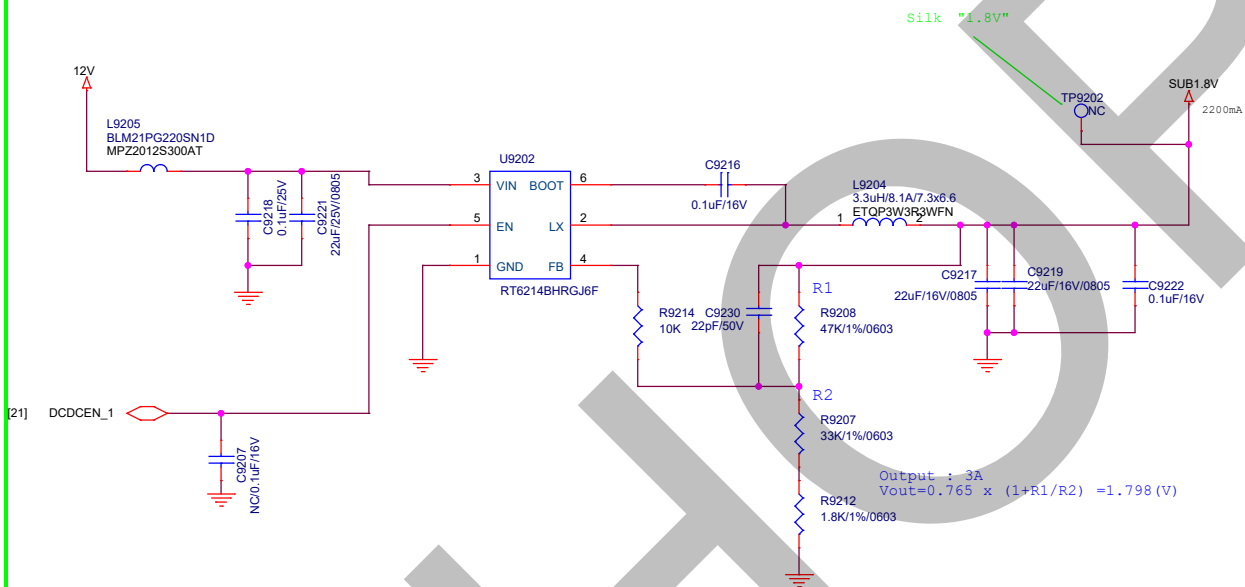
3.3V

R1,R2: Chip size 0603(1608)



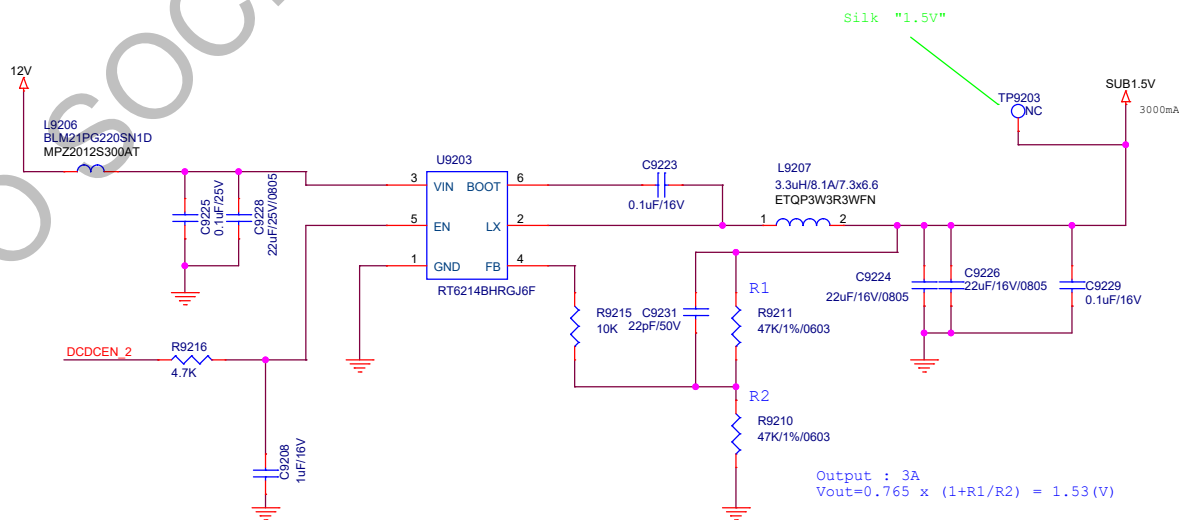
1.8V

R1,R2: Chip size 0603(1608)



1.5V

R1,R2: Chip size 0603(1608)



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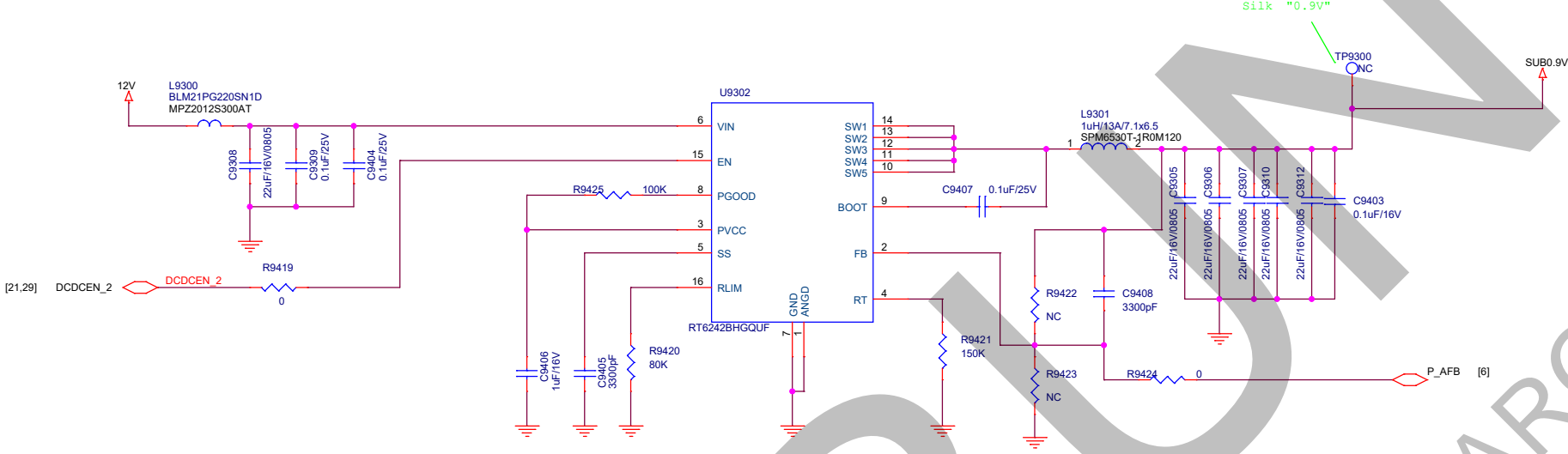
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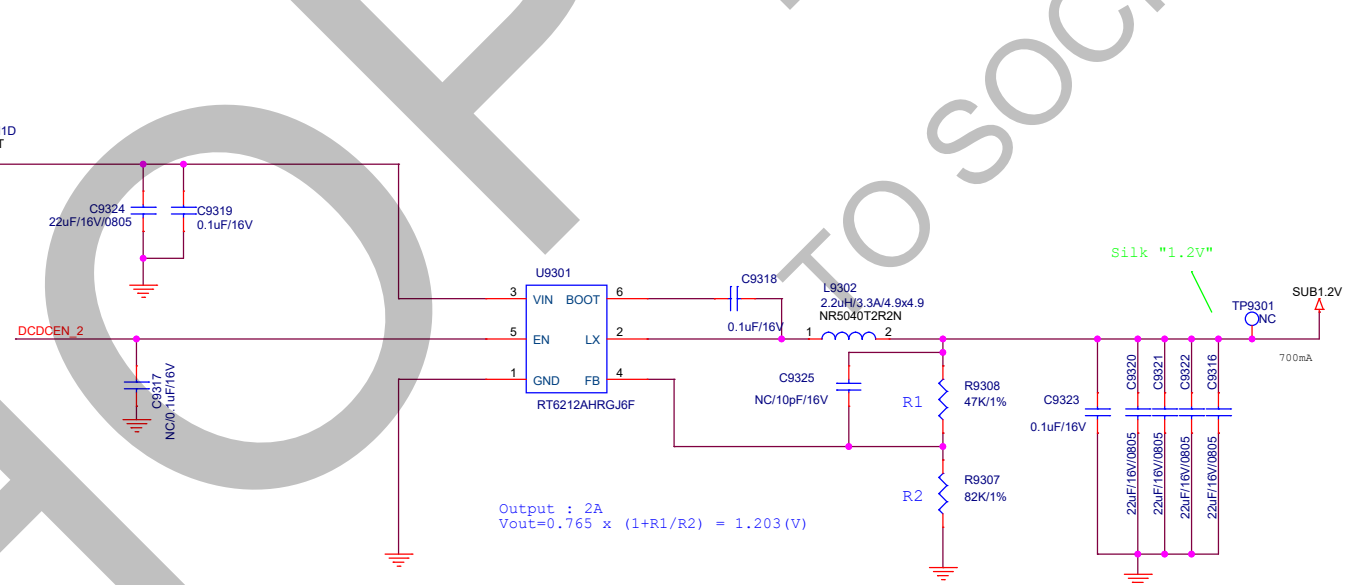
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DCDC (BE2)

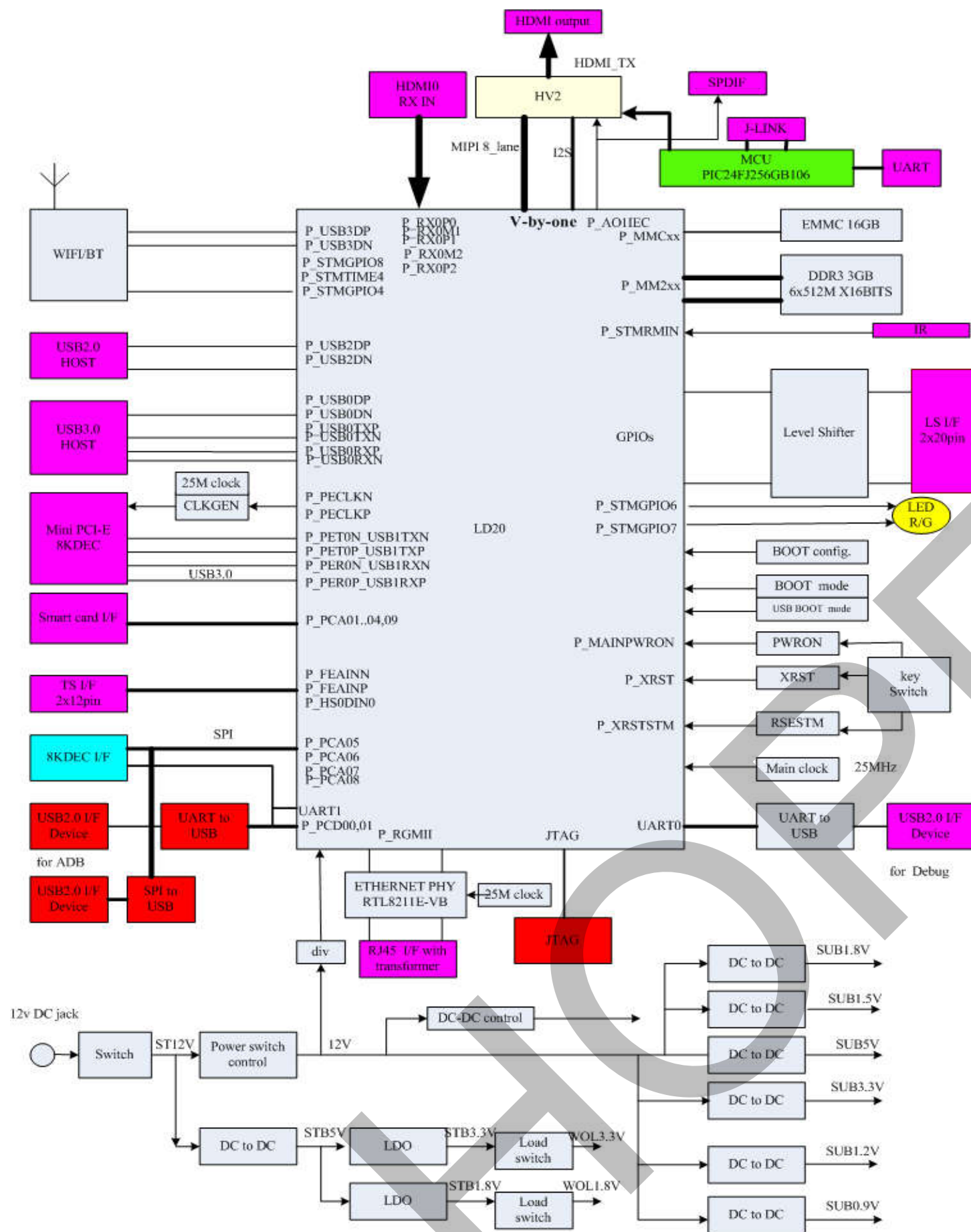
0.9V



1.2V



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LD20~
'18/4/14

- P.6 Add P_XIRQ19 and P_XIRQ20 to correspond nets of P.25。」
- P.17 Add R2447, R2448, D2403 and D2404 for power supply LED indicator.
- P.18 Add U2502 (FT230XQ), CN2502 micro USB circuits for USB ADB.
- P.25 Change CN5400 SPDIF output pin with current part number。」
- P.26 Change CN6002 1X12Pin connector package with FH2.0X4.6R-1X12P。」
- P.26 Add SPI to USB circuits with MAX3421E.

LD20~
'18/5/15

- P.18 Change UART to USB circuits with flow control for USB ADB。」

LD20~
'18/6/16

- P.3 Add MCU -PIC24FJ256GB106 circuits to control HV2

LD20~
'19/5/14

- P.25 Remove CN2502 all related circuits
- P.16 Add 4 User LEDs and related circuits
- P.16 Add LEDs for WiFi and BT, be controlled by PWMs of SoC.
- P.18 Remove IR related circuits, Page 23 becomes page 18.
- P.27 Remove smartcard related circuits
- P.27 The tuner Interface be changed to follow up 96Boards TV spec 2.0
- P.27 Change WiFi-BT module related circuits
- P.22 Mounting "BLM21PG221SN1" in FB3600, and change R3700 to 33ohm
- P.13 SW2001 and SW2003 change to the bigger components
- P.27 Modified Lever shift circuit U6000~U6003 OE Pins connection
- P.29 Modified the CAPs C9201/C9214/C9221/C9228 Voltage value from 16V to 25V.
- P.27 Modified U6002 Pin-B5 connection from net P_XIRQ1 to P_XIRQ3

LD20~
'19/5/17

- P.27 Removed the U6005 related parts and mount R6028 = 0ohm
- P.27 Removed D9401.
- P.03 Exchanged the Nets PIC_TXD and PIC_RXD on the pin of J0201
- P.14 Add 10K pull-down resistances to the following nets
STMDDCSDA1/STMDDCSDA2/STMDDCSDA3
STMDDCSCL1/STMDDCSCL2/STMDDCSCL3

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