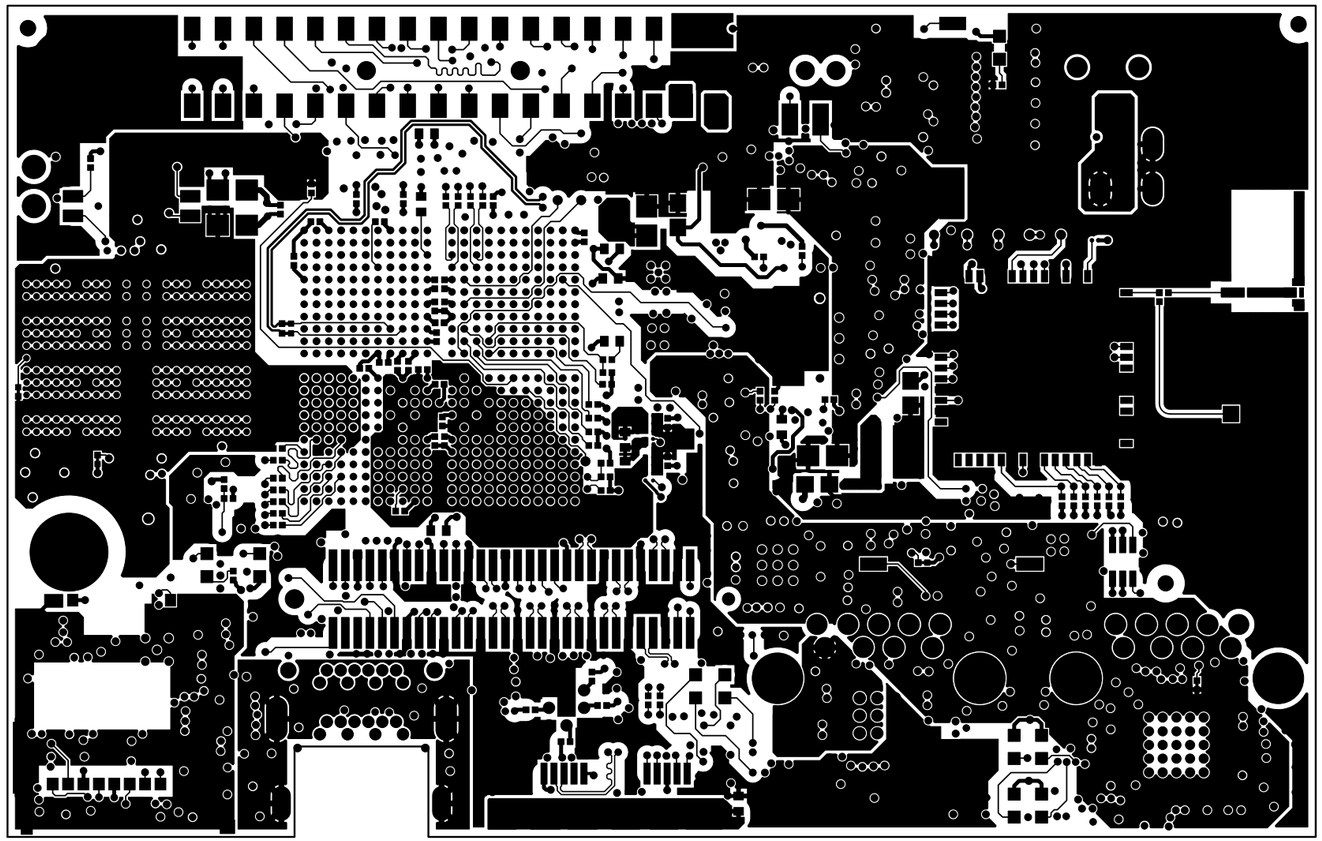
CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:47 2018 - (Untitled) : pwb-usdev-1_layer01.pho



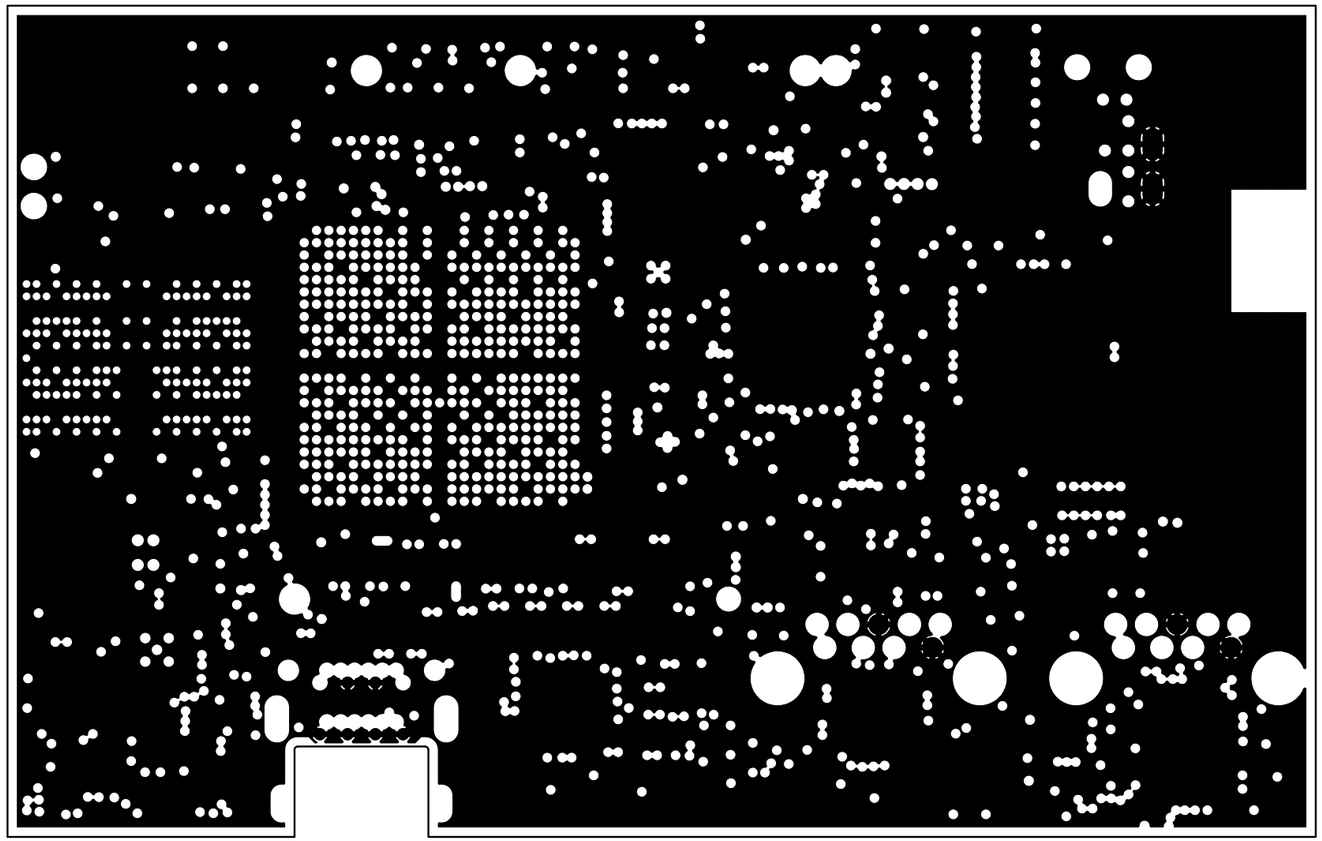
ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	

SHEET 1 OF 16

LAYER:

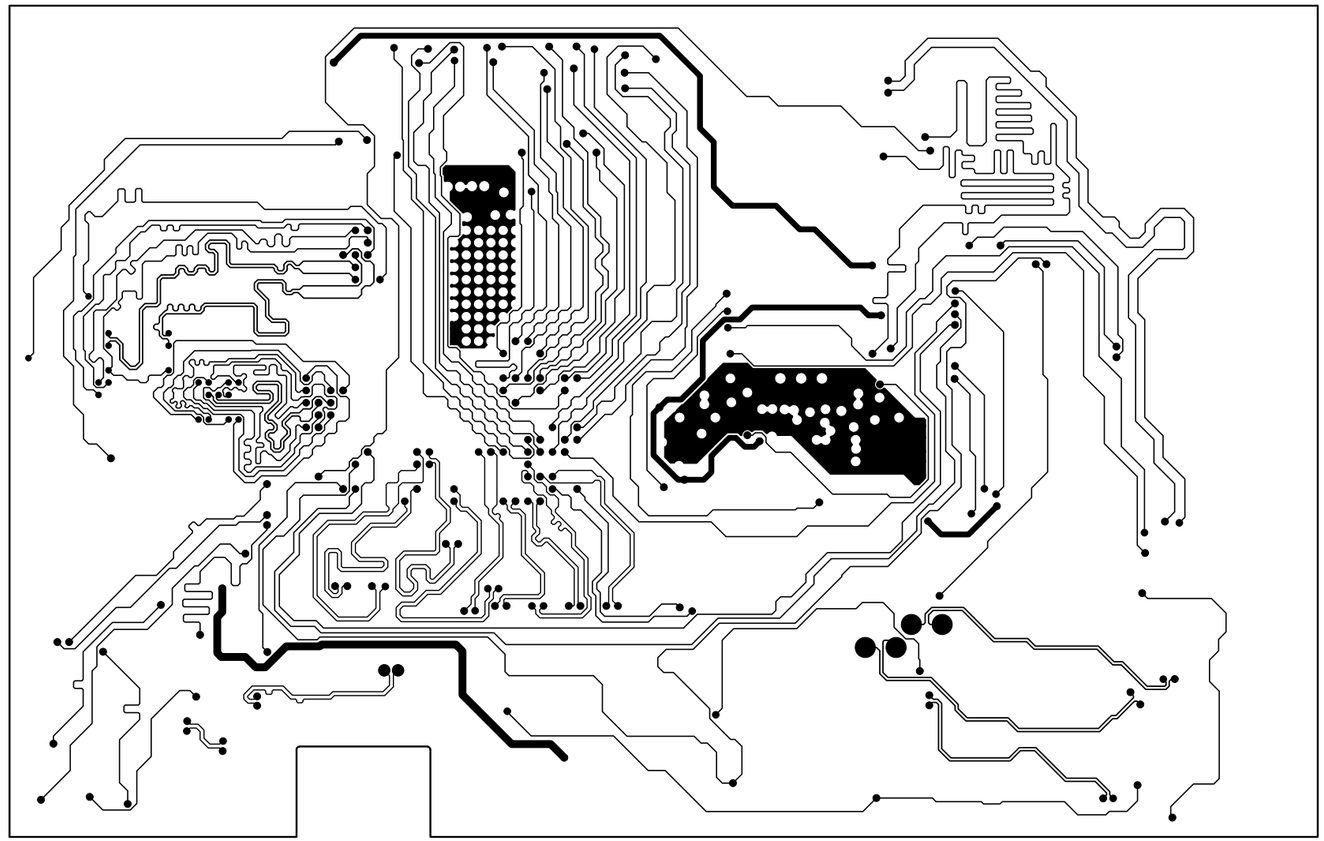
LAYER01 - ETCH LAYER 1 - (SIGNAL)

CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:47 2018 - (Untitled) : pwb-usdev-1_layer02.pho



ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	
SHEET 2 OF 16 LAYER: LAYER02 - ETCH LAYER 2 - (PLANE)	

CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:47 2018 - (Untitled) : pwb-usdev-1_layer03.pho



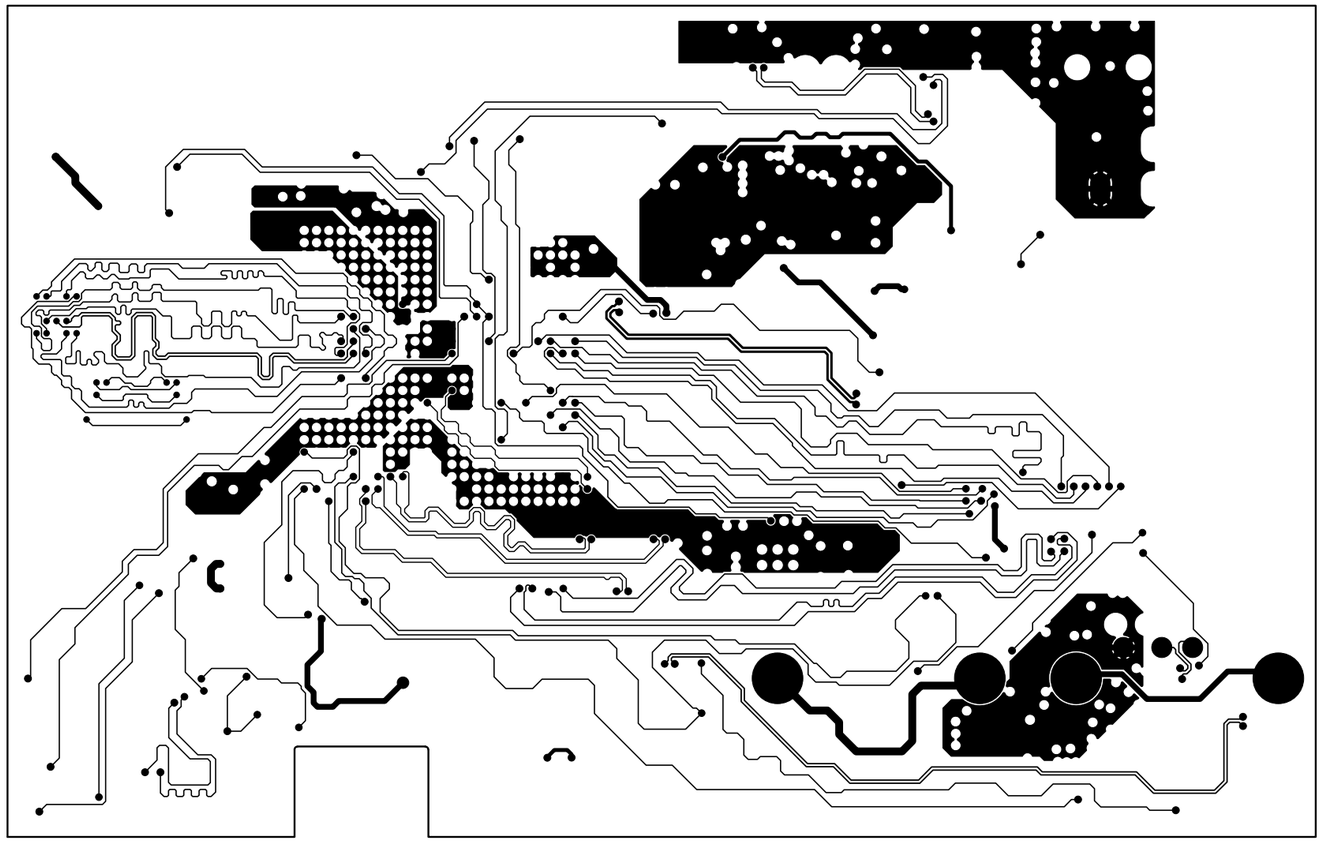
ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	

SHEET 3 OF 16

LAYER:

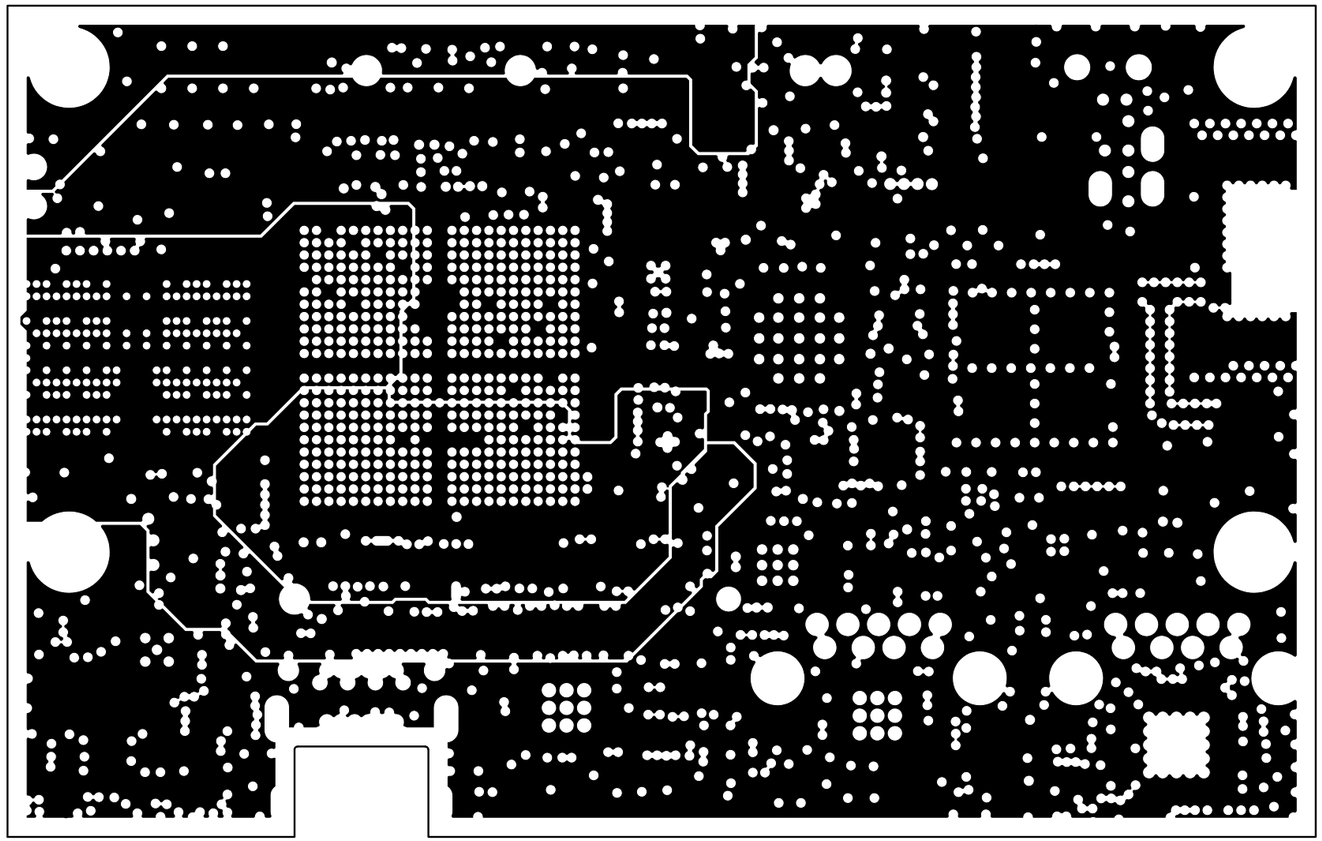
LAYER03 - ETCH LAYER 3 - (SIGNAL)

CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:47 2018 - (Untitled) : pwb-usdev-1_layer04.pho



ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	
SHEET 4 OF 16 LAYER: LAYER04 - ETCH LAYER 4 - (SIGNAL)	

CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:47 2018 - (Untitled) : pwb-usdev-1_layer05.pho



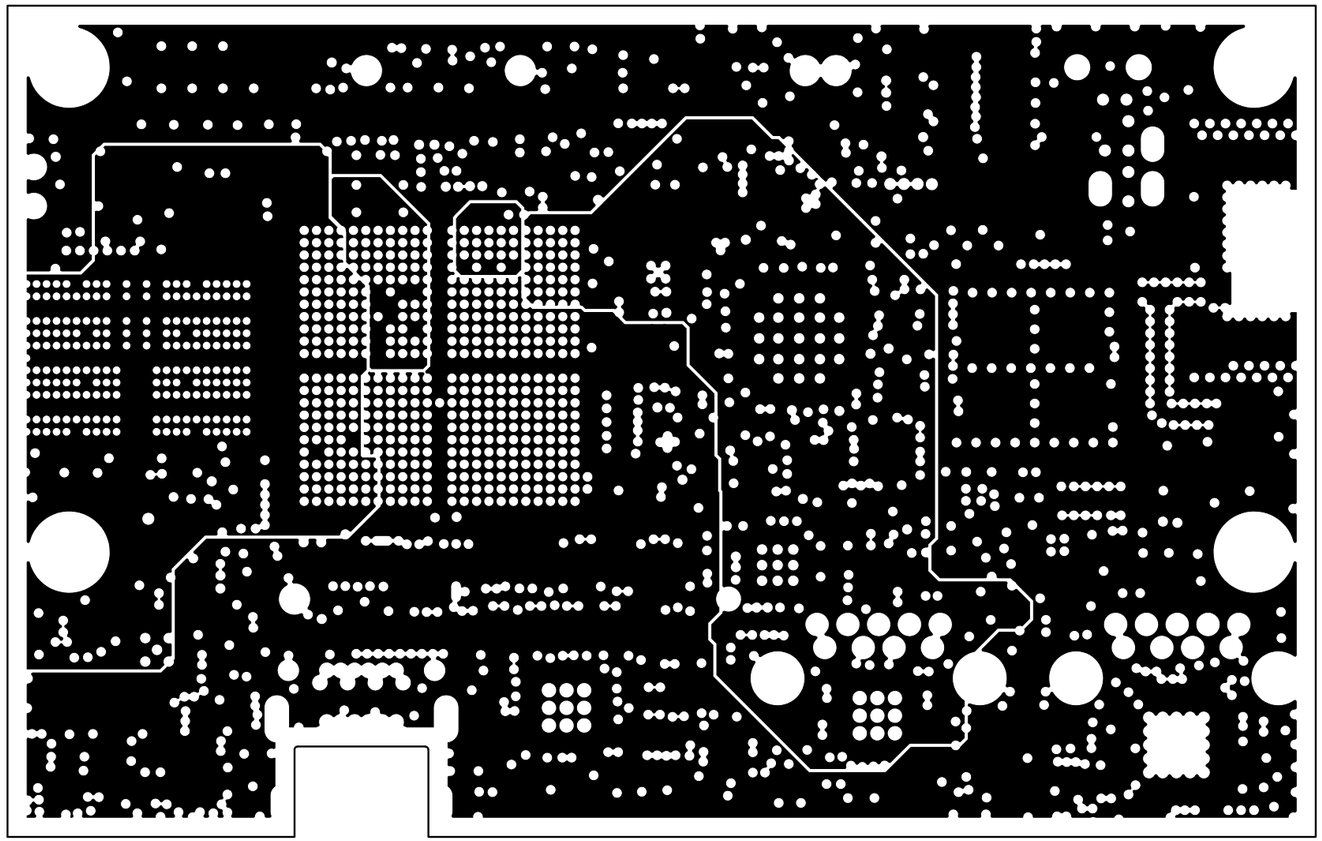
ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	

SHEET 5 OF 16

LAYER:

LAYER05 - ETCH LAYER 5 - (PLANE)

CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:48 2018 - (Untitled) : pwb-usdev-1_layer06.pho



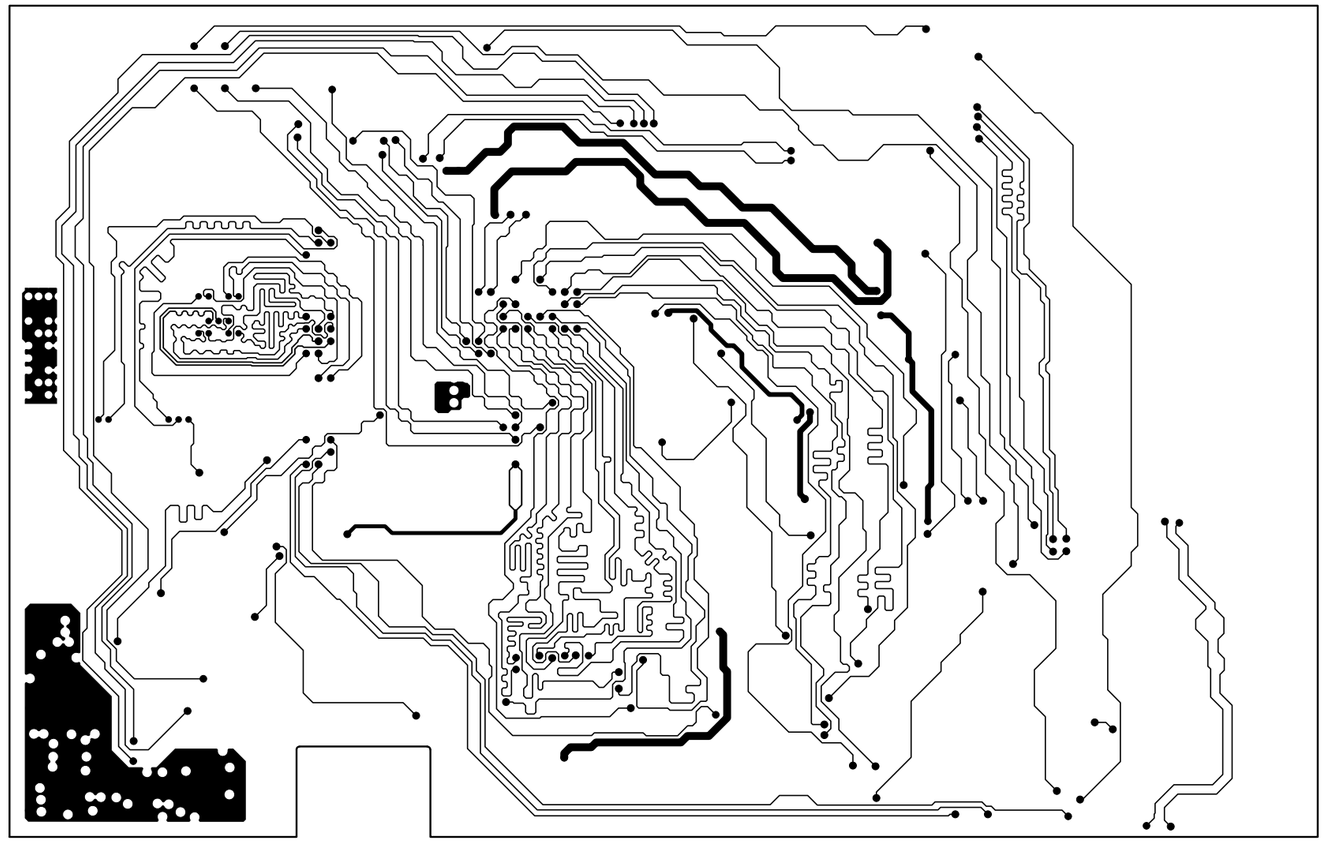
ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	

SHEET 6 OF 16

LAYER:

LAYER06 - ETCH LAYER 6 - (PLANE)

CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:48 2018 - (Untitled) : pwb-usdev-1_layer07.pho



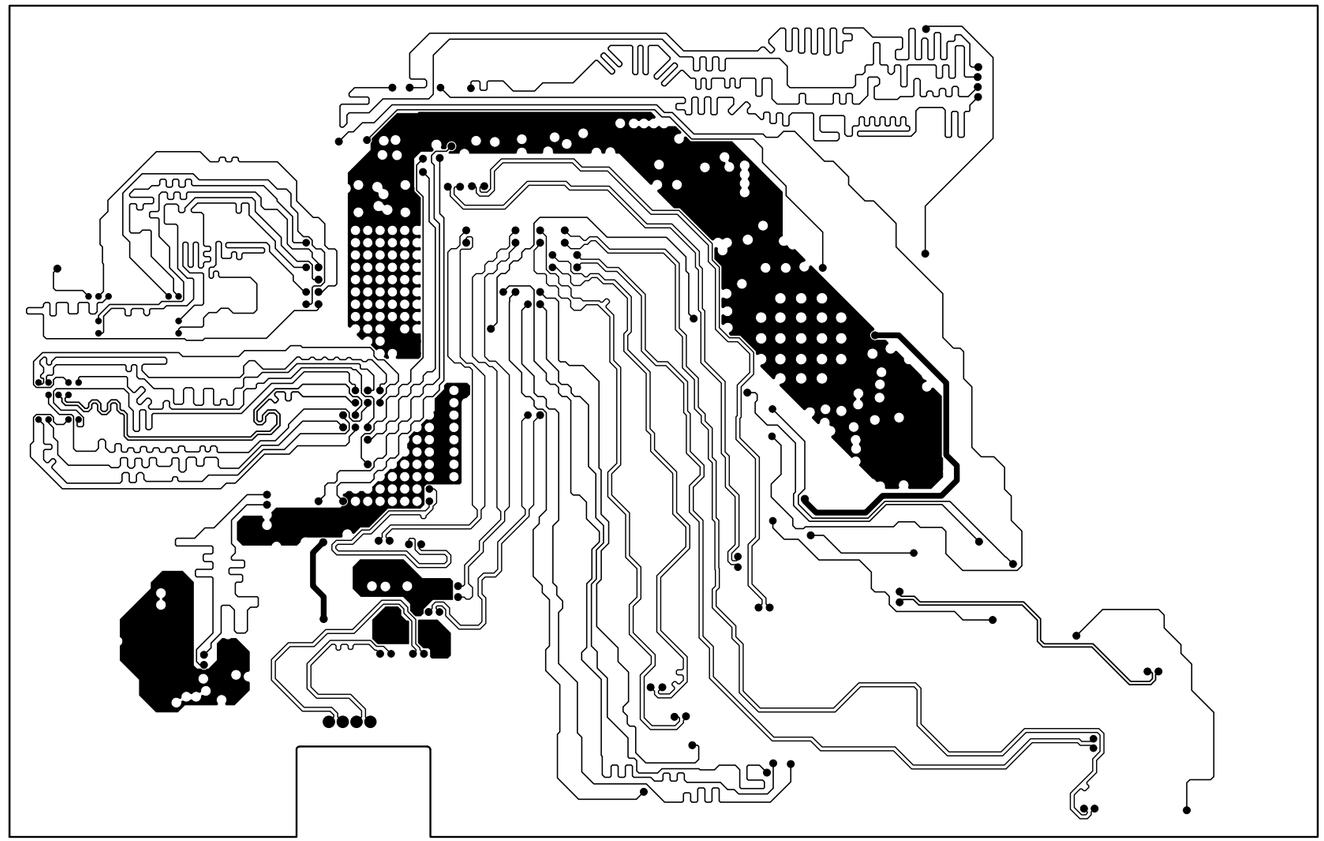
ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	

SHEET 7 OF 16

LAYER:

LAYER07 - ETCH LAYER 7 - (SIGNAL)

CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:48 2018 - (Untitled) : pwb-usdev-1_layer08.pho



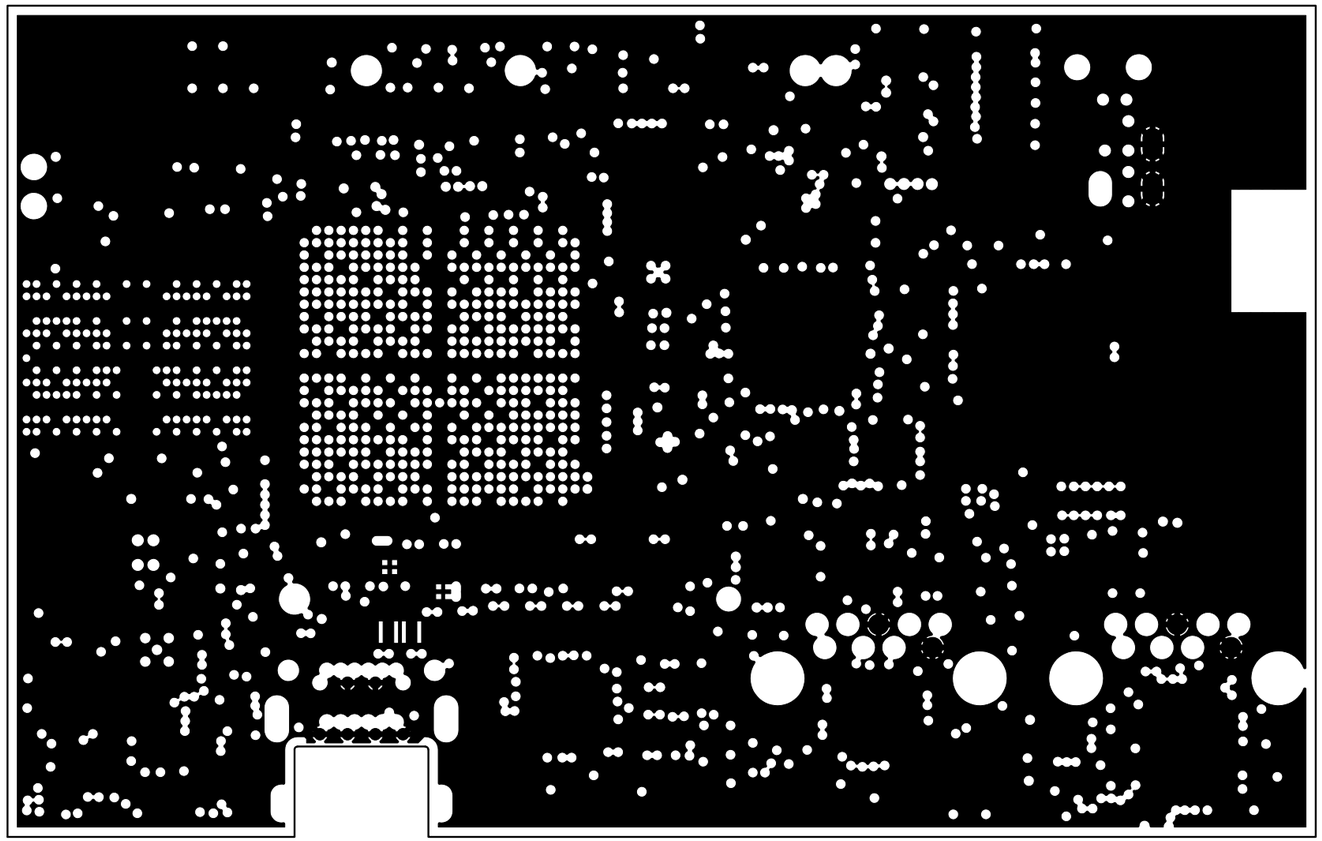
ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	

SHEET 8 OF 16

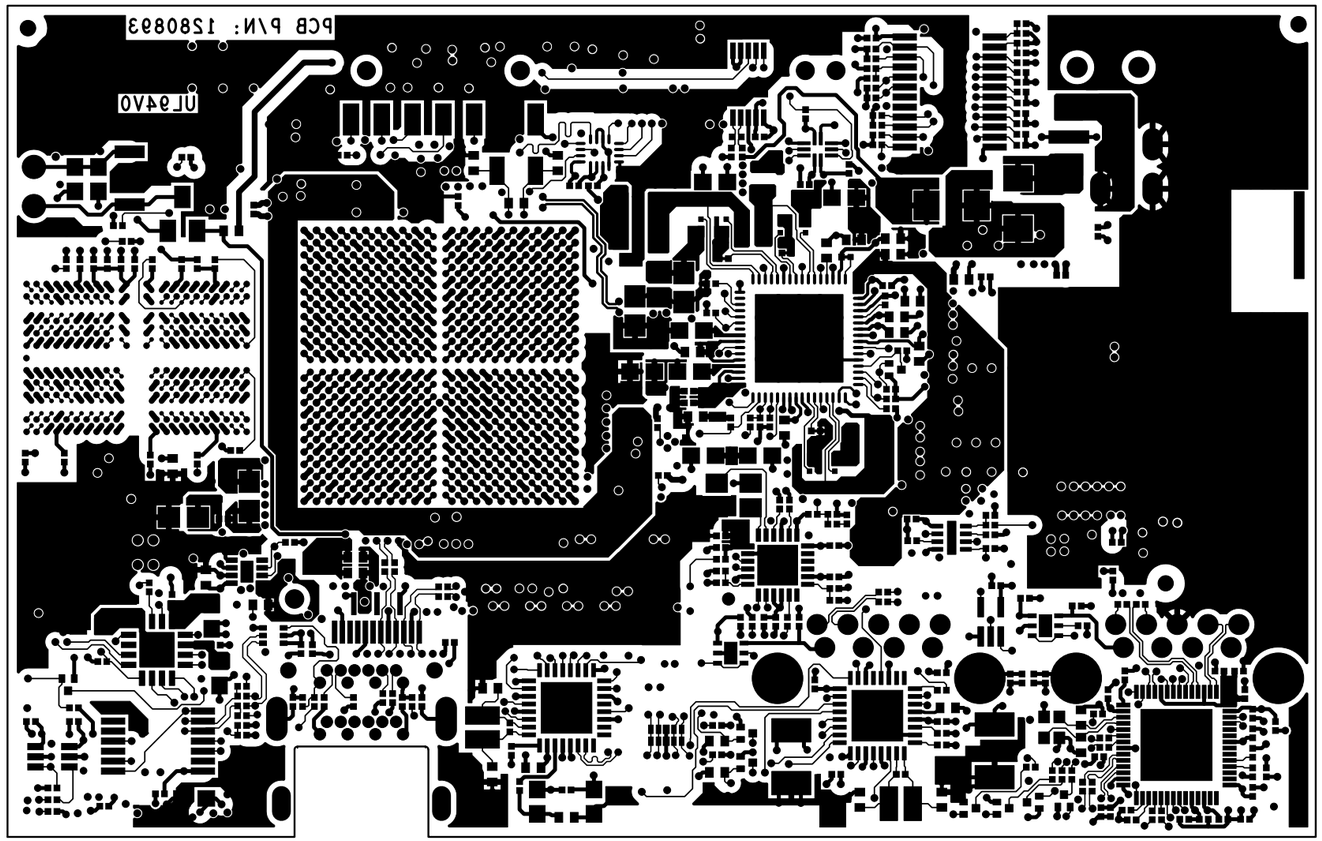
LAYER:

LAYER08 - ETCH LAYER 8 - (SIGNAL)

CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:48 2018 - (Untitled) : pwb-usdev-1_layer09.pho

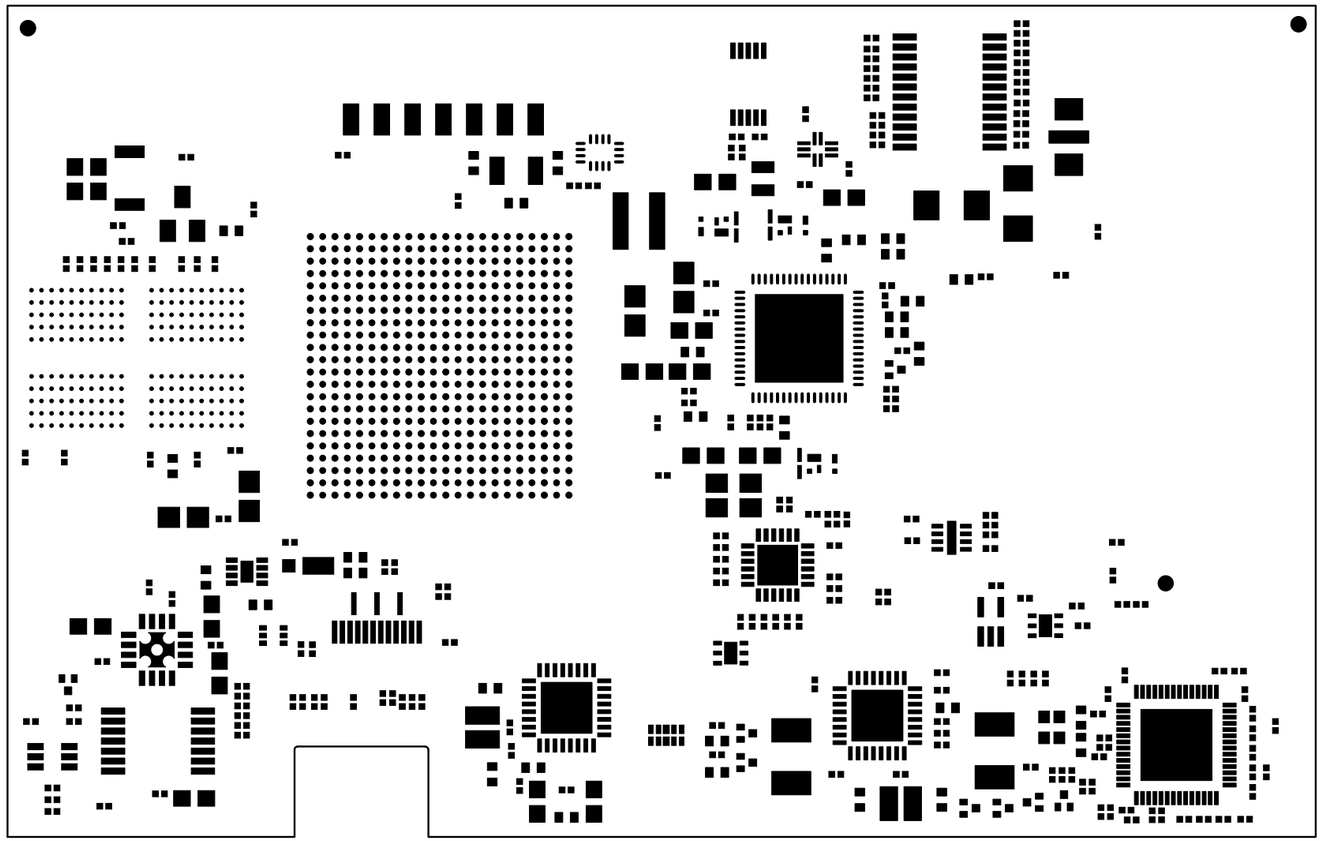


ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	
SHEET 9 OF 16 LAYER: LAYER09 - ETCH LAYER 9 - (PLANE)	



ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	
SHEET 10 OF 16 LAYER: LAYER10 - ETCH LAYER 10 - (SIGNAL)	

CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:48 2018 - (Untitled) : pwb-usdev-1_paste_bot.pho



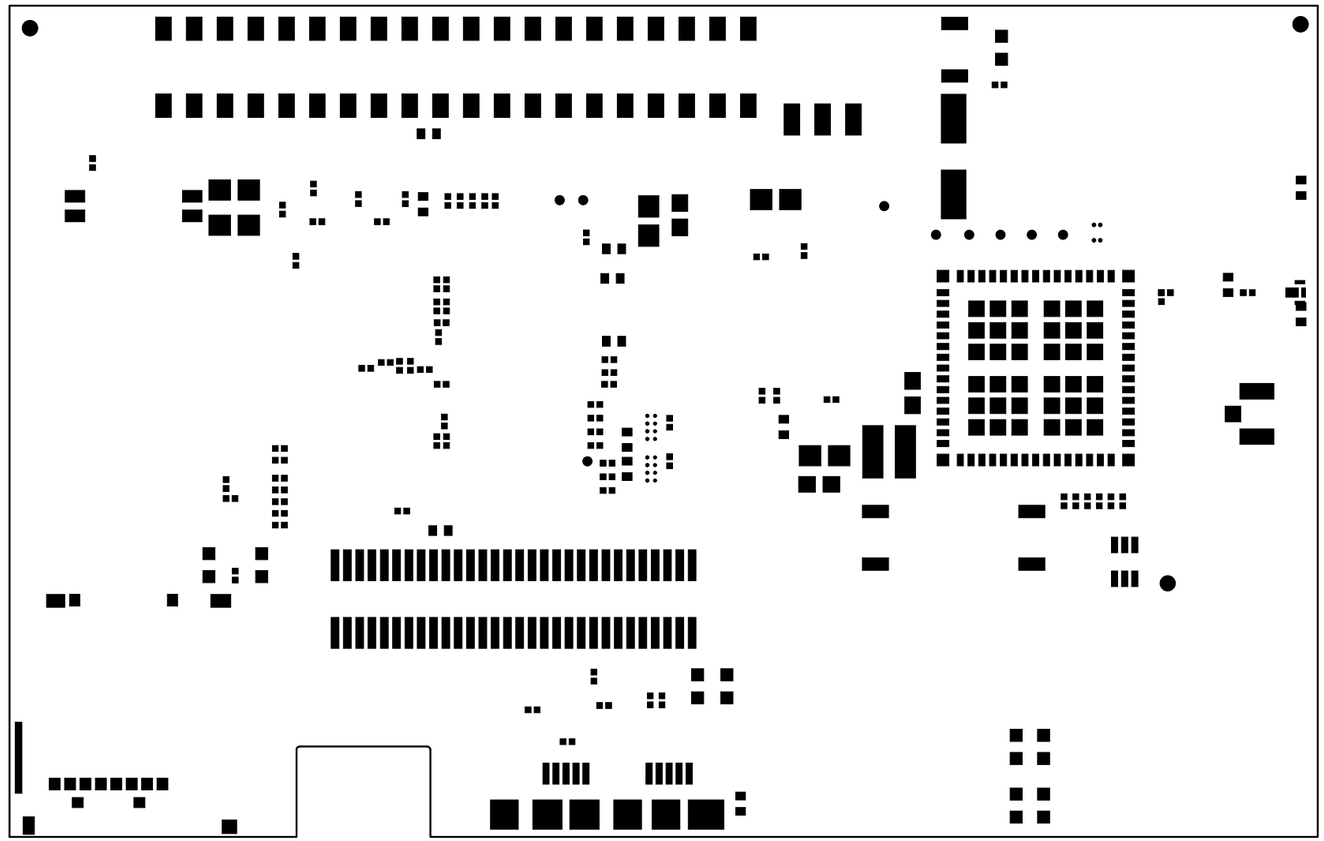
ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	

SHEET 16 OF 16

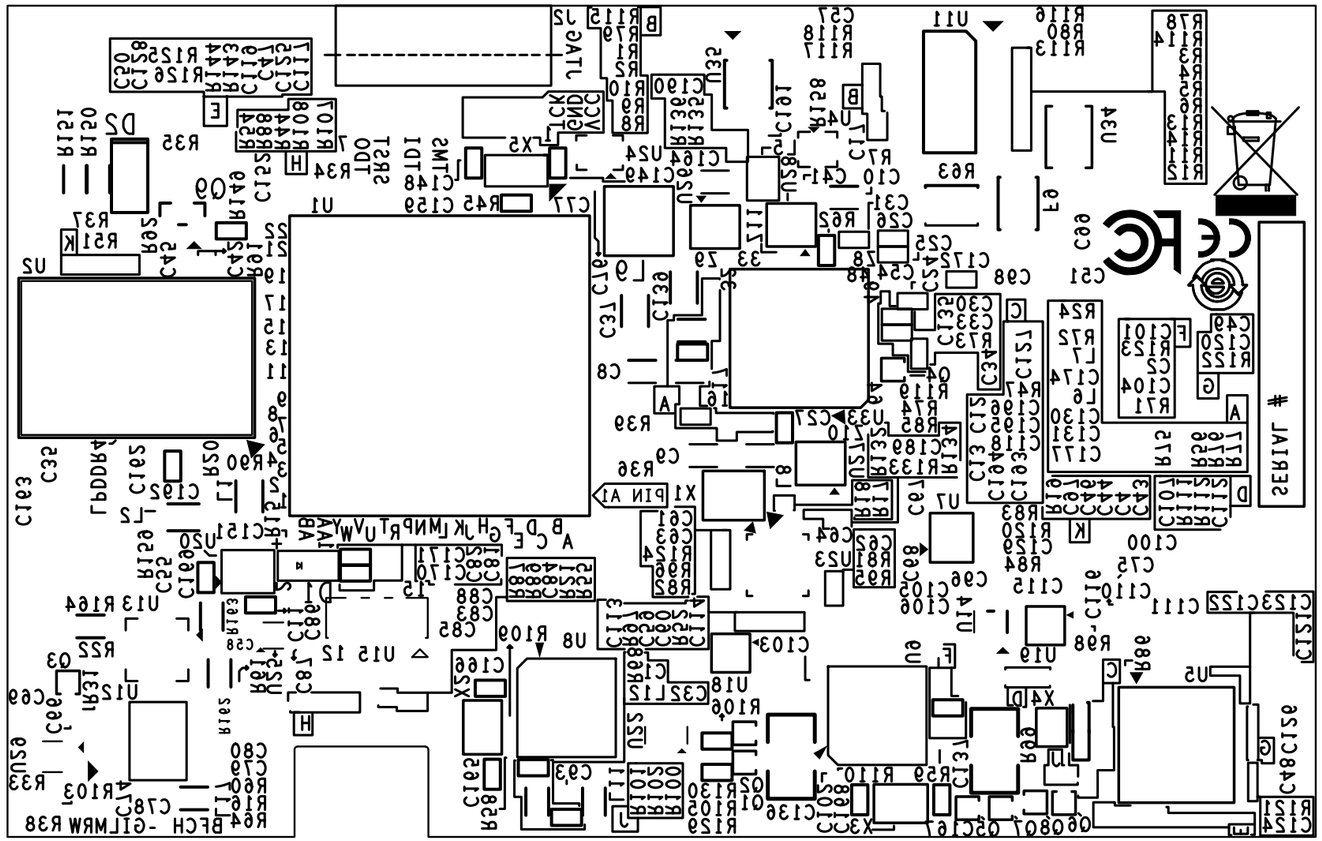
LAYER:

PASTEMASK BOTTOM

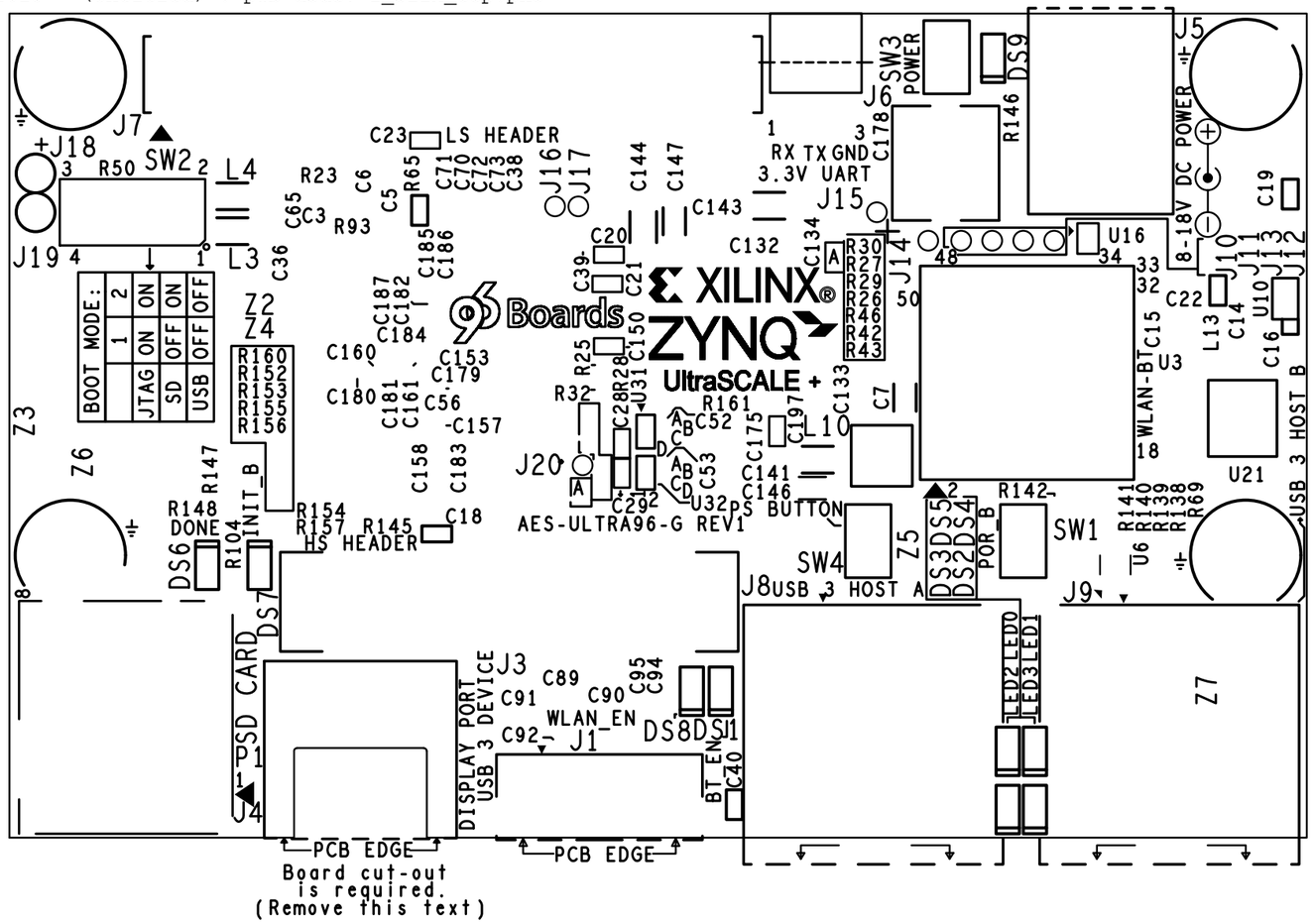
CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:48 2018 - (Untitled) : pwb-usdev-1_paste_top.pho



ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	
SHEET 15 OF 16 LAYER: PASTEMASK TOP	

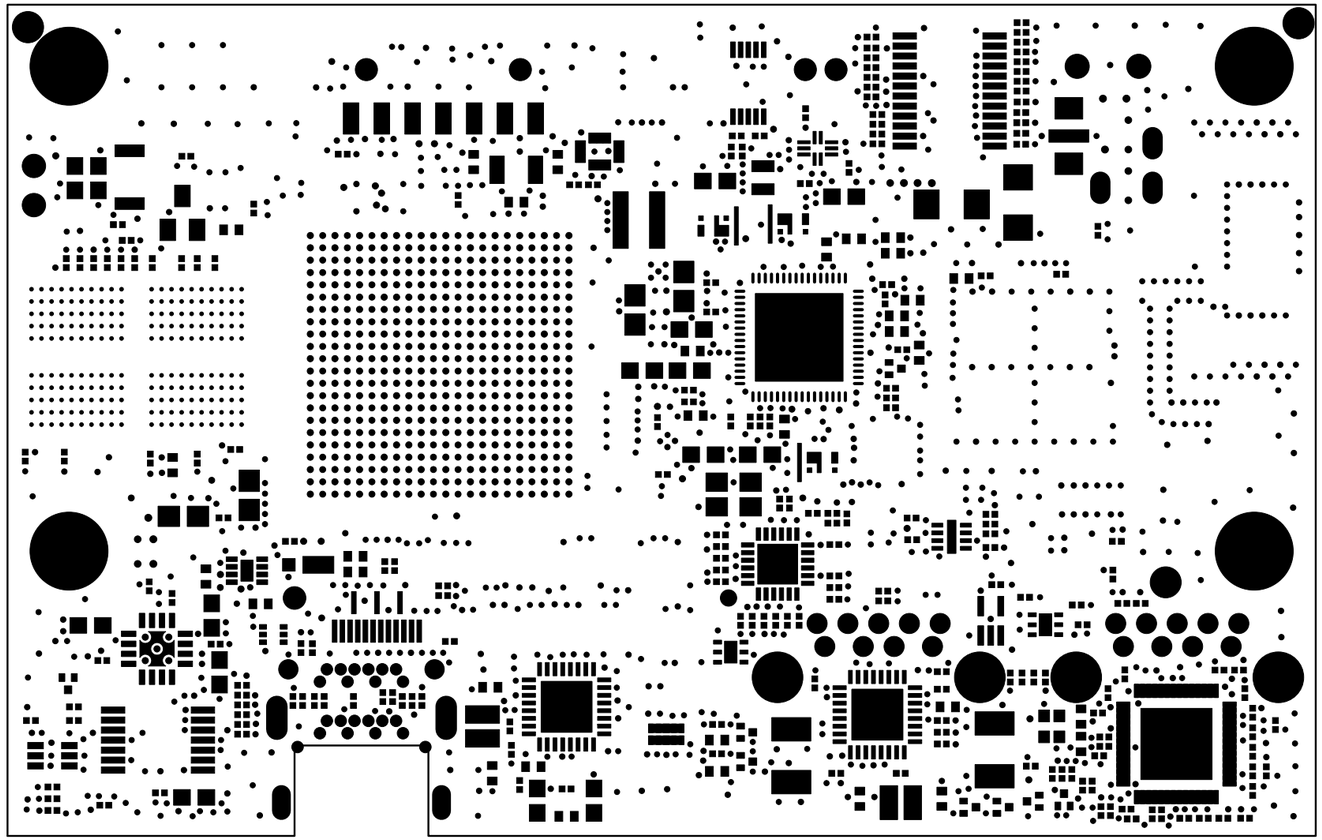


ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	
SHEET 14 OF 16 LAYER: SILKSCREEN BOTTOM	



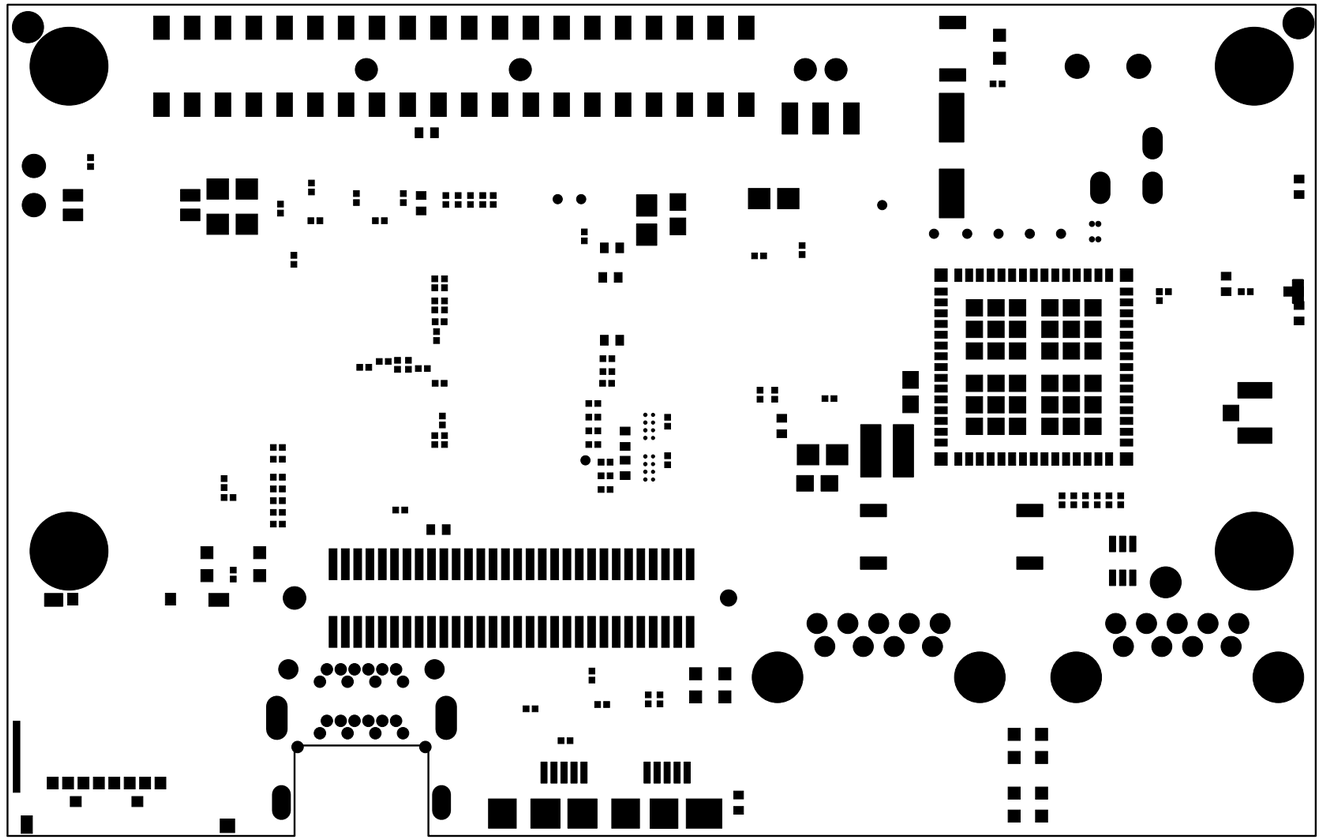
ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	
SHEET 13 OF 16 LAYER: SILKSCREEN TOP	

CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:49 2018 - (Untitled) : pwb-usdev-1_solder_bot.pho



ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	
SHEET 12 OF 16 LAYER: SOLDERMASK BOTTOM	

CAM350/DFMSTREAM V 11.0 : Thu Mar 15 15:34:49 2018 - (Untitled) : pwb-usdev-1_solder_top.pho



ARTWORK, ROHS COMPLIANT, AES-ULTRA96-G	
PCB # PWB-USDEV1 REV 1	
PCB Designer: A.D.S.	DATE: 03/15/2018
Schematic Eng: Brian F.	
SHEET 11 OF 16 LAYER: SOLDERMASK TOP	