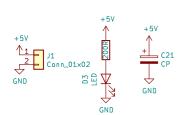
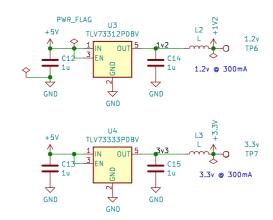
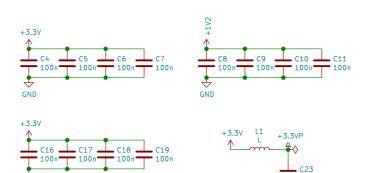
Power Supply

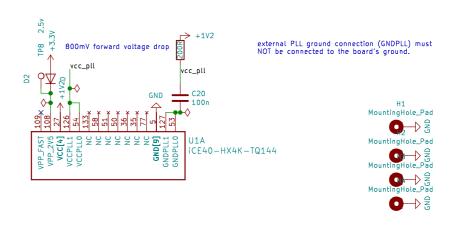




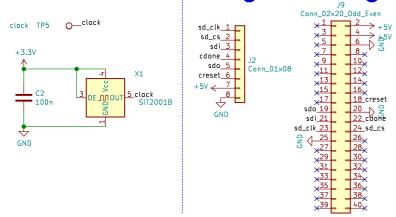
20 S 22 cdohe

24_sd_cs

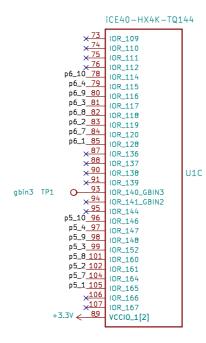


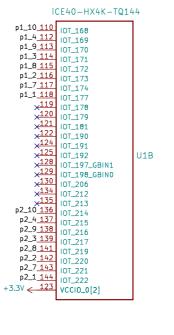


Clock

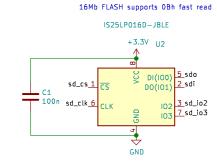


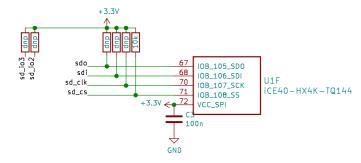
FPGA Programming





FLASH

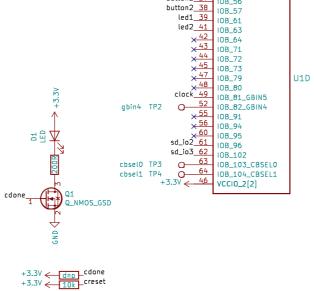




pullup on ss means configure as SPI master to read configuration from FLASH at boot



OB_56



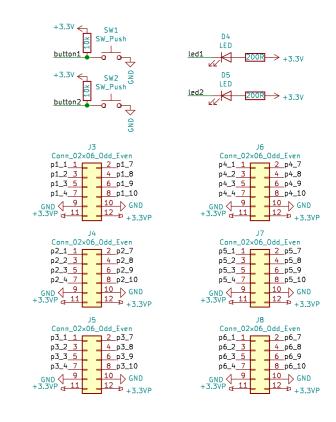
button1 37

D4_10_1 IOL_2A p4_4_2 p4_9_3 p4_3_4 IOL_3A 10L_3B p4_8_7 p4_2_8 p4_7_9 INI 4A IOL_4B IOL_5A IOL_5B p4_1 10 ×11 ×15 ×16 ×17 ×18 ×19 ×20 ×21 ×22 ×23 IOL_8A OL_8B IOL 10B OL_12A IOL_12B IOL_13A IOL_13B_GBIN7 IOL 14A GBIN6 IOL_14B IDI 17A p3_10_25 p3_4_26 p3_9_28 OL_17B IOL_18A IOL_18B IOL_23A p3_3<u>29</u> p3_8<u>31</u> IOL_23B IOL_24A p3_2_32 p3_7_33 IOL_24B IOL_25A p3_1<u>34</u>

IDI 25B +3.3V ← 6 VCCIO_3[2]

iCE40-HX4K-TQ144

Peripherals



things to check: clock and reset gbin, will pll be ok? flash — pullups needed? check fpga pinout against lattice docs

