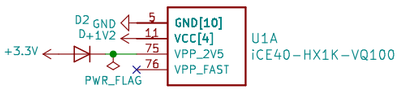
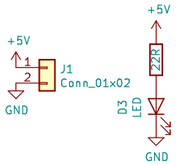
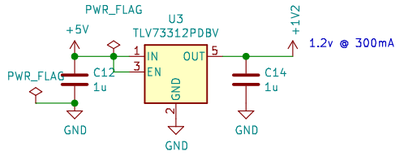
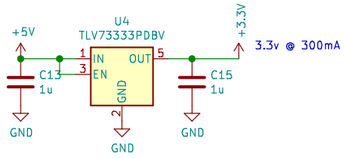
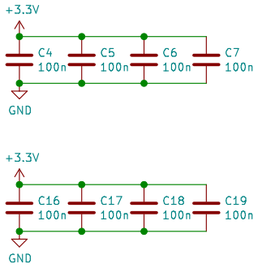
Power Supply

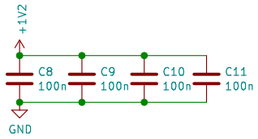








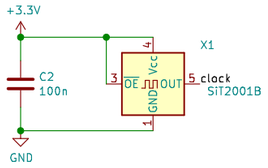




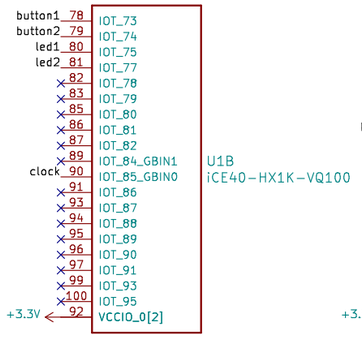
things to check:
clock and reset gbin, will pll be ok?
flash - pullups needed?
check fpga pinout against lattice docs
why no vcc and gnd pll on the v100?
sequencing psu?

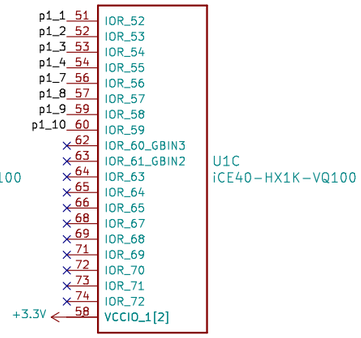
todo:

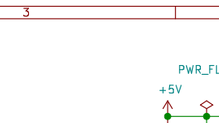
Clock



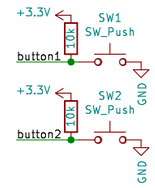
FPGA

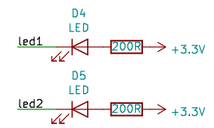


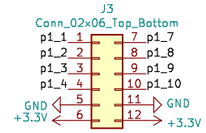


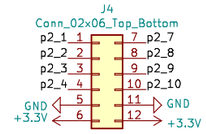


Peripherals

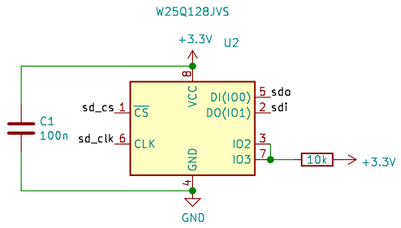


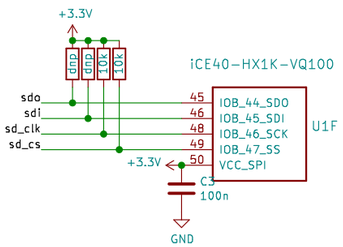






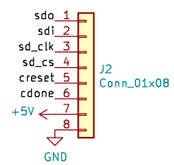
FLASH





icestick pull ups on sck and ss
icebreaker pullups on all
olimex pullups on ss. sdi & sdo joined with 22r

Programming



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