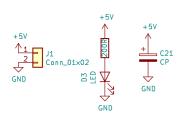
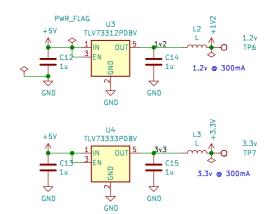
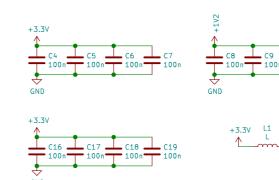
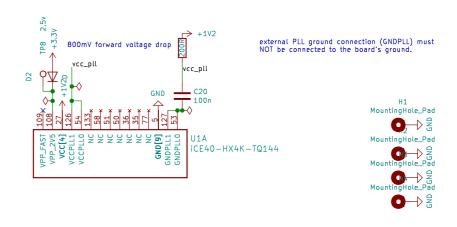
Power Supply



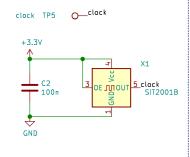






Clock

FLASH



16Mb FLASH supports 0Bh fast read

+3.3V U2

2 sdi

102 3_sd_io2 7_sd_io3

IOB_105_SD0

IOB_107_SCK

iCE40-HX4K-TQ144

68 | IOB_105_SD0 | TOB_106_SD1 | IOB_107_SCK | IOB_108_SS

VCC SPI

pullup on ss means configure as SPI master to read configuration from FLASH at boot

100n

GND

IS25LP016D-JBLE

GND

sd_cs_1 CS

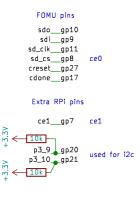
100n sd_clk_6

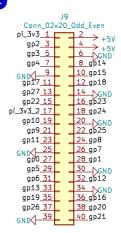
+3,3V

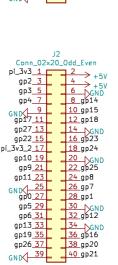
sd clk

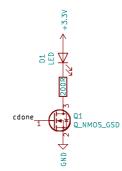
10k sd_cs

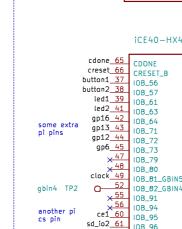




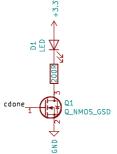




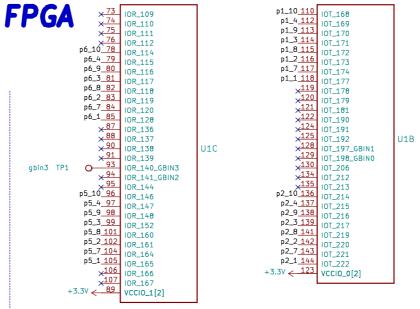




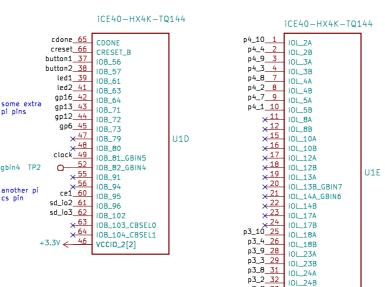
 $+3.3V \leftarrow 10k$ -creset



iCE40-HX4K-TQ144 iCE40-HX4K-TQ144 **Peripherals** IOR_109 p1_10 110 OT_168 p1_4_112



+3.3VP



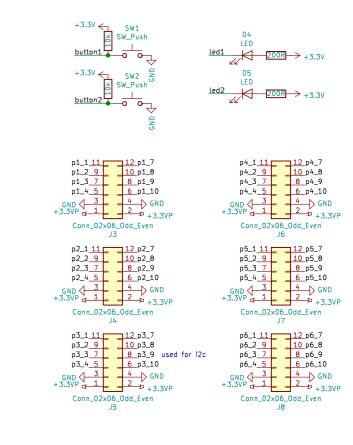
OL_25A

0L_25B

VCCI0_3[2]

p3_1_34

+3.3V ← 6



things to check: clock and reset gbin, will pll be ok? flash — pullups needed? check fpga pinout against lattice docs