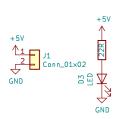
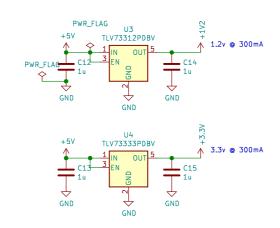
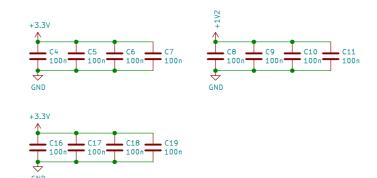
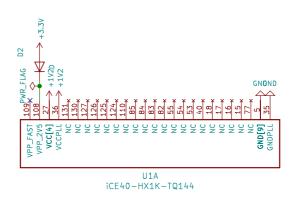
Power Supply

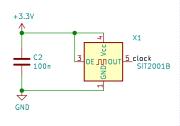




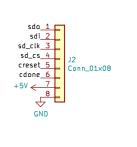




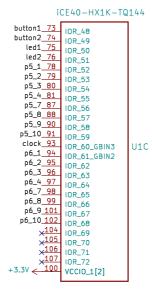
Clock



Programming



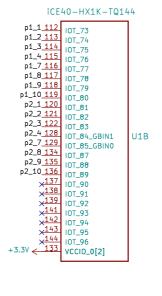
FPGA

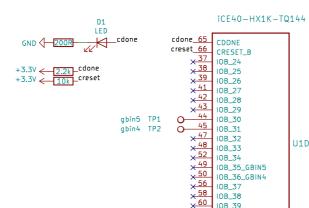


U1D

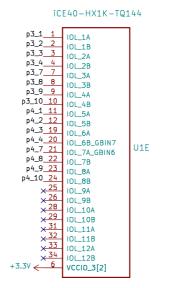
IOB_42_CBSELO

IOB_43_CBSEL1 VCCI0_2[2]

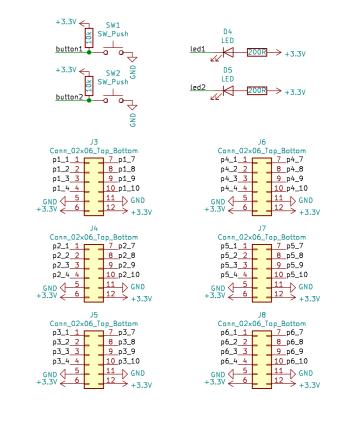




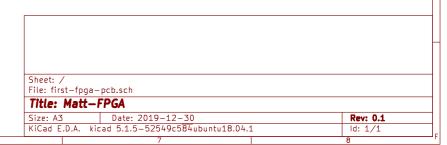
cbsel0 TP3 O 63 cbsel1 TP4 O 64 +3.3V 46



Peripherals

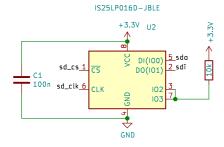


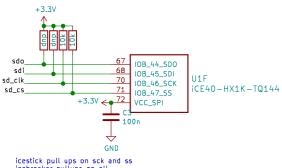
things to check: clock and reset gbin, will pll be ok? flash — pullups needed? check fpga pinout against lattice docs



FLASH

16Mb FLASH supports 0Bh fast read





icestick pull ups on sck and ss icebreaker pullups on all olimex pullups on ss. sdi & sdo joined with 22r