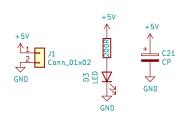
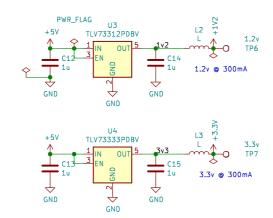
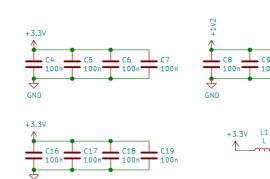
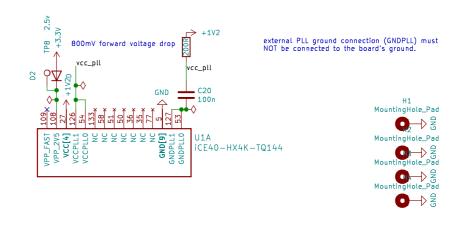
Power Supply



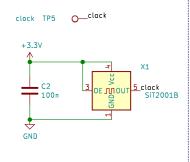






Clock

FLASH



16Mb FLASH supports 0Bh fast read IS25LP016D-JBLE

+3.3V U2

GND

2 sdi

102 3 sd_io2 7 sd_io3

IOB_105_SD0

IOB_107_SCK

68 | IOB_105_SD0 70 | IOB_106_SDI 71 | IOB_107_SCK 10B_108_SS

VCC SPI

pullup on ss means configure as SPI master to read configuration from FLASH at boot

sd_cs_1_CS

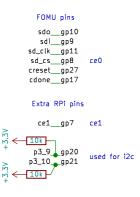
100n sd_clk_6

+3,3V

sd clk

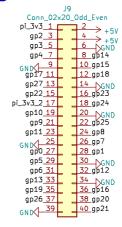
10k sd_cs

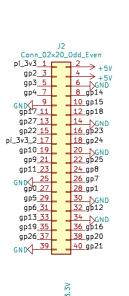


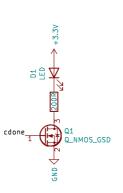


pullups required for safe operation of flash

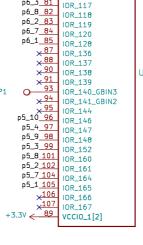
iCE40-HX4K-TQ144







FPGA ×73 ×74 ×75 ×76 p6_10_78 IOR_109 INR 111 OR_112 IOR_114 IOR_115 p6_4 79 p6_9<u>80</u> OR_116 p6_3 81 IOR_117 p6_8<u>82</u> p6_2<u>83</u> OR 119 p6_7 84 OR_120 p6_1<u>85</u> IOR_128 IOR_136 ×87 ×88 ×90 ×91 O 93 IOR_137 U1C IDR 138 qbin3 TP1 IDR 140 GBIN3 ×94 ×95 p5_10_96 IOR_141_GBIN2 IDR 144 OR_146



iCE40-HX4K-TQ144

iCE40-HX4K-TQ144

OT_168

OT 170

OT_171

OT_173

OT_177

OT 179

OT_181

NT 190

OT_191

OT 206

OT_212

OT_213

OT_214

OT_215 OT_216

DT 219

DT 221

0L_25B

VCCI0_3[2]

+3.3V ← 6

OT 197 GBIN1

U1B

U1E

p1_10 110

p1_9<u>113</u>

p1_3_114

p1_2 116

p1_1_118

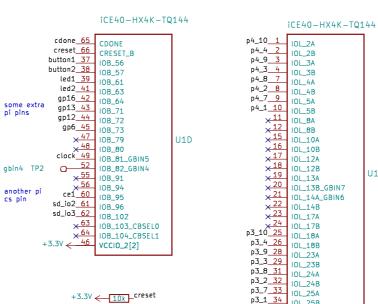
p2_4_137 p2_9_138

p2_8 141

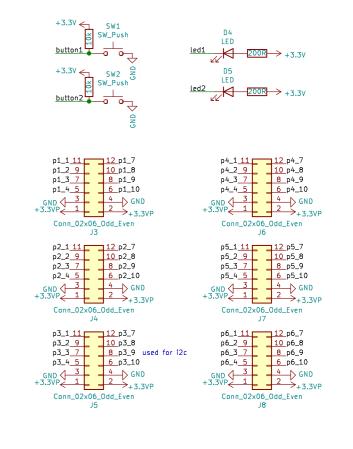
p2_2<u>142</u>

p2_1_144

+3.3V < 123 VCCIO_0[2]



Peripherals



things to check: clock and reset gbin, will pll be ok? flash — pullups needed? check fpga pinout against lattice docs

