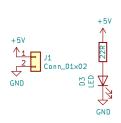
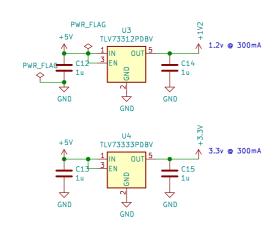
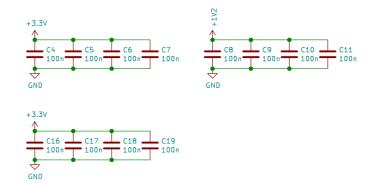
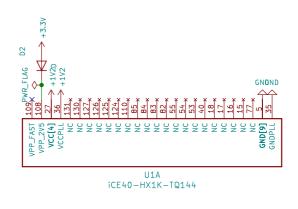
Power Supply

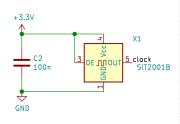




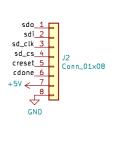




Clock

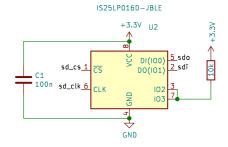


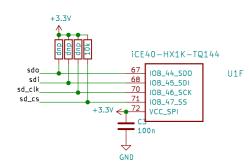
Programming



FLASH

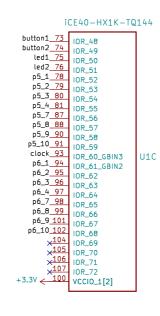


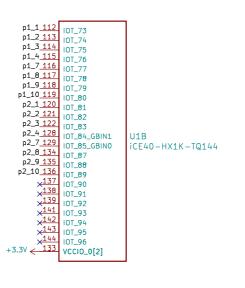




pullup on ss means configure as SPI master to read configuration from FLASH at boot

FPGA



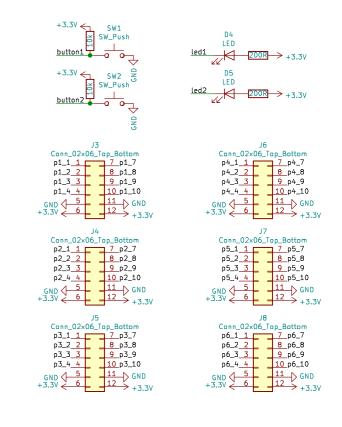


iCE40-HX1K-TQ144

cdone p3_2<u>2</u> p3_3<u>3</u> IOL 1B GND - 200R creset 66 × 37 × 38 × 39 × 41 CRESET_B p3_4<u>4</u> p3_7<u>7</u> IOL_2B IOL_3A +3.3V 2.2k cdone +3.3V 10k creset 0B_25 p3_8_8 IOL_3B p3_9_9 OL_4A OR 27 0B_28 p4_1<u>11</u> p4_2<u>12</u> IDI 5A 0B_29 gbin5 TP1 gbin4 TP2 0-IOB_30 p4_3<u>19</u> DI 6A p4_4_20 IOL_6B_GBIN7 OB 32 U1D iCE40-HX1K-TQ144 P4-8 22 P4-9 23 IOL_7A_GBIN6 IOB_34 p4_9_23 p4_10_24 lol_8B x_25 x_26 lol_9B lol_10A x_29 lol_10B lol_10B lol_11A x_31 lol_11A lol_11B x_33 lol_12A lol_12B yccio_3[2] IOB_35_GBIN5 IOB_36_GBIN4 IOB_37 DB 39 cbsel0 TP3 O 63 cbsel1 TP4 O 64 +3.3V 46 IOB_42_CBSELO IOB_43_CBSEL1

VCCI0_2[2]

Peripherals



things to check: clock and reset gbin, will pll be ok? flash — pullups needed? check fpga pinout against lattice docs

