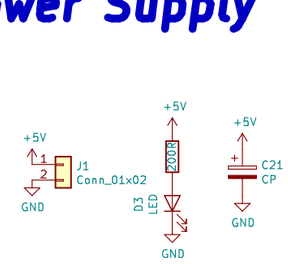
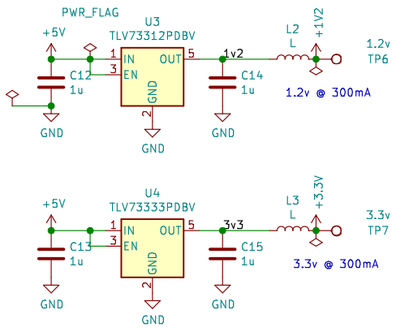
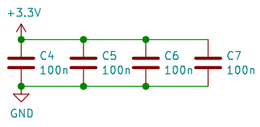
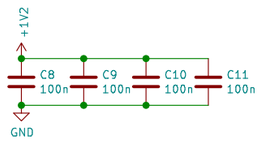
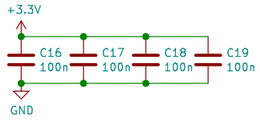
Power Supply

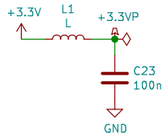


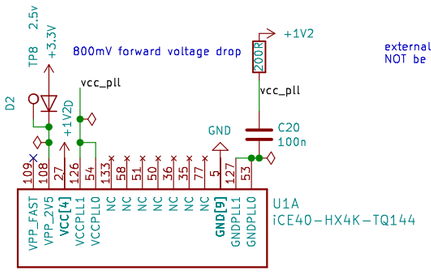




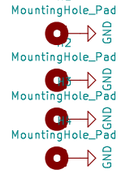




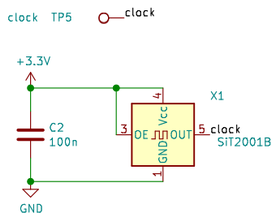




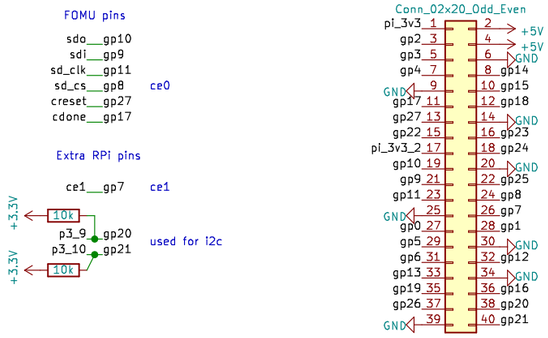
external PLL ground connection (GNDPLL) must NOT be connected to the board's ground.

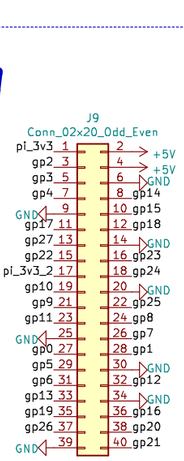


Clock



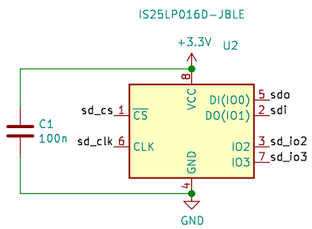
Programming

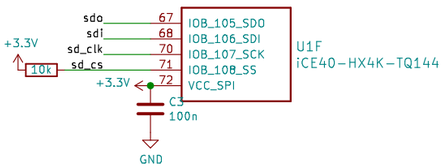




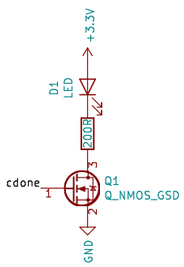
FLASH

16Mb FLASH supports 0Bh fast read

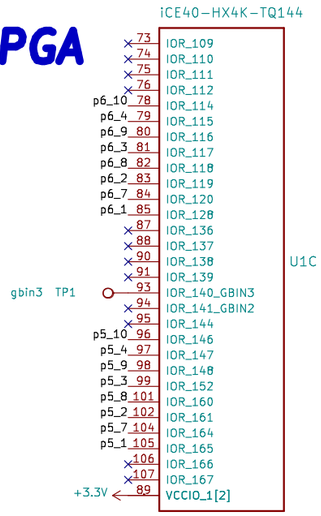


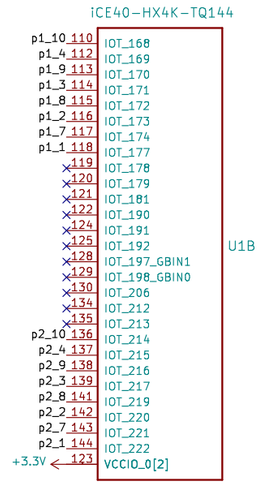


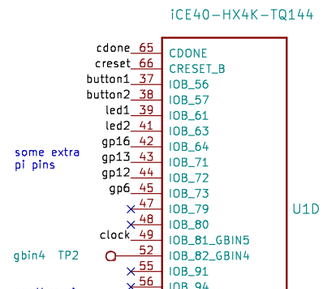
pullup on ss means configure as SPI master to read configuration from FLASH at boot

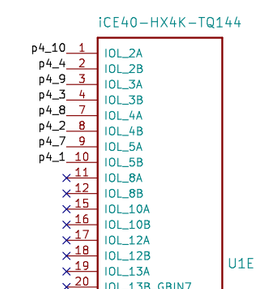


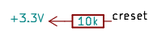
FPGA



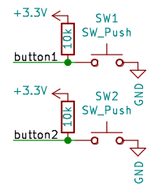


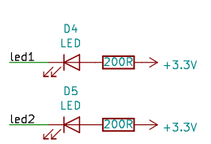


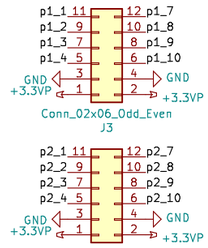




Peripherals







things to check:
clock and reset gbin, will pll be ok?
flash – pullups needed?
check fpga pinout against lattice docs