

LED-PWR R12 680,1% Power

LED1 LED-RED, RA

LED-PTT R13 680,1% PTT

LED2 LED-RED, RA

LED-RT R15 680,1% Sync

LED3 LED-RED, RA

LED-ERR R16 680,1% Clip/Error

LED4 LED-YEL, RA

GND

Diagram illustrating the connection of the SWCLK and SWDIO signals to the CN1 HDR100-3 connector. The SWCLK signal is connected to pin 1, and the SWDIO signal is connected to pin 2. A common ground connection is shown for pin 3. Resistors R19 and R20 (22.1%) are connected in series with the signals.

	U1A	STM32F405
	23 PA0	97 PE0
AIN1	24 PA1	98 PE1
AIN2	25 PA2	1 PE2
	26 PA3	2 PE3
DAC1_OUT	29 PA4	3 PE4
DAC2_OUT	30 PA5	4 PE5
	31 PA6	5 PE6
	32 PA7	38 PE7
	67 PA8	39 PE8
VBUS	68 PA9	40 PE9
OTG_ID	69 PA10	41 PE10
OTG_DM	70 PA11	42 PE11
OTG_DP	71 PA12	43 PE12
SWDIO	72 PA13	44 PE13
SWCLK	76 PA14	45 PE14
	77 PA15	46 PE15
	35 PB0	81 PD0 SELECT
	36 PB1	82 PD1 BACK
BOOT1	37 PB2	83 PD2
	89 PB3	84 PD3
	90 PB4	85 PD4
SCL	91 PB5	86 PD5 OTG_OVR_CUR
	92 PB6	87 PD6
	93 PB7	88 PD7 BOOT0
	95 PB8	55 PD8 EXT-PTT
SDA	96 PB9	56 PD9 TEST
USART3_TX	47 PB10	57 PD10 CPPT
USART3_RX	48 PB11	58 PD11
	51 PB12	59 PD12 LED-PWR
	52 PB13	60 PD13 LED-PTT
	53 PB14	61 PD14 LED-RT
	54 PB15	62 PD15 LED-ERR
OTG_PWR_ON	15 PC0	
	16 PC1	
	17 PC2	PH0 12 OSC_IN
	18 PC3	PH1 13 OSC_OUT
	33 PC4	
	34 PC5	
	63 PC6	PC14 8
	64 PC7	PC15 9
	65 PC8	
	66 PC9	
	78 PC10	NRST 14 NRST
	79 PC11	
	80 PC12	
	7 PC13	BOOT0 94 BOOT0

**NOTE: SW1 HELD ON POWER UP
FORCES BOOT TO SYSTEM
MEMORY (STLINK)**

Sheet: 1/2

