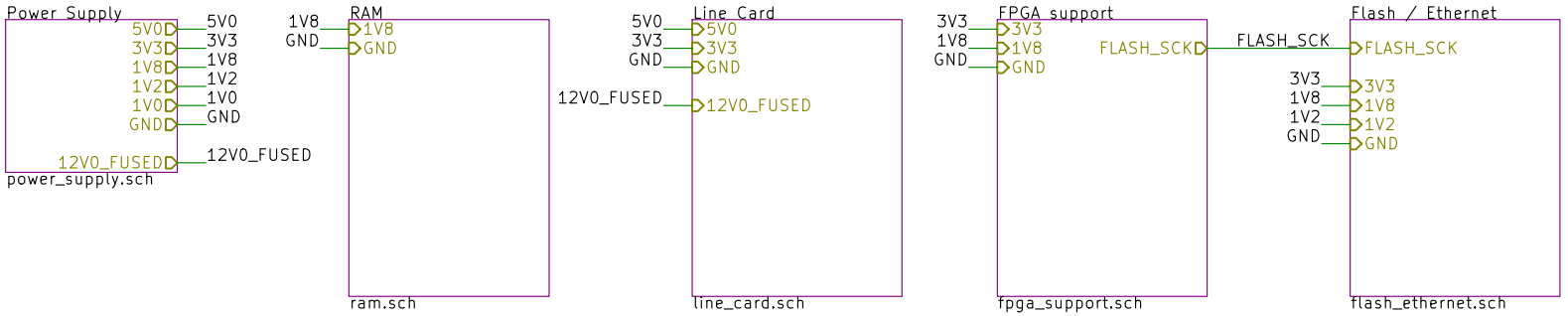


Top level

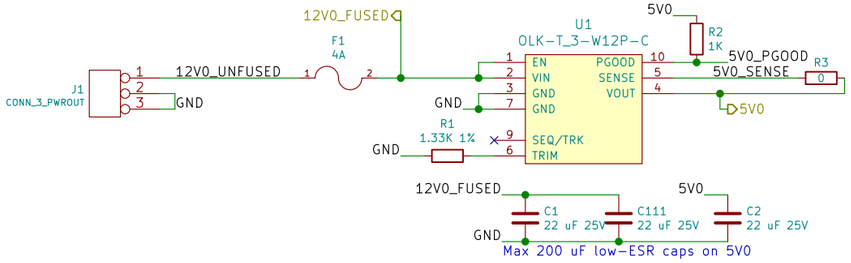
Andrew D. Zonenberg

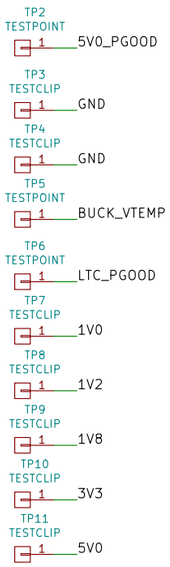
Sheet: /

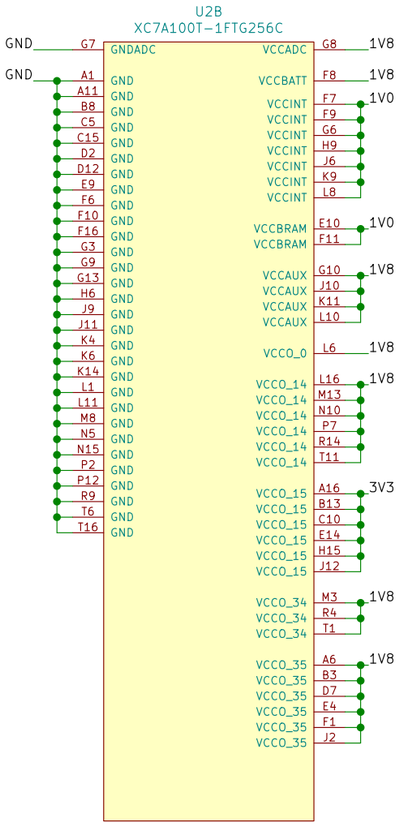
File: host-x1.sch

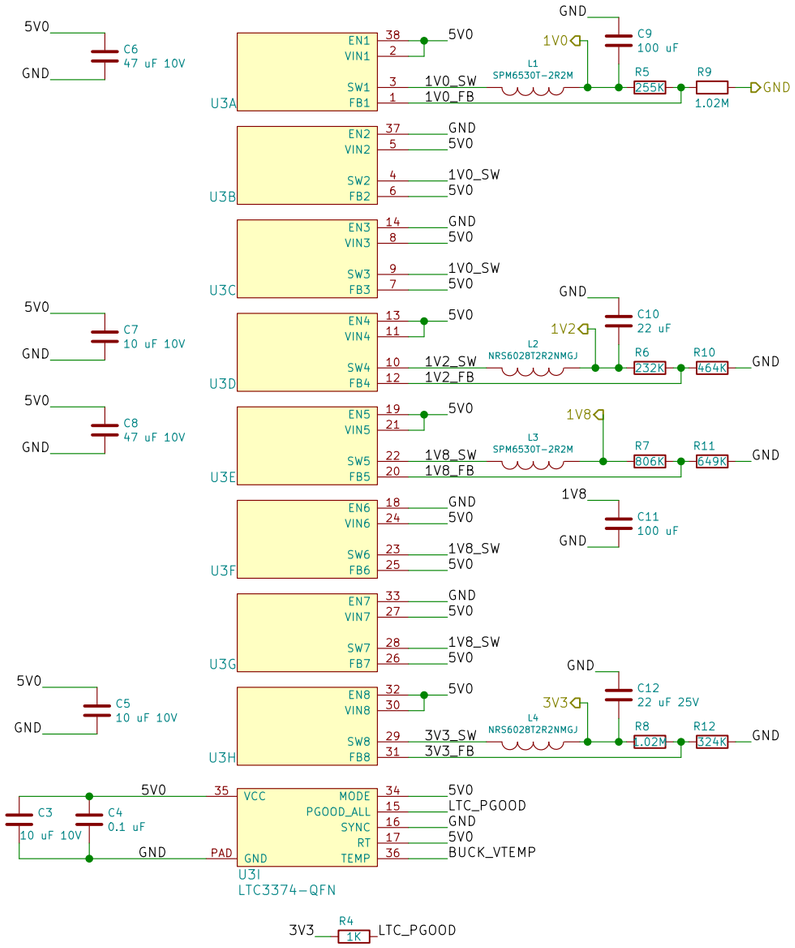
Title: STARSHIPRAIDER Single-Lane Host

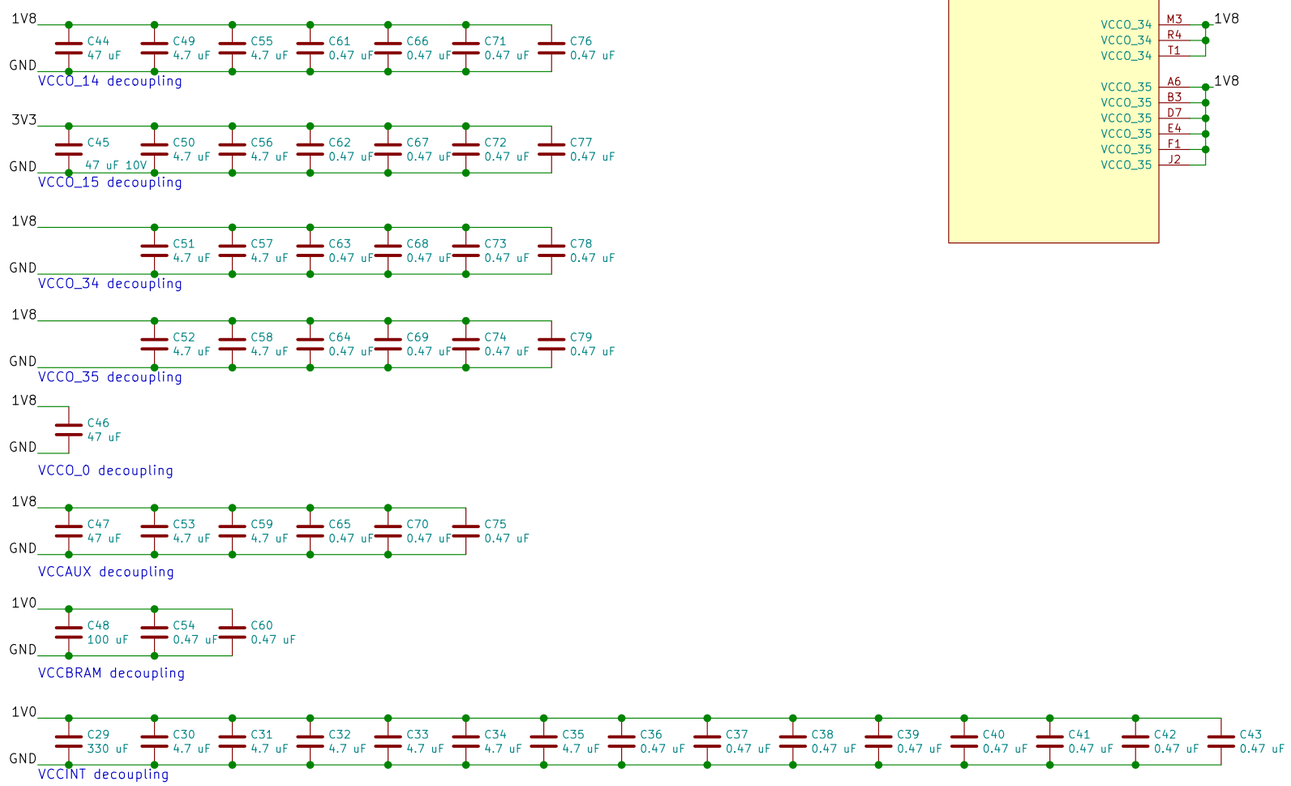
Size: A4	Date: 2017-05-14	**Rev: 0.1**
KiCad E.D.A. kicad (6.0.0-rc1-dev-1427-g10887868d)		Id: 1/6









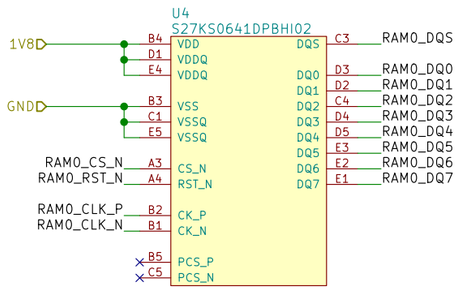


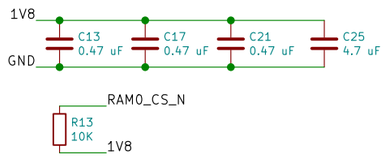
TODO: Check if we already have LTC3374 feedback resistors in inventory and remove from DigiKey cart if so

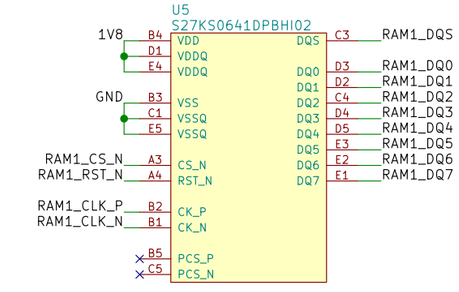
Power Supply
Andrew D. Zonenberg
Sheet: /Power Supply/
File: power_supply.sch

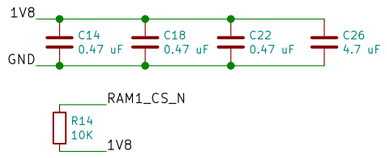
Title: STARSHIPRAIDER Single-Lane Host

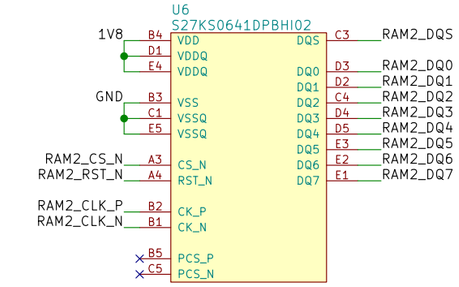
Size: A3	Date: 2017-05-14	**Rev: 0.1**
KiCad E.D.A. kicad (6.0.0-rc1-dev-1427-g10887868d)		Id: 2/6

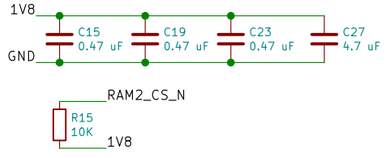


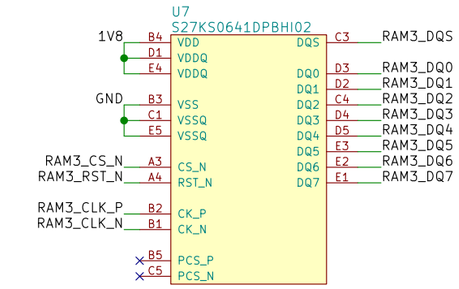


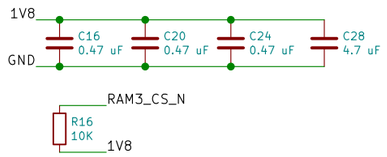






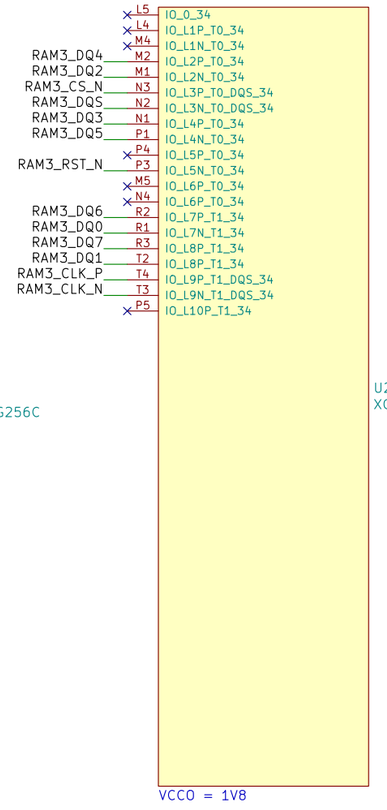


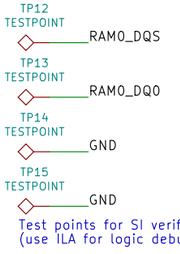




No termination on DQ lines.
FPGA and RAM both have programmable drive strength

TODO: Termination resistors for differential clock?



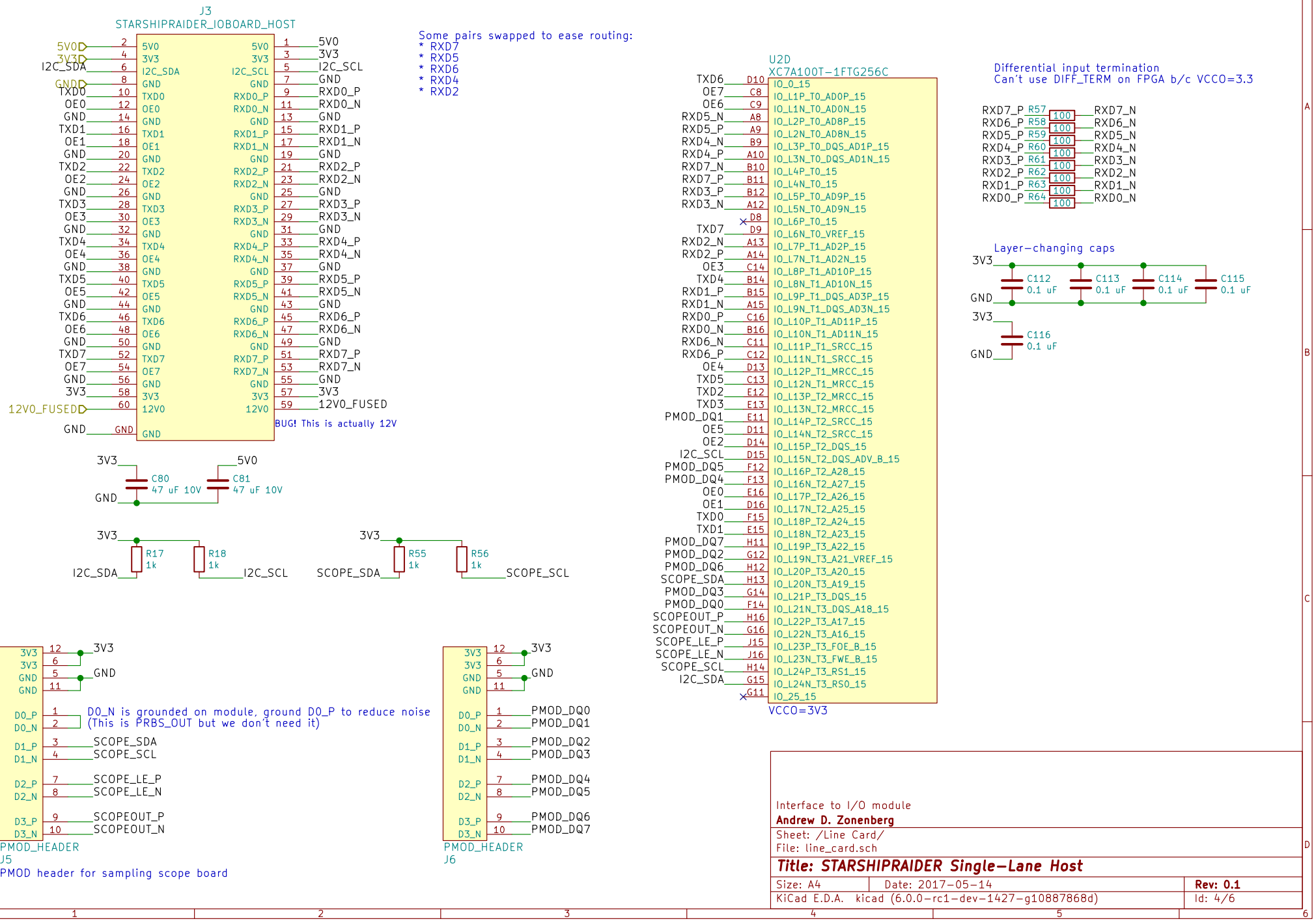


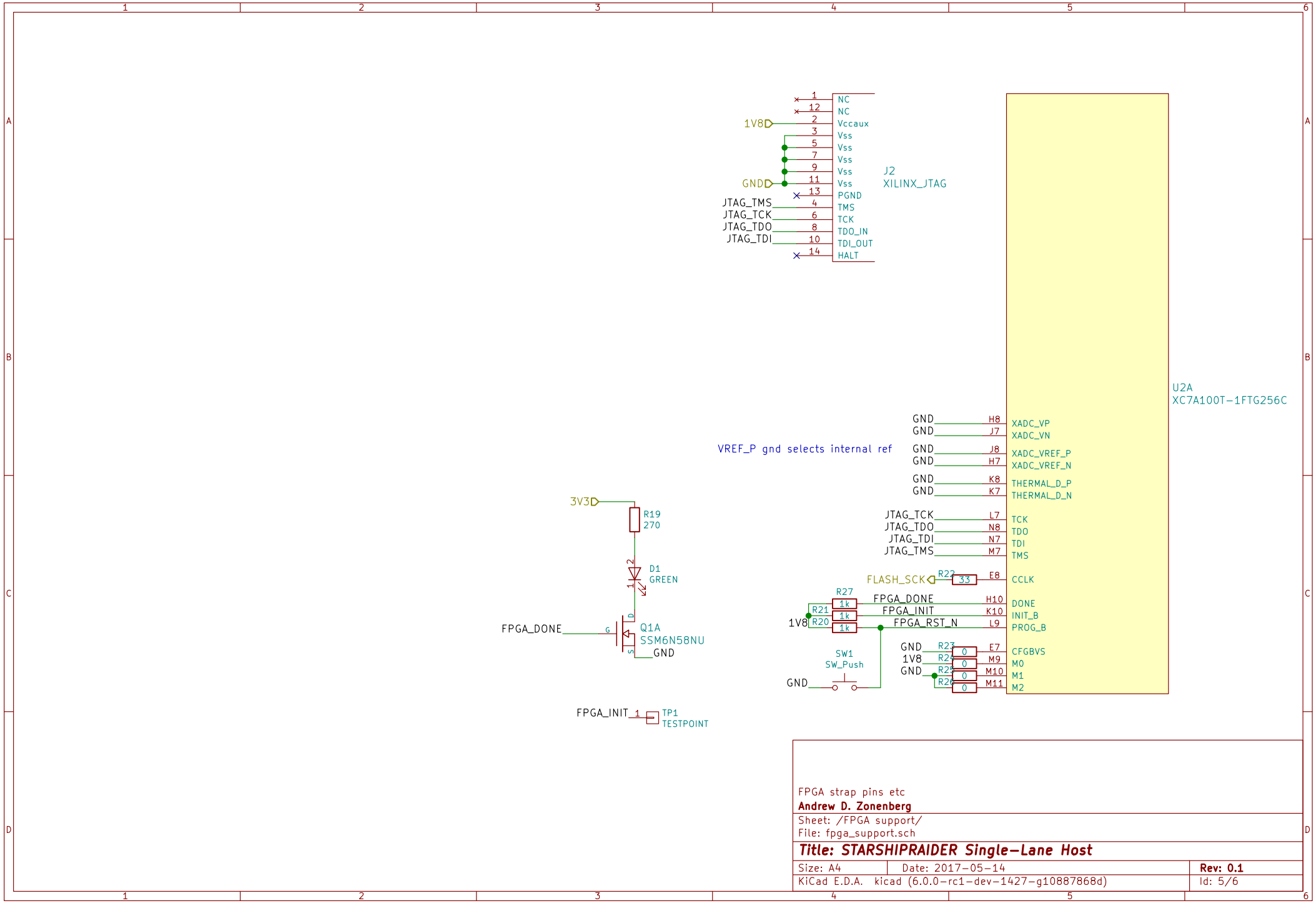
Test points for SI verification
(use ILA for logic debug)

32-bit HyperRAM
Andrew D. Zonenberg
Sheet: /RAM/
File: ram.sch

Title: STARSHIPRAIDER Single-Lane Host

Size: A3	Date: 2017-05-14	**Rev: 0.1**
KiCad E.D.A. kicad (6.0.0-rc1-dev-1427-g10887868d)		Id: 3/6


J3
STARSHIPRAIDER_IOBOARD_HOST
5V0
3V3
I2C_SDA
GND
TXD0
OE0
TXD1
OE1
TXD2
OE2
TXD3
OE3
TXD4
OE4
TXD5
OE5
TXD6
OE6
TXD7
OE7
12V0_FUSED
Some pairs swapped to ease routing:
* RXD7
* RXD5
* RXD6
* RXD4
* RXD2
BUG! This is actually 12V
C80 47 uF 10V
C81 47 uF 10V
R17 1k
R18 1k
R55 1k
R56 1k
SCOPE_SDA
SCOPE_SCL
U2D
XC7A100T-1FTG256C
VCCO=3V3
Differential input termination
Can't use DIFF_TERM on FPGA b/c VCCO=3.3
R57 100
R58 100
R59 100
R60 100
R61 100
R62 100
R63 100
R64 100
Layer-changing caps
C112 0.1 uF
C113 0.1 uF
C114 0.1 uF
C115 0.1 uF
C116 0.1 uF
D0_N is grounded on module, ground D0_P to reduce noise
(This is PRBS_OUT but we don't need it)
PMOD_HEADER
J5
PMOD header for sampling scope board
PMOD_HEADER
J6
Interface to I/O module
Andrew D. Zonenberg
Sheet: /Line Card/
File: line_card.sch
Title: STARSHIPRAIDER Single-Lane Host
Size: A4
Date: 2017-05-14
Rev: 0.1
KiCad E.D.A. kicad (6.0.0-rc1-dev-1427-g10887868d)
Id: 4/6



FPGA strap pins etc

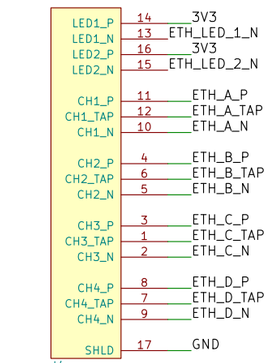
Andrew D. Zonenberg

Sheet: /FPGA support/

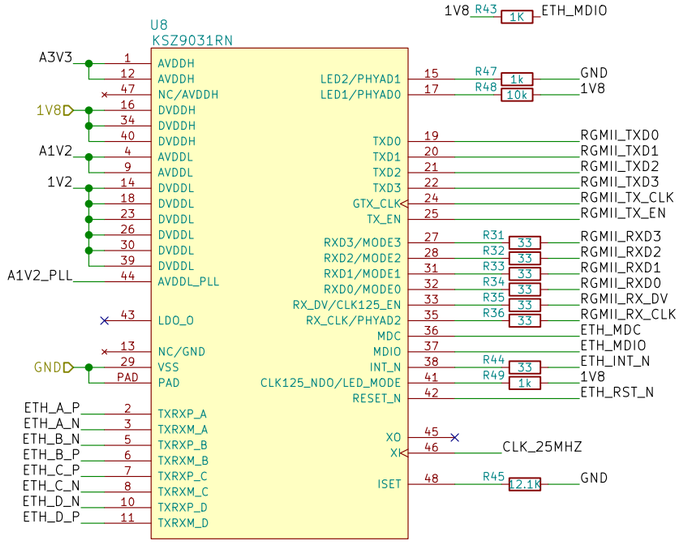
File: fpga_support.sch

Title: STARSHIPRAIDER Single-Lane Host

Size: A4	Date: 2017-05-14	**Rev: 0.1**
KiCad E.D.A. kicad (6.0.0-rc1-dev-1427-g10887868d)		Id: 5/6

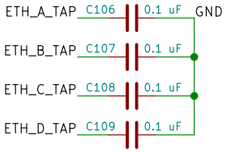


J4
BEL_FUSE_0826-1G1T-23-F



1V8 R43 1K ETH_MDIO

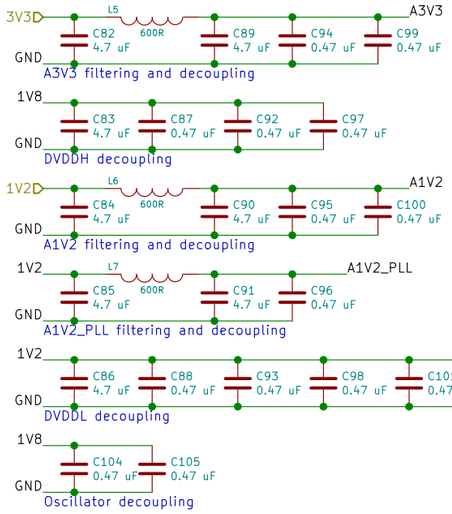
Need to pull RGMII_RXD[3:0] to 4'b1110,
and RGMII_RX_CLK to 1'b0, during reset of PHY
Use FPGA on-die pullups/downs for this

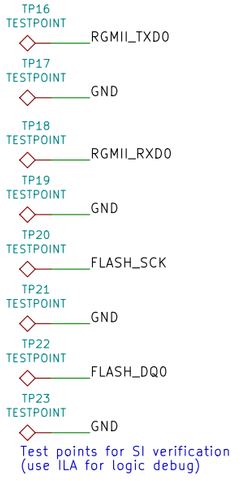


B/D pairs swapped for easier routing
(KSZ9031 auto-corrects)

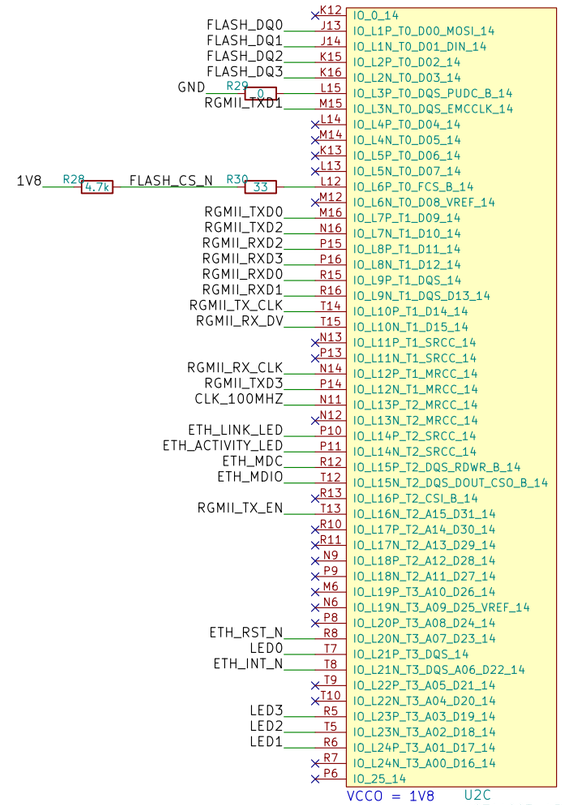
U9
DSC6101CI2A-025.0000
1V8 E/D# CLK R41 33 CLK_25MHZ
GND Vdd
Vss

U10
DSC6102CI2A-100.0000
1V8 E/D# CLK R42 33 CLK_100MHZ
GND Vdd
Vss

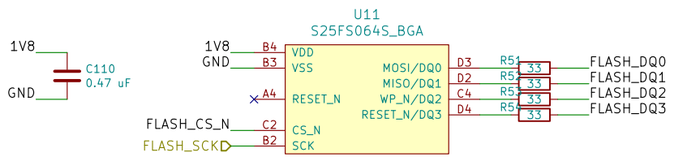


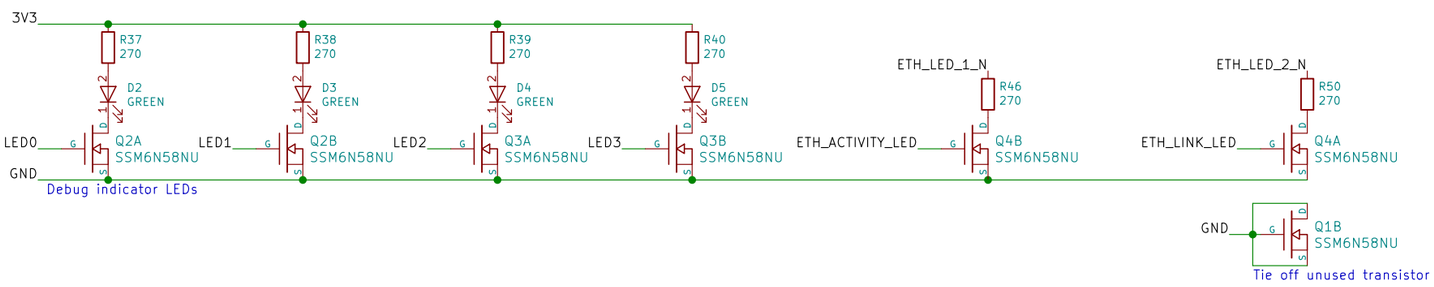


Test points for SI verification
(use ILA for logic debug)



VCCO = 1V8 U2C
XC7A100T-1FTG256C





Andrew D. Zonenberg
Sheet: /Flash / Ethernet/
File: flash_ethernet.sch

Title: STARSHIPRAIDER Single-Lane Host

Size: A3	Date: 2017-05-14	**Rev: 0.1**
KiCad E.D.A. kicad (6.0.0-rc1-dev-1427-g10887868d)		Id: 6/6