**Integration Manual**

**For**

**DigColPs**

**VERSION: 2.0**

**DATE: 12-MAY-2016**

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**Location:** The official version of this document is stored in the Nexteer Configuration Management System.

**Revision History**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Sl. No.** | **Description** | **Author** | **Version** | **Date** |
| 1 | Initial version | Jared | 1.0 | 08/22/13 |
| 2 | Implemented FDD v015 – ES20D | JK | 2.0 | 05/12/16 |

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# Abbrevations And Acronyms

|  |  |
| --- | --- |
| **Abbreviation** | **Description** |
| DFD | Design functional diagram |
| MDD | Module design Document |
|  | <ADD more to the table if applicable> |
|  |  |
|  |  |

# References

This section lists the title & version of all the documents that are referred for development of this document

|  |  |  |
| --- | --- | --- |
| **Sr. No.** | **Title** | **Version** |
| 1 | ES20D FDD | 015 |
|  | <Add if more available> |  |

# Dependencies

## SWCs

|  |  |
| --- | --- |
| **Module** | **Required Feature** |
| I2cNxtr | All functions |

Note : Referencing the external components should be avoided in most cases. Only in unavoidable circumstance external components should be referred. Developer should track the references.

## Global Functions(Non RTE) to be provided to Integration Project

None

# Configuration REQUIREMeNTS

## Build Time Config

|  |  |  |
| --- | --- | --- |
| **Modules** | **Notes** |  |
| **None** |  |  |

## Configuration Files to be provided by Integration Project

<Configuration file that will generated from this components that will require Da Vinci Config generation or manual generation. Describe each parameter >

## Da Vinci Parameter Configuration Changes

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Notes** | **SWC** |
| **<Configurator Changes for parameters>** |  |  |

## DaVinci Interrupt Configuration Changes

|  |  |  |  |
| --- | --- | --- | --- |
| **ISR Name** | **VIM #** | **Priority Dependency** | **Notes** |
| **<Configurator Changes for Interrupts>** |  |  |  |

## Manual Configuration Changes

|  |  |  |
| --- | --- | --- |
| **Constant** | **Notes** | **SWC** |
| D\_COMMBUFFERSIZE\_CNT\_U08 | 3 | I2cNxtr |
| I2c\_Notification | DigColPsInt\_InterruptNotification | I2cNxtr |
| D\_I2CREG\_STRCPTR | i2cREG1 | I2cNxtr |
| D\_VCLK\_HZ\_F32 | Set to corresponding VCLK frequency, commonly 8000000.0 for a 160.0 MHz part. | I2cNxtr |

# Integration DATAFLOW REQUIREMENTS

## Required Global Data Inputs

Refer .m file in FDD

## Required Global Data Outputs

Refer .m file in FDD

## Specific Include Path present

Yes

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| **Init** | **Scheduling Requirements** | **Trigger** |
| DigColPs\_Init1 | None | RTE(Init) |

|  |  |  |
| --- | --- | --- |
| **Runnable** | **Scheduling Requirements** | **Trigger** |
| DigColPs\_Per1 | Early in 2 ms task to minimize jitter | RTE (2 ms) |
| DigColPs\_Per2 | None | RTE (4 ms) |
| DigColPs\_Per3 | None | RTE (100 ms) |

**.**

# Memory Map REQUIREMENTS

## Mapping

|  |  |  |
| --- | --- | --- |
| **Memory Section** | **Contents** | **Notes** |
| DIGCOLPS\_START\_SEC\_VAR\_CLEARED\_32 | float32,uint32 |  |
| DIGCOLPS\_START\_SEC\_VAR\_CLEARED\_16 | uint16 |  |
| DIGCOLPS\_START\_SEC\_VAR\_CLEARED\_8 | uint8, sint8 |  |
| DIGCOLPS\_START\_SEC\_VAR\_CLEARED\_BOOLEAN | Boolean |  |
| DIGCOLPS\_START\_SEC\_VAR\_CLEARED\_UNSPECIFIED | LPF32KSV\_Str |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| **Feature** | **RAM** | **ROM** |
| **None** |  |  |

Table 1: ARM Cortex R4 Memory Usage

## NvM Blocks

Rte\_Pim\_DigColPsEOL

# Compiler Settings

## Preprocessor MACRO

None

## Optimization Settings

None

# Appendix

None