```
5980646 end // else: !if(`DWC_USB3_SSPHY_INTERFACE == 1)
5980626   #(`DWC_USB3_NUM_U3_ROOT_PORTS)
5980627    U_DWC_usb3_debounce_filter_PowerPresent (
5980628   .mac_clk               (mac_clk),
5980629   .mac_hwr_gswr_rst_n    (mac_hwr_gswr_rst_n),
5980630   .reset_filt_cntr       (reset_filt_cntr),
5980631   .reload_filt_cntr      (reload_filt_cntr),
5980632   .dat_in                (pipe3_PowerPresent_uf),
5980633   .debounce_time         (time_5ms),
5980634   .posedge_filter        (1'b1),
5980635   .bypass_filter         (bus_filter_bypass[1] | sb2ml_ssic_en),
5980636   .master_bypass         (sb2md_filter_bypass),
5980637   .ssr_restore           (ssr_restore),
5980638   .restore_value         (ssr_filter_cmd [3+`DWC_USB3_NUM_U3_ROOT_PORTS+`DWC_USB3_NUM_U2_ROOT_PORTS-1:3+`DWC_USB3_NUM_U2_ROOT_PORTS]),
5980639   .dat_filtered          (pipe3_PowerPresent_w),
5980640   .filter_done           (pwr_present_filter_done)
5980641  );
5980642 end // block: i_debounce_filter_PowerPresent
5980643 else begin : noti_debounce_filter_PowerPresent
5980644   assign pipe3_PowerPresent_w = 0;
5980645   assign pwr_present_filter_done = {(`DWC_USB3_NUM_U3_ROOT_PORTS){1'b1}};
5980646 end // else: !if(`DWC_USB3_SSPHY_INTERFACE == 1)
5980647 endgenerate
5980648
5980649 endmodule
5980650 MMMMMMMMMM_file_E_MMMMMMMMMMMM
5980651 ./d_ip_usb_ss_thang/usb30drd/rtl/taihang_usb3/src/bius/u3drd_DWC_usb3_bus_gs.v
5980652 MMMMMMMMMM_file_S_MMMMMMMMMMMM
5980653 //===========================================================================================
5980654 //
5980655 //  ------------------------------------------------------------------------
5980656 //
5980657 //                   (C) COPYRIGHT 2018 SYNOPSYS, INC.
5980658 //                           ALL RIGHTS RESERVED
5980659 //
5980660 //  proprietary to Synopsys, Inc.  Your use or disclosure of this
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5980662 //  license agreement between you, or your company, and Synopsys, Inc.
5980663 //
5980664 // The entire notice above must be reproduced on all authorized copies.
5980665 //
5980666 // Component Name   : DWC_usb3
5980667 // Component Version: 3.30b
5980668 // Release Type     : GA
5980669 //  ------------------------------------------------------------------------
5980670
5980671 //
5980672 //  Filename        : DWC_usb3_bus_gs.v
5980673 //  Author          : S.Arvind
5980674 //  Release version : 3.30b
5980675 //  Date            : $Date: 2018/04/23 $
5980676 //  File Version    : $Revision: #1 $
5980677 //  Revision        : $Id: //dwh/usb3_iip/rel/usb3_br_3.30a_cust_BF/DWC_usb3/src/bius/DWC_usb3_bus_gs.v#1 $
5980678 //  Description     : Slave BUS Interface Module. This conditionally instantiates
5980679 //                    either AHB, AXI, or OCP Slave Interface Module
5980680 //                Defines
5980681 //                  DWBB_BUS_GS_AHB_EN or DWBB_BUS_GS_AXI_EN or DWBB_BUS_GS_OCP_EN
5980682 // Modification History:
```