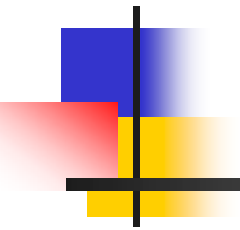
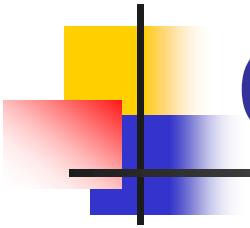


DSP ARCHITECTURE

18.12.2003



Outline

- Introduction
- Special Properties of DSP Architectures
- DSP Landscape
- Alternatives to DSP Processors
- Conclusions

Introduction

- A digital signal processor (DSP) is a type of microprocessor - one that is incredibly fast and powerful.
- It is a key component in many communication, medical, military and industrial products.
- A class of microprocessors optimized for DSP
- Have adventage in speed, cost and energy efficiency.

Introduction cont'd

- The FPGA Alternative:
  - Field-Programmable Gate Arrays have the capability of being reconfigurable within a system
  - But more expensive, have high power dissipation
- The ASIC Alternative:(Application Specific Integrated C.)
  - Application-specific ICs can be tailored to perform specific functions extremely well, and can be made quite power efficient.
  - But since ASICS are not field-programmable, their functionality cannot be iteratively changed or updated while in product development.

What is special for DSP?

- DSP architectures are molded by DSP algorithms.
- Fast Multipliers
- Multiple Execution Units
- Efficient Memory Access
- Data Format
- Efficient Zero-Overhead Looping
- Streamlined I/O
- Specialized Instruction Sets

Fast Multipliers:

- One of most used known algorithm:
  FIR filter.(Used to test processors)
  $y=\sum xh$
  x: vector of input data
  h: filter coefficients

Main operations: multiply & add

- Multiplication is one of the most common operations in signal processing (convolution, IIR filtering, Fourier Transforms...)

Fast Multipliers:

- Need fast multipy-accumulate operations
- Shift,multiply and add in a loop. Each require one or more cycle.
- Need to develope special hardware for multiplication
  - In 1982, Texas Instruments(TMS32010) (in a single clock cycle)
- All modern DSP processors include at least
  - one or more “dedicated, single-cycle multiplier” or
  - combined multiply-accumulate unit (MAC).

Multiple Execution Units

- Need to perform high computational tasks:
  - In real time
  - E.g. Filtering signals in 10-100Khz sampling rate in real time
- Several independent execution units required
  - Should operate in parallel
  - e.g. Arithmetic Logic Unit (ALU) and a shifter in parallel to MAC units

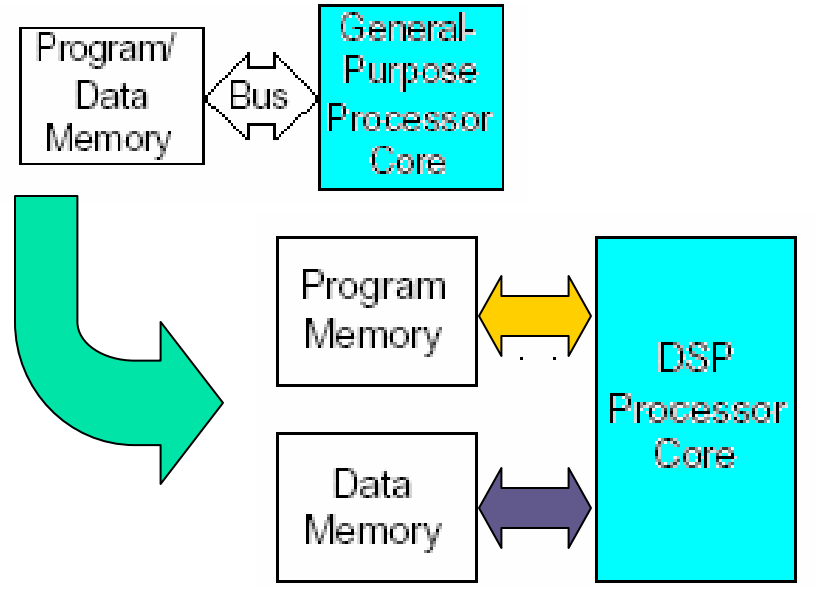
Efficient Memory Access

- Executing a MAC in a single cycle means:
  - → Fetching the MAC instruction in a single cycle
  - → Fetching a data sample in a single cycle
  - → Fetching a filter coefficient in a single cycle

  So, good performance requires high memory bandwidth!
- Commonly used approach:
  - Use two or more seperate memory banks:
    1. Each have its own bus
    2. Each could be read or written during every cycle.

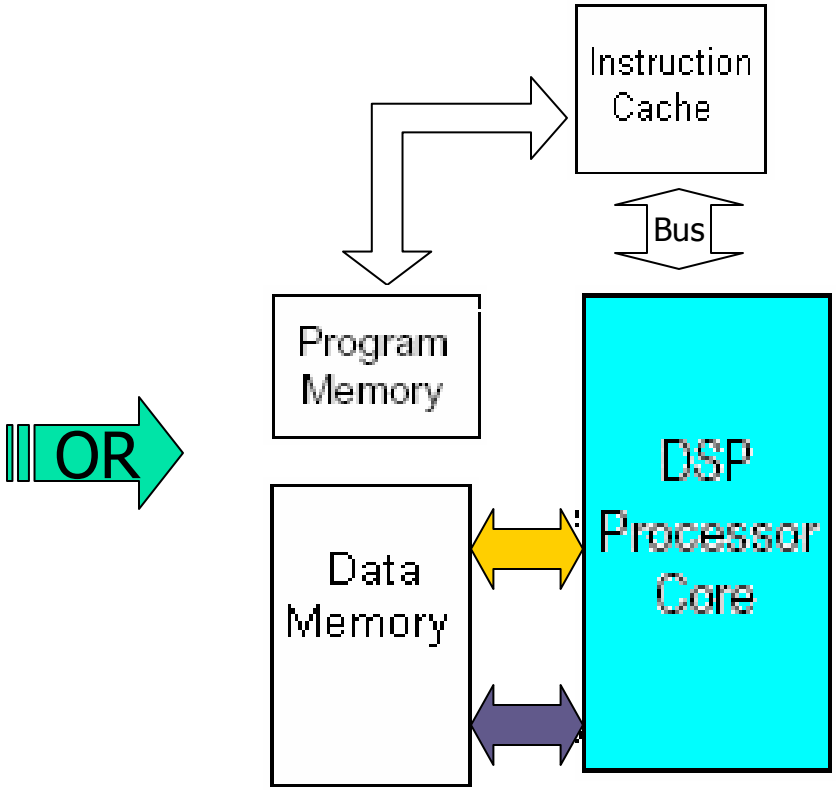
Efficient Memory Access

General purpose processors



Early DSP processors

More optimized DSP processors



High memory bandwidth requirement

- Support via dedicated hardware for calculating memory addresses:

  → Address Generation Units
- In DSP algorithms memory access is very predictable
  - E.g: FIR filter: coefficients accessed sequentially
- Use:
  1. Register indirect addressing with post increment
     - Inrement address pointer where repetitive computations are performed on a series of data.
  2. Circular Addressing
     - Allows processor to access data sequentially and then automatically wrap around to the beginning address

Data Format:

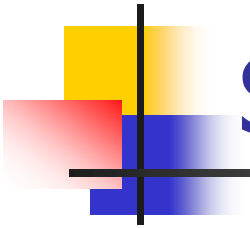
- DSP algorithms generally use floating point formats.
- Fixed point processors:
  - Cheaper and less power consuming
- Floating point formats require more complex hardware
- Use shortest data word width that will provide adequate accuracy
  - Consider the cost & energy consumption.

Data Format:

- Most fixed point DSP processors use 16 bit data words.
  - Sufficient for many applications
- Some use 20, 24 or 32 bit data word for better accuracy.
- Most DSP processors include one or more accumulator registers
- Accumulator Registers:
  - wider than other registers
  - Provide extra guard bits to avoid overflow

Efficient Zero Overhead Looping:

- DSP algorithms have many loops:
  - Use efficient looping
- Special loop: Zero Overhead Looping
  - No loop counter
  - No branching back to the top of the loop



Streamlined I/O:

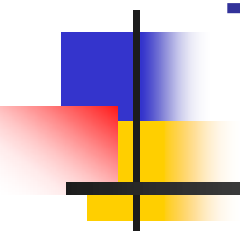
- Specialized serial or parallel I/O interfaces
- Streamlined I/O handling mechanisms
- E.g.:
  - Low overhead interrupts
  - Direct memory access, DMA.

Specialized Instruction Sets:

- Two goals in instruction sets:
  1. Make maximum use of hardware, increase efficiency
     - Programmer can specify parallel operations in single inst.s
  2. Minimize memory space required to store DSP programs.(Memory is a cost!)
     - Keep inst.s short.
       - → Use mode bits rather than encoding
       - → Restrict operations to specific registers
       - → Restrict operation combinations in the ints.
- This makes DSP instructions complicated

Specialized Instruction Sets:

- DSPs aren't usually programmed in high level languages: C,C++..etc
- Program optimization is essential
  - Programmer should optimize code in assembly level
- More easier inst. set , more desirable it is for programmer.



The Current DSP Architectures

1.Conventional DSP Processors

- 1980s' architecture.
- One ints. per cycle
- Include a single multiplier or MAC unit, an ALU, few execution units.
- 20-50Mhz operation frequency.
- Examples:
  - Analog Devices' ADSP-21xx family
  - Texas Instruments' TMS320C2xx family
  - Motorola's DSP560xx family

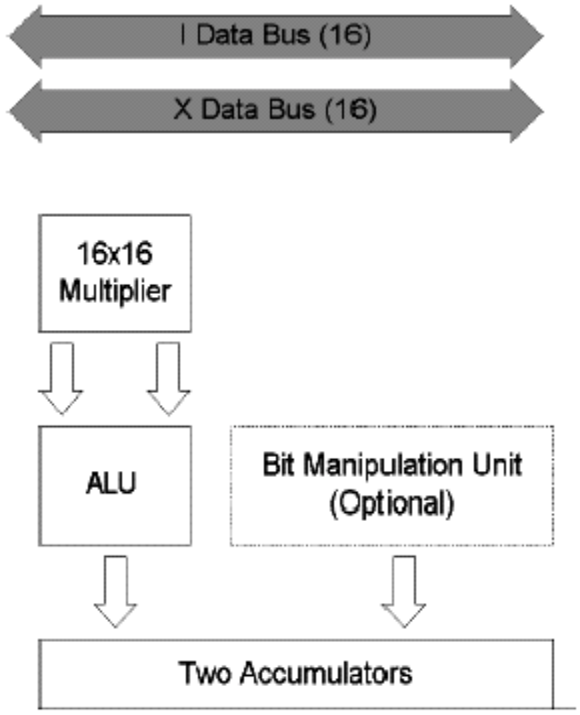
1.Conventional DSP Processors

- Midrange Processors:
  - Eg:
    - Motorola DSP563xx,
    - Texas InstrumentsTMS320C54x
    - Increased clock speed (100-150MHz)
    - Additional barrel shifter or instruction cache
    - Deeper pipeline
    - Low cost, low energy consuming
    - Used in wireless telecommunications applications, high speed modems

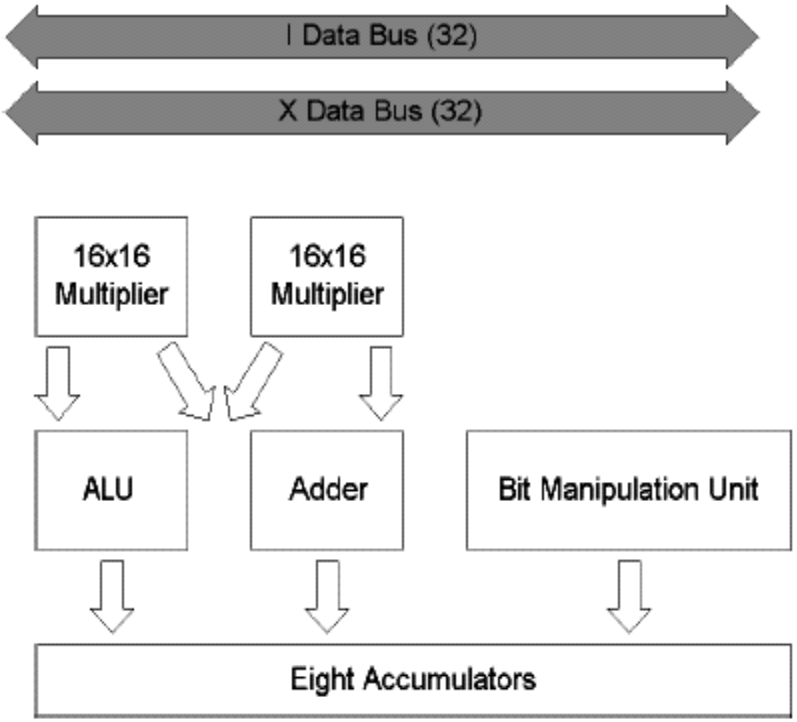
2. Enhanced DSP Processors

- Parallel execution units:
  - Second multiplier, adder units
- Extended instructions sets
  - More operations in a single instruction
- 2 MACS per clock cycle
- Wider data buses (more data words per clock cycle)

2. Enhanced DSP Processors



Conventional DSP processor (Lucent DSP16xx)



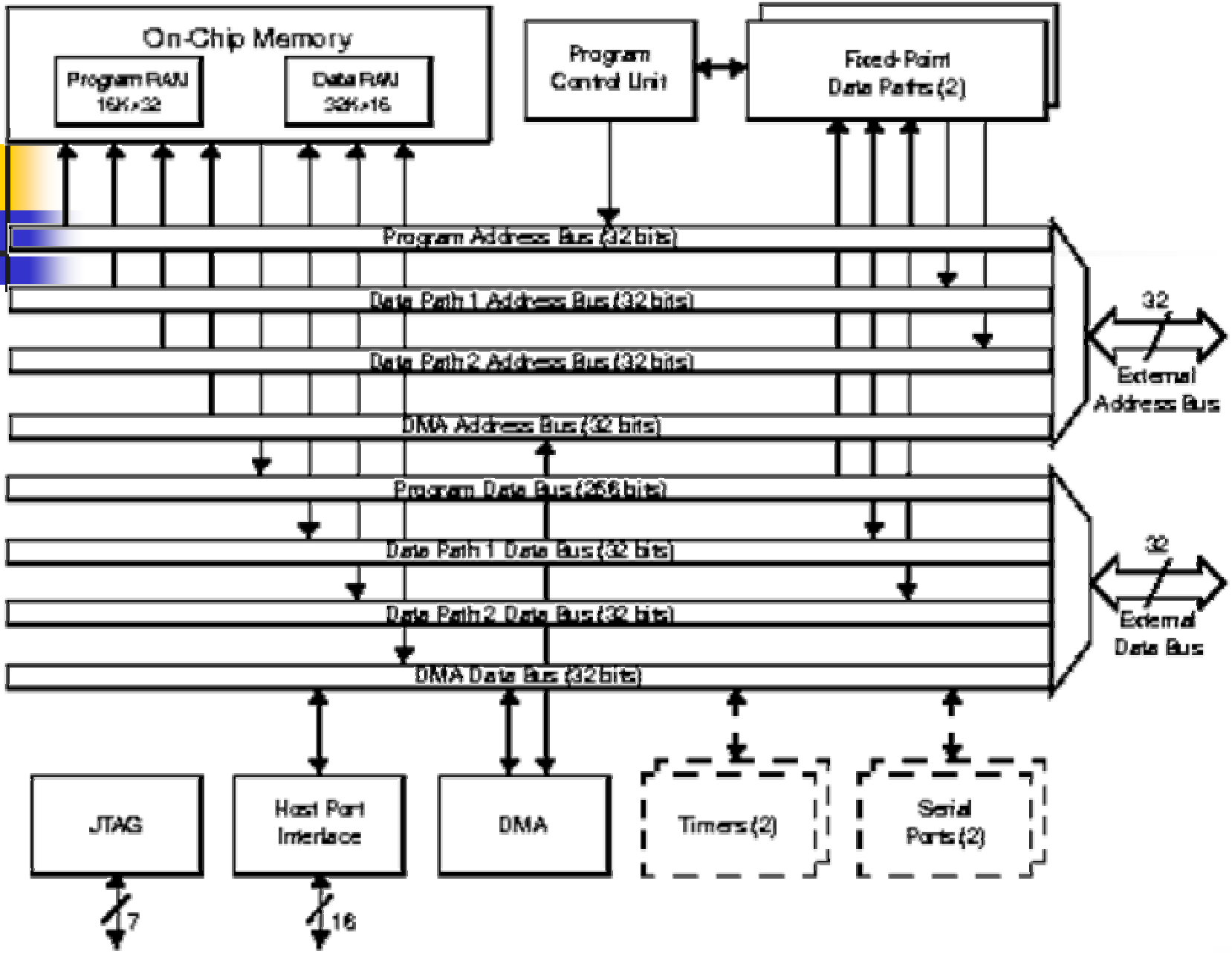
Enhanced conventional DSP processor (Lucent DSP16xxx)

3. Multi Issue Architectures

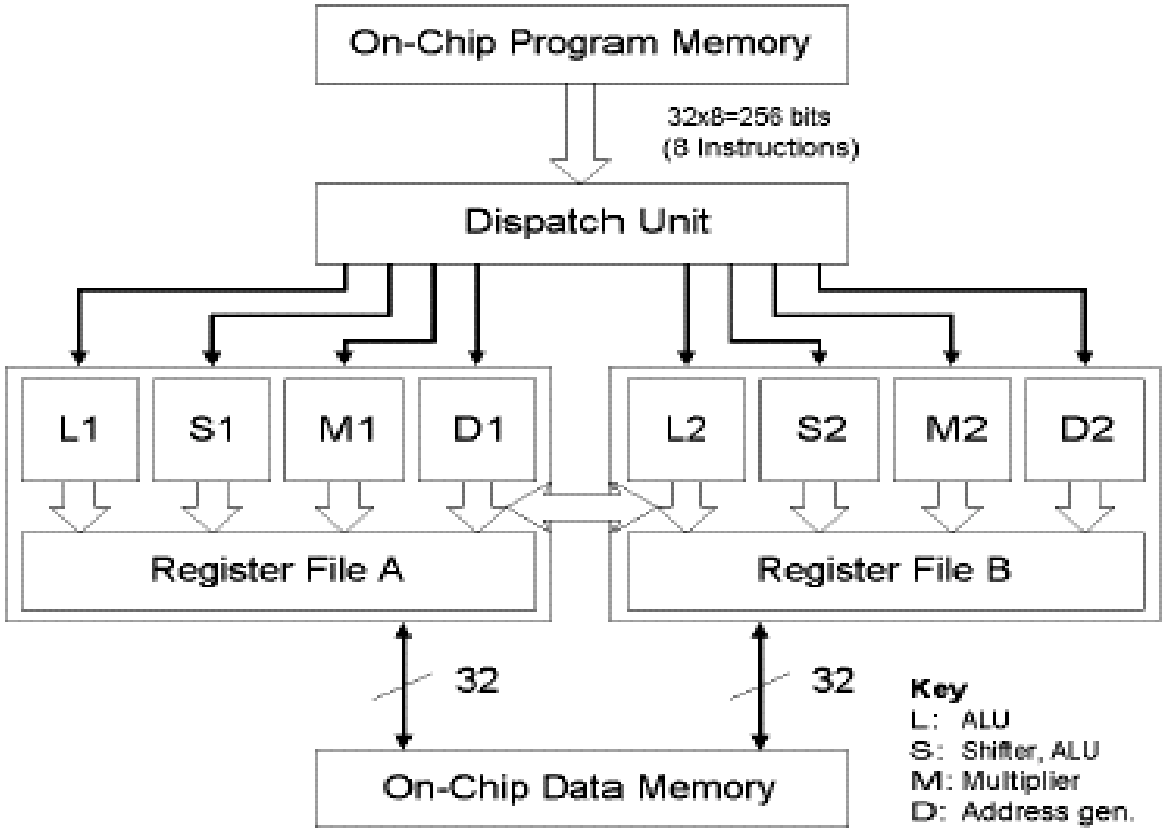
- Goal: Make programming easy. (Previous ones were difficult in assembly)
- Use very simple instructions
- Issuing & executing instructions in parallel groups
- Uses simple instructions:
  - Simpler instruction decoding and execution
- Now all vendors (TI, Analog Devices, Motorola, Lucent) employ multi issue architectures
- All current multi-issue DSP processors use VLIW approach

3. Multi Issue Architectures

- VLIW (Very long instruction word): A class of architectures that execute multiple insts. in parallel.
- VLIW provide many exec. units each is executing its own instruction.
- Typically issue a maximum of four or eight instructions per cycle
- The programmer specifies the instructions to be executed in parellel.
- Instructions grouped at the time program is assembled
- 32 bits instruction word rather than 16bits.


On-Chip Memory
Program RAM 16K×32
Data RAM 32K×16
Program Control Unit
Fixed-Point Data Paths (2)
Program Address Bus (32 bits)
Data Path 1 Address Bus (32 bits)
Data Path 2 Address Bus (32 bits)
DMA Address Bus (32 bits)
32
External Address Bus
Program Data Bus (256 bits)
Data Path 1 Data Bus (32 bits)
Data Path 2 Data Bus (32 bits)
DMA Data Bus (32 bits)
32
External Data Bus
JTAG
Host Port Interface
DMA
Timers (2)
Serial Ports (2)
7
16

3. Multi Issue Architectures



TMS320C62xx exec. units and memory architecture. It has eigth exec. units

Multi Issue Architectures

- L Units: (L1 for data path one, L2 for data path two)
  - each contain a 40-bit integer ALU
  - They are used for 32/40-bit arithmetic and compare operations, 32-bit logical operations, normalization, and bit count operations.
  - All L-unit operations execute in a single instruction cycle
- S Units: (S1 for data path one, S2 for data path two)
  - each contain a 32-bit integer ALU and a 40-bit shifter.
  - Used to perform 32-bit arithmetic, logical and bit field operations, and 32/40-bit shifts, branching, constant generation, and register transfers to and from control registers.
  - All S-unit operations execute in a single instruction cycle

- M Units:(M1 for data path one, M2 for data path two)
  - capable of performing 16x16->32-bit multiplications
- D Units:(D1 for data path one, D2 for data path two)
  - each contain a 32-bit adder/subtracter
  - used for address generation including linear and circular address calculations
- In the best case, all units operate in parallel, and the processor performs four arithmetic operations, two multiplications, and two address calculations in one instruction cycle.

3. Multi Issue Architectures

- Wider instructions
- Adventages:
  - Use of larger more uniform register sets
  - Specify which functional unit will exec. the instruction
  - Instructions have few restrictions on register usage and addressing modes making easier to program in assembly language
- Disadventages:
  - Simple instructions so,
    - require more instructions to perform a task
      - But words are wider
        - High program memory usage, high chip cost!

3. Multi Issue Architectures

- VLIW architectures use
  - Positional super instruction or
  - Keep routing information within each sub-instruction
- VLIW processors use wide buses to access data memory
- Faster and simpler lending itself to efficient compiler code generation
- But suffers energy consumption
- Can’t used in cellular phone

4. SIMD Technique

- SIMD(Single Instruction Multiple Data)
- Improves performance on some algorithms by allowing the processor to execute multiple instances of the same operation in parallel using different data.
- Increase performance on for vector operations
- Programmer must arrange data in memory.
- SIMD is only effective in algorithms that can process data in parallel!

Alternatives to DSP Processors

High Performance CPUs

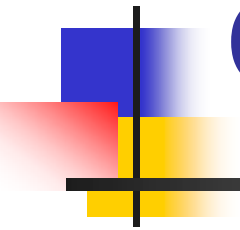
- Pentiums, PowerPCs.
- Added SIMD based instruction sets.
  - E.g: MMX ans SSE for Pentium, AltiVec for the PowerPC.
- Those have:
  - 64 bit data bus, 64 bit registers, 64 bit ALU.
  - 4 times the performance on 16 bit data (data size most offen used in DSP)
- Those CPUs typically operate at up 500MHz (much more than DSP processors' range)

High Performance CPUs

- So, why do we use DSP processor at all?
  - DSP processors provide the best mixture of:
    - Performance
    - Power consumption and
    - Price
  - Availability of development tools
  - For real time applications those CPU's can be problematic for their dynamic features.

DSP/Microcontroller Hybrids

- Used in applications that require mixture of "control oriented software" and "DSP software".
  - E.g : digital cellular phone
- Microcontroller: Good in contolling bad in DSP task
- DSP processors: Opposite of microcontroller.
- Combination performed using two seperate proc.:
  - A microcontroller and a DSP processor.
- Some vendors (Hitachi, ARM) added DSP functionality to microprocessor designs.



Conclusions

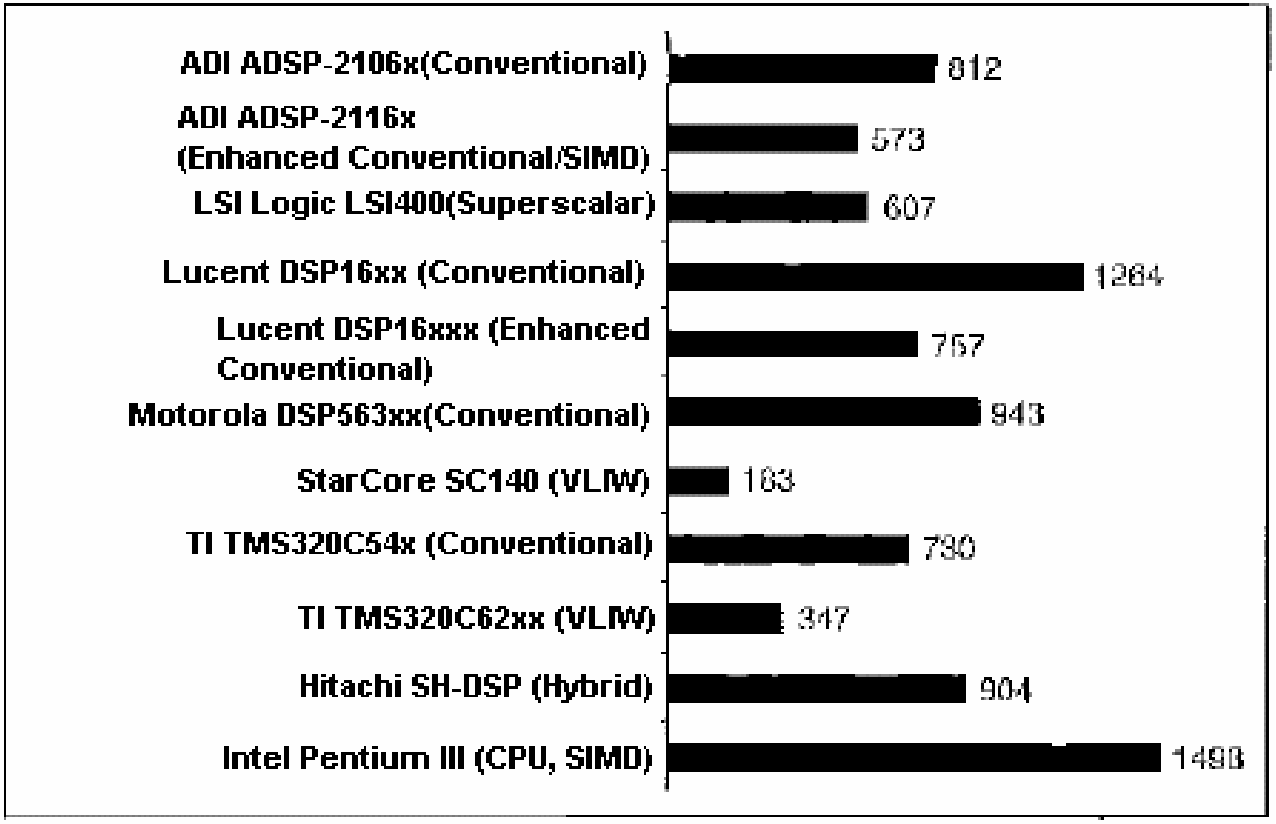
Conclusions

- Future works done for DSPs with increased speed, lower energy consumption, decreased memory usage.
- More influence on architecture that facilitate development of more efficient compilers.
- Focal point of new designs:
  - Allowing DSP applications to be written in high level language

Conclusions

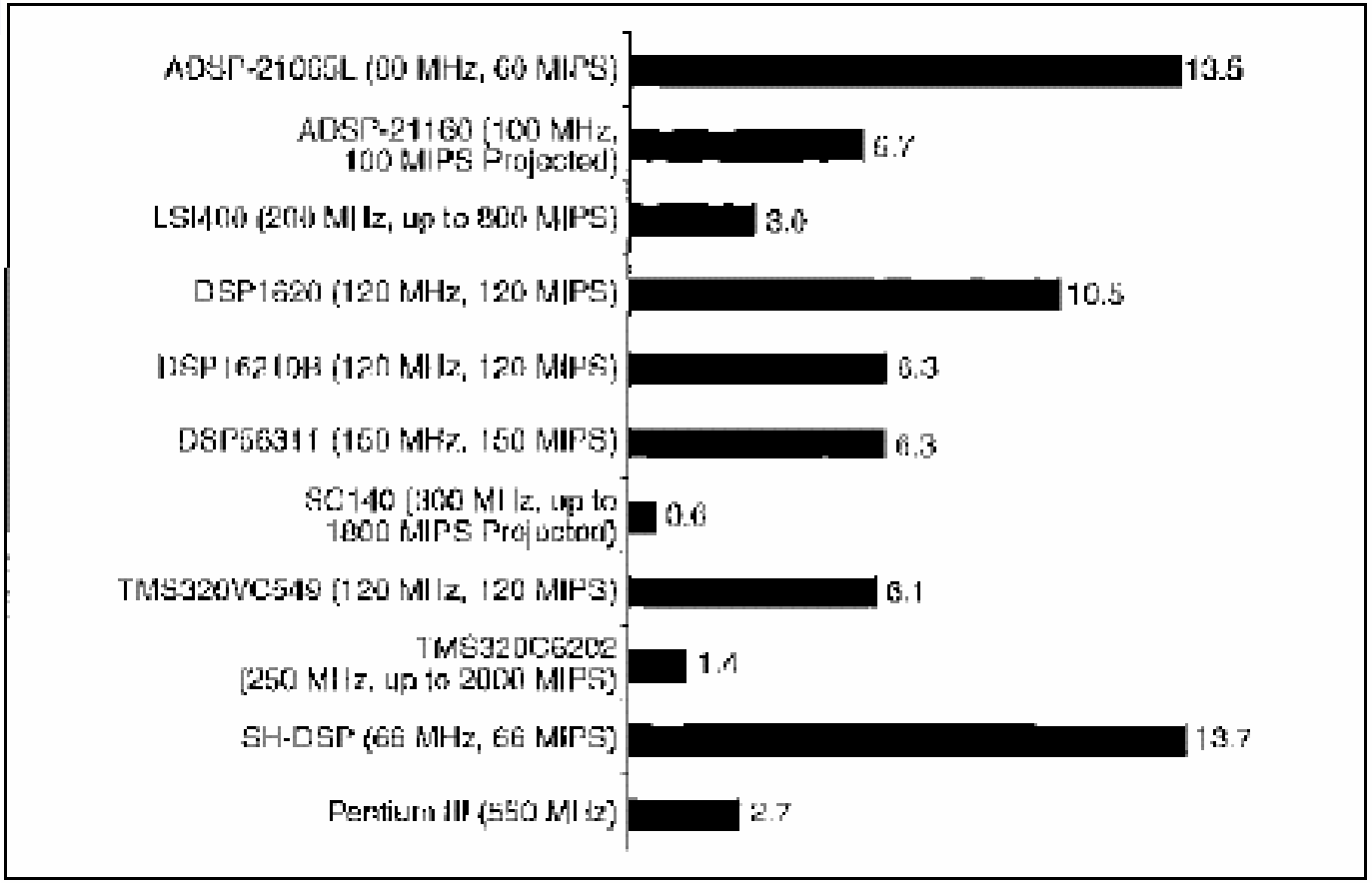
- Performance criteria:
  - The number of cycles required to exec. a task
  - Speed
  - Energy consumption
  - Memory usage

Comparing Performance



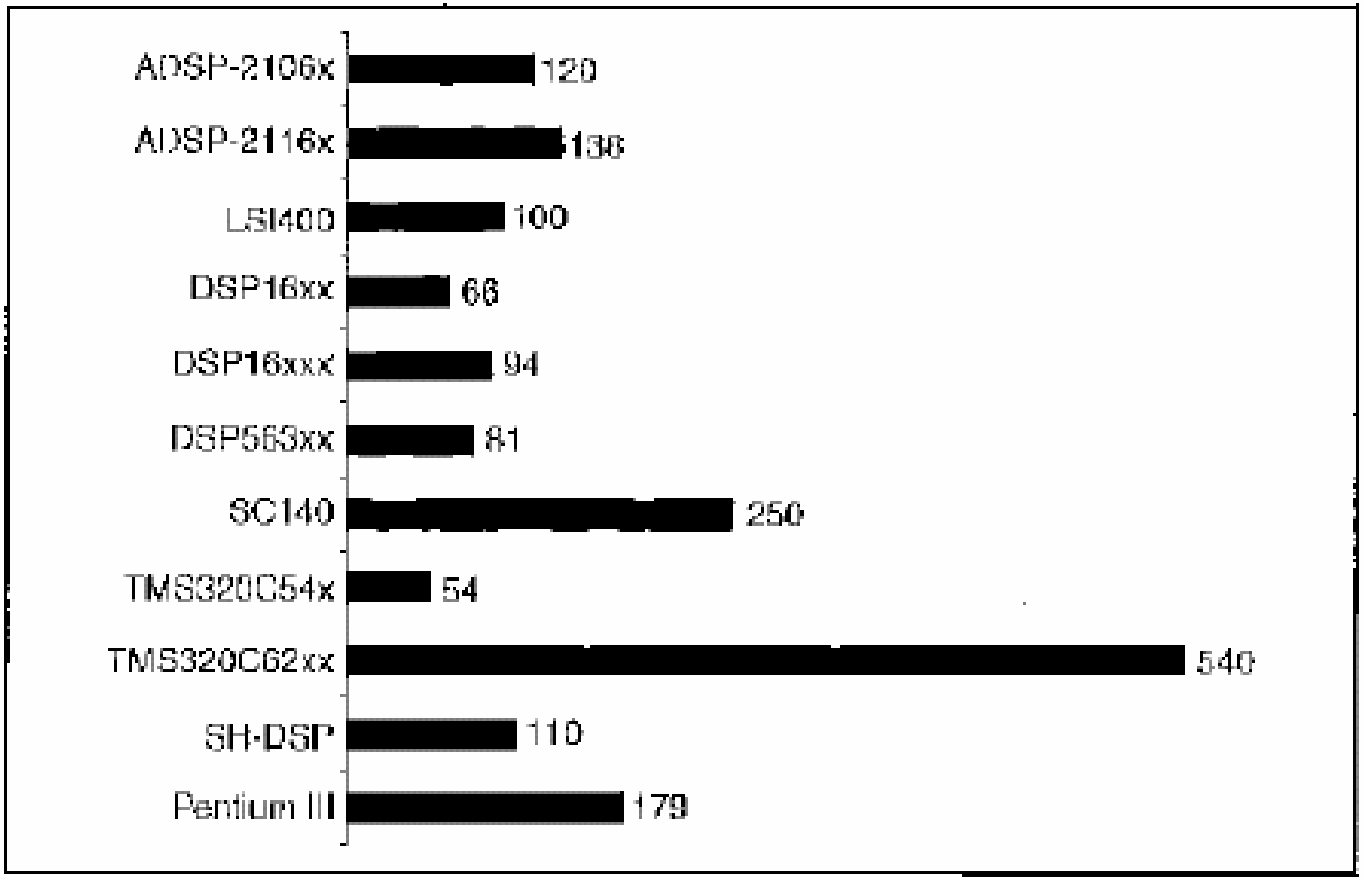
Cycle counts for FIR filter

Comparing Performance



Execution times for FIR filter

Comparing Performance



Program memory usage for FIR filter