Power Management

an embedded system perspective

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Agenda

- Introduction
- Basic Principles of Power Consumption
- Low Power Design
  - PM Techniques
  - Architectural Blocks for PM

Why should we interest on *Power Management*?


AP / Paul Sakuma

It make us happy!?

The need of more and more complex portable and wireless applications requires better effort on designing low power system solutions

Introduction
Low Power Design Concerns

Battery lifetime

Cooling and energy costs

System reliability

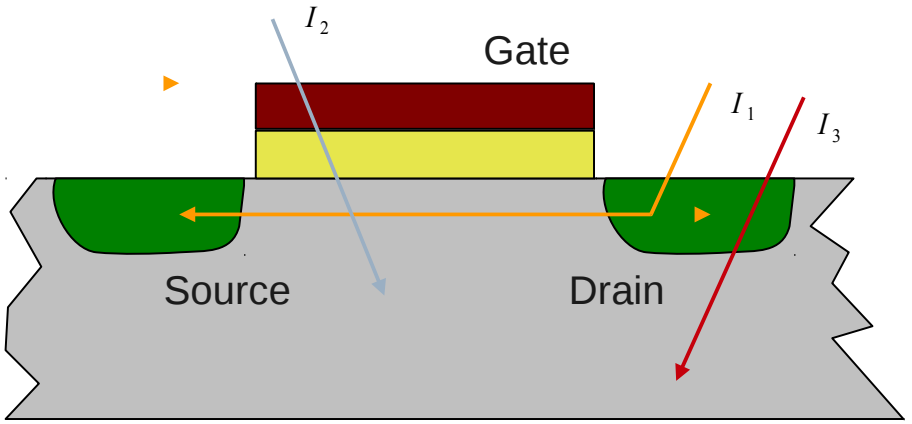
Environmental concerns

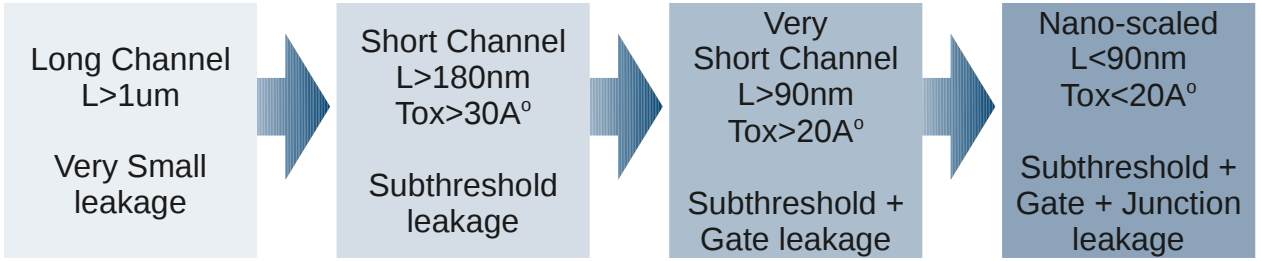
- Physical Gate Length decrease
  new IC are manufactured using sub-micro production technology process
- Transistors number increase
  more and more transistors are integrated within single chips
- Frequency increase
  modern embedded systems could operate at hundreds MHz
- Performances increase
  more and more complex operations delivered by single chip
- Battery discharge rate is super-linearly related to the average power consumption in the VLSI circuits
  excessive discharge rate and varying load conditions will have a negative effect and shorten the battery life

higher power density and increasing leakage

Power Consumption
Leakage Components

- Main components
  - Subthreshold Leakage
  - Gate Leakage
  - Junction Leakage
- Other components
  - Gate Induced Drain Leakage
  - Impact Ionization current
- Overall and relative contribution depends on technology node





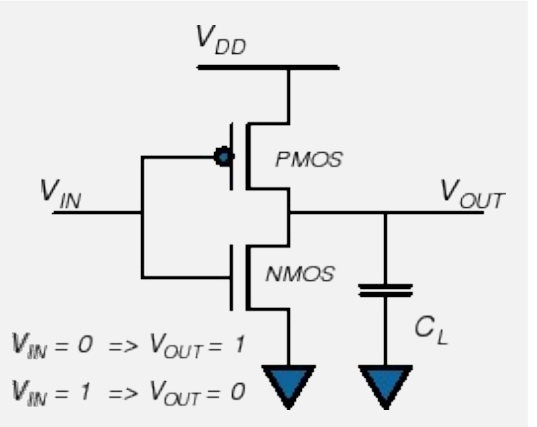
Power Consumption
Basic Principles

$$P = 0.5V_{DD}^2 f_{clock} C_L E_{sw} + t_{sc} V_{DD} I_{peak} f_{0\to1} + V_{DD} I_l$$

- Switching (or dynamic) power

  E_{sw} *represents the probability that the output node makes a transition at each clock cycle*

  models the fact that, in general, switching does not occur at the clock frequency
  it is called the switching activity of the gate



CMOS Inverter

- Short-circuit power
- Leakage (or static) power

  $I_L \sim I_{SUB} + I_{GATE}$

  in older technologies (250nm and above) was marginal w.r.t. switching power

  in deep sub-micron processes becomes critical accounting for about 35-50% of power budget at 90nm

Power Consumption
Technology Scaling Effects on Power Consumption

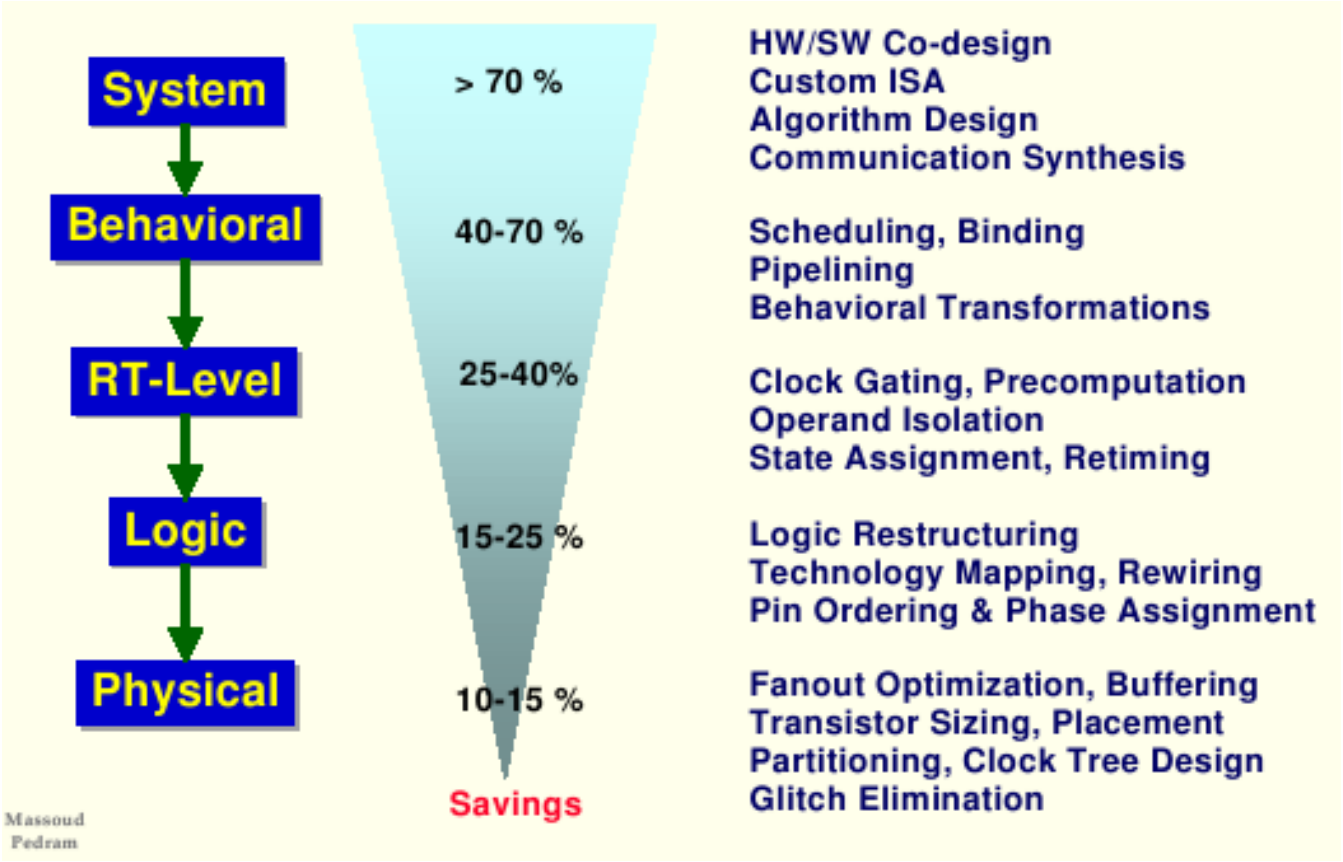
- Higher device densities
  - *smaller capacitance per gate to be charged and discharged*
  - *… but many more gates per chip*
  - => higher switched capacitance
- Higher clock frequencies

Increased dynamic-power consumptions

- Lower supply voltages
  - *lower switching power, lower speed*
  - *… but lower threshold voltages*
- Higher operating temperatures

Increased leakage-power consumptions

Power Consumption
Power Saving Opportunities

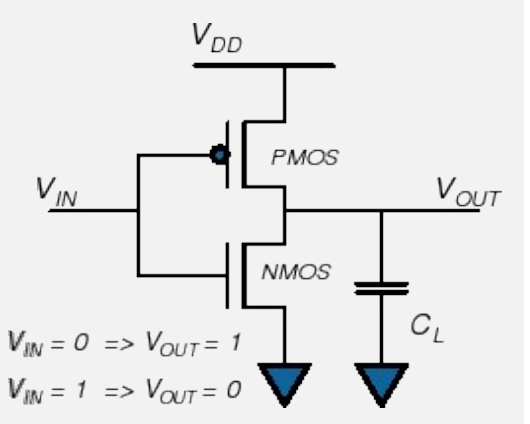


Power Consumption

Architectural Power Reduction Approaches

$$P = 0.5V_{DD}^2 f_{clock} C_L E_{sw} + t_{sc} V_{DD} I_{peak} f_{0\to1} + V_{DD} I_l$$

- Switching (or dynamic) power
  - reduce supply voltage
    - *quadratic effect => higher savings*
    - *negative effect on performance*
  - reduce clock frequency
  - reduce switched capacitance
  - reduce wasteful switching
- Short-circuit power
- Leakage (or static) power
  - reduce supply voltage
- Many techniques apply at logical and physical level



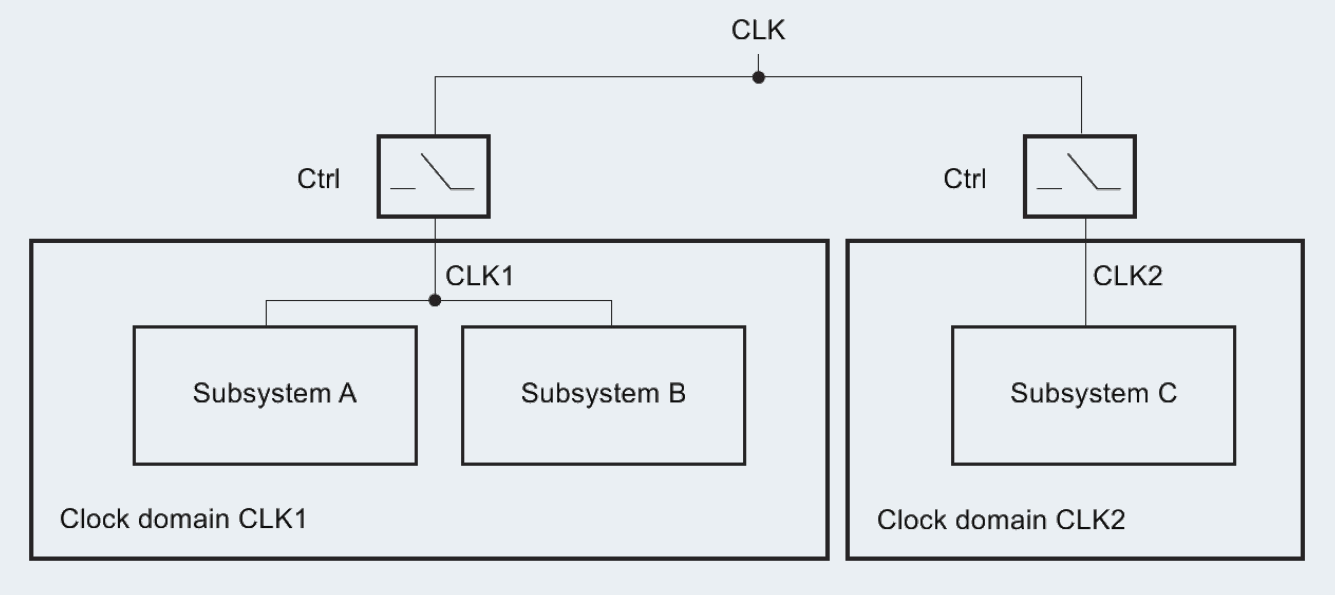
Architectural Blocks for PM
Clock Domains

- Group of modules fed with the same gated clock
- Support clock gating

  cut a clock to a group of inactive modules to lower their active power consumption

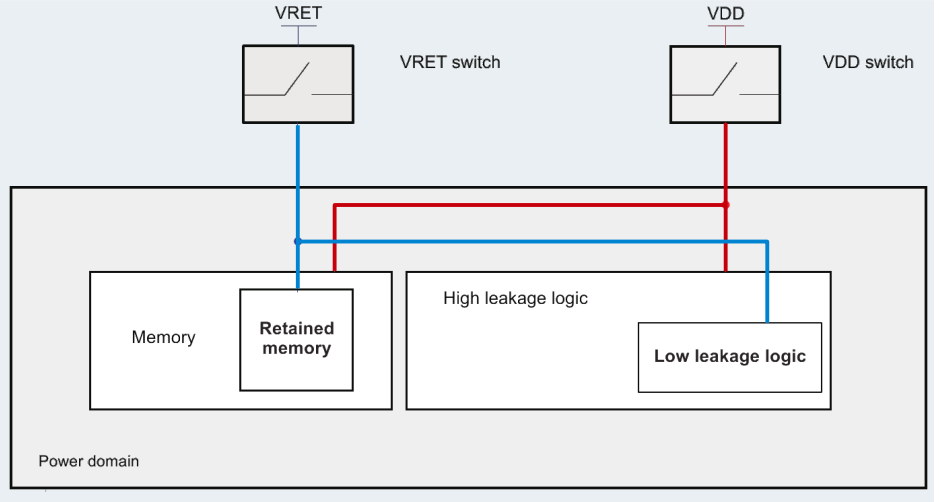
  two possible states: active or inactive

  => control of dynamic power consumption



Architectural Blocks for PM
Power Domains

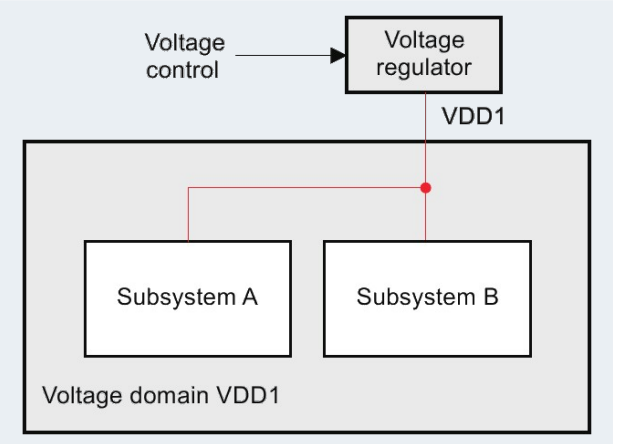
- Section of the device with dedicated power rails
- Supplied by two voltage sources
  - VDD active voltage source (normal operating voltage)
  - VRET retention voltage source
    - *less than active voltage => less power consumption*
    - *logic and memory are not operational, but their content or state is retained*



- Retention state
  - in addition to on/off
    - *useful for quickly switching to low-power idle mode without losing the context and quickly switching back to active state when necessary*

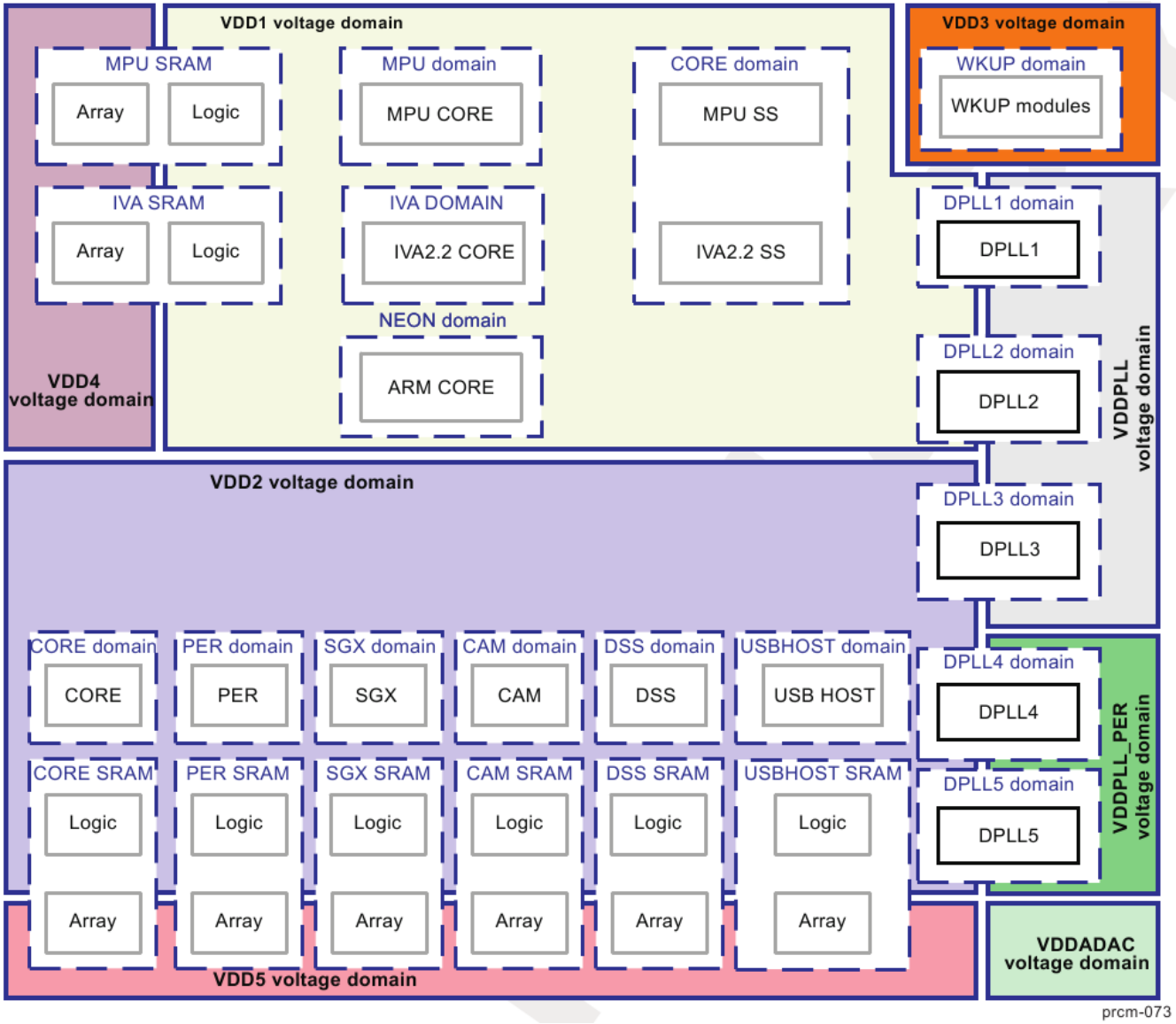
Architectural Blocks for PM
Voltage Domains

- Group of modules supplied by the same V regulator
  - power consumptions can be controlled by regulating voltages independently
- Assign different operating V to the different modules
  - voltage scaling of device subsections
    - *based on application performance requirements*
- Lower voltage to reduce power consumption
  - when all modules are inactive
  - switch back to normal operating V only when a wake-up event is received



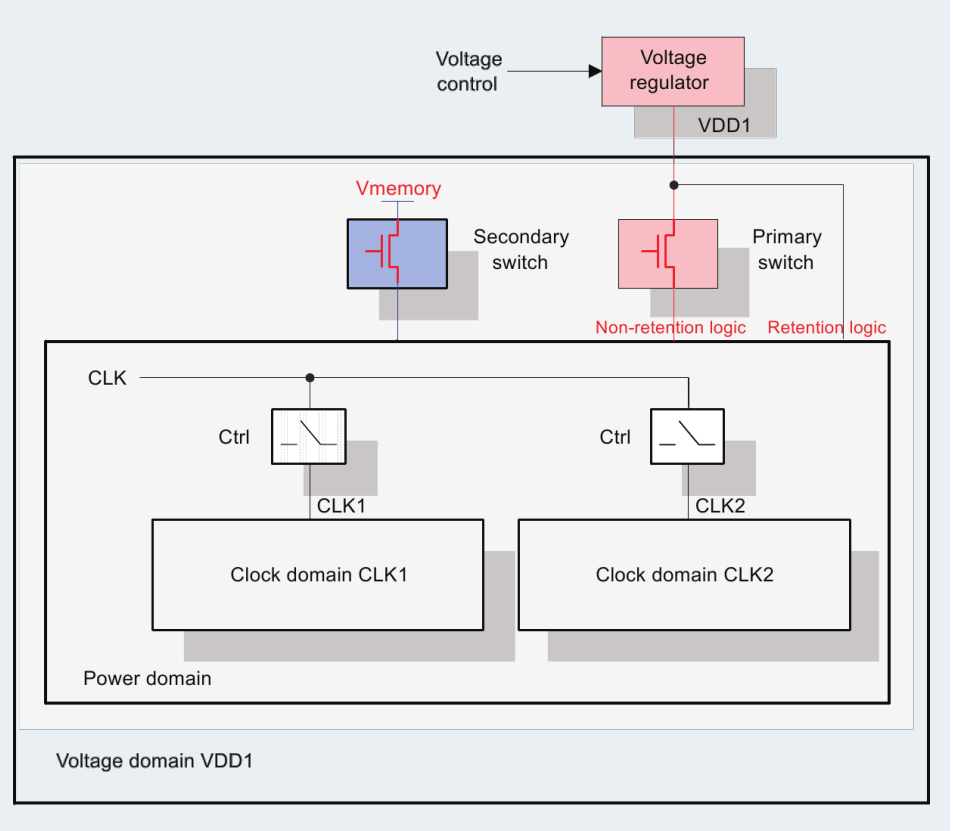
Architectural Blocks for PM

OMAP35xx Voltage Domains



Device PM Architecture
Domains Hierarchical Architecture

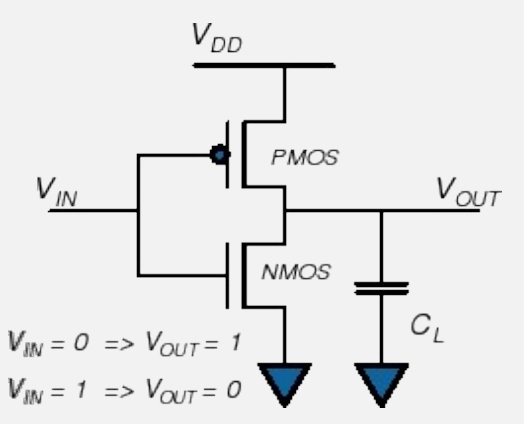
- Scalable/switchable voltage domains
- Switchable power domains
- Switchable clock domains
  - subset of a power domain



Power Management Techniques
System Power Reduction Approaches

$$P = 0.5V_{DD}^2 f_{clock} C_L E_{sw} + t_{sc} V_{DD} I_{peak} f_{0\to1} + V_{DD} I_l$$

- Switching (or dynamic) power
  - reduce supply voltage
    - *quadratic effect => higher savings*
    - *negative effect on performance*
  - reduce clock frequency
  - reduce switched capacitance
  - reduce wasteful switching
- Short-circuit power
- Leakage (or stand-by) power
  - reduce supply voltage
- Many techniques apply at logical and physical level



Power Management Techniques
Interface and Functional Clocks

- Each module can have two type of clock

Interface clocks (ICLK)

ensure proper communication

supply the module interface and registers

can have several

synchronous across the entire device

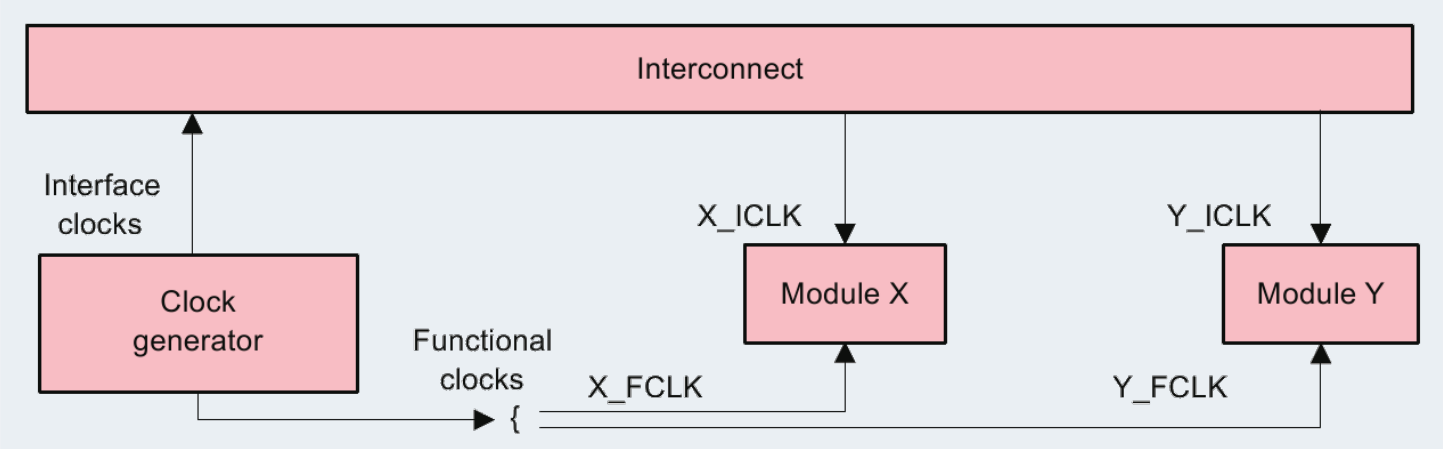
management is done at the device level

Functional clocks (FCLK)

supply the functional part

can have several or none at all

several modules can share the same



Power Management Techniques
Auto-idle Clock Control

- Device can supports an auto-idle clock control scheme
  - for the module interface clocks (ICLK)
  - executes under hardware control
    - *HW controller automatically activate/deactivate ICLK*
- Two device module types
  - *Initiator* (e.g. uP, DMA, MMU)
    - *can generate bus transactions (read, write, etc.)*
    - *active: when generates transactions*
  - *Target*
    - *passive module that can process bus transactions*
    - *active: when ICLK and some or all FCLK are available*
- Idle modules can have ICLK gated
  - can still receive functional clocks
    - *can generate interrupts, DMA requests, async wakeup-requests*

Power Management Techniques
DVFS - Dynamic Voltage and Frequency Scaling

- Allocate a variable amount of energy to perform a task
  - power consumption of a digital CMOS circuits

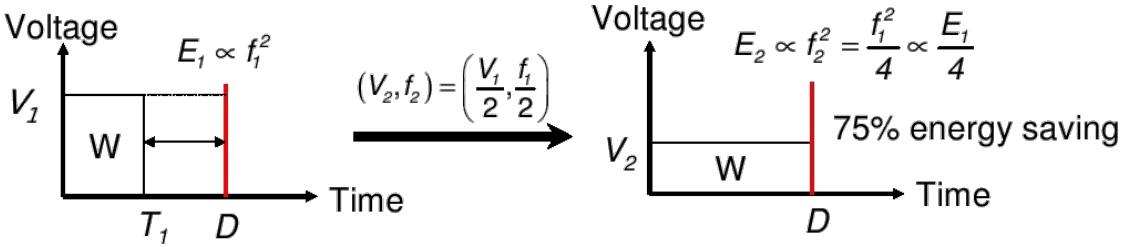
$$P = \alpha \cdot C_{eff} \cdot V^2 \cdot f$$

α	*switching factor*
C_{eff}	*effectivecapacitance*
V	*operating voltage*
f	*operating frequency*

  - energy required to run a task during T

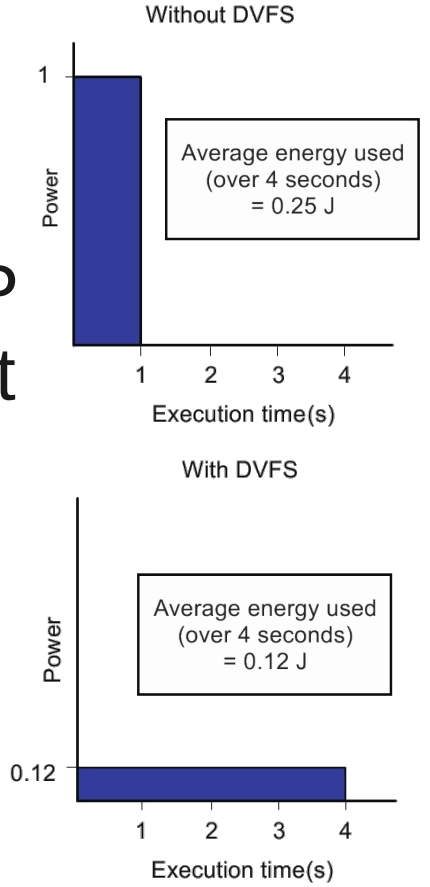
$$E = P \cdot T \propto V^2 \qquad (assuming\ f \propto V\ ,\ T \propto f^{-1})$$

Lowering V, while simultaneously and proportionately cutting f, causes a quadratic reduction in E



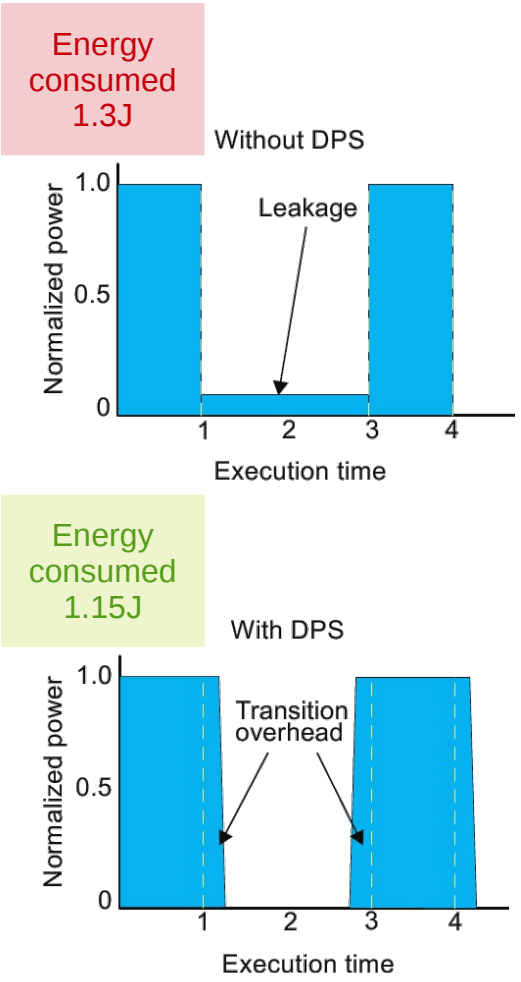
Power Management Techniques
DVFS - Dynamic Voltage and Frequency Scaling (Cont.)

- Minimize system idle time
  - dynamic selection of optimal frequency and voltage
    - *allow a task to be performed in the required amount of time while still meeting task requirements*
- Operating Performance Points (OPP)
  - a voltage (V) and frequency (F) pair
- The system always runs at the lowest OPP that meets the performance requirement at a given time
    - => *reduces both dynamic and leakage power consumption*
- We must be able to identify optimal OOP



Power Management Techniques
DPS - Dynamic Power Switching

- Maximize system idle time
  - automatic switch to a low-power mode
    - *minimum power consumption*
    - *if wake-up latency conditions allow it*
  - runs tasks at the highest OPP
    - *complete tasks quickly*
- Aimed at reducing active power consumption
  - reduces only leakage power consumption
  - introduce transitions overhead
    - *slight dynamic power consumption*
    - *exit-latency*
- Must predict dynamical performance requirement of applications

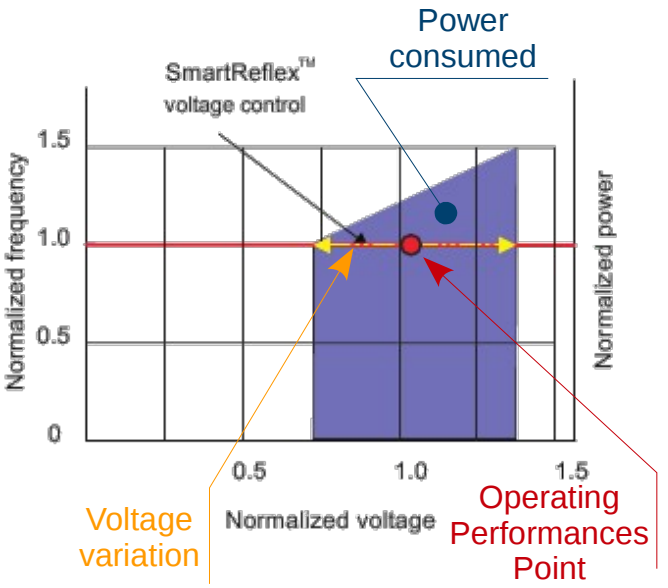


Power Management Techniques
SLM - Standby Leakage Management

- Trades static power consumption for wake-up latency
  - remains in lowest static power mode (retention modes)
    - *compatible with the system response time requirement*
- Similar to DPS
    - *switching the system between high- and low-power modes*
  - different operating timescales
    - *latency allowed for mode transitions*
      - *DPS: compared to time constraints or deadlines of the application*
      - *SLM: compared to user sensitivity so that they do not degrade user experience*
  - different context
    - *who define the transition constraints*
      - *DPS: tasks are running and we must grant application performances*
      - *SLM: applications not running and must grant system responsiveness*
  - different wake-up events
    - *events used to exit the low-power mode*
      - *DPS: application-related, e.g. timer, DMA request, peripheral interrupt, ...*
      - *SLM: user-related, e.g. touch screen, key pressed, peripheral connections, ...*

Power Management Techniques
AVC - Adaptive Voltage Control

- Provide automatic control of the operating voltage
- Silicon performances/power trade-off
  - depends on
    - *technology process*
    - *operating temperature variations*
- Power-supply voltage is adapted to silicon performance
  - statically
    - *based on performance points*
  - dynamically
    - *based on the temperature-induced real-time performance of the device*

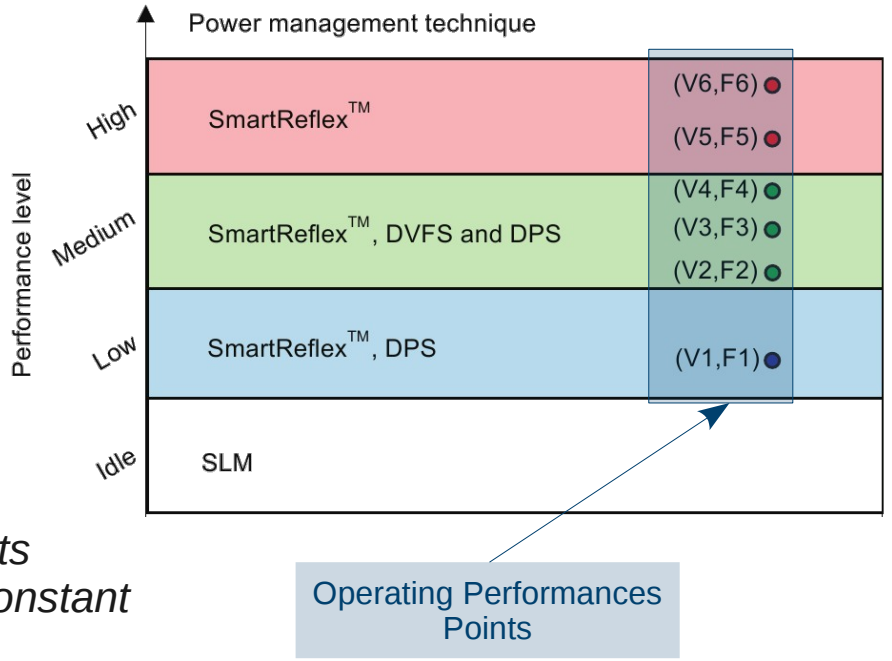


- Achieves optimal performance/power trade-off
  - *for all devices and across the technology process spectrum and temperature variations*

Power Management Techniques
Combining PM Techniques

- PM techniques are most effective when used under specific conditions

  best active power saving is obtained by combining them



AVC

boot-time: adapt voltage to device process characteristics
always: compensate temperature variations

DVFS

varying application performances requirements
without DPS to scale F while keeping the V constant
reduce peak power consumption
improve temperature dissipation and battery life

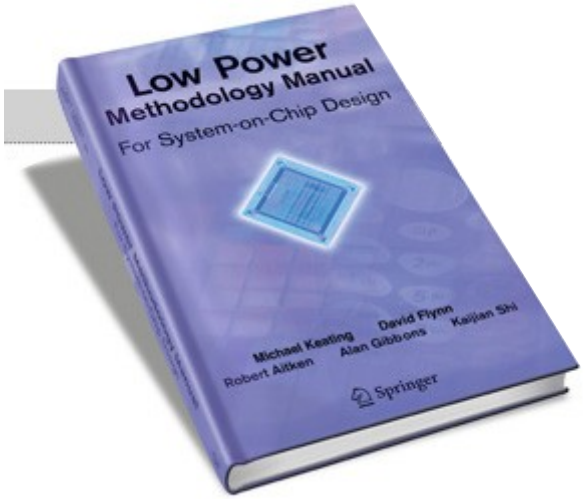
DPS

performance requirements between two OPPs or below the lowest OPP
with DVFS: always set F to max allowed at given V

SLM

no applications running and performance requirement drops to zero

References



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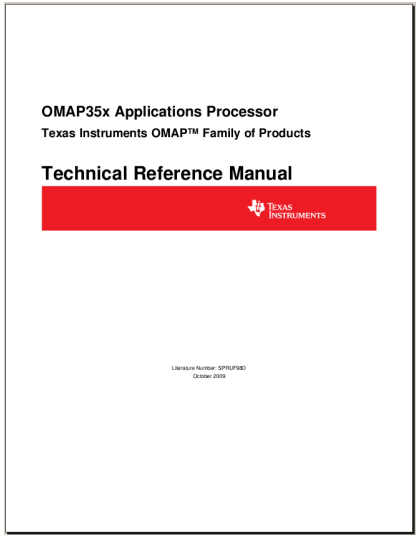

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