

POLITECNICO DI MILANO



High Performance Processors and Systems

Dynamic Scheduling

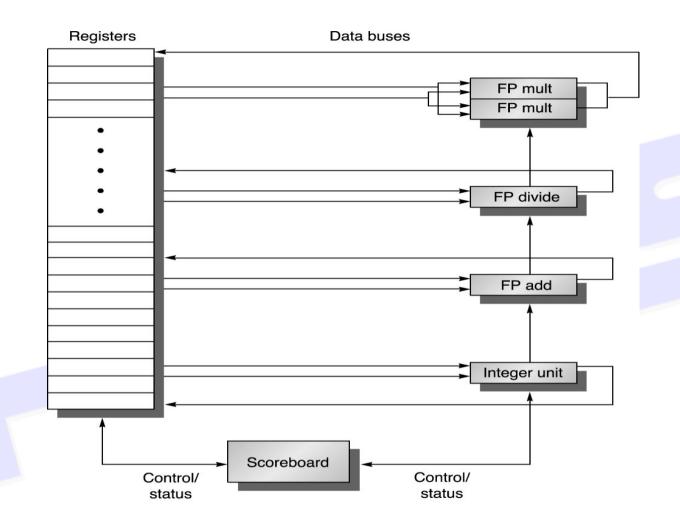
Welcome to the world of Scoreboard and Tomasulo - aka T&S those strangers...

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MIPS with Scoreboard



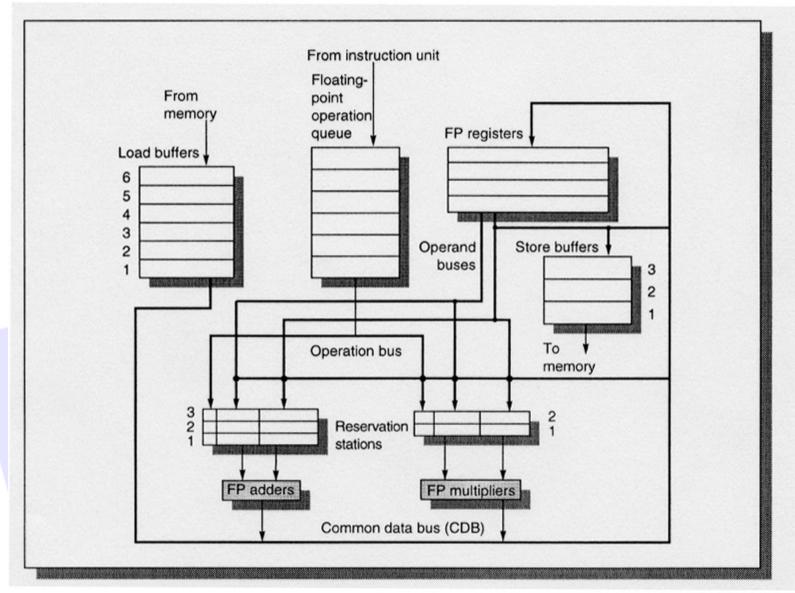
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Tomasulo Approach







RAW Conflict

S1: ADDD F0, F2, F4

S2: MULTD F2 F6, F8

S3: MULTD F10, F0, F2







S1: ADDD F0, F2, F4

S2: MULTD F2 F6, F8

S3: MULTD F10, F0, F2

Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	P	Rk	Εt	lst		Issue	Read Op	Exec Co.	W. ite	R.
Mult1	YES	MULT	F2	F6	F8			NO	NO	Λ	S2	addd	1	2	4		5
mult2	YES	MULT	F10	F0	F2		MULT1	YES	NO		S3	multd	2	3	7		
Add1	YES	ADD2	F0	F12	F14			TES	TES	Z	54	multd	3				
Add2	NO											addd	6	7			
F0	F2	F4	F6	F8	F10	F12	F14										
ADD1	MULT1				MULT2												





S1: ADDD F0, F2, F4

S2: MULTD F2 F6, F8

S3: MULTD F10, F0, F2

Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk /	Et	lst		Issue	Read Op	Exec Co.	Write R.
Mult1	NO											addd	1	2	4	5
mult2	YES	MULT	F10	F0	F2			YES	YES		S3	multd	2	3	7	8
Add1	YES	ADD2	F0	F12	F14			NO	NO	П	54	multd	3			
Add2	NO											addd	6	7		
F0	F2	F4	F6	F8	F10	F12	F14									
ADD1					MULT2											







S1: ADDD F0, F2, F4

S2: MULTD F2 F6, F8

S3: MULTD F10, F0, F2

_																
Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk /	Et	lst		Issue	Read Op	Exec Co.	Wite R.
Mult1	NO											addd	1	2	4	5
mult2	YES	MULT	F10	F0	F2			YES	YES	4	S3	multd	2	3	7	8
Add1	YES	ADD2	F0	F12	F14			NO	NO	U	54	multd	3	9		
Add2	NO											addd	6	7	9	
F0	F2	F4	F6	F8	F10	F12	F14									
ADD1					MULT2											







S1: ADDD F0, F2, F4

S2: MULTD F2, F6, F8

S3: MULTD F10, F0, F2

Name	Op	Vj	Vk	Qj	Qk	E time			Issue	Exec Co.	Write R.
mult1	MULT	R(F6)	R(F8)			0		addd	1	3	4
mult2	MULT	M(A1)			MULT1			multd	2	6	
add1								multd	3		
add2	ADD	R(F12)	R(F14)			0		addd	4	6	
F0	F2	F4	F6	F8	F10	F12	F14				
ADD2	MULT1				MULT2						
						1		1			







S1: ADDD F0, F2, F4

S2: MULTD F2 F6, F8

S3: MULTD F10, F0, F2

Name	Op	Vj	Vk	Qj	Qk	Lime			issue	Exec Co.	Write R.
mult1								addd	1	3	4
mult2	MULT	M(A1)	M(M1)					multd	2	6	7
add1								multd	3		
add2	ADD	R(F12)	R(F14)			()	addd	4	6	
F0	F2	F4	F6	F8	F10	F12	F14				
ADD2					MULT2						







S1: ADDD F0, F2, F4

S2: MULTD F2 F6, F8 S3: MULTD F10, F0, F2

Name	Op	Vj	Vk	Qj	Qk	Etim€			Issue	Exec Co.	Write R.
mult1						<u>+</u>		addd	1	3	4
mult2	MULT	M(A1)	M(M1)			3		multd	2	6	7
add1								multd	3		
add2								addd	4	6	8
F0	F2	F4	F6	F8	F10	F12	F14				
					MULT2						







S1: ADDD F0, F2, F4

S2: MULTD F2 F6, F8

S3: MULTD F10, F0, F2

S4: ADDD F0, F12, F14

Exe: 8, 9, 10, 11

Name	Op	Vj	Vk	Qj	Qk	Etime			issue	Exec C	o. I	Nrite R.
mult1								addd	1		3	4
mult2	MULT	M(A1)	M(M1)			0		multd	2		6	7
add1								multd	3	1	11	
add2								addd	4		6	8
F0	F2	F4	F6	F8	F10	F12	F14					
					MULT2							





WAR Conflict

S1: ADDD F0, F2, F4

S2: MULTD F2, F6, F8

S3: MULTD F10, F0 F2 S4: ADDD F0 F12, F14









S1: ADDD F0, F2, F4

S2: MULTD F2, F6, F8

S3: MULTD F10, F0, F2

S4: ADDD F0 F12, F14

S4 can complete its exe but it MUST WAIT to WriteR

till \$3 reads the op

Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk	Εt	lst		Issue	Read Op	Exec Co.	Write R.
Mult1	NO											addd	1	2	4	5
mult2	YES	MULT	F10	F0	F2			YES	YES	4	S3	multd	2	3	7	8
Add1	YES	ADD2	F0	F12	F14			INO	NO	0	S4	multd	3	9		
Add2	NO											aaaa	р	1	9	
F0	F2	F4	F6	F8	F10	F12	F14									
ADD1					MULT2											







S1: ADDD F0, F2, F4

S2: MULTD F2, F6, F8

S3: MULTD F10, F0 F2

S4: ADDD F0 F12, F14

_																			
	Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk	Et	lst			Issue	Read Op	Exec Co.	Write R.	
	Mult1	NO												addd	1	2	4	5	5
	mult2	YES	MULT	F10	F0	F2			NO	NO	3	S3		multd	2	3	7	8	3
	Add1	NO								1				multd	3	9			
	Add2	NO												addd	9	7	9	10)
	F0	F2	F4	r6	F8	F10	F12	F14		Rj,	R	k u	pdate:	10					
						MULT2													
																			_

Si - Sj (i<j): WAR

MUST: Clk_EXE_ Sj < Clk_WRITE_Sj

If: Clk_READ_ Si < Clk_EXE_ Sj no prob at all</pre>

If: Clk_READ_ Si ≥ Clk_EXE_ Sj MUST BE: Clk_WRITE_ Sj > Clk_READ_ Si

(Clk_WRITE_ Sj = Clk_READ_ Si + 1)







S1: ADDD F0, F2, F4

S2: MULTD F2, F6, F8

F0 = M(A1) S3: MULTD F10, F0, F2 F0 ≠ F0

Thou ho

S4: ADDD F0, F12, F14

They have the same name, but they *ARE different*!!!

Name	Op	Vj	Vk	Qj	Qk	Etime			Issue	Exec Co.	Write R.
mult1	MULT	R(F6)	R(F8)			0		addd	1	3	4
mult2	MULT	M(A1)			MULT1			multd	2	6	
add1								multd	3		
add2	ADD	R(F12)	R(F14)			0		addd	4	6	
F0	F2	<u> 54</u>	F6	F8	F10	F12	F14				
ADD2	MULT1				MULT2						







S1: ADDD F0, F2, F4

S2: MULTD F2, F6, F8

S3: MULTD F10, F0, F2

F0 = M(A1)

Name	Op	Vj	Vk	Qj	Qk	Etime			Issue	Exec Co.	Write R.
mult1	MULT	R F6)	R(F8)			0		addd	1	3	4
mult2	MULT	M(A1)			MULT1			multd	2	6	
add1								multd	3		
add2								addd	4	6	7
F0	F2	F4	F6	F8	F10	F12	F14				
	MULT1				MULT2						



Tomasulo - loop

```
# include <s raio.h >
int main(void)

{
  int count;
  for (count = 1; count <= 500; count ++)
    print f("I will not throw paper dirplanes in class.");
  return 0;
}

MEND 10-3
```





Instruct	ion stati	<u>us</u>				Executi	o Write		
Instruct	ion <i>j</i>		K	iteration	Issue	comple	t (Result	,	Busy Address
LD F	0	0	R1	1	1			Load1	Yes 80
MULTIF	4	F0	F2	1	2			Load2	No
SD F	4	0	R1	1	3			Load3	No Qi
LD F	0	0	R1	2				Store1	Yes 80 Mult1
MULT F	4	F0	F2	2				Store2	No
SD F	4	0	R1	2		4455		Store3	No
Reserva	ation Sta	tio	ns		<i>S</i> 1	<i>S2</i>	RS for	RS for I	<u> </u>
7	ime Nan	пе	Busy	/ Op	Vj	Vk	Qj	Qk	Code:
	0 Add	1	No						LD F0 0 R1
	0 Add	2	No						MULTIF4 FO F2
	0 Add	3	No						SD F4 0 R1
	0 Mult	1	Yes	MULTD		R(F2)	Load1		SUBI R1 R1 #8
	0 Mult	2	No						BNEZ R1 Loop
Registe	r result s	sta	tus						
Clock	D1			F0	<i>F2</i>	F4	F6	F8	F10 F12 F30
3	80		Qi	Load1		Mult1			





Instruction status	<u>; </u>		Executio Write						
Instruction <i>j</i>	k iteration	Issue	complete	Result		Busy A	ddress		
LD FO 0	O R1 1	1			Load1	Yes	80		
MULT F4 F0) F2 1	2			Load2	No			
SD F4 0) R1 1	3			Load3	No	Qi		
LD FO 0	O R1 2				Store1	Yes	80 Mult1		
MULT F4 F0	O F2 2				Store2	No			
SD F4 0	O R1 2				Store3	No			
Reservation Station	S1	<i>S2</i>	RS for	RS for I	k				
Time Name	Busy Op	Vj	Vk	Qj	Qk	Code:			
0 Add1	No					LD F	0 0 R1		
0 Add2	No					MULT F	4 F0 F2		
0 Add3	No					SD F	4 0 R1		
0 Mult1	Yes MULTD		R(F2)	Load1		SUBI R	.1 R1 #8		
0 Mult2	No					BNEZ R	1 Loop		
Register result status									
Clock R1	F0	<i>F2</i>	F4	F6	F8	F10 F	F12 F30		
4 72	Qi Load1		Mult1						
LD F0 00 MULTIF4 F0 SD F4 00 Reservation Statio Time Name 0 Add1 0 Add2 0 Add3 0 Mult1 0 Mult2 Register result state Clock R1	OR1 2 OF2 2 OR1 2 ONS	S1 Vj	<i>Vk</i> R(F2) <i>F4</i>	Qj Load1	Store1 Store2 Store3 RS for k	Yes No No Code: LD F MULTIF SD F SUBI R BNEZ R	0 0 R1 4 F0 F2 4 0 R1 1 R1 #8 1 Loop		





Instruction	status				Executi	o Write					
Instruction	j	K	iteration	Issue	comple	t Result	_	Busy	Add	ress	
LD FO	0	R1	1	1			Load1	Yes	80		
MULT F4	FO	F2	1	2			Load2	No			
SD F4	0	R1	1	3			Load3	No		Qi	
LD FO	0	R1	2				Store1	Yes	80	Mult	:1
MULT F4	FO	F2	2				Store2	No			
SD F4	0	R1	2				Store3	No			
Reservation	n Statio	ns		<i>S</i> 1	<i>S2</i>	RS for	RS for I	k			
Time	Name	Busy	/ Op	Vj	Vk	Qj	Qk	Code:	•		
0	Add1	No						LD	FO	0	R1
0	Add2	No						MULT	F4	FO	F2
0	Add3	No						SD	F4	0	R1
0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1	#8
0	Mult2	No						BNEZ	R1	Loo	p
Register result status											
Clock	R1		F0	<i>F2</i>	F4	F6	F8	F10	F1.	ź	F30
5	72	Qi	Load1		Mult1						





Instruction s	status				Execution	o Write				
Instruction	j	K	iteration	Issue	complet	Result	_	Busy	Addr	ess
LD F0	0	R1	1	1			Load1	Yes	80	
MULT F4	FO	F2	1	2			Load2	Yes	72	
SD F4	0	R1	1	3			Load3	No		Qi
LD FO	0	R1	2	6			Store1	Yes	80	Mult1
MULT F4	FO	F2	2				Store2	No		
SD F4	0	R1	2				Store3	No		
Reservation Stations S1 S2 RS for RS for						RS for I	K			
Time	Name	Busy	[′] Ор	Vj	Vk	Qj	Qk	Code:		
0 /	Add1	No						LD	FO	0 R1
0 /	Add2	No						MULT	F4	FO F2
0	Add3	No						SD	F4	0 R1
0 1	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1 #8
0 1	Mult2	No						BNEZ	R1	Loop
Register result status										
Clock	R1		FO	<i>F2</i>	F4	F6	F8	F10	F12	F30
6	72	Qi	Load2		Mult1					







Questions





