POLITECNICO DI MILANO

High Performance Processors and Systems

Dynamic Scheduling

- Tomasulo loop -

Marco D. Santambrogio: marco.santambrogio@polimi.it

HPPS

The architecture

- 1 LOAD/STORE unit with latency equal to 1
- 2 MULT units with latency equal to 5
- 3 ADD/SUBD unit with latency equal to 2

- First load 8 clock cycles (cache miss)
- Followings 1 clock cycle (hit)
- **R1 = 10**

The code

```
Loop:    LD F2 0 R1
         ADDD F0 F2 F4
         MULTD F10 F0 F6
         ADDD F0 F12 F14
         SUBI R1 R1 #2
         BNEZ R1 Loop
```

Table

t = R1 =

Name	Op	Vj	Vk	Qj	Qk	Etime
mult1						
mult2						
add1						
add2						
add3						

	Busy	Addr
Load		

F0	F2	F4	F6	F10	F12

Solution table...

	Issue	Exec Co.	Write R.
LD			
ADDD			
MULTD			
ADDD			
LD			
ADDD			
MULTD			
ADDD			
LD			
ADDD			
MULTD			
ADDD			
LD			
ADDD			
MULTD			
ADDD			
LD			
ADDD			
MULTD			
ADDD			

A possible solution...

	Issue	Exec Co.	Write R.
LD	1	9	10
ADDD	2	12	14
MULTD	3	19	20
ADDD	4	6	7
LD	11	12	13
ADDD	12	15	16
MULTD	13	21	23
ADDD	14	16	17
LD	17	18	19
ADDD	18	21	22
MULTD	21	27	28
ADDD	22	24	25
LD	25	26	27
ADDD	26	29	30
MULTD	27	35	37
ADDD	28	30	31
LD	31	32	33
ADDD	32	35	36
MULTD	33	41	42
ADDD	34	36	38

Some considerations...

	Issue	Exec Co.	Write R.
LD	1	9	10
ADDD	2	12	14
MULTD	3	19	20
ADDD	4	6	7
LD	11	12	13
ADDD	12	15	16
MULTD	13	21	23
ADDD	14	16	17
LD	17	18	19
ADDD	18	21	22
MULTD	21	27	28
ADDD	22	24	25
LD	25	26	27
ADDD	26	29	30
MULTD	27	35	37
ADDD	28	30	31
LD	31	32	33
ADDD	32	35	36
MULTD	33	41	42
ADDD	34	36	38

LD F2 0 R1

ADDD F0 F2 F4

...

MULTD F10 F0 F6

ADDD F0 F2 F4

SUBI R1 R1 #2

BNEZ R1 Loop

ADDD F0 F12 F14

SUBI R1 R1 #2

BNEZ R1 Loop

LD F2 0 R1

....

Open issues...