Problem 1

Assume that two given architecture (CPU1 and CPU2) are able to execute the different classes of instructions reported in the following table. Assume a clock cycle equal to 2 ns for CPU1, while CPU2 is working at a clock frequency equal to 700 MHz.

Instruction Class	Frequency (%)	CPU1 (Cycles)	CPU2 (Cycles)
A	30	2	2
B	10	3	3
C	20	4	3
D	30	2	2
E	10	4	3

a) Determine the **average CPI** for each architecture

b) Which CPU is faster?

Assume that, thanks to a hardware optimization, CPU1 has now the following description:

- MISS Penalty = 6
- Memory stall ignored
- All the instruction can be executed with a CPI = 7.5

Assume that, the MISS RATE is equal to 13% and that the memory average access is equal to 3:

c) Compute the CPI for the new CPU1 with an ideal cache (100% hit)

d) Assume that no cache is available, determine the CPI for CPU1

Problem 2

Assume that a given 5 stage pipeline MIPS architecture is working with a clock cycle equal to 2 ns. Using the MIPS code shown below,

```
I1: lw $s2, 4($s0)
I2: lw $s1, 16($s0)
I3: sub $s4, $s1, 2
I4: add $s3, $s2, 1
```

a) Draw the pipeline schema showing all the RAW data conflicts.

Assuming that all the possible forwarding paths are introduced:

b) All the possible forwarding paths are introduced. Draw the pipeline schema showing all forwarding paths introduced.

Problem 2

Assume that a given 5 stage pipeline MIPS architecture is working with a clock cycle equal to 2 ns. Using the MIPS code shown below,

```
I1: add $s3, $s2, 2
I2: sub $s4, $s3, $s1
I3: add $s5, $s4, $s1
I4: lw $s6, 4($s4)
I5: sub $s7, $s4, $s6
```

a) Draw the pipeline schema showing all the RAW data conflicts.

b) All the possible forwarding paths are introduced. Draw the pipeline schema showing all forwarding paths introduced.

c) Reschedule the instructions to reduce the stalls; Draw the pipeline schema showing all the RAW data conflicts.

d) Starting from (c). All the possible forwarding paths are introduced. Draw the pipeline schema showing all forwarding paths introduced.