Problem 1

Assume that two given architecture (CPU1 and CPU2) are able to execute the different classes of instructions reported in the following table. Assume a clock cycle equal to 2 ns for CPU1, while CPU2 is working at a clock frequency equal to 700 MHz.

Instruction Class	Frequency (%)	CPU1 (Cycles)	CPU2 (Cycles)
A	30	2	2
B	10	3	3
C	20	4	3
D	30	2	2
E	10	4	3

a) Determine the **average CPI** for each architecture

b) Which CPU is faster?

Assume that, thanks to a hardware optimization, CPU1 has now the following description:

- MISS Penalty = 6
- Memory stall ignored
- All the instruction can be executed with a CPI = 7.5

Assume that, the MISS RATE is equal to 13% and that the memory average access is equal to 3:

c) Compute the CPI for the new CPU1 with an ideal cache (100% hit)

d) Assume that no cache is available, determine the CPI for CPU1

Solution 1:

a) Determine the **average CPI** for each architecture

CPI – CPU1 = 0.3*2 + 0.1*3 + 0.2*4 + 0.3*2 + 0.1*4 =
0.6+0.3+0.8+0.6+0.4=**2.7**

CPI – CPU2 = 0.3*2 + 0.1*3 + 0.2*3 + 0.3*2 + 0.1*3 =
0.6+0.3+0.6+0.6+0.3=**2.4**

b) Which CPU is faster?

Exe-CPU1 = (IC * CPI1)/Freq1

Exe-CPU2 = (IC * CPI2)/Freq2

Speedup = Exe-CPU1/Exe-CPU2 = ((IC * CPI1)/Freq1)*(Freq2/(IC * CPI2)) = (IC * CPI1 * Freq2)/(IC * CPI1 * Freq1) = (CPI1*Freq2)/(CPI1 * Freq1) = (2.7 * 700MHz)/(2.4 * 500MHz) = 1890/1200 = **1.575**

c) Compute the CPI for the new CPU1 with an ideal cache (100% hit)

MISS Penalty = 6
CPI_exe = 7.5
MISS RATE = 0.13
Riferimenti in memoria = 3

CPI_cache = CPI_exe + (Riferimenti * MISS_Penalty * MISS_RATE) = 7.5 + (3*0.13*6) = 7.5 + 2.34 = **9.84**

CPI_cache_ideale = **7.5**

d) Assume that no cache is available, determine the CPI for CPU1

CPI_senza_cache = 7.5 + (3*6) = 7.5 + 18 = **25.5**

Problem 2

Assume that a given 5 stage pipeline MIPS architecture is working with a clock cycle equal to 2 ns. Using the MIPS code shown below,

```
I1: lw $s2, 4($s0)
I2: lw $s1, 16($s0)
I3: sub $s4, $s1, 2
I4: add $s3, $s2, 1
```

a) Draw the pipeline schema showing all the RAW data conflicts.

Assuming that all the possible forwarding paths are introduced:

b) All the possible forwarding paths are introduced. Draw the pipeline schema showing all forwarding paths introduced.

Solution 2

	1	2	3	4	5	6	7	8	9	10	11
a.1)	I1	IF	ID	EXE	MEM	WB					
	I2		IF	ID	EXE	MEM	WB				
	I3			IF	ID	EXE	MEM	WB			
	I4				IF	ID	EXE	MEM	WB		
a.2)	I1	IF	ID	EXE	MEM	WB					
	I2		IF	ID	EXE	MEM	WB				
	I3			IF	O	O	ID	EXE	MEM	WB	
	I4						IF	ID	EXE	MEM	WB
b)	I1	IF	ID	EXE	MEM	WB					
	I2		IF	ID	EXE	MEM	WB				
	I3			IF	O	ID	EXE	MEM	WB		
	I4					IF	ID	EXE	MEM	WB	

Problem 3

Assume that a given 5 stage pipeline MIPS architecture is working with a clock cycle equal to 2 ns. Using the MIPS code shown below,

```
I1: add $s3, $s2, 2
I2: sub $s4, $s3, $s1
I3: add $s5, $s4, $s1
I4: lw $s6, 4($s4)
I5: sub $s7, $s4, $s6
```

a) Draw the pipeline schema showing all the RAW data conflicts.

b) All the possible forwarding paths are introduced. Draw the pipeline schema showing all forwarding paths introduced.

c) Reschedule the instructions to reduce the stalls; Draw the pipeline schema showing all the RAW data conflicts.

d) Starting from (c). All the possible forwarding paths are introduced. Draw the pipeline schema showing all forwarding paths introduced.

Solution 3

		1	2	3	4	5	6	7	8	9	10	11	12
a.1)	I1	IF	ID	EXE	MEM	WB							
	I2		IF	ID	EXE	MEM	WB						
	I3			IF	ID	EXE	MEM	WB					
	I4				IF	ID	EXE	MEM	WB				
	I5					IF	ID	EXE	MEM	WB			
a.2)	I1	IF	ID	EXE	MEM	WB							
	I2		IF	O	O	ID	EXE	MEM	WB				
	I3					IF	O	O	ID	EXE	MEM	WB	
	I4								IF	ID	EXE	MEM	WB
	I5									IF	O	O	ID
b)	I1	IF	ID	EXE	MEM	WB							
	I2		IF	ID	EXE	MEM	WB						
	I3			IF	ID	EXE	MEM	WB					
	I4				IF	ID	EXE	MEM	WB				
	I5					IF	O	ID	EXE	MEM	WB		
c.1)	I1	IF	ID	EXE	MEM	WB							
	I2		IF	ID	EXE	MEM	WB						
	I4			IF	ID	EXE	MEM	WB					
	I3				IF	ID	EXE	MEM	WB				
	I5					IF	ID	EXE	MEM	WB			
c.2)	I1	IF	ID	EXE	MEM	WB							
	I2		IF	O	O	ID	EXE	MEM	WB				
	I4					IF	O	O	ID	EXE	MEM	WB	
	I3								IF	ID	EXE	MEM	WB
	I5									IF	O	ID	EXE
d)	I1	IF	ID	EXE	MEM	WB							
	I2		IF	ID	EXE	MEM	WB						
	I4			IF	ID	EXE	MEM	WB					
	I3				IF	ID	EXE	MEM	WB				
	I5					IF	ID	EXE	MEM	WB			