EECS 151/251A FPGA Lab 3: Simulation, Button Parser

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1 Before You Start This Lab

Run `git pull` in `fpga_labs_sp20`.

We suggest that you look through these two documents that will help you better understand some Verilog constructs.

1. wire_vs_reg.pdf - The differences between wire and reg nets and when to use each of them.
2. always_at_blocks.pdf - Understanding the differences between the two types of always @ blocks and what they synthesize to.

Also, please note that we adopt the "No register inference" policy in this semester (refer to slide 18, Lec 4). Therefore, you should not write any sequential always blocks in your code. You should not need to use non-blocking assignments or reg nets for state elements. Instead, **please instantiate a REGISTER* module in lib/EECS151.v from our lab Github repository whenever you want to declare a register/state element**. This only applies to Verilog design file, but not necessarily to testbench code as we will see later.

In this lab, we cover Simulation using Vivado Design suite. We also learn how to design a Debouncer Circuit which can reliably sample button presses to provide control signals for our sequential digital circuits. Read the "What is Switch Bounce" section about why we need a debouncer circuit. Read the "Digital Switch Debouncing" section about the implementation of a debouncer circuit.

2 Simulation

In the previous lab, you have designed basic digital circuits and verified them on the PYNQ-Z1 board using the LEDs, buttons, and switches. However, that testing approach only works for small designs. Imagine you want to create a 100-bit adder or counter; the board clearly does not have enough IO for you to test your circuit. A more empirical way of verifying whether your circuit meets the functional specification is RTL simulation (or functional/behavioral simulation). To do that, we need a software simulator. There are many simulators out there including free, open-source ones as well as commercial products. In the past labs, we used ModelSim (from Mentor Graphics) or VCS (from Synopsys) which are available in our server. They generally require licenses if you want to use them outside of the lab machines. In this lab, we use Vivado simulator (xsim) as it is a

part of the Vivado Design suite software. If you have a Vivado WebPACK installed in your laptop, you should be able to use xsim too. You might also be interested to learn about other open-source simulators such as Verilator or Icarus Verilog (IVerilog). xsim is recommended for the FPGA labs, but feel free to take advantage of any simulation software you like or are familiar with.

Besides a simulator software, you will need to write your own testbench in Verilog. The testbench instantiates the module you want to test (say, your 100-bit adder, or we often refer to it as "DUT" – design-under-test), and provides stimuli (e.g., test cases) to your DUT. Your job is to check if the output of your DUT matches your expectation. You can either print out the output values or dump a waveform file that can be opened by a waveform viewer software. xsim has its own waveform viewer, so you don't have to worry about installing another tool. If you are looking for free tool, GTKWave is decent and able to support the output waveform generated by Verilator/IVerilog/VCS.

Let's do some lab exercises to see how it actually works.

3 Simulating Your 32-bit Structural Adder

Reuse the structural adder code you did in Lab 2. You need to parameterize your adder so that it can support arbitrary bitwidth. Update the files `lab3/src/full_adder.v`, `lab3/src/structural_adder.v` with your own code. A testbench code has been provided to you.

Create a new Vivado project (or reuse existing project). Add the following files to your project: `lab3/src/structural_adder.v`, `lab3/src/full_adder.v`. Add the testbench file to your project (make sure to select *Add or create simulation sources* when you add it): `lab3/sim/structural_adder_tb.v`. Let's take a look at the testbench code.

```
`timescale 1ns/1ns
```

The timescale declaration needs to be at the top of every testbench file.

The first argument to the timescale declaration is the simulation step time. It defines the granularity of discrete time units in which the simulation advances. In this case, we have defined the simulation step time to be one nanosecond, so we can advance the simulation time by as little as 1ns at a time.

The second argument to the timescale declaration is the simulation resolution. In our example it is also 1ns. The resolution allows the simulator to model transient behavior of your circuit in between simulation time steps. For this lab, we aren't modeling any gate delays, so the resolution can safely equal the step time.

```
module structural_adder_tb();
```

Next, we have a Verilog module `structural_adder_tb` that does not have any input or output signal, as it is not meant for being synthesized to a bitstream. Simulation is a totally separate step from what we have learned in the previous lab which we have a tool flow from *Synthesis* → *Implementation* → *Generate Bitstream*; the testbench code does not necessarily go through the flow.

```
reg clock;
initial clock = 0;
```

```
always #(4) clock <= ~clock;
```

This is the clock generation code. The clock signal needs to be generated in our testbench so it can be fed to the DUT. The initial statement sets the value of the clock net to 0 at the very start of the simulation. The next line toggles the clock signal every 4ns, i.e. half period of 125 MHz clock.

```
reg [N-1:0] operand1, operand2;
wire [N:0]  adder_output;
```

Here are the inputs and output of our `structural_adder`. Notice that the inputs to the `structural_adder` are declared as `reg` type nets and the outputs are declared as `wire` type net. This is because we will be driving the inputs in our testbench inside an `initial` block and we will be reading the output.

A parameterized 32-bit structural adder is instantiated in the testbench module. This is the "design-under-test" module. We assign the input and output signals to our DUT.

```
module structural_adder #(32) dut(
  .a(operand1),
  .b(operand2),
  .sum(adder_output)
);
```

You could instantiate multiple modules for testing in a single testbench, but it is generally recommended to have a separate, small testbench for each DUT to not overload yourself with many debug information to keep track of, and also to catch easier bugs. Once you are done with making sure individual modules work properly, you can go up to the next design hierarchy to test their integration. We will see that in later lab exercises and project.

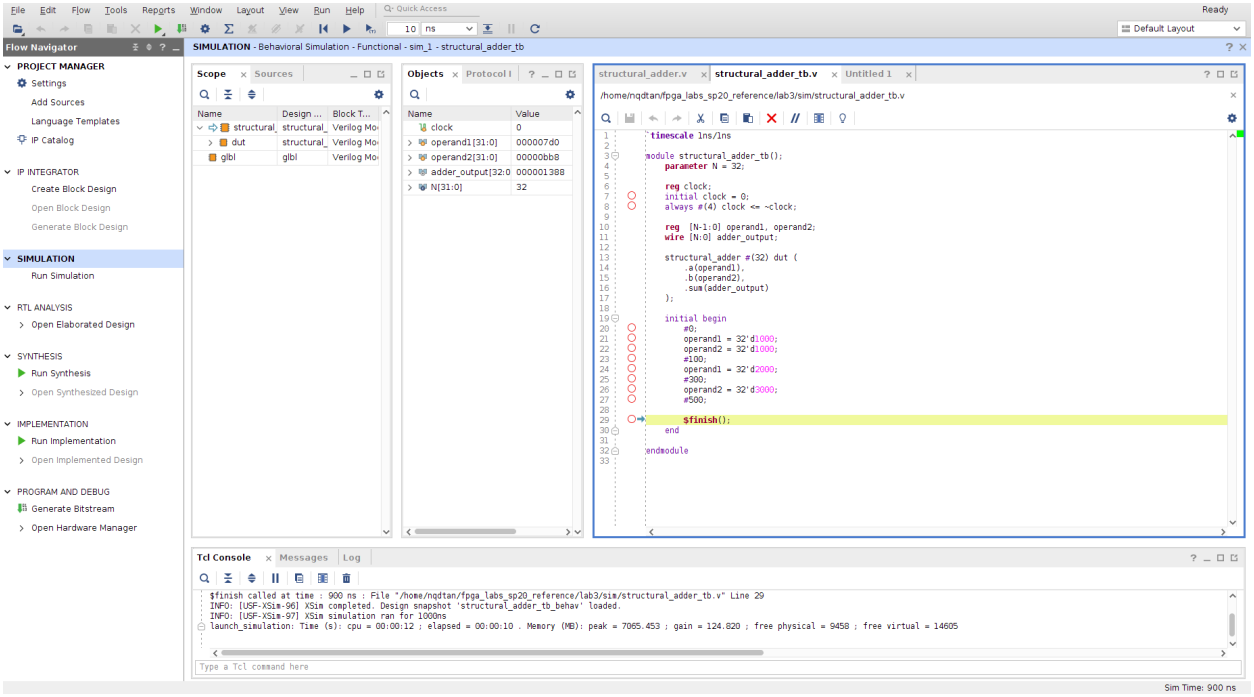
```
initial begin
    #0;                  // at the start of simulation
    operand1 = 32'd1000; // (1)
    operand2 = 32'd1000; // (2)
    #100;                // forward time by 100ns
    operand1 = 32'd2000; // (3)
    #300;                // forward time by 300ns
    operand2 = 32'd3000; // (4)
    #500;                // forward time by 500ns

    $finish();
end
```

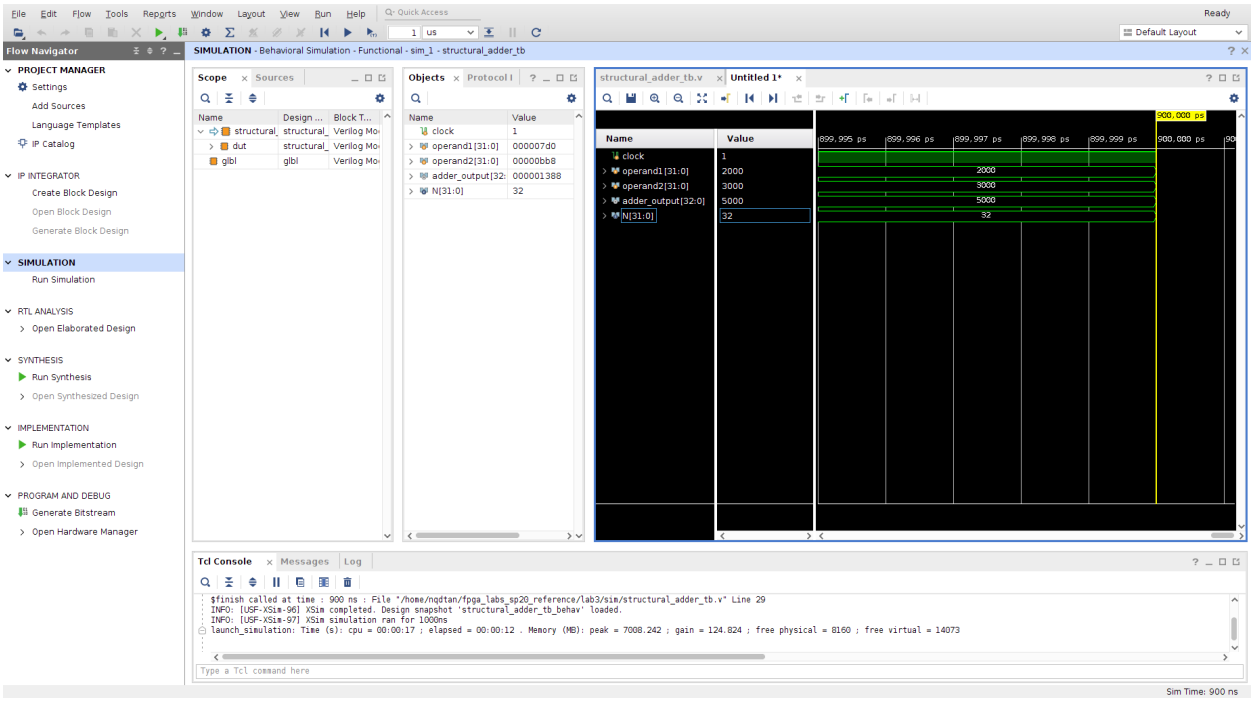
In this initial block, you assign some values to the inputs of your DUT. Think of those assignments as events as they happen at specific timestamps. For example, (1) and (2) happen at the start of the simulation, (3) happens at 100ns from the start, and (4) happens at 400ns from the start. The statement `#X;` tells the simulator to advance the simulation by `X` $\times$ simulation step time. The keyword `$finish()` tells the simulator to exit the simulation. In our example, the simulation finishes after 900ns.

Let's run our first simulation to understand what it means. In the *Flow Navigator*, click *Simulation*

→ *Run Simulation*. Make sure to choose *Run Behavioral Simulation*. Vivado will compile your Verilog code and launch the simulator. By default, Vivado simulation automatically runs until it hits `$finish()`. You will see that it stops at the statement `$finish();` in the testbench.

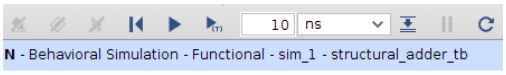


Go to the waveform tab (*Untitled 1*) to observe the waveform. Check the timings of those assignments as well as the values of `adder_output` signal to see if they make sense to you. The simulation should stop at 900ns. By default, the multi-bit signals such as `operand1`, `operand2`, `adder_output` are displayed in hex format. You can convert them to decimal format by selecting those signals, then right click → *Radix* → *Unsigned Decimal*. You should expect to see something as follows.



Spend some time to explore the functions of the buttons in the waveform window. Things like *Next Transition* or *Previous Transition* along with *Markers* are helpful when you want to track the transitions of your signals. You can do `Ctrl +` your mouse wheel to zoom in/out part of the waveform. Click *Zoom Fit* to see the entire waveform from the start to the end.

Next, we explore the functions of the simulation buttons (right under Vivado top menu bar). Click *Restart* button (or `Ctrl + Shift + F5`) to restart your simulation. You will see that all the signals are in 'X' state (uninitialized). Click *Run All* button (or `F3`) to run the simulation. This will run the simulation until finish. The tool also provides an option to run the simulation for some amount of time that you want (click *Run for ...* or `Shift + F2`). There's also a debug breakpoint capability which we won't cover here.



Try changing a few things in the initial block of your testbench. After making changes to the code, you can relaunch the simulation by clicking the *Relaunch simulation* button.

You can also save your waveform (`Ctrl + S`) before exiting Simulation or Vivado to retain the configuration (such as Decimal radix) for next time you open it up.

3.1 Questions

1. The adder output is updated immediately with the inputs. This is because our adder circuit is a combinational circuit. Modify the structural adder so that the adder output is updated at every clock edge. Remember to use a REGISTER module from the EECS151.v library.

Run the simulation again to see if your `adder_output` signal now is synchronous with the clock signal (remember to also wire the clock signal to your DUT). Screenshot the waveform and submit it to the lab report (pick a region of the waveform which the output transition w.r.t clock signal can be observed clearly).

2. Instead of manually setting the values of `operand1` and `operand2` in the initial block, modify the testbench to provide test vectors of 10 values for `operand1` and `operand2`. You can define arbitrary values for your test vectors. A test vector can be an array of wires or regs (or integer) with pre-defined values. Drive each value in the test vectors per clock cycle to your DUT. You can write some sequential always block(s) for this task. Submit the modified testbench and a screenshot of your waveform to the lab report.

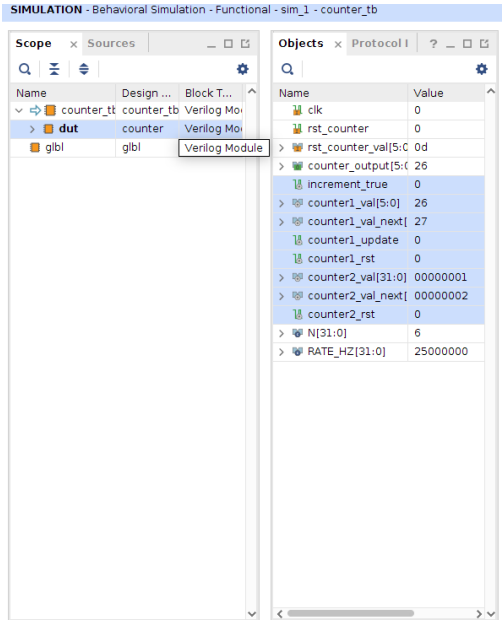
You can also have multiple `initial` blocks in your testbench code. They will run at the same time from the start to the end.

If you are unsure or confused about any of the steps above, don't hesitate to discuss with a TA.

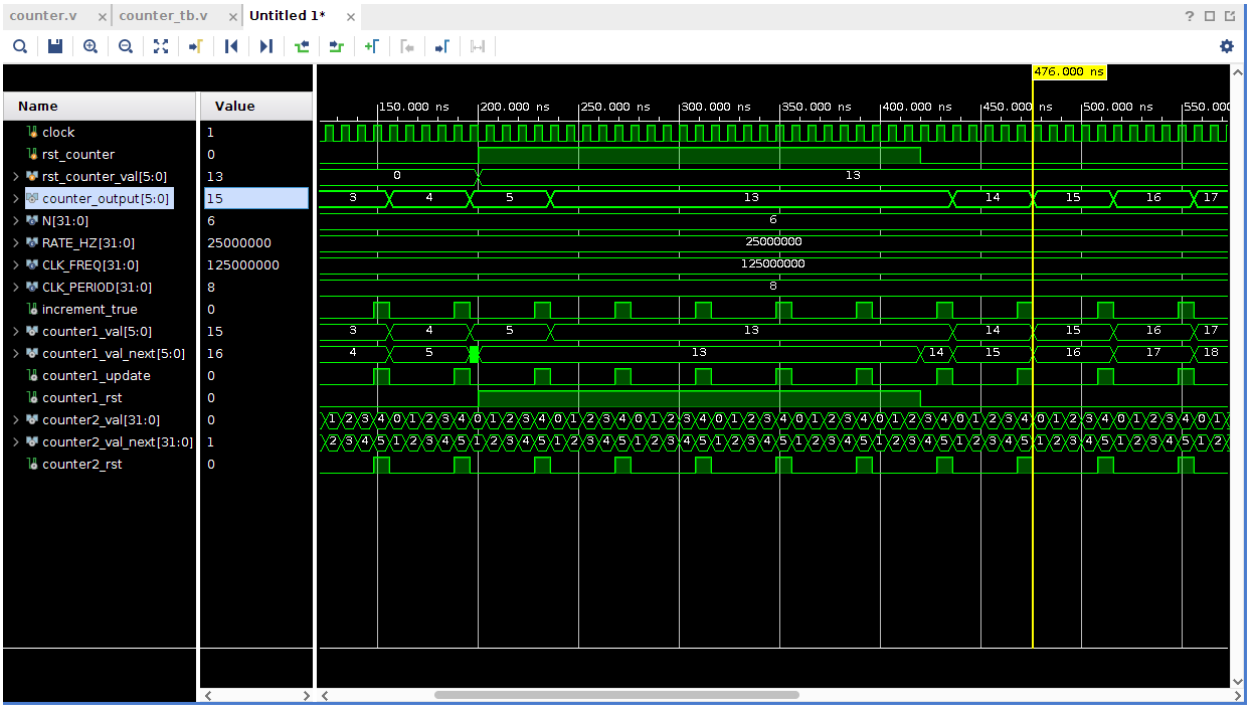
4 Simulating Your Counter

Reuse the counter code you did in Lab 2. You need to parameterize the bitwidth of your counter as well as the update rate (it was 1 second, or 1 Hz in the previous lab). You can assume that the update rate is a factor of 125 MHz. In addition, your counter has two inputs: `rst_counter` which resets the counter when HIGH, and `rst_counter_val` which is the reset value. Update the files `lab3/src/counter.v` with your own code. Please use REGISTER* modules declared in the EECS151 library file (`lib/EECS151.v`). A testbench code has been provided to you with a 6-bit counter with a rate of 25 MHz. Run the simulation and observe the waveform to check if the behavior of your counter is correct.

You can also add the signals in your DUT module (or any sub-module) to the waveform viewer as in the following example. Select the sub-module under *Scope* tab, then select the signals of interest under *Objects* tab, right click → *Add to Wave Window*.



Restart and *Run all* the simulation after adding new signals to the Wave window. You should expect to see your waveform similar to this.



Feel free to change the `(N, RATE_HZ)` parameters to test different configurations of your counter.

4.1 Questions

1. Screenshot your parameterized counter code to the lab report.

5 Additional Testbench Techniques

- `@(posedge <signal>)` and `@(negedge <signal>)` - These are a different type of delay statement from what you have seen before. `#10` would advance the simulation by 10 timesteps. These commands will advance the simulation until the `<signal>` rises or falls.

  For example:

  ```
  @(posedge signal);
  @(posedge signal);
  ```

  Simulation time will advance until we have seen two rising edges of `signal`.

- `repeat` - it acts like a `for` loop but without an increment variable

  For example:

  ```
  repeat (2) @(negedge clk);
  repeat (10) begin
    @(posedge clk);
  end
  ```

  The simulation will advance until we have seen 2 falling clock edges and will then advance further until we have seen 10 rising clock edges.

- `$display` - acts as a print statement. Similar to languages like C, if you want to print out a wire, reg, integer, etc... value in your testbench, you will need to format the string. It works like `printf()` in C. It is a great debug method if you are not a fan of waveform.

  For example:

  ```
  $display("Wire x in decimal is %d", x);
  $display("Wire x in binary is %b", x);
  // You can even print out the current simulation time
  $display("Time %d", $time);
  ```

- `tasks` - tasks are subroutines where you can group and organize some commands rather than haphazardly putting them everywhere. They can take inputs and assign outputs.

  ```
  task wait_for_n_clocks();
  input [7:0] num_edges;
  begin
    repeat (num_edges) @(posedge clk);
  end
  endtask
  ```

- `fork/join` - Allows you to execute testbench code in parallel. You create a fork block with the keyword `fork` and end the block with the keyword `join`.

For example:

```
fork
  begin
    task1();
  end
  begin
    $display("Another thread");
    task2();
  end
join
```

Multiple threads of execution are created by putting multiple begin/end blocks in the fork-join block. In this example, thread 1 runs `task1()`, while thread 2 first `$display`s some text then runs `task2()`. The threads operate in parallel.

- Hierarchical Paths - you can access signals inside an instantiated module for debugging purposes. This can be helpful in some cases where you want to look at an internal signal but don't want to create another output port just for debug.

  For example:

```
$display("counter2_val: %d", dut.counter2_val);
$display("counter2_reg_q: %d", dut.counter2_reg.q);
```

As a general tip, you don't have to create separate projects for different Vivado simulations. You can add all the source files and testbench files to a single project. You need to set which one is the top-level module for *Simulation*. In the *Sources* pane, under *Simulation Sources*, right click on the testbench file of the DUT you want to test and choose *Set as top*.

6 Input Conditioning Circuits

To safely use the button signals on the PYNQ board with respect to clock signal of our circuits, we have to design input conditioning circuits to handle metastability and button bounce. Check the prelab reading on Debouncer circuit 1 if you have not done so.

6.1 Synchronizer

In Verilog (RTL), digital signals are either 0's or 1's. In a digital circuit, a 0 or 1 corresponds to a low or high voltage. If the circuit is well designed and timed (fully synchronous), we only have to worry about the low and high voltage states.

The signals coming from the push buttons and slide switches on the PYNQ board don't have an associated clock (asynchronous). When the button signals are put through a register, its hold or setup time may be violated. This may put that register into a *metastable* state (Figure 1).

An asynchronous signal could violate timing constraints, and cause a 'mid-rail' voltage from a

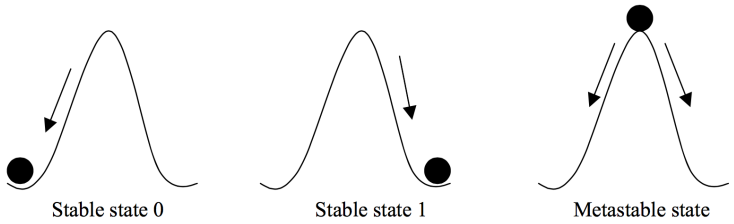


Figure 1: The 'ball on a hill' metaphor for metastability. If a register's timing constraints are violated, its output voltage oscillates and after some time unpredictably settles to a stable state.

register to propagate to other logic elements. This can cause catastrophic timing violations that the tools never saw coming.

We will implement a synchronizer circuit that will safely bring an asynchronous signal into a synchronous circuit. The synchronizer needs to have a very small probability of allowing metastability to propagate into our synchronous circuit.

This synchronizer circuit for this lab is relatively simple (Figure 2). For synchronizing one bit, it is a pair of flip-flops connected serially.

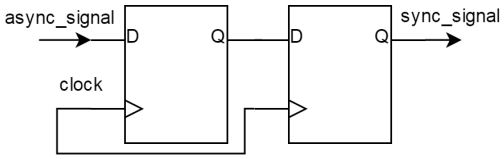


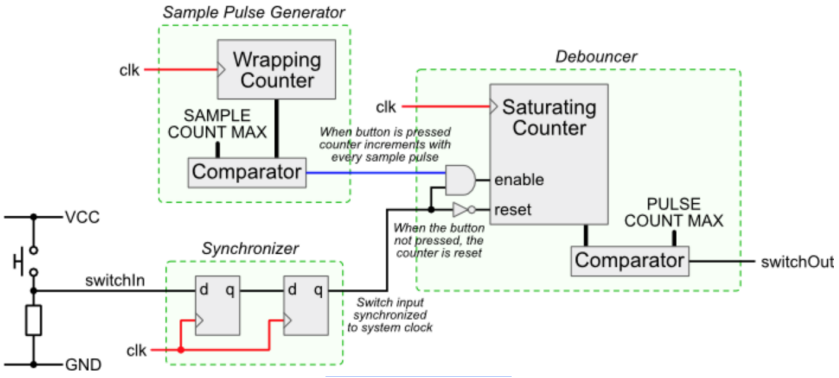
Figure 2: 1-bit 2 Flip-Flop Synchronizer

Edit `lab3/src/synchronizer.v` to implement the two flip-flop synchronizer. This module is parameterized by a `width` parameter which controls the number of one-bit signals to synchronize.

6.1.1 Synchronizer Simulation

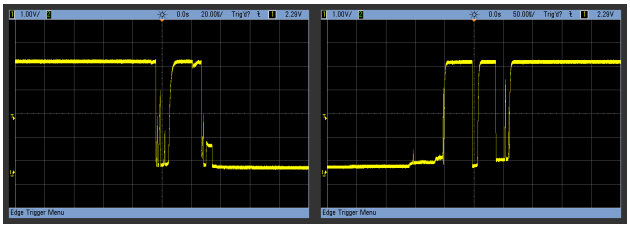
A testbench is provided in `lab3/sim/sync_tb.v`. Run it using Vivado simulation.

6.2 Debouncer



Recall this graphic from the prelab debouncer reading.

The debouncer circuit takes a button's glitchy digital signal and outputs a clean signal indicating a single button press. The reason we need a circuit for this can be seen in the figure below.



When we press or depress a button, the signal doesn't behave like a perfect step function. Instead the button signal is glitchy due to mechanical "bounce". If we naively used the button signal directly there would be many spurious "button presses".

Look at `lab3/src/debouncer.v`. This is a parameterized debouncer which can debounce `width` signals at a time. The other parameters reference the constants used in the circuit from the prelab reading.

The debouncer consists of:

1. **Sample Pulse Generator** - Tells our saturating counter when to sample the input signal. It should output a 1, every `sample_count_max` clock cycles. By default `sample_count_max` is set to 25000.

2. **Saturating Counter** - This is a counter that counts up to `pulse_count_max`. If the sample pulse is high at a clock edge, increment the counter if the input signal is also high, else reset the counter to 0. Once the saturating counter reaches `pulse_count_max`, it should hold that value indefinitely until the sampled input signal becomes 0. The `debounced_signal` of your debouncer should be an equality check between the saturating counter and `pulse_count_max`.

You can use the same sample pulse generator for all input signals into your `debouncer`, but you should have a separate saturating counter per input signal.

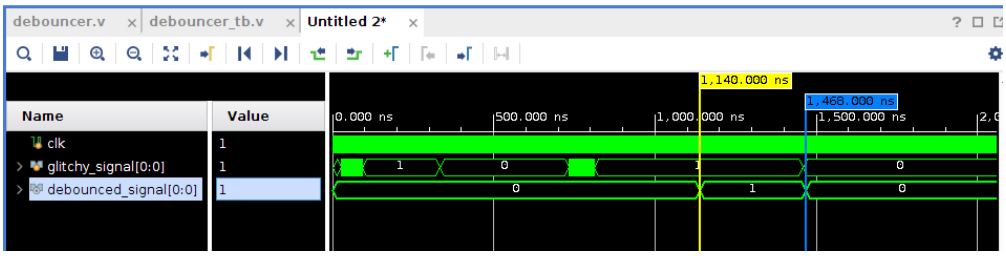
6.2.1 Debouncer Simulation

A testbench has been provided in `lab3/sim/debouncer_tb.v`. Make sure you understand what the testbench is doing. Run it as usual.

The debouncer testbench has 2 tests:

1. Verifies that if a glitchy signal initially bounces and then stays high for **less** than the saturation time, that the debouncer output never goes high.
2. Verifies that if a glitchy signal initially bounces and then stays high for **more** than the saturation time, that the debouncer goes high and stays high until the glitchy signal goes low.

You should expect to see a waveform similar to this. Pay attention to the printouts in the *TCL Console* to see if tests are passed or failed.



6.3 Edge Detector

The debouncer will act to *smooth-out* the button press signal. It is then followed up with an edge detector that can take the low-to-high transition of the debouncer output and use it to generate a 1 clock cycle wide pulse that the rest of our digital design can use.

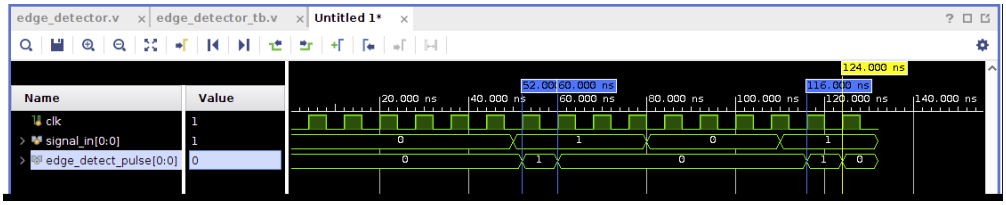
Create a parameterized-width edge detector in `lab3/src/edge_detector.v`.

6.3.1 Edge Detector Simulation

A testbench is provided in `edge_detector_testbench.v`. Run as usual.

The edge detector testbench tests 2 scenarios, when the `signal_in` transitions from low-to-high twice. At each time, the `edge_detect_pulse` goes high at the next clock edge and stays high for one cycle.

You should expect to see a waveform similar to this. Pay attention to the printouts in the *TCL Console* to see if tests are passed or failed.



6.4 Button Parser on the FPGA

In this section, we use the buttons on the PYNQ board to provide various control signals to our digital circuits.

6.4.1 Static Counter with with Button Parser

Look at `src/button_parser.v` which combines the synchronizer, debouncer, and edge detector in a chain. Create a Vivado project. Add these files `lab3/src/synchronizer.v`, `lab3/src/debouncer.v`, `lab3/src/edge_detector.v`, `lab3/src/button_parser.v`, `lab3/src/z1top_static_counter.v`, and `lab3/constraints/pynq-z1.xdc`. Set `z1top_static_counter` as the top-level module. Generate a bitstream and test this circuit on the PYNQ board. Check that each button performs the right action as written in the code.

6.4.2 Rate Counter with with Button Parser

Create a Vivado project. Add these files `lab3/src/synchronizer.v`, `lab3/src/debouncer.v`, `lab3/src/edge_detector.v`, `lab3/src/button_parser.v`, `lab3/src/z1top_rate_counter.v`, and `lab3/constraints/pynq-z1.xdc`.

You should make some change to the file `lab3/src/z1top_rate_counter.v` to implement a 4-bit counter that counts up with a rate of 1 Hz. You can reuse your code in previous lab exercises. For this exercise, we add new features to our counter such that:

1. `BUTTON[0]` increases the rate of the counter.
2. `BUTTON[1]` decreases the rate of the counter.
3. `BUTTON[2]` pauses/resumes the counter. When a counter is paused, the rate cannot be changed.
4. `BUTTON[3]` resets the counter and the rate to the original value. The counter operates normally after reset.

You can decide how much you want to add or subtract the rate as long as the rate changes of the LEDs are recognizable.

7 Lab Deliverables (due: 11.59PM, Feb 13th, 2020)

7.1 Lab Checkoff

To checkoff for this lab, have these things ready to show the TA:

1. Demonstrate a working static counter with button parser.
2. Demonstrate a working rate counter with button parser.

7.2 Lab Report

Please submit a short report to Gradescope with the following items.

1. Your answers to the questions 3.1 and 4.1.
2. Your code for `lab3/src/z1top_rate_counter.v`, `lab3/src/debouncer.v`, `lab3/src/edge_detector.v`, `lab3/src/synchronizer.v`.

A Local Dev Setup

Besides Vivado, we'll cover installing free tools for simulation for each OS here so you can have more options to do your lab/homework exercises.

A.1 Linux/OSX

1. Add vivado to your `$PATH` by adding this in your `.bashrc`:

   ```
   export PATH="/opt/Xilinx/Vivado/2019.1/bin:$PATH"
   ```

2. Install Icarus Verilog
   - Linux: `sudo apt install iverilog`
   - OSX: `brew install icarus-verilog`
3. Install Verilator
   - Linux: `sudo apt install verilator`
4. Install gtkwave
   - Linux: `sudo apt install gtkwave`
   - OSX: Download the app

In a terminal you should be able to successfully run `vivado`, `iverilog`, `gtkwave`.

A.1.1 Sharing PYNQ USB Device from OSX to Linux VM

TODO add screenshots

A.2 Windows

Windows packages for Icarus are available. You should be able to download the appropriate .exe for your machine. Gtkwave can be installed along with Icarus (just make sure you check the box for it). Lastly, here is a link to install Cygwin. When you install Cygwin, you need to check the boxes for make and git as shown in Fig. 3, and also Python 3.6.

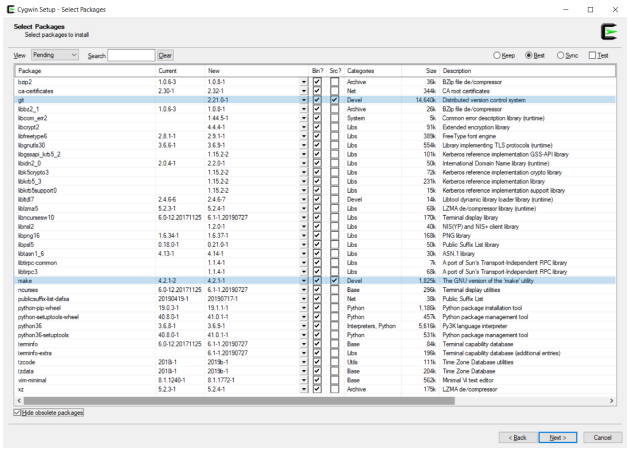


Figure 3: Check make and git with your cygwin install!

After installing Icarus, gtkwave, and cygwin, you'll need add Vivado, Icarus, and gtkwave to your Windows PATH with the below steps.

- Go the windows control panel and find the "Edit the system variables menu". Alternatively, if you just search for "system variables", the menu should pop up.
- Click the "Environment Variables" button near the window's bottom right corner (Fig. 4).
- Double click the "Path" variable in the user variables dialog (Fig. 5).
- Click the next empty row and paste the path of the appropriate program (Fig. 6). Hit okay and you're done!

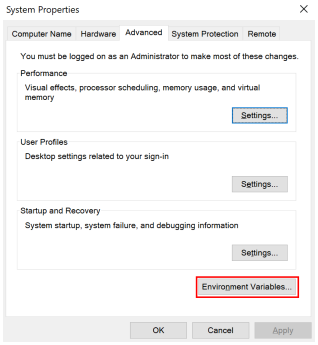


Figure 4: The System variables dialogue.

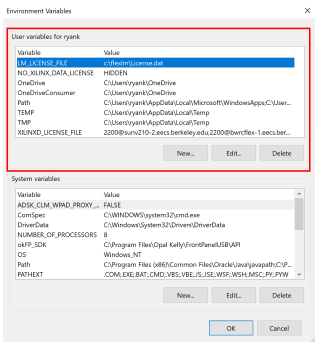


Figure 5: Environment variables dialogue.

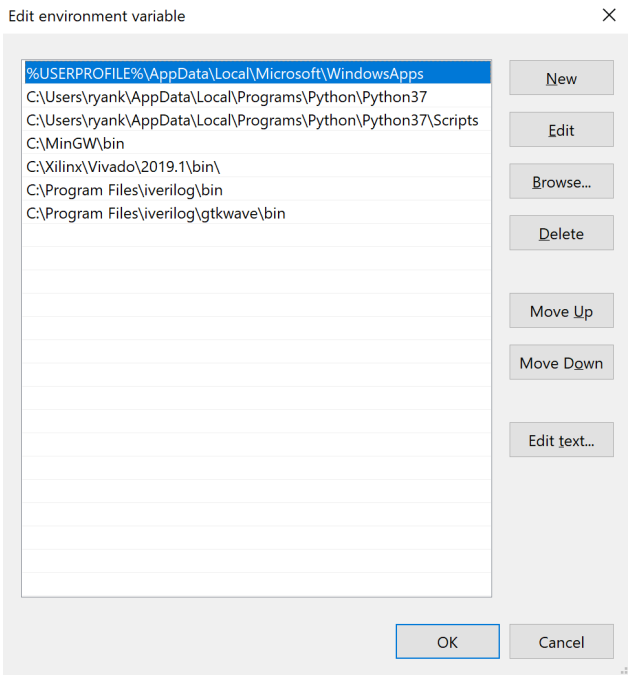


Figure 6: Adding programs to your PATH.

Ackowlegement

This lab is the result of the work of many EECS151/251 GSIs over the years including:

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