MSB of RAM BANK LATCH is ROMSW.
PLD enables ROM (ROMEN = 0) when ROMSW = 0.
PLD disables ROM (ROMEN = 1) when ROMSW = 1.

RAM banks are driven by the lower 6 bits giving 63 x 8k banks
ROMSEL (bit 6) selects between the lower and upper 32k of ROM

```
DEFAULT MEMORY ADDRESS MAP:
============================
0x0000  -- FIXED RAM START / ZEROPAGE
0x0100  -- STACK
------------------------------------------------------
0x0200  -- FIXED RAM START
0xBEFF  -- FIXED RAM END
------------------------------------------------------
0xBF00  -- IO - BANK LATCH (MSB = ROM SWITCH) (banks 0-63)
0xBF10  -- IO - ACIA / UART
0xBF20  -- IO - VIA1 / SPI / Some IO
0xBF30  -- IO - VIA2 / Peripheral IO
0xBF40  -- IO - VDP / TMS9918A Clone
0xBF50  -- IO - JSEN / Joy Stick
0xBF60  -- IO - SNEN / SN76489
0xBF..  -- RESERVED IO / Unused.
------------------------------------------------------
0xC000  -- HIGH / BANKED RAM / 64 x 8kb banks ram
------------------------------------------------------
0xE000  -- ROM / 8KB rom
0xFFFA  -- VECTORS / HW vectors
0xFFFF  -- END OF ALL MEMORY
```

RESET SUPERVISOR

JOYSTICK

SYSTEM CLOCK

CPU

ROM

LOW RAM

BANKED RAM

BUS & IRQ

MEMORY BANK LATCH

SDCARD

SPI BUS

GPIO

UART CLOCK

USER LED

SPI BUS
SN76489 PSG

GPIO VIA

UART

VDP / PICO9918

https://www.github.com/6502-retro/

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