

**DALLAS**  
SEMICONDUCTOR

**DS1216B**  
SmartWatch/RAM 16K/64K

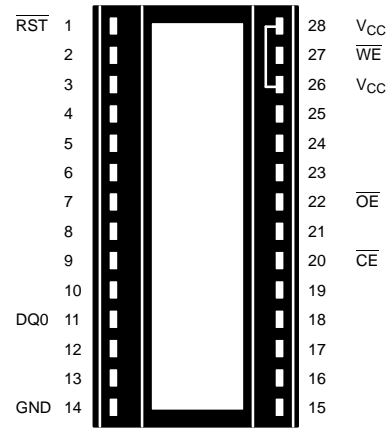
## FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 2K x 8 and 8K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month; leap year compensation valid up to 2100
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Proven gas-tight socket contacts
- Full  $\pm 10\%$  operating range
- Operating temperature range  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$
- Accuracy is better than  $\pm 1$  min./month @  $25^{\circ}\text{C}$

## DESCRIPTION

The DS1216B SmartWatch/RAM 16/64K is a 28-pin, 600 MIL wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either 24-pin 2K x 8 or 28-pin 8K x 8 JEDEC byte-wide CMOS static RAM. When the socket is mated with a CMOS SRAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM. The SmartWatch monitors  $V_{CC}$

## PIN ASSIGNMENT



28-PIN INTELLIGENT SOCKET

## PIN DESCRIPTION

All Pins Pass Through Except 20, 26, 28

Pin 1	$\overline{\text{RST}}$	– Reset
Pin 11	DQ0	– Data Input/Output 0
Pin 14	GND	– Ground
Pin 20	$\overline{\text{CE}}$	– Conditioned Chip Enable
Pin 22	$\overline{\text{OE}}$	– Output Enable
Pin 26	$V_{CC}$	– Switched $V_{CC}$ for 24-Pin RAM
Pin 27	$\overline{\text{WE}}$	– Write Enable
Pin 28	$V_{CC}$	– Switched $V_{CC}$ for 28-Pin RAM

for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent loss of watch and RAM data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated RAM take up no more area than the memory alone. The SmartWatch uses pins 28, 27, 26, 22, 20, 11, and 1 for RAM and watch control. All other pins are passed straight through to the socket receptacle.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

OPERATION

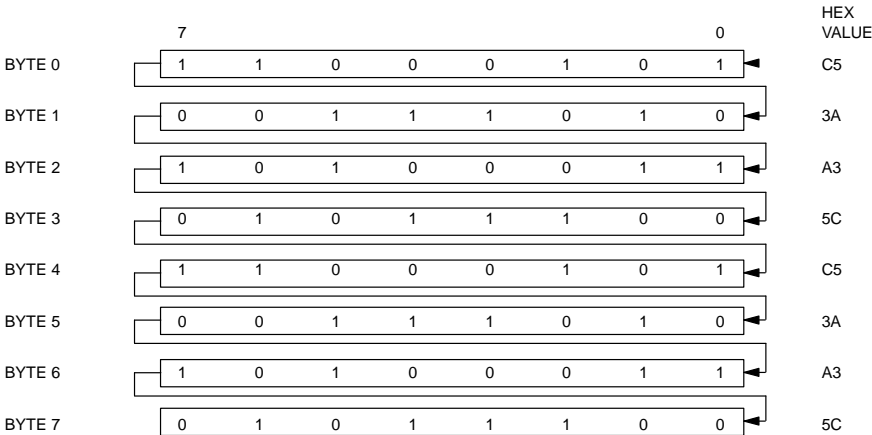
Communication with the SmartWatch is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the SmartWatch, and memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable ( $\overline{CE}$ ), Output Enable ( $\overline{OE}$ ), and Write Enable ( $\overline{WE}$ ). Initially, a read cycle to any memory location using the  $\overline{CE}$  and  $\overline{OE}$  control of the SmartWatch starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the  $\overline{CE}$  and

$\overline{WE}$  control of the SmartWatch. These 64 write cycles are used only to gain access to the SmartWatch. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the SmartWatch are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a SmartWatch scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the SmartWatch to either receive or transmit data on DQ0, depending on the level of the  $\overline{OE}$  pin or the  $\overline{WE}$  pin. Cycles to other locations outside the memory block can be interleaved with  $\overline{CE}$  cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1



NOTE:

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the SmartWatch is less than 1 in 10<sup>19</sup>. This pattern is sent to the SmartWatch LSB to MSB.

## NONVOLATILE CONTROLLER OPERATION

The DS1216B SmartWatch performs circuit functions required to make a CMOS RAM nonvolatile. First, a switch is provided to direct power from the battery or  $V_{CC}$  supply, depending on which voltage is greater. This switch has a voltage drop of less than 0.2 volts. The second function which the SmartWatch provides is power-fail detection. Power-fail detection occurs at  $V_{TP}$ . The DS1216B constantly monitors the  $V_{CC}$  supply. When  $V_{CC}$  goes out of tolerance, a comparator outputs a power-fail signal to the chip enable logic. The third function accomplishes write protection by holding the chip enable signal to the memory within 0.2 volts of  $V_{CC}$  or battery. During nominal power supply conditions the memory chip enable signal will track the chip enable signal sent to the socket with a maximum propagation delay of 20 ns.

## FRESHNESS SEAL

Each DS1216B is shipped from Dallas Semiconductor with its lithium energy source disconnected, insuring full energy capacity. When  $V_{CC}$  is first applied at a level greater than the lithium energy source is enabled for battery backup operation.

## SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in eight registers of eight bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each register must be handled in groups of eight bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch register is in binary coded decimal format (BCD). Reading and writing the

registers is always accomplished by stepping through all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

## AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours).

## OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the  $\overline{\text{RESET}}$  and oscillator functions. Bit 4 controls the  $\overline{\text{RESET}}$  (pin 1). When the  $\overline{\text{RESET}}$  bit is set to logic 1, the  $\overline{\text{RESET}}$  input pin is ignored. When the  $\overline{\text{RESET}}$  bit is set to logic 0, a low input on the  $\overline{\text{RESET}}$  pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

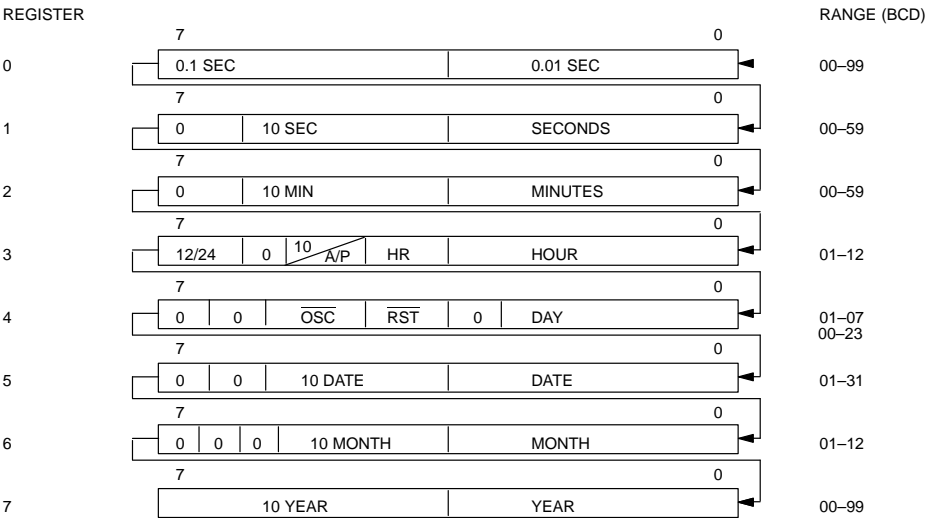
## ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

## ADDITIONAL INFORMATION

Please see Application Notes 4 and 52 for information regarding optional modifications and utilization of the Phantom Clock contained within the SmartWatch.

SMARTWATCH REGISTER DEFINITION Figure 2



**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground

–0.3V to +7.0V

Operating Temperature

0°C to 70°C

Storage Temperature

–40°C to +70°C

Soldering Temperature

260°C for 10 seconds (See Note 6)

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26L, PIN 28L Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	1, 3
Logic 1	$V_{IH}$	2.2		$V_{CC} + 0.3$	V	1, 10
Logic 0	$V_{IL}$	–0.3		+0.8	V	1, 10

**DC ELECTRICAL CHARACTERISTICS**(0°C to 70°C;  $V_{CC}=4.5$  to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26L, PIN 28L Supply	$I_{CCI}$			5	mA	3, 4, 5
PIN 26U, PIN 28U Supply Voltage	$V_{CCO}$	$V_{CC}-0.2$			V	3, 8
PIN 26U, PIN 28U Supply Current	$I_{CCO}$			80	mA	3, 8
Input Leakage	$I_{IL}$	–1.0		+1.0	$\mu$ A	4,10,13
Output @ 2.4V	$I_{OH}$	–1.0			mA	2
Output @ 0.4V	$I_{OL}$			4.0	mA	2
Write Protection Voltage	$V_{TP}$	4.25		4.5	V	

(0°C to 70°C;  $V_{CC} < 4.5V$ )

PIN 20U Output	$V_{OHL}$	$V_{CC}-0.2$ $V_{BAT}-0.2$			V	3
PIN 26U, PIN 28U Battery Current	$I_{BAT}$			1	$\mu$ A	3
PIN 26U, PIN 28U Battery Voltage	$V_{BAT}$	2	3	3.6	V	3

**CAPACITANCE**(t<sub>A</sub> = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_{IN}$			5	pF	
Output Capacitance	$C_{OUT}$			7	pF	

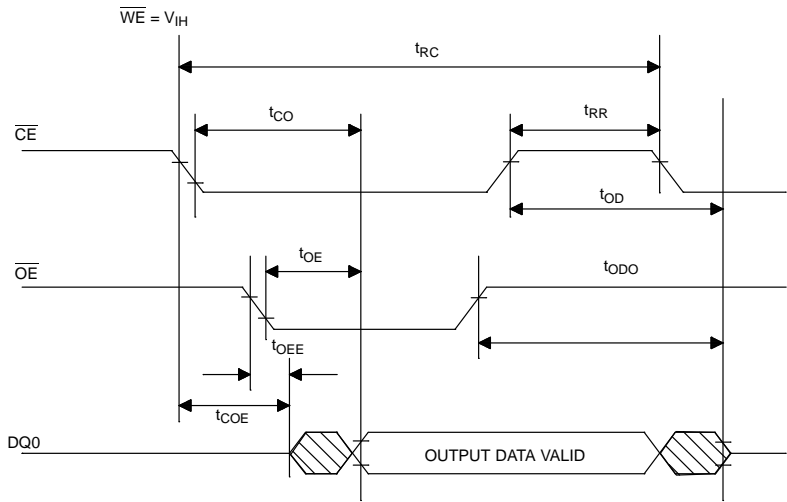
**AC ELECTRICAL CHARACTERISTICS**(0°C to 70°C;  $V_{CC}=4.5$  to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	$t_{RC}$	250			ns	
$\overline{CE}$ Access Time	$t_{CO}$			200	ns	
$\overline{OE}$ Access Time	$t_{OE}$			100	ns	
$\overline{CE}$ To Output Low Z	$t_{COE}$	10			ns	
$\overline{OE}$ To Output Low Z	$t_{OEE}$	10			ns	
$\overline{CE}$ To Output High Z	$t_{OD}$			100	ns	
$\overline{OE}$ To Output High Z	$t_{ODO}$			100	ns	
Read Recovery	$t_{RR}$	50			ns	
Write Cycle Time	$t_{WC}$	250			ns	
Write Pulse Width	$t_{WP}$	170			ns	
Write Recovery	$t_{WR}$	50			ns	11
Data Setup Time	$t_{DS}$	100			ns	12
Data Hold Time	$t_{DH}$	0			ns	12
$\overline{CE}$ Pulse Width	$t_{CW}$	170			ns	
RESET Pulse Width	$t_{RST}$	200			ns	
$\overline{CE}$ Propagation Delay	$t_{PD}$	5	10	20	ns	2, 9
$\overline{CE}$ High to Power-Fail	$t_{PF}$			0	ns	

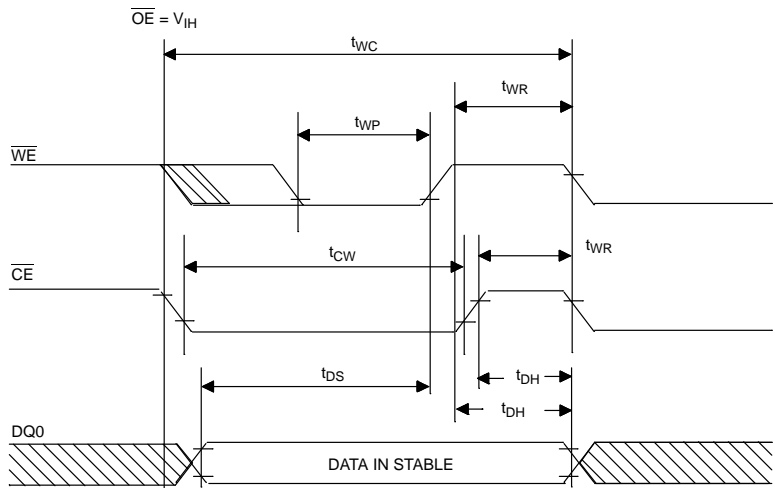
(0°C to 70°C;  $V_{CC} < 4.5V$ )

Recovery at Power-Up	$t_{REC}$			2	ms	
$V_{CC}$ Slew Rate 4.5 – 3V	$t_F$	0			$\mu s$	
$\overline{CE}$ Pulse Width	$t_{CE}$			1.5	$\mu s$	7

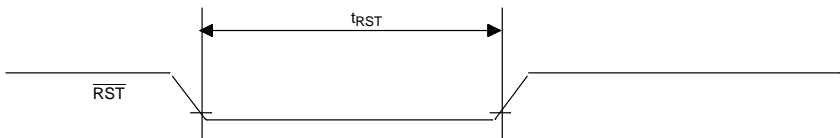
**TIMING DIAGRAM: READ CYCLE TO SMARTWATCH**



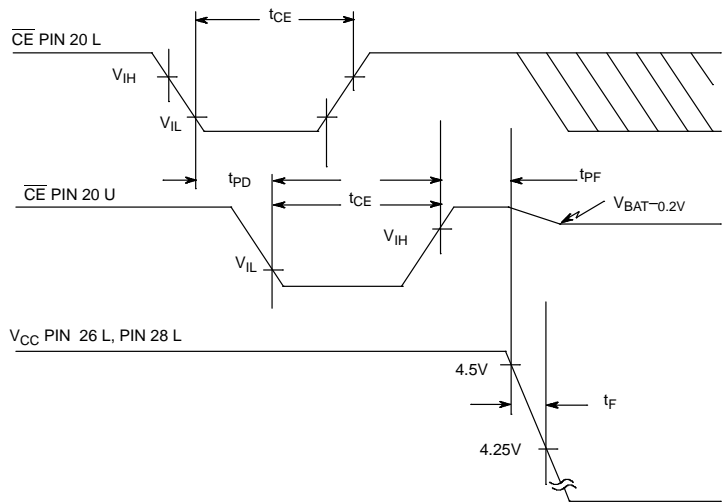
**TIMING DIAGRAM: WRITE CYCLE TO SMARTWATCH**



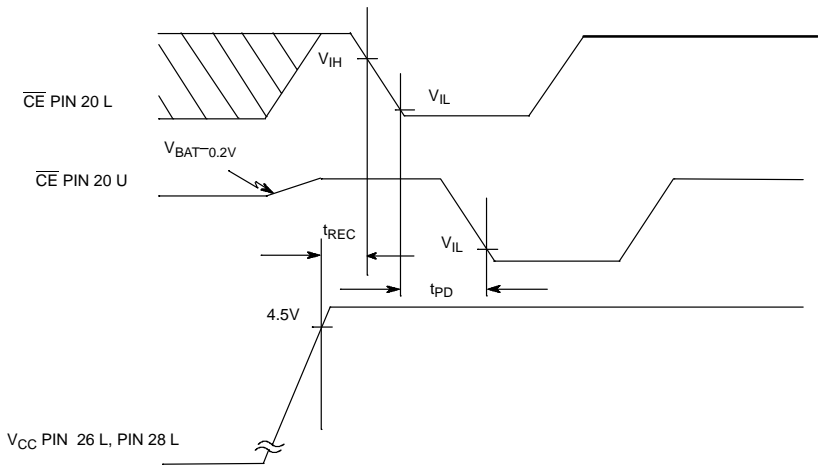
**TIMING DIAGRAM: RESET FOR SMARTWATCH**



**TIMING DIAGRAM: POWER-DOWN**



**TIMING DIAGRAM: POWER-UP**



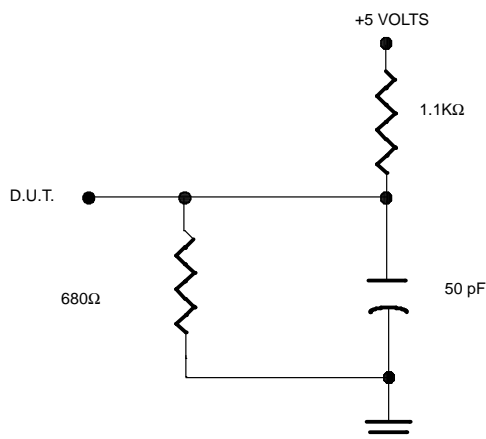
**WARNING:**

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode. Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

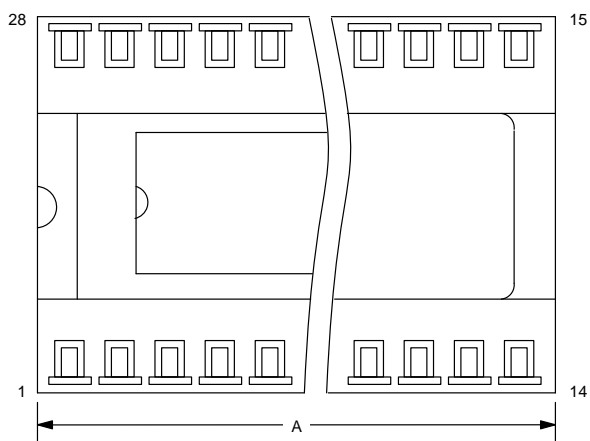


**NOTES:**

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 3.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Pin 26L can be connected to  $V_{CC}$  or left disconnected at the PC board.
6. SmartWatch sockets can be successfully processed through some conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. However, post solder cleaning with water washing techniques is not permissible. Discharge to the lithium energy source may result, even if de-ionized water is utilized. It is equally imperative that ultrasonic vibration is not used in order to avert damage to the quartz crystal resonator employed by the oscillator circuit.
7.  $t_{CE\ max.}$  must be met to ensure data integrity on power loss.
8.  $V_{CC}$  is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.
10. Applies to Pins 1 L, 11 L, 20 L, 22 L, and 27 L.
11.  $t_{WR}$  is a function of the latter occurring edge of  $\overline{WE}$  or  $\overline{CE}$ .
12.  $t_{DH}$  and  $t_{DS}$  are a function of the first occurring edge of  $\overline{WE}$  or  $\overline{CE}$ .
13.  $\overline{RST}$  (Pin 1) has an internal pull-up resistor.

**OUTPUT LOAD Figure 3**

## DS1216B SMARTWATCH



PKG	28-PIN		32-PIN	
DIM	MIN	MAX	MIN	MAX
A IN. MM	1.390 35.31	1.420 36.07	1.580 40.13	1.620 41.14
B IN. MM	0.690 17.53	0.720 18.29	0.690 17.53	0.720 18.29
C IN. MM	0.420 10.67	0.470 11.94	0.400 10.16	0.470 11.94
D IN. MM	0.035 0.89	0.065 1.65	0.035 0.89	0.065 1.65
E IN. MM	0.055 1.39	0.075 1.90	0.055 1.39	0.075 1.90
F IN. MM	0.120 3.04	0.160 4.06	0.120 3.04	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53	0.015 0.38	0.021 0.53
L IN. MM	0.380 9.65	0.420 10.67	0.380 9.65	0.420 10.67

