**Goal:**

The goal of this design is to provide a low power but quality bench power supply powered from a USB port. The envisioned typical use case is prototyping, experimenting and debugging when a full bench top power supply is an inconvenient option. Specs are Vout from 0V to 12V, Iout as much as possible, varies with Vout.

**System Design:**

Input is 5V +/-0.5V. Current available is assumed to be at least 500mA and as high as 1A. It is assumed that the power source current limits itself to protect from overload. The design will be done around a 5V @ 1A supply.

Output voltage will be adjustable from 0V to 12V.

Due to the very limited power available from a USB port (5W), efficiency is important. To be a quality bench power supply requires reasonably low noise, low ripple and good transient response. The first stage must be a buck/boost configuration dc-dc converter. Designers generally understand that bench power supplies are virtually always linear supplies due to their low noise output characteristics. We must use a buck/boost converter in this design however since we want output voltages above and below our input voltage. As a starting point we will assume a 2 stage design. The first stage will be a buck/boost stage whose output tracks the system output voltage with a +1.5V offset. The second stage is a linear regulator which, at 1.5V input-output voltage will provide good noise rejection.

**IOUT vs VOUT:**

Buck-boost converters preserve constant power at their input vs output (minus a little loss from conversion efficiency). For a fixed 5V, 1A (5W) input, the output is always capable of 5W of power. The buck-boost converter output current capability would be Iout = Eff x 5W / Vout, shown in Figure 1. At a output voltage of 5V this means ~1A, at lower voltages current capability is higher, at higher output voltages the current capability is lower. There is a slight offset of the Iout vs Vout curve due to efficiency of the converter. Realistically we will likely find an LDO that has a current limit of 1.5A or below so the second curve in Figure 1 shows a more likely result.

Figure 1: Iout vs Vout if loaded to the full input capability of 5A/1A or 5W, assuming 90% efficiency

Given this output current curve we can calculate power dissipated per stage versus output voltage, shown in Figure 2. A few things stand out when looking at Figure 2:

1. We need to design for over 2W dissipated power in the linear regulator
2. The DC-DC converter dissipates a constant power vs Vout because we assumed a constant efficiency of 90%
3. The DC-DC converter dissipates less power at low Vout because we assumed the LDO would current limit at 1.5A
4. At lower output voltages much of the 5W of available power is dissipated into the linear regulator, leaving less than 3W for the load.

Figure 2: Dissipated power in each stage and in the entire unit.

There is clearly a significant trade-off in available power to the load at lower output voltages due to the linear regulator’s efficiency, even at only 1.5V headroom. Figure 3 shows a similar analysis, but translated into output current, for a single stage buck/boost without a linear for comparison. The buck/boost is assumed to be current limited at 1.5A due to its switch current limit. While a given IC may have a different current limit, this is a reasonable assumption for thinking in general trends. Notice that at potentially the most common output voltages where high current is needed, 3.3V and 5V, the buck/boost only design can provide far more current to the load.

Figure 3: 1 vs 2 stage current delivered to the load vs Vout with both linear and buck/boost limited to 1.5A output current

This trade-off between noise and current available to the load is quite significant. Looking at the noise aspect further, there are three sources of noise in a DC-DC converter:

1. Flicker noise, or 1/f noise, which is prevalent at low frequencies
2. Thermal, or broadband, noise which is prevalent at all frequencies
3. Ripple voltage superimposed due to inductor ripple current into Coutand its ESR, usually 1-2MHz.
4. Switching noise due to fast transients during switching, inducing voltages in parasitic inductances and capacitances, usually up to several to 10’s of MHz or higher.

It turns out that DC-DC converters commonly have 100’s of uV of RMS noise from flicker and thermal noise sources compared to 10’s of µV of RMS noise in linear regulators. The linear regulator 2nd stage would reject virtually all of the switching supply’s flicker and low frequency thermal noise so the low frequency output noise would be only that of the linear itself. DC-DC supplies have much higher ripple voltage (10’s mV RMS) and switching noise (many 10’s or 100’s of mV excursions). The linear would not, however, do much to reject ripple voltage or switching noise because the linear’s control loop doesn’t have bandwidth extending to the MHz range.

Looking at typical bench power supplies, they specify 100’s of µV RMS output noise. If we could adequately filter the ripple and switching noise from the dc-dc converter then the noise benefits associated with adding the linear regulator would no longer be worth the efficiency and space trade-off except for the most noise sensitive applications. Given the reduction in available output current in the sweet spot of 3.3V to 5V, we will pursue a 1 stage buck/boost design as our primary approach with a linear regulator 2nd stage as an option to see how them compare on the bench.

**First stage, non-inverting buck/boost converter:**

Input voltage is 4.5V to 5.5V. If the LDO is included then output voltage ranges from 1.5V to 13.5V. If there is no LDO then Vout is 0V to 12V. We will design for 0V to 13.5V.

We will start by calculating our range of duty cycles. Below ~5V we are in buck mode, above ~5V we are in boost mode. Figure 4 and equations (1) and (2) describe these:

DBUCK = VOUT / (VIN x η) (1)

DBOOST = 1 – (VIN x η)/ VOUT (2)

Figure 4: Duty cycle vs Vout assuming 5V VIN and 85% efficiency

A few interesting points can be observed from Figure 4:

* Duty cycle goes all the way to zero at 0V output. How do we deliver 1.5A of current with the regulator not switching?
* The converter switches from buck to boost mode between 3.8V to 4.7V. Fortunately this falls nicely below 5V and well above 3.3V.
* When a control loop changes from one mode to another it may not behave well right at that transition. It will be interesting to test this regulator right at those points.

The next step in power stage design is to calculate the required inductor value. Inductor choice is one of the most key decisions in a DC-DC converter design. Typically there’s a minimum inductance that should be used in order to keep ripple current within a desirable range. Upper inductor value is determined by size/cost/efficiency vs output voltage ripple. In a lab supply we tend to trade off size/cost/efficiency for improved ripple and we will do so here. Minimum inductor values are governed by:

LMIN,BUCK = [ VOUT x (VIN – VOUT) ] / (KRIPPLE x FSW x VIN x IOUT) (3)

LMIN,BOOST = VIN x (VOUT – VIN) / (KRIPPLE x FSW x VOUT x IOUT) (4)

KRIPPLE is the ripple coefficient which is the amount of ripple current in the inductor as a fraction of the total output current of the regulator. Typical values are 0.2 to 0.4. Ripple current translates directly into output voltage ripple. Being a lab supply, we will design for less ripple current and will target 0.2. Figure 5 shows the calculated minimum inductor value vs output voltage using equations (3) and (4):

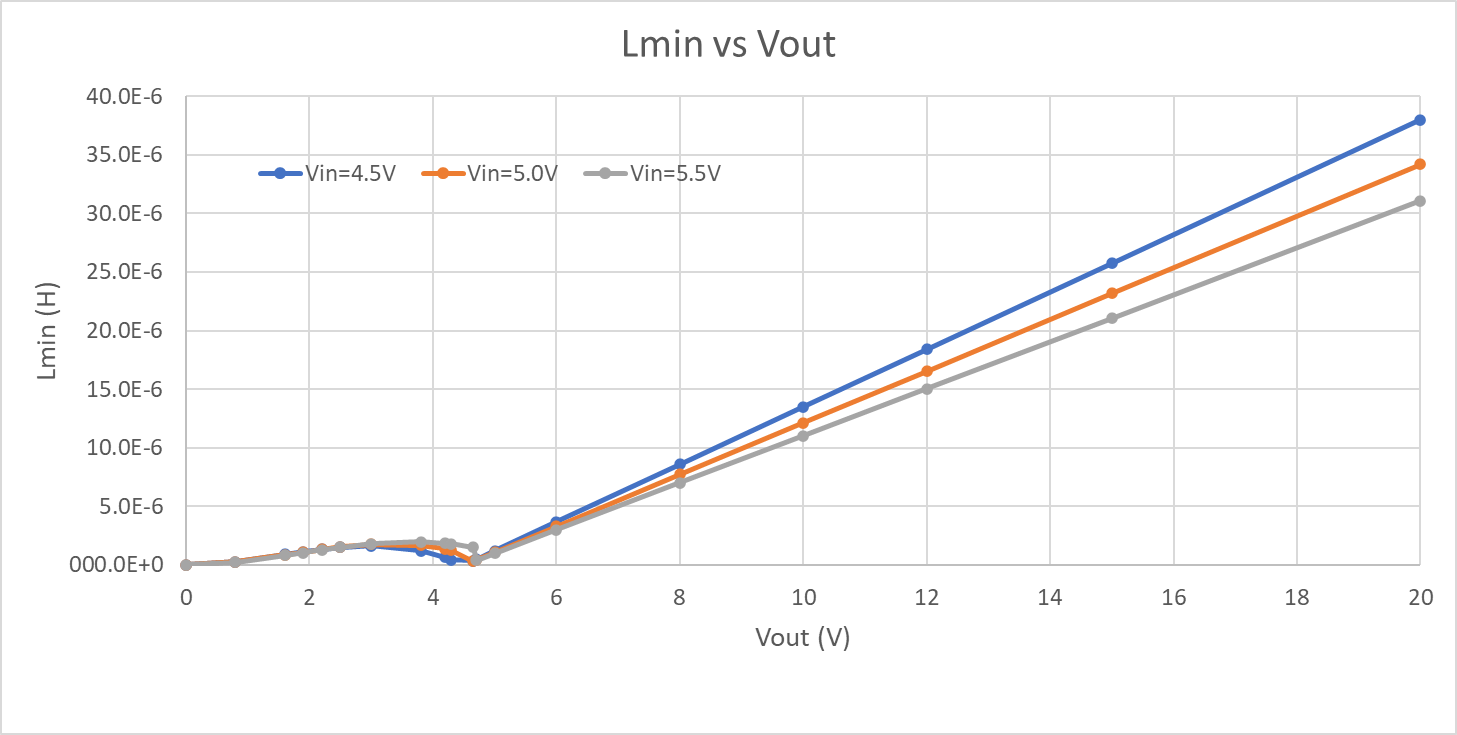


Figure 5: Minimum inductance vs output voltage at min/typ/max Vin

Some observations about Figure 5:

* Minimum inductance value is determined by maximum output voltage (maximum boost ratio)
* Ripple current will be very low at lower Vout values and highest at maximum Vout
* There are good power inductors up to the 33µH range so it may be possible to extend Vout to 20V.

Let’s choose an inductor of 22µH. Now we can calculate the Maximum switch current as determined by equation (5) and is shown in Figure 6:

ISW,MAX,BUCK = IRIPPLE/2 + IOUT (5)

IRIPPLE,BUCK = (VIN – VOUT) x D / (FSW x L) (6)

ISW,MAX,BOOST = IRIPPLE/2 + IOUT/(1-D) (7)

IRIPPLE,BOOST = (VIN x D) / (FSW x L) (8)

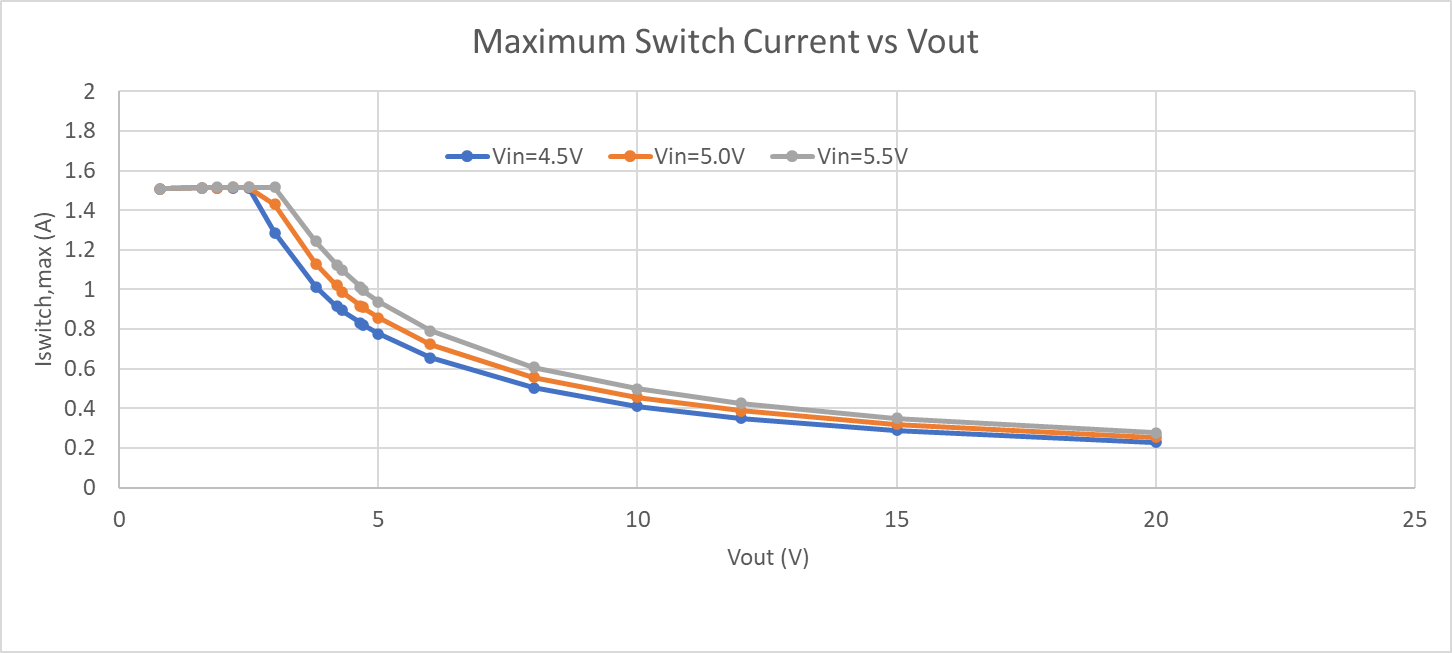


Figure 6: Maximum switch current vs Vout at min and max VIN

As would be expected, maximum switch current in Figure 6 follows the available output current curve from Figure 3. Typical integrated FET switch converter ICs have switch current limits in the 1A to 2A range so the 1.5A output current limit imposed earlier looks reasonable.

Typical power stage design has a required output current; input current is whatever it ends up being. In our case we have a fixed available 1A of input current, so output current ends up whatever it ends up being, as shown in Figure 3.

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**Linear stage**

Given that we assumed the buck/boost has a constant efficiency independent of Vout and we know that maximum Pin = 5V \* 1A = 5W, we then know that maximum Pout,buck-boost = 5A \* 90% = 4.25W.

For the linear regulator stage we will control the system to keep Vin = Vout + 1.5V. Iout=Iin for linear regulators so the current curve follows that of the buck-boost shown in Figure 1. The result, shown in Figure 2, is that the Iout vs Vout curve of the linear regulator is identical to that of the buck-boost converter except offset by the 1.5V offset of Vin – Vout.

Figure 2. Linear regulator Iout capability vs Vout

In most cases linear regulators are less efficient than switching converters. The trade-off is that they have excellent noise rejection, low noise and fast transient response. For a lab supply this trade-off is acceptable. For the modest power capability of a USB supply (~5W), the fraction of power lost to linear regulator efficiency is significant at some voltages and may leave little left to power the device under test. Figure 3 shows the power dissipated in the buck-boost converter, the linear regulator, and the corresponding power delivered to the load. Figure 2 is a good description of the capability of the power supply, Figure 3 is a good picture of the thermal design we need to think about. In reality we will likely choose a linear regulator with a current limit far less than 4.5A so the power dissipated in the linear stage will peak at less than half of what is depicted.

Figure 3: Power dissipated in each stage and maximum power to the load

**USB Port Protection**

USB specifications require that devices communicate to the host usb controller, through a process called enumeration, to request more than 100mA of power. Some usb devices do not go through enumeration but instead tell the user not to plug the device into a port that can’t supply, for example, 500mA. The USB host is supposed to shut down any device that draws more than it’s allowed current but for the most part if a USB host is capable of providing 500mA then it will do so, even without enumeration. A properly designed USB device wouldn’t do this and a properly designed USB host would protect itself from damage. That said, there is no guarantee that a particular laptop does have such protection in place so to be safe this power supply could be used only by USB wall chargers, limiting the potential damage that can be done to the host. In practice there are relatively few reports of damaged USB hubs in computers so users could choose to accept the risk and run it off of a computer USB port.

Inrush current should be limited so as not to trigger a fault by the USB host controller. Input capacitance will be limited to 10µF per the USB spec and the buck/boost converter will be configured to start up slow enough to prevent this condition.

**Buck-boost converter design:**

Buck-boost converters come in multiple forms. One appealing option is a single-inductor 4 switch converter that operates in either buck or boost mode with a smooth crossover between the two modes. Compared to SEPIC and flyback topologies a key advantage here is potentially higher efficiency and smaller solution size, lower current stress on switches and other minor advantages.

The LT3114-1 is such an IC. It provides a compact solution with integrated switches that have the current capacity to supply this project. One downside to the choice of this particular IC is that its switching frequency is 1.2MHz, a high enough frequency that the subsequent linear regulator is not likely to suppress ripple much. Its power stage design is covered here.

Typical power supply designs have an input that is either fixed (such as the output of a prior regulator) or varies (such as a battery or unregulated supply). The goal of the regulator is to provide a fixed output voltage under all conditions. A bench power supply turns that concept on its head by having an output voltage that varies from 0V to some upper limit, 12V in our case. Typical design equations found in data sheets, text books, application notes and the like must be used with care, they may not fit our specific design.

Our first stage, the buck/boost regulator will be based on the TPS63060, a 4-switch buck/boost, will have an input voltage of 5V +/-10% (the USB specification). The linear regulator that follows will be provided an input voltage that is 1.5V higher than its output. The linear regulator’s output voltage varies from 0V to 12V so it will be provided 1.5V to 13.5V. This becomes the output voltage range of our buck/boost stage.

The buck/boost will operate as a buck converter when the output is lower than the input (e.g. 5.0V to 2.5V) and as a boost converter when its output is higher than it’s input (e.g. 5.0V to 10V). We will do two design analyses in parallel: a buck and a boost and use the results that satisfy both designs.

The power stage design starts with determining the minimum value allowed for the inductor. As a buck converter, minimum inductance is given by equation 1.

L = (VIN x (VOUT – VIN)) / (ΔIL x fS x VOUT) (1)

Where ΔIL­ is the target ripple current and fS is the switching frequency. In a buck converter the average current through the inductor is equal to the input current. A common rule of thumb is that the ripple current should be 20% to 40% of the input current. Inductor ripple current will translate into output voltage ripple so lower ripple current equates to lower output voltage ripple. One might expect the ripple current to A bench power supply typically prioritizes performance over cost and size