Advanced MOSFETs and Novel Devices

Dr.-Ing. Josef Biba

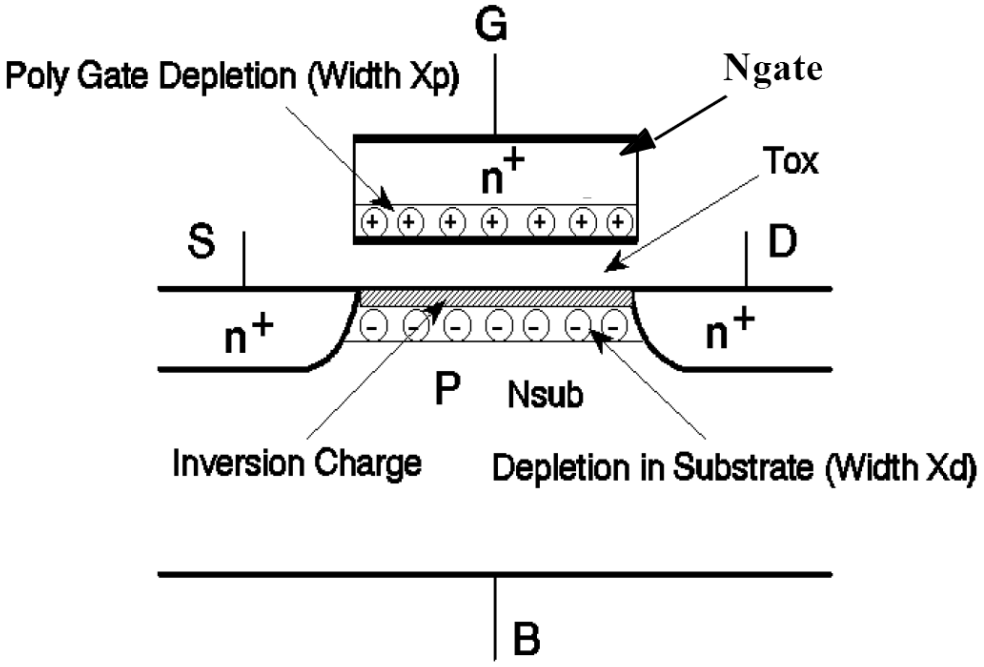
8. Tutorial & Exercise

Gate Depletion

Poly Gate Depletion - Introduction

- For a switched on n-channel MOSFET the n^+ polysilicon gate is biased in depletion
- High doping of polysilicon ($5*10^{19}$ – $1*10^{20}$ cm^{-3}) => small depletion region w_{poly} (1 – 2 nm) < w_{max}
- Additional space charge capacitance

$$C''_{poly} = \frac{\epsilon_0 \epsilon_{poly}}{w_{poly}}$$

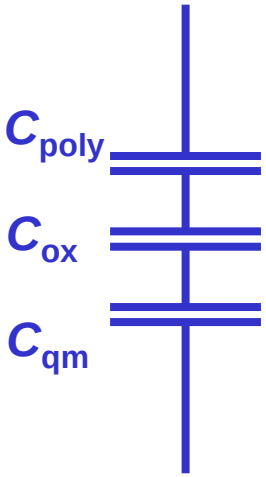


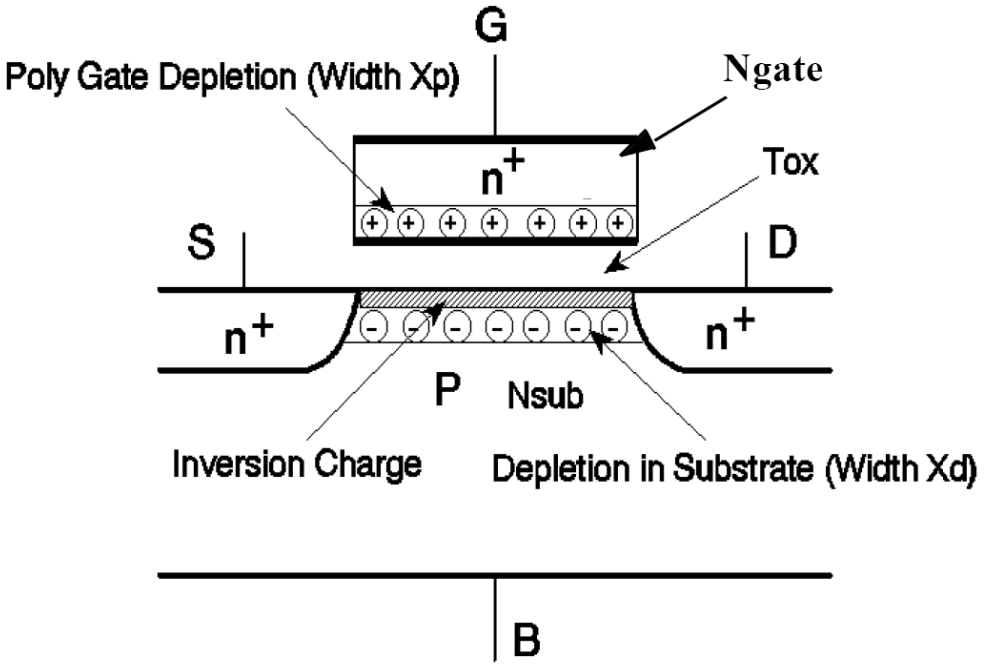
Poly Gate Depletion - Introduction

$$C''_{poly} = \frac{\epsilon_0 \epsilon_{poly}}{w_{poly}}$$

$$C''_{Ox} = \frac{\epsilon_0 \epsilon_{SiO_2}}{d_{Ox}}$$

$$C''_{qm} = \frac{\epsilon_0 \epsilon_{Si}}{d_{qm}}$$





Capacities in series order.

Capacity of Cdep ?
Answer: the device is switched on, so the channel inversion charge is shielding the Cdep, so we do not have to take into account !

Poly Gate Depletion - Exercise

Exercise:

Determine the influence of the poly gate depletion effect on the *p*-channel MOSFET from tutorial #4 (180 nm technology node). Calculate the change of the threshold voltage V_T for the original device and for the two following scaling steps (constant voltage scaling; $S = \sqrt{2}$).

How does the saturation current I_{sat} change at V_{GS}=-V_{DD}.

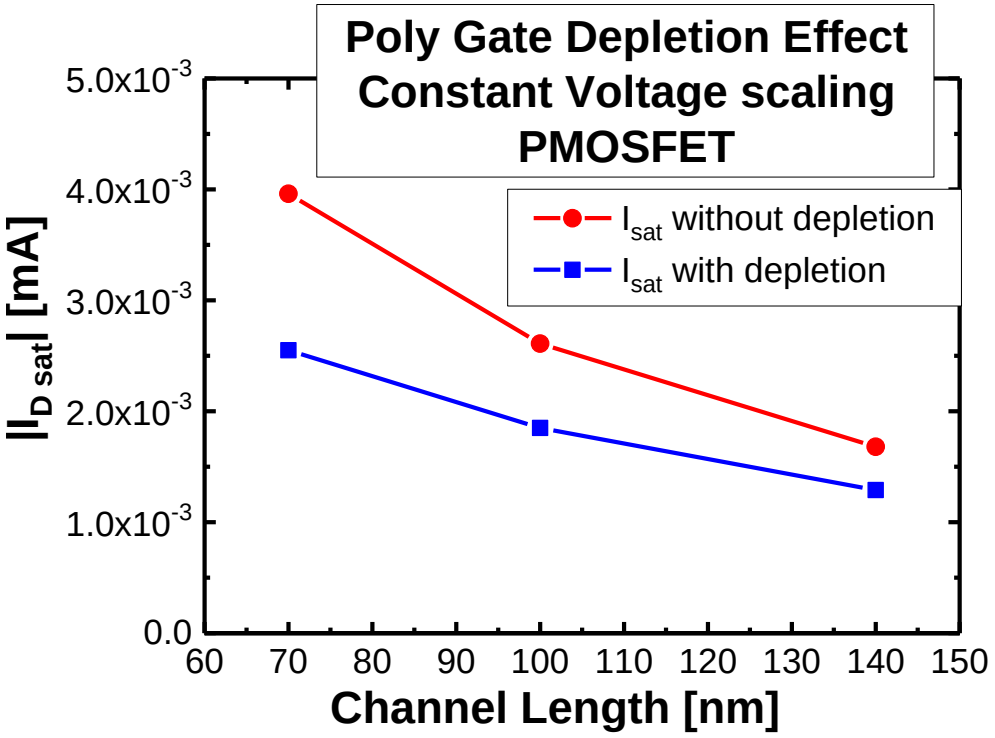
Use the gradual channel approximation. Neglect oxide charges and the effect of quantum mechanical charge distribution in the channel. Assume that the depletion region in the poly gate has a width w_{poly} = 1.5 nm.

V_{DD}	d_{OX}	N_D	L	W	ϕ_m-χ_{Si}	μ_p
1.8 V	3 nm	1e18 cm^{-3}	140 nm	3*L	1.12 V	500 cm^2/ Vs

Results from tutorial #4:

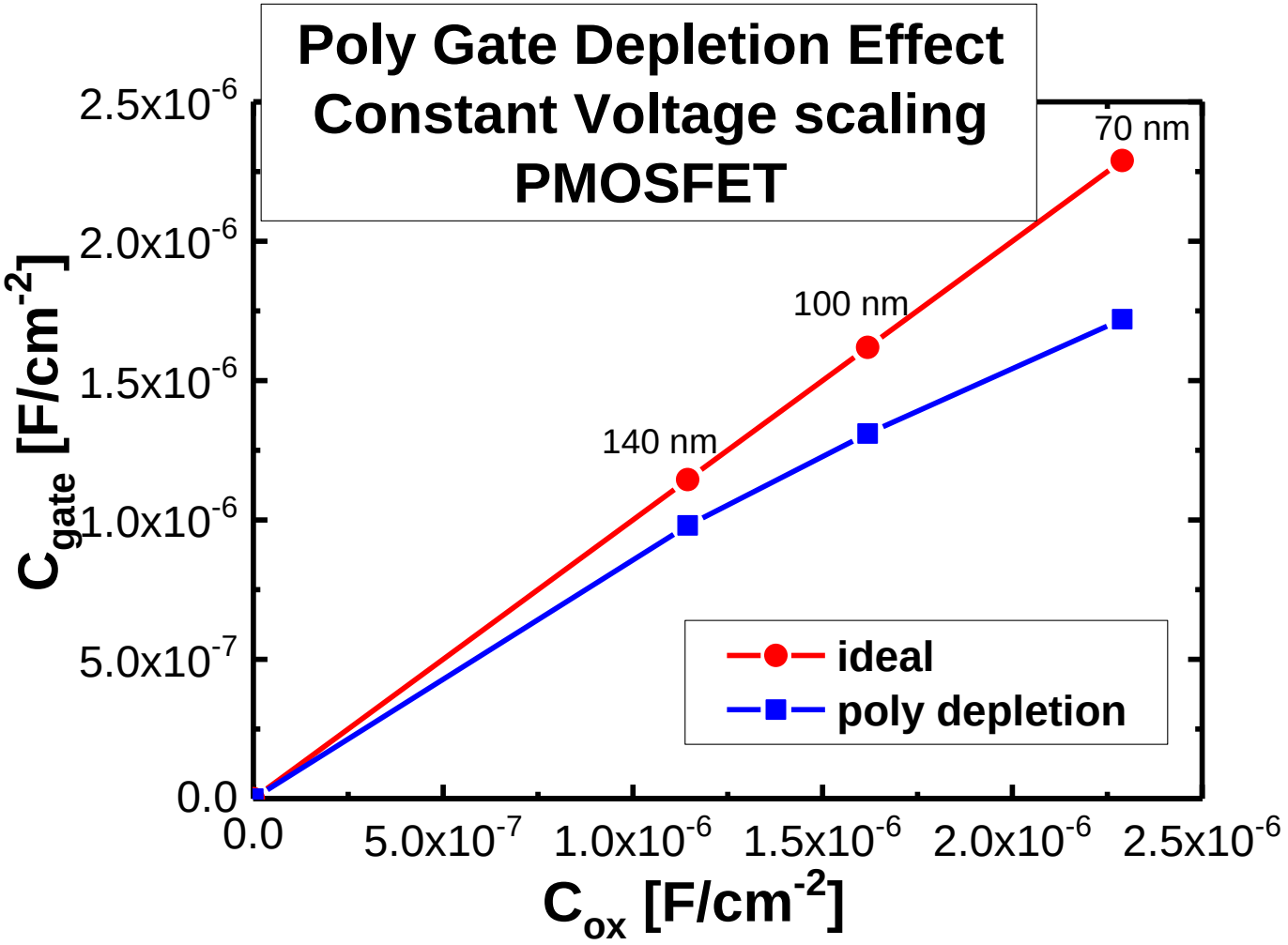
L	140 nm	100 nm	70 nm
V_T	-400 mV	-340 mV	-280 mV

Poly Gate Depletion - Results



L	**140 nm**	**100 nm**	**70 nm**
V_T	-400 mV	-340 mV	-280 mV
$V_{T\ poly\ depletion}$	-479 mV	-432 mV	-400 mV
$\lvert I_{D\ sat}\rvert$	1.69 mA	2.62 mA	3.98 mA
$\lvert I_{D\ sat\ poly\ depletion}\rvert$	1.29 mA	1.85 mA	2.54 mA
$I_{D\ sat}$ reduction	24%	29%	36%

Poly Gate Depletion - Results



Wider poly depletion zone causes lower gate capacitance. This results in reduced charging times and therefore in reduced circuit frequency.