
Advanced MOSFETs and Novel Devices

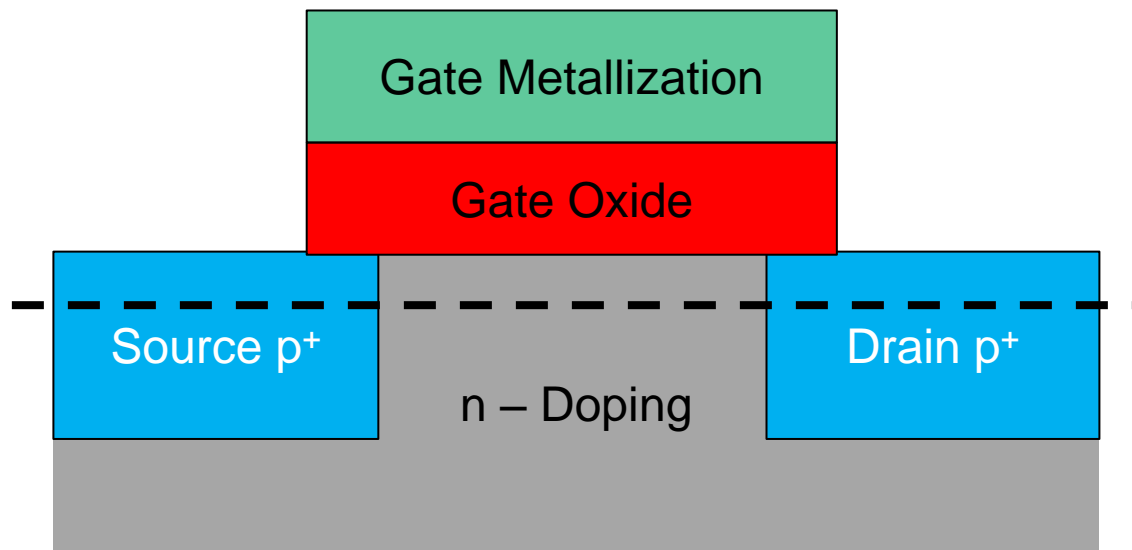
Dr.-Ing. Josef Biba

3. Tutorial & Exercise

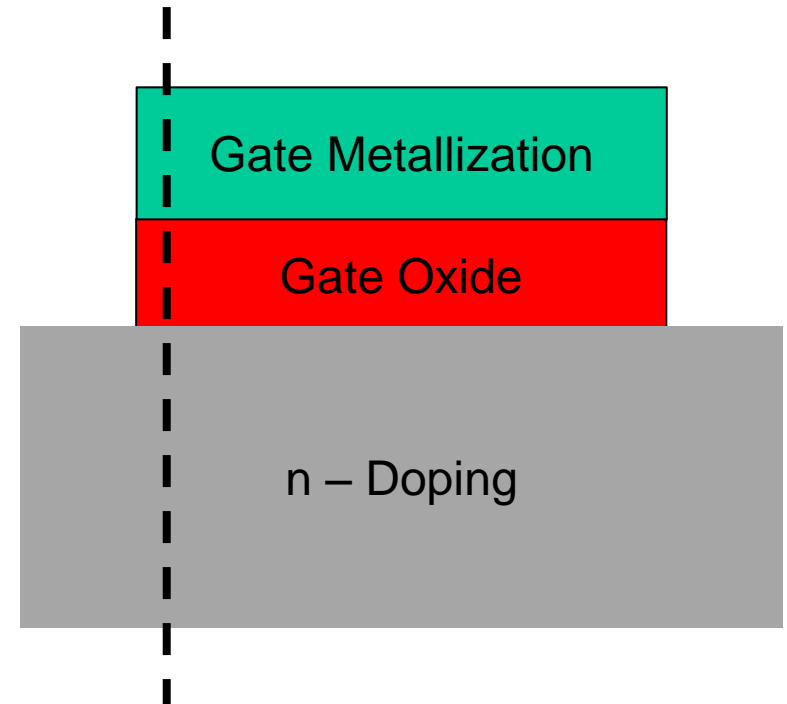
Threshold Voltage

Threshold Voltage – Band diagram MOSFET

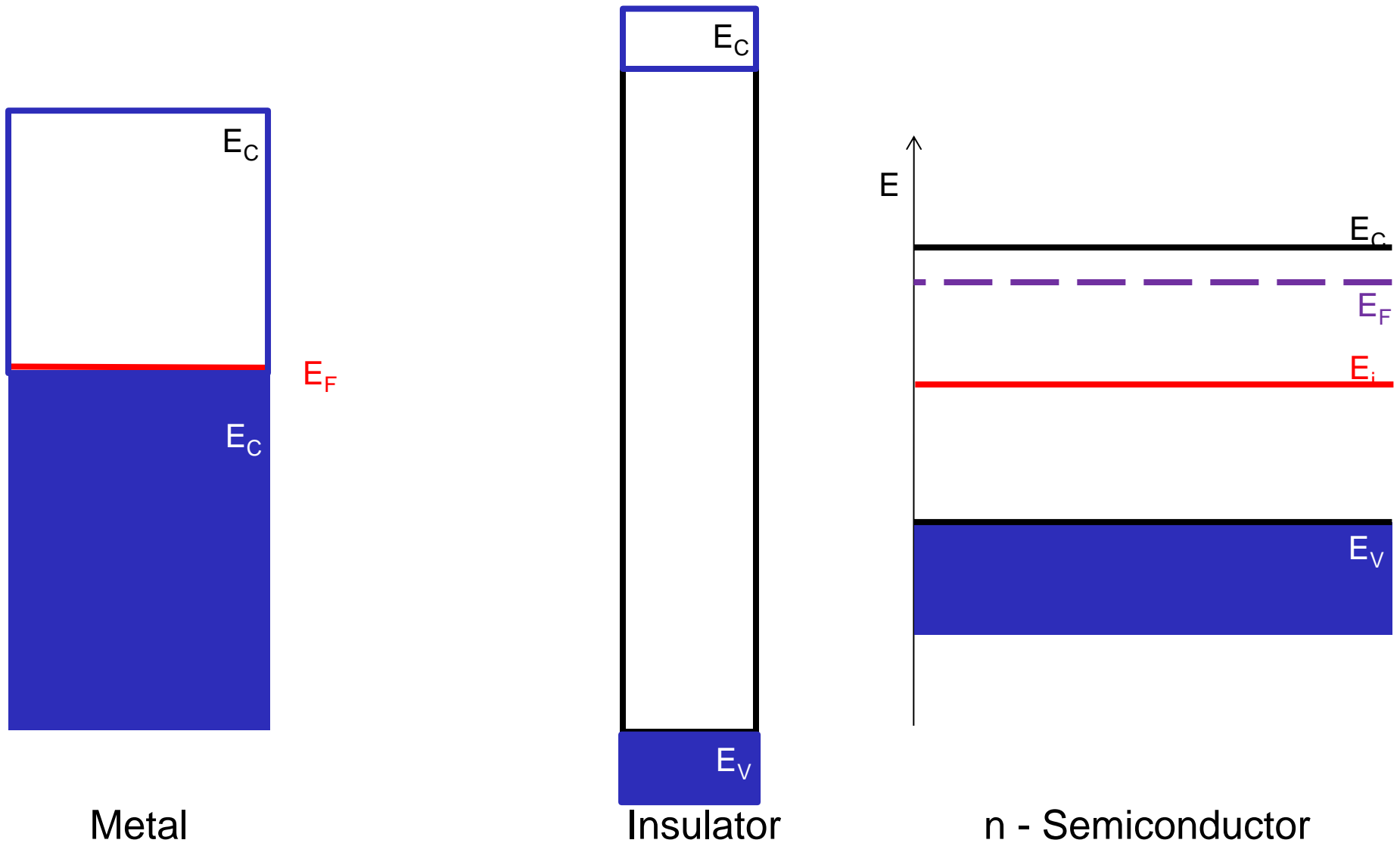
p-Channel MOSFET



MOS-Capacity

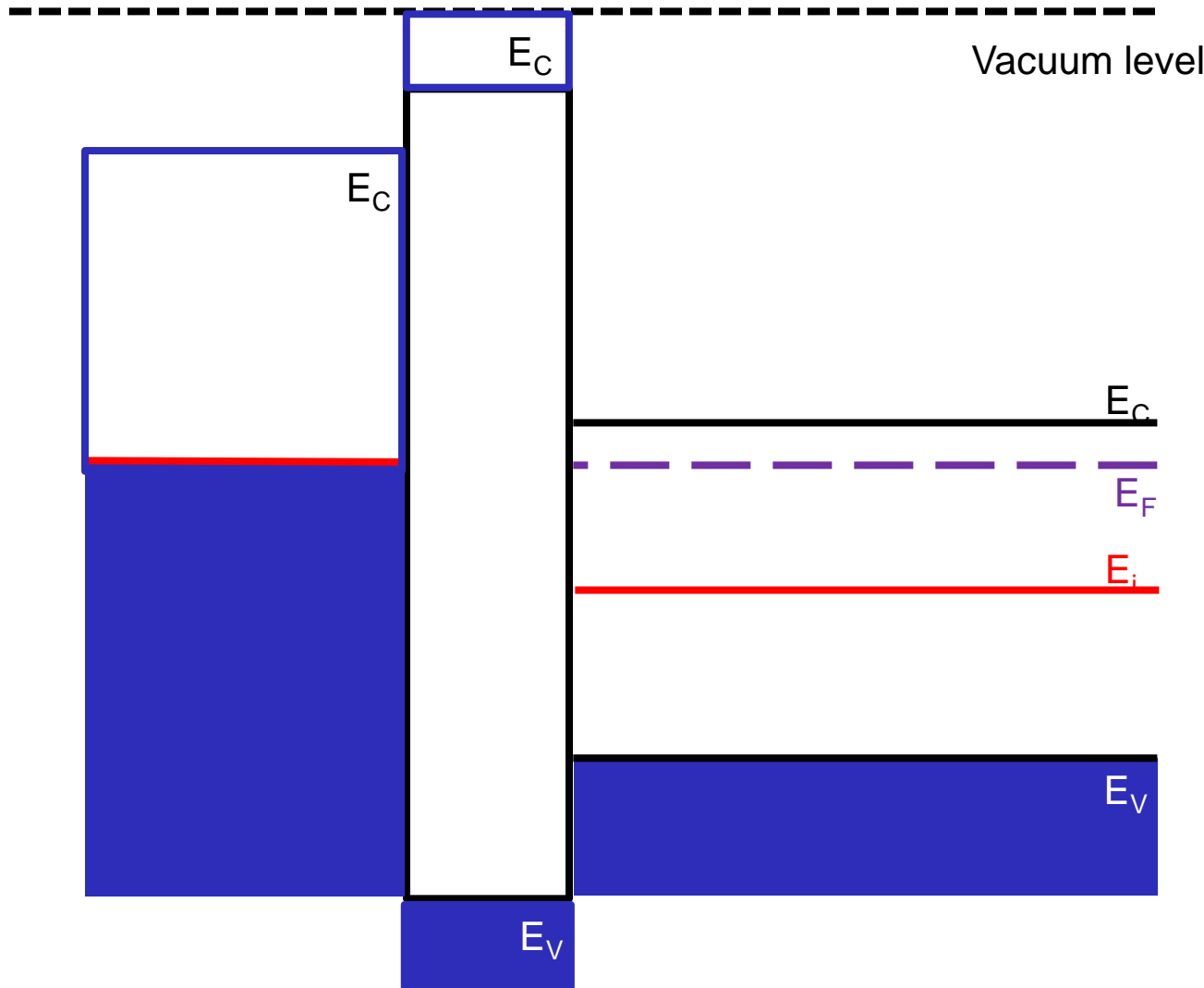


Threshold Voltage – Band diagram MOS-Capacity



Threshold Voltage – Band diagram MOS-Capacity

n - semiconductor

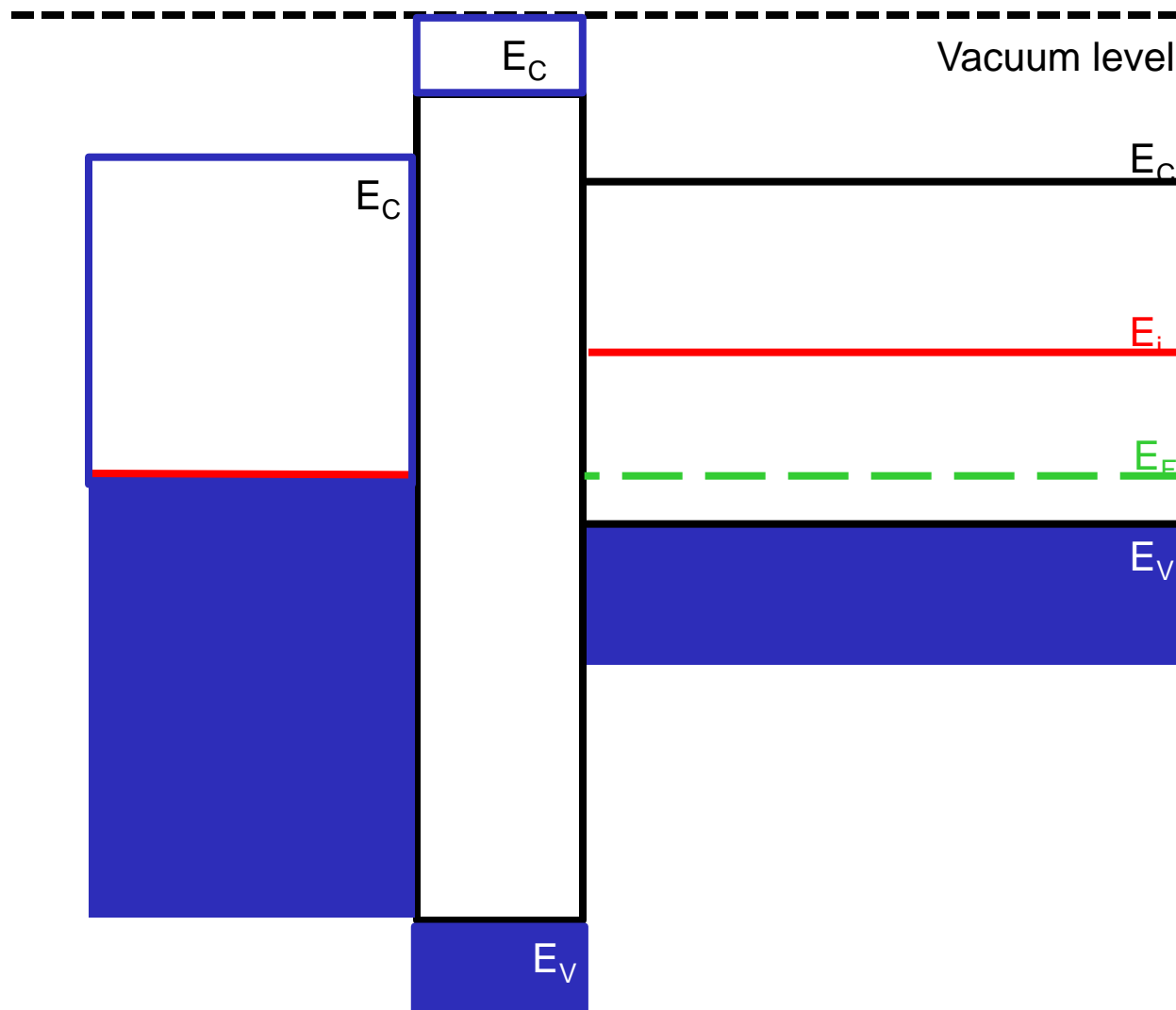


Assume:

- No work function difference between metal and semiconductor.
- Resistivity of the insulator is infinite.
- No oxide charges.

Threshold Voltage – Band diagram MOS-Capacity

p - semiconductor



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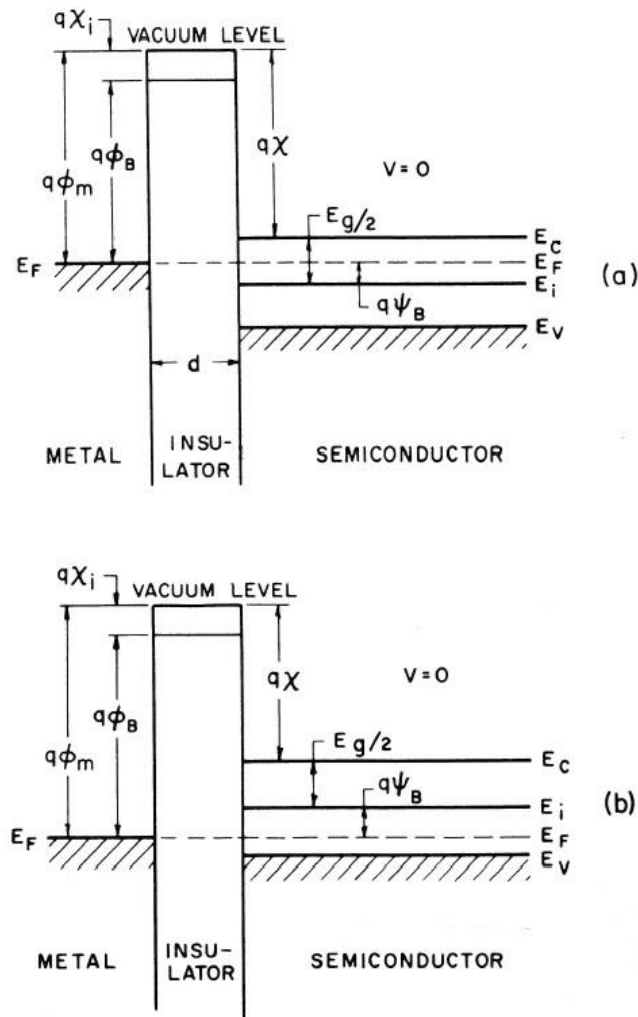


Fig. 2 Energy-band diagrams of ideal MIS diodes at $V = 0$. (a) n -type semiconductor. (b) p -type semiconductor.

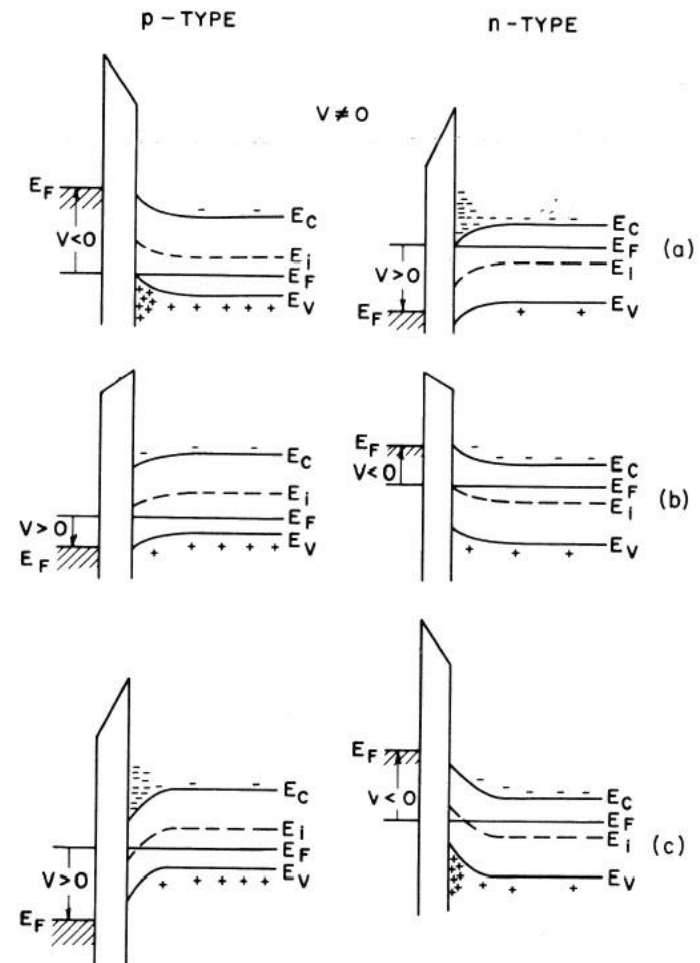
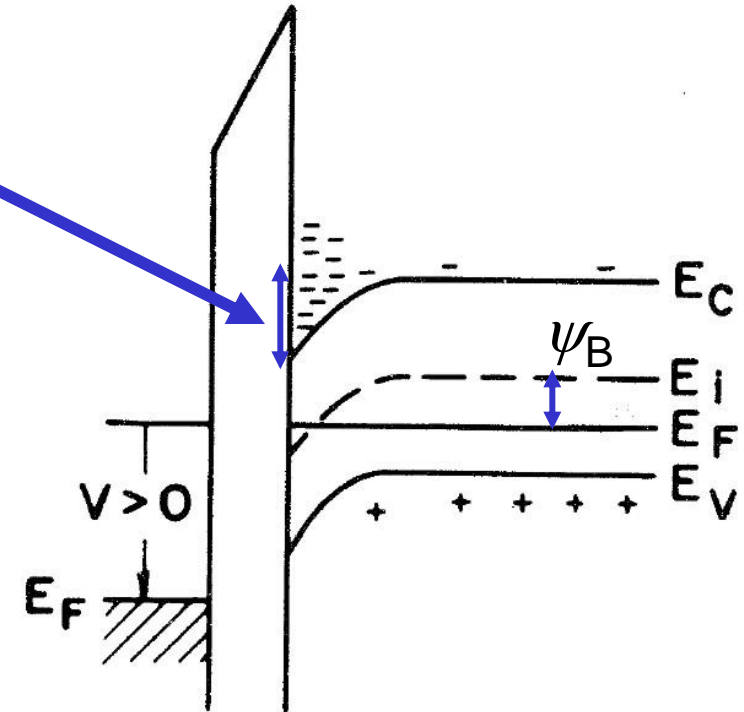
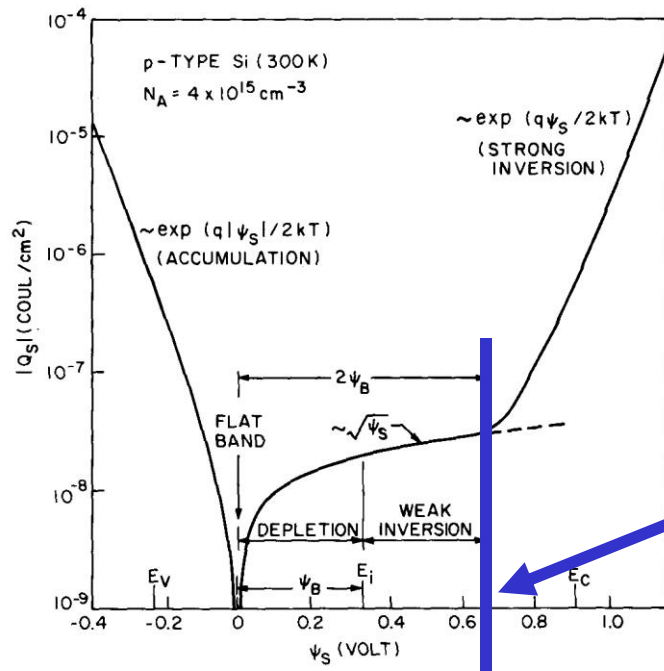


Fig. 3 Energy-band diagrams for ideal MIS diodes when $V \neq 0$, for the following cases: (a) accumulation; (b) depletion; (c) inversion.

Threshold Voltage – Definition

Definition: band bending at the Si-SiO₂-Interface is equal to $2\psi_B$

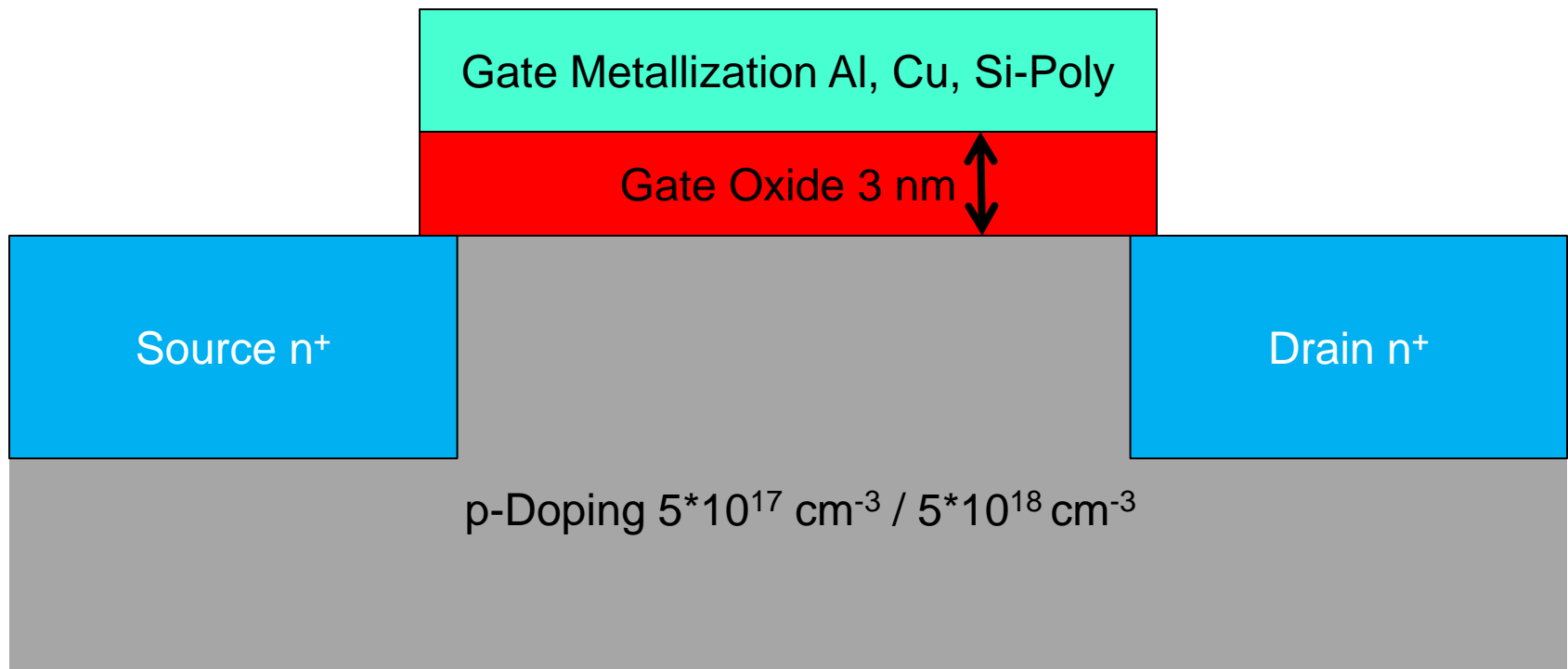
=> concentration of minority exceeds outnumbers the concentration of majority carriers in the bulk silicon



$$V_T = \phi_{MS} \pm \frac{Q''_{OX}}{C''_{OX}} \pm \frac{Q''_{Depl}}{C''_{OX}} \pm / 2\psi_B /$$

Threshold Voltage – Exercise

Determine the threshold voltage V_T for a n -channel MOSFET with different gate metallization (Al, Cu, n - and p -poly Si) for two different channel dopings ($5 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{18} \text{ cm}^{-3}$) at room temperature. The thickness of the gate oxide is 3 nm. Oxide charges can be considered zero.



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| Physical Constants | e | ϵ_0 | k_B |
|--------------------|--------------|-----------------|---------------|
| | 1.6E(-19) As | 8.85E(-14) F/cm | 8.6E(-5) eV/K |

| Parameters | E_g | χ | ϵ_r | n_i |
|------------------|---------|--------|--------------|---------------------------------------|
| Si | 1.12 eV | 4.05 V | 11.9 | $1.45 \times 10^{10} \text{ cm}^{-3}$ |
| SiO ₂ | 8.8 eV | 1.00 V | 3.9 | - |

| Metal | Al | Cu | n -poly Si | p -poly Si |
|-----------------------------|----------|--------|--------------|--------------|
| $\phi_M - \chi_{\text{Si}}$ | - 0.06 V | 0.63 V | 0.0 V | 1.12 V |

Threshold Voltage – Exercise

V_T Results

| | Al | Cu | <i>n</i> -poly Si | <i>p</i> -poly Si |
|------------------------------|----|----|-------------------|-------------------|
| $N_A = 5e17 \text{ cm}^{-3}$ | | | | |
| $N_A = 5e18 \text{ cm}^{-3}$ | | | | |

Major Design Parameters for V_T :

- Channel doping
- Work function of gate metallization
- Oxide thickness

Threshold Voltage – Solution

Threshold voltage: $V_T = \left| \frac{Q_{Depl}''}{C_{ox}''} \right| + |2\Psi_B| + \Phi_{MS} - \frac{Q_{ox}''}{C_{ox}''}$ N-channel MOSFET

Oxide charges: $Q_{ox}'' = 0 \Rightarrow \frac{Q_{ox}''}{C_{ox}''} = 0$

Workfunction difference: $\Phi_{MS} = \Phi_M - \left(X_{si} + \frac{E_g}{2q} + |\Psi_B| \right)$

Electrostatic bulk potential: $\Psi_B = \frac{k_B T}{q} \cdot \ln\left(\frac{N_{dop}}{n_i}\right)$

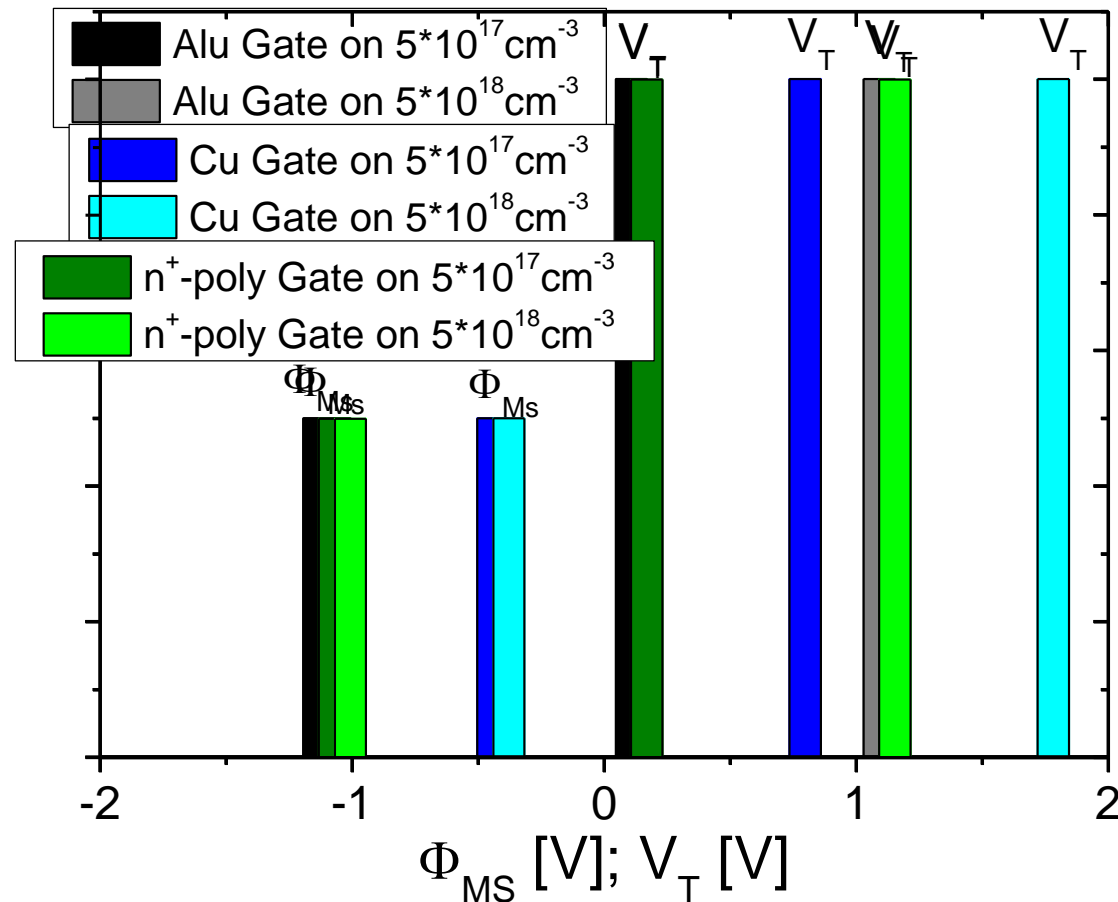
Normalized Capacitor: $C = \epsilon_0 \epsilon_r \frac{A}{d} \quad C_{ox}'' = \frac{C_{ox}}{A} = \frac{\epsilon_0 \epsilon_{SiO_2}}{d_{ox}}$

Space charge: $Q_{Depl}'' = \int_0^{w_{max}} \rho_S(x) dx = w_{max} e N_A$

Depletion region: $w_{max} = \sqrt{\frac{4 \epsilon_0 \epsilon_{Si} |\Psi_B|}{e N_A}}$

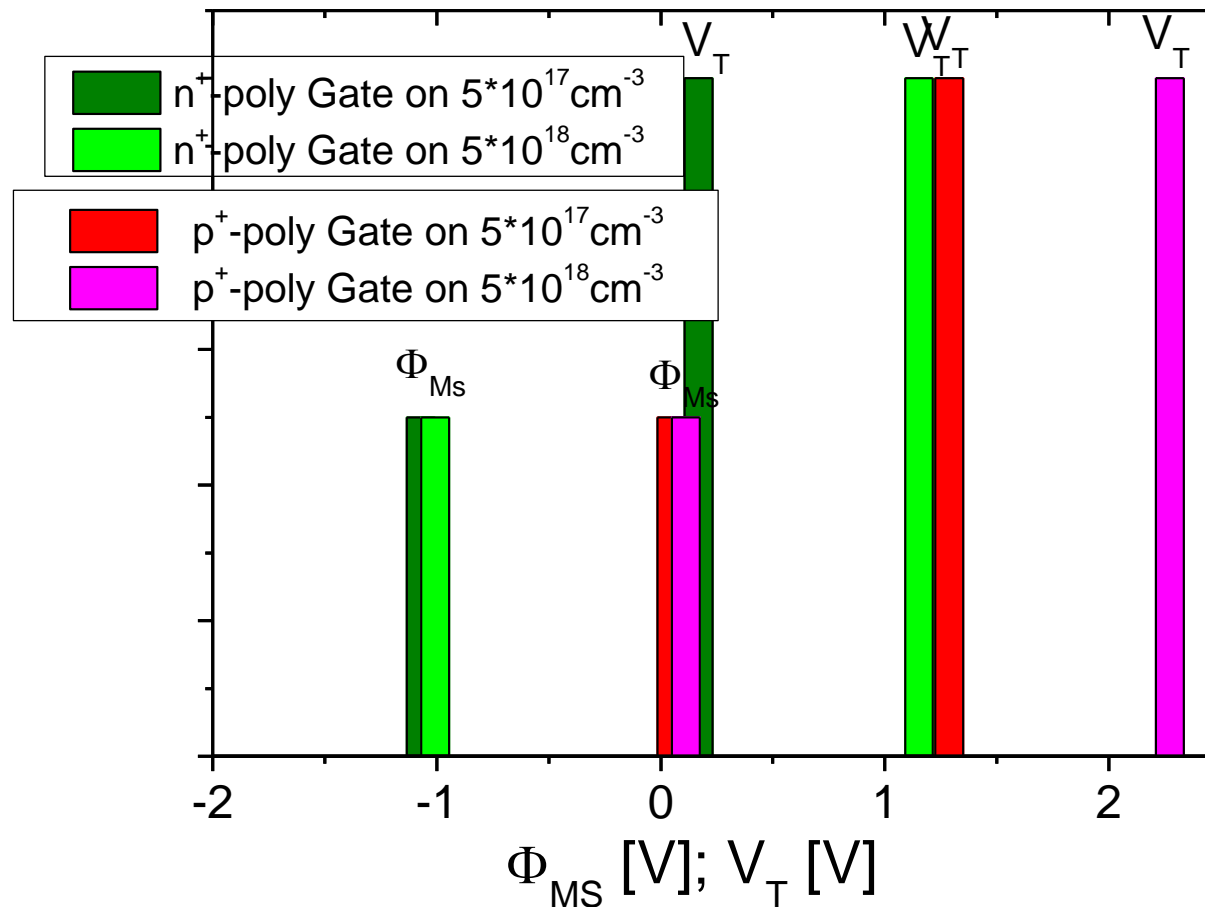
Threshold Voltage – Solution

Using different gate metals



We can see that the threshold voltage can be adjusted by the metal

Changing the doping of the polysilicon gate



Threshold Voltage – Solution

V_T calculations for a symmetric CMOS-Inverter

