
Advanced MOSFETs and Novel Devices

Dr.-Ing. Josef Biba

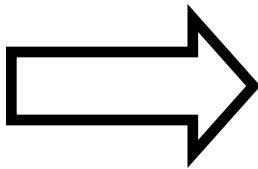
4. Tutorial & Exercise

Shrinking

Constant Field scaling (ideal):

Factor $S > 1$

- Lateral dimensions (L, W) $1/S$
- Vertical dimensions (d_{OX}, r_j) $1/S$
- Channel doping (N_A, N_D) $*S$
- Supply voltage (V_{DD}) $1/S$



electric field in transistor remains constant

Constant Voltage scaling:

- Lateral dimensions $1/S$
- Vertical dimensions $1/S$
- Channel doping $*S$

Shrinking - Exercise

Determine the influence of constant field scaling on a p -channel MOSFET of the 180 nm technology node ($S = \sqrt{2}$). Calculate the threshold voltage V_T and draw the output characteristics for different gate-source voltages ($|V_{GS}| = V_{DD}$, $0.75 \cdot V_{DD}$, $0.5 \cdot V_{DD}$ and $0.25 \cdot V_{DD}$) for the original and the scaled device. Use the gradual channel approximation. Neglect fixed and trapped oxide charges.

Technology parameters:

V_{DD}	d_{OX}	N_D	L	W	$\phi_M - \chi_{Si}$	μ_p
1.8 V	3 nm	$1e18 \text{ cm}^{-3}$	140 nm	$3 \cdot L$	1.12 V	$500 \text{ cm}^2/\text{Vs}$

Threshold voltage:

$$V_T = \Phi_{MS} - \left| \frac{Q''_{Depl}}{C''_{Ox}} \right| - |2\Psi_B| - \frac{Q''_{Ox}}{C''_{Ox}}$$

Workfunction difference:

$$\Phi_{MS} = \Phi_M - \left(\chi_{Si} + \frac{E_g}{2q} - |\Psi_B| \right)$$

Electrostatic bulk potential:

$$\Psi_B = \frac{k_B T}{q} \cdot \ln\left(\frac{N_{dop}}{n_i}\right)$$

Normalized Capacitor:

$$C''_{Ox} = \frac{C_{Ox}}{A} = \frac{\epsilon_0 \epsilon_{SiO_2}}{d_{Ox}}$$

Space charge:

$$Q''_{Depl} = \int_0^{w_{max}} \rho_S(x) dx = w_{max} e N_D$$

Depletion region:

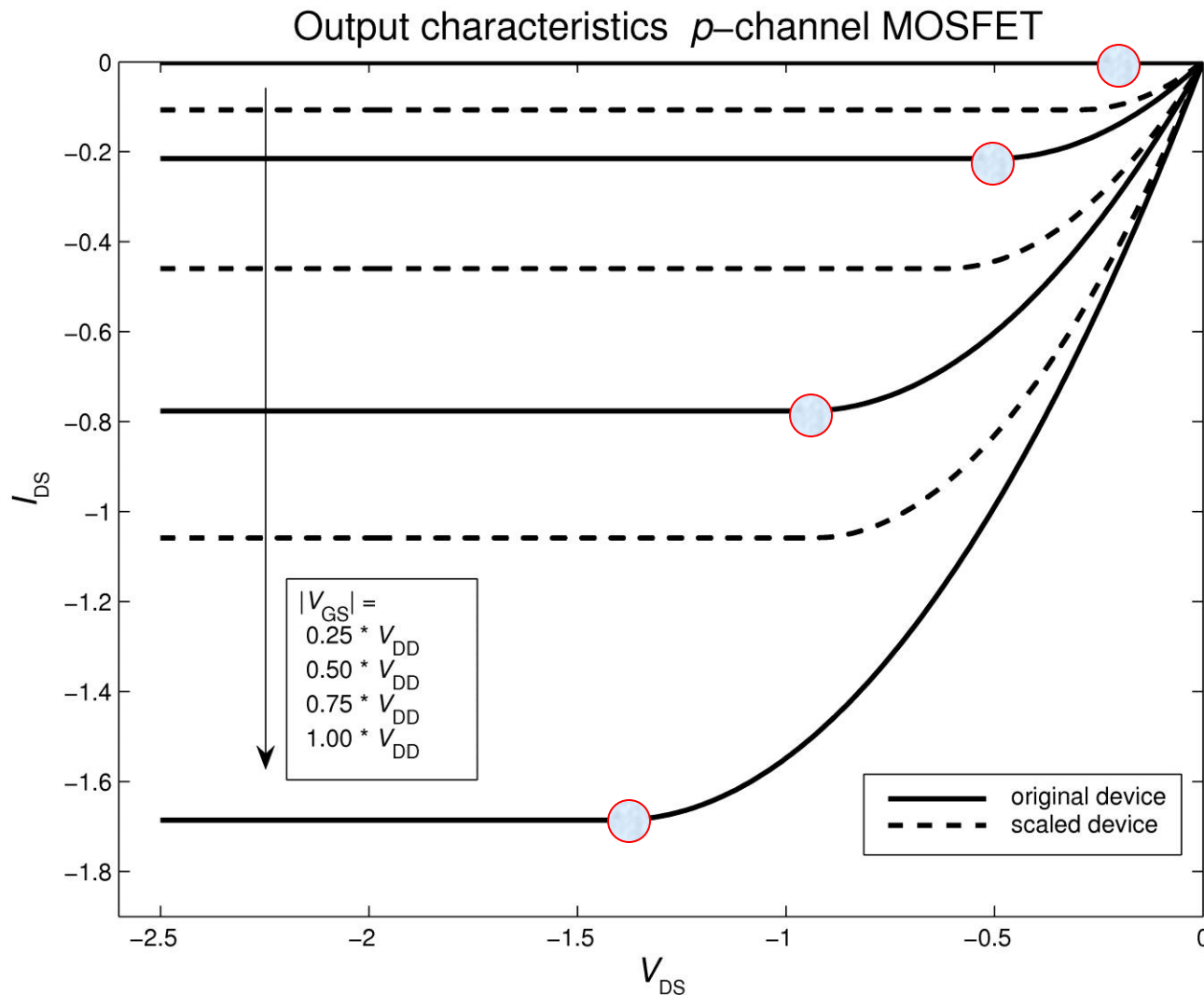
$$w_{max} = \sqrt{\frac{4\epsilon_o \epsilon_{Si} |\Psi_B|}{e N_D}}$$

Selected points of the output characteristic

$$V_{DD1} = V_{DD} = 1.8V$$

$$V_{DD2} = V_{DD1} / S = 1.27V$$

V_{GS}	$- \frac{1}{4} V_{DD}$	$- \frac{1}{2} V_{DD}$	$- \frac{3}{4} V_{DD}$	$- V_{DD}$
$V_{GS1} - V_{T1}$				
I_{Dsat1}				
$V_{GS2} - V_{T2}$				
I_{Dsat2}				



$$V_{DD \text{ orig}} = 1.8 \text{ V}$$

$$V_{DD \text{ scaled}} = 1.8 / S \text{ V}$$

$$= 1.27 \text{ V}$$

Result:
Shrunked device shows lower I ,
but because following C_{gate} is
shrunked as well, the lower I can
charge the next gate faster ?