ECE385 Spring 2023 – Lab 1 Report

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Introduction

This lab introduces the concept of static hazard and presents a solution. Adding a redundant term to the 2:1 MUX prevents the output from "jumping" between circles in the K-map and eliminates the temporary `0` glitches when the output should be a constant `1`.

Circuit Behavior

This triple-input circuit is intended to work as a 2:1 MUX, in which `B = 1` selects `A` and `B = 0` selects `C`. The SOP expression is `AB+CB'`, and DeMorgan's Law realizes our two-level logic with 3 NAND gates. Moreover, connecting a NAND's two inputs together gives a NOT gate, so `B'` can fit into the fourth NAND gate. A minimum of one 7400 chip would suffice!

Yet the circuit suffers from static hazard. Suppose `A`, `B`, and `C` are all `1`s at the beginning, and we now flip `B` to `0`. But it takes several nanoseconds for the NAND gate to take effect and flip `B'` to `1`, and during this period of ambiguity, `B` and `B'` are both `0`s, `AB` and `CB'` are both `0`s, and so the circuit's output is briefly glitched to `0`.

We add a redundant term `AC` to "bridge" the two circles in the minimized K-map. This ensures that at least one of the three terms in SOP is `1` when the output is supposed to be `1` – in the above case, `AC` remains `1` even before `B'` is flipped to `1`. This redundant term eliminates the static hazard even though it involves an extra 7410 chip.

Component Layout

- 2:1 MUX – Switches to `A`, `B`, `C`, LED to `AB+CB'` ("OUT")

B	1	14	VCC
B	2	13	A
B'	3	12	B
B'	4	11	(AB)'
C	5	10	(AB)'
(CB')'	6	9	(CB')'
GND	7	8	OUT

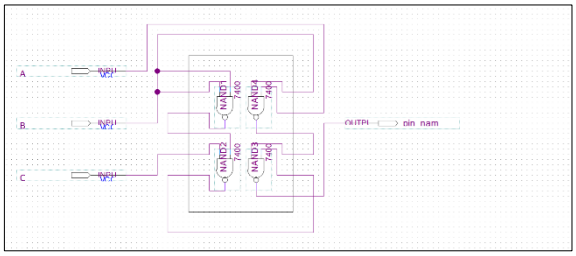
7400

- 2:1 MUX with a redundant term – Switches to A, B, C, LED to AB+CB’+AC (“OUT”)

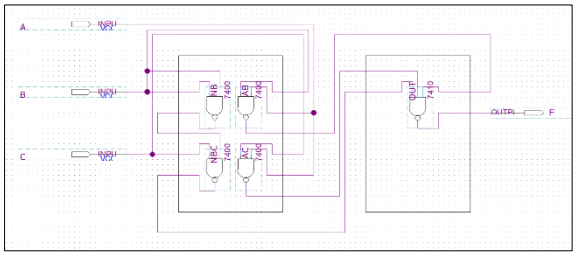
B	1		14	VCC
B	2		13	A
B’	3	7400	12	B
B’	4		11	(AB)’
C	5		10	A
(CB’)’	6		9	C
GND	7		8	(AC)’

(AC)’	1		14	VCC
(CB’)’	2		13	(AB)’
	3	7410	12	OUT
	4		11	
	5		10	
	6		9	
GND	7		8	

Circuit Diagrams



2:1 MUX (AB+CB’)



2:1 MUX with a redundant term (AB+CB’+AC)

Lab Documentation

- Truth Tables

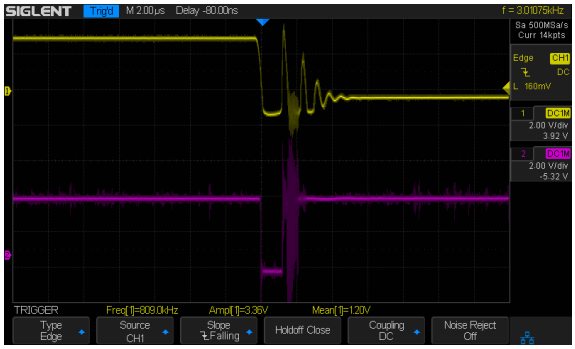
A	B	C	AB+CB’
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

A	B	C	AB+CB’+AC
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

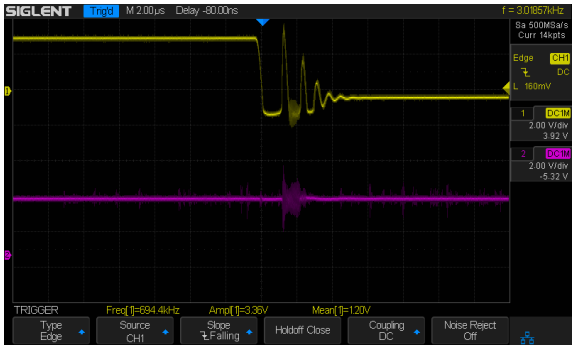
- Pre-Lab Question

Chaining a series of inverters or adding a small capacitor to the inverter’s output both enhance the static hazard. That’s because the inverter’s maximum delay time is lengthened in both cases – either the delay is multiplied by the number of chained inverters, or the output is made “reluctant” to flip by charging or discharging the capacitor.

- Oscilloscope Printouts (Courtesy of Zuofu Cheng)



2:1 MUX (AB+CB')



2:1 MUX with a redundant term (AB+CB'+AC)

Post-Lab Questions

- Timing Diagram

Time (ns)	-20	0	20	40	60	80	100	120	140	160	180
A	1	1	1	1	1	1	1	1	1	1	1
B	1	0	0	0	0	0	1	1	1	1	1
C	1	1	1	1	1	1	1	1	1	1	1
B'	0	?	1	1	1	1	?	0	0	0	0
(AB)'	0	?	1	1	1	1	?	0	0	0	0
(CB')'	1	?	?	0	0	0	?	?	1	1	1
Z	1	?	?	?	1	1	?	?	?	1	1

Z is unstable for 20 (NOT B) + 20 (NAND with C) + 20 (NAND with (AB)') = 60 ns.

- Debouncer Circuit

On the one hand, the single-pole double-throw switch physically prevents the switch from bouncing between OPEN and CLOSED states.

On the other hand, the cross-coupled NAND latch can buffer the output to remain stable. Consider a desired steady state in which the switch is at A, D = 0, G = 1, E = Q' = 0, and F = Q = 1. Suppose now Q glitches to 0. This

(1) brings F to 0 and Q' to F NAND G = 0 NAND 1 = 1, which in turn

(2) brings E to 1 and Q to D NAND E = 0 NAND 1 = 1. **(Auto-correction!)**

(3) The **correct** value of Q = 1 is then propagated back to F = 1, which

(4) brings Q' to F NAND G = 1 NAND 1 = 0, E to 0, and finally,

(5) Q to D NAND E = 0 NAND 0 = 1. The circuit is now stable.

In other words, the circuit has an internal mechanism to correct a glitched output swiftly.

Questions from the General Guide

- Noise Immunity (GG.6)

The advantage of having a large noise immunity is that the circuit is more tolerant towards floating voltage, therefore reducing the chance of the hardware logic behaving abnormally in case the voltage supply falls significantly below 5V.

Only the *last* inverter is observed, because the element with the smallest noise immunity determines the noise immunity of the whole logic circuit. Even if the *first* inverter is very noise tolerant, the circuit will behave abnormally if some chip in the middle of the interconnection is exceptionally strict about the voltage level.

For the inverter circuit in GG.7:

- When the input is H (1.35~5.00V), the output is L (0.35V).

  Positive noise immunity is $\frac{5-1.35}{2} = 1.825V$.

- (1.35, 0.35), (1.15, 2.00), and (x, 3.50) falls on the same line, then $x \approx 0.97$V.
- When the input is L (0.00 ~ 0.97V), the output is H (3.50V).

  Negative noise immunity is $\frac{0.97-0}{2} \approx 0.484V$.

Note: *The diagram presents another algorithm based on "nominal ranges." The positive noise immunity is 3.5 – 1.35 = 1.15 V, and the negative immunity is 1.15 – 0.35 = 0.8 V.*

- Resistors in LED (GG.31)

If several LEDs share the same resistor, they are connected in parallel, which lowers their collective resistance. The LEDs experience a smaller voltage drop which, combined with the divided current, may not be sufficient to drive them to emit light.

Conclusion

Except that we sometimes have to chain several inverters or add a capacitor to amplify the static hazard, it appears as a significant malfunction of the circuit especially when it comes to clock edges. The redundant term method provides a remedy which guarantees that *at least one output of the gates remains unchanged at a single flip of signals*. This effect is confirmed by observing the circuit's response to a square wave "selection" signal.