`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 2017/07/16 17:21:37

// Design Name:

// Module Name: counter

// Project Name:

// Target Devices:

// Tool Versions:

// Description: 时间控制模块

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

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//////////////////////////////////////////////////////////////////////////////////

module counter(

input clk,

input rst,

output clk\_bps

);

reg [13:0]cnt\_first,cnt\_second;//clk时钟信号是10^-8秒，clk\_bps时钟信号是1秒

always @( posedge clk or posedge rst )

if( rst )

cnt\_first <= 14'd0;

else if( cnt\_first == 14'd10000 )//每当cnt\_first到达10000，cnt\_first清零

cnt\_first <= 14'd0;

else

cnt\_first <= cnt\_first + 1'b1;//每收到1个clk信号，cnt\_first+1

always @( posedge clk or posedge rst )

if( rst )

cnt\_second <= 14'd0;

else if( cnt\_second == 14'd10000 )//每当cnt\_second到达10000，cnt\_second清零

cnt\_second <= 14'd0;

else if( cnt\_first == 14'd10000 )

cnt\_second <= cnt\_second + 1'b1;//每当cnt\_first到达10000，cnt\_second+1，cnt\_first清零

assign clk\_bps = cnt\_second == 14'd10000 ? 1'b1 : 1'b0;//每当cnt\_second到达10000，clk\_bps=1

endmodule