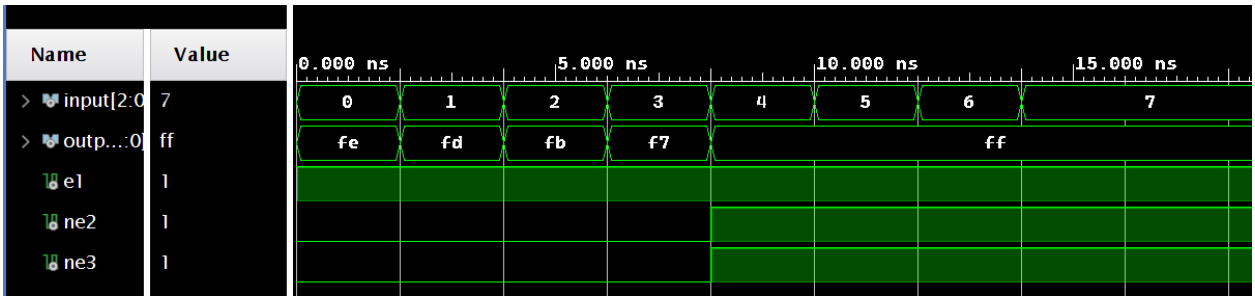
1 功能说明

输入引脚：input(3bit), e1, ne2, ne3

输入引脚：output(8bit)

当 e1, ne2, ne3 为 100 时，38 译码器使能，正常工作。

仿真结果



主要代码

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_arith.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;

entity decoder38_1 is
    port(
        e1 : in std_logic := '0';
        ne2 : in std_logic := '0';
        ne3 : in std_logic := '0';
        input: in std_logic_vector(2 downto 0);
        output: out std_logic_vector(7 downto 0));
end decoder38_1;

architecture Behavioral of decoder38_1 is
begin
    output<= "11111110" when input="000" and e1 = '1' and ne2 = '0' and ne3 = '0'
        else "11111101" when input="001" and e1 = '1' and ne2 = '0' and ne3 = '0'
        else "11111011" when input="010" and e1 = '1' and ne2 = '0' and ne3 = '0'
        else "11110111" when input="011" and e1 = '1' and ne2 = '0' and ne3 = '0'
        else "11101111" when input="100" and e1 = '1' and ne2 = '0' and ne3 = '0'
        else "11011111" when input="101" and e1 = '1' and ne2 = '0' and ne3 = '0'
        else "10111111" when input="110" and e1 = '1' and ne2 = '0' and ne3 = '0'
        else "01111111" when input="111" and e1 = '1' and ne2 = '0' and ne3 = '0'
        else "11111111";
end Behavioral;
```