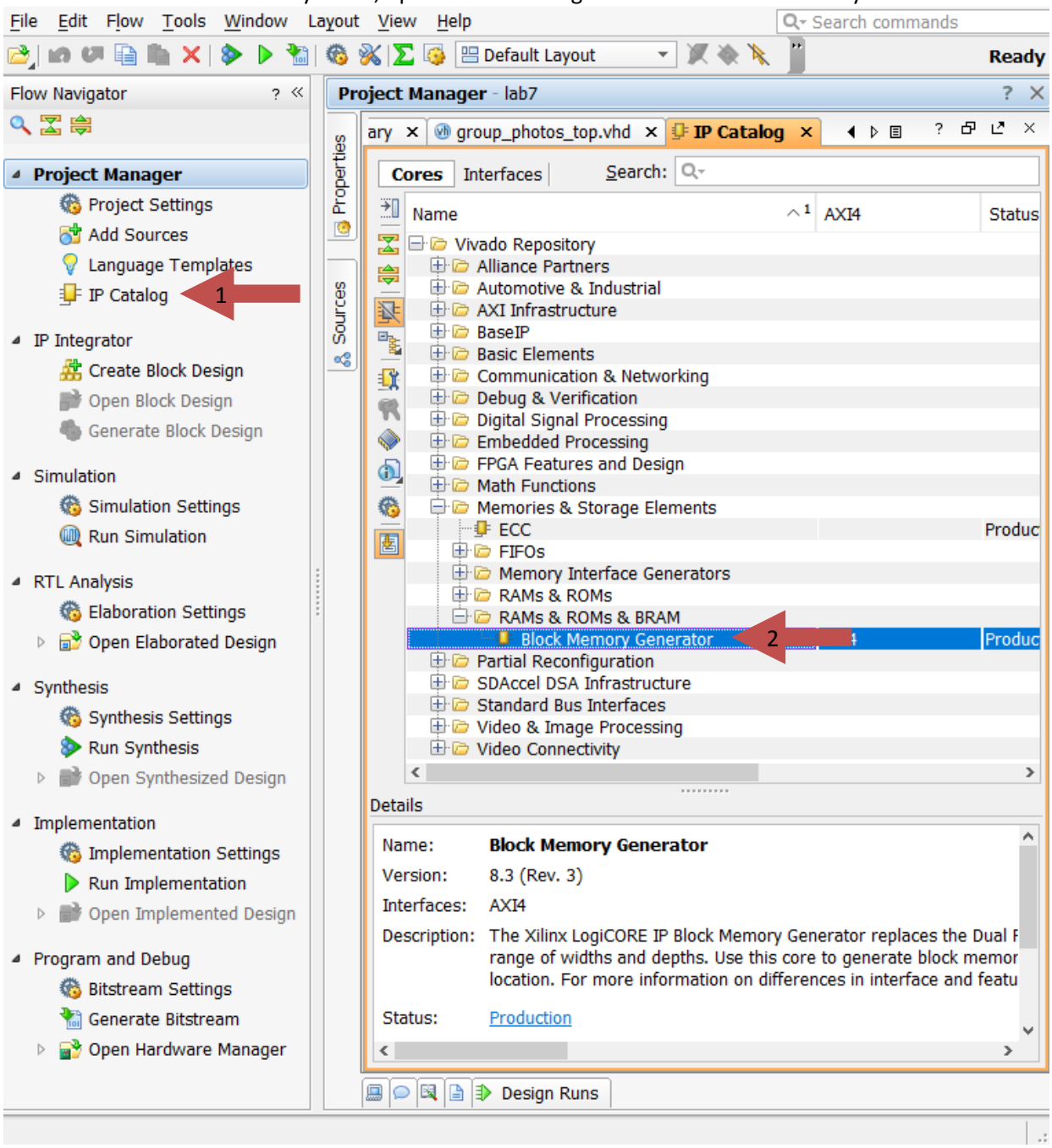
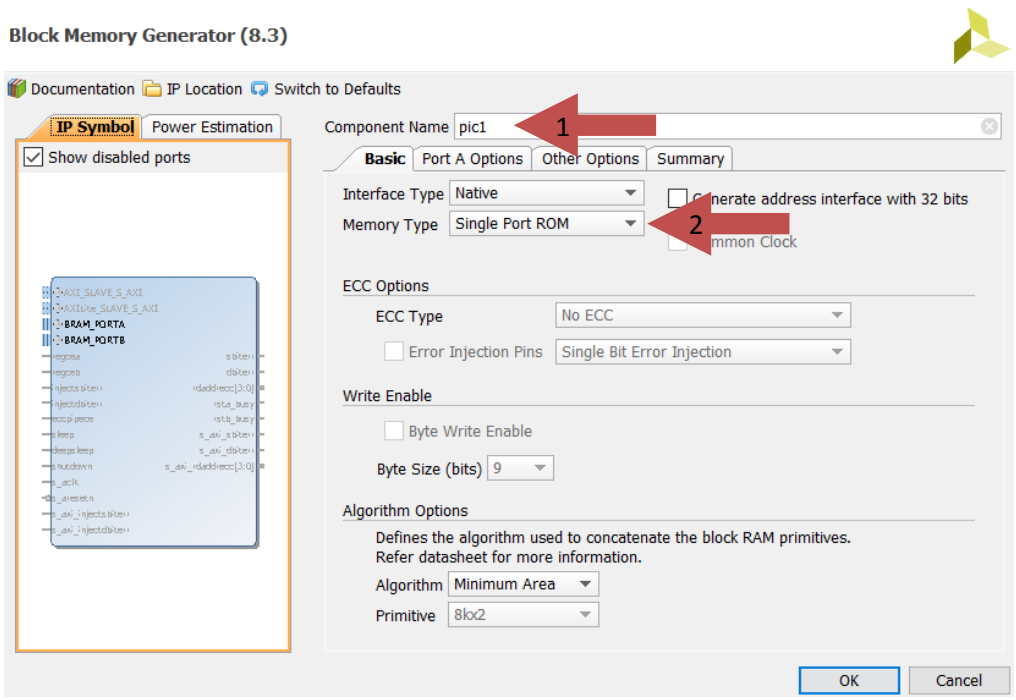
Creating Block Memory IP

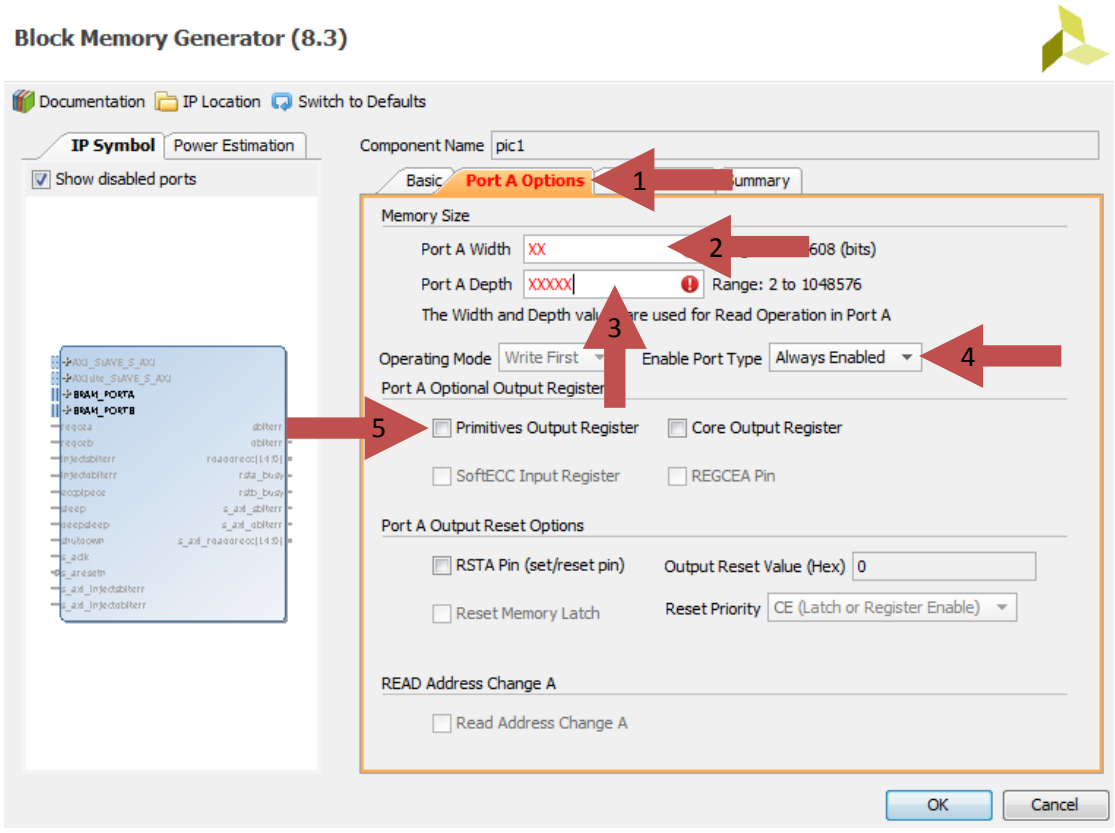
To store our images, we will create use the block memory on the FPGA. We need to create an IP core in order to use the block memory. First, open the IP Catalog and find the Block Memory Generator.

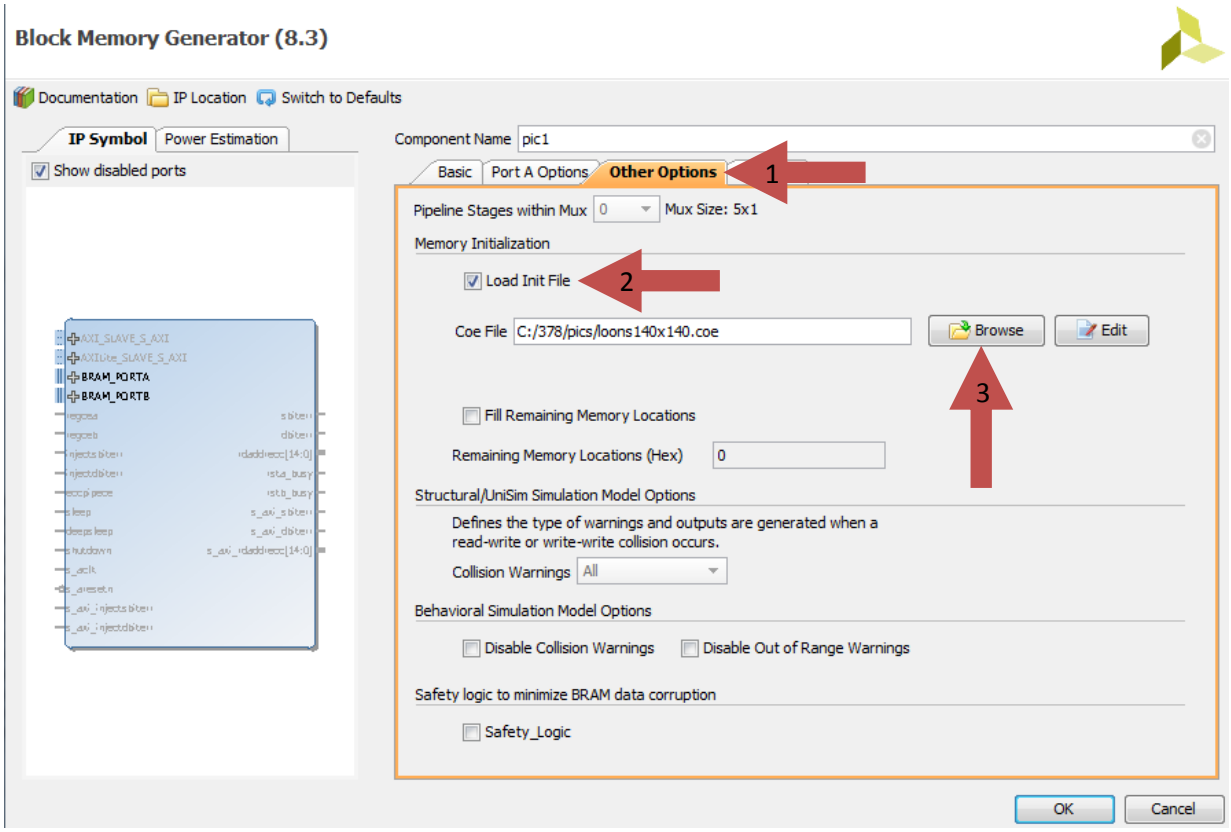


Then in the window that pops up give the IP a name and change it to a single-port ROM. This will remove the data input bus and the second port since we don't need them.

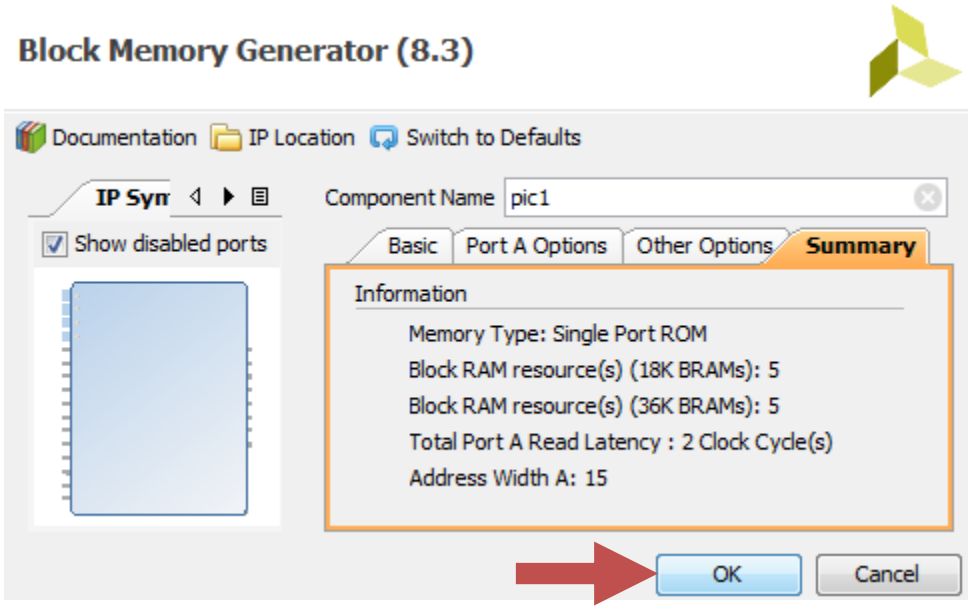


Then select the Port A Options tab. Change the Port Width to be 8 or 12, depending on whether you used img2coe8.m to produce an 8-bit color image or img2coe12.m to produce a 12-bit color image. Then change the Port Depth to match the number of pixels required. Finally, set the port to Always Enabled and disable the output register.

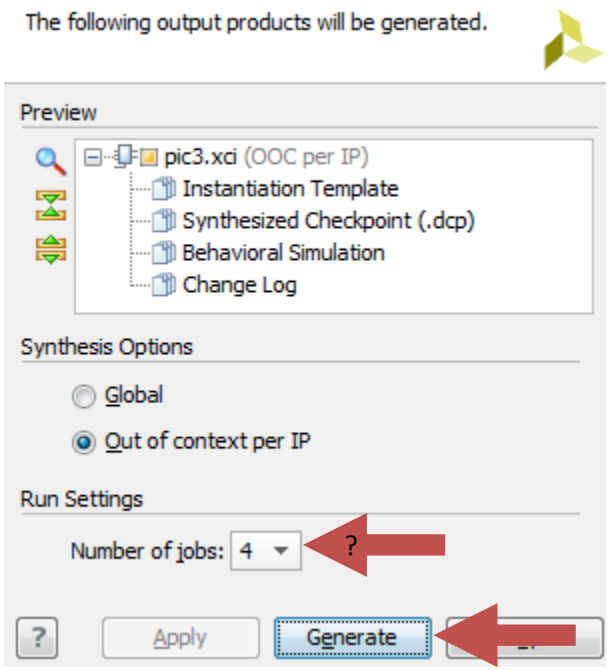




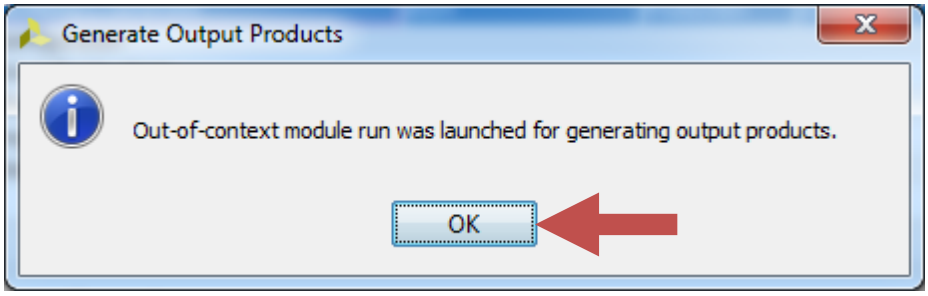
The last tab shows how many block RAMs (BRAMs) will be used by this memory and the width of the address bus required. For reference, the Artix 7 FPGA on the Nexys 4 board (XC7S100) has 120 36k BRAMs.



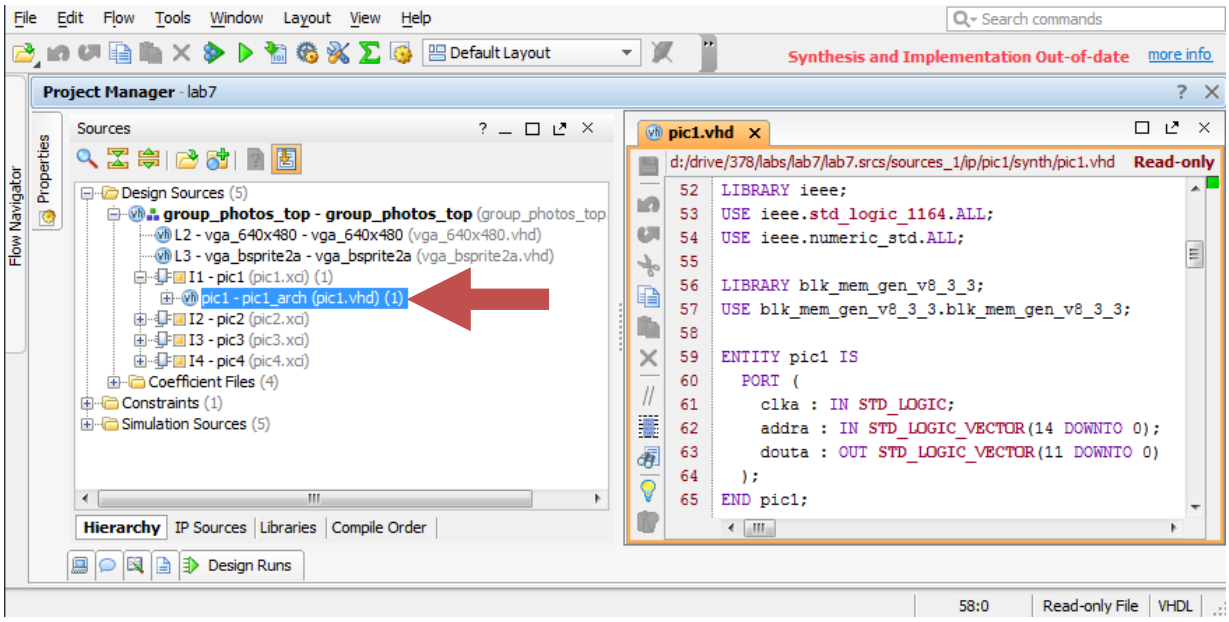
Now a window will pop-up to generate the IP core. You can change the number of jobs to be the same number of cores on your machine if you will be generating more ROMs after this one so the generations run in parallel.



Press OK on the pop-up window telling you that a synthesis run has been started for your ROM. This takes about 2 minutes to complete per ROM on a moderately-powered desktop.



To find the Entity so you know what the component declaration should be, expand the ROM and open the top VHD file. You can use this information to port-map the ROM into your design.



That's it! Now you can repeat these steps for as many ROMs as you need.