Outline of Final Report
ECE/CSI 4710 / 5710

The final written report should include the following:

1. A title page containing a **group photo** with names of all group members.

2. A Table of Contents

3. An Abstract
   A single paragraph that describes the overall project and the results, biggest challenges and how you overcame them.

4. An Introduction
   Describe the overall problem and the constraints of the design. Include an outline of the rest of the report.

5. A section that describes the top-level design
   Describe any alternate design choices for all sub-systems and justify the choices that you made.

6. A section that describes the details of your VHDL design. Include clear figures of all datapaths and state diagrams where appropriate. Include a block diagram of your top-level design.

7. A section that describes the overall performance of the project, the biggest challenges that you had to overcome and how you overcame them, and future improvements/features that could be added.

8. A Conclusion

9. List of References

Upload 2 files:

1. **the entire report in a single Word .DOCX file**
2. **the entire report in a PDF file**