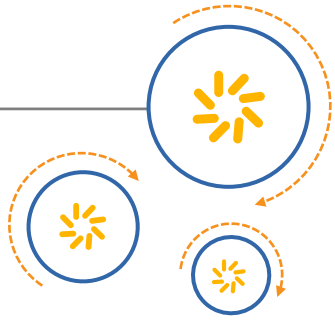
Qualcomm Atheros, Inc.



QCA9886 Single-Band 2x2 with 2 SS MIMO 802.11 a/n/ac WLAN SoC

Device Specification

80-Y9735-1 Rev. F

July 25, 2016

Qualcomm Atheros, Inc.
1700 Technology Drive
San Jose, CA 95110
U.S.A.

Revision history

Revision	Date	Description
A	July 2015	Initial version
B	October 2015	Updated Chapter 1.2 RF Features, Interfaces
		Added new Chapter 3.
C	October 2015	Updated Chapter 1.2 WLAN features
D	March 2016	■ Updated Chapter 1.1 with support for internal LNAs ■ Updated Chapter 1.2 with 40 MHz clock support ■ Added Chapter 3.5 Radio Characteristics ■ Added Chapter 3.6 Power Consumption Parameters ■ Added Chapter 4.5 Thermal Characteristics ■ Added Chapter 7 Part Reliability
E	June 2016	■ Updated description for AOVDD11
F	July 2016	■ Removed support for 48 MHz crystal ■ Updated Table 3-2

Contents

1 Introduction 7
- 1.1 General Description 7
- 1.2 Features 7
- 1.3 High-level System Diagram 9
- 1.4 Functional Specification 10
  - 1.4.1 Functional Block Diagram 10
  - 1.4.2 GPIO 11

2 Pin Descriptions 13

3 Electrical Characteristics 19
- 3.1 Absolute Maximum Ratings 19
- 3.2 Recommended Operating Conditions 20
- 3.3 GPIO DC Electrical Characteristics 20
- 3.4 Power Up Sequencing 21
- 3.5 Radio Characteristics 22
  - 3.5.1 Receiver Characteristics 22
  - 3.5.2 Transmitter Characteristics 24
  - 3.5.3 Synthesizer Characteristics 26
- 3.6 Power Consumption Parameters 26

4 Mechanical Information 27
- 4.1 Device Physical Dimensions 28
- 4.2 Part Marking 31
- 4.3 Device Ordering Information 32
- 4.4 Device Moisture-sensitivity Level 33
- 4.5 Thermal Characteristics 33

5 Carrier, Storage, and Handling 34
- 5.1 Carrier 34
  - 5.1.1 Tape and Reel Information 34
  - 5.1.2 Matrix Tray Information 35
- 5.2 Storage 36
  - 5.2.1 Bagged Storage Conditions 36
  - 5.2.2 Out-of-bag Duration 36

5.3 Handling 36
5.3.1 Baking 36
5.3.2 Electrostatic Discharge 36

6 PCB Mounting Guidelines 37
6.1 RoHS Compliance 37
6.2 SMT Parameters 37
6.2.1 Land Pad and Stencil Design 37
6.2.2 Reflow Profile 37
6.2.3 SMT Peak Package-body Temperature 38
6.2.4 SMT Process Verification 39
6.3 Board-level Reliability 39

7 Part Reliability 40
7.1 Reliability qualification summary 40
7.2 Qualification Sample Description 41

Figures

Figure 1-1 QCA9886 Block Diagram 9
Figure 1-2 QCA9886 Functional Block Diagram 10
Figure 2-1 Package Pinout (See-Through Top View) 14
Figure 3-1 QCA9886 Power Up Sequencing 21
Figure 4-1 QCA9886 Package A Details 28
Figure 4-2 QCA9886 Package B Details 30
Figure 4-3 QCA9886 Marking (top view, not to scale) 31
Figure 4-4 Device Identification Code 32
Figure 5-1 Tape Orientation on Reel 34
Figure 5-2 Part Orientation in Tape 35
Figure 5-3 Matrix Tray Part Orientation 35
Figure 6-1 Typical SMT Reflow Profile 38

Tables

Table 1-1 Functional blocks 10
Table 1-2 GPIO 11
Table 2-1 Signal to Pin Relationships and Descriptions 14
Table 2-2 External Switch Control/GPIO Pins 16
Table 2-3 Power and Ground Pins 17
Table 3-1 Absolute maximum ratings 19
Table 3-2 Recommended Operating Conditions 20
Table 3-3 GPIO DC Electrical Characteristics 20
Table 3-4 PCIE Interface Timing Parameters 21
Table 3-5 Rx Characteristics for 5 GHz Operation 22
Table 3-6 Rx Impedance Characteristics for 5 GHz Operation 23
Table 3-7 Tx Characteristics for 5 GHz Operation 24
Table 3-8 Tx Impedance Characteristics for 5 GHz Operation 25
Table 3-9 Synthesizer Composite Characteristics for 5-GHz Operation 26
Table 3-10 Power consumption for 5 GHz operation (VHT20) 26
Table 3-11 Power consumption for 5 GHz operation (VHT40) 26
Table 3-12 Power consumption for 5 GHz operation (VHT80) 26
Table 4-1 Package A Dimensions 29
Table 4-2 Package B Dimensions 30
Table 4-3 QCA9886 Marking Line Definitions 31
Table 4-4 QCA9886 Order Numbers 32
Table 4-5 Thermal Resistance 33
Table 6-1 Typical SMT Reflow Profile Conditions (for reference only) 38
Table 7-1 Reliability Evaluation Results 40
Table 7-2 QCA9886 characteristics 41

1 Introduction

1.1 General Description

The QCA9886 with Qualcomm® VIVE™ 802.11ac technology is a highly integrated wireless local area network (WLAN) system-on-chip (SoC) for 5 GHz 802.11ac WLAN applications. The QCA9886 includes a CPU, memory for WLAN Media Access Layer (MAC), Physical Layer (PHY) management and provides host offload of other high-level networking tasks. It enables high-performance 2x2 MU-MIMO with 2 spatial streams for wireless applications demanding a robust link quality and maximum throughput and range. The QCA9886 integrates a multi-protocol MAC, PHY, analog-to-digital/digital-to-analog converters (ADC/DAC), 2x2 MU-MIMO radio transceivers, and PCIE interface in an all-CMOS device for low power consumption and small form-factor applications.

The QCA9886 implements half-duplex OFDM supporting 867 Mbps for 802.11ac 80 MHz channel operation in 5 GHz mode and IEEE 802.11a/n/ac data rates. Additional features include 802.11ac explicit transmit beamforming (TxBF), 802.11 compatible implicit TxBF, multi-user MIMO (MU-MIMO), Dynamic Bandwidth Switching, Per Packet Switching between 2SS/80 MHz, Maximal Likelihood (ML) decoding, Low-Density Parity Check (LDPC), Maximal Ratio Combining (MRC), Space Time Block Code (STBC), and On-Chip One-Time Programmable (OTP) memory to eliminate the need for an external flash and to further reduce the external component count and BOM cost. The QCA9886 supports 802.11 wireless MAC protocol, 802.11i security, Wi-Fi offload, error recovery, and 802.11e quality of service (QoS).

The QCA9886 supports up to two simultaneous spatial streams integrating two Tx and two Rx chains for high throughput and extended coverage. Tx chains combine PHY in-phase (I) and quadrature (Q) signals, convert them to the desired frequency and drive the RF signal through internal or external power amplifiers (PAs). Rx chains receive from antennas through internal or external LNAs. The frequency synthesizer supports 1-MHz steps to match frequencies defined by IEEE 802.11a/n/ac specifications. The QCA9886 supports frame data transfer to and from the host using a PCIE interface that supports interrupt generation and reporting and status reporting. Other external interfaces include EEPROM and GPIOs.

1.2 Features

General

- 2x2 MU-MIMO technology improves effective throughput and range over existing 802.11a products
- Support for up to two spatial streams
- Support for 40 MHz
- 100-pin, 9 mm x 9 mm DRQFN package

WLAN

- Supports 20/40/80 MHz at 5 GHz
- Supports up to 256 QAM
- Data rates of up to 867 Mbps in 802.11ac 80 MHz channels using reduced (short) guard interval (GI)
- Multi-user MIMO (MU-MIMO) beamformer
- 802.11ac explicit transmit beamforming (TxBF) and legacy implicit TxBF for both beamformer and beamformee
- TCP and UDP checksum offload
- Dynamic bandwidth switching
- Dynamic frequency selection (DFS) in required 5-GHz bands when used as an AP
- Maximal likelihood (ML) decoding
- Supports spatial multiplexing, cyclic-delay diversity (CDD), low-density parity check (LDPC), maximal ratio combining (MRC), Space Time Block Code (STBC)
- AMSDU and AMPDU frame aggregation
- 802.11e-compatible bursting
- Digital predistortion
- Support for locationing (RSSI and RTT-based, 802.11REVmc compliant)

Supported Standards

- 802.11a/n/ac

CPU/Memory

- Integrated CPU for Wi-Fi offload with memory
- On-chip OTP memory

RF

- Support for internal/external PA
- Support for internal/external LNA

Security

- AES-CCMP at 128/256 bits
- AES-GCMP at 128/256 bits
- WEP, TKIP hardware encryption
- WAPI hardware encryption

Interfaces

- PCI Express 1.1 interface
- I^2C EEPROM support
- GPIOs
- JTAG for debugging and boundary scan
- MIPI RFFE

1.3 High-level System Diagram

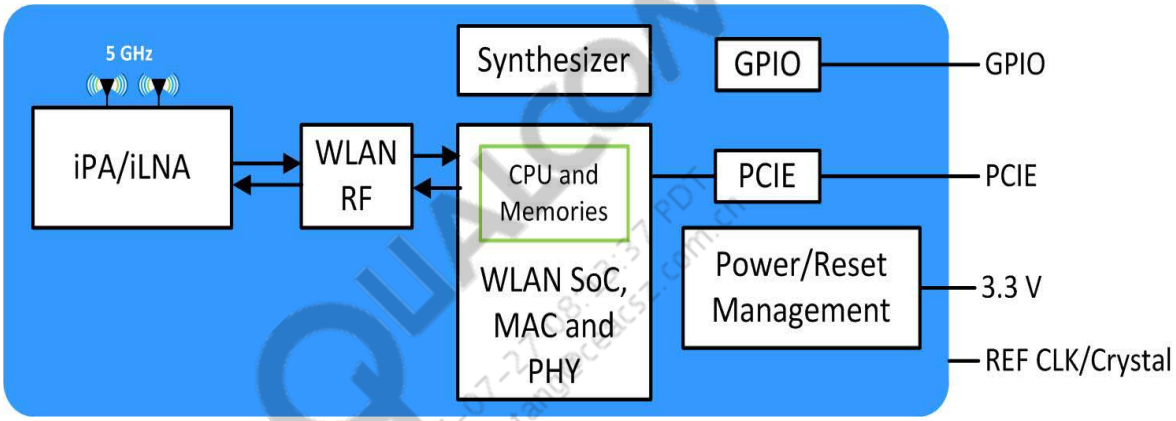


Figure 1-1 QCA9886 Block Diagram

1.4 Functional Specification

1.4.1 Functional Block Diagram

Figure 1-2 illustrates the QCA9886 functional block diagram.

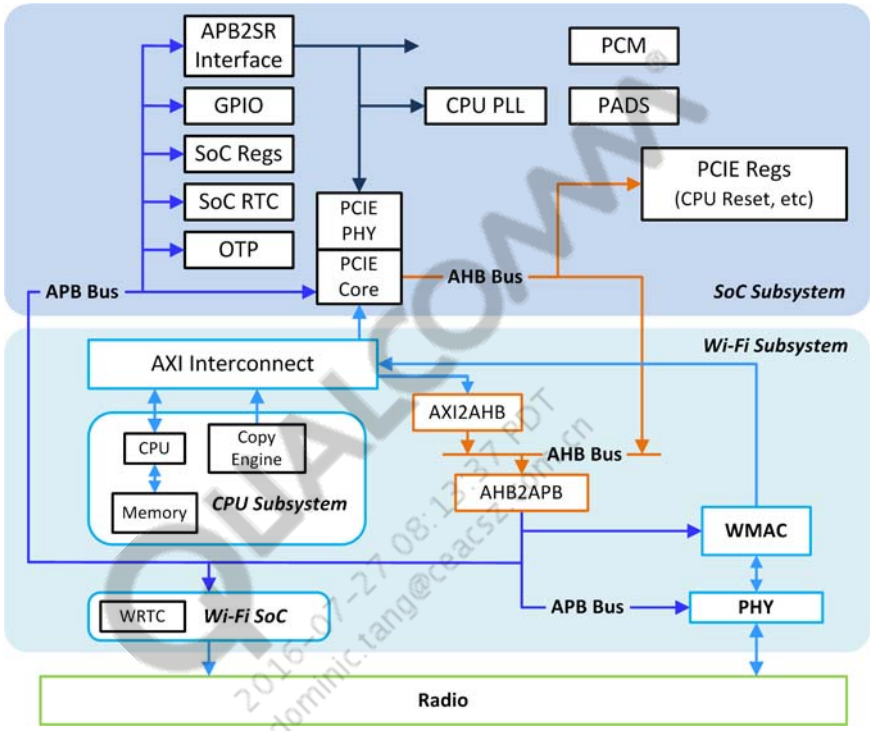


Figure 1-2 QCA9886 Functional Block Diagram

The QCA9886 is comprised of several internal functional blocks, as summarized in Table 1-1.

Table 1-1 Functional blocks

Block	Description
GPIOs	All digital pins map to 27 GPIOs. These GPIOs are used for a variety of purposes such as UART, I^2C, SPI, JTAG. See GPIO.
OTP	WLAN one-time programmable (OTP) memory
WRTC	Controls the clocks and power going to other modules within the chip. Its inputs consist of sleep requests from these modules and its outputs consists of clock enable signals used to gate the clocks going to these modules. This block also manages resets going to other modules within the device.

Table 1-1 Functional blocks (cont.)

Block	Description
AXI Interconnect	The AXI bus is accessed simultaneously by multiple masters in the PCIE host memory, CPU memory, and all programmable registers. The WLAN portion of the AXI fabric supports split transactions to achieve higher utilization on the PCIE bus. All register access from the CPU route through the AXI fabric. A bridge converts AXI requests to AHB requests, and the AHB arbiter selects between PCIE register access requests and CPU register access requests on a round-robin basis. All register accesses for all modules including the MAC, CE, and blocks such as GPIOs, RTC, or OTP use the APB protocol. A bridge converts AHB requests into APB. It must be noted here that the entire AXI fabric, AHB, and APB interfaces all run synchronously on the SoC clock domain. See GPIO.
Copy Engine	The copy engine establishes a communication channel between firmware and the host. It performs a DMA copy from source memory to destination memory, and it can perform this DMA copy operation in a batch under software control. A copy involves a read operation from the source memory, followed by a write operation to the destination memory.
CPU Core and Memory Controller	The CPU is a Tensilica XTENSA LX2 processor with a hardware abstraction layer (HAL) to support low level WLAN activity with minimal support from the PCIE host. The CPU is configured with a peripheral interface (PIF). The outbound PIF is used by the CPU for register access. The inbound PIF is used by the other AXI masters (MAC and CE) to access the data memory (DMEM) connected to the CPU.
WMAC/PHY/Radio	The integrated 5 GHz 802.11ac MAC/PHY/radio includes the features of maximal likelihood (ML) decoding, low-density parity check (LDPC), and maximal ratio combining (MRC). The MAC supports A-MSDU scatter and gather, L2 header encapsulation and decapsulation, IP/TCP/UDP checksum, and Rx classification.
PCIE Registers	The QCA9886 PCIE configuration space also maps to the host memory space. Most programmable registers can be accessed either by the host over PCIE or by the internal CPU over AHB. Some additional registers are accessible only by the host over PCIE. These registers run on the PCIE clock domain, allowing the PCIE host to determine the sleep status of the SoC and to wake up the SoC if needed.
PCIE Core/ PCIE PHY	All programmable registers can be accessed by either the PCIE host or by the internal CPU. The PCIE core provides a simple proprietary interface for register accesses.

1.4.2 GPIO

The QCA9886 provides 27 configurable bi-directional general purpose I/O ports. Each GPIO port can be configured independently as input or output using the GPIO control registers. The GPI/GPIOs are used for a variety of purposes such as UART, I^2C, SPI, JTAG, and so on.

Most GPIOs have normal mode functionality as well as test-mode functionality. GPIO mapping is shown in Table 1-2. On reset bootstrap values are sampled. Global test mode is on GPIO_5. If this pin is sampled high during initialization, the chip enters test mode.

Table 1-2 GPIO

Pin	Name	Functional Alternate	Description
B9	GPIO_0	GPIO	General purpose I/O
A11	GPIO_1	GPIO	
A12	GPIO_2	GPIO	
B11	GPIO_3	GPIO	
A13	GPIO_4	GPIO	

Table 1-2 GPIO

Pin	Name	Functional Alternate	Description
A14	GPIO_5	GPIO	General purpose I/O
B13	GPIO_6	SWCOM2	External antenna select
A19	GPIO_7	SWCOM3	External antenna select
B15	GPIO_8	SWCOM4	External antenna select
A20	GPIO_9	SWCOM5	External antenna select
B23	GPIO_11	GPIO	General purpose I/O
B22	GPIO_12	GPIO	
A28	GPIO_13	GPIO	
B24	GPIO_14	GPIO	
B29	GPIO_16	GPIO	
A37	GPIO_17	GPIO	
A38	GPIO_18	GPIO	
B31	GPIO_19	EEPROM_PROT	EEPROM protection
A40	GPIO_20	I2C_SDA	I2C data
B33	GPIO_21	GPIO	General purpose I/O
B34	GPIO_22	I2C_CLK	I2C clock
A42	GPIO_23	GPIO	General purpose I/O
A43	GPIO_24	GPIO	
B36	GPIO_25	GPIO	
A45	GPIO_26	GPIO	
A46	GPIO_32	SWCOM0	External Tx/Rx switch control
B39	GPIO_33	SWCOM1	External Tx/Rx switch control

2 Pin Descriptions

This section contains both a package pinout and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
IO	A digital bidirectional signal
OA	An analog output signal
OD	An open-drain digital output signal
O	A digital output signal
P	A power or ground signal

Figure 2-1 shows the QCA9886 pinout.

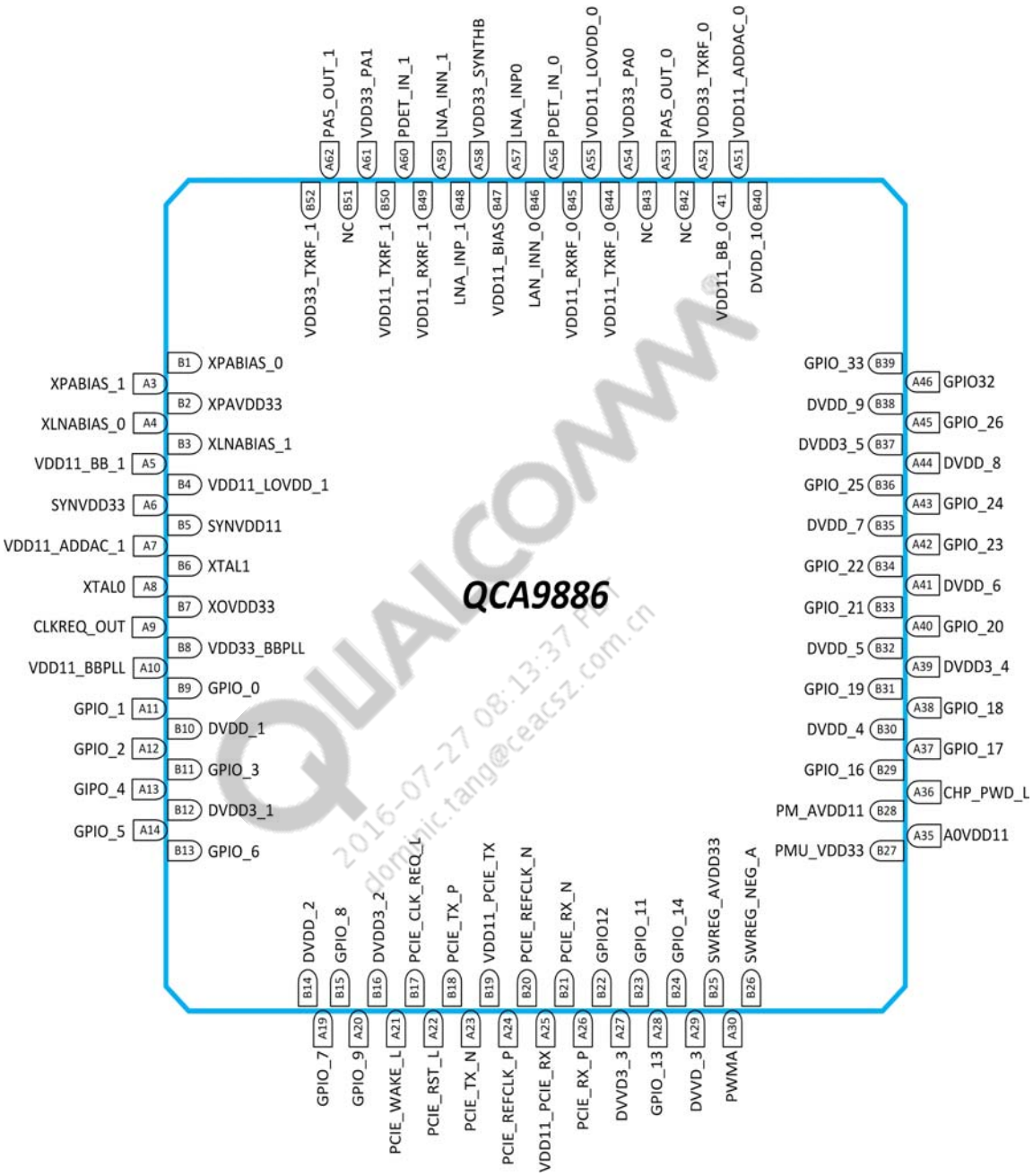


Figure 2-1 Package Pinout (See-Through Top View)

Table 2-1 provides the signal-to-pin relationship information for the QCA9886.

Table 2-1 Signal to Pin Relationships and Descriptions

Signal Name	Pins	Type	Description
Clock			
XTALI	B6	—	40 MHz crystal
XTALO	A8	—	

Table 2-1 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pins	Type	Description
CLKREQ_OUT	A9	—	Reference clock request signal
Radio			
LNA5_INp_0	A57	IA	5 GHz LNA differential input pair for chain 0
LNA5_INp_0	B46	IA	
LNA5_INp_1	B48	IA	5 GHz LNA differential input pair for chain 1
LNA5_INn_1	A59	IA	
PA5_OUT_0	A53	OA	5 GHz PA single-ended output
PA5_OUT_1	A62	OA	
PDET_IN0	A56	IA	PDET input 5 GHz
PDET_IN1	A60	IA	
Analog Interface			
XPABIAS_0	B1	OA	5 GHz external PA bias at 3.3 V
XPABIAS_1	A3	OA	
XLANBIAS_0	A4	O	5 GHz external LNA control, 12 mA
XLANBIAS_1	B3	O	
PCI Express Endpoint			
PCIE_TX_N	A23	OA	Differential transmit
PCIE_TX_P	B18	OA	
PCIE_RX_N	B21	IA	Differential receive
PCIE_RX_P	A26	IA	
PCIE_REFCLK_N	B20	IA	Differential reference clock (100 MHz)
PCIE_REFCLK_P	A24,	IA	
PCIE_RST_L	A22	I	PCIE reset
PCIE_CLK_REQ_L	B17	OD	PCIE reference clock requests; open drain. An external pull up resistor to 3.3 V is required. Drive strength 16 mA.
PCIE_WAKE_L	A21	OD	PCIE request to service a function-initiated wake event; open drain. An external pull up resistor to 3.3 V is required. Drive strength 16 mA.

Table 2-2 External Switch Control/GPIO Pins

Signal Name	Pins	Type	Description
GPIO_0	B9	IO	General purpose IO, programmable, can be used as JTAG, SPI, UARTs, LED control. ■ GPIO_6, GPIO_7, GPIO_8, GPIO_9, GPIO_32, and GPIO_33 are multiplexed pins that default to the antenna switch control (SWCOM) interface. ■ GPIO_6 through GPIO_9 and GPIO_32 GPIO_33 use a 16 mA driven strength. ■ Other GPIO use an 8 mA drive strength. Default input pins can be grounded, and default output pins can be left open if not used. See Table 1-2 on page 11.
GPIO_1	A11	IO	
GPIO_2	A12	IO	
GPIO_3	B11	IO	
GPIO_4	A13	IO	
GPIO_5	A14	IO	
GPIO_6	B13	IO	
GPIO_7	A19	IO	
GPIO_8	B15	IO	
GPIO_9	A20	IO	
GPIO_11	B23	IO	
GPIO_12	B22	IO	
GPIO_13	A28	IO	
GPIO_14	B24	IO	
GPIO_16	B29	IO	
GPIO_17	A37	IO	
GPIO_18	A38	IO	
GPIO_19	B31	IO	
GPIO_20	A40	IO	
GPIO_21	B33	IO	
GPIO_22	B34	IO	
GPIO_23	A42	IO	
GPIO_24	A43	IO	
GPIO_25	B36	IO	
GPIO_26	A45	IO	
GPIO_32	A46	IO	
GPIO_33	B39	IO	

Table 2-3 Power and Ground Pins

Symbol	Pin	Description
Power		
DVDD_1	B10	1.1 V supply[1]
DVDD_2	B14	
DVDD_3	A29	
DVDD_4	B30	
DVDD_5	B32	
DVDD_6	A41	
DVDD_7	B35	
DVDD_8	A44	
DVDD_9	B38	
DVDD_10	B40	
DVDD3_1	B12	3.3 V supply
DVDD3_2	B16	
DVDD3_3	A27	
DVDD3_4	A39	
DVDD3_5	B37	
RF Power		
AVDD11		1.1 V supply[1]
ADDACVDD11_0	A51	1.1 V supply for ADC/DAC
ADDACVDD11_1	A7	
BBVDD11_0	B41	1.1 V supply Tx/Rx BB FLTs
BBVDD11_1	A5	
VDD33_PA0	A54	3.3 V supply for PA chain 0
VDD33_PA1	A61	3.3 V supply for PA chain 1
BBPLLVDD33	B8	3.3 V supply for BB PLL
BBPLLVDD11	A10	1.1 V supply for BB PLL
LOVDD11_0	A55	1.1 V supply for LO
LOVDD11_1	B4,	
RXRFVDD11_0	B45	1.1 V supply for Rx RF
RXRFVDD11_1	B49	
TXRFVDD11_0	B44	1.1 V supply for Tx RF
TXRFVDD11_1	B50	
TXRFVDD33_0	A52	3.3 V supply for Tx RF
TXRFVDD33_1	B52	
XOVDD33	B7	3.3 V supply for XO

Table 2-3 Power and Ground Pins (cont.)

Symbol	Pin	Description
SYNVDD11	B5	1.1 V supply for synth
VDD11_BIAS	B47	1.1 V supply for bias
SYNVDD33	A6	3.3 V supply for synth
VDD33_SYNTHB	A58	3.3 V supply for synth
PCIE Power		
VDD11_PCIE_TX	B19	1.1 V supply for PCIE PHY Tx
VDD11_PCIE_RX	A25	1.1 V supply for PCIE PHY Rx
Voltage Regulators		
CHP_PWD_L	A36	Chip power down control Must be de-asserted after both 3.3 V power and 1.1 V power become stable.
PMU_VDD33	B27	3.3 V supply for PMU
SWREG_AVDD33	B25	3.3 V power input to the voltage regulator. Should be connected to GND.
SWREG_NEG_A	B26	voltage regulator ground
AOVDD11	A35	LDO output pin. Only connect to decoupling capacitor for internal LDO
PM_AVDD11	B28	Feedback from the voltage regulator. Connect o 1.1 V rail.
PWMA	A30	Voltage regulator switching outputs. Leave floating.
Ground Pad		
NC	B42, B43,B51	No connection

1. When using external regulator, both AVDD_*n* and DVDD11 must be powered from a single regulator. The minimum current rating of regulator is1 A. The external regulator tolerance requirement is +5%/-3%.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the QCA9886.

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document is not recommended.

Table 3-1 Absolute maximum ratings

Symbol	Parameter		Max Rating	Unit
DVDD_*,	Supply from external digital regulator voltage		-0.3 to 1.21	V
AVDD11, ADDACVDD11_*, BBVDD11_*, LOVDD11_*, RFRXVDD11_*, TXRFVDD11_*,	Supply from external analog regulator voltage			
VDD11_PCIE_TX	PCIE PHY Tx supply			
VDD11_PCIE_RX	PCIE PHY Rx supply			
PMU_VDD33	Maximum supply for PMU		-0.3 to 3.63	V
DVDD3_*	Digital I/O voltage			
BBPLLVDD33, VDD33_PA0, VDD33_PA1, TXRFVDD33_0, TXRFVDD33_1, XOVDD33	Analog I/O voltage			
PCIE_VDDH	PCIE PHY I/O			
RF_{in}	Maximum RF input (reference to 50 Ω)		+10	dBm
T_{store}	Storage temperature		-60 to 150	°C
T_j	Junction temperature		125	°C
ESD	Electrostatic discharge tolerance	HBM	2000	V
		CDM	500	

3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DVDD_*,	Supply from external digital regulator voltage	—	—	1.13	—	V
AVDD11, ADDACVDD11_*, BBVDD11_*, LOVDD11_*, RFRXVDD11_*, TXRFVDD11_*,	Supply from external analog regulator voltage	±5%	1.073	1.13	1.187	V
DVDD3_*	Digital I/O voltage	±5%	3.135	3.3	3.465	V
BBPLLVDD33, VDD33_PA0, VDD33_PA1, TXRFVDD33_0, TXRFVDD33_1, XOVDD33	Analog I/O voltage	±5%	3.135	3.3	3.465	V
VDD11_PCIE_TX	PCIE PHY Tx supply	±5%	1.073	1.13	1.187	V
VDD11_PCIE_RX	PCIE PHY Rx supply	±5%	1.073	1.13	1.187	V
T_{case}	Commercial case temperature	—	0	—	110	°C
	Industrial case temperature	—	-40	—	110	°C

3.3 GPIO DC Electrical Characteristics

Table 3-3 lists the GPIO DC electrical characteristics, with: T_a = 25 °C

Table 3-3 GPIO DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	0.7 * V_{DD33}	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	0.3 * V_{DD33}	V
V_{OH}	High Level Output Voltage	—	0.9 * V_{DD33}	—	—	V
V_{OL}	Low Level Output Voltage	—	0	—	0.1 * V_{DD33}	V

3.4 Power Up Sequencing

Figure 3-1 depicts the required reset sequence for the QCA9886 PCIE interface. Table 3-4 shows the QCA9886 PCIE interface timing parameters.

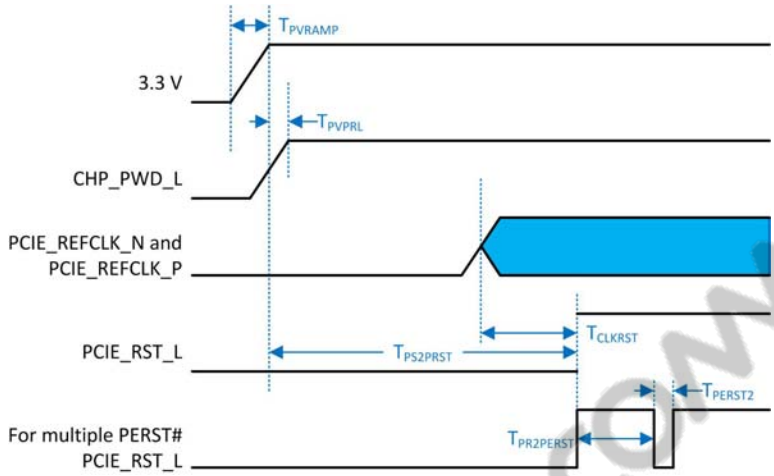


Figure 3-1 QCA9886 Power Up Sequencing

Table 3-4 PCIE Interface Timing Parameters

Symbol	Parameter	Min	Max	Unit
T_{PVRAMP}	Power supply ramp on 3.3 V	—	25	ms
T_{PVPRL}	Power valid to RESET_L asserted	0[1]	—	µs
T_{PRCLK}	RESET_L deasserted to PCIE_REFCLK_N and PCIE_REFCLK_P stable	100	—	µs
T_{CLKRST}	PCIE_REFCLK_N and PCIE_REFCLK_P stable to PCIE_RST_L deasserted	100[2]	—	µs
$T_{PS2PRST}$	Power supply stable to PCIE_RST_L deassert	10[3]	—	ms
$T_{PR2PERST}$	Initial PCIE_RST_L deassert to subsequent multiple PCIE_RST_L	40	—	ms
T_{PERST2}	Subsequent PCIE_RST_L asserted for multiple PCIE_RST_L	1	—	ms

1. When using an external voltage regulator, CHP_PWD_L must be deasserted after both 3.3 V power and 1.13V power have become stable.
2. This timing depends on hardware interface designs, such as Express Card, PCIE Mini Card, or PCIE desktop applications. The system must follow PCIE specifications, as well as TCLKRST.
3. $T_{PS2PRST}$ minimum timing must be observed.

3.5 Radio Characteristics

The following conditions apply to the typical per chain characteristics unless otherwise specified:

V_{DD11} = 1.13 V, V_{DD33} = 3.3V, T_{amb} = 25 °C

3.5.1 Receiver Characteristics

See Table 3-5 for QCA9886 receiver characteristics:

Table 3-5 Rx Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range	5 MHz center frequency	5.18	—	5.825	GHz
NF	Receive chain noise figure (max gain)	See Note 1	—	5.0	—	dB
S_{rf}	Sensitivity					
	OFDM, 6 Mbps	See Note 2	-82	-91	—	dBm
	OFDM, 54 Mbps		-65	-76	—	
	HT20, MCS0, 1 stream, 1 Tx, 1 Rx		-82	-91	—	
	HT20, MCS7, 1 stream, 1 Tx, 1 Rx		-64	-73	—	
	HT40, MCS0, 1 stream, 1 Tx, 1 Rx		-79	-89	—	
	HT40, MCS7, 1 stream, 1 Tx, 1 Rx		-61	-70	—	
	VHT20, MCS0, 1 stream, 1 Tx, 1 Rx		-82	-93	—	
	VHT20, MCS8, 1 stream, 1 Tx, 1 Rx		-59	-70	—	
	VHT40, MCS0, 1 stream, 1 Tx, 1 Rx		-79	-90	—	
	VHT40, MCS9, 1 stream, 1 Tx, 1 Rx		-54	-67	—	
	VHT80, MCS0, 1 stream, 1 Tx, 1 Rx		-76	-86	—	
	VHT80, MCS9, 1 stream, 1 Tx, 1 Rx		-51	-63	—	
	VHT20, MCS10, 2 stream, 2Tx, 2 Rx		-82	-92	—	
	VHT20, MCS18, 2 stream, 2Tx, 2 Rx		-59	-69	—	
	VHT40, MCS10, 2 stream, 2 Tx, 2 Rx		-79	-89	—	
	VHT40, MCS19, 2 stream, 2 Tx, 2 Rx		-54	-66	—	
	VHT80, MCS10, 2 stream, 2 Tx, 2 Rx		-76	-86	—	
	VHT80, MCS19, 2 stream, 2 Tx, 2 Rx		-51	-62	—	
IP1dB	Input 1 dB compression (min. gain)	—	—	—	—	dBm
IIP3	Input third intercept point (min. gain)	—	—	-42	—	dBm

Table 3-5 Rx Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{adj}	Adjacent channel rejection					
	11a OFDM, 6 Mbps	See Note 3	16	26	—	dB
	11a OFDM, 54 Mbps		-1	9	—	
	HT20, MCS0		16	26	—	dB
	HT20, MCS15		-2	8	—	
	HT40, MCS0		16	27	—	dB
	HT40, MCS15		-2	9	—	
	VHT20, MCS0, 1 stream		16	25	—	dB
	VHT20, MCS15, 2 stream		-7	3	—	
	VHT40, MCS0, 1 stream		16	26	—	dB
	VHT40, MCS15, 2 stream		-9	3	—	
	VHT80, MCS0, 1 stream		16	24	—	dB
	VHT80, MCS9, 2 stream		-9	2	—	

1. For improved sensitivity performance, an external LNA may be used.
2. Sensitivity performance based on Qualcomm Atheros reference design, which includes Tx/Rx antenna switch with LDPC enabled. Minimum values based on IEEE 802.11 specifications.
3. Typical values measured with reference design. Minimum values based on IEEE 802.11 specifications.

Table 3-6 Rx Impedance Characteristics for 5 GHz Operation

Symbol	Parameter	Description	Typ		Unit
Z_{RFin_input}	Recommended LNA differential drive impedance	**Chain0**	P	N	Ω
		5180	7.5389+j96.065	7.4737+j103.89	
		5500	2.3706+j102.10	1.9368+j107.39	
		5825	2.8788+j115.25	2.5590+j121.47	
		Chain1	P	N	
		5180	7.3946+j71.554	7.0783+j74.824	
		5500	4.9877+j80.302	4.0185+j80.900	
		5825	4.6907+j90.134	3.9774+j89.356	

3.5.2 Transmitter Characteristics

See Table 3-7 for the QCA9886 transmitter characteristics:

Table 3-7 Tx Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	20 MHz center frequency	5.18	—	5.825	GHz
P_{out}	Mask compliant output power					
	6M	See Note 1	—	19	—	dBm
	VHT20 MCS0		—	19	—	dBm
	VHT40 MCS0		—	19	—	dBm
	VHT80 MCS0		—	18	—	dBm
	EVM compliant output power					
	802.11a, 54 Mbps - single Tx chain	See Note 1	—	18	—	dBm
	802.11n, MCS7, HT20 - single Tx chain		—	17	—	dBm
	802.11n, MCS7, HT40 - single Tx chain		—	17	—	dBm
	802.11ac, MCS8, VHT20 - single Tx chain		—	16	—	dBm
	802.11ac, MCS9, VHT40- single Tx chain		—	15	—	dBm
	802.11ac, MCS9, VHT80 - single Tx chain		—	15	—	dBm
SP_{gain}	PA gain step	See Note 2	—	0.25	—	dB
A_{pl}	Accuracy of power leveling loop	See Note 3	—	±2	—	dB
SS	Sideband suppression	—	—	-35	—	dBc
LO_{leak}	LO leakage: at 2/3 of the RF output					
	@ RF=5.15-5.35 GHz (FCC)	—	—	-32	—	dBm
	@ RF=5.35-5.725 GHz (ETSI)			-36	—	dBm
	@ RF=5.725-5.825 GHz (FCC)			-30	—	dBm
RS	Synthesizer reference spur	—	—	-68	—	dBc

Table 3-7 Tx Characteristics for 5 GHz Operation (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EVM		Tx Power (dBm)[4]				
	802.11ac, MCS9, VHT80:1 Tx Chain	-15	—	-37	—	dB
		-13	—	-37	—	
		-10	—	-37	—	
		-8	—	-37	—	
		-7	—	-37	—	
		-5	—	-37	—	
		-3	—	-37	—	
		-1	—	-37	—	
		1	—	-37	—	
		3	—	-36	—	
		5	—	-35	—	
		7	—	-35	—	
		9	—	-35	—	
		11	—	-34	—	
		13	—	-34	—	
		15	—	-33	—	
		17	—	-31	—	

1. Measured with reference design including switch
2. Guaranteed by design.
3. Manufacturing calibration required.
4. Measured at the RF connector's output.

Table 3-8 Tx Impedance Characteristics for 5 GHz Operation

Symbol	Parameter	Description	Typ	Unit
Z_{RFout_load}	Output Impedance See Note 1	**Chain0**		Ω
		5180	12.684+j7.3283	
		5500	13.683+j33.267	
		5825	14.297+j55.226	
		Chain1		
		5180	11.929+j27.726	
		5500	8.0882+j49.142	
		5825	4.5618+j61.848	

1. See the sample impedance matching circuit in the Qualcomm Atheros reference design schematics. To achieve good RF performance, it is strongly recommended not to alter the RF portion of the Qualcomm Atheros reference design for different matching networks.

3.5.3 Synthesizer Characteristics

Table 3-9 summarizes the synthesizer characteristics for the QCA9886.

Table 3-9 Synthesizer Composite Characteristics for 5-GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out)					
	At 30 KHz offset	—	—	-97	—	dBc/Hz
	At 100 KHz offset		—	-98	—	
	At 500 KHz offset		—	-103	—	
	At 1 MHz offset		—	-112	—	
F_C	Center channel frequency	Center frequency at 5 MHz spacing[1]	5.18	—	5.825	GHz
F_{ref}	Reference oscillator frequency	± 20 ppm[2]	—	40	—	MHz

1. Frequency is measured at the Tx output.
2. Over temperature variation and aging.

3.6 Power Consumption Parameters

These conditions apply to the typical characteristics unless otherwise specified: V_{DD33} = 3.3V, T_{amb} = 25 °C. The Table 3-10 through Table 3-12 shows typical power consumption as a function of operating mode.

Table 3-10 Power consumption for 5 GHz operation (VHT20)[1]

Operating Mode	AVDD33	DVDD33	AVDD11	DVDD11	Unit
Tx (Two-Chain[2]) with Internal PA	750	230	110	240	mA
Rx (Two-Chain)	150	210	132	180	mA

1. MCS8
2. Tx output power of 18 dBm

Table 3-11 Power consumption for 5 GHz operation (VHT40)[1]

Operating Mode	AVDD33	DVDD33	AVDD11	DVDD11	Unit
Tx (Two-Chain[2]) with Internal PA	760	240	120	260	mA
Rx (Two-Chain)	160	220	140	190	mA

1. MCS9
2. Tx output power of 18 dBm

Table 3-12 Power consumption for 5 GHz operation (VHT80)[1]

Operating Mode	AVDD33	DVDD33	AVDD11	DVDD11	Unit
Tx (Two-Chain[2]) with Internal PA	783	260	129	268	mA
Rx (Two-Chain)	177	241	145	206	mA

1. MCS9
2. Tx output power of 18 dBm

4 Mechanical Information

The QCA9886 uses a 100-pin, dual-row, quad flat, no-leads (DRQFN) package.

4.1 Device Physical Dimensions

The QCA9886 DRQFN-100 package drawings and dimensions are provided in Figure 4-1 and Figure 4-2, and in Table 4-1 and Table 4-2.

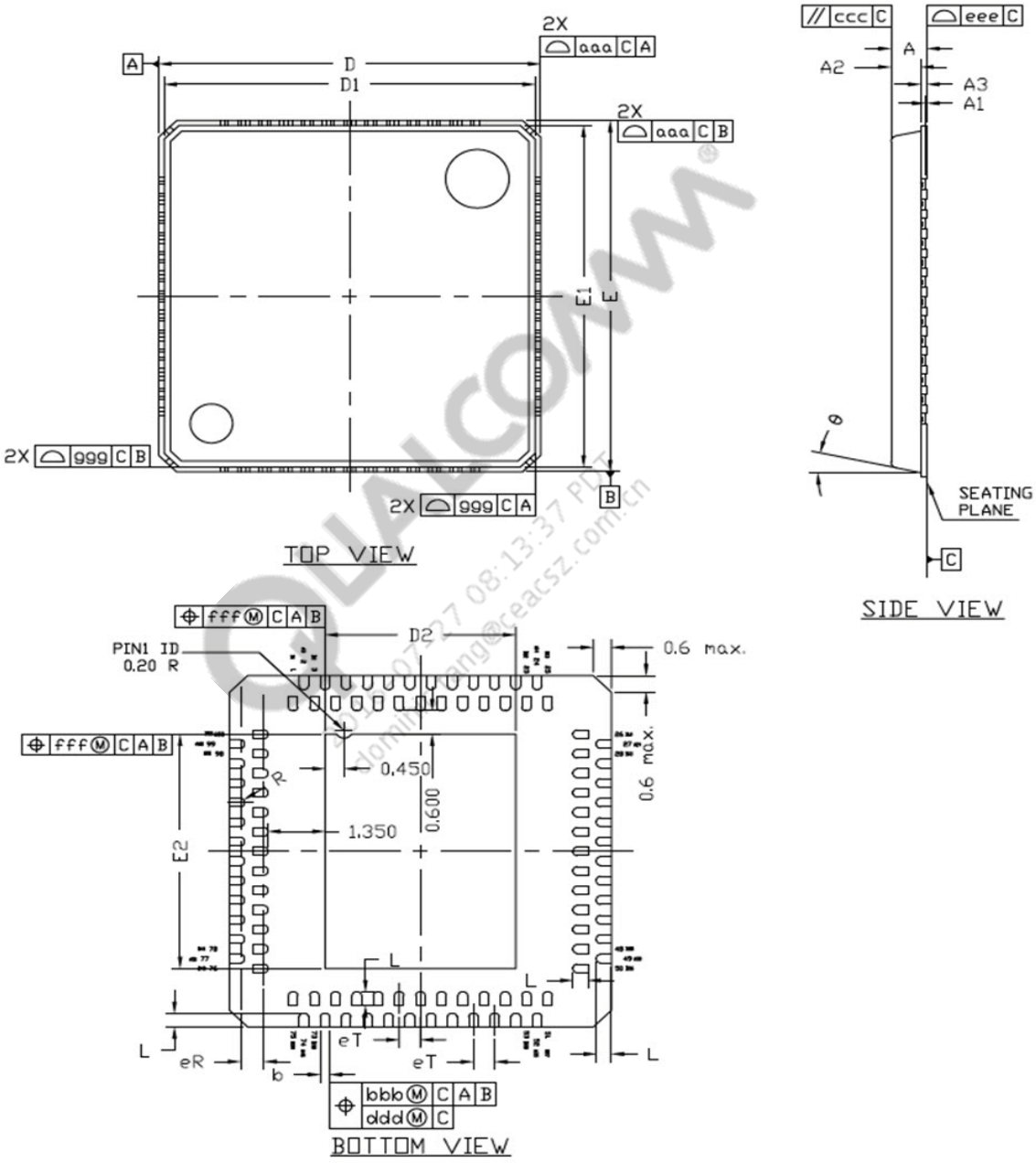


Figure 4-1 QCA9886 Package A Details

Table 4-1 Package A Dimensions

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.800	0.850	0.900	mm	0.031	0.033	0.035	inches
A1	0.000	0.020	0.050	mm	0.000	0.001	0.002	inches
A2	0.650	0.700	0.750	mm	0.026	0.028	0.030	inches
A3		0.152 REF		mm		0.006 REF		inches
b	0.180	0.220	0.300	mm	0.007	0.009	0.012	inches
D/E	8.900	9	9.100	mm	0.350	0.354	0.358	inches
D1/E1		8.750 BSC				3.444 BSC		
D2	4.400	4.500	4.600	mm	0.173	0.177	0.181	inches
E2	5.900	6.000	6.100	mm	0.232	0.236	0.240	inches
eT		0.500 BSC				0.020 BSC		
eR		0.550 BSC				0.022 BSC		
L	0.250	0.350	0.450	mm	0.010	0.014	0.018	inches
θ	5°	—	15°	degrees	5°	—	15°	degrees
R	0.090	—	0.140	mm	0.004	—	0.006	inches
aaa		0.100		mm		0.004		inches
bbb		0.100		mm		0.004		inches
ccc		0.100		mm		0.004		inches
ddd		0.050		mm		0.002		inches
eee		0.080		mm		0.003		inches
fff		0.100		mm		0.004		inches
ggg		0.200		mm		0.008		inches
Controlling dimension: Millimeters								

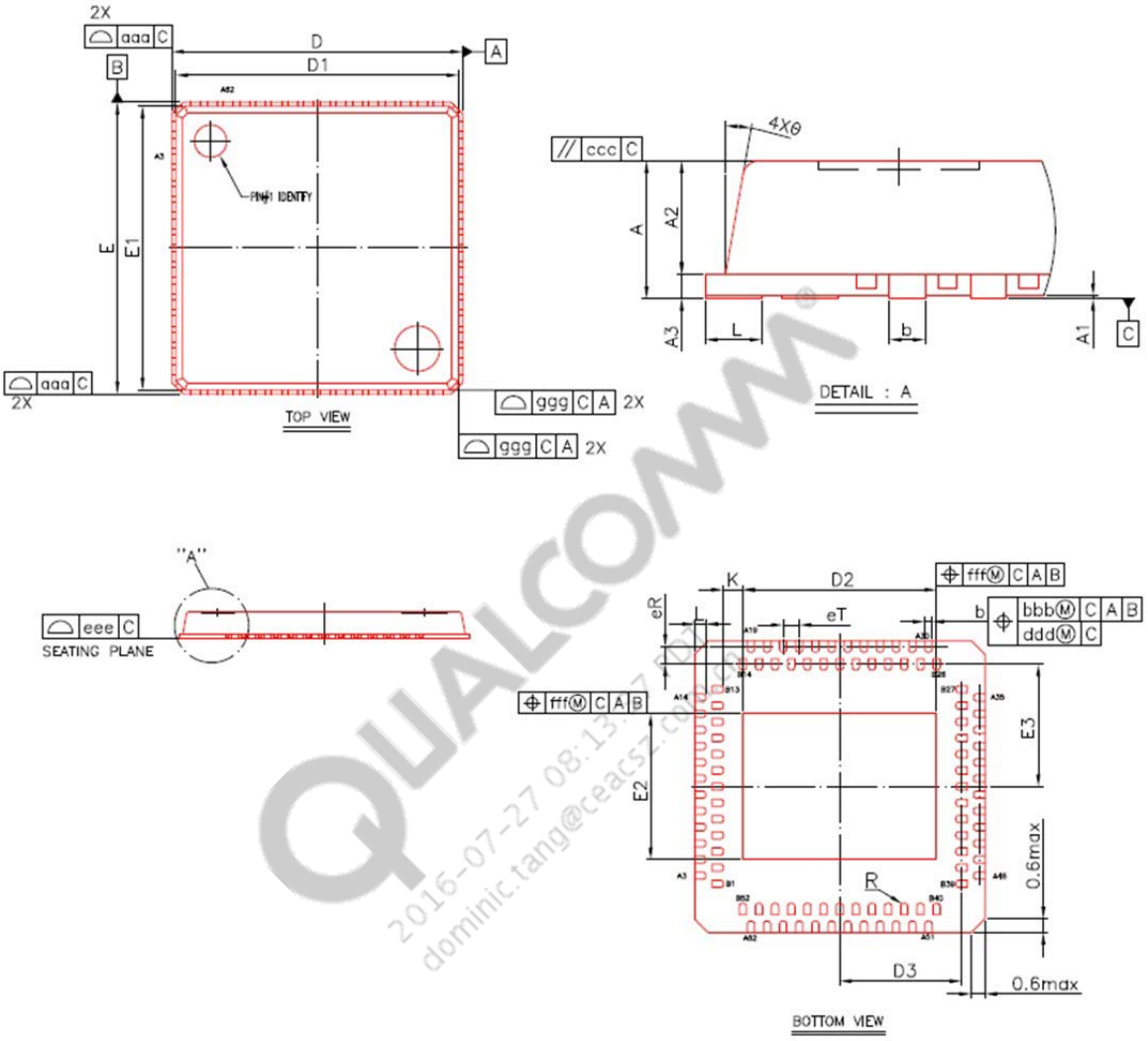


Figure 4-2 QCA9886 Package B Details

Table 4-2 Package B Dimensions

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.031	0.033	0.035	inches
A1	0.00	0.02	0.05	mm	0.000	0.001	0.002	inches
A2	0.65	0.70	0.75	mm	0.026	0.028	0.030	inches
A3		0.15 REF		mm		0.006 REF		inches
b	0.18	0.22	0.30	mm	0.007	0.009	0.012	inches
D/E	8.90	9.00	9.10	mm	0.350	0.354	0.358	inches
D1/E1		8.75 BSC		mm		0.344 BSC		inches
D2	5.90	6.00	6.10	mm	0.232	0.236	0.240	inches
E2	4.40	4.50	4.60	mm	0.173	0.177	0.181	inches

Table 4-2 Package B Dimensions

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
D3/E3		3.775 BSC		mm		0.149 BSC		inches
eT		0.50 BSC		mm		0.020 BSC		inches
eR		0.55 BSC		mm		0.022 BSC		inches
L	0.25	0.35	0.45	mm	0.010	0.014	0.018	inches
θ	5°	—	15°	degrees	5°	—	15°	degrees
R	0.09	—	0.14	mm	0.004	—	0.006	inches
K	0.20	—	—	mm	0.008	—	—	inches
aaa		0.10		mm		0.004		inches
bbb		0.10		mm		0.004		inches
ccc		0.10		mm		0.004		inches
ddd		0.05		mm		0.002		inches
eee		0.08		mm		0.003		inches
fff		0.10		mm		0.004		inches
ggg		0.20		mm		0.008		inches
Controlling dimension: Millimeters								

4.2 Part Marking

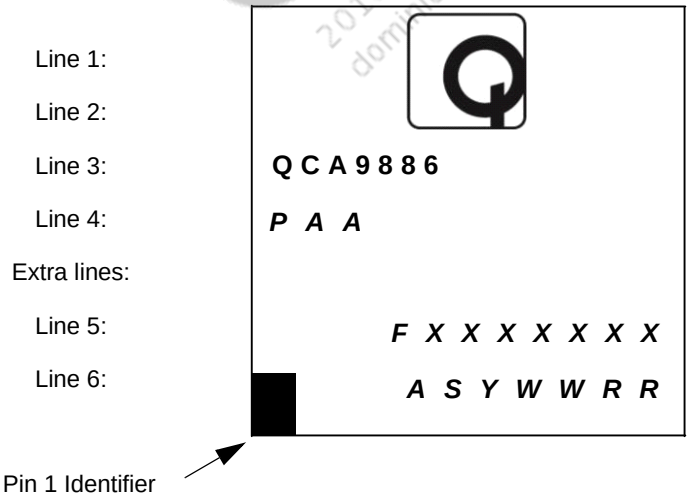


Figure 4-3 QCA9886 Marking (top view, not to scale)

Table 4-3 QCA9886 Marking Line Definitions

Line	Marking	Description
1 and 2	Qualcomm logo	Qualcomm name or logo
3	QCA9886	Qualcomm product name

Table 4-3 QCA9886 Marking Line Definitions (cont.)

Line	Marking	Description
4	PAA	P = Product configuration code AA = Product feature code
5	FXXXXXXX	F = fab code XXXXXXX = wafer lot ID
6	ASYWWRR	A = Assembly site code S = Assembly sequence number Y = Single, last digit of year WW = Work week (based on calendar year) RR = Product revision code
Additional lines may appear on the part marking for some samples; this is manufacturing information that is only relevant to Qualcomm and Qualcomm suppliers.		

4.3 Device Ordering Information

Order numbers have the form shown in Figure 4-4.

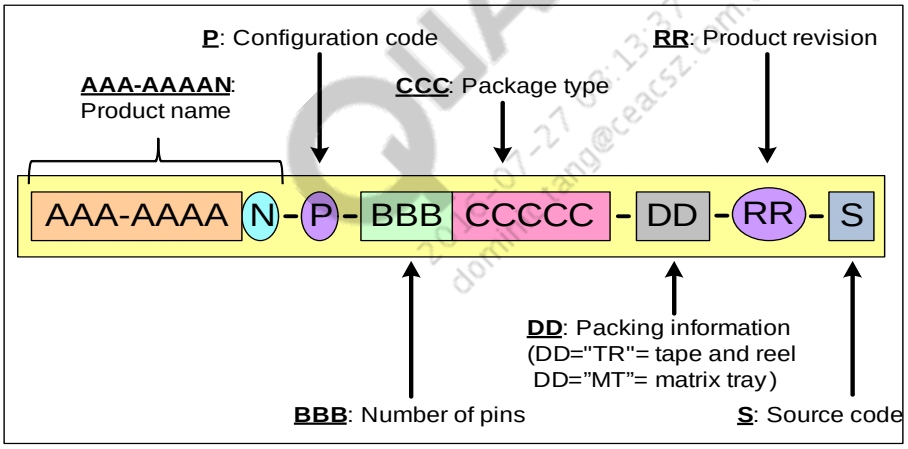


Figure 4-4 Device Identification Code

Table 4-4 shows the available order numbers.

Table 4-4 QCA9886 Order Numbers

Number	Descriptions
QCA-9886-0-100DRQFN-MT-04-0	RoHS & BrCl-free
QCA-9886-0-100DRQFN-TR-04-0	RoHS & BrCl-free, Tape-and-Reel

4.4 Device Moisture-sensitivity Level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. Qualcomm follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. The QCA9886 is classified as MSL3; the qualification temperature was 250ºC.

4.5 Thermal Characteristics

Table 4-5 Thermal Resistance

Parameter		Comment	Typical	Unit
θ_{JA}	Junction-to-Ambient	■ With 30 thermal vias ■ Jedec JESD51-2A ■ Jedec JESD51-5	26.39	°C/W
θ_{JB}	Junction-to-Board	■ With no thermal vias ■ Jedec JESD51-7 ■ Jedec JESD51-8	13.48	°C/W
θ_{JC}	Junction-to-Case	■ With no thermal vias ■ Jedec JESD51-7 ■ Jedec JESD51-8	8.82	°C/W

5 Carrier, Storage, and Handling

5.1 Carrier

5.1.1 Tape and Reel Information

Carrier tape system conforms to EIA-481- D standards.

Simplified sketches of the QCA9886 tape carrier is shown in Figure 5-1 and Figure 5-2, including the part orientation. Tape and reel details for the QCA9886 are as follows:

- Reel diameter: 330 mm
- Hub size: 102 mm
- Tape width: 16 mm
- Tape pocket pitch: 12 mm
- Feed: Single
- Units per reel: 4000

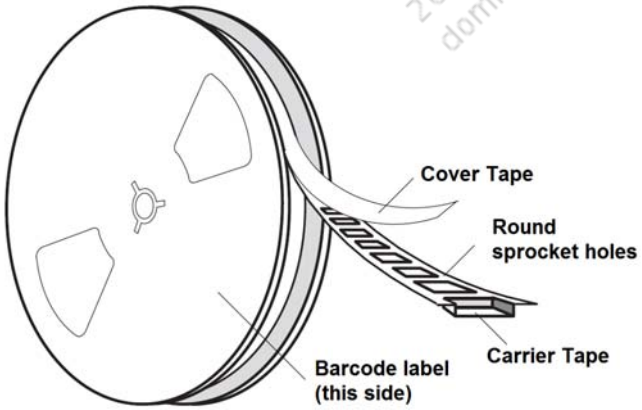


Figure 5-1 Tape Orientation on Reel

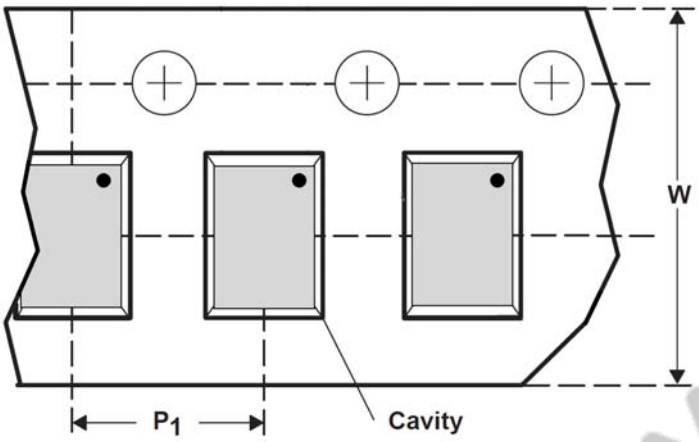
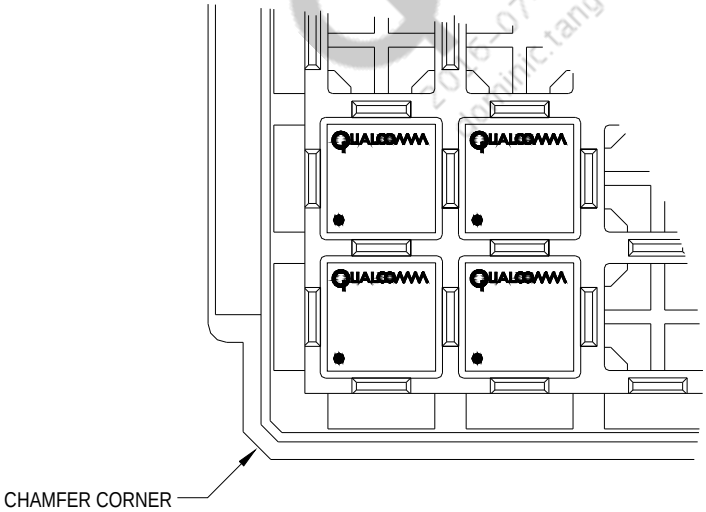


Figure 5-2 Part Orientation in Tape

5.1.2 Matrix Tray Information

All QTI matrix tray carriers confirm to JEDEC standards. The device pin 1 is oriented to the chamfered corner of the matrix tray. Each tray of the QCA9886 contains up to 152 devices. See Figure 5-3 for matrix-tray key attributes and dimensions.



Key dimensions	
Array	10 × 26 = 260
M	10.35 mm
M1	10.00 mm
M2	11.80 mm
M3	12.80 mm

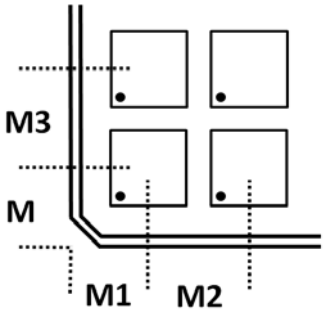


Figure 5-3 Matrix Tray Part Orientation

5.2 Storage

5.2.1 Bagged Storage Conditions

QCA9886 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag Duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling is described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is **not necessary** to bake the QCA9886 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the QCA9886 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see *ASIC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic Discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment.*

6 PCB Mounting Guidelines

Guidelines for mounting the QCA9886 device onto a PCB are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification.

6.1 RoHS Compliance

The QCA9886 device is externally lead-free and RoHS-compliant. Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products.

6.2 SMT Parameters

This section describes board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land Pad and Stencil Design

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil-pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability. Review the land pattern and stencil pattern design recommendations as a guide for characterization:

PCB Land and Stencil Design Guide (LS90-NG134-1).

6.2.2 Reflow Profile

Reflow profile conditions typically used by Qualcomm for lead-free systems are listed in Table 6-1 and are shown in Figure 6-1.

Table 6-1 Typical SMT Reflow Profile Conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Dry-out and flux activation	150 to 190°C	60 to 120sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C. This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

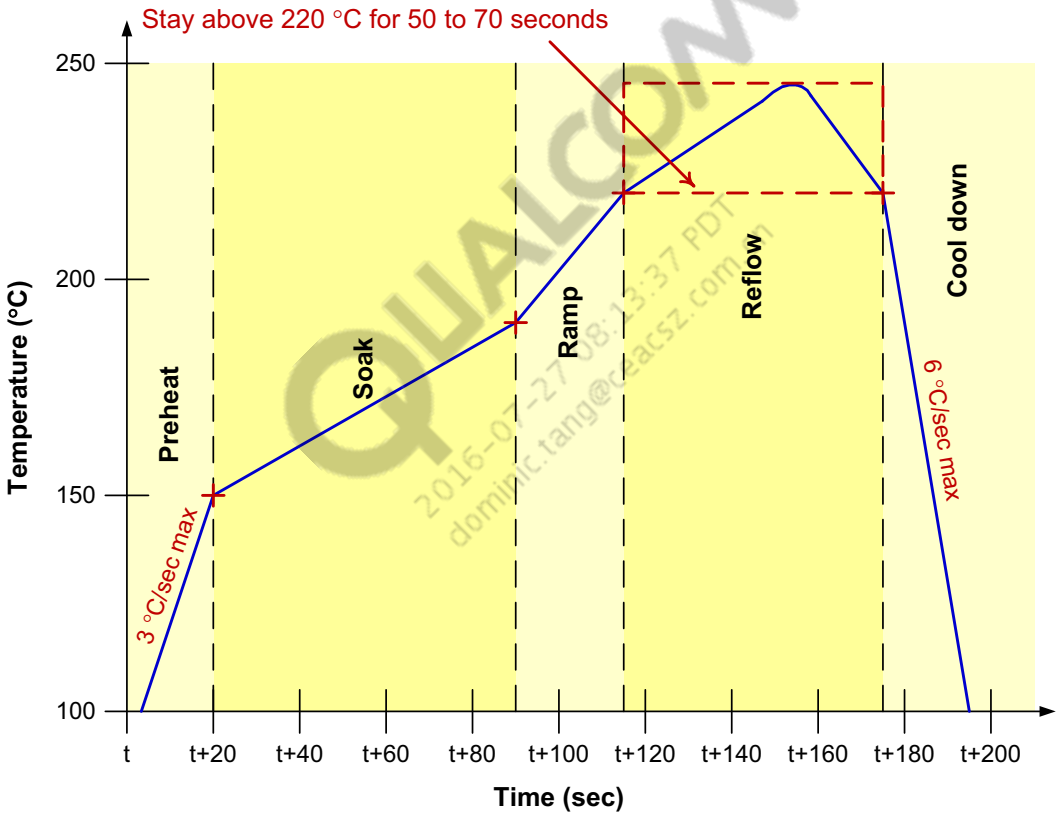


Figure 6-1 Typical SMT Reflow Profile

6.2.3 SMT Peak Package-body Temperature

During a production board's reflow process, the temperature seen by the package must be controlled. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more). Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the Qualcomm recommended limits must not be exceeded.

6.2.4 SMT Process Verification

Qualcomm recommends verification of the SMT process prior to high-volume board assembly, including:

- Electrical continuity
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume

6.3 Board-level Reliability

Qualcomm conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

For board-level reliability data, refer to *Board-Level Reliability DRQFN/mQFN* (BR80-NT096-1).

7 Part Reliability

7.1 Reliability qualification summary

QCA9886 reliability evaluation report.

Table 7-1 Reliability Evaluation Results

Tests, standards, and conditions	Sample Size	Result
Average failure rate (AFR, λ) in FIT Failure in billion device-hours Functional HTOL: JESD22-A108-A	231	λ = 11.8 FIT PASS
Mean time to failure (MTTF, million hours) t = 1/λ	231	84.5
ESD - Human-body model (HBM) rating JESD22-A114-B	3	PASS[1]
ESD - Charge-device model (CDM) rating JESD22-C101-D	3	PASS[2]
Latch-up (I-test): EIA/JESD78 Trigger current: ±100 mA; Temperature: 85°C	6	PASS
Latch-up (V-supply Overvoltage): EIA/JESD78 Trigger voltage: 1.5xVdd; Temperature: 85°C	6	PASS
Moisture resistance test (MRT): **MSL3**, J-STD-020 3 x Reflow Cycles @ 260 C +5/-0 °C 100% CSAM Delamination Inspection	1386	PASS
Temperature cycle: JESD22-A104 Temperature: -65 °C to +150 °C; Number of cycles: 1000 Soak time at min/max temperature: 8-10 minutes Cycle rate: 2 cycles per hour (cph) **Preconditioning: MSL3**; JESD22-A113 Reflow temperature: 260 °C +5/-0 °C	462	PASS
Unbiased highly accelerated stress test JESD22-A118 **Preconditioning: MSL3;** JESD22-A113 (130 C / 85% RH and 96 hrs duration) Reflow temperature: 260 °C +5/-0 °C	462	PASS
Biased highly accelerated stress test (bHAST): JESD22-A110 **Preconditioning: MSL3;** JESD22-A113 (110C / 85% RH and 264 hrs duration) Reflow temperature: 260 °C +5/-0 °C	154	PASS

Table 7-1 Reliability Evaluation Results (cont.)

Tests, standards, and conditions	Sample Size	Result
High-Temperature Storage Life: JESD22-A103 Temperature 150°C, 500, 1000 hours duration	462	PASS
Physical dimensions: JESD22-B100 Package outline drawing in Section 4.1	15	PASS

1. ±2000 V; all pins
2. ±500 V; all pins

7.2 Qualification Sample Description

Table 7-2 QCA9886 characteristics

Device name	QCA9886
Package type	0.5mm DRQFN
Package body size	9 x 9 x 0.9 mm
Pin count	100
Pin composition	Sn
Process	40 nm