DB120

802.11 a/b/g/n DBDC (Dual Band Dual Concurrent) Dev Board
AR9344 + AR9380+ AR8327 4 LAN+1 WAN 10/100/1000 router

DATE	REVISION NUMBER	INITIALS	DESCRIPTION
6/8/2010	245-02042-010	SC	INITIAL VERSION
8/9/2010	245-02042-011	JaiW	1. 25MHz Xtal, 22pF Xtal caps 2. Updt GPIOx cfg strap changes 3. Rst cap = 0.01uF 4. RF changes: 2G C94,C64 NO Load C98,C61 = 1.2pF;C97,C60= 1.5pF;C99,C57=1.8pF,C100,C58=2.2nH, C101,C54=1.8pF; 5G: C59 is 1.8nH C106 is 1.8nH C66, C67, C103, C104 =3.9pF C68, C109 = 2.2pF L10,L19 = 1.8nH
8/9/2010	245-02042-012	JaiW	Updt RF reworks for 5G: - 6 components noLOAD (3 per chain) C68, C59, L10 = noLOAD C109, C106,L19 =noLOAD - 8 components change (4 per chain) C67= 0ohms L11 =0.9nH C66=2.2pF C62=0.5pF C104=0 ohms L20 =0.8nH C103= 2.2pF C105=0.5pF
8/9/2010	245-02042-013	JaiW	Changed Sw Inductor L23 for lower DCR, higher rating
9/17/2010	245-02042-020	Jai,JK,SC	Changed Ethernet switch to AR8327N - page 09,10 Changed VR2 reg for AR8316 to 3.3V optional for AR8327 Added separation for BB, SYNTH pins from main 1.2_RF and 3.3V_RF Added separation for 1.2V_USB from 1.2_PU and VDD33_USB from VDD33_AR9344 Added separation for VDD33_SWREG from VDD33_AR9344 Changed GPIO allocation Corrected cfg strap connections Added Page 13 - T/R Switch, Ant; Changed the RX2G match topology; C367,C406 = 8.2pF
10/27/2010	245-02042-021	Jai,JK,SC	R295 = NL R397 = 10K R532 = 10K DS2, DS5 = load 2G TX: C101, C1xx = 1.2pF (was 1.8pF) 5G TX: Ch0: C67 = 0.6nH C68=0.2pF L11=0 5G TX: Ch1: AR9344 Pwr supply: Replaced all 22nH with 0 ohms. L11 - 0 Ohms C703 = 0.1uF
11/12/2010	245-02042-022	Jai,JK,SC	2G: L51 NL AR8327: MDC R583 = 330E MDIO R565 =1K Pwr: C706 C704 C703 C707 C344 C376 C708 C705 C379 C380 = 0.1uF 5G: Ch-0 C62 - 1.8pF C66 - 1.2pF C67 - 0.6nH C68 - 0.2pF C721 - 2.2pF Ch-1 C103 - 1.2pF C105 - 1.5pF C104 - 1.2nH C109 - 0.2pF C734 - 2.2pF
12/10/2010	245-02042-023	Jai/SC	1. Changed mem part to 64M for 128M total 2. LNA chain 0 changes C724 = 1.2pF R567 = 49.9ohm R605 = NL R609,R606 = 0 ohm;
12/19/2010	245-02042-030	Jai/SC	1. Added xPAs for 5G AR9344 2. Added PAs, LNAs for AR9380 3. Moved optional reg to 1.15V rail for AR8327 4. GPIO connections for boot_MDIO, MDC corrected 5. bufr option on MDC pullup opt to 3.3V on MDIO
1/21/2011	245-02042-031	Jai	1. 40Mhz xtal sel R396 = 10K 2. MDC pullup R583 = 560E 3. 2G Tx match changed: C94, C64= 0.3pF; C95,C96, C63, C65 = 6.8pF; C101, C54=1.5pF; 4. SWrst option R499 = NC
2/10/2011	245-02042-032	SC	For 2G Tx match: C97,C98,C60,C61 = 1.3pF C101,C54 = 1.0pF C99, C57 = 1.8pF VDD33_RF (for 5G flatness issue) R676 = 1.0nH VDD12_BB decoupling: C706=1000pF
2/17/2011	245-02042-033	Jai	1. (spectral flatness) L11 = 1.5nH 0201 2. (ch0 revert LNA to rec. values) R567 = 27E, C724 = 6.8pF 3. (DDR ck term change): R355,R356, R88, R89 = 0E R357, R87 = 100E
4/05/2011	245-02042-040	Jai	Correcting error for Ops. U5 VSSDL connected to GND. some silk text updt.
4/28/2011	245-02042-041	Jai	Memory part updated for more effective BOM

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Title: Title And Revision

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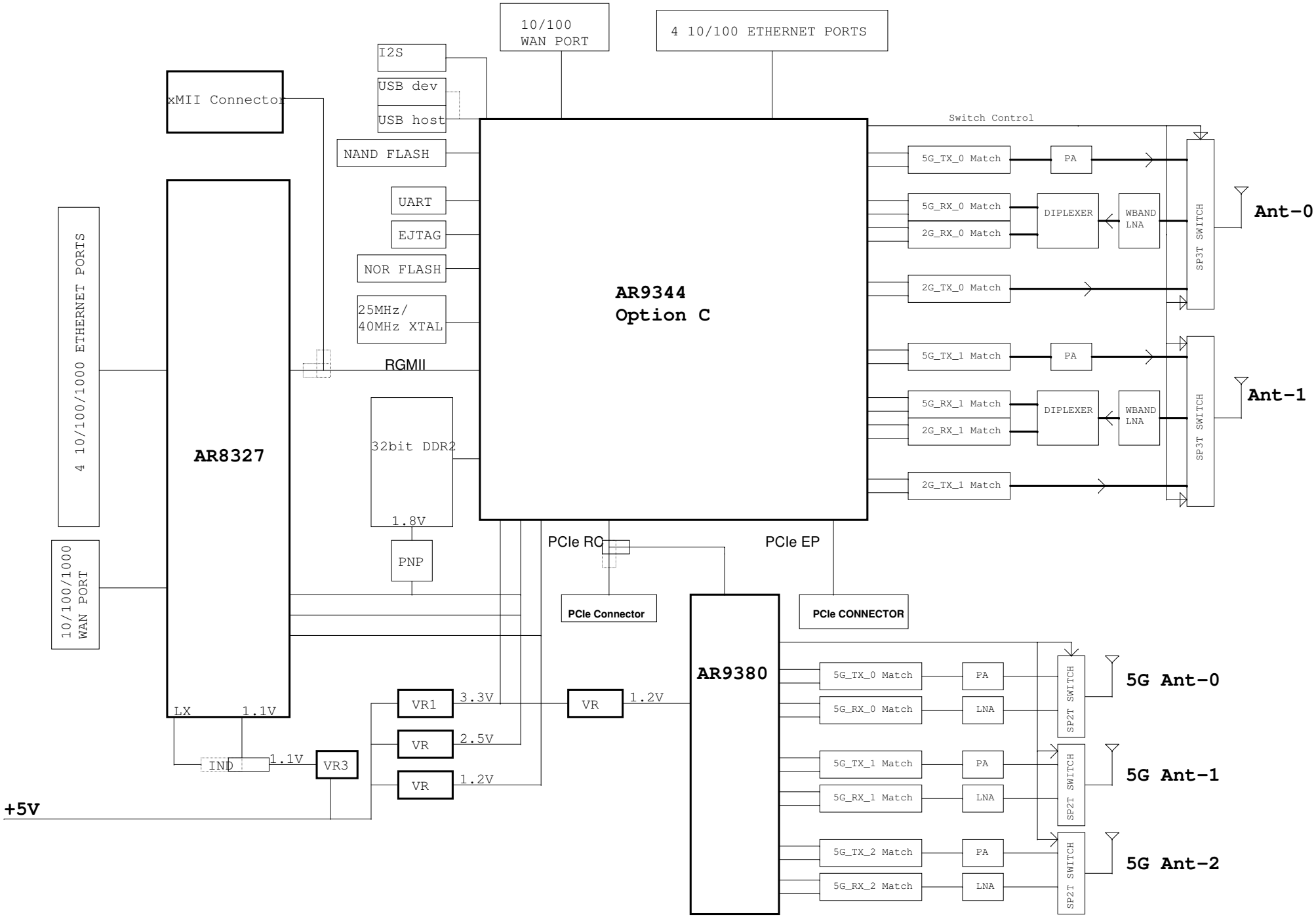

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Atheros Communications, Inc 1700 Technology Drive San Jose, CA 95110				Title: Block Diagram	
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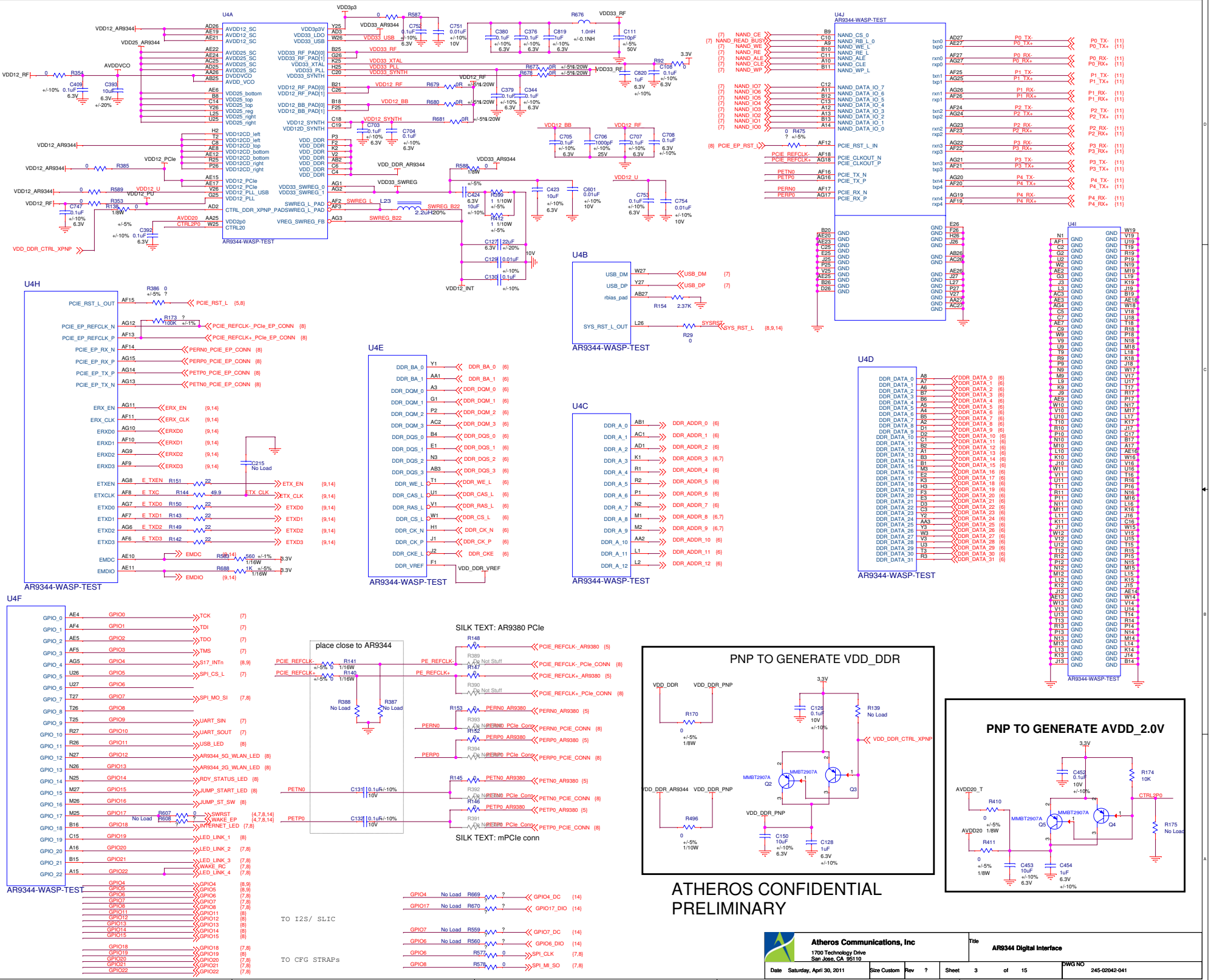
U4A
AR9344-WASP-TEST
U4H
U4E
U4B
U4C
U4D
U4J
U4I
U4F
SILK TEXT: AR9380 PCIe
SILK TEXT: mPCIe conn
place close to AR9344
PNP TO GENERATE VDD_DDR
PNP TO GENERATE AVDD_2.0V
TO I2S/ SLIC
TO CFG STRAPs
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AR9344 Digital Interface
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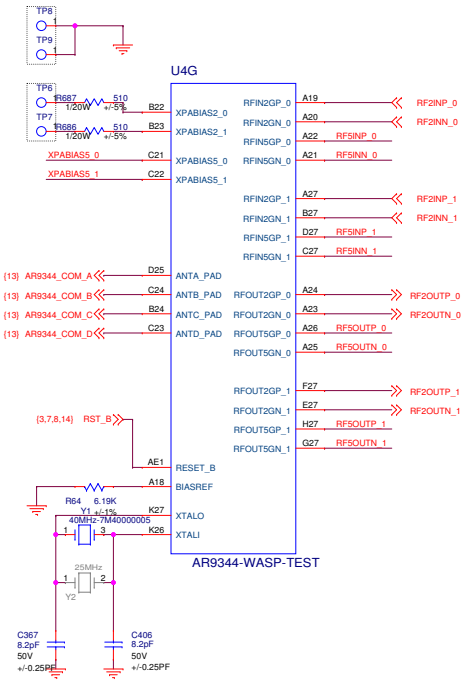

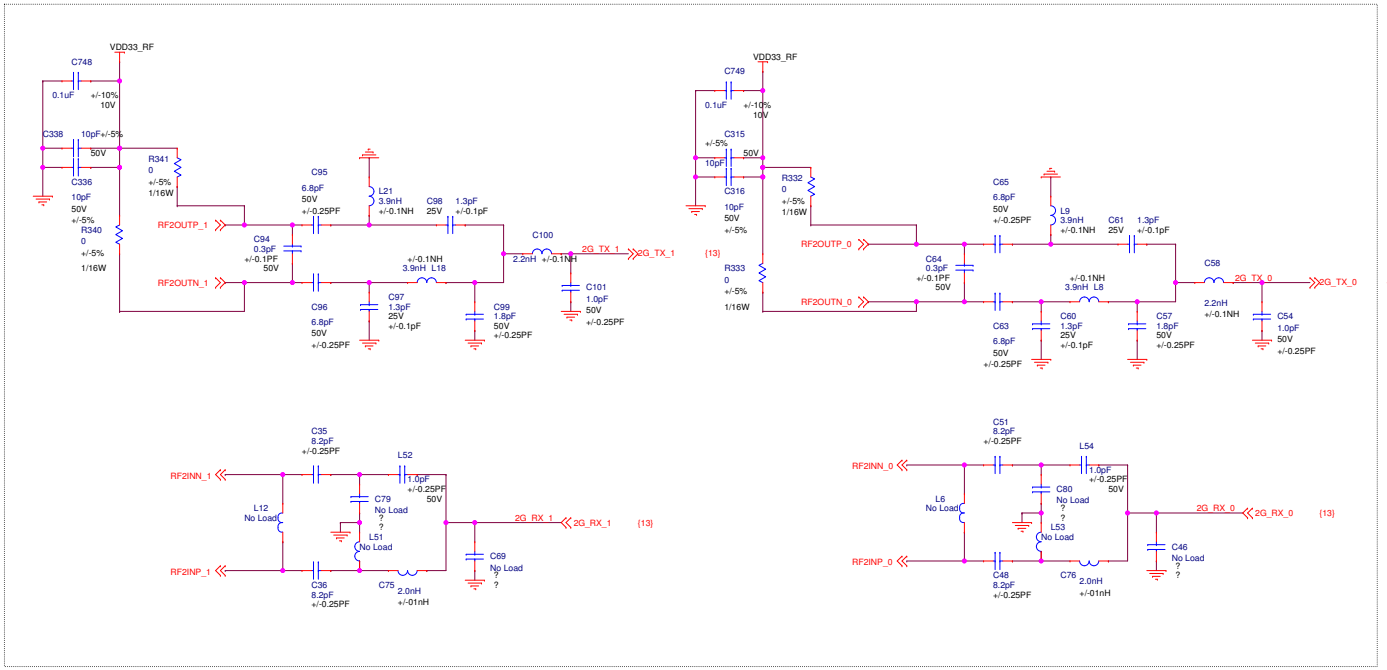

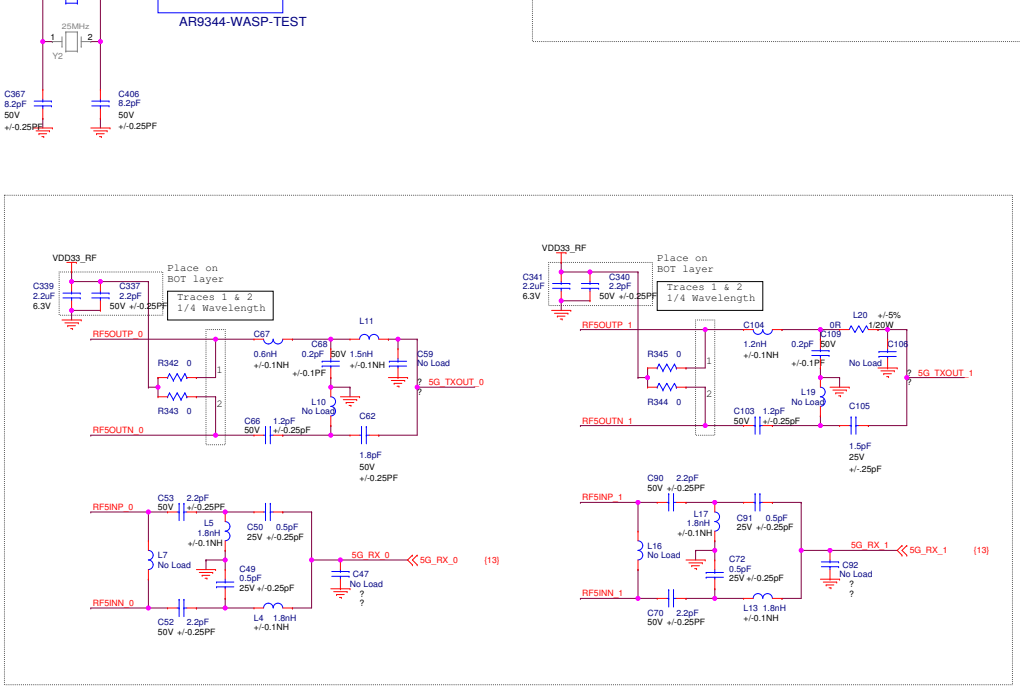

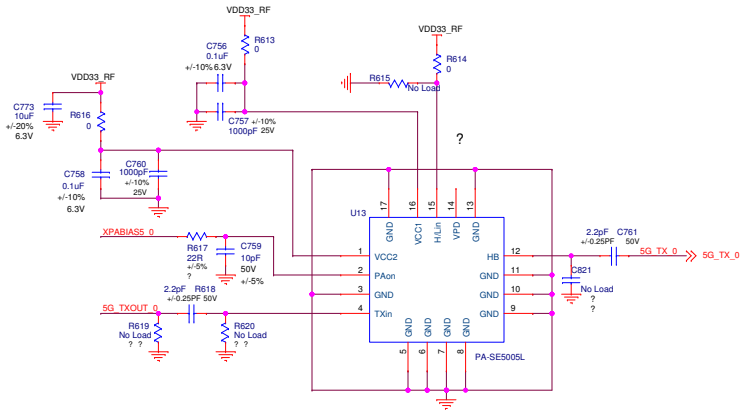

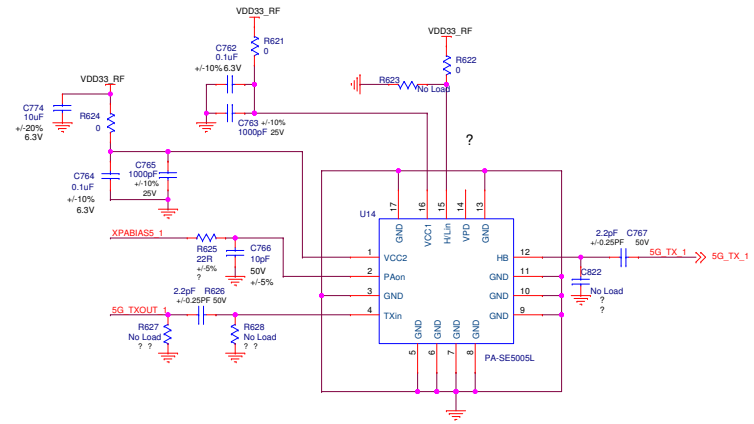

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Atheros Communications, Inc 1700 Technology Drive San Jose, CA 95110			Title: Atheros RF Interface		
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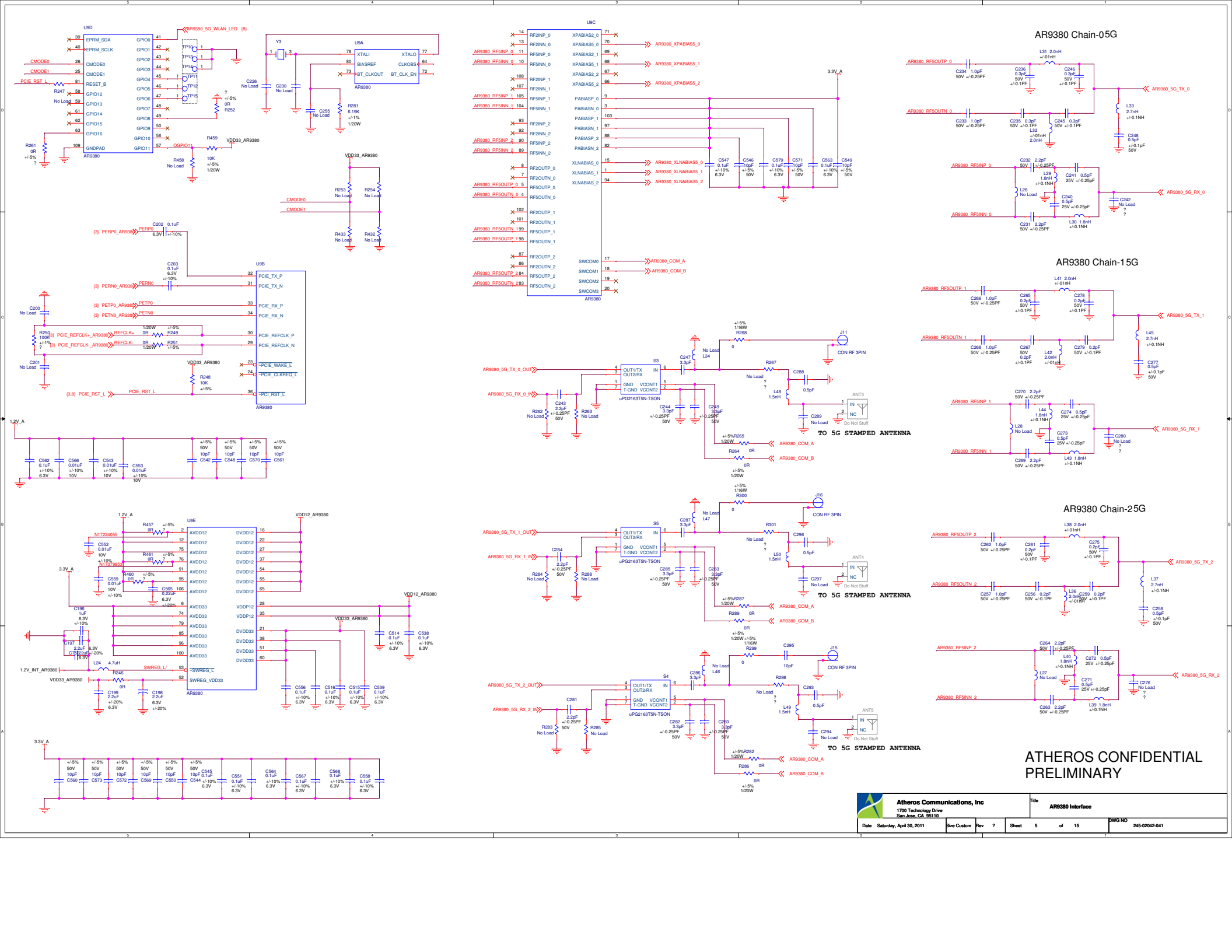
U9D
U9A
U9C
U9B
U9E
Y3
AR9380
AR9380 Chain-05G
AR9380 Chain-15G
AR9380 Chain-25G
TO 5G STAMPED ANTENNA
TO 5G STAMPED ANTENNA
TO 5G STAMPED ANTENNA
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AR9380 Interface
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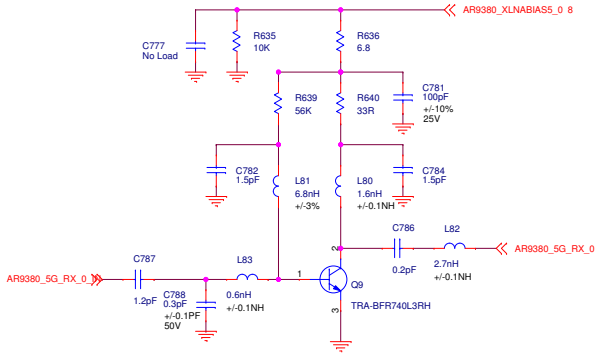

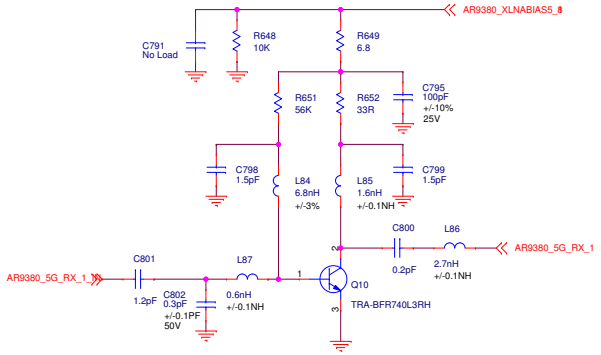

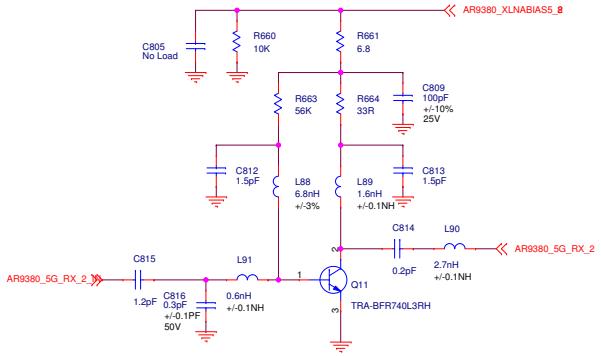

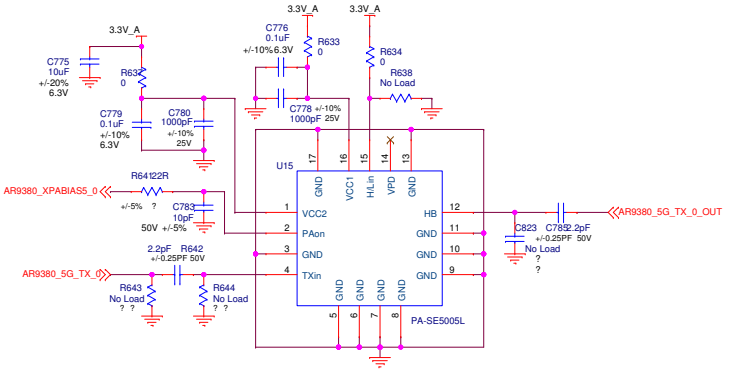

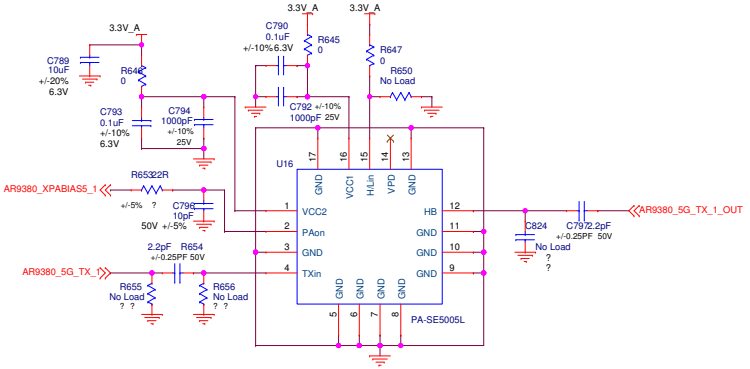

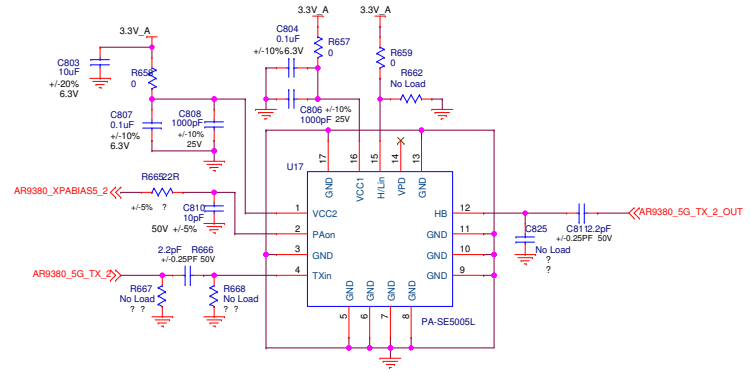

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Atheros Communications, Inc 1700 Technology Drive San Jose, CA 95110				Title	AR9380 RF Front end
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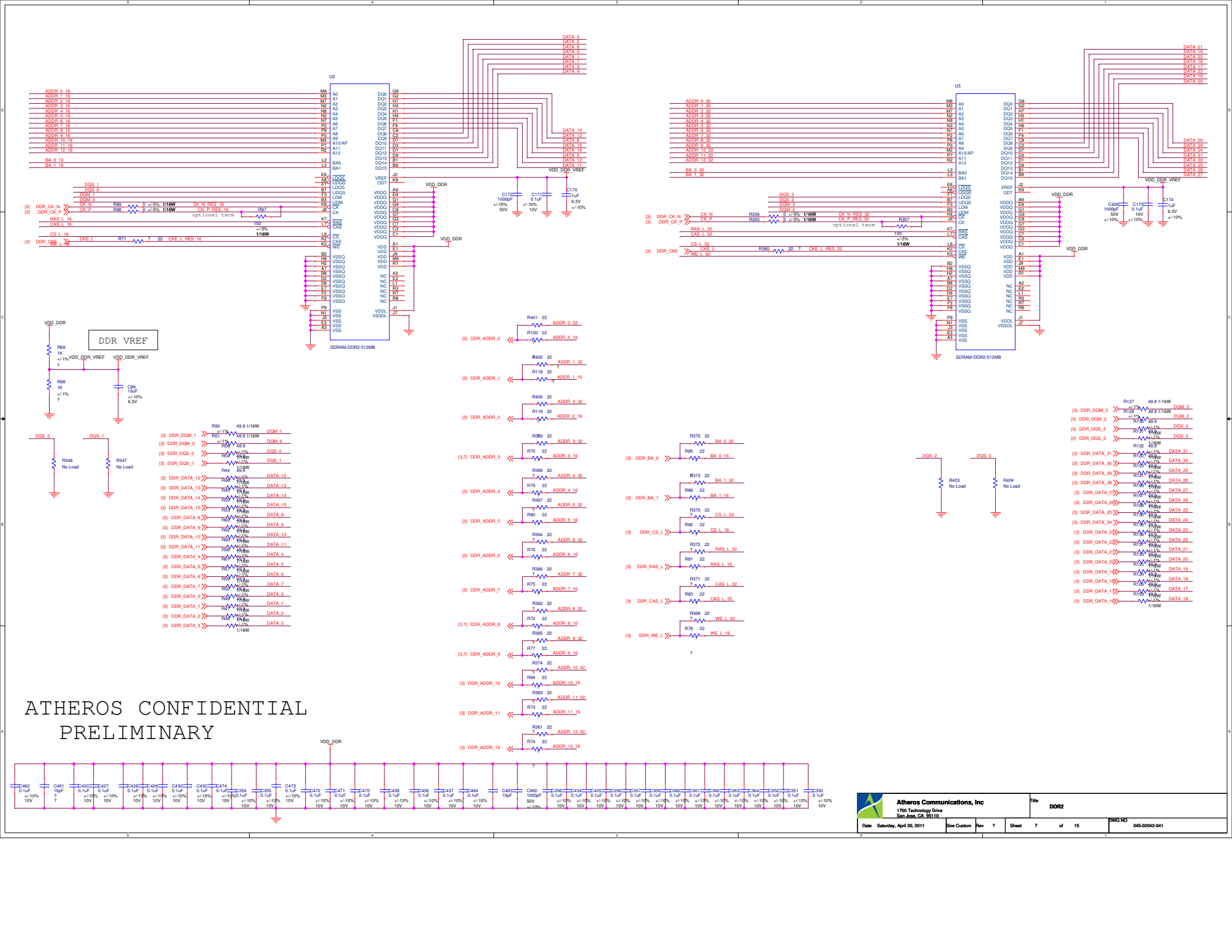
U3
SDRAM-DDR2-512MB
U5
SDRAM-DDR2-512MB
DDR VREF
VDD_DDR
VDD_DDR_VREF
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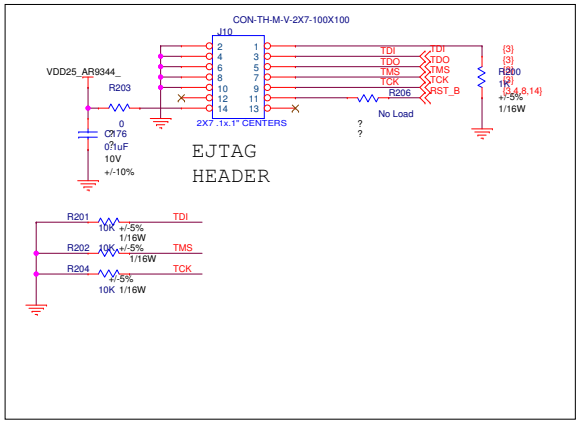

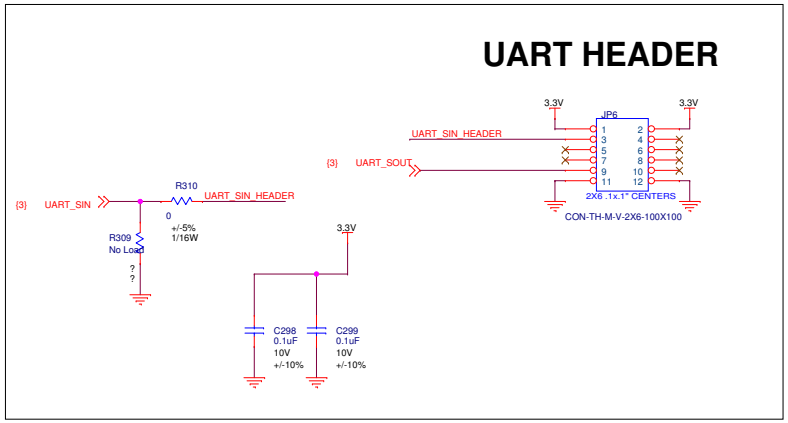

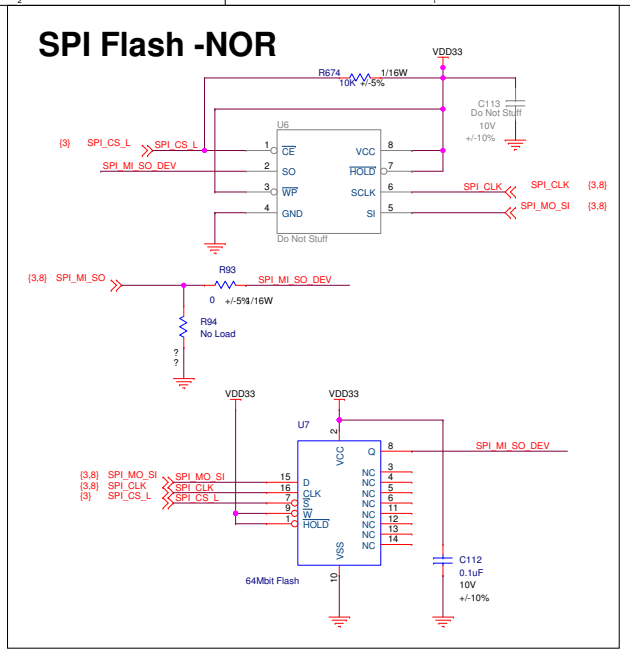

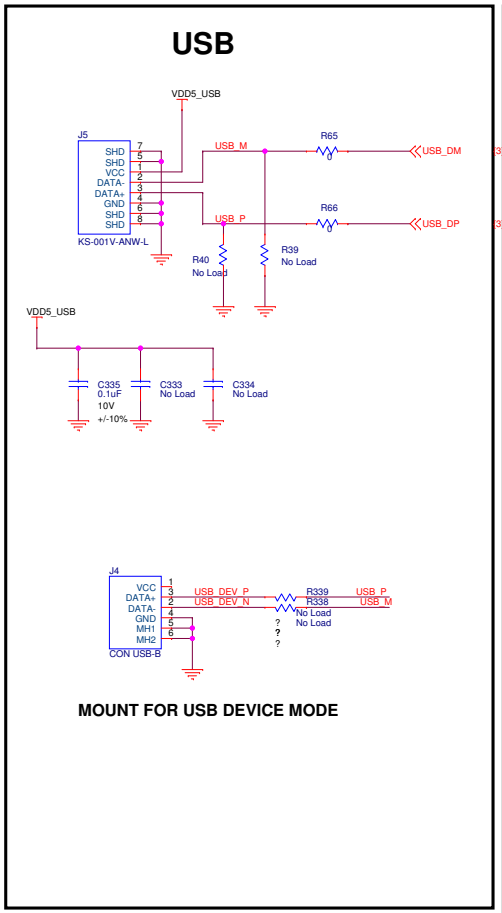

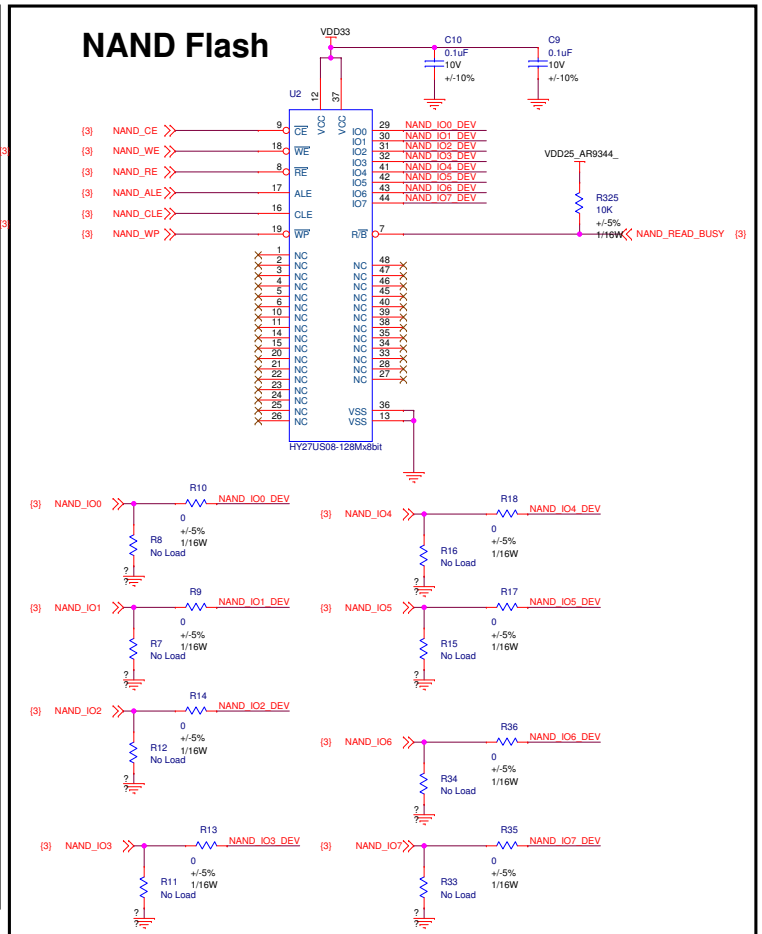

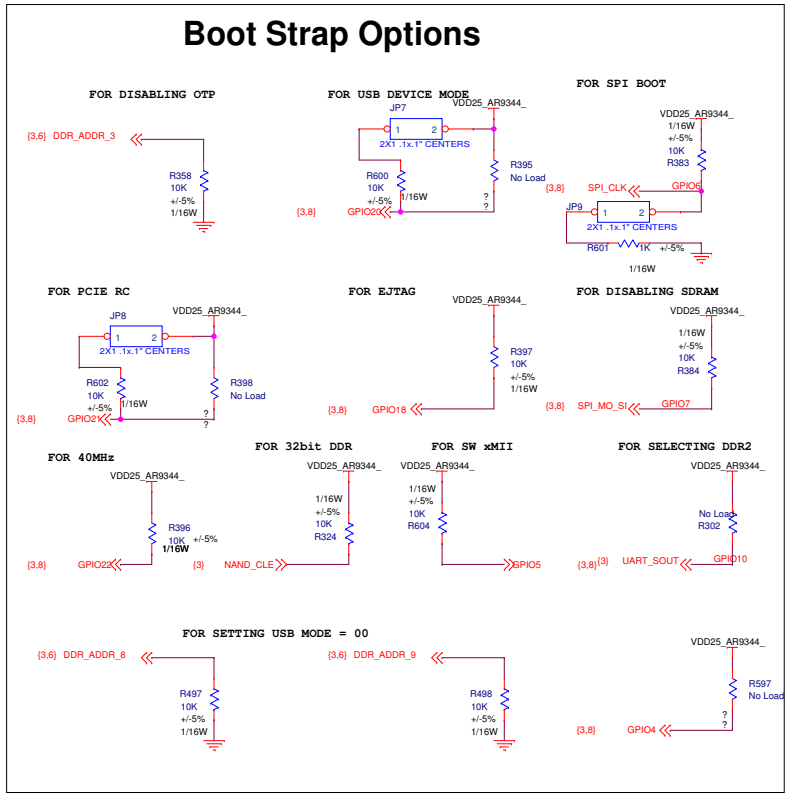

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Atheros Communications, Inc 1700 Technology Drive San Jose, CA 95110		Title	EJTAG USB UART
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RGMII i/f to AR9344

5GE LED i/f to LED display

5GE i/f to Transformer

Power On Strapping

pin-B44	S17_SPI_DO	MDIO_EN (D:1)
pin-B49	RG1_RXD2	SPI_SIZE(D:0)
p i	S17_INTn0	LED_OPEN_EN(D:1)
pin-A65	RXCLK	SPI_EN(D:0)
pin-A54	RG1_RXDV	AZ_EN
pin-A69	RXD1	Mode_oclk_selH for LX(D:0) (1) 1¡¦b1, 1.15V for ; (2) 1¡¦b0, 1.1V;

place close to S17

Normal Setting

pin-A65 RXDV 10K R527; RXD3 10K R528; pin-A69 RXD2 No Load R584 10K R529; RXD0_1 10K R585 No Load R586

11: most save power; PHY power is minimize.
01: short cable save some power, long cable does not.
10: short and long cable all save some power. (recommended)
00: not save power.

25MHz Source

X3 25MHz; XTLI — C612 27pF — 25MHz — C713 27pF — XTLO

Amplitude of XTLI input clock must be less than 1.5V.

SPI Interface

U12 16Bit Mode 93LC66B-SO

S17_SPI_CS	1	CS	VCC 8
S17_SPI_CLK	2	CLK	NC2 7
S17_SPI_DO	3	DI	NC1 6
S17_SPI_DI	4	DO	GND 5

C715 No Load (1000pF); C617 No Load

Reset

SYS_RST_L — R533 0 — S17_RSTL; R532 10K (100K); C618 +/-5% 1/16W No Load (0.1uF); +/-5% 1/16W

1.25V PLL Power

AVDDVCO_O — R535 0 — C625 0.1uF — C626 No Load; AVDDVCO_I — C636 0.1uF — C637 No Load

Atheros

AR8327N

Close to S17: L62 4.7uH; LX_S17 — R536 No Load — C645 No Load

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01 Development

Atheros Communications, Inc 1700 Technology Drive San Jose, CA 95110					Title	GIGA Switch AR8327N
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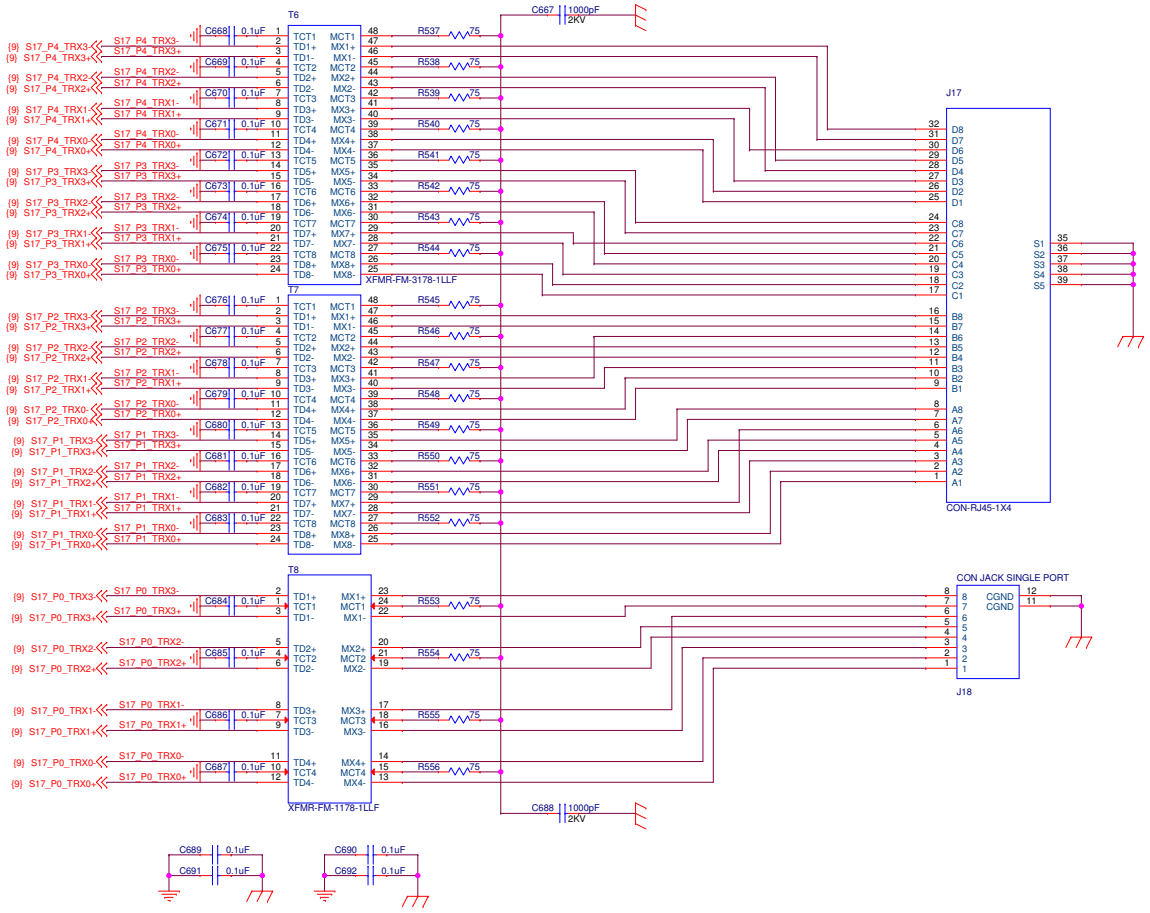

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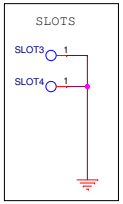

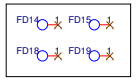

01 Development

Atheros Communications, Inc 1700 Technology Drive San Jose, CA 95110				Title	TRANSFORMERS, RJ45'S
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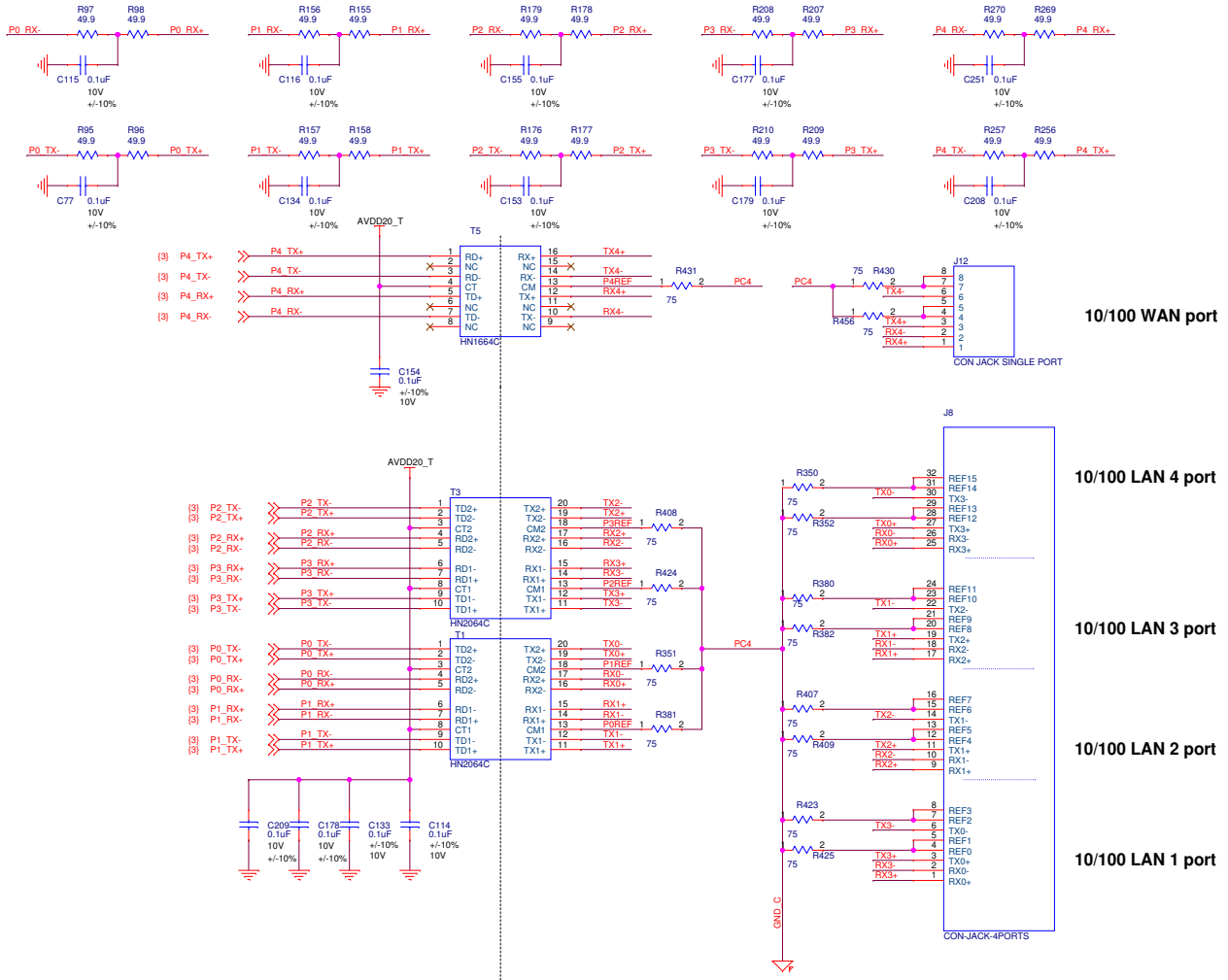

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SLOTS
SLOT1
SLOT2

LOCAL FIDUCIALS
FD2 FD5 FD4 FD3

LOGO
X2
LOGO-AP-LARGE

GLOBAL FIDUCIALS
FD1 FD8 FD6 FD9 FD7 FD10

MOUNTING HOLES
ZH4 ZH2 ZH1 ZH3

01 Development

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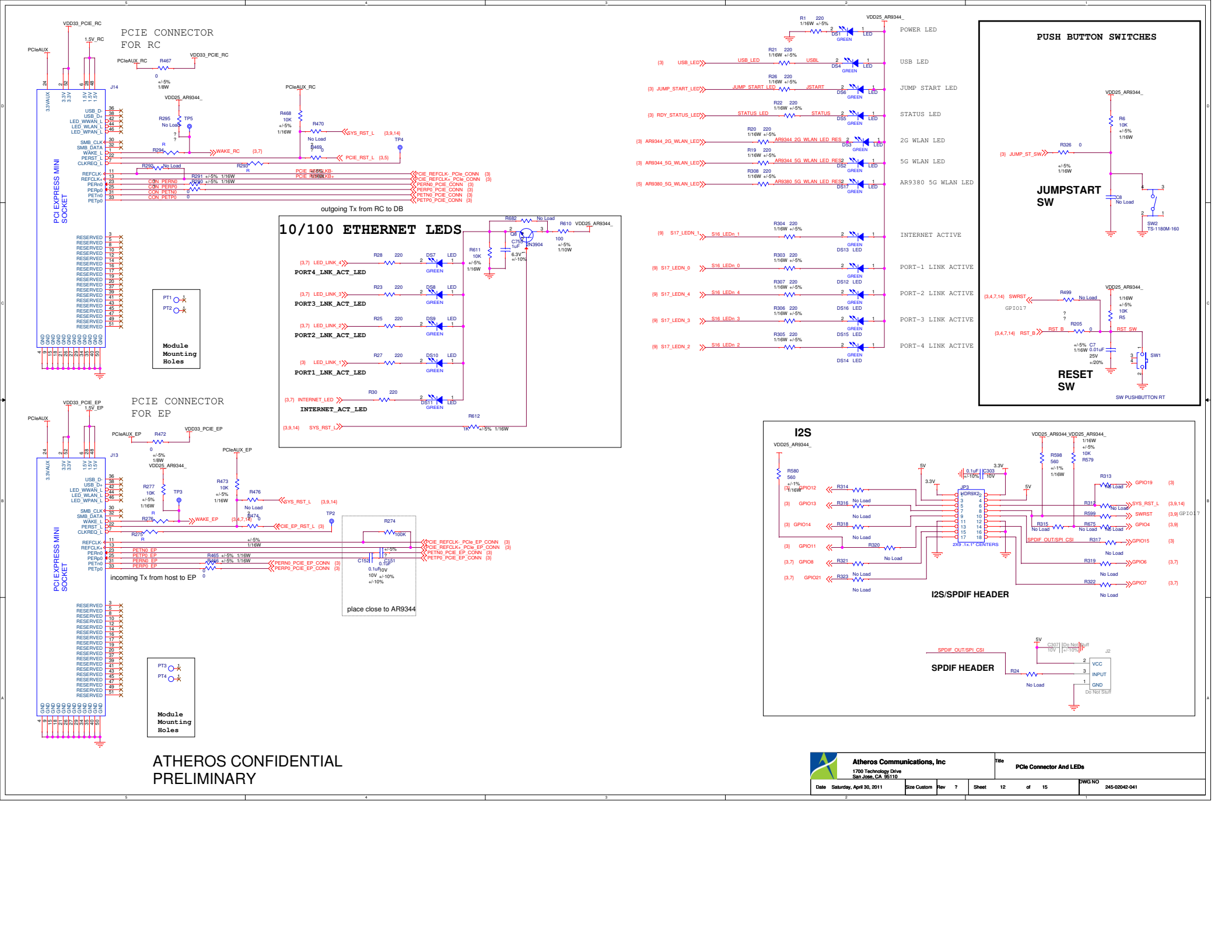
PCIE CONNECTOR FOR RC
PCIE CONNECTOR FOR EP
10/100 ETHERNET LEDS
PORT4_LNK_ACT_LED
PORT3_LNK_ACT_LED
PORT2_LNK_ACT_LED
PORT1_LNK_ACT_LED
INTERNET_ACT_LED
outgoing Tx from RC to DB
incoming Tx from host to EP
place close to AR9344
Module Mounting Holes
POWER LED
USB LED
JUMP START LED
STATUS LED
2G WLAN LED
5G WLAN LED
AR9380 5G WLAN LED
INTERNET ACTIVE
PORT-1 LINK ACTIVE
PORT-2 LINK ACTIVE
PORT-3 LINK ACTIVE
PORT-4 LINK ACTIVE
PUSH BUTTON SWITCHES
JUMPSTART SW
RESET SW
SW PUSHBUTTON RT
I2S
I2S/SPDIF HEADER
SPDIF HEADER
PCI EXPRESS MINI SOCKET
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Atheros Communications, Inc
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PCIe Connector And LEDs
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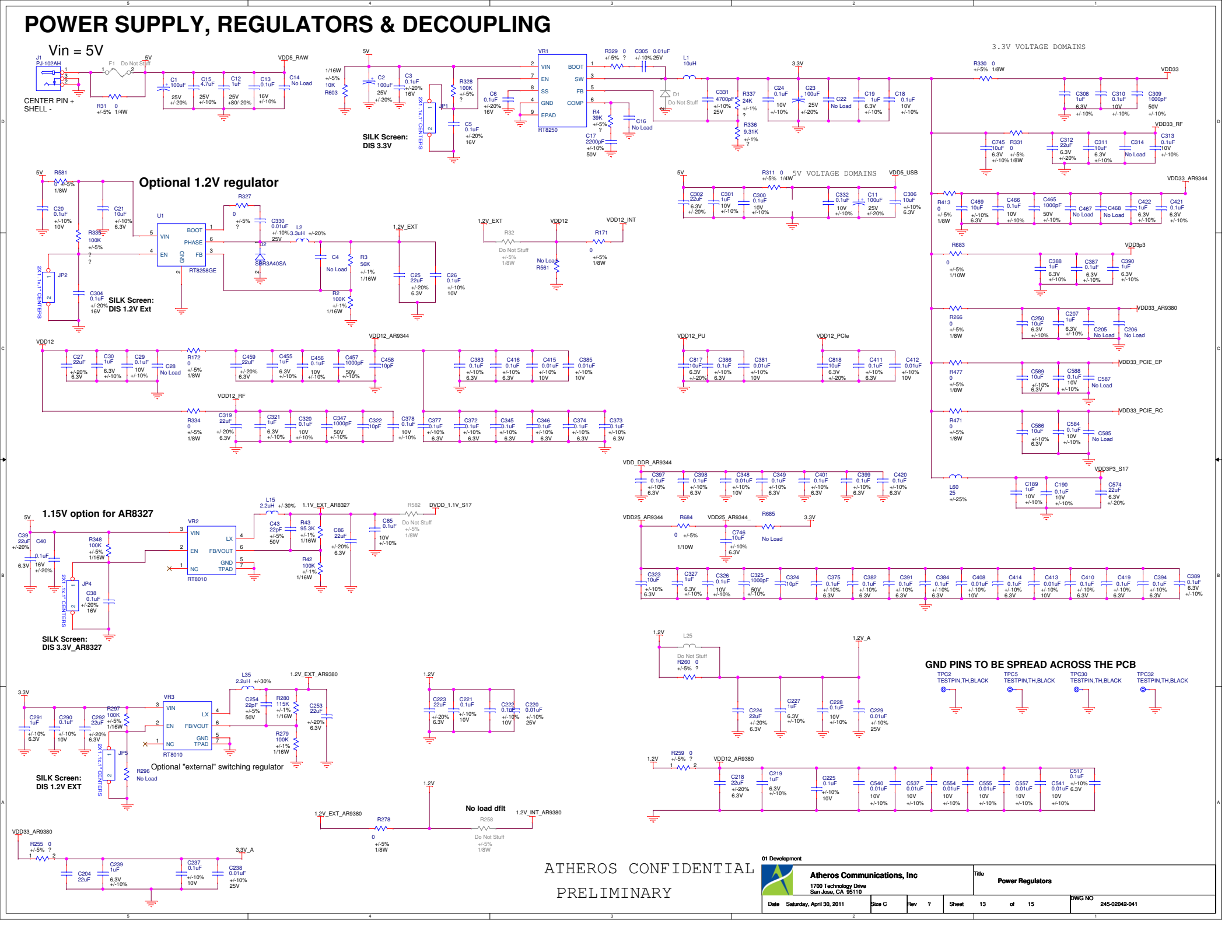
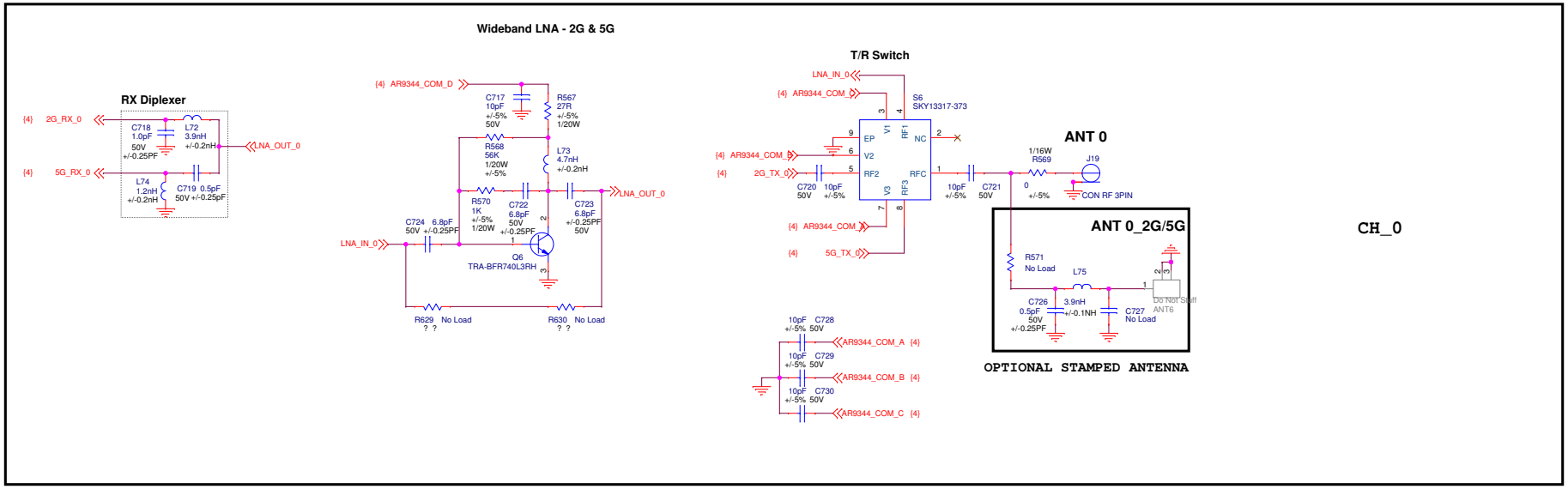
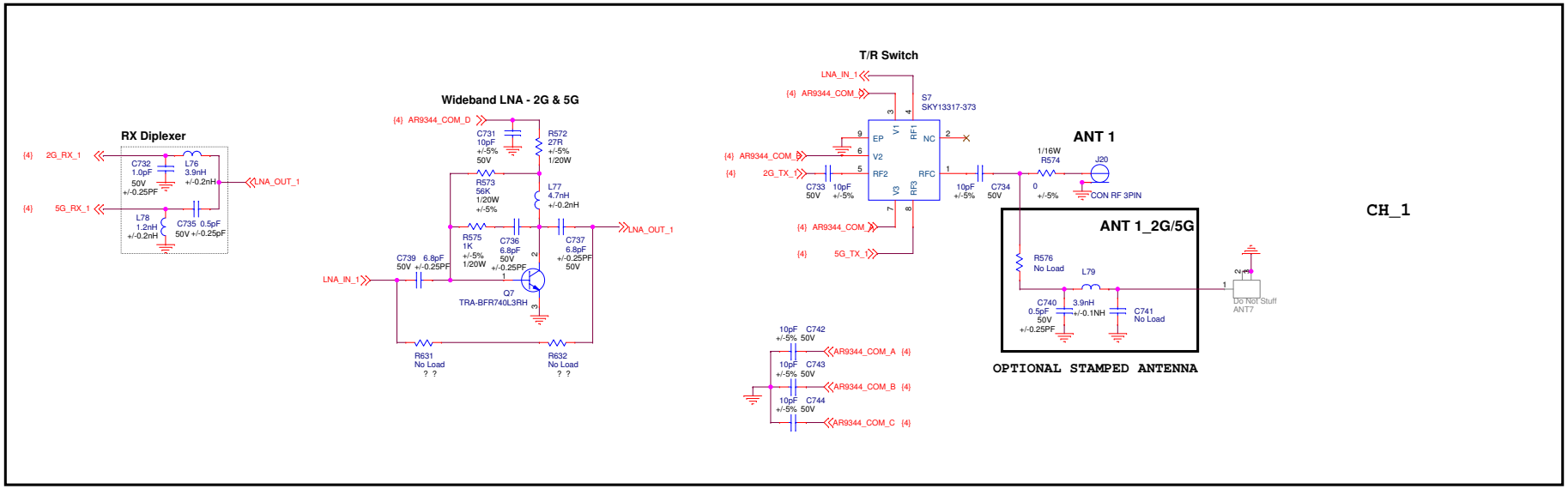
POWER SUPPLY, REGULATORS & DECOUPLING







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Atheros Communications, Inc 1700 Technology Drive San Jose, CA 95110				Title	T/R Switch, Antenna
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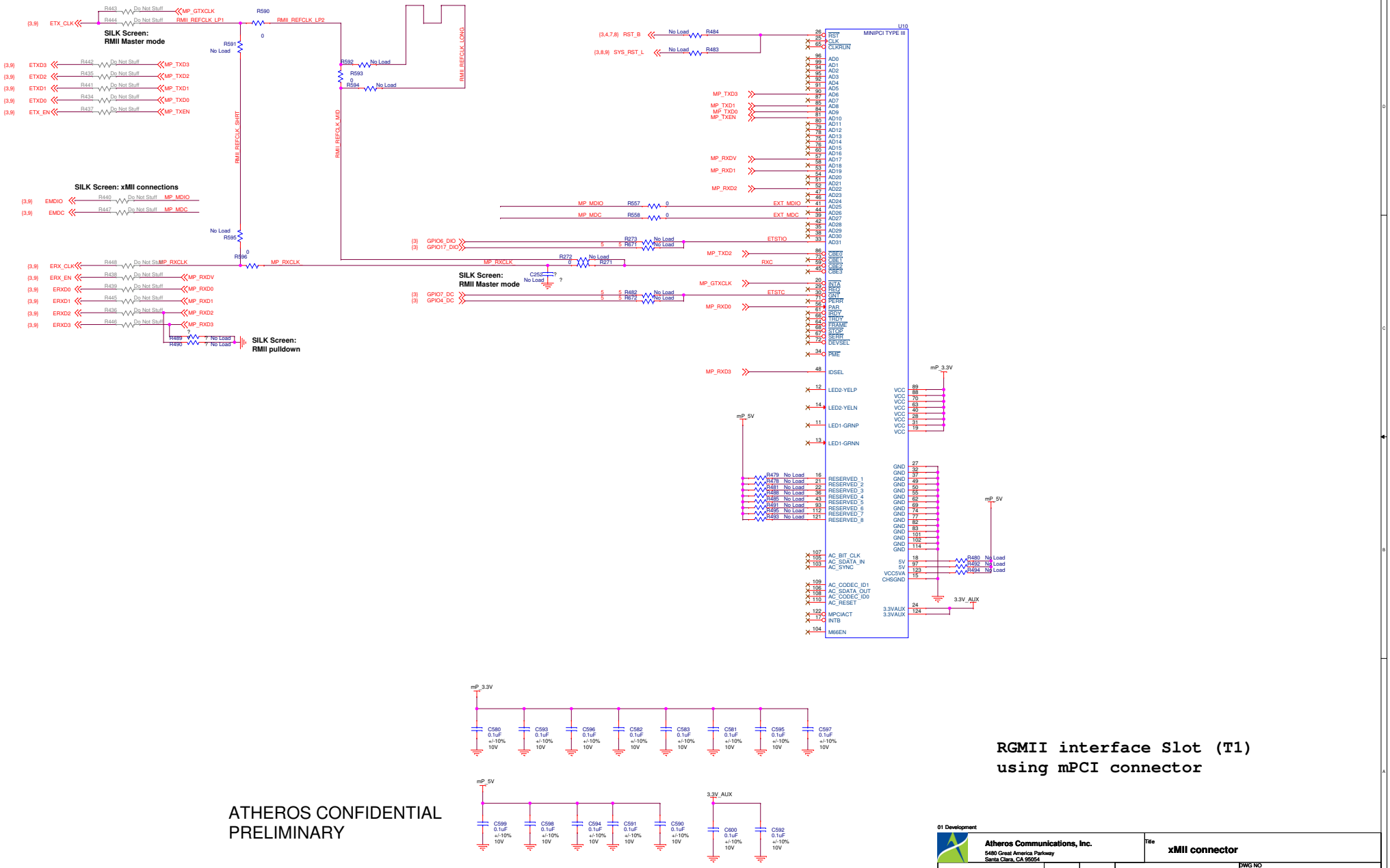

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RGMII interface Slot (T1)
using mPCI connector

01 Development

Atheros Communications, Inc.
5480 Great America Parkway
Santa Clara, CA 95054

Title: xMII connector

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