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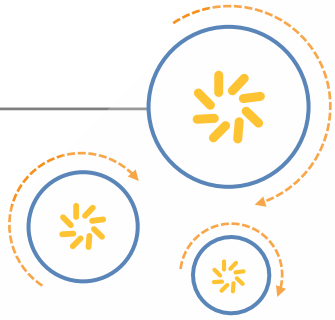

QCA8075 Five-Port 10/100/1000 Mbps Ethernet Transceiver

Hardware Programming Reference

80-Y9112-2 Rev. B

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For additional information or to submit technical questions go to https://createpoint.qti.qualcomm.com/

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Revision History

Revision	Date	Description
A	April 2015	Initial release
B	October 2015	Updated: ■ Chapter 3 □ Section 3.2.1 MII registers ■ Chapter 4 □ Chapter 4 Power-On Strapping ■ Chapter 6 □ Section 6.1.2 Copper auto-negotiation, Section 6.1.5 MDI/MDI-X auto crossover, and Section 6.2.3 Fiber auto-negotiation ■ Chapter 9 □ Section 9.2.2 Hibernation ■ Chapter 11 □ Chapter 11 Wake-On-Line ■ Chapter 16 □ Section 16.4 INTn and INTn_WOL ■ Chapter 17 □ Table 17-1 Register bit types, Table 17-8 PHY identifier 2 register, Table 17-31 Smart speed register, and Table 17-40 Copper hibernation control register

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1 Overview

This Hardware Programming Reference (HPR) document describes how to use the QCA8075 in different working modes and how to configure QCA8075 for the different function tests.

The QCA8075 is a low power, low cost 5-port Gigabit Ethernet PHY chip. The QCA8075 includes two SerDes. one can be configured to PSGMII or QSGMII for connection with MAC. The other can be configured to SGMII for connection with MAC or fiber port combined with copper port 4 to constitute a combo port. The QCA8075 only uses single 3.3 V power supply with integrated switching regulator to achieve optimized RBOM.

2 Management Interface

The QCA8075 supports the management interface defined in the IEEE 802.3 clause 22, provides access to the internal registers of the QCA8075 transceiver via the MDC and MDIO pins. MDC is the management data clock input from the management entity (MAC or SoC). MDIO is the management data input/output that runs synchronously to MDC.

The management interface supports broadcast write operation. If broadcast write is enabled, write command with broadcast address are accepted by all the ports simultaneously. Broadcast write is disabled by default.

The management frame consists of 32-bit preamble, 2-bit start of frame, 2-bit operation code, 5-bit PHY address, 5-bit PHY register address, 2-bit turn around, 16-bit data field and at least 1-bit idle. The frame bits are transmitted in sequence from PRE to IDEL and each bit is triggered on the rising edge of MDC.

Table 2-1 and Table 2-2 show the management interface format.

Table 2-1 Management interface frame fields

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Table 2-2 Management interface field definitions

Field	Definition
PRE	A sequence of 32 contiguous single logic bits on MDIO with corresponding cycles on MDC to provide PHY with a pattern for synchronization.
ST	2-bit start of frame
OP	2-bit operation code. 10 = read transaction, 01 = write transaction
PHYAD	5-bit PHY device address. The bits[2:0] in the PHY address are configured by power-on strapping, thus eight PHYs can be connected to a single management interface. The PHYs connected to the same bus have unique PHY addresses. The first PHY address bit transmitted and received is the MSB of the address.
REGAD	5-bit register address. The 5-bit register address allows 32 registers to be addressed at each PHY. The first register address bit transmitted and received is the MSB of the address.
TA	2-bit field to avoid contention during a read operation. In read operation, both MAC and PHY are at high-impedance state for the first bit time. The PHY drives a zero during the second bit time of the turnaround. In write operation, the MAC must drive 10.

Table 2-2 Management interface field definitions (cont.)

Field	Definition
DATA	16-bit data from accessed register. MSB is transmitted first.
IDLE	High-impedance without driving state of the MDIO. At least one clocked idle state is required between frames.

3 PHY Address and Register

3.1 PHY address allocation

Six register spaces in QCA8075 are for port 0-4 and PSGMII IP separately. Each register space has one dedicated 5-bit PHY address PHYAD[4:0].

The bits[4:3] are determined by power-on strapping configuration. The bits[2:0] are fixed to 0-5 for port 0-4 and PSGMII IP respectively. The PHY addresses are listed as below:

- Port 0 address = xx000 (xx is set by PHYAD[4:3].)
- Port 1 address = port 0 address + 1
- Port 2 address = port 0 address + 2
- Port 3 address = port 0 address + 3
- Port 4 address = port 0 address + 4
- PSGMII address = port 0 address + 5

3.2 Register types

Three types of registers present in QCA8075:

- MII register
- Debug register
- MMD register

3.2.1 MII registers

MII registers are defined by IEEE and can be accessed directly through only one management frame. Refer to MII registers.

3.2.2 Debug registers

Debug registers are defined by Qualcomm Atheros. Refer to Debug registers.

The registers can be accessed indirectly via Debug port — address offset set bit register 0x1D and Debug port — data port bit register 0x1E by 2 steps:

1. Write the offset address of debug register to Debug port — address offset set bit register 0x1D.

2. Read/Write the data from/to Debug port — data port bit register 0x1E.

Example: Writing 0xBC40 to Copper hibernation control register 0xB

1. Write 0xB to Debug port — address offset set bit register 0x1D.
2. Write 0xBC40 to Debug port — data port bit register 0x1E.

3.2.3 MMD registers

IEEE defined MDIO Manageable Device (MMD) register. Refer to "MMD1 registers, MMD3 registers and MMD7 registers". MMD registers can be accessed indirectly via MII register 0xD and 0xE by four steps:

1. Write the device address (1/3/7 for MMD1/3/7) of the MMD register to MMD access control register 0xD.
2. Write the offset address of the MMD register to MMD access address data register 0xE.
3. Remove address operation inMMD access control register 0xD.
4. Read/write the data from/to MMD access address data register 0xE.

Example: Writing 0x8000 to MMD3 — PCS control register 0x0

1. Write 0x3 to MMD access control register 0xD.
2. Write 0x0 to MMD access address data register 0xE.
3. Write 0x4003 to MMD access control register 0xD.
4. Write 0x8000 to MMD access address data register 0xE.

3.3 Register access

To access a certain PHY register space via the management interface, the PHYAD in the management interface frame filed should be equal to this PHY's PHY address. Otherwise, the PHY will not react to the management frame. See Table 2-1. A special PHY address (the broadcast write address) is mentioned in Management Interface. After the broadcast write feature of a certain port is enabled, if the PHYAD in a write command is equal to the broadcast write address, this port will also react to this management frame.

Broadcast write is disabled by default. To enable broadcast write, write 1 to MMD7 — MDIO broadcast control register 0x8028 bit[15]. The default broadcast address is 0x1F, and can be overwritten by writing MMD7 — MDIO broadcast control register 0x8028 bits[4:0]

4 Power-On Strapping

QCA8075 includes 10 LED pins. During hardware reset, these 10 LED pins are used as input for Power-On Strapping (POS) usage. After hardware reset is released, these 10 LED pins are used as output driven by internal PHY status. The POS functions are listed below.

PIN Symbol	POS Configuration bit	Description	Default internal weak pull-up/down
LED_100_0	MODE[0]	MODE[2:0] are latched to configure chip operation mode. ■ 111 = PSGMII □ 5 copper ports ■ 110 = PSGMII □ 4 copper ports + 1 COMBO port (copper/fiber) ■ 101 = QSGMII + SGMII □ 5 copper ports ■ Others = Reserved The operation mode can be overwritten by port4 register 0x1F[2:0].	pull up
LED_1000_0	MODE[1]		pull up
LED_100_1	MODE[2]		pull up
LED_1000_1	PHYAD3	The upper two bits of the physical address are set by PHYAD[4:3]. The PHYAD[2:0] are fixed to 0-5 for ports 0-4 and PSGMII respectively. Refer to PHY address allocation.	pull up
LED_100_2	PHYAD4		pull up
LED_1000_2	CONTROL_DAC0	CONTROL_DAC[2:0] configure power saving scheme in 1000BASE-T mode.	pull up
LED_100_3	CONTROL_DAC1		pull up
LED_1000_3	CONTROL_DAC2		pull up
LED_100_4	AZ_SEL	AZ_SEL is latched to MMD7 register 0x3C bits[2:1] to enable/disable IEEE 802.3az.	pull up
LED_1000_4	Reserved	Must be pulled up.	pull up

5 Operation Mode

QCA8075 supports 3 operation modes as the following which are configured by POS pins or by Chip configuration bit register 0x1F bits[2:0].

5.1 PSGMII application: 5 copper ports

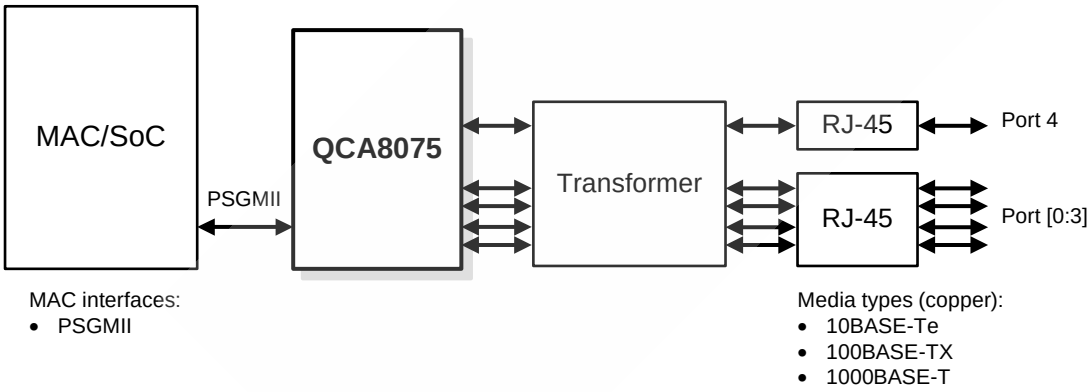


Figure 5-1 PSGMII application: 5 copper ports

Configuration:

POS_MODE[2:0] = 111 or Chip configuration bit register 0x1F bits[2:0] = 000.

5.2 PSGMII application: 4 copper ports and 1 Combo port

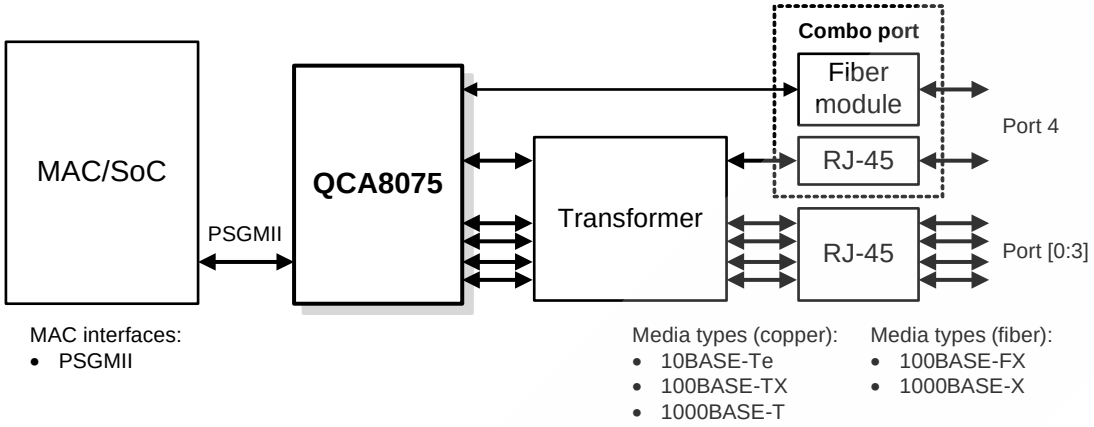


Figure 5-2 PSGMII application: 4 copper ports and 1 Combo port

Configuration:

POS_MODE[2:0] = 110 or Chip configuration bit register 0x1F bits[2:0] = 011.

5.3 QSGMII+SGMII application: 5 copper ports

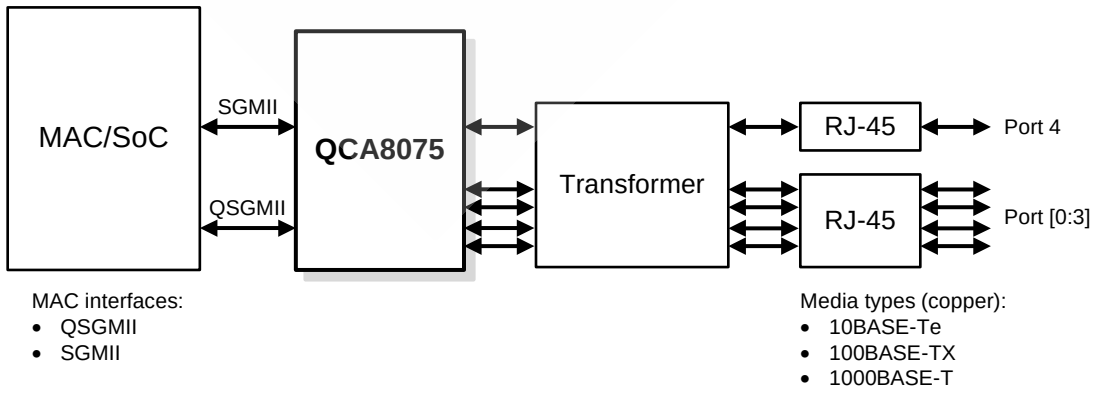


Figure 5-3 QSGMII+SGMII application: 5 copper ports

Configuration:

POS_MODE[2:0] = 101 or Chip configuration bit register 0x1F bits[2:0] = 100.

In this mode, QSGMII is corresponding to port0-3 and SGMII is corresponding to port4.

6 Link Management

6.1 Copper link management

6.1.1 Copper link status

The port link status includes speed, duplex, link and pause which can be read from PHY specific status register — copper page 0x11.

- Bits[15:14] = Speed
- Bit[13] = Duplex
- Bit[10] = Link
- Bit[3] = Transmit pause enabled
- Bit[2] = Received pause enabled

Status register — copper page 0x1 bit[2] can also indicate the link status. Different from PHY specific status register — copper page 0x11 bit[10], this bit is used to indicate whether the link was lost since the last read. If read as 0, it means the link is down. Reading this bit for 2 times continuously can get the real link status.

6.1.2 Copper auto-negotiation

The auto-negotiation function for 10BASE-Te/100BASE-TX/1000BASE-T copper complies with IEEE 802.3 clauses 28 and 40.

Auto-negotiation provides a mechanism to exchange information between a pair of link partners to choose the optimized mode of operation in terms of speed, duplex modes, and Master/Slave preference.

Auto-negotiation is enabled by default. To disable auto-negotiation, write 0 to Control register — copper page 0x0 bit[12].

If auto-negotiation is enabled, configure Auto-negotiation advertisement register — copper page 0x4 and 1000BASE-T control register 0x9 to advertise speed, duplex and pause abilities.

- Auto-negotiation advertisement register — copper page 0x4
  - Bit[11] = Asymmetric pause
  - Bit[10] = PAUSE
  - Bit[8] = 100BASE-TX full-duplex

- Bit[7] = 100BASE-TX half-duplex
- Bit[6] = 10BASE-Te full-duplex
- Bit[5] = 10BASE-Te half-duplex

- 1000BASE-T control register 0x09
  - Bit[9] = 1000BASE-T full-duplex

Table 6-1 Auto-negotiation register configuration

Mode	PHY register 0x04	PHY register 0x09
10/100/1000BASE-T auto-negotiation	0x1DE1	0x200
1000BASE-T full-duplex	0x1C01	0x200
100BASE-TX full-duplex	0x1D01	0x0
100BASE-TX half-duplex	0x1C81	0x0
10BASE-Te full-duplex	0x1C41	0x0
10BASE-Te half-duplex	0x1C21	0x0

If auto-negotiation is disabled, configure Control register — copper page 0x0 bit[13], bit[8] and bit[6] to select speed and duplex modes.

- Bit[13] and bit[6] = Speed
- Bit[8] = Duplex mode

NOTE Force 1000BASE-T is not a common usage and for test purpose only. QCA8075 supports force 1000Base-T only when its link partner is also the Qualcomm Atheros Ethernet PHY.

Table 6-2 Force mode register configuration

Force Mode	PHY register offset 0x00
100BASE-TX full-duplex	0x2100
100BASE-TX half-duplex	0x2000
10BASE-Te full-duplex	0x0100
10BASE-Te half-duplex	0x0000

To restart auto-negotiation, write 0x1200 to Control register — copper page 0x0.

6.1.3 Pause priority resolution

Priority resolution for pause capability is resolved by auto-negotiation. The resolved PAUSE priority is stored in PHY specific status register — copper page 0x11 bits[3:2].

- Bit[3] = TRANSMIT PAUSE ENABLED
  - This bit indicates pause transmit enabled/disabled.

- Bit[2] = RECEIVE PAUSE ENABLED
  - This bit indicates pause receive enabled/disabled.

The auto-negotiation exchanges pause capabilities between the local device and link partner. The local pause capability can be configured and stored in MII register 0x04 bits[11:10]. The link partner's pause capability is stored in Link partner ability register — copper page 0x5 bits[11:10].

- Auto-negotiation advertisement register — copper page 0x4
  - Bit[11] = ASYMMETRIC PAUSE
  - Bit[10] = PAUSE
- Link partner ability register — copper page 0x5
  - Bit[11] = ASYMMETRIC PAUSE
  - Bit[10] = PAUSE

6.1.4 1000BASE-T Master/Slave resolution

The 1000BASE-T PHY can be configured as either Master or Slave. The Master/Slave relationship is resolved during auto-negotiation. The Master/Slave configuration includes both manual configuration and automatic configuration.

To enable automatic Master/Slave configuration, write 0 to 1000BASE-T control register 0x9 bit[12]. If automatic Master/Slave configuration is enabled, configure 1000BASE-T control register 0x9 bit[10] to set preferred port type. In general, a multi-port device is set to be MASTER and a single-port device is set to be SLAVE.

To enable manual Master/Slave configuration, write 1 to 1000BASE-T control register 0x9 bit[12]. If manual Master/Slave configuration is enabled, configure 1000BASE-T control register 0x9 bit[11] to select Master/Slave mode.

- 1000BASE-T control register 0x9
  - Bit[12] = Master/Slave manual configuration enable
  - Bit[11] = Master/Slave configuration
  - Bit[10] = Port type

The Master/Slave resolution result is stored in 1000BASE-T status register 0xA bits[15:14].

- 1000BASE-T status register 0xA
  - Bit[15] = Master/Slave configuration fault
  - Bit[14] = Master/Slave configuration resolution

6.1.5 MDI/MDI-X auto crossover

QCA8075 supports the auto crossover function defined in IEEE 802.3 clause 40.4.4. Automatic MDI/MDI-X configuration is intended to eliminate the need for crossover cables between similar devices.

MDI/MDI-X auto crossover function is enabled by default. To disable MDX/MDI-X auto crossover, write 00 (MDI mode) or 01 (MDI-X mode) to Function control register 0x10 bits[6:5].

- Function control register 0x10
  - Bits[6:5] = MDI crossover mode

To check the MDI/MDI-X crossover status, read PHY specific status register — copper page 0x11 bit[6]. 0 means MDI mode; 1 means MDI-X mode.

- PHY specific status register — copper page 0x11
  - Bit[6] = MDI crossover status

6.1.6 Smart speed downgrade

QCA8075 copper port supports 1000BASE-T, 100BASE-TX and 10BASE-Te. Auto-negotiation will select the highest common ability. With the standard auto-negotiation, if the link cannot be established with the selected ability, auto-negotiation will retry indefinitely.

The smart speed downgrade function introduces a mechanism to downgrade the highest advertised ability to a lower level when auto-negotiation retry reaches a predefined number. The indefinite auto-negotiation retry can be avoided. The predefined maximum retry number can be programmable.

The smart speed function is enabled by default. To disable smart speed function, write 1 to Smart speed register 0x14 bit[5].

To change the predefined maximum retry number, set Smart speed register 0x14 bits[4:2]. The maximum retry number equals (the value of bits[4:2] + 2).

Smart speed register 0x14 bits[4:2] is 0x3 by default. Auto-negotiation will retry 5 times for a higher speed mode, then downgrade to a lower one if it can not link up.

- Smart speed register 0x14
  - Bit[5] = SMARTSPEED_EN
  - Bits[4:2] = SMARTSPEED_RETRY_LIMIT

6.2 Fiber link management

If port 4 works in Combo mode, the fiber port supports both 1000BASE-X and 100BASE-FX defined in IEEE 802.3.

In MII registers, offset addresses (0x0, 0x1, 0x4, 0x5, 0x6 and 0x11) can be used as either copper page or fiber/SGMII page.

To select fiber/SGMII page, write 0 to Chip configuration bit register 0x1F bit[15].

6.2.1 Fiber mode selection

QCA8075 can be programmed to support fiber mode auto-detection. The expected fiber mode is configured by MMD7 — Fiber mode auto-detection register 0x807E bit[0] and Chip configuration bit register 0x1F bit[8].

- If MMD7 — Fiber mode auto-detection register 0x807E bit[0] is set to 1, the port supports auto-detection of fiber mode. In this mode, Chip configuration bit register 0x1F bit[8] is read-only and indicates the auto-detection result.
- If MMD7 — Fiber mode auto-detection register 0x807E bit[0] is set to 0 (default), the port does not support auto-detection of fiber mode. In this mode, configure the Chip configuration bit register 0x1F bit[8] can force the fiber mode to 1000BASE-X or 100BASE-FX.

Chip configuration bit register 0x1F

- Bit[8] = FIBER_MODE_AUTO

MMD7 — Fiber mode auto-detection register 0x807E

- Bit[0] = EN_FIBER_MODE_AD

6.2.2 Fiber link status

The fiber port link status includes speed, duplex, link and pause which can be read from PHY specific status register — fiber/SGMII page 0x11.

- Bits[15:14] = Speed
- Bit[13] = Duplex
- Bit[10] = Link
- Bit[3] = Transmit pause enabled
- Bit[2] = Receive pause enabled

Bit[2] in Status register — fiber/SGMII page 0x1 can also indicate the link status. Different from bit[10], this bit is used to indicate whether the link was lost since the last read. If read as 0, it means link is down. Reading this bit for 2 times continuously can get the real link status.

6.2.3 Fiber auto-negotiation

QCA8075 supports 1000BASE-X auto-negotiation defined in IEEE 802.3 clause 37.

1000BASE-X auto-negotiation is enabled by default. To disable auto-negotiation, write 0 to Control register — fiber/SGMII page 0x0 bit[12].

If 1000BASE-X auto-negotiation is enabled, configure Auto-negotiation advertisement register — fiber/SGMII page 0x4 to advertise duplex and pause abilities.

- Auto-negotiation advertisement register — fiber/SGMII page 0x4
  - Bit[8] = Asymmetric pause
  - Bit[7] = Pause

- Bit[6] = 1000BASE-X half-duplex
- Bit[5] = 1000BASE-X full-duplex

If 1000BASE-X auto-negotiation is disabled, configure Control register — fiber/SGMII page 0x0 bit[8] to select duplex mode.

To restart auto-negotiation, write 0 to Control register — fiber/SGMII page 0x0 bit[9].

6.2.4 Pause priority resolution

Priority resolution for pause capability is resolved by auto-negotiation. The resolved PAUSE priority is stored in PHY specific status register — fiber/SGMII page 0x11 bits[3:2].

Bit[3] indicates pause transmit is enabled/disabled.

- Bit[3] = TRANSMIT PAUSE ENABLED

Bit[2] indicates pause receive is enabled/disabled.

- Bit[2] = RECEIVE PAUSE ENABLED

The auto-negotiation exchanges pause capabilities between the local device and link partner. The local pause capability is configured and stored in Auto-negotiation advertisement register — fiber/SGMII page 0x4 bits[8:7]. The link partner's pause capability is stored in Link partner ability register — fiber/SGMII page 0x5 bits[8:7].

Auto-negotiation advertisement register — fiber/SGMII page 0x4

- Bit[8] = ASYMMETRIC PAUSE
- Bit[7] = PAUSE

Link partner ability register — fiber/SGMII page 0x5

- Bit[8] = ASYMMETRIC PAUSE
- Bit[7] = PAUSE

6.2.5 Unidirectional ability

The QCA8075 transceiver can encode and transmit data from MII/GMII regardless of whether the PHY has determined that a valid link has been established. This feature is usually enabled in carrier products (disabled by default). It is supported only when auto-negotiation is disabled and the PHY operates in full-duplex mode.

Unidirectional ability is disabled by default. To enabled it, write 1 to Control register — fiber/SGMII page 0x0 bit[5].

To check whether the fiber port support unidirectional or not, read Status register — fiber/SGMII page 0x1 bit[7].

7 Combo Port Auto-Media Detection

QCA8075 Combo port supports auto-media detection feature which allows MAC to detect active link partners and process data from copper or fiber interface according to the priority setting and link status.

If the active link partners over both fiber and copper are detected, the port operation mode is defined by priority setting. Priority is configured by Chip configuration bit register 0x1F.

- Bit[10] = PRIORITY_SEL
  - 0 = Copper
  - 1 = Fiber

To check which media is detected, read Media select status register 0x1A bits[5:3].

- Bit5 = 1, means copper media is detected and link up.
- Bit4 = 1, means 1000BASE-X is detected and link up.
- Bit3 = 1, means 100BASE-FX is detected and link up.

8 SGMII/PSGMII/QSGMII Auto-Negotiation

8.1 SGMII auto-negotiation

If QCA8075 works in QSGMII + SGMII mode, the SGMII interface uses auto-negotiation to pass the link information of port 4 to the MAC. The link information transferred during auto-negotiation includes link status, speed mode, duplex mode, link partner's pause ability and asymmetry pause ability.

To disable the SGMII auto-negotiation, write 0 to Control register — fiber/SGMII page 0x0 bit[12].

8.2 PSGMII/QSGMII auto-negotiation

If QCA8075 works in PSGMII/QSGMII mode, the PSGMII/QSGMII interface uses auto-negotiation to pass the copper port link information to the MAC. The link information transferred during auto-negotiation includes link status, speed mode, duplex mode, link partner's pause ability and asymmetry pause ability.

9 Low Power Control

9.1 Copper port

QCA8075 copper port supports the following low power features.

9.1.1 Software power down

QCA8075 copper port supports software power-down mode. To enter the power-down mode, write 1 to Control register — copper page 0x0 bit[11].

9.1.2 Power saving per cable length

The QCA8075 1000BASE-T transceiver supports power saving per cable length. The power saving is done via adjusting analog MDI driver's amplitude and bias current. The power saving scheme is configured by CONTROL_DAC[2:0].

CONTROL_DAC[2:0]

- 000 = Full amplitude; full bias current
- 001 = Amplitude follow DSP (amplitude is adjusted based on cable length); half bias current
- 010 = Full amplitude; bias current follow DSP (bias current is adjusted based on cable length)
- 011 = Both amplitude and bias current follow DSP
- 100 = Full amplitude; half bias current
- 101 = Amplitude follow DSP setting; 1/4 bias current when cable<10m, otherwise half bias current
- 110 = Full amplitude; same bias current setting with “010” and “011”, but half more bias current is reduced when cable <10m
- 111 = Amplitude follow DSP; same bias current setting with “110”

9.1.3 IEEE 802.3AZ

QCA8075 supports both 1000BASE-T EEE and 100BASE-TX EEE by default. To disable EEE ability, write 0 to MMD7 — EEE advertisement register 0x3C bits[2:1].

MMD7 — EEE advertisement register 0x3C

- Bit[2] = Local 1000BASE-T EEE advertisement

- Bit[1] = Local 100BASE-TX EEE advertisement.

After auto-negotiation, the link partner's EEE ability is stored in MMD7 — EEE LP advertisement register 0x3D bits[2:1].

MMD7 — EEE LP advertisement register 0x3D

- Bit[2] = Link partner's 1000BASE-T EEE advertisement
- Bit[1] = Link partner's 100BASE-TX EEE advertisement

EEE auto-negotiation result is stored in MMD7 — EEE capability auto-negotiation results register 0x8000 bits[2:1].

MMD7 — EEE capability auto-negotiation results register 0x8000

- Bit[2] = 1000BASE-T EEE is enabled.
- Bit[1] = 100BASE-TX EEE is enabled.

For each bit, 1 means both sides support EEE operation, and EEE operation is desired; 0 means either side does not support EEE operation for 1000BASE-T, or EEE operation is not desired.

For 1000BASE-T, if both sides support EEE and their MACs forward the Low Power Idle (LPI) pattern, then both sides will enter LPI state simultaneously. For 100BASE-TX, if both sides support EEE and either side's MAC forward LPI pattern, then this side's Tx and the other side's Rx will enter LPI state.

To check LPI status, read MMD3 — PCS status register 0x1 bits[11:8].

MMD3 — PCS status register 0x1

- Bit[11] = Tx LPI received
- Bit[10] = Rx LPI received
- Bit[9] = Tx LPI indication
- Bit[8] = Rx LPI indication

Bits[9:8] indicate the current LPI state and bits[11:10] indicate whether the LPI signals are received since the last read.

9.1.4 Hibernation

The copper port enters hibernation mode in about 10 seconds after cable is unplugged. If the cable is reconnected, the port wakes up to restore normal function.

The copper port hibernation mode is enabled by default. To disable hibernation mode, write 0 to Copper hibernation control register 0xB bit[15].

9.2 Fiber Port

QCA8075 fiber port supports the following low power control features.

9.2.1 Power Down

QCA8075 fiber port supports software power down mode. To enter power down mode, write 1 to Control register — fiber/SGMII page 0x0 bit[11].

9.2.2 Hibernation

QCA8075 fiber port enters the hibernation mode after 1 second if the fiber cable is unplugged and unidirectional ability is disabled.

Fiber port hibernation is enabled by default. To disable fiber hibernation, write 0 to MMD7 — Fiber Hibernation register 0x8005 bit[15].

To check fiber port hibernation status, read MMD7 — Fiber hibernation control register 0x805E bit[12]. Bit[12] is 1 that means fiber port is in hibernation mode.

9.3 SGMII/PSGMII/QSGMII

QCA8075 SGMII/PSGMII/QSGMII support low power mode.

In PSGMII:

- 5 copper ports application
  - If all five copper ports enter hibernation or software power down, the PSGMII interface is shut down and enter the low power mode.
- 4 copper ports + 1 Combo port application
  - If all copper ports and fiber port enter hibernation or software power down, the PSGMII interface is shut down and enter the low power mode.

In QSGMII + SGMII:

- 5 copper ports application
  - If ports 0-3 enter hibernation or software power down, the QSGMII interface is shut down and enter the low power mode.
  - If port 4 enters hibernation or software power down, the SGMII interface is shut down and enter the low power mode.

The PSGMII/QSGMII low power mode is enabled by default. To disable this mode, write 0 to MMD3 — PSGMII SerDes control register 0x805A bit[15].

The SGMII low power mode is enabled by default. To disable this mode, write 0 to MMD7 — SGMII low power control register 0x8012 bit[15].

10 Loopback Mode

Loopback modes are used for test or debug only. Each port of QCA8075 supports 3 different loopback modes:

- Internal loopback (Digital loopback)
- External loopback
- Remote PHY loopback

10.1 Internal Loopback

Internal loopback (also named as digital loopback) loops the transmitted data back to the receiver using digital circuit in QCA8057 shown as Figure 10-1 and Figure 10-2.

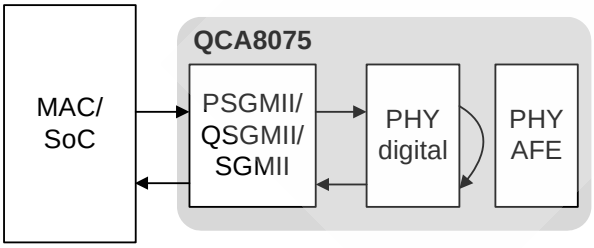


Figure 10-1 Digital loopback, copper port 0 to 4

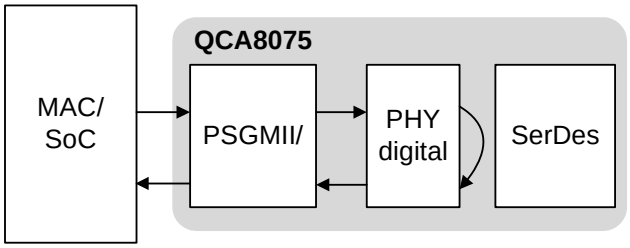


Figure 10-2 Digital loopback, fiber port 4

To configure the copper port internal loopback:

- Copper 1000M loopback: write 0x4140 to Control register — copper page 0x0
- Copper 100M loopback: write 0x6100 to Control register — copper page 0x0
- Copper 10M loopback: write 0x4100 to Control register — copper page 0x0

To configure fiber port internal loopback:

- Fiber 1000M loopback: write 0x4140 to Control register — fiber/SGMII page 0x0
- Fiber 100M loopback: write 0x6100 to Control register — fiber/SGMII page 0x0

10.2 External loopback

External loopback can loop PSGMII/QSGMII/SGMII/MDI Tx back to Rx through the complete digital and analog path and an external cable shown as Figure 10-3 and Figure 10-4.

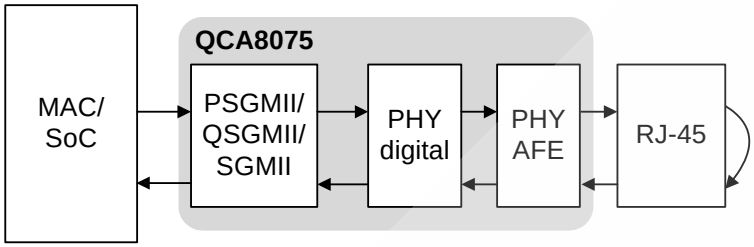


Figure 10-3 External cable loopback, copper port 0 to 4

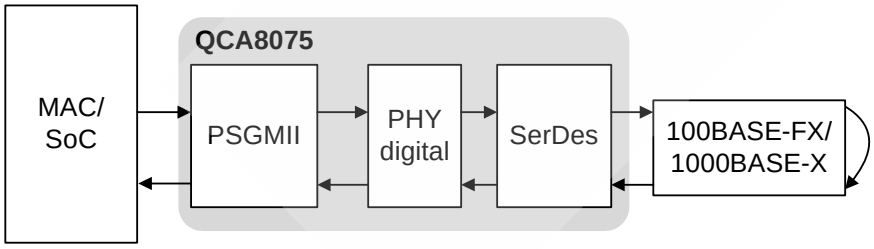


Figure 10-4 External cable loopback, fiber port 4

To configure the copper port external loopback:

1. Plug in an external loopback cable (1 wiring 3, 2 wiring 6, 4 wiring 7, and 5 wiring 8).
2. Set Copper hibernation control register 0xB bit[15] to 0 to disable hibernate mode.
3. Set External loopback control register 0x11 bit[0] to 1 to enable external loopback.
4. Set Control register — copper page 0x0 to select loopback modes:
   - 1000M loopback: Control register — copper page 0x0 = 0x8140
   - 100M loopback: Control register — copper page 0x0 = 0xA100
   - 10M loopback: Control register — copper page 0x0 = 0x8100

NOTE In external loopback mode, if cable is removed and reconnected to 1000 Mbps mode, the Control register — copper page 0x0 must be configured again to 0x8140 to establish the PHY link.

To configure fiber port external loopback:

1. Loop fiber cable Tx to Rx.

10.3 Remote PHY loopback

Remote PHY loopback can loop the GMII/MII RXD to TXD to have the remote link partner detect the connectivity in the loop shown as Figure 10-5 and Figure 10-6.

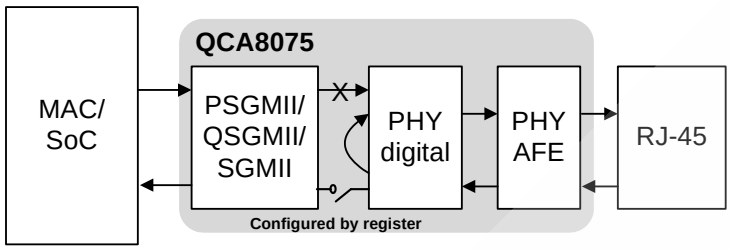


Figure 10-5 Remote PHY loopback, copper port 0 to 4

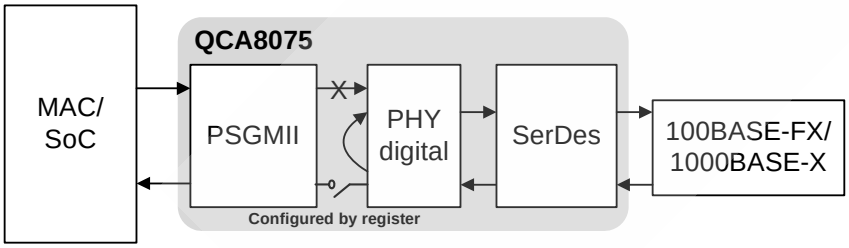


Figure 10-6 Remote PHY loopback, copper port 4

In remote PHY loopback mode, the normal trace from RXD to upper layer is cut off by default, which means the upper layer will not see any frame if the link partner sends frames to QCA8075. This feature is enabled by default. To disable cutting off the trace feature, write 0 to MMD3 — Remote PHY loopback register 0x805A bit[1].

To enable remote PHY loopback, write 1 to MMD3 — Remote PHY loopback register 0x805A bit[0].

11 Wake-On-Line

Wake-on-LAN (WoL) is a mechanism to manage and regulate the total network power consumption.

QCA8075 supports the following WoL features:

- QCA8075 supports automatic detection of a specific frame from any port and notify the receiving of the WOL frame via dedicated hardware interrupt pin INTn_WOL or via common hardware interrupt pin INTn. The specific frame contains a specific data sequence located anywhere inside the packet. The data sequence consists of 6 bytes of consecutive 1 (0xFFFFFFFFFFFF), followed by 16 repetitions of the MAC address of the computer to be waked up. The 48-bit MAC address is written in each port's MMD3 0x804A, 0x804B, 0x804C registers. For example, to write a specific MAC address (0xAAAABBBBCCCC) to PHY, write MMD3 0x804A = 0xAAAA, 0x804B = 0xBBBB, and 0x804C = 0xCCCC. The PHY internal MAC address can be set to any value. This MAC address is not a real MAC address, it is only a symbol to indicate the content of the frame.

  Figure 11-1 shows the WoL system application structure.

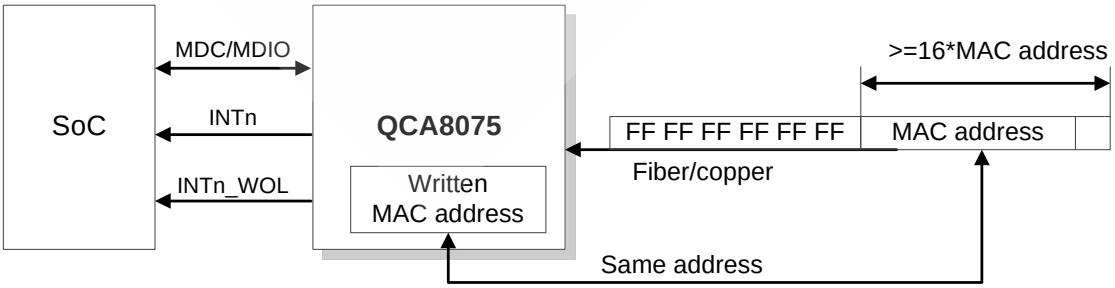


Figure 11-1 WoL application structure

- Two hardware pins can be used for triggering WoL interrupt:
  - Active low signal through the INTn pin. When the interrupt bit in interrupt enable registers 0x12 bit[0] is set to 1, QCA8075 generates interrupt at the reception of WOL packet. See Interrupt enable register — for port 0-3 and Interrupt enable register — for port 4 for details.
  - Active low with pulse width of 32 clock cycles through the INTn_WOL pin at the reception of WOL packet. Clock frequencies for different traffic rates are:
    - 1000 Mbps: 125 MHz
    - 100 Mbps: 25 MHz
    - 10 Mbps: 2.5 MHz

For example, if the link speed is 1000 Mbps, the clock frequency is 125 MHz and the clock cycle is 8 ns, the WOL is active with a 32 × 8 ns low pulse.

When WOL interrupt occurs, bit[0] in interrupt status registers 0x13 is set to 1. This bit is cleared after read operation. See Interrupt status register — for port 0-3 and Interrupt status register — for port 4 for details.

When bit[0] in interrupt enable registers 0x12 is set to 1, the external INTn pin is triggered when interrupt occurs. See Interrupt enable register — for port 0-3 and Interrupt enable register — for port 4 for details.

When bit[0] in interrupt enable registers 0x12 is set to 0, the external INTn pin cannot be triggered even when this interrupt occurs. See Interrupt enable register — for port 0-3 and Interrupt enable register — for port 4 for details.

The WOL function is enabled by default. To disable WOL, write 0 to MMD3 — Wake-on-LAN control register 0x8012 bit[5].

12 CRC Checker

The CRC checker is used to perform CRC check for each ingress and egress packet at PHY, and maintains counters for correct and corrupted packets. The CRC checker is illustrated in Figure 12-1 and Figure 12-2 for copper mode and fiber mode.

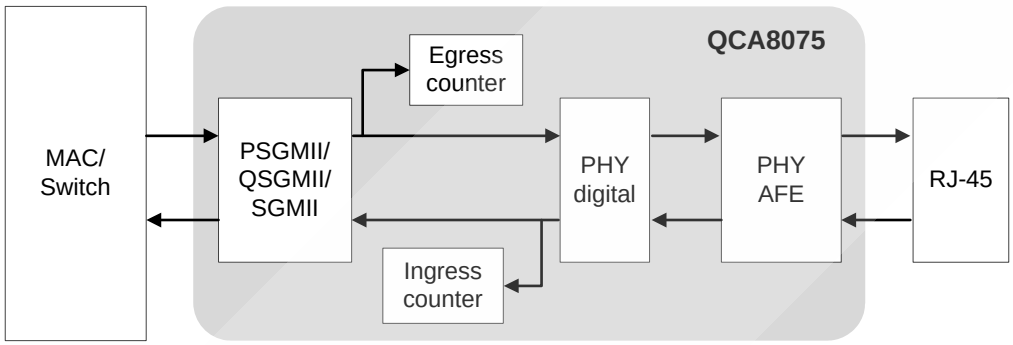


Figure 12-1 CRC checker, copper mode

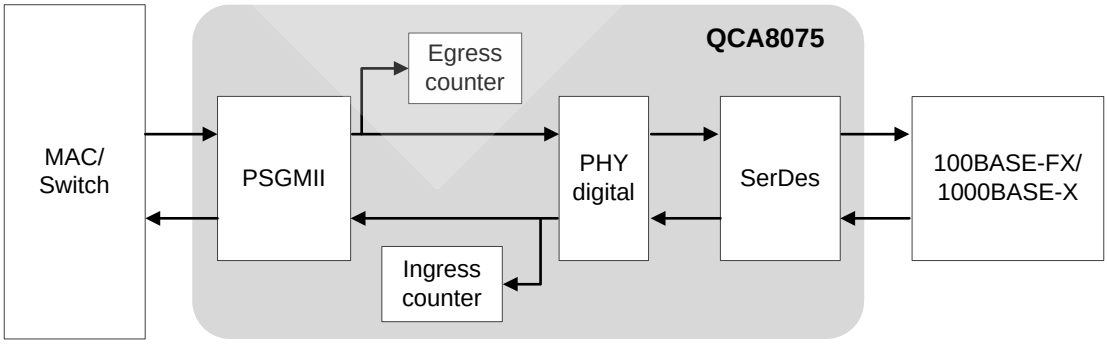


Figure 12-2 CRC checker, fiber mode

To perform CRC check:

1. Write 1 to MMD7 — CRC checker and packet counter register 0x8029 bit[0] to enable CRC checker for both ingress and egress traffics.
2. Read the MMD7 registers 0x802A-0x802F to check packet counters.
    a. MMD7 — Valid ingress packet counter 1 register 0x802A and MMD7 — Valid ingress packet counter 2 register 0x802B indicate the number of ingress packet with good CRC. MMD7 — Erred ingress packet counter register 0x802C indicates the number of ingress packet with corrupted CRC.

b. MMD7 — Valid egress packet counter 1 register 0x802D and MMD7 — Valid egress packet counter 2 register 0x802E indicate the number of egress packet with good CRC. MMD7 — Erred egress packet counter register 0x802F indicates the number of egress packet with corrupted CRC.

3. The counters are not clear-on-read by default. To enable clear-on-read, write 1 to MMD7 — CRC checker and packet counter register 0x8029 bit[1].

13 Cable Diagnostic Test

The Cable Diagnostic Test (CDT) can be performed when no link partner is present. DSP algorithm is used to measure the cable length when the link partner is performing auto-negotiation.

To perform CDT test:

1. Write 1 to Cable diagnostic test control register 0x16 bit[15] to enable CDT.
2. Read MMD3 — Cable diagnostics register 0x8064 to check cable status.
   - Bits[15:12] indicate the cable status for pair0.
   - Bits[11:8] indicate the cable status for pair1.
   - Bits[7:4] indicate the cable status for pair2.
   - Bits[3:0] indicate the cable status for pair3.
3. Read MMD3 — Cable diagnostics pair 0 length register 0x8065, MMD3 — Cable diagnostics pair 1 length register 0x8066, MMD3 — Cable diagnostics pair 2 length register 0x8067 and MMD3 — Cable diagnostics pair 3 length register 0x8068 to check the length information of cable pairs connected to MDI pair 0, 1, 2, and 3.
   - Bits[15:8] indicate the distance between inter-pair short point and the PHY.
   - Bits[7:0] indicate the distance between intra-pair short point and the PHY.

14 SGMII/PSGMII/QSGMII Drive Control

14.1 SGMII drive control

SGMII SerDes has programmable Tx driver strength. The output differential voltage (Vdiff, pp) can be configured by MMD7 — SGMII drive control register 0x8011 bits[15:13].

- 000 = 500 mV
- 001 = 600 mV (Default)
- 010 = 700 mV
- 011 = 800 mV
- 100 = 900 mV
- 101 = 1 V
- 110 = 1.1 V
- 111 = 1.2 V
- Others = Reserved

14.2 PSGMII/QSGMII drive control

PSGMII/QSGMII SerDes has programmable Tx driver strength. The output differential voltage (Vdiff, pp) can be configured by PSGMII/QSGMII drive control 1 register 0xB bits[7:4].

- 1010 = 400 mV
- 1011 = 500 mV
- 1100 = 600 mV (Default)
- 1101 = 700 mV
- 1110 = 800 mV
- 1111 = 900 mV
- Others = Reserved

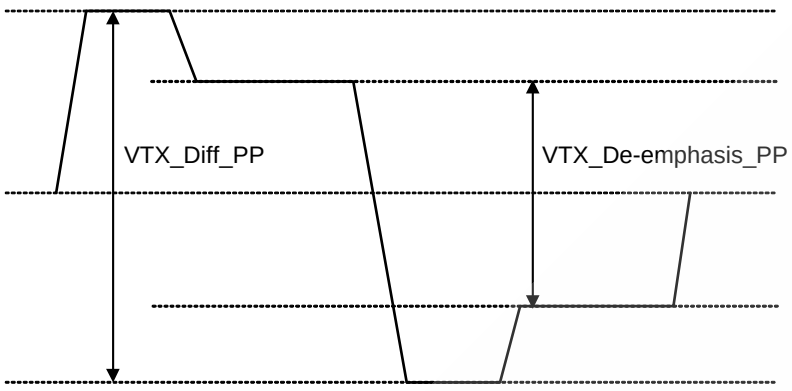
PSGMII/QSGMII SerDes supports programmable transmit de-emphasis. The de-emphasis is to compensate for the transmission loss due to long PCB traces.

To control PSGMII/QSGMII de-emphasis level, set PSGMII/QSGMII drive control 2 register 0xC bits[1:0].

- 00 = No de-emphasis

- 01 = -1.6dB de-emphasis (Default)
- 10 = -3.5dB de-emphasis
- 11 = -6dB de-emphasis

Figure 14-1 shows the PSGMII/QSGMII de-emphasis.



TXDe-emphasis (Db) = -20log (VTX_Diff_PP/VTX_De-emphasis_PP)

Figure 14-1 PSGMII/QSGMII de-emphasis

15 PRBS Test

QCA8075 supports PRBS test on PSGMII/QSGMII/SGMII interface. The PRBS is used to test the quality of high speed serial transmission line.

To perform SGMII PRBS test:

1. Write 1 to SGMII PBRS control register 0x1B bit[15] to enable PRBS generator to generate random bit stream.
2. Write 1 to SGMII PBRS control register 0x1B bit[14] to enable PRBS receiver to check bit stream.
3. Read MMD7 — PRBS error count 2 register 0x800F bit[15] to check PRBS sync status.
   - If this bit is 0, the PRBS pattern is not synced and test is invalid.
   - If this bit is 1, the PRBS pattern is synced, then read MMD7 — PRBS error count 2 register 0x800F bits[14:0], MMD7 — PRBS error count 1 register 0x800E bits[15:0], the 31-bit is the PRBS error counter.

To perform PSGMII/QSGMII PRBS test:

1. Write 1 to MMD1 — PSGMII/QSGMII PRBS control register 0x54 bit[1] to enable PRBS generator to generate random bit stream.
2. Write 1 to MMD1 — PSGMII/QSGMII PRBS control register 0x54 bit[2] to enable PRBS receiver to check bit stream.
3. Read MMD1 — PSGMII PRBS error count 2 register 0x53 bit[15] to check PRBS sync status.
   - If this bit is 0, the PRBS pattern is not synced and test is invalid.
   - If this bit is 1, the PRBS pattern is synced, then read MMD1 — PSGMII PRBS error count 2 register 0x53 bits[14:0], MMD1 — PSGMII PRBS error count 1 register 0x52 bits[15:0], the 31-bit is the error counter.

16 Digital Pin Control

QCA8075 includes total 16 digital pins:

- 10 LED pins: support 2.7 V I/O with 3.3 V tolerance
- MDC/MDIO, RESETn, INTn, INTn_WOL and LOS: support 1.5 V/1.8 V/2.7 V I/O

If pin VDD15_REG is connected to pin VDD25_REG, 2.7 V I/O with 3.3 V tolerance is used; if not, 1.5 V/1.8 V is used. Default is 1.8 V. To select 1.5 V, write 0 to PHY control debug 0 register 0x1F bit[3].

16.1 LED control

QCA8075 includes 10 status LED pins, two for each port. Each LED pin can be programmed to force on/off/blink or to indicate the port status such as link, speed, active and collision.

- To force LED_100_n on/off/blink, configure MMD7 — LED_100_n control 2 register 0x8075 bits[15:13].
- To force LED_1000_n on/off/blink, configure MMD7 — LED_1000_n control 2 register 0x8077 bits[15:13].

MMD7 — LED_100_n control 1 register 0x8074 can be programmed to control LED_100_n for indicating the copper port status. The default configuration indicates the link and active status of 10BASE-Te and 100BASE-TX.

MMD7 — LED_1000_n control 1 register 0x8076 can be programmed to control LED_1000_n for indicating the copper port status. The default configuration indicates link and active status of 1000BASE-T.

MMD7 — LED_100_n control 2 register 0x8075 bits[12:0] can be programmed to control LED_100_n for indicating the fiber port 4 status. The default configuration indicates link and active status of 100BASE-FX.

MMD7 — LED_1000_n control 2 register 0x8077 bits[12:0] can be programmed to control LED_1000_n for indicating the fiber port 4 status. The default configuration indicates link and active status of 1000BASE-X.

The LED blink frequency and duty cycle can be programmed by MMD7 — Global LED control bit description 0x8073. The default blink frequency is 4 Hz and the default duty cycle is 50%.

16.2 MDIO control

The MDIO pin is normal I/O by default and can be configured to open drain by writing 1 to MMD7 — PAD control register 0x8016 bit[6]. If used as normal I/O, the MDIO can have the programmable output drive ability. To adjust MDIO output drive ability, configure MMD7 — PAD control register 0x8016 bits[5:4].

16.3 LOS control

The LOS pin is open drain by default and can be configured to normal output by writing MMD7 — PAD control register 0x8016 bit[7].

16.4 INTn and INTn_WOL

QCA8075 includes two interrupt pins, INTn and INTn_WOL, which are used as interrupt function by default and can be configured to GPIO by writing 0 to MMD7 — PAD control register 0x8016 bit[12].

If used as interrupt function, INTn and INTn_WOL are open-drain output, active low and can be configured to normal I/O, active low by writing 0 to MMD7 — PAD control register 0x8016 bit[8].

- INTn_WOL is dedicated for WOL. Refer to Wake-On-Line.
- INTn is the global interrupt output pin.

Two interrupt registers can be used to configure the interrupt signals:

- Interrupt enable register — for port 0-3 0x12 and Interrupt enable register — for port 4 0x12
- Interrupt status register — for port 0-3 0x13 and Interrupt status register — for port 4 0x13

When an enabled interrupt condition (configured in Interrupt enable register — for port 0-3 and Interrupt enable register — for port 4) takes place, the corresponding status bits in Interrupt status register — for port 0-3 and Interrupt status register — for port 4 can be set and the INTn pin is driven low until the interrupt is cleared. The interrupt is cleared automatically by reading the Interrupt status register — for port 0-3 and Interrupt status register — for port 4.

If INTn is used as GPIO:

1. Configure MMD7 — PAD control register 0x8016 bit[13] to set the direction of GPIO 1.
   - 1 = Output
   - 0 = Input
2. If output direction is selected, configure MMD7 — PAD control register 0x8016 bit[14] to change the output value.
   - 1 = Output high
   - 0 = Output low

3. If input direction is selected, read MMD7 — PAD control register 0x8016 bit[15] to check the input value.
   - 1 = Input high
   - 0 = Input low

If INTn_WOL is used as GPIO:

1. Configure MMD7 — PAD control register 0x8016 bit[9] to set the direction of GPIO 2.
   - 1 = Output
   - 0 = Input
2. If output direction is selected, configure MMD7 — PAD control register 0x8016 bit[10] to change the output value.
   - 1 = Output high
   - 0 = Output low
3. If input direction is selected, read MMD7 — PAD control register 0x8016 bit[11] to check the input value.
   - 1 = Input high
   - 0 = Input low

17 Registers

17.1 Register bit type

Table 17-1 shows the register bit types.

Table 17-1 Register bit types

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs.
Retain	Value written to a register field takes effect without a software reset.
SC	Self-clear. Writing a one to this register causes the desired function to execute immediately, and the register field clears to zero when the function is complete.
Update	The value written to the register field can not be read and does not take effect until a software reset is executed.
RO	Read Only
R/W	Read/Write

17.2 MII registers

Table 17-2 summarizes the QCA8075 MII registers.

Table 17-2 MII registers summary

Address	Description
0x0	“Control register — copper page” on page 44
0x0	“Control register — fiber/SGMII page” on page 45
0x1	“Status register — copper page” on page 46
0x1	“Status register — fiber/SGMII page” on page 48
0x2	“PHY identifier 1 register” on page 49
0x3	“PHY identifier 2 register” on page 49
0x4	“Auto-negotiation advertisement register — copper page” on page 50
0x4	“Auto-negotiation advertisement register — fiber/SGMII page” on page 53

Table 17-2 MII registers summary (cont.)

Address	Description
0x5	“Link partner ability register — copper page” on page 54
0x5	“Link partner ability register — fiber/SGMII page” on page 55
0x6	“Auto-negotiation expansion register — copper page” on page 56
0x6	“Auto-negotiation expansion register — fiber/SGMII page” on page 57
0x7	“Next page transmit register” on page 58
0x8	“Link partner next page register” on page 58
0x9	“1000BASE-T control register” on page 60
0xA	“1000BASE-T status register” on page 63
0xB	“PSGMII/QSGMII drive control 1 register” on page 64
0xC	“PSGMII/QSGMII drive control 2 register” on page 64
0xD	“MMD access control register” on page 65
0xE	“MMD access address data register” on page 65
0xF	“Extended status register” on page 65
0x10	“Function control register” on page 66
0x11	“PHY specific status register — copper page” on page 67
0x11	“PHY specific status register — fiber/SGMII page” on page 69
0x12	“Interrupt enable register — for port 0-3” on page 70
0x12	“Interrupt enable register — for port 4” on page 71
0x13	“Interrupt status register — for port 0-3” on page 71
0x13	“Interrupt status register — for port 4” on page 72
0x14	“Smart speed register” on page 73
0x14	“Fiber/SGMII control register” on page 74
0x16	“Cable diagnostic test control register” on page 75
0x1A	“Media select status register” on page 75
0x1B	“SGMII PBRS control register” on page 76
0x1D	“Debug port — address offset set bit register” on page 76
0x1E	“Debug port — data port bit register” on page 76
0x1F	“Chip configuration bit register” on page 77

17.2.1 Control register — copper page

Offset: 0x0

Table 17-3 Control register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
15	RESET	R/W	0x0	Retain	PHY software reset Writing '1' to this bit causes the PHY reset operation. After the reset is done, this bit is cleared to '0' automatically. The reset occurs immediately. ■ 1 = PHY reset ■ 0 = Normal operation
14	LOOPBACK	R/W	0x0	Retain	PHY internal loopback When loopback is enabled, data on TXD is looped back to RXD. ■ 1 = Enable Loopback ■ 0 = Disable Loopback
13	SPEED_ SELECTION_ LSB	R/W	0x0	Retain	Link speed can be selected via either the auto-negotiation process or manual speed selection. Manual speed selection is allowed when auto-negotiation is disabled by setting bit[12] to 0. This bit is used in conjunction with bit[13] to select the speed of operation. Force_speed = {bit[6], this bit}: ■ 00 = 10 Mbps ■ 01 = 100 Mbps ■ 10 = 1000 Mbps ■ 11 = Reserved
12	AUTO_ NEGOTIATION	R/W	0x1	Retain	■ 1 = Enable auto-negotiation process ■ 0 = Disable auto-negotiation process
11	POWER_ DOWN	R/W	0x0	Retain	When the port is switched from power down to normal operation, software reset and restart auto-negotiation are performed, even when bit[15] and bit[9] are not set by the user. In power down mode, shut off the Base-T analog end. ■ 1 = Power down ■ 0 = Normal operation
10	Reserved	R/O	0x0	Retain	–
9	RESTART_ AUTO_ NEGOTIATION	R/W	0x0	Retain	Auto-negotiation automatically restarts after hardware or software reset regardless of whether the bit[9] is set or not. ■ 1 = Restart auto-negotiation process ■ 0 = Normal operation

Table 17-3 Control register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
8	DUPLEX_ MODE	R/W	0x0	Retain	The duplex mode can be selected via either the auto-negotiation process or manual duplex selection. Manual duplex selection is allowed when auto-negotiation is disabled by setting bit[12] to 0. ■ 0 = Half-duplex ■ 1 = Full-duplex
7	Reserved	R/O	0x0	Retain	
6	SPEED_ SELECTION_ MSB	R/W	0x1	Retain	See this register bit[13].
5:0	Reserved	R/O	0x0	Retain	Always be 0.

17.2.2 Control register — fiber/SGMII page

Offset: 0x0

Table 17-4 Control register — fiber/SGMII page

Bit	Field	Access type	HW reset	SW reset	Description
15	RESET	R/W	0x0	Retain	PHY software reset Writing a '1' to this bit causes the PHY the reset operation is done, this bit is cleared to '0' automatically. The reset occurs immediately. ■ 1= PHY reset ■ 0 =Normal operation
14	LOOPBACK	R/W	0x0	Retain	100BASE-FX, 1000BASE-X, SGMII loopback When loopback is activated, 10-bit TXD to SerDes is looped back to 10-bit RXD. ■ 1 = Enable loopback ■ 0 = Disable loopback
13	SPEED_ SELECTION_ LSB	R/W	0x0	Retain	For SGMII only. Force_speed {bit[6], this bit}: ■ 00 = 10 Mbps ■ 01 = 100 Mbps ■ 10 = 1000 Mbps ■ 11 = Reserved The force speed is only valid when bit[12] is 0 and Fiber/SGMII control register 0x14 bit[0] is 1.
12	AUTO_ NEGOTIATION	R/W	0x1	Retain	For 1000BASE-X, SGMII. ■ 1 = Enable auto-negotiation process ■ 0 = Disable auto-negotiation process No auto-negotiation in 100BASE-FX.

Table 17-4 Control register — fiber/SGMII page

Bit	Field	Access type	HW reset	SW reset	Description
11	POWER_DOWN	R/W	0x0	0	For 100BASE-FX, 1000BASE-X, SGMII. When the port is switched from power down to normal operation, software reset and restart auto-negotiation are performed even when bit[5] and bit[9] are not set by the user. ■ 1 = Power down, shut off SerDes ■ 0 = Normal operation
10	Reserved	R/O	0x0	Retain	–
9	RESTART_AUTO_NEGOTIATION	R/W	0x0	1	For 1000BASE-X, SGMII. Auto-negotiation automatically restarts after hardware or software reset regardless of whether the this bit is set or not. ■ 1 = Restart auto-negotiation process ■ 0 = Normal operation
8	DUPLEX_MODE	R/W	0x1	Retain	Take effect in 1000BASE-X auto-negotiation disable mode (bit[12] = 0), or 100BASE-FX mode. ■ 1 = Full-duplex ■ 0 = Half-duplex
7	Reserved	R/O	0x0	Retain	–
6	SPEED_SELECTION_MSB	R/W	0x1	Retain	See bit[13].
5	UNIDIRECTION	R/W	0x0	Retain	■ 1 = Enable unidirection function (valid when bit[12] is 0) ■ 0 = Disable
4:0	Reserved	R/O	0x0	Retain	–

17.2.3 Status register — copper page

Offset: 0x1

Table 17-5 Status register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
15	100BASE-T4	R/O	0x0	Retain	Always be 0. ■ 1 = PHY supports 100BASE-T4. ■ 0 = PHY does not support 100BASE-T4.
14	100BASE-TX_FULL-DUPLEX	R/O	0x1	Retain	Always be 1. ■ 1 = PHY supports 100BASE-TX full-duplex. ■ 0 = PHY does not support 100BASE-TX full-duplex.

Table 17-5 Status register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
13	100BASE-TX_ HALF-DUPLEX	R/O	0x1	Retain	Always be 1. ■ 1 = PHY supports 100BASE-TX half-duplex. ■ 0 = PHY does not support 100BASE-TX half-duplex.
12	10BASE-TE_ FULL-DUPLEX	R/O	0x1	Retain	Always be 1. ■ 1 = PHY supports 10BASE-Te full-duplex. ■ 0 = PHY does not support 10BASE-Te full-duplex.
11	10BASE-TE_ HALF-DUPLEX	R/O	0x1	Retain	Always be 1. ■ 1 = PHY supports 10BASE-Te half-duplex. ■ 0 = PHY does not support 10BASE-Te half-duplex.
10	100BASE-T2_ FULL-DUPLE	R/O	0x0	Retain	Always be 0. ■ 1 = PHY supports 100BASE-T2. ■ 0 = PHY does not support 100BASE-T2.
9	100BASE-T2_ HALF-DUPLEX	R/O	0x0	Retain	Always be 0. ■ 1 = PHY supports 100BASE-T2. ■ 0 = PHY does not support 100BASE-T2.
8	EXTENDED_ STATUS	R/O	0x1	Retain	Always be 1. ■ 1 = Extended status information in Extended status register 0xF ■ 0 = No extended status information in Extended status register 0xF
7	Reserved	R/O	0x0	Retain	Always be 0.
6	MF_ PREAMBLE_ SUPPRESSIO N	R/O	0x1	Retain	Always be 1. ■ 1 = PHY accepts management frames with preamble suppressed. ■ 0 = PHY does not accept management frames with preamble suppressed.
5	AUTO_ NEGOTIATION _COMPLETE	R/O	0x0	Retain	■ 1 = Auto-negotiation process is complete. ■ 0 = Auto-negotiation process is not complete.
4	REMOTE_ FAULT	R/O	0x0	Retain	■ 1 = Remote fault condition is detected. ■ 0 = Remote fault condition is not detected.
3	AUTO_ NEGOTIATION _ABILITY	R/O	0x1	Retain	Always be 1. ■ 1 = Able to perform auto-negotiation. ■ 0 = Not able to perform auto-negotiation.

Table 17-5 Status register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
2	LINK_STATUS	R/O	0x0	Retain	This register bit indicates whether the link was lost since the last read. For the current link status, read PHY specific status register — copper page 0x11 bit[10]. ■ 1 = Link is up. ■ 0 = Link is down.
1	JABBER_ DETECT	R/O	0x0	Retain	■ 1 = Jabber condition is detected. ■ 0 = Jabber condition is not detected.
0	EXTENDED_ CAPABILITY	R/O	0x1	Retain	Always be 1. ■ 1 = Extended register capabilities ■ 0 = Basic register set capabilities only

17.2.4 Status register — fiber/SGMII page

Offset: 0x1

Table 17-6 Status register — fiber/SGMII page

Bit	Field	Access type	HW reset	SW reset	Description
15	Reserved	R/O	0x0	Retain	–
14	FX100_FULL_ DUPLEX	R/O	0x1	Retain	Capable of 100BASE-FX full-duplex operation
13	FX100_HALF_ DUPLEX	R/O	0x1	Retain	Capable of 100BASE-FX full-duplex operation
12:9	Reserved	R/O	0x0	Retain	–
8	EXTENDED_ STATUS	R/O	0x1	Retain	Extended status information in PHY specific status register — fiber/SGMII page 0xF
7	UNIDIRECTIO NAL_ABILITY	R/O	0x1	Retain	PHY has the uni-direction ability.
6	MF_ PREAMBLE_ SUPPRESSIO N	R/O	0x1	Retain	PHY accepts management frames with preamble suppressed.
5	AUTO_ NEGOTIATION _COMPLETE	R/O	0x0	Retain	■ 1 = Auto-negotiation process is complete. ■ 0 = Auto-negotiation process is not complete.
4	REMOTE_ FAULT	R/O	0x0	Retain	■ 1 = Remote fault condition is detected. ■ 0 = Remote fault condition is not detected.
3	AUTO_ NEGOTIATION _ABILITY	R/O	0x1	Retain	■ 1 = 1000BASE-X is able to perform auto-negotiation. Always be 1.

Table 17-6 Status register — fiber/SGMII page

Bit	Field	Access type	HW reset	SW reset	Description
2	LINK_STATUS	R/O	0x0	Retain	This bit indicates whether the 1000BASE-X and 100BASE-FX link is lost since the last read. For the current link status, read PHY specific status register — copper page 0x11 bit[10]. ■ 1 = Link is up ■ 0 = Link is down
1	Reserved	R/O	0x0	Retain	–
0	EXTENDED_ CAPBILITY	R/O	0x1	Retain	■ 1 = Extended register capabilities Always be 1.

17.2.5 PHY identifier 1 register

Offset: 0x2

Table 17-7 PHY identifier 1 register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	OUI_ BITS[3:18]	R/O	0x4D	Retain	Organizationally unique identifier bits[18:3] Always be 0x004D.

17.2.6 PHY identifier 2 register

Offset: 0x3

Table 17-8 PHY identifier 2 register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	OUI_BITS_ MSB [19:24], MODEL_ NUMBER, REVISION_ NUMBER	R/O	0xD0B0	Retain	Organizationally unique identifier bits[19:24] Always be 0xD0B1.

17.2.7 Auto-negotiation advertisement register — copper page

Offset: 0x4

Table 17-9 Auto-negotiation advertisement register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
15	NEXT_PAGE	R/W	0x0	Retain	The value of this bit can be updated immediately after writing this register. But the value written to this bit does not take effect until any one of the following occurs: ■ Software reset is asserted. (Control register — copper page 0x0 bit[15]) ■ Restart auto-negotiation is asserted. (Control register — copper page 0x0 bit[9]) ■ Power down (Control register — copper page 0x0 bit[11]) transitions from power down to normal operation ■ Link goes down. If 1000BASE-T is advertised, then the required next pages are automatically transmitted. This bit should be set to 0 if no additional next pages are needed. ■ 1 = Advertise ■ 0 = Not advertised
14	ACK	R/O	0x0	Retain	Always be 0.
13	REMOTE_ FAULT	R/W	0x0	Retain	■ 1 = Set Remote Fault bit. ■ 0 = Do not set Remote Fault bit.
12	XNP_ABLE	R/W	0x1	Retain	Extended next page enable control bit ■ 1 = Local device supports transmission of extended next pages. ■ 0 = Local device does not support transmission of extended next pages. This bit is updated immediately after the writing operation. However, the configuration does not take effect until any of the following occurs: ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Restart auto-negotiation is triggered by writing Control register — copper page 0x0 bit[9]. ■ The port is switched from power down to normal operation by writing Control register — copper page 0x0 bit[11]. ■ Link goes down.

Table 17-9 Auto-negotiation advertisement register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
11	ASYMMETRIC_PAUSE	R/W	0x1	Retain	■ 1 = Asymmetric Pause ■ 0 = No asymmetric Pause The value of this bit can be updated immediately after writing this register. But the value written to this bit does not take effect until any one of the following occurs: ■ Software reset is asserted. (Control register — copper page 0x0 bit[15]) ■ Restart auto-negotiation is asserted. (Control register — copper page 0x0 bit[9]) ■ Power down (Control register — copper page 0x0 bit[11]) transitions from power down to normal operation ■ Link goes down.
10	PAUSE	R/W	0x1	Retain	■ 1 = MAC PAUSE is implemented. ■ 0 = MAC PAUSE is not implemented. The value of this bit can be updated immediately after writing this register. But the value written to this bit does not take effect until any one of the following occurs: ■ Software reset is asserted. (Control register — copper page 0x0 bit[15]) ■ Restart auto-negotiation is asserted. (Control register — copper page 0x0 bit[9]) ■ Power down (Control register — copper page 0x0 bit[11]) transitions from power down to normal operation ■ Link goes down.
9	100BASE_T4	R/O	0x0	Retain	Always be 0. ■ 1 = Able to perform 100BASE-T4. ■ 0 = Not able to perform 100BASE-T4.
8	100BASE-X_FULL-DUPLEX	R/W	0x1	Retain	■ 1 = Advertise ■ 0 = Not advertised The value of this bit can be updated immediately after writing this register. But the value written to this bit does not take effect until any one of the following occurs: ■ Software reset is asserted. (Control register — copper page 0x0 bit[15]) ■ Restart auto-negotiation is asserted. (Control register — copper page 0x0 bit[9]) ■ Power down (Control register — copper page 0x0 bit[11]) transitions from power down to normal operation ■ Link goes down.

Table 17-9 Auto-negotiation advertisement register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
7	100BASE-X_ HALF-DUPLEX	R/W	0x1	Retain	■ 1 = Advertise ■ 0 = Not advertised The value of this bit can be updated immediately after writing this register. But the value written to this bit does not take effect until any one of the following occurs: ■ Software reset is asserted. (Control register — copper page 0x0 bit[15]) ■ Restart auto-negotiation is asserted. (Control register — copper page 0x0 bit[9]) ■ Power down (Control register — copper page 0x0 bit[11]) transitions from power down to normal operation ■ Link goes down.
6	10BASE-TE_ FULL-DUPLEX	R/W	0x1	Retain	■ 1 = Advertise ■ 0 = Not advertised The value of this bit can be updated immediately after writing this register. However, the value written to this bit does not take effect until any one of the following occurs: ■ Software reset is asserted. (Control register — copper page 0x0 bit[15]) ■ Restart auto-negotiation is asserted. (Control register — copper page 0x0 bit[9]) ■ Power down (Control register — copper page 0x0 bit[11]) transitions from power down to normal operation ■ Link goes down.

Table 17-9 Auto-negotiation advertisement register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
5	10BASE-TE_ HALF-DUPLEX	R/W	0x1	Retain	■ 1 = Advertise ■ 0 = Not advertised The value of this bit can be updated immediately after writing this register. However, the value written to this bit does not take effect until any one of the following occurs: ■ Software reset is asserted (Control register — copper page 0x0 bit[15]) ■ Restart auto-negotiation is asserted (Control register — copper page 0x0 bit[9]) ■ Power down (Control register — copper page 0x0 bit[11]) transitions from power down to normal operation ■ Link goes down.
4:0	SELECTOR_ FIELD	R/O	0x1	Retain	Selector Field mode Always be 00001. 00001 = 802.3

17.2.8 Auto-negotiation advertisement register — fiber/SGMII page

Offset: 0x4

Table 17-10 Auto-negotiation advertisement register — fiber/SGMII page

Bit	Field	Access type	HW reset	SW reset	Description
15	NEXT_PAGE	R/W	0x0	Retain	This bit indexes if the additional next pages are needed. ■ 1 = Advertise ■ 0 = Not advertised
14	Reserved	R/O	0x0	Retain	–
13:12	REMOTE_ FAULT	R/W	0x0	Retain	■ 00 = LINK_OK ■ 10 = LINK_FAILURE ■ 11 = AUTO_ERROR
11:9	Reserved	R/O	0x0	Retain	–
8	ASYMMETRIC _PAUSE	R/W	0x3	Retain	■ 1 = Asymmetric pause ■ 0 = No asymmetric pause
7	PAUSE	R/W	0x3	Retain	■ 1 = MAC PAUSE is implemented. ■ 0 = MAC PAUSE is not implemented.
6	1000BASE-X_ HALF-DUPLEX	R/W	0x0	Retain	1000BASE-X half-duplex ability

Table 17-10 Auto-negotiation advertisement register — fiber/SGMII page

Bit	Field	Access type	HW reset	SW reset	Description
5	1000BASE-X_ FULL-DUPLEX	R/W	0x1	Retain	1000BASE-X full-duplex ability
4:0	Reserved	R/O	0x0	Retain	–

17.2.9 Link partner ability register — copper page

Offset: 0x5

Table 17-11 Link partner ability register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
15	NEXT_PAGE	R/O	0x0	Retain	Received code word bit[15] ■ 1 = Link partner supports next page. ■ 0 = Link partner does not support next page.
14	ACK	R/O	0x0	Retain	Acknowledge received code word bit[14] ■ 1 = Link partner received link code word. ■ 0 = Link partner does not receive link code word.
13	REMOTE_ FAULT	R/O	0x0	Retain	Remote fault received code word bit[13] ■ 1 = Link partner detected remote fault. ■ 0 = Link partner does not detected remote fault.
12	Reserved	R/O	0x0	Retain	Technology ability field Received code word bit[12]
11	ASYMMETRIC _PAUSE	R/O	0x0	Retain	Technology ability field Received code word bit[11] ■ 1 = Link partner requests asymmetric pause. ■ 0 = Link partner does not request asymmetric pause.
10	PAUSE	R/O	0x0	Retain	Technology ability field Received code word bit[10] ■ 1 = Link partner supports pause operation. ■ 0 = Link partner does not support of pause operation.
9	100BASE-T4	R/O	0x0	Retain	Technology ability field Received code word bit[9] ■ 1 = Link partner supports 100BASE-T4. ■ 0 = Link partner does not support 100BASE-T4.

Table 17-11 Link partner ability register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
8	100BASE-TX_ FULL-DUPLEX	R/O	0x0	Retain	Technology ability field Received code word bit[8] ■ 1 = Link partner supports 100BASE-TX full-duplex. ■ 0 = Link partner does not support 100BASE-TX full-duplex.
7	100BASE-TX_ HALF-DUPLEX	R/O	0x0	Retain	Technology ability field Received code word bit[7] ■ 1 = Link partner supports 100BASE-TX half-duplex. ■ 0 = Link partner does not support 100BASE-TX half-duplex.
6	10BASE-TE_ FULL-DUPLEX	R/O	0x0	Retain	Technology ability field Received code word bit[6] ■ 1 = Link partner supports 10BASE-Te full-duplex. ■ 0 = Link partner does not support 10BASE-Te full-duplex.
5	10BASE-TE_ HALF-DUPLEX	R/O	0x0	Retain	Technology ability field Received code word bit[5] ■ 1 = Link partner supports 10BASE-Te half-duplex. ■ 0 = Link partner does not support 10BASE-Te half-duplex.
4:0	SELECTOR_ FIELD	R/O	0x0	Retain	Selector field Received code word bits[4:0]

17.2.10 Link partner ability register — fiber/SGMII page

Offset: 0x5

Table 17-12 Link partner ability register — fiber/SGMII page

Bit	Field	Access type	HW reset	SW reset	Description
15	NEXT_PAGE	R/O	0x0	Retain	Received code word bit[15] ■ 1 = Link partner supports Next Page ■ 0 = Link partner does not support Next Page
14	ACK	R/O	0x0	Retain	Acknowledge Received code word bit[14] ■ 1 = Link partner received link code word ■ 0 = Link partner failed to receive link code word

Table 17-12 Link partner ability register — fiber/SGMII page

Bit	Field	Access type	HW reset	SW reset	Description
13:12	REMOTE_ FAULT	R/O	0x0	Retain	Remote fault Received code word bits[13:12] ■ 00 = LINK_OK ■ 01 = LINK_FAILURE ■ 10 = OFFLINE ■ 11 = AUTO_ERROR
11:9	Reserved	R/O	0x0	Retain	–
8	ASYMMETRIC _PAUSE	R/O	0x0	Retain	Technology ability field Received code word bit[8] ■ 1 = Link partner requests asymmetric pause ■ 0 = Link partner does not request asymmetric pause
7	PAUSE	R/O	0x0	Retain	Technology ability field Received code word bit[7] ■ 1 = Link partner supports pause operation ■ 0 = Link partner does not support pause operation
6	1000_BASE-X_ HALF-DUPLEX	R/O	0x0	Retain	Technology ability field Received code word bit[6] ■ 1 = Link partner supports 1000BASE-X half-duplex ■ 0 = Link partner does not support 1000BASE-X half-duplex
5	1000_BASE-X_ FULL-DUPLEX	R/O	0x0	Retain	Technology ability field Received code word bit[6] ■ 1 = Link partner supports 1000BASE-X full-duplex ■ 0 = Link partner does not support 1000BASE-X full-duplex
4:0	Reserved	R/O	0x0	Retain	–

17.2.11 Auto-negotiation expansion register — copper page

Offset: 0x6

Table 17-13 Auto-negotiation expansion register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
15:5	Reserved	R/O	0x0	Retain	Always be 0.
4	PARALLEL_ DETECTION_ FAULT	R/O	0x0	Retain	■ 1 = A fault is detected. ■ 0 = No fault is detected.

Table 17-13 Auto-negotiation expansion register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
3	LP_NEXT_ PAGE_ABLE	R/O	0x0	Retain	■ 1 = Link partner supports next page. ■ 0 = Link partner does not support next page.
2	LOCAL_ NEXT_PAGE_ ABLE	R/O	0x0	Retain	■ 1 = Local device supports next page. ■ 0 = Local device does not support next page.
1	PAGE_ RECEIVED	R/O	0x0	Retain	■ 1 = A new page is received. ■ 0 = No new page is received.
0	LP_AUTO_ NEG_ABLE	R/O	0x0	Retain	■ 1 = Link partner supports auto-negotiation. ■ 0 = Link partner does not support auto-negotiation.

17.2.12 Auto-negotiation expansion register — fiber/SGMII page

Offset: 0x6

Table 17-14 Auto-negotiation expansion register — fiber/SGMII page

Bit	Field	Access type	HW reset	SW reset	Description
15:4	Reserved	R/O	0x0	Retain	Always be 0.
3	LP_NEXT_ PAGE_ABLE	R/O	0x0	Retain	For 1000BASE-X, SGMII. ■ 1 = Link partner supports next page. ■ 0 = Link partner does not support next page.
2	LOCAL_ NEXT_PAGE_ ABLE	R/O	0x0	Retain	For 1000BASE-X, SGMII. ■ 1 = Local device supports next page. ■ 0 = Local device does not support next page.
1	PAGE_ RECEIVED	R/O	0x0	Retain	For 1000BASE-X, SGMII. ■ 1 = A new page has been received. ■ 0 = No new page is received.
0	MR_PAGE_RX	R/O	0x0	Retain	For 1000BASE-X, SGMII. ■ 1 = A new page has been received. ■ 0 = No new page is received.

17.2.13 Next page transmit register

Offset: 0x7

Table 17-15 Next page transmit register

Bit	Field	Access type	HW reset	SW reset	Description
15	TX_NEXT_PAGE	R/W	0x0	Retain	Transmit code word bit[15] ■ 1 = The page is not the last page. ■ 0 = The page is the last page.
14	Reserved	R/O	0x0	Retain	Transmit code word bit[14]
13	MESSAGE_PAGE_MODE	R/W	0x1	Retain	Transmit code word bit[13] ■ 1 = Message page ■ 0 = Unformatted page
12	ACK2	R/W	0x0	Retain	Transmit code word bit[12] ■ 1 = Comply with message. ■ 0 = Cannot comply with message.
11	TOGGLE	R/O	0x1	Retain	Transmit code word bit[11] ■ 1 = This bit in the previously exchanged code word is logic 0. ■ 0 = The toggle bit in the previously exchanged code word is logic 1.
10:0	MESSAGE/UNFORMATTED_FIELD	R/W	0x1	Retain	Transmit code word bits[10:0] These bits are encoded as message code field when Next page transmit register 0x7 bit[13] is set to 1, or as unformatted code field when Next page transmit register 0x7 bit[13] is set to 0.

17.2.14 Link partner next page register

Offset: 0x8

Table 17-16 Link partner next page register

Bit	Field	Access type	HW reset	SW reset	Description
15	NEXT_PAGE	R/O	0x0	Retain	Received code word bit[15] ■ 1 = This page is not the last page. ■ 0 = This page is the last page.
14	Reserved	R/O	0x0	Retain	Received code word bit[14]
13	MESSAGE_PAGE_MODE	R/O	0x0	Retain	Received code word bit[13] ■ 1 = Message page ■ 0 = Unformatted page
12	ACK2	R/O	0x0	Retain	Received code word bit[12] ■ 1 = Comply with message. ■ 0 = Cannot comply with message.

Table 17-16 Link partner next page register

Bit	Field	Access type	HW reset	SW reset	Description
11	TOGGLE	R/O	0x0	Retain	Received code word bit[11] ■ 1 = This bit in the previously exchanged code word is logic 0. ■ 0 = The toggle bit in the previously exchanged code word is logic 1.
10:0	MESSAGE/UNFORMATTED_FIELD	R/O	0x0	Retain	Received code word bits[10:0] These bits are encoded as message code field when bit (0x8[13]) is set to 1, or as unformatted code field when bit(0x8[13]) is set to 0.

17.2.15 1000BASE-T control register

Offset: 0x9

Table 17-17 1000BASE-T control register

Bit	Field	Access type	HW reset	SW reset	Description
15:13	TEST_MODE	R/W	0x0	Retain	The TX_TCLK signals from the RX_CLK pin is for jitter testing in test mode 2 and 3. When exiting the test mode, hardware reset or software reset through writing Control register — copper page 0x0 bit[15] must be performed to ensure the normal operation. ■ 000 = Normal mode ■ 001 = Test mode 1 □ Transmit waveform test ■ 010 = Test mode 2 □ Transmit jitter test (MASTER mode) ■ 011 = Test mode 3 □ Transmit jitter test (SLAVE mode) ■ 100 = Test mode 4 □ Transmit distortion test ■ Others = Reserved
12	MASTER/SLAVE_MANUAL_CONFIG_ENABLE	R/W	0x0	Retain	■ 1 = Manual MASTER/SLAVE configuration ■ 0 = Automatic MASTER/SLAVE configuration The value of this bit will be updated immediately after writing this register. However, the value written to this bit does not take effect until any one of the following occurs: ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Restart auto-negotiation is triggered by writing Control register — copper page 0x0 bit[9]. ■ The port is switched from power down to normal operation by writing Control register — copper page 0x0 bit[11]. ■ Link goes down.

Table 17-17 1000BASE-T control register

Bit	Field	Access type	HW reset	SW reset	Description
11	MASTER/SLAVE_CONFIG	R/W	0x0	Retain	The value of this bit will be updated immediately after writing this register. However, the value written to this bit does not take effect until any one of the following occurs: ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Restart auto-negotiation is triggered by writing Control register — copper page 0x0 bit[9]. ■ The port is switched from power down to normal operation by writing Control register — copper page 0x0 bit[11]. ■ Link goes down. This bit can be ignored if bit[12] is 0. ■ 1 = Manual configure as MASTER ■ 0 = Manual configure as SLAVE
10	PORT_TYPE	R/W	0x1	Retain	The value of this bit will be updated immediately after writing this register. However, the value written to this bit does not take effect until any one of the following occurs: ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Restart auto-negotiation is triggered by writing Control register — copper page 0x0 bit[9]. ■ The port is switched from power down to normal operation by writing Control register — copper page 0x0 bit[11]. ■ Link goes down. This bit can be ignored if bit[12] is 1. ■ 1 = Prefer multi-port device (MASTER) ■ 0 = Prefer single port device (SLAVE)

Table 17-17 1000BASE-T control register

Bit	Field	Access type	HW reset	SW reset	Description
9	1000BASE-T_ FULL-DUPLEX	R/W	0x1	Retain	■ 1 = Advertise ■ 0 = Not advertised The value of this bit will be updated immediately after writing this register. However, the value written to this bit does not take effect until any one of the following occurs: ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Restart auto-negotiation is triggered by writing Control register — copper page 0x0 bit[9]. ■ The port is switched from power down to normal operation by writing Control register — copper page 0x0 bit[11]. ■ Link goes down.
8	1000BASE-T_ HALF-DUPLEX	R/W	0x0	Retain	■ 1 = Advertise ■ 0 = Not advertised The value of this bit will be updated immediately after writing this register. However, the value written to this bit does not take effect until any one of the following occurs: ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Restart auto-negotiation is triggered by writing Control register — copper page 0x0 bit[9]. ■ The port is switched from power down to normal operation by writing Control register — copper page 0x0 bit[11]. ■ Link goes down.
7:0	Reserved	R/W	0x0	Retain	Must be 0.

17.2.16 1000BASE-T status register

Offset: 0xA

Table 17-18 1000BASE-T status register

Bit	Field	Access type	HW reset	SW reset	Description
15	MASTER/SLAVE_CONFIG_FAULT	R/O	0x0	Retain	This register bit will clear on read operation. ■ 1 = Master/Slave configuration fault is detected. ■ 0 = No fault is detected.
14	MASTER/SLAVE_CONFIG_RESOLUTION	R/O	0x0	Retain	This bit is not valid unless the Auto-negotiation expansion register — copper page 0x6 bit[1] is 1. ■ 1 = Local PHY configuration resolved to Master ■ 0 = Local PHY configuration resolved to Slave
13	LOCAL_RECEIVER_STATUS	R/O	0x0	Retain	■ 1 = Local receiver is OK. ■ 0 = Local receiver is not OK.
12	REMOTE_RECEIVER_STATUS	R/O	0x0	Retain	■ 1 = Remote receiver is OK. ■ 0 = Remote receiver is not OK.
11	LP_1000BASE-T_FULL-DUPLEX_CAPABILITY	R/O	0x0	Retain	This bit is not valid unless the Auto-negotiation expansion register — copper page 0x6 bit[1] is 1. ■ 1 = Link partner supports 1000BASE-T full duplex. ■ 0 = Link partner does not support 1000BASE-T full duplex.
10	LP_1000BASE-T_HALF-DUPLEX_CAPABILITY	R/O	0x0	Retain	This bit is not valid unless the Auto-negotiation expansion register — copper page 0x6 bit[1] is 1. ■ 1 = Link Partner supports 1000Base-T half duplex. ■ 0 = Link Partner does not support 1000Base-T half duplex.
9:8	Reserved	R/O	0x0	Retain	Always be 0.
7:0	IDEL_ERROR_COUNT	R/O	0x0	Retain	MSB of idle error counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and does not roll over.

17.2.17 PSGMII/QSGMII drive control 1 register

Offset: 0xB

Table 17-19 PSGMII/QSGMII drive control 1 register

Bit	Field	Access type	HW reset	SW reset	Description
15:8	Reserved	R/W	0x0	Retain	–
7:4	TX_DRIVER	R/W	0xC	Retain	TX driver amplitude adjustment ■ 0000, Vpp_diff = 140 mV ■ 0001, Vpp_diff = 160 mV ■ 0010, Vpp_diff = 180 mV ■ 0011, Vpp_diff = 200 mV ■ 0100, Vpp_diff = 220 mV ■ 0101, Vpp_diff = 240 mV ■ 0110, Vpp_diff = 260 mV ■ 0111, Vpp_diff = 280 mV ■ 1000, Vpp_diff = 300 mV ■ 1001, Vpp_diff = 320 mV ■ 1010, Vpp_diff = 400 mV ■ 1011, Vpp_diff = 500 mV ■ 1100, Vpp_diff = 600 mV
3:0	Reserved	R/W	0xA	Retain	–

1. This register is available in PSGMII IP only.

17.2.18 PSGMII/QSGMII drive control 2 register

Offset: 0xC

Table 17-20 PSGMII/QSGMII drive control 2 register

Bit	Field	Access type	HW reset	SW reset	Description
15:2	Reserved	R/W	0x0	Retain	–
1:0	REG_PSGMII_TX_EMP_LVL	R/W	0x1	Retain	De-emphasis level control code from digital ■ 00 = No de-emphasis ■ 01 = -1.6 dB ■ 10 = -3.5 dB ■ 11 = -6 dB

1. This register is available in PSGMII IP only.

17.2.19 MMD access control register

Offset: 0xD

Table 17-21 MMD access control register

Bit	Field	Access type	HW reset	SW reset	Description
15:14	FUNCTION	R/W	0x0	Retain	■ 00 = Address ■ 01 = Data (no post increment) ■ 10 = Data (post increment on reads and writes) ■ 11 = Data (post increment on writes only)
13:5	Reserved	R/O	0x0	Retain	Always be 0.
4:0	DEVAD	R/W	0x0	Retain	MMD register device address ■ 00011 = MMD3 ■ 00111 = MMD7

17.2.20 MMD access address data register

Offset: 0xE

Table 17-22 MMD access address data register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	ADDRESS_ DATA	R/O	0x0	Retain	If MMD access control register 0xD bits[15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register.

17.2.21 Extended status register

Offset: 0xF

Table 17-23 Extended status register

Bit	Field	Access type	HW reset	SW reset	Description
15	1000BASE-X_ FULL-DUPLEX	R/O	0x1 for port 4 0x0 for port 0-3	Retain	■ 1 = PHY supports 1000BASE-X full-duplex. ■ 0 = PHY does not supports 1000BASE-X full-duplex. Always be 0.

Table 17-23 Extended status register

Bit	Field	Access type	HW reset	SW reset	Description
14	1000BASE-X_ HALF-DUPLEX	R/O	0x0	Retain	■ 1 = PHY supports 1000BASE-X half-duplex. ■ 0 = PHY does not support 1000BASE-X half-duplex. Always be 0.
13	1000BASE-X_ FULL-DUPLEX	R/O	0x1	Retain	■ 1 = PHY supports 1000BASE-T full-duplex. ■ 0 = PHY does not supports 1000BASE-T full-duplex. Always be 1.
12	1000BASE-X_ HALF-DUPLEX	R/O	0x0	Retain	■ 1 = PHY supports 1000BASE-T half-duplex. ■ 0 = PHY does not support 1000BASE-T half-duplex. Always be 0.
11:0	Reserved	R/O	0x0	Retain	Always be 0.

17.2.22 Function control register

Offset: 0x10

Table 17-24 Function control register

Bit	Field	Access type	HW reset	SW reset	Description
15:7	Reserved	R/O	0xD0	Retain	–
6:5	MDI_ CROSSOVER_ MODE	R/W	0x3	Update	Changes made to these bits disrupt the normal operation, thus a software reset is mandatory after the change. ■ 00 = Manual MDI configuration ■ 01 = Manual MDIX configuration ■ 10 = Reserved ■ 11 = Enable automatic crossover for all modes
4:3	Reserved	R/O	0x0	Retain	–
2	SQE_TEST	R/W	0x0	Retain	■ 1 = SQE test is enabled. ■ 0 = SQE test is disabled. Note: SQE test is automatically disabled in full-duplex mode regardless the setting in this bit.

Table 17-24 Function control register

Bit	Field	Access type	HW reset	SW reset	Description
1	POLARITY_ REVERSAL	R/W	0x1	Retain	If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te. ■ 1 = Polarity reversal is enabled. ■ 0 = Polarity reversal is disabled. Note: Write 1 to this bit, it will be 0; write 0 to this bit, it will be 1.
0	DISABLE_ JABBER	R/W	0x0	Retain	Jabber takes effect in 10BASE-Te half-duplex mode only. ■ 1 = Disable jabber function ■ 0 = Enable jabber function

17.2.23 PHY specific status register — copper page

Offset: 0x11

Table 17-25 PHY specific status register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
15:14	SPEED	R/O	0x0	Retain	These status bits are valid only when this register bit[11] is 1. Bit[11] is set when auto-negotiation is completed or auto-negotiation is disabled. ■ 11 = Reserved ■ 10 = 1000 Mbps ■ 01 = 100 Mbps ■ 00 = 10 Mbps
13	DUPLEX	R/O	0x0	Retain	This status bit is valid only when this register bit[11] is 1. Bit[11] is set when auto-negotiation is completed or auto-negotiation is disabled. ■ 1 = Full-duplex ■ 0 = Half-duplex
12	PAGE_ RECEIVED(REAL-TIME)	R/O	0x0	Retain	■ 1 = Page is received. ■ 0 = Page is not received.
11	SPEED_AND_ DUPLEX_ RESOLVED	R/O	0x0	Retain	When auto-negotiation is disabled, this bit is set to 1 for force speed mode. ■ 1 = Resolved ■ 0 = Not resolved
10	LINK(REAL-TIME)	R/O	0x0	Retain	■ 1 = Link up ■ 0 = Link down
9:7	CABLE_ LENGTH	R/O	0x0	Retain	Always be 0.

Table 17-25 PHY specific status register — copper page

Bit	Field	Access type	HW reset	SW reset	Description
6	MDI_ CROSSOVER_ STATUS	R/O	0x0	Retain	This status bit is valid only when this register bit[11] is 1. Bit[11] is set when auto-negotiation is completed or auto-negotiation is disabled. The bit value depends on the Function control register 0x10 bits[6:5] configurations. Function control register 0x10 configurations take effect after software reset. ■ 1 = MDIX ■ 0 = MDI
5	WIRESPEED_ DOWNGRADE	R/O	0x0	Retain	■ 1 = Downgrade ■ 0 = No Downgrade
4	Reserved	R/O	0x1	Retain	–
3	TRANSMIT_ PAUSE_ ENABLE	R/O	0x0	Retain	This status bit is valid only when this register bit[11] is 1. Bit[11] is set when auto-negotiation is completed.This bit indicates MAC pause resolution. This bit is for information purpose only and is not used by the device. In force mode, this bit is set to be 0. ■ 1 = Transmit pause is enabled. ■ 0 = Transmit pause is disabled.
2	RECEIVE_ PAUSE_ ENABLE	R/O	0x0	Retain	This status bit is valid only when this register bit[11] is 1. Bit[11] is set when auto-negotiation is completed. This bit indicates MAC pause resolution. This bit is for information purpose only and is not used by the device. In force mode, this bit is set to be 0. ■ 1 = Receive pause is enabled. ■ 0 = Receive pause is disabled.
1	POLARITY_ REAL_TIME	R/O	0x0	Retain	■ 1 = Reverted ■ 0 = Normal
0	JABBER_ REAL_TIME	R/O	0x0	Retain	■ 1 = Jabber ■ 0 = No jabber

17.2.24 PHY specific status register — fiber/SGMII page

Offset: 0x11

Table 17-26 PHY specific status register — fiber/SGMII page

Bit	Field	Access type	HW reset	SW reset	Description
15:14	SPEED	R/O	0x1	Retain	■ 11 = Reserved ■ 10 = 1000 Mbps ■ 01 = 100 Mbps ■ 00 = 10 Mbps
13	DUPLEX	R/O	0x1	Retain	■ 1 = Full-duplex ■ 0 = Half-duplex
12	PAGE_ RECEIVED_ REAL_TIME	R/O	0x0	Retain	■ 1 = Page is received. ■ 0 = Page is not received.
11	SPEED_AND_ DUPLEX_ RESOLVED	R/O	0x0	Retain	When auto-negotiation is disabled, this bit is set to 1 for force speed mode. ■ 1 = Resolved ■ 0 = Not resolved
10	LINKREAL_ TIME	R/O	0x0	Retain	For 1000BASE-X, 100BASE-FX: ■ 1 = Link up ■ 0 = Link down
9	MR_AN_ COMPLETE	R/O	0x0	Retain	For 1000BASE-X, SGMII: ■ 1 = Auto-negotiation is completed. ■ 0 = Auto-negotiation is not completed.
8	SYNC_ STATUS	R/O	0x0	Retain	For 1000BASE-X only. ■ 1= 1000BX is synced. ■ 0= 1000BX is not synced.
7:4	Reserved	R/O	0x0	Retain	–
3	TRANSMIT_ PAUSE_ ENABLE	R/O	0x0	Retain	This is a reflection of the MAC pause resolution. This bit is for information purpose and is not used by the device. This status bit is valid only after PHY specific status register — fiber/SGMII page 0x11 bit[11] = 1. The resolved bit is set when auto-negotiation is completed; while in force mode, this bit is set to be 0. ■ 1 = Transmit pause enabled ■ 0 = Transmit pause disabled

Table 17-26 PHY specific status register — fiber/SGMII page

Bit	Field	Access type	HW reset	SW reset	Description
2	RECEIVE_ PAUSE_ ENABLE	R/O	0x0	Retain	This is a reflection of the MAC pause resolution. This bit is for information purpose and is not used by the device. This status bit is valid only after PHY specific status register — fiber/SGMII page 0x11 bit[11] = 1. The resolved bit is set when auto-negotiation is completed; while in force mode, this bit is set to be 0. ■ 1 = Receive pause enabled ■ 0 = Receive pause disabled
1:0	Reserved	R/O	0x0	Retain	–

17.2.25 Interrupt enable register — for port 0-3

Offset: 0x12

Table 17-27 Interrupt enable register — for port 0-3

Bit	Field	Access type	HW reset	SW reset	Description
15	AUTO-NEGOTIATION _ERROR	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
14	SPEED_ CHANGED	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
13	DUPLEX_ CHANGED_ INT	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
12	PAGE_ RECIEVED_ INT	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
11	LINK_FAIL_ INT	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
10	LINK_ SUCCESS_INT	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
9:6	Reserved	R/W	0x0	Retain	–
5	DOWNGRADE _INT	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
4:1	Reserved	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
0	WOL_INT	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable

17.2.26 Interrupt enable register — for port 4

Offset: 0x12

Table 17-28 Interrupt enable register — for port 4

Bit	Field	Access type	HW reset	SW reset	Description
15	Reserved	R/W	0x0	Retain	–
14	SPEED_ CHANGED	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
13	Reserved	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
12	MEDIA_ STATUS_ CHANGE_INT	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
11	LINK_FAIL_ INT	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
10	LINK_ SUCCESS_INT	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
9	Reserved	R/W	0x0	Retain	–
8	LNK_FAIL_BX	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
7	LNK_ SUCCESS_BX	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable
6:1	Reserved	R/W	0x0	Retain	–
0	WOL_INT	R/W	0x0	Retain	■ 1 = Interrupt enable ■ 0 = Interrupt disable

17.2.27 Interrupt status register — for port 0-3

Offset: 0x13

Table 17-29 Interrupt status register — for port 0-3

Bit	Field	Access type	HW reset	SW reset	Description
15	AUTO-NEGOTIATION _ERROR	R/O	0x0	Retain	An error can occur if either Master/Slave does not resolve, or no common HCD, or link does not come up after negotiation is completed. ■ 1 = Auto-negotiation error ■ 0 = No auto-negotiation error
14	SPEED_ CHANGED	R/O	0x0	Retain	■ 1 = Speed is changed. ■ 0 = Speed is not changed.
13	DUPLEX_ CHANGED_ INT	R/O	0x0	Retain	■ 1 = Duplex is changed. ■ 0 = Duplex is not changed.

Table 17-29 Interrupt status register — for port 0-3

Bit	Field	Access type	HW reset	SW reset	Description
12	PAGE_ RECIEVED_ INT	R/O	0x0	Retain	■ 1 = Page is received. ■ 0 = Page is not received.
11	LINK_FAIL_ INT	R/O	0x0	Retain	■ 1 = Link down takes place. ■ 0 = No link down takes place.
10	LINK_ SUCCESS_INT	R/O	0x0	Retain	■ 1 = Link up takes place. ■ 0 = No link up takes place.
9:6	Reserved	R/O	0x0	Retain	–
5	DOWNGRADE _INT	R/O	0x0	Retain	■ 1 = Smart speed downgrade happened. ■ 0 = Smart speed downgrade did not happen.
4:1	Reserved	R/O	0x0	Retain	–
0	WOL_INT	R/O	0x0	Retain	■ 1 = Wake on LAN packet is received. ■ 0 = No wake on LAN packet is received.

17.2.28 Interrupt status register — for port 4

Offset: 0x13

Table 17-30 Interrupt status register — for port 4

Bit	Field	Access type	HW reset	SW reset	Description
15	Reserved	R/O	0x0	Retain	–
14	SPEED_ CHANGED	R/O	0x0	Retain	■ 1 = Speed is changed ■ 0 = Speed does not changed.
13	Reserved	R/O	0x0	Retain	Always be 0.
12	MEDIA_ STATUS_ CHANGE_INT	R/O	0x0	Retain	In Combo mode: ■ 1 = Fiber copper link status is changed or media type is changed. ■ 0 = Not changed.
11	LINK_FAIL_ INT	R/O	0x0	Retain	■ 1 = Link down takes place. ■ 0 = No link down takes place.
10	LINK_ SUCCESS_INT	R/O	0x0	Retain	■ 1 = Link up takes place. ■ 0 = No link up takes place.
9	Reserved	R/O	0x0	Retain	–
8	LNK_FAIL_BX	R/O	0x0	Retain	■ 1 = 1000BASE-X/100BASE-FX link down happened. ■ 0 = 1000BASE-X/100BASE-FX link down did not happen.

Table 17-30 Interrupt status register — for port 4

Bit	Field	Access type	HW reset	SW reset	Description
7	LNK_ SUCCESS_BX	R/O	0x0	Retain	■ 1 = 1000BASE-X/100BASE-FX link up happened. ■ 0 = 1000BASE-X/100BASE-FX link up did not happen.
6:1	Reserved	R/O	0x0	Retain	–
0	WOL_INT	R/O	0x0	Retain	■ 1 = Wake-on-Lan takes place. ■ 0 = Wake-on-Lan does not take place.

17.2.29 Smart speed register

Offset: 0x14

Table 17-31 Smart speed register

Bit	Field	Access type	HW reset	SW reset	Description
15:6	Reserved	R/O	0x20	Retain	–
5	SMARTSPEED _EN	R/W	0x1	Update	This field is not updated immediately after writing, and the configuration does not take effect until software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ 1 = Enable smarts-peed (default) ■ 0 = Disable smarts-peed When this bit is set to 1 while training phase cannot finish, the device automatically adjusts the speed to the next lower rate (from 1000 to 100 to 10) after a few failed attempts.
4:2	SMARTSPEED _RETRY_ LIMIT	R/W	0x3	Update	This field is not updated immediately after writing, and the configuration does not take effect until software reset is asserted by writing PHY specific status register — copper page 0x0 bit[15]. Smarts-peed training retries many times before speed downgrading. ■ 000 = 2 times ■ 001 = 3 times ■ 010 = 4 times ■ 011 = 5 times (default) ■ 100 = 6 times ■ 101 = 7 times ■ 110 = 8 times ■ 111 = 9 times
1	Reserved	R/W	0x0	Update	–
0	Reserved	R/O	0x0	Retain	–

17.2.30 Fiber/SGMII control register

Offset: 0x14

Table 17-32 Fiber/SGMII control register

Bit	Field	Access type	HW reset	SW reset	Description
15	PAUSE_ SGBX_SEL	R/O	0x1	Retain	For SGMII mode: ■ 1 = Send link partner's pause ability ■ 0 = Send pause resolution result
14:9	Reserved	R/O	0x0	Retain	Always be 0.
8	ATHR_CSCO_ MODE_25M	R/O	0x1	Retain	SGMII base page selection
7	MR_AN_ ENABLE_ SGBX_SEL	R/O	0x1	Retain	■ 1 = If force or loopback mode, the internal AN_ENABLE is 0. ■ 0 = Internal AN_ENABLE is this bit.
6:5	PAUSE_ SGBX_MAC	R/O	0x3	Retain	In SGMII MAC mode, the pause ability transmitted by SGMII interface.
4	SGBX_INT_ SEL	R/O	0x1	Retain	For debug
3	MEDIA_LNK_ RL_LPBK	R/O	0x1	Retain	For 1000BX, SGMII; ■ 1 = A new page is received. ■ 0 = No new page does not received.
2	MEDIA_LNK_ RL_SEL	R/O	0x1	Retain	If fiber/SGMII is in SGMII MAC and loopback mode: ■ 0 = Media link is down. ■ 1 = Media link is up.
1	MEDIA_LNK_ RL	R/O	0x0	Retain	If fiber/SGMII is in SGMII MAC mode and autoneg enable bit in Control register — fiber/SGMII page 0x0 is 0, STA should monitor media's link status, and set this register to tell SGMII MAC. ■ 0 = Media link is down. ■ 1 = Media link is up.
0	FORCE_ SPEED	R/O	0x0	Retain	In SGMII mode and autoneg enable bit in reg0 is 0 then: ■ 0 = Speed of SGMII comes from media ■ 1 = Speed of SGMII comes from Control register — fiber/SGMII page 0x0 bit[13], bit[6]

1. This register is available in port 4 only.

17.2.31 Cable diagnostic test control register

Offset: 0x16

Table 17-33 Cable diagnostic test control register

Bit	Field	Access type	HW reset	SW reset	Description
15	ENABLE_CDT	R/W	0x0	Retain	Enable or disable CDT. When CDT is complete, hardware automatically set this bit to 0. ■ 1 = Enable CDT ■ 0 = Disable CDT
14	Reserved	R/O	0x0	Retain	–
13	ENABLE_ INTER-PAIR_ SHORT_CHK	R/W	0x1	Retain	■ 1 = Disable inter-pair short check. ■ 0 = Enable inter-pair short check.
12	Reserved	R/O	0x0	Retain	–
11	CABLE_ DIAGNOSTICS _STATUS	R/W	0x0	Retain	■ 1 = CDT test is in progress. ■ 0 = CDT test is complete.
10:0	Reserved	R/O	0x400	Retain	–

17.2.32 Media select status register

Offset: 0x1A

Table 17-34 Media select status register

Bit	Field	Access type	HW reset	SW reset	Description
15:6	Reserved	R/O	0x0	Retain	–
5	AUTO_MDET_ TO_BT	R/O	0x0	Retain	1 = Copper is detected and the link is up.
4	AUTO_MDET_ TO_ 1000BASE-X	R/O	0x0	Retain	1 = 1000BASE-X is selected.
3	AUTO_MDET_ TO_100BASE-FX	R/O	0x0	Retain	1 = 100BASE-FX is selected.
2:0	Reserved	R/O	0x0	Retain	–

1. This register is available in port 4 only.

17.2.33 SGMII PBRS control register

Offset: 0x1B

Table 17-35 SGMII PBRS control register

Bit	Field	Access type	HW reset	SW reset	Description
15	SGMII_PRBS_EN	R/W	0x0	Retain	■ 1 = PRBS is enabled to generate random data bit and send it through SerDes Tx. ■ 0 = PRBS is disabled.
14	SGMII_PRBS_BERT_EN	R/W	0x0	Retain	This bit takes effect after the PRBS_EN is set to 1. ■ 1 = Enable checking bit error rate for the received random data bit generated by PRBS. ■ 0 = Disable checking bit error rate for the received random data bit generated by PRBS.
13:0	Reserved	R/O	0x400	Retain	–

1. This register is available in port 4 only.

17.2.34 Debug port — address offset set register

Offset: 0x1D

Table 17-36 Debug port — address offset set bit register

Bit	Field	Access type	HW reset	SW reset	Description
15:6	Reserved	R/O	0x0	Retain	–
5:0	ADDRESS_OFFSET	R/W	0x0	Retain	The address index of the register is either write or read.

17.2.35 Debug port — data port register

Offset: 0x1E

Table 17-37 Debug port — data port bit register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	DEBUG_DATA_PORT	R/W	0x0	Retain	The data port of debug register The address offset must be set in Debug port — address offset set bit register 0x1D before accessing this register.

17.2.36 Chip configuration register

Offset: 0x1F

Table 17-38 Chip configuration bit register

Bit	Field	Access type	HW reset	SW reset	Description
15	BT_BX_REG_SEL	R/W	POS	Retain	POS pin Copper page fiber page select bit: ■ 1 = Select copper page registers ■ 0 = Select fiber page registers
14	Reserved	R/O	0x0	Retain	–
13	SGMII_IMP_50_75_AUTO	R/W	0x0	Retain	Rx/Tx impedance of SerDes in Combo mode ■ 1 = 75 Ω ■ 0 = 50 Ω
12:11	Reserved	R/O	0x0	Retain	–
10	PRIORITY_SEL	R/W	0x1	Retain	In Combo mode: ■ 0 = Prefer copper ■ 1 = Prefer fiber
9	Reserved	R/O	0x0	Retain	–
8	FIBER_MODE_AUTO	R/W	0x1	Retain	In Combo mode: ■ 1 = 1000BASE-FX fiber ■ 0 = 100BASE-FX fiber
7:4	Reserved	R/O	0x0	Retain	–
3:0	MODE_CFG	R/W	POS	Retain	POS pin Chip mode configure bits: ■ 0000 = PSGMII (5 copper ports) ■ 0011 = PSGMII (4 copper ports + 1 Combo port) ■ 0100 = QSGMII + SGMII (5 copper ports)

1. This register is available in port 4 only.

17.3 Debug registers

Table 17-39 Debug registers summary

Address	Description
0xB	“Copper hibernation control register” on page 78
0x10	“100BASE-TX test mode select register” on page 78
0x11	“External loopback control register” on page 79

Table 17-39 Debug registers summary (cont.)

Address	Description
0x12	“10BASE-Te test mode register” on page 79
0x1F	“PHY control debug 0 register” on page 79

17.3.1 Copper hibernation control register

Offset: 0xB

Table 17-40 Copper hibernation control register

Bit	Field	Access type	HW reset	SW reset	Description
15	Enable hibernation	R/W	0x1	Retain	Power hibernate control bit for copper interface only ■ 1 = Enable hibernate ■ 0 = Disable hibernate
14:0	Reserved	R/O	0x3C80	Retain	–

17.3.2 100BASE-TX test mode select register

Offset: 0x10

Table 17-41 100BASE-TX test mode select register

Bit	Field	Access type	HW reset	SW reset	Description
15:8	Reserved	R/O	0x40	Retain	–
7:5	TEST_MODE	R/W	0x0	Retain	100BASE-TX Active Output Interface (AOI) test mode select: ■ 001 = Duty cycle distortion test. The output waveform consists of the MLT-3 transitions generated by a 01010101 NRZ bit sequence. ■ 010 = Overshoot test. The output waveform consists of 14 bit times of no transition preceded by a transition from zero to either plus or minus VOUT. ■ 011 = Overshoot test. The output waveform consists of 12 bit times of no transition preceded by a transition from zero to either plus or minus VOUT. This is for some special testers. ■ 100 = Jitter test. The output waveform consists of the MLT-3 transitions generated by scrambled HALT line state. ■ Others = Reserved
4:0	Reserved	R/O	0x0	Retain	–

17.3.3 External loopback control register

Offset: 0x11

Table 17-42 External loopback control register

Bit	Field	Access type	HW reset	SW reset	Description
15:1	Reserved	R/O	0x35	Retain	–
0	External loopback	R/W	0x0	Retain	■ 1 = Enable external loopback of the PHY ■ 0 = Disable external loopback of the PHY

17.3.4 10BASE-Te test mode register

Offset: 0x12

Table 17-43 10BASE-Te test mode register

Bit	Field	Access type	HW reset	SW reset	Description
15:6	Reserved	R/O	0x130	Retain	–
5	TEST_ MODE[2]	R/W	0x0	Retain	Bit2 of TEST_MODE Used with TEST_MODE[1:0] together.
4:2	Reserved	R/O	0x1	Retain	–
1:0	TEST_ MODE[1:0]	R/W	0x0	Retain	10BASE-Te test mode select ■ 001 = Packet with all-1, 10 MHz sine wave, for harmonic test ■ 010 = Pseudo random, for TP_ IDLE/Jitter/ Differential Voltage test ■ 011 = Normal link pulse only ■ 100 = 5 MHz sin wave ■ Others = Normal mode

17.3.5 PHY control debug 0 register

Offset: 0x1F

Table 17-44 PHY control debug 0 register

Bit	Field	Access type	HW reset	SW reset	Description
15:4	Reserved	R/O	0x30	Retain	–
3	SEL_LP5_ LP8_POS_ REG	R/W	0x1	Retain	1.5/1.8 V regulator output control: ■ 1 = 1.8 V ■ 0 = 1.5 V Reset by on chip hardware reset only.
2:0	Reserved	R/O	0x0	Retain	–

17.4 MMD1 registers

Table 17-45 MMD1 registers summary

Address	Description
0x5	"MMD1 — PMA package register" on page 80
0x8	"MMD1 — Device present register" on page 80
0x52	"MMD1 — PSGMII PRBS error count 1 register" on page 81
0x53	"MMD1 — PSGMII PRBS error count 2 register" on page 81
0x54	"MMD1 — PSGMII/QSGMII PRBS control register" on page 81

17.4.1 MMD1 — PMA package register

Offset: 0x5

Table 17-46 MMD1 — PMA package register

Bit	Field	Access type	HW reset	SW reset	Description
15:8	Reserved	R/O	0x0	Retain	–
7	AUTO_NEG_ PRESENT	R/O	0x1	Retain	■ 1 = Auto-negotiation presents in package. ■ 0 = Auto-negotiation does not present in package.
6:4	Reserved	R/O	0x0	Retain	–
3	PCS_ PRESENT	R/O	0x1	Retain	■ 1 = PCS presents in package. ■ 0 = PCS does not present in package.
2	Reserved	R/O	0x0	Retain	–
1	PMA_ PRESENT	R/O	0x1	Retain	■ 1 = PMA presents in package. ■ 0 = PMA does not present in package.
0	MII_REG_ PRESENT	R/O	0x1	Retain	■ 1 = Clause 22 registers present in package. ■ 0 = Clause 22 registers do not present in package.

17.4.2 MMD1 — Device present register

Offset: 0x8

Table 17-47 MMD1 — Device present register

Bit	Field	Access type	HW reset	SW reset	Description
15:14	DEVICE_ PRESENT	R/O	0x2	Retain	Always be 10. 10 = MMD1 for PMA presents.
13:0	Reserved	R/O	0x0	Retain	Always be 0.

17.4.3 MMD1 — PSGMII PRBS error count 1 register

Offset: 0x52

Table 17-48 MMD1 — PSGMII PRBS error count 1 register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	PSGMII_MMD_REG_QSGMII_PRBS_ERR_CNT_15_0	R/O	0x0	Retain	PSGMII PRBS error counter bits[15:0]

1. This register is available in PSGMII IP only.

17.4.4 MMD1 — PSGMII PRBS error count 2 register

Offset: 0x53

Table 17-49 MMD1 — PSGMII PRBS error count 2 register

Bit	Field	Access type	HW reset	SW reset	Description
15	PSGMII_MMD_REG_QSGMII_PRBS_BITSYNC	R/O	0x0	Retain	PSGMII PRBS bit sync indicator
14:0	PSGMII_MMD_REG_QSGMII_PRBS_ERR_CNT_30_16	R/O	0x0	Retain	PSGMII PRBS error counter bits[30:16]

1. This register is available in PSGMII IP only.

17.4.5 MMD1 — PSGMII/QSGMII PRBS control register

Offset: 0x54

Table 17-50 MMD1 — PSGMII/QSGMII PRBS control register

Bit	Field	Access type	HW reset	SW reset	Description
15:3	Reserved	R/O	0x102	Retain	–
2	PQSGMII_PRBS_BERT_EN	R/W	0x0	Retain	This bit takes effect after the PRBS_EN is set to 1. ■ 1 = Enable checking bit error rate for the received random data bit generated by PRBS. ■ 0 = Disable checking bit error rate for the received random data bit generated by PRBS.

Table 17-50 MMD1 — PSGMII/QSGMII PRBS control register

Bit	Field	Access type	HW reset	SW reset	Description
1	PQSGMII_ PRBS_EN	R/W	0x0	Retain	■ 1 = PRBS is enabled to generate random data bit and send it through SerDes Tx. ■ 0 = PRBS is disabled.
0	Reserved	R/O	0x0	Retain	PSGMII PRBS error indicator

1. This register is available in PSGMII IP only.

17.5 MMD3 registers

Table 17-51 MMD3 registers summary

Address	Description
0x0	"MMD3 — PCS control register" on page 83
0x1	"MMD3 — PCS status register" on page 83
0x5	"MMD3 — PCS package register" on page 84
0x8	"MMD3 — device present register" on page 84
0x14	"MMD3 — EEE capability register" on page 84
0x16	"MMD3 — EEE wake error counter register" on page 85
0x8012	"MMD3 — Wake-on-LAN control register" on page 85
0X804A	"MMD3 — Internal MAC address 1 register" on page 85
0X804B	"MMD3 — Internal MAC address 2 register" on page 85
0X804C	"MMD3 — Internal MAC address 3 register" on page 86
0X805A	"MMD3 — Remote PHY loopback register" on page 86
0X805A	"MMD3 — PSGMII SerDes control register" on page 86
0x8064	"MMD3 — Cable diagnostics register" on page 87
0x8065	"MMD3 — Cable diagnostics pair 0 length register" on page 90
0x8066	"MMD3 — Cable diagnostics pair 1 length register" on page 90
0x8067	"MMD3 — Cable diagnostics pair 2 length register" on page 91
0x8068	"MMD3 — Cable diagnostics pair 3 length register" on page 91

17.5.1 MMD3 — PCS control register

Offset: 0x0

Table 17-52 MMD3 — PCS control register

Bit	Field	Access type	HW reset	SW reset	Description
15	PCS_RST	R/W	0x0	1	This bit is used to restore the MMD3/MMD7 registers to default states and trigger a software reset. ■ 1 = PCS reset ■ 0 = Normal operation
14	PCS_LPBK	R/O	0x0	Retain	Always be 0.
13:11	Reserved	R/O	0x0	Retain	–
10	Reserved	R/O	0x0	Retain	–
9:0	Reserved	R/O	0x0	Retain	–

17.5.2 MMD3 — PCS status register

Offset: 0x1

Table 17-53 MMD3 — PCS status register

Bit	Field	Access type	HW reset	SW reset	Description
15:12	Reserved	R/O	0x0	Retain	–
11	TX_LPI_IDLE_RECEIVED	R/O	0x0	Retain	■ 1 = Low power idle signal is received on PCS Tx side since the last read operation to this register. ■ 0 = No low power idle signal is received on PCS Tx side since the last read operation to this register.
10	RX_LPI_IDLE_RECEIVED	R/O	0x0	Retain	■ 1 = Low power idle signal is received on PCS Rx side since the last read operation to this register. ■ 0 = No low power idle signal is received on PCS Rx side since the last read operation to this register.
9	TX_LPI_IDLE_INDICATION	R/O	0x0	Retain	■ 1 = Low power idle signal is currently entering PCS Tx side. ■ 0 = Low power idle signal is not currently entering PCS Tx side.
8	RX_LPI_IDLE_INDICATION	R/O	0x0	Retain	■ 1 = Low power idle signal is currently entering PCS Rx side. ■ 0 = Low power idle signal is not currently entering PCS Rx side.
7:0	Reserved	R/O	0x0	Retain	–

17.5.3 MMD3 — PCS package register

Offset: 0x5

Table 17-54 MMD3 — PCS package register

Bit	Field	Access type	HW reset	SW reset	Description
15:8	Reserved	R/O	0x0	Retain	–
7	AUTO_NEG_ PRESENT	R/O	0x1	Retain	Always be 1.
6:4	Reserved	R/O	0x0	Retain	–
3	PCS_ PRESENT	R/O	0x1	Retain	Always be 1.
2	Reserved	R/O	0x0	Retain	–
1	PMA_ PRESENT	R/O	0x1	Retain	Always be 1.
0	MII_REG_ PRESENT	R/O	0x1	Retain	Always be 1.

17.5.4 MMD3 — device present register

Offset: 0x8

Table 17-55 MMD3 — device present register

Bit	Field	Access type	HW reset	SW reset	Description
15:14	DEVICE_ PRESENT	R/O	0x2	Retain	Always be 10. MMD3 for PCS presents.
13:0	Reserved	R/O	0x0	Retain	–

17.5.5 MMD3 — EEE capability register

Offset: 0x14

Table 17-56 MMD3 — EEE capability register

Bit	Field	Access type	HW reset	SW reset	Description
15:3	Reserved	R/O	0x0	Retain	–
2	BT1000_EEE	R/O	0x1	Retain	EEE is supported for 1000Base-T. Always be 1.
1	BT100_EEE	R/O	0x1	Retain	EEE is supported for 100Base-TX. Always be 1.
0	Reserved	R/O	0x0	Retain	–

17.5.6 MMD3 — EEE wake error counter register

Offset: 0x16

Table 17-57 MMD3 — EEE wake error counter register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	EEE_WAKE_ ERROR_ COUNTER	R/O	0x0	Retain	The counter is incremented by 1 when the PHY fails to complete normal wake-up sequence within the time frame required for the PHY type. This counter is cleared after read. When overflow takes place, the counter is filled with all-1.

17.5.7 MMD3 — Wake-on-LAN control register

Offset: 0x8012

Table 17-58 MMD3 — Wake-on-LAN control register

Bit	Field	Access type	HW reset	SW reset	Description
15:6	Reserved	R/O	0x0	Retain	–
5	WOL_EN	R/W	0x1	Retain	Wake-on-LAN control ■ 0 = Disable WoL ■ 1 = Enable WoL
4:0	Reserved	R/O	0x0	Retain	–

17.5.8 MMD3 — Internal MAC address 1 register

Offset: 0x804A

Table 17-59 MMD3 — Internal MAC address 1 register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	LOC_MAC_ ADDR[47:32]	R/W	0x0	Retain	Bits[47:32] of internal address Used for WoL.

17.5.9 MMD3 — Internal MAC address 2 register

Offset: 0x804B

Table 17-60 MMD3 — Internal MAC address 2 register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	LOC_MAC_ ADDR[31:16]	R/W	0x0	Retain	Bits[31:16] of internal address Used for WoL.

17.5.10 MMD3 — Internal MAC address 3 register

Offset: 0x804C

Table 17-61 MMD3 — Internal MAC address 3 register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	LOC_MAC_ ADDR[15:0]	R/W	0x0	Retain	Bits[15:0] of internal address Used for WoL.

17.5.11 MMD3 — Remote PHY loopback register

Offset: 0x805A

Table 17-62 MMD3 — Remote PHY loopback register

Bit	Field	Access type	HW reset	SW reset	Description
15:1	Reserved	R/O	0x1801	Retain	–
0	REM_PHY_ LPBK	R/W	0x0	Retain	Loopback received data packets to link partner ■ 1 = Enable remote PHY loopback ■ 0 = Disable remote PHY loopback

17.5.12 MMD3 — PSGMII SerDes control register

Offset: 0x805A

Table 17-63 MMD3 — PSGMII SerDes control register

Bit	Field	Access type	HW reset	SW reset	Description
15	PSGMII_ SERDES_ SHDN	R/W	0x0	Retain	■ 1 = Enable shut down PSGMII SerDes ■ 0 = Disable shut down PSGMII SerDes
14:0	Reserved	R/W	0x0	Retain	–

1. This register is available in port 4 only.

17.5.13 MMD3 — Cable diagnostics register

Offset:0x8064

Table 17-64 MMD3 — Cable diagnostics register

Bit	Field	Access type	HW reset	SW reset	Description
15:12	MDI_PAIR0_ STATUS	R/O	0x0	Retain	MDI pair 0 diagnostic status ■ 0x0 = Invalid, cable diagnostics routine did not complete successfully ■ 0x1 = Pair OK, no fault detected ■ 0x2 = Pair open ■ 0x3 = Intra pair short ■ 0x4 = Inter pair short with pair 1 and intra pair OK ■ 0x8 = Inter pair short with pair 2 and intra pair OK ■ 0xC = Inter pair short with pair 3 and intra pair OK ■ 0x6 = Inter pair short with pair 1 and intra pair open ■ 0xA = Inter pair short with pair 2 and intra pair open ■ 0xE = Inter pair short with pair 3 and intra pair open ■ 0x7 = Inter pair short with pair 1 and intra pair short ■ 0xB = Inter pair short with pair 2 and intra pair short ■ 0xF = Inter pair short with pair 3 and intra pair short ■ 0x9 = Pair busy ■ Other = Reserved
11:8	MDI_PAIR1_ STATUS	R/O	0x0	Retain	MDI pair 1 diagnostic status ■ 0x0 = Invalid, cable diagnostics routine did not complete successfully ■ 0x1 = Pair OK, no fault detected ■ 0x2 = Pair open ■ 0x3 = Intra pair short ■ 0x4 = Inter pair short with pair 1 and intra pair OK ■ 0x8 = Inter pair short with pair 2 and intra pair OK ■ 0xC = Inter pair short with pair 3 and intra pair OK ■ 0x6 = Inter pair short with pair 1 and intra pair open ■ 0xA = Inter pair short with pair 2 and intra pair open ■ 0xE = Inter pair short with pair 3 and intra pair open ■ 0x7 = Inter pair short with pair 1 and intra pair short ■ 0xB = Inter pair short with pair 2 and intra pair short ■ 0xF = Inter pair short with pair 3 and intra pair short ■ 0x9 = Pair busy ■ Other = Reserved

Table 17-64 MMD3 — Cable diagnostics register

Bit	Field	Access type	HW reset	SW reset	Description
7:4	MDI_PAIR2_STATUS	R/O	0x0	Retain	MDI pair 2 diagnostic status ■ 0x0 = Invalid, cable diagnostics routine did not complete successfully ■ 0x1 = Pair OK, no fault detected ■ 0x2 = Pair open ■ 0x3 = Intra pair short ■ 0x4 = Inter pair short with pair 1 and intra pair OK ■ 0x8 = Inter pair short with pair 2 and intra pair OK ■ 0xC = Inter pair short with pair 3 and intra pair OK ■ 0x6 = Inter pair short with pair 1 and intra pair open ■ 0xA = Inter pair short with pair 2 and intra pair open ■ 0xE = Inter pair short with pair 3 and intra pair open ■ 0x7 = Inter pair short with pair 1 and intra pair short ■ 0xB = Inter pair short with pair 2 and intra pair short ■ 0xF = Inter pair short with pair 3 and intra pair short ■ 0x9 = Pair busy ■ Other = Reserved

Table 17-64 MMD3 — Cable diagnostics register

Bit	Field	Access type	HW reset	SW reset	Description
3:0	MDI_PAIR3_STATUS	R/O	0x0	Retain	MDI pair 3 diagnostic status ■ 0x0 = Invalid, cable diagnostics routine did not complete successfully ■ 0x1 = Pair OK, no fault detected ■ 0x2 = Pair open ■ 0x3 = Intra pair short ■ 0x4 = Inter pair short with pair 1 and intra pair OK ■ 0x8 = Inter pair short with pair 2 and intra pair OK ■ 0xC = Inter pair short with pair 3 and intra pair OK ■ 0x6 = Inter pair short with pair 1 and intra pair open ■ 0xA = Inter pair short with pair 2 and intra pair open ■ 0xE = Inter pair short with pair 3 and intra pair open ■ 0x7 = Inter pair short with pair 1 and intra pair short ■ 0xB = Inter pair short with pair 2 and intra pair short ■ 0xF = Inter pair short with pair 3 and intra pair short ■ 0x9 = Pair busy ■ Other = Reserved

Note:

For inter pair diagnose, CDT test supports: (X, Y, Z are any three pairs of the cable)

1. pair X's X+ or X- short with pair Y+ or Y-;
2. pair X's X+ short with Y+ (Y-), and X- short with Y-(Y+).

Does not support:

1. pair X inter short with more than one pair, In this case, the register below only record that X inter short with the pair who reflects the largest energy on pair X.
2. pair X's X+ short with Y+ or Y- and X- short with Z+ or Z-
3. pair X inter short with Y at more than one points. In this case, only the nearest short point is recorded.

17.5.14 MMD3 — Cable diagnostics pair 0 length register

Offset: 0x8065

Table 17-65 MMD3 — Cable diagnostics pair 0 length register

Bit	Field	Access type	HW reset	SW reset	Description
15:8	PAIR_0_ INTER_ SHORT_ POINT	R/O	0x0	Retain	Inter short distance for pair 0 The distance is in sample cycle, and can be transfered in meter by being multiplied by about 0.8. If CDT is done and MMD3 — Cable diagnostics register 0x8064 bits[15:12] is 0x1, 0x4, 0x8 or 0xC, then the value is invalid.
7:0	PAIR_0_ INTAR_ SHORT_ POINT	R/O	0x0	Retain	Intra short distance for pair 0 If CDT is done while Cable diagnostic test control register 0x16 bit[13] is 0, these bits indicate the inter short distance between pair 0 and the pair indicated by MMD3 — Cable diagnostics register 0x8064 bits[15:12]. The distance is in sample cycle, and can be transfered in meter by being multiplied by about 0.8.

17.5.15 MMD3 — Cable diagnostics pair 1 length register

Offset: 0x8066

Table 17-66 MMD3 — Cable diagnostics pair 1 length register

Bit	Field	Access type	HW reset	SW reset	Description
15:8	PAIR_1_ INTER_ SHORT_ POINT	R/O	0x0	Retain	Inter short distance for pair 1 The distance is in sample cycle, and can be transfered in meter by being multiplied by about 0.8. If CDT is done and MMD3 — Cable diagnostics register 0x8064 bits[11:8] is 0x1, 0x4, 0x8 or 0xC, then the value is invalid.
7:0	PAIR_1_ INTAR_ SHORT_ POINT	R/O	0x0	Retain	Intra short distance If CDT is done while Cable diagnostic test control register 0x16 bit[13] is 0, these bits indicate the inter short distance between pair 1 and the pair indicated by MMD3 — Cable diagnostics register 0x8064 bits[11:8]. The distance is in sample cycle, and can be transfered in meter by being multiplied by about 0.8.

17.5.16 MMD3 — Cable diagnostics pair 2 length register

Offset: 0x8067

Table 17-67 MMD3 — Cable diagnostics pair 2 length register

Bit	Field	Access type	HW reset	SW reset	Description
15:8	PAIR_2_ INTER_ SHORT_ POINT	R/O	0x0	Retain	Inter short distance for pair 2 The distance is in sample cycle, and can be transfered in meter by being multiplied by about 0.8. If CDT is done and MMD3 — Cable diagnostics register 0x8064 bits[7:4] is 0x1, 0x4, 0x8 or 0xC, then the value is invalid.
7:0	PAIR_2_ INTAR_ SHORT_ POINT	R/O	0x0	Retain	Intra short distance If CDT is done while Cable diagnostic test control register 0x16 bit[13] is 0, these bits indicate the inter short distance between pair 2 and the pair indicated by MMD3 — Cable diagnostics register 0x8064 bits[7:4]. The distance is in sample cycle, and can be transfered in meter by being multiplied by about 0.8.

17.5.17 MMD3 — Cable diagnostics pair 3 length register

Offset: 0x8068

Table 17-68 MMD3 — Cable diagnostics pair 3 length register

Bit	Field	Access type	HW reset	SW reset	Description
15:8	PAIR_3_ INTER_ SHORT_ POINT	R/O	0x0	Retain	Inter short distance for pair 3 The distance is in sample cycle, and can be transfered in meter by being multiplied by about 0.8. If CDT is done and MMD3 — Cable diagnostics register 0x8064 bit[3:0] is 0x1, 0x4, 0x8 or 0xC, then the value is invalid.
7:0	PAIR_3_ INTAR_ SHORT_ POINT	R/O	0x0	Retain	Intra short distance If CDT is done while Cable diagnostic test control register 0x16 bit[13] is 0, these bits indicate the inter short distance between pair 3 and the pair indicated by MMD3 — Cable diagnostics register 0x8064 bit[3:0]. The distance is in sample cycle, and can be transfered in meter by being multiplied by about 0.8.

17.6 MMD7 registers

Table 17-69 MMD7 registers summary

Address	Description
0x0	"MMD7 — Auto-negotiation control register" on page 93
0x5	"MMD7 — Auto-negotiation package register" on page 93
0X3C	"MMD7 — EEE advertisement register" on page 94
0X3D	"MMD7 — EEE LP advertisement register" on page 95
0X8000	"MMD7 — EEE capability auto-negotiation results register" on page 96
0X8005	"MMD7 — Fiber Hibernation register" on page 96
0X800E	"MMD7 — PRBS error count 1 register" on page 97
0X800F	"MMD7 — PRBS error count 2 register" on page 97
0X8011	"MMD7 — SGMII drive control register" on page 97
0X8012	"MMD7 — SGMII low power control register" on page 98
0X8016	"MMD7 — PAD control register" on page 98
0X8028	"MMD7 — MDIO broadcast control register" on page 99
0X8029	"MMD7 — CRC checker and packet counter register" on page 100
0X802A	"MMD7 — Valid ingress packet counter 1 register" on page 100
0X802B	"MMD7 — Valid ingress packet counter 2 register" on page 101
0X802C	"MMD7 — Erred ingress packet counter register" on page 102
0X802D	"MMD7 — Valid egress packet counter 1 register" on page 103
0X802E	"MMD7 — Valid egress packet counter 2 register" on page 104
0X802F	"MMD7 — Erred egress packet counter register" on page 105
0X805E	"MMD7 — Fiber hibernation control register" on page 105
0X8073	"MMD7 — Global LED control bit description" on page 106
0X8074	"MMD7 — LED_100_n control 1 register" on page 108
0X8075	"MMD7 — LED_100_n control 2 register" on page 109
0X8076	"MMD7 — LED_1000_n control 1 register" on page 111
0X8077	"MMD7 — LED_1000_n control 2 register" on page 112
0X807E	"MMD7 — Fiber mode auto-detection register" on page 114

17.6.1 MMD7 — Auto-negotiation control register

Offset: 0x0

Table 17-70 MMD7 — Auto-negotiation control register

Bit	Field	Access type	HW reset	SW reset	Description
15:14	Reserved	R/W	0x0	1	–
13	XNP_CTRL	R/W	0x1	Retain	If Auto-negotiation advertisement register — copper page 0x4 bit[12] is set to 0, the setting of this bit have no effect. ■ 1 = Local device intends to enable the exchange of extended next page. ■ 0 = Local device does not intend to enable the exchange of extended next page.
12:0	Reserved	R/O	0x0	Retain	Always be 0.

17.6.2 MMD7 — Auto-negotiation package register

Offset: 0x5

Table 17-71 MMD7 — Auto-negotiation package register

Bit	Field	Access type	HW reset	SW reset	Description
15:8	Reserved	R/O	0x0	Retain	–
7	AUTO_NEG_ PRESENT	R/O	0x1	Retain	Always be 1.
6:4	Reserved	R/O	0x0	Retain	–
3	PCS_ PRESENT	R/O	0x1	Retain	Always be 1.
2	Reserved	R/O	0x0	Retain	–
1	PMA_ PRESENT	R/O	0x1	Retain	Always be 1.
0	MII_REG_ PRESENT	R/O	0x1	Retain	Always be 1.

17.6.3 MMD7 — EEE advertisement register

Offset: 0x3C

Table 17-72 MMD7 — EEE advertisement register

Bit	Field	Access type	HW reset	SW reset	Description
15:3	Reserved	R/O	0x0	Retain	–
2	EEE_1000BT	R/W	0x1	Retain	The initial value of this bit depends on power-on strapping configuration by pin TDO. ■ 1 = Local device supports EEE operation for 1000BASE-T. The EEE operation is preferred. ■ 0 = Either local device does not support EEE operation for 1000BASE-T or EEE operation is not preferred. This bit is updated immediately after the writing operation. However, the configuration does not take effect until any of the following occurs: ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Restart auto-negotiation is triggered by writing Control register — copper page 0x0 bit[9]. ■ The port is switched from power down to normal operation by writing Control register — copper page 0x0 bit[11]. ■ Link goes down.

Table 17-72 MMD7 — EEE advertisement register

Bit	Field	Access type	HW reset	SW reset	Description
1	EEE_100BT	R/W	0x1	Retain	The initial value of this bit depends on power-on strapping configuration by pin TDO. ■ 1 = Local device supports EEE operation for 100BASE-TX. EEE operation is preferred. ■ 0 = Either local device does not support EEE operation for 100BASE-TX or EEE operation is not preferred. This bit is updated immediately after the writing operation. However, the configuration does not take effect until any of the following occurs: ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Restart auto-negotiation is triggered by writing Control register — copper page 0x0 bit[9]. ■ The port is switched from power down to normal operation by writing Control register — copper page 0x0 bit[11]. ■ Link goes down.
0	Reserved	R/O	0x0	Retain	–

17.6.4 MMD7 — EEE LP advertisement register

Offset: 0x3D

Table 17-73 MMD7 — EEE LP advertisement register

Bit	Field	Access type	HW reset	SW reset	Description
15:3	Reserved	R/O	0x0	Retain	–
2	EEE_1000BT_LP	R/O	0x0	Retain	■ 1 = Link partner supports EEE operation for 1000BASE-T. EEE operation is preferred. ■ 0 = Link partner does not support EEE operation for 1000BASE-T, or EEE operation is not preferred.
1	EEE_100BT_LP	R/O	0x0	Retain	■ 1 = Link partner supports EEE operation for 100BASE-TX. EEE operation is preferred. ■ 0 = Link partner does not support EEE operation for 100BT, or EEE operation is not preferred.
0	Reserved	R/O	0x0	Retain	–

17.6.5 MMD7 — EEE capability auto-negotiation results register

Offset: 0x8000

Table 17-74 MMD7 — EEE capability auto-negotiation results register

Bit	Field	Access type	HW reset	SW reset	Description
15:3	Reserved	R/O	0x0	Retain	–
2	EEE_1000T_EN	R/O	0x0	Retain	■ 1 = 1000BASE-T 802.3az is enabled. Both sides support EEE operation for 1000BASE-T. EEE operation is preferred. ■ 0 = 1000BASE-T 802.3az is disabled. Either side does not support EEE operation for 1000BASE-T, or EEE operation is not preferred.
1	EEE_100T_EN	R/O	0x0	Retain	■ 1 = 100BASE-TX 802.3az is enabled. Both sides support EEE operation for 100BASE-TX. EEE operation is preferred. ■ 0 = 100BASE-TX 802.3az is disabled. Either side does not support EEE operation for 100BASE-TX, or EEE operation is not preferred.
0	Reserved	R/O	0x0	Retain	–

17.6.6 MMD7 — Fiber Hibernation register

Offset: 0x8005

Table 17-75 MMD7 — Fiber Hibernation register

Bit	Field	Access type	HW reset	SW reset	Description
15	FIB_HIB_EN	R/W	0x1	Retain	■ 1 = Enable hibernation for fiber ■ 0 = Disable hibernation for fiber
14:0	Reserved	R/W	0X20C6	Retain	–

1. This register is available in port 4 only.

17.6.7 MMD7 — PRBS error count 1 register

Offset: 0x800E

Table 17-76 MMD7 — PRBS error count 1 register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	ERR_ CNT[15:0]	R/O	0x0	0x0	PBRS error counter[15:0] for SGMII The lower bits of PRBS error counter. These bits are used together with MMD7 — PRBS error count 2 register 0x800F bits[14:0]. This counter does not support clear-on-read. To clear the counter, write 0 to bit[14] in SGMII PBRS control register 0x1B.

1. This register is available in port 4 only.

17.6.8 MMD7 — PRBS error count 2 register

Offset: 0x800F

Table 17-77 MMD7 — PRBS error count 2 register

Bit	Field	Access type	HW reset	SW reset	Description
15	BIT_SYNC	R/O	0x0	Retain	Bit synced for PRBS test of SGMII
14:0	ERR_ CNT[30:16]	R/O	0x0	Retain	PBRS error counter[30:16] for SGMII

1. This register is available in port 4 only.

17.6.9 MMD7 — SGMII drive control register

Offset: 0x8011

Table 17-78 MMD7 — SGMII drive control register

Bit	Field	Access type	HW reset	SW reset	Description
15:13	SGMII_TXDR_ CTRL	R/W	0x1	Retain	TX driver strength control ■ 000 = driver output Vdiff, pp = 500 mV ■ 001 = 600 mV (default) ■ 010 = 700 mV ■ 011 = 800 mV ■ 100 = 900 mV ■ 101 = 1 V ■ 110 = 1.1 V ■ 111 = 1.2 V
12:11	Reserved	R/O	0x0	Retain	–

Table 17-78 MMD7 — SGMII drive control register

Bit	Field	Access type	HW reset	SW reset	Description
10:8	Reserved	R/W	0x6	Retain	–
7:0	Reserved	R/O	0x0	Retain	–

1. This register is available in port 4 only.

17.6.10 MMD7 — SGMII low power control register

Offset: 0x8012

Table 17-79 MMD7 — SGMII low power control register

Bit	Field	Access type	HW reset	SW reset	Description
15	EN_SGBX_ NA_SGMII	R/W	0x1	Retain	SGMII low power control ■ 1 = Enable low power mode ■ 0 = Disable low power mode
14:0	Reserved	R/W	0x53C4	Retain	–

1. This register is available in port 4 only.

17.6.11 MMD7 — PAD control register

Offset: 0x8016

Table 17-80 MMD7 — PAD control register

Bit	Field	Access type	HW reset	SW reset	Description
15	GPIO1_I	R/O	0x1	Retain	The input value of GPIO 1
14	GPIO1_O	R/W	0x1	Retain	Change the output value of GPIO 1 ■ 1 = Output high ■ 0 = Output low
13	GPIO1_D	R/W	0x1	Retain	This bit sets the direction of GPIO 1 if INTn pin is configured as GPIO. ■ 1 = Output ■ 0 = Input
12	SEL_INT_ GPIO	R/W	0x1	Retain	Select INTn and INTn_WOL as interrupt or GPIO. ■ 1 = Interrupt ■ 0 = GPIO
11	GPIO2_I	R/O	0x1	Retain	The input value of GPIO 2
10	GPIO2_O	R/W	0x0	Retain	Change the output value of GPIO 2 ■ 1 = Output high ■ 0 = Output low

Table 17-80 MMD7 — PAD control register

Bit	Field	Access type	HW reset	SW reset	Description
9	GPIO2_D	R/W	0x1	Retain	This bit sets the direction of GPIO 2 if INTn_WOL pin is configured as GPIO. ■ 1 = Output ■ 0 = Input
8	INT_PIN_TYPE	R/W	0x1	Retain	INTn and INTn_WOL pin type select: ■ 1 = Open drain ■ 0 = Normal I/O
7	LOS_PIN_ TYPE	R/W	0x1	Retain	LOS pin type select: ■ 1 = Open drain ■ 0 =Normal I/O
6	MDIO_PIN_ TYPE	R/W	0x0	Retain	MDIO pin type select: ■ 1 = Open drain ■ 0 = Normal IO
5:4	DR_MDIO	R/W	0x1	Retain	Control MDIO drive strength ■ 00 = Full drive strength ■ 01 = Half drive strength ■ 10/11 = 1/4 drive strength
3:0	Reserved	R/O	0x6	Retain	–

1. This register is available in port 4 only.

17.6.12 MMD7 — MDIO broadcast control register

Offset: 0x8028

Table 17-81 MMD7 — MDIO broadcast control register

Bit	Field	Access type	HW reset	SW reset	Description
15	EN_ BROADCAST_ ADDR	R/W	0x0	Retain	■ 1 = Enable MDIO broadcast ■ 0 = Disable MDIO broadcast
14:5	Reserved	R/O	0x0	Retain	Always be 0.
4:0	BROADCAST_ ADDR	R/W	0x1F	Retain	Broadcast address

17.6.13 MMD7 — CRC checker and packet counter register

Offset: 0x8029

Table 17-82 MMD7 — CRC checker and packet counter register

Bit	Field	Access type	HW reset	SW reset	Description
15:2	Reserved	R/O	0x0	Retain	–
1	CNT_ SELFCLR	R/W	0x0	Retain	■ 1 = Counter is cleared to 0 after read operation. ■ 0 = Counter is not cleared after read operation.
0	FRAME_CHK_ EN	R/W	0x0	Retain	■ 1 = Enable CRC checker and packet counter to record ingress and egress packets. ■ 0 = Disable CRC checker and packet counter.

17.6.14 MMD7 — Valid ingress packet counter 1 register

Offset: 0x802A

Table 17-83 MMD7 — Valid ingress packet counter 1 register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	IG_FRAME_ RECV_ CNT[31:16]	R/O	0x0	Retain	The high bits for valid ingress packet counter Used together with MMD7 — Valid ingress packet counter 2 register 0x802B. The counter indicates the number of valid packets received from link partner with good CRC. This register is cleared at either of the following occasions. ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Auto-negotiation is restarted by writing Control register — copper page 0x0 bit[9]. ■ Port is switched from down to normal status by writing Control register — copper page 0x0 bit[11]. ■ Clear-on-read operation is triggered. ■ Port is unplugged for 3 seconds. (exception: when port is set to a forced speed and manual MDI/MDIX, unplug action does not clear this register).

17.6.15 MMD7 — Valid ingress packet counter 2 register

Offset: 0x802B

Table 17-84 MMD7 — Valid ingress packet counter 2 register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	IG_FRAME_RECV_CNT[15:0]	R/O	0x0	Retain	The low bits for valid ingress packet counter Used together with MMD7 — Valid ingress packet counter 1 register 0x802A. The counter indicates the number of valid packets received from link partner with good CRC. This register is cleared at either of the following occasions. ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Auto-negotiation is restarted by writing Control register — copper page 0x0 bit[9]. ■ Port is switched from down to normal status by writing Control register — copper page 0x0 bit[11]. ■ Clear-on-read operation is triggered. ■ Port is unplugged for 3 seconds. (exception: when port is set to a forced speed and manual MDI/MDIX, unplug action does not clear this register).

17.6.16 MMD7 — Erred ingress packet counter register

Offset: 0x802C

Table 17-85 MMD7 — Erred ingress packet counter register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	IG_FRAME_ ERR_CNT	R/O	0x0	Retain	Indicate number of packets received from link partner with corrupted CRC. This register is cleared at either of the following occasions. ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Auto-negotiation is restarted by writing Control register — copper page 0x0 bit[9]. ■ Port is switched from down to normal status by writing Control register — copper page 0x0 bit[11]. ■ Clear-on-read operation is triggered. ■ Port is unplugged for 3 seconds. (exception: when port is set to a forced speed and manual MDI/MDIX, unplug action does not clear this register).

17.6.17 MMD7 — Valid egress packet counter 1 register

Offset: 0x802D

Table 17-86 MMD7 — Valid egress packet counter 1 register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	EG_FRAME_RECV_CNT[31:16]	R/O	0x0	Retain	The high bits for valid egress packet counter Used together with MMD7 — Valid egress packet counter 2 register 0x802E. The counter indicates the number of valid packets received from external MAC with good CRC. This register is cleared at either of the following occasions. ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Auto-negotiation is restarted by writing Control register — copper page 0x0 bit[9]. ■ Port is switched from down to normal status by writing Control register — copper page 0x0 bit[11]. ■ Clear-on-read operation is triggered. ■ Port is unplugged for 3 seconds. (exception: when port is set to a forced speed and manual MDI/MDIX, unplug action does not clear this register).

17.6.18 MMD7 — Valid egress packet counter 2 register

Offset: 0x802E

Table 17-87 MMD7 — Valid egress packet counter 2 register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	EG_FRAME_RECV_CNT[15:0]	R/O	0x0	Retain	The low bits for valid egress packet counter Used together with MMD7 — Valid egress packet counter 1 register 0x802D. The counter indicates the number of valid packets received from external MAC with good CRC. This register is cleared at either of the following occasions. ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Auto-negotiation is restarted by writing Control register — copper page 0x0 bit[9]. ■ Port is switched from down to normal status by writing Control register — copper page 0x0 bit[11]. ■ Clear-on-read operation is triggered. ■ Port is unplugged for 3 seconds. (exception: when port is set to a forced speed and manual MDI/MDIX, unplug action does not clear this register).

17.6.19 MMD7 — Erred egress packet counter register

Offset: 0x802F

Table 17-88 MMD7 — Erred egress packet counter register

Bit	Field	Access type	HW reset	SW reset	Description
15:0	EG_FRAME_ERR_CNT	R/O	0x0	Retain	Indicate number of valid packets received from external MAC with corrupted CRC. This register is cleared at either of the following occasions. ■ Software reset is asserted by writing Control register — copper page 0x0 bit[15]. ■ Auto-negotiation is restarted by writing Control register — copper page 0x0 bit[9]. ■ Port is switched from down to normal status by writing Control register — copper page 0x0 bit[11]. ■ Clear-on-read operation is triggered. ■ Port is unplugged for 3 seconds. (exception: when port is set to a forced speed and manual MDI/MDIX, unplug action does not clear this register).

17.6.20 MMD7 — Fiber hibernation control register

Offset: 0x805E

Table 17-89 MMD7 — Fiber hibernation control register

Bit	Field	Access type	HW reset	SW reset	Description
15:13	Reserved	R/W	0x3	Retain	–
12	FIBER_HIBERNATION	R/W	0x0	Retain	■ 1 = Enable Fiber hibernation ■ 0 = disable fiber hibernation
11:0	Reserved	R/W	0xF65	Retain	–

1. This register is available in port 4 only.

17.6.21 MMD7 — Global LED control register

Offset: 0x8073

Table 17-90 MMD7 — Global LED control bit description

Bit	Field	Access type	HW reset	SW reset	Description
15	Reserved	R/W	0x1	Retain	–
14	COL_BLK_SEL	R/W	0x0	Retain	Blinking mode selection for frequency and duty cycle when collision is detected. ■ 0 = Blink_1 mode ■ 1 = Blink_2 mode See bits[11:0] for blink_1 and blink_2 mode.
13	LPBK_LED_ DIS	R/W	0x1	Retain	In digital loopback mode: ■ 0 = Enable LED blink if active. ■ 1 = MII register 0x0 (copper page or fiber/SGMII page) bit[14] is set to 1, disable LED blink if active.
12	Reserved	R/W	0x1	Retain	–

Table 17-90 MMD7 — Global LED control bit description (cont.)

Bit	Field	Access type	HW reset	SW reset	Description
11:6	BLINK_1	R/W	0x8	Retain	[11:9]: Frequency select for blink_1 mode ■ 000 = 2 Hz ■ 001 = 4 Hz ■ 010 = 8 Hz ■ 011 = 16 Hz ■ 100 = 32 Hz ■ 101 = 64 Hz ■ 110 = 128 Hz ■ 111 = 256 Hz [8:6]: Duty cycle select for blink_1 mode ■ 000 = 50% on 50% off ■ 001 = 75% on 25% off ■ 010 = 25% on 75% off ■ 011 = 33% on 67% off ■ 100 = 67% on 33% off ■ 101 = 17% on 83% off ■ 110 = 83% on 17% off ■ 111 = 8% on 92% off
5:0	BLINK_2	R/W	0x10	Retain	[5:3]: Frequency select for blink_2 mode ■ 000 = 2 Hz ■ 001 = 4 Hz ■ 010 = 8 Hz ■ 011 = 16 Hz ■ 100 = 32 Hz ■ 101 = 64 Hz ■ 110 = 128 Hz ■ 111 = 256 Hz [2:0]: Duty cycle select for blink_2 mode ■ 000 = 50% on 50% off ■ 001 = 75% on 25% off ■ 010 = 25% on 75% off ■ 011 = 33% on 67% off ■ 100 = 67% on 33% off ■ 101 = 17% on 83% off ■ 110 = 83% on 17% off ■ 111 = 8% on 92% off

17.6.22 MMD7 — LED_100_n control 1 register

Offset: 0x8074

Table 17-91 MMD7 — LED_100_n control 1 register

Bit	Field	Access type	HW reset	SW reset	Description
15:14	Reserved	R/O	0x0	Retain	Always be 0.
13	Reserved	R/W	0x0	Retain	–
12	LED_FDX_ ON_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n is on when copper link is up at full-duplex mode. ■ 0 = This bit is invalid and does not control LED behavior.
11	LED_HDX_ ON_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n is on when copper link is up at half-duplex mode. ■ 0 = This bit is invalid and does not control LED behavior.
10	LED_TXACT_ BLK_EN_1	R/W	0x1	Retain	■ 1 = LED_100_n blinks when copper Tx is active and LED_100 is on. ■ 0 = This bit is invalid and does not control LED behavior.
9	LED_RXACT_ BLK_EN_1	R/W	0x1	Retain	■ 1 = LED_100_n blinks when copper Rx is active and LED_100 is on. ■ 0 = This bit is invalid and does not control LED behavior.
8	LED_TXACT_ ON_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n is on when copper Tx is active. ■ 0 = This bit is invalid and does not control LED behavior.
7	LED_RXACT_ ON_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n is on when copper Rx is active. ■ 0 = This bit is invalid and does not control LED behavior.
6	LED_GT_ON_ EN_1	R/W	0x0	Retain	■ 1 = LED_100_n is on when 1000BASE-T link is up. ■ 0 = This bit is invalid and does not control LED behavior.
5	LED_HT_ON_ EN_1	R/W	0x1	Retain	■ 1 = LED_100_n is on when 100BASE-TX link is up. ■ 0 = This bit is invalid and does not control LED behavior.
4	LED_BT_ON_ EN_1	R/W	0x1	Retain	■ 1 = LED_100_n is on when 10BASE-Te link is up. ■ 0 = This bit is invalid and does not control LED behavior.
3	LED_COL_ BLK_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n blinks when copper link is up and collision occurs. ■ 0 = This bit is invalid and does not control LED behavior.

Table 17-91 MMD7 — LED_100_n control 1 register

Bit	Field	Access type	HW reset	SW reset	Description
2	LED_GT_BLK_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n blinks when 1000BASE-T link is up. ■ 0 = This bit is invalid and does not control LED behavior.
1	LED_HT_BLK_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n blinks when 100BASE-TX link is up. ■ 0 = This bit is invalid and does not control LED behavior.
0	LED_BT_BLK_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n blinks when 10BASE-Te link is up. ■ 0 = This bit is invalid and does not control LED behavior.

17.6.23 MMD7 — LED_100_n control 2 register

Offset: 0x8075

Table 17-92 MMD7 — LED_100_n control 2 register

Bit	Field	Access type	HW reset	SW reset	Description
15	LED_1_FORCE_EN	R/O	0x0	Retain	■ 1 = LED_100_n force mode ■ 0 = LED_100_n normal mode
14:13	LED_1_FORCE_MODE	R/W	0x0	Retain	Valid only when bit[15] is 1. ■ 11 = Force LED_100_n to blink at blink_2 mode. ■ 10 = Force LED_100_n to blink at blink_1 mode. ■ 01 = Force LED_100_n on. ■ 00 = Force LED_100_n off.
12	Reserved	R/W	0x0	Retain	–
11	LED_FIBER_COL_BLK_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n blinks when port 4 fiber link is up and collision occurs. ■ 0 = This bit is invalid and does not control LED behavior.
10	LED_FIBER_TXACT_BLK_EN_1	R/W	0x1	Retain	■ 1 = LED_100_n blinks when port 4 fiber link is up, LED_100_n is on, and Tx is active. ■ 0 = This bit is invalid and does not control LED behavior.
9	LED_FIBER_RXACT_BLK_EN_1	R/W	0x1	Retain	■ 1 = LED_100_n blinks when port 4 fiber link is up, LED_100_n is on, and Rx is active. ■ 0 = This bit is invalid and does not control LED behavior.

Table 17-92 MMD7 — LED_100_n control 2 register

Bit	Field	Access type	HW reset	SW reset	Description
8	LED_FIBER_1000BX_BLK_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n blinks when port 4 fiber link is up and speed mode is 1000BASE-X. ■ 0 = This bit is invalid and does not control LED behavior.
7	LED_FIBER_100FX_BLK_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n blinks when port 4 fiber link is up and speed mode is 100BASE-FX. ■ 0 = This bit is invalid and does not control LED behavior.
6	LED_FIBER_FDX_ON_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n is on when port 4 fiber link is up and duplex mode is full. ■ 0 = This bit is invalid and does not control LED behavior.
5	LED_FIBER_HDX_ON_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n is on when port 4 fiber link is up and duplex mode is half. ■ 0 = This bit is invalid and does not control LED behavior.
4	LED_FIBER_TXACT_ON_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n is on when port 4 fiber link is up and Tx is active. ■ 0 = This bit is invalid and does not control LED behavior.
3	LED_FIBER_RXACT_ON_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n is on when port 4 fiber link is up and Rx is active. ■ 0 = This bit is invalid and does not control LED behavior.
2	LED_FIBER_1000BX_ON_EN_1	R/W	0x1	Retain	■ 1 = LED_100_n is on when port 4 fiber link is up and speed mode is 1000BASE-X. ■ 0 = This bit is invalid and does not control LED behavior.
1	LED_FIBER_100FX_ON_EN_1	R/W	0x0	Retain	■ 1 = LED_100_n is on when port 4 fiber link is up and speed mode is 100BASE-FX. ■ 0 = This bit is invalid and does not control LED behavior.
0	Reserved	R/W	0x0	Retain	–

1. Bits[12:0] are available in port 4 only.

17.6.24 MMD7 — LED_1000_n control 1 register

Offset: 8076

Table 17-93 MMD7 — LED_1000_n control 1 register

Bit	Field	Access type	HW reset	SW reset	Description
15:14	Reserved	R/O	0x0	Retain	Always be 0.
13	Reserved	R/W	0x0	Retain	–
12	LED_FDX_ ON_EN_2	R/W	0x0	Retain	■ 1 = LED_1000_n is on when copper link is up at full-duplex mode. ■ 0 = This bit is invalid and does not control LED behavior.
11	LED_HDX_ ON_EN_2	R/W	0x0	Retain	■ 1 = LED_1000_n is on when copper link is up at half-duplex mode. ■ 0 = This bit is invalid and does not control LED behavior.
10	LED_TXACT_ BLK_EN_2	R/W	0x1	Retain	■ 1 = LED_1000_n blinks when copper Tx is active and LED_100 is on. ■ 0 = This bit is invalid and does not control LED behavior.
9	LED_RXACT_ BLK_EN_2	R/W	0x1	Retain	■ 1 = LED_1000_n blinks when copper Rx is active and LED_100 is on. ■ 0 = This bit is invalid and does not control LED behavior.
8	LED_TXACT_ ON_EN_2	R/W	0x0	Retain	■ 1 = LED_1000 is on when copper Tx is active. ■ 0 = This bit is invalid and does not control LED behavior.
7	LED_RXACT_ ON_EN_2	R/W	0x0	Retain	■ 1 = LED_1000 is on when copper Rx is active. ■ 0 = This bit is invalid and does not control LED behavior.
6	LED_GT_ON_ EN_2	R/W	0x1	Retain	■ 1 = LED_1000 is on when 1000BASE-T link is up. ■ 0 = This bit is invalid and does not control LED behavior.
5	LED_HT_ON_ EN_2	R/W	0x0	Retain	■ 1 = LED_1000 is on when 100BASE-TX link is up. ■ 0 = This bit is invalid and does not control LED behavior.
4	LED_BT_ON_ EN_2	R/W	0x0	Retain	■ 1 = LED_1000 is on when 10BASE-Te link is up. ■ 0 = This bit is invalid and does not control LED behavior.
3	LED_COL_ BLK_EN_2	R/W	0x0	Retain	■ 1 = LED_1000 blinks when copper link is up and collision occurs. ■ 0 = This bit is invalid and does not control LED behavior.

Table 17-93 MMD7 — LED_1000_n control 1 register

Bit	Field	Access type	HW reset	SW reset	Description
2	LED_GT_BLK_EN_2	R/W	0x0	Retain	■ 1 = LED_1000 blinks when 1000BASE-T link is up. ■ 0 = This bit is invalid and does not control LED behavior.
1	LED_HT_BLK_EN_2	R/W	0x0	Retain	■ 1 = LED_1000 blinks when 100BASE-TX link is up. ■ 0 = This bit is invalid and does not control LED behavior.
0	LED_BT_BLK_EN_2	R/W	0x0	Retain	■ 1 = LED_1000 blinks when 10BASE-Te link is up. ■ 0 = This bit is invalid and does not control LED behavior.

17.6.25 MMD7 — LED_1000_n control 2 register

Offset: 0x8077

Table 17-94 MMD7 — LED_1000_n control 2 register

Bit	Field	Access type	HW reset	SW reset	Description
15	LED_2_FORCE_EN	R/O	0x0	Retain	■ 1 = LED_1000_n force mode ■ 0 = LED_1000_n normal mode
14:13	LED_2_FORCE_MODE	R/W	0x0	Retain	Valid only when bit[15] is 1. ■ 11 = Force LED_1000_n to blink at blink_2 mode. ■ 10 = Force LED_1000_n to blink at blink_1 mode. ■ 01 = Force LED_1000 on. ■ 00 = Force LED_1000 off.
12	Reserved	R/W	0x0	Retain	–
11	LED_FIBER_COL_BLK_EN_2	R/W	0x0	Retain	■ 1 = LED_1000_n blinks when port 4 fiber link is up and collision occurs. ■ 0 = This bit is invalid and does not control LED behavior.
10	LED_FIBER_TXACT_BLK_EN_2	R/W	0x1	Retain	■ 1 = LED_1000_n blinks when port 4 fiber link is up, LED_1000_n is on, and Tx is active. ■ 0 = This bit is invalid and does not control LED behavior.
9	LED_FIBER_RXACT_BLK_EN_2	R/W	0x1	Retain	■ 1 = LED_1000_n blinks when port 4 fiber link is up, LED_1000_n is on, and Rx is active. ■ 0 = This bit is invalid and does not control LED behavior.

Table 17-94 MMD7 — LED_1000_n control 2 register

Bit	Field	Access type	HW reset	SW reset	Description
8	LED_FIBER_1000BX_BLK_EN_2	R/W	0x0	Retain	■ 1 = LED_1000_n blinks when port 4 fiber link is up and speed mode is 1000BASE-X. ■ 0 = This bit is invalid and does not control LED behavior.
7	LED_FIBER_100FX_BLK_EN_2	R/W	0x0	Retain	■ 1 = LED_1000_n blinks when port 4 fiber link is up and speed mode is 100BASE-FX. ■ 0 = This bit is invalid and does not control LED behavior.
6	LED_FIBER_FDX_ON_EN_2	R/W	0x0	Retain	■ 1 = LED_1000_n is on when port 4 fiber link is up and duplex mode is full. ■ 0 = This bit is invalid and does not control LED behavior.
5	LED_FIBER_HDX_ON_EN_2	R/W	0x0	Retain	■ 1 = LED_1000_n is on when port 4 fiber link is up and duplex mode is half. ■ 0 = This bit is invalid and does not control LED behavior.
4	LED_FIBER_TXACT_ON_EN_2	R/W	0x0	Retain	■ 1 = LED_1000_n is on when port 4 fiber link is up and Tx is active. ■ 0 = This bit is invalid and does not control LED behavior.
3	LED_FIBER_RXACT_ON_EN_2	R/W	0x0	Retain	■ 1 = LED_1000_n is on when port 4 fiber link is up and Rx is active. ■ 0 = This bit is invalid and does not control LED behavior.
2	LED_FIBER_1000BX_ON_EN_2	R/W	0x1	Retain	■ 1 = LED_1000_n is on when port 4 fiber link is up and speed mode is 1000BASE-X. ■ 0 = This bit is invalid and does not control LED behavior.
1	LED_FIBER_100FX_ON_EN_2	R/W	0x0	Retain	■ 1 = LED_1000_n is on when port 4 fiber link is up and speed mode is 100BASE-FX. ■ 0 = This bit is invalid and does not control LED behavior.
0	Reserved	R/W	0x0	Retain	–

1. Bits[12:0] are available in port 4 only.

17.6.26 MMD7 — Fiber mode auto-detection register

Offset: 0x807E

Table 17-95 MMD7 — Fiber mode auto-detection register

Bit	Field	Access type	HW reset	SW reset	Description
15:4	Reserved	R/O	0x0	Retain	–
3:3	FIBER_ MODE_AD	R/O	0x1	Retain	Fiber mode auto-detection result ■ 1 = 1000BASE-X mode. ■ 0 = 100BASE-FX mode.
2:1	Reserved	R/O	0x0	Retain	Always be 0.
0:0	EN_FIBER_ MODE_AD	R/W	0x0	Retain	Enable fiber mode auto-detection ■ 1 = Enable auto-detection of fiber mode. ■ 0 = Disable auto-detection of fiber mode.

1. This register is available in port 4 only.