QCA9558 802.11n 3x3 Dual Band Features WLAN SoC

Data Sheet

80-Y0805-3 Rev. E

March 2014

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Revision history

Rev	Date	Description
A	November 2012	Initial release
B	March 2013	Updated Table 3-5 and Table 3-6, DDR configurations. Edit to Table 3-17, GPIO Output Select Values. Updated Figure 3-1, Functional Block Diagram.
C	June 2013	Edited $T_{MDHOLDW}$ values in Table 12-7.
D	July 2013	Added MAC_PCU_LOCATION_MODE_TIMER register Updated MDIO Timing, section 12.7 Updated ordering information
E	March 2014	■ Updated Table 3-5, DDR Configurations when DDR_CONFIG2_SWAP_A26_A27 = 0 ■ Updated Section 10.11.11, Pulse Width Modulation Control (PWM_CTL)

Contents

1 Introduction

1.1 General Description

The Qualcomm® XSPAN™ QCA9558 is a highly integrated and feature-rich IEEE 802.11n 3x3 2.4/5 GHz System-on-a-Chip (SoC) for advanced WLAN AP/router platforms.

It includes a MIPS 74Kc processor, one PCI Express 1.1 Root Complex and one PCI Express Root Complex/Endpoint interfaces, one RGMII interface, one SGMII interface, two USB 2.0 MAC/PHY, and external memory interface for serial Flash, DDR1 or DDR2, I^2S/SPDIF-Out audio interface, SLIC VOIP/PCM interface, two UARTs, and GPIOs that can be used for LED controls or other general purpose interface configurations.

The QCA9558 supports 802.11n operations up to 216.7 Mbps for 20 MHz and 450 Mbps for 40 MHz, and 802.11a/b/g data rates. Additional features include Maximal Likelihood (ML) decoding, Low-Density Parity Check (LDPC), Maximal Ratio Combining (MRC), Tx Beamforming (TxBF), and On-Chip One-Time Programmable (OTP) memory.

The QCA9558 PCIE Root Complex interface can be used to connect to an endpoint such as the Qualcomm Atheros single-chip MAC/PHY/radio for dual concurrent WLAN applications. The QCA9558 supports booting from either SPI NOR or NAND flash. If NOR flash is used as boot codestore, an additional NAND flash device can still be connected, for end-user multi-media storage and other applications.

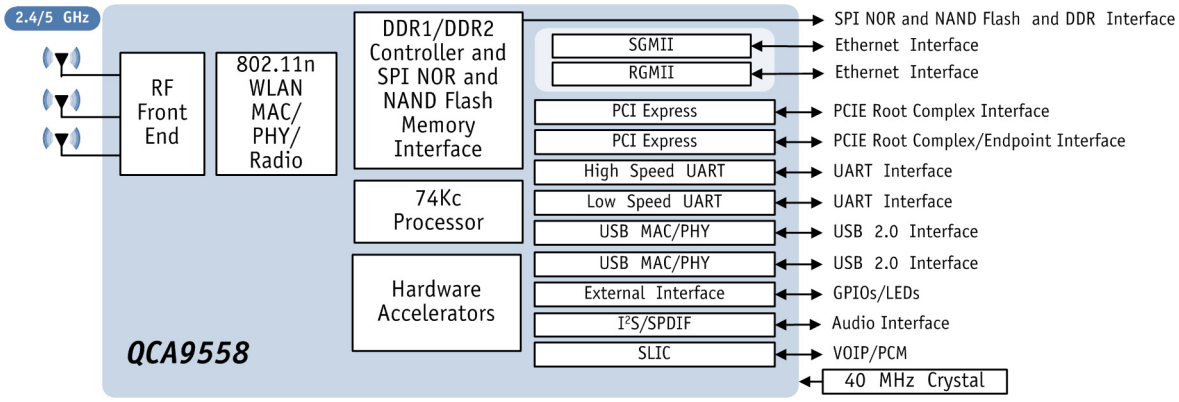
When connecting the QCA9558 to an external host through the PCIE Endpoint interface, or the USB Device interface, the QCA9558 can off load the host CPU from computation-intensive functions, allowing it to focus on its dedicated tasks.

1.2 Features

- 74Kc MIPS processor with 64 KB I-Cache and 32 KB D-Cache, target to operate at up to 720 MHz
- External 16- or 32-bit DDR1, DDR2 target to operate at up to 300 MHz (600 M transfers/sec)
- NAND and SPI NOR Flash memory support
- One RGMII interface
- One SGMII interface
- Hardware-based NAT and ACL accelerators for Ethernet interface
- Both PCI Express 1.1 Root Complex and Root Complex/Endpoint interfaces supported simultaneously
- Two USB 2.0 controllers with built-in MAC/ PHY, support Host mode and Host or Device mode

- Boot from external CPU via PCIE, USB, xMII, SGMII, eliminating need for external flash
- I^2S/SPDIF-out audio interface
- SLIC for VOIP/PCM
- One low-speed UART (115 Kbps), one high-speed UART (3 Mbps), and multiple GPIO pins for general purpose I/O
- Single-ended RF ports with integrated matching to simplify board design and layout
- Integrated RF Front-End including LNAs
- Optional external LNA
- 20 and 40 MHz channelization
- 40 MHz reference clock input
- 1.2 V switching regulator
- 415-pin 18 x 18 mm BGA package

1.3 QCA9558 System Block Diagram



2 Pin Descriptions

This section contains both a package pinout and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
OD	An open-drain digital output signal
O	A digital output signal
P	A power or ground signal

Table 2-1 shows the top left see-through view of the QCA9558 pinout.

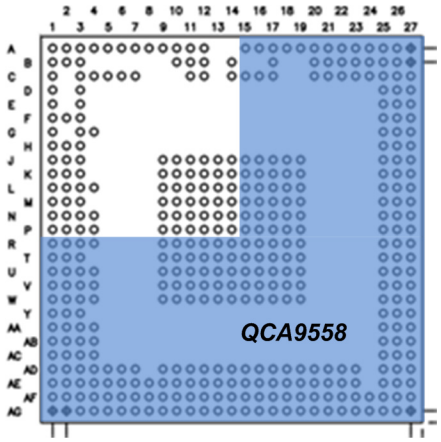


Table 2-1 QCA9558 Pinout (Top Left)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	TX2G_0	TX5G_0	PABIAS 5G_0	GND	RX2G_ 1	AVDD12_ IPDRF_1	RX5G_ 1	PABIAS 2G_1	TX2G_ 1	TX5G_1	PABIA S5G_1	GND		
B	AVDD33_ IPDRF	NC	GND							AVDD33_ IPDRF_1	GND	AVDD12 _SYNTH		AVDD12_ SYNTHD
C	PABIAS 2G_0		GND	AVDD12 _PHY_0	NC	XLNA BIAS_1	GND				GND	AVDD33 _SYNTH		AVDD12_ LO
D	RX5G_0		GND											
E	AVDD12_ IPDRF_0		XLNABIA S_0											
F	RX2G_0	GND	GND											
G	GND		GND	GND										
H	GPIO21	GPIO22	GPIO23											
J	GPIO18	GPIO19	GPIO20						GND	GND	GND	GND	GND	GND
K	GPIO17	GPIO16	VDD25						GND	GND	GND	GND	GND	GND
L	GPIO15	GPIO14	GND	GND					GND	GND	GND	GND	GND	GND
M	GPIO13	GPIO12	GPIO11						GND	GND	GND	GND	GND	GND
N	NAND_ DATA_ IO_2	NAND_ DATA_ IO_1	NAND_ DATA_IO_ 0	DVDD12					GND	GND	GND	GND	GND	GND
P	NAND_ DATA_ IO_4	NAND_ DATA_ IO_3	DVDD12	DVDD12					GND	GND	GND	GND	GND	GND

Table 2-2 shows the bottom left see-through view of the QCA9558 pinout.

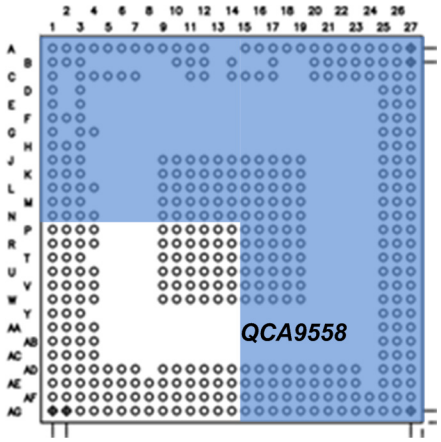


Table 2-2 QCA9558 Pinout (Bottom Left)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
R	NAND_ DATA_ IO_7	NAND_ DATA_ IO_6	NAND_ DATA_ IO_5	DVDD12					GND	GND	GND	GND	GND	GND
T	NAND_ ALE	NAND_ WE_L	NAND_ WP_L						GND	GND	GND	GND	GND	GND
U	NAND_ CS_0	NAND_ CLE	GND	GND					GND	GND	GND	GND	GND	GND
V	USB2_ DP	USB2_ DM	NAND_ RE_L	AVDD33_ USB2					GND	GND	GND	GND	GND	GND
W	USB1_ DP	USB1_ DM	DVDD12 _USB1	DVDD12 _USB1_ PLL					GND	GND	GND	GND	GND	GND
Y	DDR_ DATA_0	DDR_ DATA_1	NAND_ RB_L_0											
AA	DDR_ DATA_2	DDR_ DATA_3	GND	GND										
AB	DDR_ DATA_4	DDR_ DATA_5	DVDD12	DVDD12										
AC	DDR_ DATA_6	DDR_ DATA_7	VDD_ DDR	VDD_ DDR										
AD	DDR_ DQS_0	DDR_ DQM_0	VDD_ DDR	GND	VDD_ DDR	VDD_ DDR	GND		DVDD12	DVDD12	GND	VDD_ DDR	VDD_ DDR	DVDD12
AE	DDR_ DATA_15	DDR_ DATA_ 14	GND	DDR_ VREF_0	VDD_ DDR	VDD_ DDR	GND	AVDD33 _DPLLS	DVDD12	DDR_ DATA_17	GND	VDD_ DDR	VDD_ DDR	DVDD12
AF	DDR_ DATA_13	DDR_ DATA_ 11	DDR_ DATA_23	DDR_ DATA_22	DDR_ DATA_21	DDR_ DATA_20	DDR_ DATA_ 19	DDR_ CKE_L	DDR_ DATA_18	DDR_A_ 12	DDR_ DATA_ 16	DDR_A_ 9	DDR_A_8	DDR_ DATA_31
AG	DDR_ DATA_12	DDR_ DATA_ 10	DDR_ DATA_9	DDR_ DATA_8	DDR_A_ 10	DDR_ DQS_1	DDR_ DQM_1	DDR_ CK_N	DDR_ CK_P	DDR_A_ 13	DDR_ A_11	DDR_ DQS_2	DDR_A_7	DDR_A_6

Table 2-3 shows the top right see-through view of the QCA9558 pinout.

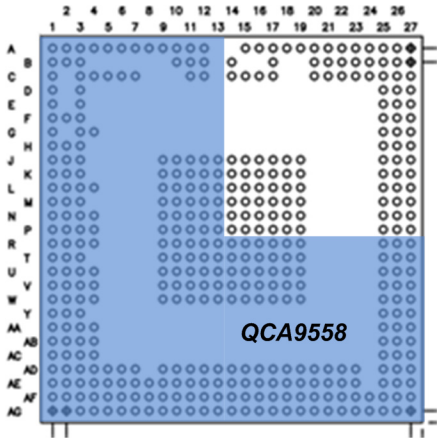


Table 2-3 QCA9558 Pinout (Top Right)

	15	16	17	18	19	20	21	22	23	24	25	26	27
A	RX2G_2	AVDD12_IPDRF_2	RX5G_2	PABIAS2G_2	TX2G_2	TX5G_2	PABIAS5G_2	GND	GPIO1	GPIO5	GPIO6	SWCOM_1	SWCOM_0
B			GND			AVD33_IPDRF_2	GND	SYS_RST_OUT_L	GPIO2	GPIO4	GPIO7	AVD33_PLL	XPABIAS5_2
C	NC	XLNABIAS_2	GND			GND	GND	GPIO0	GPIO3	VDD25_GPIO	XPABIAS2_2	XPABIAS5_1	XPABIAS2_1
D											XPABIAS5_0	XPABIAS2_0	XTALO
E											AVDD12_PHY_1	AVDD12_BIAS	XTALI
F											AVDD12_PLL	GND	AVD33_XTAL
G											GPIO8	GPIO9	GPIO10
H											VDD25	PCIE1_RST_L	PCIE1_CLKOUT_N
J	GND	GND	GND	GND	GND						DVDD12	PCIE1_CLKOUT_P	PCIE1_RX_N
K	GND	GND	GND	GND	GND						AVDD12_PCIE	PCIE1_RX_P	PCIE1_TX_P
L	GND	GND	GND	GND	GND						AVDD12_PCIE	PCIE1_TX_N	PCIE0_CLKOUT_N
M	GND	GND	GND	GND	GND						AVDD12_PCIE	PCIE0_CLKOUT_P	PCIE0_RX_N
N	GND	GND	GND	GND	GND						AVDD12_PCIE	PCIE0_RX_P	PCIE0_TX_P
P	GND	GND	GND	GND	GND						DVDD12	PCIE0_TX_N	PCIE0_RST_OUT_L

Table 2-4 shows the bottom right see-through view of the QCA9558 pinout.

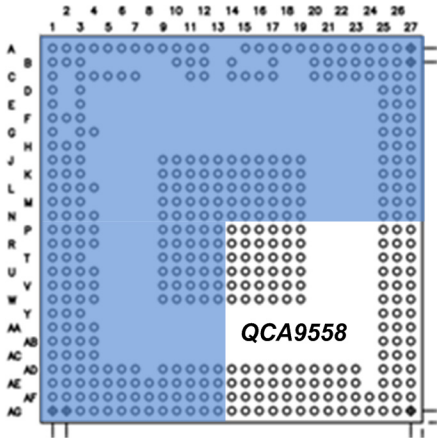


Table 2-4 QCA9558 Pinout (Bottom Right)

	15	16	17	18	19	20	21	22	23	24	25	26	27
R	GND	GND	GND	GND	GND						ERX_EN	EMDC	EMDIO
T	GND	GND	GND	GND	GND						ERXD1	ERXD0	ERX_CLK
U	GND	GND	GND	GND	GND						GND	ERXD3	ERXD2
V	GND	GND	GND	GND	GND						ETXD0	ETX_EN	ETX_CLK
W	GND	GND	GND	GND	GND						ETXD3	ETXD2	ETXD1
Y											GND	GND	VDD25
AA											VDD_SGMII	SGMII_SIN	SGMII_SIP
AB											CTRL_DDR_XPNP	SGMII_SON	SGMII_SOP
AC											VDD33_SWREG	VDD33_LDO	RESET_L
AD	DVDD12	DVDD12	GND	VDD_DDR	VDD_DDR	VDD_DDR	GND	DVDD12	DVDD12		VDD33_SWREG	VDD33_SWREG	VDD33_SWREG
AE	DDR_DQM_2	DDR_VREF_1	GND	DDR_DATA_27	VDD_DDR	DDR_DATA_24	GND	DDR_DQM_3	DVDD12		SWREG_OUT	SWREG_OUT	SWREG_OUT
AF	DDR_DATA_30	DDR_DATA_28	DDR_DATA_29	DDR_RAS_L	DDR_DATA_26	DDR_DATA_25	DDR_DQS_3	DDR_A_1	DDR_A_3	GND	SWREG_OUT	SWREG_OUT	SWREG_OUT
AG	DDR_A_5	DDR_A_4	DDR_WE_L	DDR_CAS_L	DDR_CS_L	DDR_BA_0	DDR_BA_1	DDR_A_0	DDR_A_2	VDD33_GPIOREG	CTRL_XPNP_GPIO	VREG_SWREG_FB	SWREG_OUT

Table 2-5 provides the signal-to-pin relationship information for the QCA9558.

Table 2-5 Signal to Pin Relationships and Descriptions

Signal Name	Pin	Type	Description
General			
RESET_L	AC27	IH	External power on reset with weak pull up. This signal is internally pulled up to 3.3 V. It is recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with 3.3 V logic.
SYS_RST_OUT_L	B22	OD	System reset out, open drain, should be pulled up to V_{dd25} or V_{dd33} depends on the supply voltage of the external pin that is being driven.
XTALI	E27	I	40 MHz crystal When using an external clock (TCXO), the XTALI pin is grounded and the XTALO pin should be driven with a square wave clock. AC coupling is recommended for the clock signal to the XTALO pin. The internal circuit provides the DC bias of approximately 0.6 V. The peak-to-peak swing of the external clock can be between 0.3 V and 1.2 V. In general, larger swings and sharper edges reduce jitter, but introduce the potential of high frequency spurious tones. The phase noise of the oscillator should be lower than -145 dBc/Hz at 100 KHz carrier offset.
XTALO	D27	I/O	
Radio			
TX2G_0	A1	OA	Single-ended RF outputs for 2.4 GHz chain 0, 1, and 2 respectively
TX2G_1	A9		
TX2G_2	A19		
RX2G_0	F1	IA	Single-ended RF inputs for 2.4 GHz chain 0, 1, and 2 respectively
RX2G_1	A5		
RX2G_2	A15		
TX5G_0	A2	OA	Single-ended RF outputs for 5 GHz chain 0, 1, and 2 respectively
TX5G_1	A10		
TX5G_2	A20		
RX5G_0	D1	IA	Single-ended RF inputs for 5 GHz chain 0, 1, and 2 respectively
RX5G_1	A7		
RX5G_2	A17		
Analog Interface			
PABIAS2G_0	C1	Power amplifier bias for 2.4 GHz chain 0, 1, and 2 respectively	
PABIAS2G_1	A8		
PABIAS2G_2	A18		
PABIAS5G_0	A3	Power amplifier bias for 5 GHz chain 0, 1, and 2 respectively	
PABIAS5G_1	A11		
PABIAS5G_2	A21		
XPABIAS2_0	D26	Optional external power amplifier bias for 2.4 GHz chain 0, 1, and 2 respectively	
XPABIAS2_1	C27		
XPABIAS2_2	C25		

Table 2-5 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pin	Type	Description
XPABIAS5_0	D25	Optional external power amplifier bias for 5 GHz chain 0, 1, and 2 respectively	
XPABIAS5_1	C26		
XPABIAS5_2	B27		
XLNABIAS_0	E3	Optional external LNA bias for chain 0, 1, and 2 respectively	
XLNABIAS_1	C6		
XLNABIAS_2	C16		
External Switch Control			
SWCOM_0	A27	O	External RF switch control These output pins are in the V_{dd33} voltage domain.
SWCOM_1	A26	O	
PCI Express Root Complex			
PCIE0_CLKOUT_N	L27	OA	Differential reference clock (100 MHz), can be left open if not used
PCIE0_CLKOUT_P	M26	OA	
PCIE0_RX_N	M27	IA	Differential receive, can be left open if not used
PCIE0_RX_P	N26	IA	
PCIE0_TX_N	P26	OA	Differential transmit, can be left open if not used
PCIE0_TX_P	N27	OA	
PCIE0_RST_OUT_L	P27	OD	PCI Express reset, open drain, should be pulled up to V_{dd33} through 1 KΩ resistor, can be left open if not used.
PCI Express Root Complex/Endpoint			
PCIE1_CLKOUT_N	H27	IA/OA	Differential reference clock (100 MHz), these pins are outputs when in RC mode, and become inputs when in EP mode, can be left open if not used
PCIE1_CLKOUT_P	J26	IA/OA	
PCIE1_RX_N	J27	IA	Differential receive, can be left open if not used
PCIE1_RX_P	K26	IA	
PCIE1_TX_N	L26	OA	Differential transmit, can be left open if not used
PCIE1_TX_P	K27	OA	
PCIE1_RST_L	H26	I/OD	PCI Express reset, open drain output, should be pulled up to V_{dd33} through 1 KΩ resistor. This pin becomes input when in EP mode, can be left open if not used.

Table 2-5 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pin	Type	Description
External Memory Interface			
DDR_A_0	AG22	O	14-bit external memory address bus
DDR_A_1	AF22	O	
DDR_A_2	AG23	O	
DDR_A_3	AF23	O	
DDR_A_4	AG16	O	
DDR_A_5	AG15	O	
DDR_A_6	AG14	O	
DDR_A_7	AG13	O	
DDR_A_8	AF13	O	
DDR_A_9	AF12	O	
DDR_A_10	AG5	O	
DDR_A_11	AG11	O	
DDR_A_12	AF10	O	
DDR_A_13	AG10	O	
DDR_BA_0	AG20	O	2-bit bank address to indicate which bank the chip is accessing
DDR_BA_1	AG21	O	
DDR_CKE_L	AF8	O	Deactivates the external memory clock when the signal is high
DDR_CK_N	AG8	O	DDR_CK_P and DDR_CK_N are differential clock outputs from the QCA9558. All address and control signals timing are related to the crossing of the positive edge of DDR_CK_P and the negative edge of DDR_CK_N.
DDR_CK_P	AG9	O	
DDR_CS_L	AG19	O	External memory chip select signal, active low
DDR_CAS_L	AG18	O	When this signal is asserted, it indicates the address is a column address. Active when the signal is low.
DDR_RAS_L	AF18	O	When this signal is asserted, it indicates the address is a row address. Active when the signal is low.
DDR_DQM_0	AD2	O	DDR data mask for data byte 0, 1, 2, and 3
DDR_DQM_1	AG7	O	
DDR_DQM_2	AE15	O	
DDR_DQM_3	AE22	O	
DDR_DQS_0	AD1	I/O	DDR data strobe for data byte 0, 1, 2, and 3
DDR_DQS_1	AG6	I/O	
DDR_DQS_2	AG12	I/O	
DDR_DQS_3	AF21	I/O	
DDR_VREF_0	AE4	I	DDR reference level for SSTL signals
DDR_VREF_1	AE16	I	DDR reference level for SSTL signals
DDR_WE_L	AG17	O	When this signal is asserted, it indicates that the following transaction is write. Active when the signal is low.

Table 2-5 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pin	Type	Description
DDR_DATA_0	Y1	I/O	32-bit external memory data bus
DDR_DATA_1	Y2	I/O	
DDR_DATA_2	AA1	I/O	
DDR_DATA_3	AA2	I/O	
DDR_DATA_4	AB1	I/O	
DDR_DATA_5	AB2	I/O	
DDR_DATA_6	AC1	I/O	
DDR_DATA_7	AC2	I/O	
DDR_DATA_8	AG4	I/O	
DDR_DATA_9	AG3	I/O	
DDR_DATA_10	AG2	I/O	
DDR_DATA_11	AF2	I/O	
DDR_DATA_12	AG1	I/O	
DDR_DATA_13	AF1	I/O	
DDR_DATA_14	AE2	I/O	
DDR_DATA_15	AE1	I/O	
DDR_DATA_16	AF11	I/O	
DDR_DATA_17	AE10	I/O	
DDR_DATA_18	AF9	I/O	
DDR_DATA_19	AF7	I/O	
DDR_DATA_20	AF6	I/O	
DDR_DATA_21	AF5	I/O	
DDR_DATA_22	AF4	I/O	
DDR_DATA_23	AF3	I/O	
DDR_DATA_24	AE20	I/O	
DDR_DATA_25	AF20	I/O	
DDR_DATA_26	AF19	I/O	
DDR_DATA_27	AE18	I/O	
DDR_DATA_28	AF16	I/O	
DDR_DATA_29	AF17	I/O	
DDR_DATA_30	AF15	I/O	
DDR_DATA_31	AF14	I/O	

Table 2-5 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pin	Type	Description
GPIO			
GPIO0	C22	I/O	General purpose I/O, programmable, can to be used as JTAG, SPI, I^2S, SLIC, UARTs, LED control. Default input pins can be grounded, and default output pins can be left open if not used. Please note that GPIO18, GPIO19, and GPIO20 are open-drain GPIOs, can be used for CLKREQ#, WAKE# or similar pins needing open drain capability. When used as outputs, these pins should be pulled up to V_{dd25}. or V_{dd33} depends on the supply voltage of the external pin that is being driven.
GPIO1	A23	I/O	
GPIO2	B23	I/O	
GPIO3	C23	I/O	
GPIO4	B24	I/O	
GPIO5	A24	I/O	
GPIO6	A25	I/O	
GPIO7	B25	I/O	
GPIO8	G25	I/O	
GPIO9	G26	I/O	
GPIO10	G27	I/O	
GPIO11	M3	I/O	
GPIO12	M2	I/O	
GPIO13	M1	I/O	
GPIO14	L2	I/O	
GPIO15	L1	I/O	
GPIO16	K2	I/O	
GPIO17	K1	I/O	
GPIO18	J1	I/OD	
GPIO19	J2	I/OD	
GPIO20	J3	I/OD	
GPIO21	H1	I/O	
GPIO22	H2	I/O	
GPIO23	H3	I/O	
NAND Flash			
NAND_ALE	T1	O	Address latch enable, indicates the type of bus cycle. Unused NAND Flash pins can be left open.
NAND_CLE	U2	O	Command latch enable
NAND_CS_0	U1	O	Chip select
NAND_DATA_IO_0	N3	I/O	I/O port for transferring address, command, and data to and from the device
NAND_DATA_IO_1	N2	I/O	
NAND_DATA_IO_2	N1	I/O	
NAND_DATA_IO_3	P2	I/O	
NAND_DATA_IO_4	P1	I/O	
NAND_DATA_IO_5	R3	I/O	
NAND_DATA_IO_6	R2	I/O	
NAND_DATA_IO_7	R1	I/O	

Table 2-5 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pin	Type	Description
NAND_RB_L	Y3	I	Ready/busy, indicates the target status
NAND_RE_L	V3	O	Read enable
NAND_WE_L	T2	O	Write enable
NAND_WP_L	T3	O	Write protect
USB			
USB1_DM	W2	IA/OA	USB1 D- signal; carries USB data to and from the USB 2.0 PHY
USB1_DP	W1	IA/OA	USB1 D+ signal; carries USB data to and from the USB 2.0 PHY
USB2_DM	V2	IA/OA	USB2 D- signal; carries USB data to and from the USB 2.0 PHY
USB2_DP	V1	IA/OA	USB2 D+ signal; carries USB data to and from the USB 2.0 PHY
RGMII Interface			
EMDC	R26	O	Management control interface clock
EMDIO	R27	I/OD	Management control interface data
ERX_CLK	T27	I	Receive clock, can be grounded if not used
ERXD0	T26	I	Receive data, can be grounded if not used
ERXD1	T25	I	
ERXD2	U27	I	
ERXD3	U26	I	
ERX_EN	R25	I	Receive enable, can be grounded if not used
ETX_CLK	V27	O	Transmit clock, can be left open if not used
ETXD0	V25	O	Transmit data, can be left open if not used
ETXD1	W27	O	
ETXD2	W26	O	
ETXD3	W25	O	
ETX_EN	V26	O	Transmit enable, can be left open if not used
SGMII Interface			
SGMII_SIN	AA26	I	Differential serial input
SGMII_SIP	AA27	I	
SGMII_SON	AB26	O	Differential serial output
SGMII_SOP	AB27	O	
Regulator Control			
CTRL_DDR_XPNP	AB25	OA	External PNP Control. Connect to the base of an external PNP: collector to VDD_DDR and emitter to VDD33.

Table 2-5 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pin	Type	Description
CTRL_XPNP_GPIO	AG25	OA	External PNP control. Connect to external PNP to complete a regulator to generate 2.62 V I/O.
Internal Switching Regulator			
SWREG_OUT	AE25, AE26, AE27, AF25, AF26, AF27, AG27	P	1.2 V switching regulator output
VDD33_LDO	AC26	P	3.3 V digital supply
VDD33_SWREG	AC25, AD25, AD26, AD27	P	3.3 V input to the internal switching regulator
VREG_SWREG_FB	AG26	I	Feedback to the internal switching regulator

Symbol	Pin	Description
Power		
AVDD12_PHY_0	C4	Analog 1.2 V supply
AVDD12_PHY_1	E25	
AVDD12_BIAS	E26	
AVDD12_IPDRF_0	E1	
AVDD12_IPDRF_1	A6	
AVDD12_IPDRF_2	A16	
AVDD12_LO	C14	
AVDD12_PLL	F25	
AVDD12_SYNTH	B12	
AVDD12_SYNTHD	B14	
AVDD33_DPLLS	AE8	Analog I/O, LDO reg and SWREG 3.3 V supplies
AVDD33_IPDRF_0	B1	
AVDD33_IPDRF_1	B10	
AVDD33_IPDRF_2	B20	
AVDD33_PLL	B26	
AVDD33_SYNTH	C12	
AVDD33_USB2	V4	
AVDD33_XTAL	F27	
VDD33_GPIOREG	AG24	Digital 3.3 V supply
VDD25_GPIO	C24	Digital I/O 2.62 V supply
VDD25	H25, K3, Y27	
DVDD12	J25, N4, P3, P4, P25, R4, AB3, AB4, AD9, AD10, AD14, AD15, AD16, AD22, AD23, AE9, AE14, AE23	Digital 1.2 V supply
DVDD12_USB1	W3	
DVDD12_USB1_PLL	W4	
VDD_DDR	AC3, AC4, AD3, AD5, AD6, AD12, AD13, AD18, AD19, AD20, AE5, AE6, AE12, AE13, AE19	Digital DDR1/DDR2 supply, 1.8 V or 2.6 V

Symbol	Pin	Description
VDD_SGMII	AA25	Voltage for SGMII interface
AVDD12_PCIE	K25, L25, M25, N25	PCIE 1.2 V analog supply
GND	A4, A12, A22, B3, B11, B17, B21, C3, C7, C11, C17, C20, C21, D3, F2, F3, F26, G1, G3, G4, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, K9, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, L3, L4, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, M19, N9, N10, N11, N12, N13, N14, N15, N16, N17, N18, N19, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, T19, U3, U4, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V19, U25, W11, W12, W13, W14, W15, W16, W17, W18, W19, Y25, Y26, AA3, AA4, AD4, AD7, AD11, AD17, AD21, AE3, AE7, AE11, AE17, AE21, AF24	Ground
NC	B2, C5, C15	No Connect

3 Functional Description

3.1 Functional Block Diagram

Figure 3-1 illustrates the QCA9558 functional block diagram.

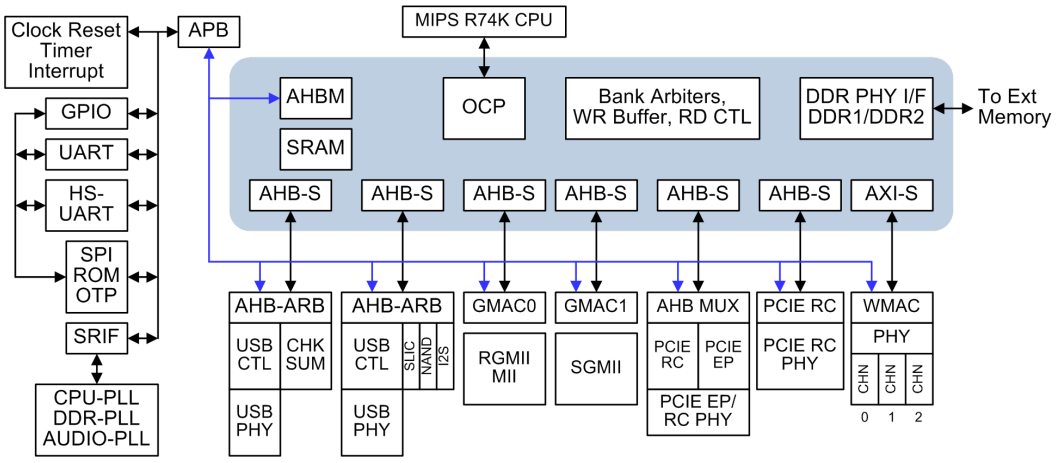


Figure 3-1 Functional Block Diagram

The QCA9558 is comprised of several internal functional blocks, as summarized in Table 3-1.

Table 3-1 Functional Blocks

Block	Description	
CPU Core and Memory Controller	MIPS R74 K supports 64 KByte I-Cache and 32 KByte D-Cache, targeted to operate at up to 720 MHz. ■ The memory controller is targeted to run at a frequency of 300 MHz (600 M transfers/sec) ■ Supports DDR self refresh mode for low power consumption ■ Asynchronous mode is also supported where the memory controller and CPU are required to work at the single clock ■ Clock dithering for DDR/CPU clocks to reduce EMI interference ■ DDR Clock dithering effected immediately after refresh cycle ■ Has internal ROM of 64 KBytes for booting ■ Has 32 KBytes of internal SRAM accessible by the CPU and by any other memory client; provides faster access to data than the external memory	
Clocking	Five internal PLLs: CPU, DDR, audio, WLAN PHY layer, and Ethernet SGMII SERDES PLLs to generate various internal clocks. The audio PLL is accurate enough to support up to 200 ppb frequency change. The QCA9558 has a separate audio clock adaptation module that can slowly change the clock assisted by CPU. The PLLs support a 40-MHz reference clock input. See PLL and Clock Control.	
DDR Memory	■ DDR1 x16/x32, DDR2 x16/x32. ■ Supports a 64-Mbyte DDR device in 16-bit Mode and a 128-Mbyte device in 32-bit mode See DDR Memory Controller.	
PCI Express Interface	Two PCIE 1.1 interfaces: ■ PCIE Root Complex interface ■ PCIE Root Complex based on bootstrap option See PCIE RC.	
USB	Two USB 2.0 ports: ■ USB 2.0 Host interface ■ USB 2.0 Host/Device port, configured using bootstrap option See USB 2.0 Interface.	
Gigabit Ethernet MAC	Two independent IEEE 802.3 complaint Gigabit (GB) Ethernet MACs. GMAC0 functions as a WAN port and GMAC1 can be connected to an external switch to provide a GB LAN solution. GMAC0 can connect through the MII/RGMII interfaces. GMAC1 connects through the SGMII interface. ■ Highly integrated CPU coupled hardware-based accelerator for NAT for both ingress and egress IPv4 traffic in the WAN port ■ Separate NAT accelerator for WAN ingress and egress; supports up to 256 entries per direction as well as hardware-based aging with separate AGE_LIMIT for TCP and UDP entries ■ Supports ACL accelerator for WAN ingress and egress traffic ACL is highly configurable and supports up to 64 entries per direction, with each entry supporting up to 5 match commands. Also supports a few global rules, and can be used in default accept mode or default reject mode. ■ Has on-the-fly checksum compute ability to cross check the TCP/UDP checksum field of an ingress IPv4, TCP/UDP packet supports 32 deep lookup engine with a key width of 48 bits and info field width of 8 bits ■ Supports a separate MDIO slave interface that can be used to download the boot code from an external host processor	
	GMAC0	Contains all the Ethernet WAN port specific accelerators
	GMAC1	Used to connect to the external switch
WLAN	3 chain / 3 stream (3x3) IEEE 802.11n WLAN MAC, PHY, and internal radio that can support 2 or 5 GHz operation. See WLAN Medium Access Control (MAC).	

Table 3-1 Functional Blocks (cont.)

Block	Description
UART and HS UART	Normal speed UART (16550 equivalent) at speeds up to 115.2 Kbps and high speed UART that can go up to 3 Mbps. Both UARTs share pins with GPIOs. See High-Speed UART Interface.
GPIO	Contains 24 highly configurable GPIO pins; any multiplexed signal can be routed to any GPIO as output, and any multiplexed input can be routed from any GPIO pin to the internal logic. See GPIO.
Audio	Support for I^2S/ SPDIF speaker OUT audio interface with sampling rate up to 96 KSps, with a sample size of up to 32-bits and I^2S Microphone IN interface with 16- and 32-bit sample size. Both I^2S master and slave modes are supported. The master clock can be internally generated from PLL and dividers or externally provided by the audio DAC circuits. See Audio Interface.
SLIC/PCM	A 8-bit, 64-slot SLIC interface with support for: ■ Both master and slave modes ■ Configurable number of active slots ■ Internal or external frame sync modes ■ Supports various frame sync widths: half-bit clock width, one-bit clock width, etc. ■ Delayed/non-delayed data modes ■ Both internal and external bit clock; the internal clock frequency is programmable ■ Both Rx and Tx on different (configurable) slots See SLIC.
Voltage Regulator and LDOs	Efficient 1.2 V switching regulator for providing analog and a digital core voltage of 1.2 V. LDOs are also provided to generate power to DDR1 (2.6 V), DDR2 (1.8 V) memory, analog domain, and IO domain (2.5 V).
NAND Flash Controller	■ ONFI2.0 Compliant with16-bit ECC capability ■ Supports SLC/MLC devices; for boot mode: SLC device only; as storage device: both MLC and SLC devices are supported ■ Provides Two Chip Select signals ■ Has DMA controller to read / write data into the DDR directly ■ No synchronous mode support available for NAND flash controller; only async mode supported See NAND Flash Controller.
Bootstrap Options	Several features of the QCA9558 can be configured or selected based on bootstrap pins whose state on power-on reset selects a given choice or configuration, for example boot from internal ROM or external flash. See Bootstrap Options.

3.2 Bootstrap Options

Table 3-2 details the QCA9558 bootstrap options. The GPIO pins have internal pull-downs and the DDR pins have internal pull-ups.

Table 3-2 Bootstrap Options

Bit	Name	Pin			Description	
17:16	BOOT_INTF	DDR_A_6	DDR_A_4	Interface	Selects the boot mode option. Valid only if BOOT_SELECT (bit [2]) is 0. By default boot from NAND Flash is selected.	
		0	0	USB		
		0	1	PCIE EP		
		1	0	Boot MDIO		
		1	1	NAND Flash		
15:13	RES	Reserved			Reserved (Reset 0x0)	
12	SOFTWARE_OPTION_2	SYS_RST_OUT_L			Can be used by software for any purpose	
11	SOFTWARE_OPTION_1	GPIO9			Can be used by software for any purpose	
10:8	RES	DDR_A_3, GPIO16, GPIO4			Reserved	
7	USB_MODE	GPIO13			0	Host mode (Default)
					1	Device mode
					To enable USB Device mode, GPIO13 should be tied to 1. Otherwise by default, it is in Host mode.	
6	RC_SELECT	GPIO12			0	Selects PCIE EP (Default)
					1	Selects PCIE RC
					To select PCIE RC, GPIO21 is tied to 1. Otherwise by default, PCIE EP is selected.	
5	JTAG_MODE	DDR_A_5			0	EJTAG
					1	JTAG (Default)
4	REF_CLK	GPIO15			Must be tied to 1 for 40 MHz REF clock operation.	
3	DDR_WIDTH	GPIO14			0	Selects DDR WIDTH 16 (Default)
					1	Selects DDR WIDTH 32
2	BOOT_SELECT	GPIO6			0	Selects boot from ROM (Default)
					1	Selects boot from SPI
					To enable boot from SPI, GPIO6 should be tied to 1. Otherwise boot from ROM is selected. The default signal available on this GPIO after reset is SPI_CLK	
1	RES	GPIO7			Reserved; the default signal available on this GPIO after reset is SPI_MOSI	
0	DDR_SELECT	GPIO10			0	Selects DDR 2 (Default)
					1	Selects DDR 1

3.3 Reset

Figure 3-2 shows the QCA9558 reset.

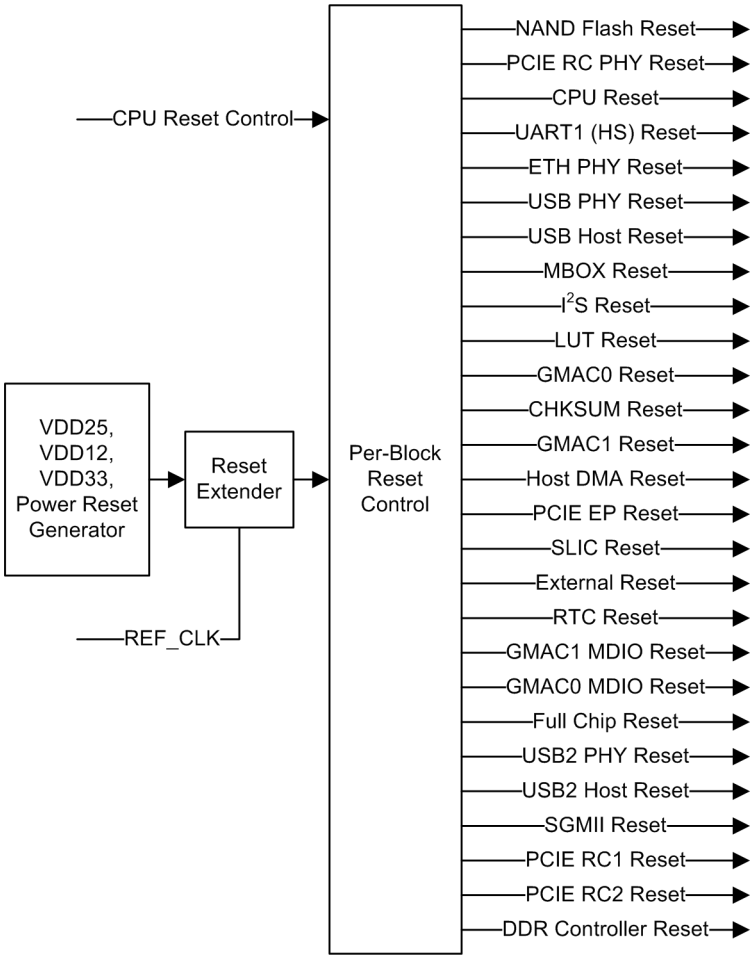


Figure 3-2 Reset

Each of the per- block resets can be issued by software by writing to the RST_RESET register. See Reset (RST_RESET) for the bit definitions for each per block reset.

3.4 PLL and Clock Control

3.4.1 Full Chip Clocking Structure

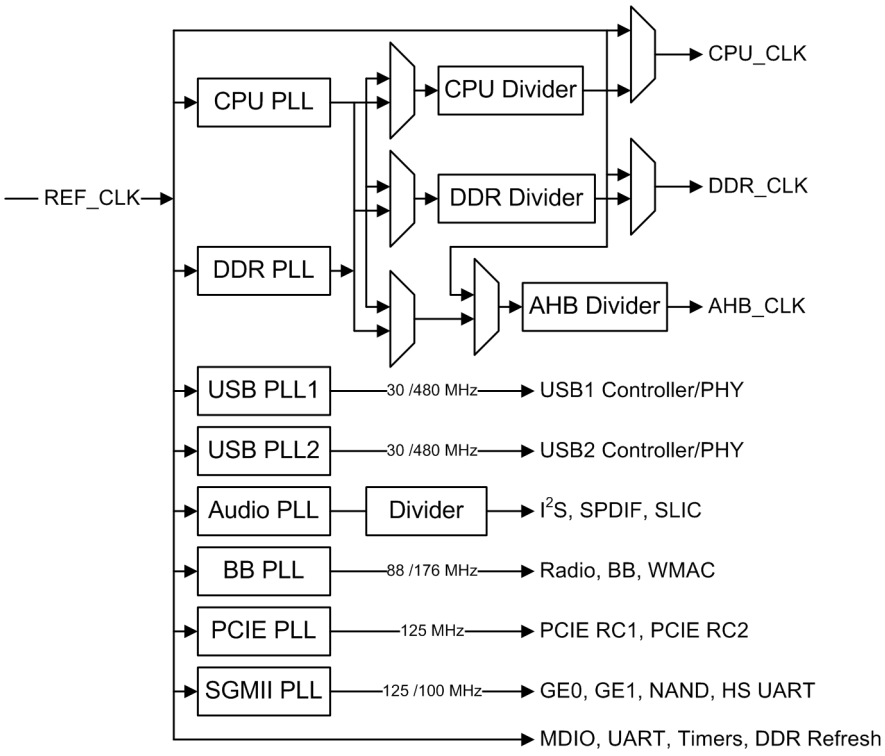


Figure 3-3 Full Chip Clocking Structure

The QCA9558 includes the audio, BB, CPU, DDR, and PCIE (digital) as well as the Ethernet and USB (analog) PLLs. See Table 3-3.

Table 3-3 QCA9558 PLLs

PLL	Description
Audio PLL	By default, the I^2S, SPDIF, and SLIC interfaces use this PLL.
BB PLL	By default, this PLL generates clocks for the radio, baseband, and WMAC.
CPU PLL	By default the source clock for the CPU_CLK, although it can also be derived from the DDR PLL.
DDR PLL	By default the source clock for DDR_CLK and AHB_CLK, though both can also be derived from the CPU PLL.
PCIE PLL	Generates the 100 MHz reference clock for the PCIE RC. The final output frequency of the PCIE PLL is similarly configurable, like the CPU and DDR PLLs, although a fixed 100 MHz clock is required. OUTDIV should be set to 3, and N=14 for 100 MHz.
Ethernet PLL	Generates the clock for all Ethernet interfaces, MAC, and so on, as well as to the high-speed UART and NAND Flash controller.
USB PLL	Generates the USB 30 MHz/480 MHz clock for USB controller.

3.4.2 CPU PLL

The CPU PLL is configured by the bit CPU_PLL_CONFIG in the registers CPU Phase Lock Loop Configuration (CPU_PLL_CONFIG) and CPU DDR Clock Control (CPU_DDR_CLOCK_CONTROL). The clock can vary slightly by changing the divider's FRAC. The dithering is controlled through the CPU PLL Dither Parameter (CPU_PLL_DITHER) register. Note that if DDR_CLK is derived from the CPU PLL, it is better to turn off dithering.

The clock switcher and dynamic clock divider guarantee any change in inputs to this module is glitch-free; thus input to this block can change. Make sure when modifying the select to the clock switcher module that both clock inputs are present as switching from one clock to another depends on both clocks. Figure 3-4 details the derivation of the CPU_CLK that clocks the MIPS processor.

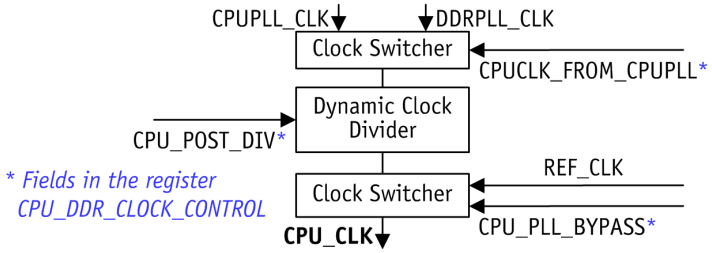


Figure 3-4 74Kc Processor CPU Clock

3.4.3 DDR PLL

The DDR PLL is configured with the registers DDR PLL Configuration (DDR_PLL_CONFIG) and CPU DDR Clock Control (CPU_DDR_CLOCK_CONTROL). The DDR PLL clock is dithered by DDR PLL Configuration (DDR_PLL_CONFIG); it is done immediately after issuing an auto refresh command to the DDR. Figure 3-5 shows the DDR_CLK and AHB_CLK select signal change to clock switching logic, which should be made only if both clock inputs are preset.

The FRAC part of the PLL is dynamic, but the INT part of the divider requires the PWD to go high and then low. Thus, changing the PLL clocks dynamically would be possible only by:

1. Asserting the PLL_BYPASS mode bit.
2. Asserting the PWD for that PLL.
3. Reconfiguring divider INT/FRAC values.
4. Deasserting the PWD for the PLL
5. Waiting for the clock to become stable by polling the UPDATE bit.
6. Removing the PLL_BYPASS bit for this PLL.

The CPU can do this procedure any time for CPU_CLK/AHB_CLK, which is useful to enter low power states leading to minimal chip power consumption. Another way to change the CPU/AHB/DDR_POST_DIV is to shift down to lower clock for these clocks. An optimal DDR and CPU frequency can be dynamically chosen, and the PLL reprogrammed for optimal power. However, make sure no DDR transaction is pending or in progress before changing DDR_CLK frequency.

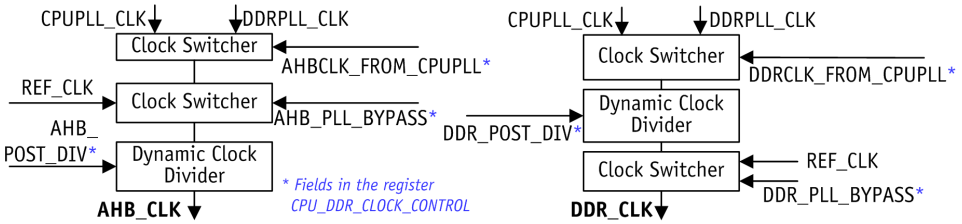


Figure 3-5 DDR_CLK and AHB_CLK

3.4.4 Audio PLL

The audio PLL is configured with the register Audio PLL Configuration (AUDIO_PLL_CONFIG). Hardware supports small variations in the PLL clock by dynamically changing the FRAC value using the Audio PLL Modulation Control (AUDIO_PLL_MODULATION) and Audio PLL Jitter Control (AUDIO_PLL_MOD_STEP) registers. See Audio PLL.

3.4.5 Ethernet PLL

The Ethernet PLL is controlled by the register Switch Clock Source Control (SWITCH_CLOCK_SPARE). When bit [7] of this register is set to 1, it selects the 100 MHz clock source from the Ethernet PLL to the high-speed UART. The Ethernet PLL generates a 50 MHz clock from the 100 MHz clock for the NAND Flash controller. Care must be taken to ensure that the clock to the NAND Flash controller is stable before taking it out of reset.

3.5 MIPS Processor

The QCA9558 integrates an embedded MIPS 74Kc processor. For more information, visit: http://www.mips.com/products/cores/32-64-bit-cores/mips32-74k/

Under Processor Cores-74K Family, refer to:

- MIPS32® 74Kc™ Processor Core Datasheet
- MIPS32® 74K® Processor Core Family Software User's Manual

Table 3-4 summarizes the configuration settings used by the QCA9558. Upon reset, the CPU puts out an address of 0xBFC00000 which is mapped to the flash address space. The QCA9558 processor supports a clock frequency of up to 560 MHz.

Table 3-4 Core Processor Configuration Settings

Setting	Description
Cache Size	The QCA9558 implements 64 KB 4-way set associative instruction cache and 32 KB four-way set associative data cache. It supports single cycle multiply-accumulate, MIPS32 and MIPS16 instruction sets, and non-blocking cached reads.
Endian	The QCA9558 implements big Endian addressing.
Block Addressing	The QCA9558 implements sequential ordering.

3.6 Address Map

Figure 3-6 shows the address space allocation.

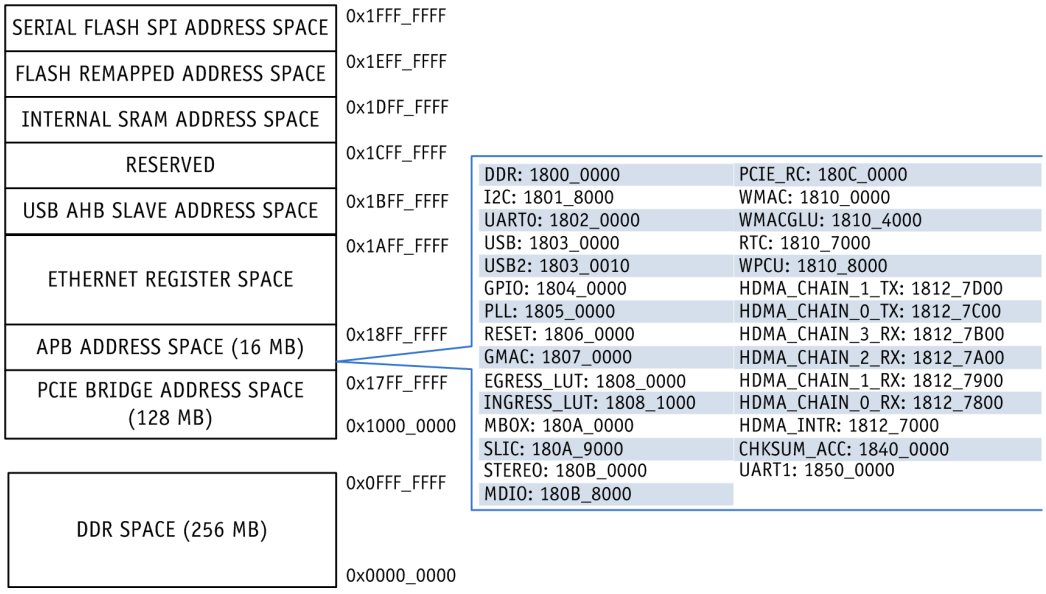


Figure 3-6 Address Space Allocation

3.7 DDR Memory Controller

The QCA9558 allows an external memory interface supporting 16- or 32-bit DDR1, or DDR2. The memory controller can enter DDR self refresh for low power modes. The DDR1 and DDR2 modes have small differences in read/write transactions. For a write transaction, DDR2 memory expects write data after a latency depending on CAS latency. DDR1 memory expects the first data immediately after the clock in which the write command is issued.

The controller uses the configurable parameter DDR2_TWL in the DDR2 Configuration (DDR2_CONFIG) register. The parameter is applicable for DDR1 and DDR2 modes: it should be set to one for DDR1 mode, and to (CAS – 1) * 2 – 1 for DDR2 mode.

On-Chip SRAM

The DDR controller provides 32 KBytes of on-chip SRAM for access to critical information. This SRAM is mapped at the base address 0x1D000000 and is accessible by CPU and all other memory clients. The SRAM can be used for critical control and data information exchange between the CPU and memory clients, when DDR memory is not accessible during low power modes and during initial boot from external hosts or NAND flash.

Enabling DDR2 Mode

Set the bit MODE_EN in DDR Controller Configuration (DDR_CTL_CONFIG) to zero, and the bit ENABLE_DDR2 in the DDR2 Configuration (DDR2_CONFIG) register to one.

- If HALF_WIDTH is set, x16 mode is selected and requires the VEC field in the register DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE) to be set to 0xFFFF.
- If HALF_WIDTH bit is not set, x32 mode is selected and requires VEC to be set to 0xFF.
- Set the bit SEL_18 in the register DDR2 Configuration (DDR2_CONFIG) to one.

3.7.1 DDR Configurations

Table 3-5 shows the DDR configurations. See the reference design for details.

Table 3-5 DDR Configurations when DDR_CONFIG2_SWAP_A26_A27 = 0

Device on Board	Total Memory (MBytes)	Mode (Bit)	DDR1	DDR2	Notes
256 Mbits x 16	32	16	Yes	Yes	For both DDR1 and DDR2, CPU address A25, A26, A27 unused
512 Mbits x 16	64	16	Yes	Yes	For both DDR1 and DDR2, CPU address A26, A27 unused
512 Mbits x 8 512 Mbits x 8	128	16	Yes	Yes	In DDR1, CPU address A26 is A11 of COL, A27 used In DDR2, A26 is A13 of ROW, A27 unused
1 Gbits x 16	128	16	Yes	Yes	In DDR1, CPU address A26 is A13 of ROW, A27 unused In DDR2, CPU address A13 is BA_2, A27 unused
1 Gbits x 8 1 Gbits x 8	256	16	No	No	DDR1 and DDR2 not supported
512 Mbits x 16 512 Mbits x 16	128	32	Yes	Yes	For both DDR1 and DDR2, CPU address A26 is A9 of COL; A27 unused
512 Mbits x 8 512 Mbits x 8 512 Mbits x 8 512 Mbits x 8	256	32	Yes	No	In DDR1, CPU address A26 is A9 of COL, A27 is A11 of COL; DDR2 not supported
1 Gbits x 16 1 Gbits x 16	256	32	No	No	DDR1 and DDR2 not supported

Table 3-6 DDR Configurations when DDR_CONFIG2_SWAP_A26_A27 = 1

Device on Board	Total Memory	Mode	DDR1	DDR2	Notes
256 Mbits x 16	32	16	Yes	Yes	For both DDR1 and DDR2, CPU address A25, A26, A27 unused
512 Mbits x 8 512 Mbits x 8	128 MBytes	16 Bit	No	Yes	DDR1 is not supported In DDR2, A26 is A13 of ROW; A27 unused
1 Gbits x 16	128 MBytes	16 Bit	Yes	Yes	In DDR1, CPU address A26 is A13 of ROW, A27 unused In DDR2, CPU address A26 is BA_2; A27 unused
1 Gbits x 8 1 Gbits x 8	256 MBytes	16 Bit	Yes	No	In DDR1, CPU address A26 is A13 of ROW, A27 is A11 of COL. DDR2 is not supported
512 Mbits x 16 512 Mbits x 16	128 MBytes	32 Bit	No	No	DDR1 and DDR2 not supported
512 Mbits x 8 512 Mbits x 8 512 Mbits x 8 512 Mbits x 8	256 MBytes	32 Bit	Yes	Yes	In DDR1, CPU address A27 is A9 of COL, A26 is A11 of COL In DDR2, CPU address A27 is A9 of COL, A26 is A13 of ROW
1 Gbits x 16 1 Gbits x 16	256 MBytes	32 Bit	Yes	Yes	In DDR1, CPU address A26 is A13 of ROW, A27 is A9 of COL In DDR2, CPU address A26 is BA_2 and A27 is A9 of COL

3.7.2 DDR Initialization Sequences

3.7.2.1 DDR1 Controller Initialization

NOTE It is extremely important to leave the reset values of many register fields untouched. Therefore software should always read a register and then modify only the required fields unless otherwise mentioned.

- Burst length (BL) should always be 8.
- Read Latency (RL) = Additive Latency (AL) + CAS Latency (CL)
- Write Latency (WL) = RL – 1
- tCK = CK_P CLK period

1. Program the register DDR Controller Configuration (DDR_CTL_CONFIG):

Bit	Bit Name	Setting	
1	HALF_WIDTH	0	For x32
		1	For x16

This step must to be done before memory initialization; the other steps do not have this dependency.

2. Set a value in DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE):
   - 0xFFFF for x16
   - 0x00FF for x32
3. If $F_{DDR\_CLK} < 2 * F_{AHB\_CLK}$ (frequency of DDR_CLK and AHB_CLK), program the DDR FSM wait control with 0x00000A24.
4. Set the timing parameters in DDR DRAM Configuration (DDR_CONFIG). These numbers typically use the values from the specification, but greater values can also be used. Numbers are in terms of the number of controller clocks.

Bit	Bit Name	Description
26:23	TMRD	Load mode register command cycle time.
22:17	TRFC	Auto-refresh command period
16:13	TRRD	Active bank a to active bank delay
12:9	TRP	Precharge command period
8:5	TRCD	Active to read or write delay
4:0	TRAS	Active to precharge time = max(tRAS_min, tRCD + CL). A greater value can be programmed if tRTP is not satisfied.

5. Set timing parameters in DDR DRAM Configuration 2 (DDR_CONFIG2). Bits [25:8] show minimum values; a greater value can also be programmed. Numbers are in terms of controller clock numbers.

Bit	Bit Name	Setting
29:26	GATE_OPEN_LATENCY	2 * CAS_LATENCY
25:21	TWTR	Write-to-read Command delay [1+BL/2 + tWTR/tCK] * 2 For example: tWTR=2 tCK; BL=8 TWTR=2 * [1+4+2]= 14
20:17	TRTP	Read-to-precharge command delay BL/2 + max(tRTP,2)-2
16:12	TRTW	Read-to-write command delay (CL + BL/2) * 2 For example: CL=3; BL=8; TRTW=7 * 2= 14
11:8	TWR	Write recovery time [BL/2+tWR/tCK] * 2 – 1 For example: BL=8; tWR= 15 ns; tCK=(1/200 MHz)= 5 ns TWR=[4+3] * 2-1= 13

6. Initialize DDR memory as shown in DDR Memory Initialization.
7. Set the register DDR Refresh Control and Configuration (DDR_REFRESH).
   E.g., for TREFI = 7.8 µs, set DDR_REFRESH[13:0] to 312 (REFCLK = 40 MHz).
8. Set the ENABLE bit.

3.7.2.2 DDR2 Controller Initialization

NOTE It is extremely important to leave the reset values of many register fields untouched. Therefore software should always read a register and then modify only the required fields unless otherwise mentioned.

- Burst length (BL) should always be 8.
- Read Latency (RL) = Additive Latency (AL) + CAS Latency (CL)
- Write Latency (WL) = RL – 1
- tCK = CK_P CLK period

1. Program the register DDR Controller Configuration (DDR_CTL_CONFIG):

Bit	Bit Name	Setting	
1	HALF_WIDTH	0	For x32
		1	For x16

This step must to be done before memory initialization; the other steps do not have this dependency.

2. Set a value in DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE):
   - 0xFFFF for x16
   - 0x00FF for x32
3. If $F_{DDR\_CLK} < 2 * F_{AHB\_CLK}$ (frequency of DDR_CLK and AHB_CLK), program the DDR FSM wait control with 0x00000A24.
4. Set the timing parameters in DDR DRAM Configuration (DDR_CONFIG). These numbers typically use the values from the specification, but greater values can also be used. Numbers are in terms of the number of controller clocks.

Bit	Bit Name	Description
26:23	TMRD	Load mode register command cycle time.
22:17	TRFC	Auto-refresh command period
16:13	TRRD	Active bank a to active bank delay
12:9	TRP	Precharge command period
8:5	TRCD	Active to read or write delay
4:0	TRAS	Active to precharge time = max(tRAS_min, tRCD + CL). A greater value can be programmed if tRTP is not satisfied.

5. Set timing parameters in DDR DRAM Configuration 2 (DDR_CONFIG2). Bits [25:8] show minimum values; a greater value can also be programmed. Numbers are in terms of controller clock numbers.

Bit	Bit Name	Setting
29:26	GATE_OPEN_LATENCY	2 * CAS_LATENCY

25:21	TWTR	[WL+BL/2 + max(2, tWTR/tCK)] * 2
		For example:
		tWTR = 7.5 ns;
		tCK = (1/200 MHz) = 5 ns;
		BL = 8; CL = 4; AL = 0
		WL = AL+CL-1 = 0+4-1 = 3
		TWTR = [3+4+max(2, 7.5/5)] * 2 = [3+4+2] * 2 = 18

20:17	TRTP	16-bit: [(AL+BL+max(tRTP/tCK,2))-2] * 2
		32-bit: [(AL+BL/2+max(tRTP/tCK,2))-2] * 2
		For example:
		tRTP = 7.5 ns;
		tCK= (1/200 MHz) = 5 ns;
		BL=8; AL=0
		For 32-bit:
		TRTP = [(0+4+2)-2] * 2 =8
		For 16-bit:
		TRTP = [(0+8+2)-2] * 2=16

16:12	TRTW	(RL+BL/2+1-WL) * 2 For example: CL = 4; BL = 8; AL = 0; WL=3; TRTW = [4+4+1-3]*2 = 12
11:8	TWR	(BL/2+tWR/tCK) * 2-1 For example: BL = 8; TWR = 15 ns; TCK = (1/200 MHz) = 5 ns TWR = [4+3] * 2-1 = 13

6. Initialize DDR memory as shown in DDR Memory Initialization.
7. Set the register DDR Refresh Control and Configuration (DDR_REFRESH)
   a. Store a refresh PERIOD value of 300 (REFCLK = 40 MHz).
   b. Set the ENABLE bit.

3.7.3 DDR Memory Initialization

These steps are performed as step 6 under DDR1 Controller Initialization, and as step 7 under DDR2 Controller Initialization.

1. To initialize DDR memory, when:
   - CKE is set low
   - Clocks are stable

   Allow a 200 µs delay then send an NOP/DESELECT command.
2. Set the CKE bit of the register DDR DRAM Configuration 2 (DDR_CONFIG2).
3. Issue a precharge all commands by setting the PREA bit of the register DDR Control (DDR_CONTROL) twice with a interval of 200 clock cycles between them.
4. Write to the register DDR Extended Mode (DDR_EXTENDED_MODE_REGISTER) to enable the DLL. Refer to the DDR memory device datasheet for bit-definitions of this register.
5. Issue an EMRS command to DDR by setting the EMRS bit in the register DDR Control (DDR_CONTROL) to enable the DLL.
6. Write to the register DDR Mode Value (DDR_MODE_REGISTER) with the value 0x1*N*3 (the reset value) to reset the DLL, where *N* indicates to set the four fields appropriately per the CAS value. Refer to the DDR memory device datasheet for bit-definitions of this register.
7. Issue an MRS command to DDR by setting the MRS bit of the register DDR Control (DDR_CONTROL).
8. Re-issue two precharge all commands again by redoing step 3.
9. After a 200 CLK second delay, issue two refresh commands by setting REF (bit [2]) of the register DDR Control (DDR_CONTROL) twice with a interval of 200 clock cycles between them.
10. Write to the register DDR Mode Value (DDR_MODE_REGISTER) with the value 0x0*N*3 to bring DLL out of reset, where *N* indicates to set the four fields appropriately per the CAS.
11. Issue an MRS command to DDR by setting the MRS bit of the register DDR Control (DDR_CONTROL).

3.7.4 CPU DDR Address Mapping

Table 3-7 shows the correspondence of the internal CPU address, the DDR interface address, and the physical memory address.

Table 3-7 CPU Address: DDR Interface Address Mapping

DDR Interface Address	Column Address[1]: 32-Bit Mode	Column Address: 16-Bit Mode	Row Address[2]: 16- or 32-Bit Mode	Bank Address: 16- or 32-Bit Mode
DDR_A_0	CPU_ADDR[2]	0	CPU_ADDR[11]	—
DDR_A_1	CPU_ADDR[3]	CPU_ADDR[2]	CPU_ADDR[12]	—
DDR_A_2	CPU_ADDR[4]	CPU_ADDR[3]	CPU_ADDR[13]	—
DDR_A_3	CPU_ADDR[5]	CPU_ADDR[4]	CPU_ADDR[14]	—
DDR_A_4	CPU_ADDR[6]	CPU_ADDR[5]	CPU_ADDR[15]	—
DDR_A_5	CPU_ADDR[7]	CPU_ADDR[6]	CPU_ADDR[16]	—
DDR_A_6	CPU_ADDR[8]	CPU_ADDR[7]	CPU_ADDR[17]	—
DDR_A_7	CPU_ADDR[23]	CPU_ADDR[8]	CPU_ADDR[18]	—
DDR_A_8	CPU_ADDR[25]	CPU_ADDR[23]	CPU_ADDR[19]	—
DDR_A_9	CPU_ADDR[26]	CPU_ADDR[25]	CPU_ADDR[20]	—
DDR_A_10	0	0	CPU_ADDR[21]	—
DDR_A_11	CPU_ADDR[27]	CPU_ADDR[26]	CPU_ADDR[22]	—
DDR_A_12	0	CPU_ADDR[27]	CPU_ADDR[24]	—
DDR_A_13 / DDR_BA_2	—	—	CPU_ADDR[26][3] [4]	CPU_ADDR[26][5]
DDR_BA_0	—	—	—	CPU_ADDR[9]
DDR_BA_1	—	—	—	CPU_ADDR[10]

1. Column address: DDR_A_0 through DDR_A_12, when the column is accessed.
2. Row address: DDR_A_0 through DDR_A_12, when the row is accessed.
3. CPU_ADDR[26] is DDR_A_13 in DDR1 1 GBit
4. CPU_ADDR[26] is DDR_BA_2 in DDR2 1 GBit
5. CPU_ADDR[26] and CPU_ADDR[27] can be swapped during column addressing, to support these on-board configurations: 2 x (DDR1 1 GBit x8), 2 x (DDR1/2 1 GBit x16)

3.7.5 Refresh

DDR memory must refresh periodically. The DDR controller has an automatic refresh command generation module that clocks with REF_CLK. Because DDR_CLK is dynamic, the auto REFRESH_PERIOD works on the fixed REF_CLK.

3.7.6 Self Refresh

The QCA9558 DDR controller supports a self refresh (SF) sequence; that is, it has hardware support to issue commands to place DDR memory into and to exit SF mode. The register DDR Self Refresh Control (DDR_SF_CTL) controls basic SF behavior.

If EN_SELF_REFRESH is set and no valid DDR transactions are in progress, the DDR controller initiates an SF enter sequence. If DDR clients have transactions in progress, the controller waits until no DDR activity is occurring.

If EN_AUTO_SF_EXIT is set, the controller initiates an exit SF sequence upon detecting a DDR request from any DDR client. If this bit is not set, DDR is in SF, a DDR new request is seen, the controller generates a miscellaneous DDR_ACTIVITY_IN_SF interrupt (see the register Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS)). Software can alternatively force the controller to exit SF by setting EN_SELF_REFRESH to 0.

The controller can also generate an interrupt to the CPU while entering SF, exiting SF, and while in SF if DDR activity is detected. Immediately after exiting SF, read commands should not be issued until TXSR is met and non-read commands should not be issued until TXSNR is met. These timing parameters can be programmed via the TXSNR and TXSR fields of the DDR_SF_CTL registers. Note that these are in terms of DDR_CLK and not REF_CLK.

While in SF, DDR_CK_P and DDR_CK_N clocks can be gated, optionally using the EN_SF_CLK_GATING bit.

3.8 PCIE EP

The QCA9558 acts like a client device to an external host via the PCIE EP interface. A descriptor-based DMA engine enables seamless transfer of packet between the external host and on-chip memory. The DMA engine consists of two parts: one handles DMA data transfer between external memory and the DMA buffer (as controlled by the external host through registers), and another handles data transfer between the DMA buffer and on-chip memory (as controlled by the on-chip processor through the local AHB/APB interface). The external host cannot access the internal registers directly, and the on-chip processor cannot access the external hosts resources directly. All information must be transferred as a stream of packets through the DMA engine. See Figure 3-7.

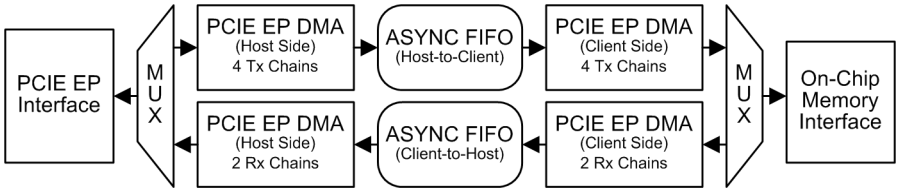


Figure 3-7 PCIE EP

3.8.1 PCIE EP DMA Interface

The PCIE EP DMA is packet-based transfer from the external host to and from on-chip memory. The external host allocates descriptors and buffers and programs the DMA engine with the descriptor start address and a start command. For data transfers from the external host (host) to on-chip memory (client), the DMA engine performs a memory read transaction through the PCIE EP interface. The received data is stored in the DMA buffer (host FIFO). When the data in the host FIFO exceeds a threshold, it triggers a signal to the client DMA to pick up data and forward it to the on-chip memory. The on-chip processor sets up the required client-side descriptors and buffers.

Similarly for data transfers from the client to the external host, the local processor sets up the client side DMA with required data transfer information. The DMA engine loads data into the DMA buffer (client FIFO). Based on a threshold, a memory write transaction is performed via the PCIE EP interface to external memory.

The required descriptors and host-side buffers are set up by the external host. Host and client transactions are simultaneous; they have priority logic to and from the channels. The DMA host side has four Tx channels (0, 1, 2, 3) and two Rx channels (0, 1). The client side of the DMA thus has four Rx channels (0, 1, 2, 3) and two Tx channels (0, 1). The capability to specify priority for any of these Tx and Rx DMA channels exists on the DMA host side.

3.8.2 PCIE EP Descriptor Format

Table 3-8 shows the AHB downstream DMA (host data to device memory).

Table 3-8 AHB Downstream DMA

	Byte 3	Byte 2	Byte 1	Byte 0
DES0	CONTROL		STATUS	
DES1	TOTALLEN		DATASIZE	
DES2	RES	LASTADDR		
DES3	RES	DATAADDR		
DES4	RES	NEXTADDR		

Table 3-9 DES0

Bit	Bit Name	Description	
31	AGG	Aggregation	
30	TAG	Tag for aggregation group	
29:26	RES	Reserved	
25	FS	First segment of a packet; Set by software to indicate this is the first descriptor for the packet	
24	LS	Last segment of a packet: ■ For memory-to-DMA controller transfers (host and client-side Tx): Set by software to indicate this is the last descriptor in the current packet. ■ For DMA controller-to-memory transfers (host and client-side Rx) Updated by the DMA controller to indicate this is the last descriptor for the current packet.	
23:17	RES	Reserved; Write zeroes to this field	
16	RETRY	Only valid for WLAN Tx DMA; write with 0 by AHB upload/download DMA	
		0	Tx Complete
		1	Retry fail
15:6	RES	Reserved; Write zeroes to this field	
5	RENC	Encrypted WLAN Rx; write with 0 by AHB upload/download DMA	
4	RAG	WLAN Rx receive aggregate frame; write with 0 using the AHB upload/download DMA	
3	RFA	First aggregation; write with 0 using the AHB upload/download DMA	
2	RLA	Last aggregation write with 0 using the AHB upload/download DMA	
1:0	OWN	Software set the OWN bits to tell the DMA controller that the descriptors belong to it. After the data transfer, the DMA controller changes the OWN bits to another DMA controller.	
		00	Descriptor is owned by the software
		01	Descriptor is owned by the DMA controller
		11:10	Reserved

Table 3-10 DES1

Bit	Bit Name	Description
31:16	TOTALLEN	Total length of buffer chains (in Bytes) of this packet.
15:0	DATASIZE	Data buffer size (in Bytes). ■ Set by Software to indicate the buffer size of the current descriptor. ■ For DMA controller-to-memory transfers (host and client-side Rx) The last descriptor is updated by DMA controller at the end of packet reception with the actual length of that last buffer

Table 3-11 DES2

Bit	Bit Name	Description
31:24	RES	Reserved
23:0	LASTADDR	The address of the last descriptor in the current packet. For DMA controller-to-memory transfers (host and client-side Rx): Updated in the first descriptor of the packet after the data transfer is complete.

Table 3-12 DES3

Bit	Bit Name	Description
31:24	RES	Reserved
23:0	DATAADDR	The address of the data buffer. Set by software to indicate the start of the data buffer (source or destination) for packet data.

Table 3-13 DES4

Bit	Bit Name	Description
31:24	RES	Reserved
23:0	NEXTADDR	The address of the next descriptor.

3.9 PCIE RC

The QCA9558 has two PCIE root complexes (RCs), each supporting a single-lane PCIE link at 2.5 GBps. The RC core implements the PCIE protocol layers: transaction, data link, and physical.

The PCIE PHY module resides outside of the RC core, interfacing through the PIPE, which is the standard interface between the PHY and the RC core. The PHY is split across the PIPE so MAC functionality is in the RC core and PHY functionality is implemented in the PIPE-compliant PHY external to the RC.

It has a sideband interface referred to as data bus interface (DBI) controlled by the CPU via APB, which programs the RC core configuration space. The DBI delivers a read/write request from application logic to the internal registers of the core. The RC core configuration space contains these register maps:

- PCI 3.0 compatible configuration space header
- PCI capabilities structures
  (starts at offset 0x40)
- PCIE extended configuration space
  (starts at offset 0x100)
- Port logic (vendor-specific registers)
  (starts at offset 0x700)

The CPU controls configuration and memory requests to the external EP through the AHB. The configuration and memory accesses to the two PCIE RC interfaces are mapped to the CPU AHB address space:

	Memory Slave	Configuration Slave
PCIE RC0	0x1000_0000 to 0x11FF_FFFF	0x1400_0000 to 0x15FF_FFFF
PCIE RC1	0x1200_0000 to 0x13FF_FFFF	0x1600_0000 to 0x17FF_FFFF

See Figure 3-8.

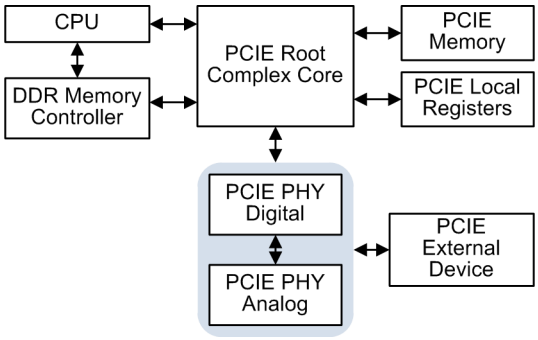


Figure 3-8 PCIE RC

3.9.1 Power Management

The PCIE RC supports L0s and L1 active state power management space. L0s is the low power standby state with lower entry/exit latencies. L1 saves more power, but with increased entry and exit latencies.

The PCIE RC includes the capacity to shut off the reference clocks going to the endpoint and powering down the RC PCIE PLL in L1 mode.

3.9.2 Interrupts

PCIE RC supports legacy INTx interrupts generated through PCIE message transactions. The application monitors the assertion and de-assertion messages for inbound INTx legacy interrupts (from the downstream component). It also supports MSI-based interrupt signalling through posted memory write transfers from EP (only one of INTx or MSI can be enabled at any time).

3.9.3 Error Reporting Capability and Status Checking

PCIE RC support advanced error reporting (AER) and has the ability to capture correctable and uncorrectable (fatal and non-fatal) errors in transmit and receive. The provision to capture these error messages as interrupts also exists.

3.9.4 Byte-Swap Option

The PCIE RC AHB interface is configured as big-Endian. Depending on whether data is to be sent to the endpoint in little- or big-Endian format, PCIE RC can add a register-configurable byte-swap in slave data going into the PCIE core. A swap option is also available on the master interface (DMA path).

3.9.5 Request Sizes and Payloads

The PCIE RC supports:

- The maximum number of outstanding incoming non-posted requests is 12
- The maximum payload size is 256
- The maximum read request size is 256
- The burst size for master requests is 64 bytes (INCR)

3.10 SLIC

3.10.1 Overview

The QCA9558 provides a single, 4-wired, multi-channel PCM digital highway for connecting to a SLIC-based VOIP interface circuit. The SLIC interface is compatible with a standard PCM interface based on T1 (24 channels at 1.544 MHz) or E1 (32 channels at 2.048 MHz).

Trunk interfaces are suitable for VOIP applications. Other non-standard channel numbers up to 64 channels and a bit rate up to 8.092 MHz are supported via register configuration. In a VOIP application, the QCA9558 SLIC controller can be configured as a bridge between the PCM voice interface and the LAN/WAN/WLAN IP packet interface. The SLIC controller can transmit/receive on 1, 2, or multiple-time multiplexed 8-bit voice channels on the PCM trunk. Up to 64 channels are supported through the bit mask channel enable registers. All Tx/Rx operations are 8-bit PCM samples transferred using descriptor-based DMA controllers (mailboxes) between the system memory and the trunk interface. Each direction (Tx and Rx) has one mailbox DMA controller.

A configurable number of 8-bit slots can be between two consecutive frame syncs, up to 64 possible slots. Software can enable any slot (they do not need to be contiguous). The SLIC Tx and Rx modules push DDR data from the buffer indicated by the descriptor to the SLIC byte by byte. To support multiple independent calls, software packages the data from each source on to a single buffer in DDR. In master mode, the bit clock can be derived from the audio PLL through a configurable divider (bits [7:0] of the SLIC Clock Control (SLIC_CLOCK_CONTROL) register).

In a configuration requiring both I^{2}S and SLIC functions, it is not recommended to use the audio PLL for the SLIC interface; the SLIC should derive its bit clock from the 125 MHz Ethernet clock, 100 MHz PCIE clock, or REFCLK. In slave mode it comes through the GPIO. GPIO must be programmed with the SLIC signals (Bit Clk, Frame Sync, DI, DO) through the GPIO module.

Major features include:

- Programmable number of SLIC_SLOTs
- Enabling multiple slots
- Master or slave programming
- Short/long frame sync
- Delayed or non-delayed data operation mode
- SLIC enable/disable
- Programmable divider clock: Option to choose the audio PLL, Ethernet CLK (125 MHz), PCIE CLK (100), or REF CLK as divider clock source.
- 8-bits/slot (maximum of 64 slots); having 16 bits/slot requires enabling two consecutive slots. In 16-bit mode, the total number of slots available becomes 32.
- Separate interrupts for Rx and Tx DMA completion
- SLIC interrupt for unexpected frame sync in slave mode
- Bit swap across byte boundary
- Configurable options to send data at various edges after frame sync
- Variations in frame sync duration
  - Frame sync can last for a half clock duration of BIT_CLK
  - Frame sync can stay for more than one clock duration of BIT_CLK (the number of clocks for which frame sync should be high is configurable)

Figure 3-9 shows the SLIC block diagram.

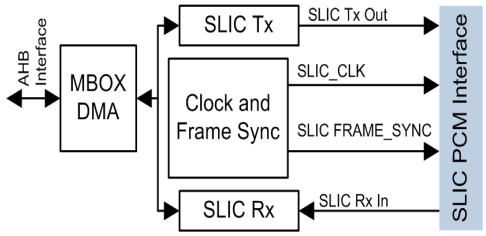


Figure 3-9 SLIC Block Diagram

3.10.2 SLIC Interface

SLIC along with I^{2}S makes use of the multi-channel versatile mailbox DMA controller for all data transfers to and from system memory. SLIC SLOT0 and SLOT1 use MBOX channels 1 and 3, respectively. See Mailbox (DMA Controller) for more information.

3.11 Segmentation/Desgementation/Checksum Accelerator

Three different operation modes are available:

- Compute checksum of a data buffer.
  Set the OFFTY field to 0x0.

  In this case, the CPU sets up one descriptor per data buffer in the Tx direction. Hardware computes the checksum for each data buffer individually, and updates the checksum in DWord1 of the descriptor.

  After processing a data buffer, hardware sets PktV bit in DWord1, showing hardware completed processing this data buffer.

- Read in a chunk of buffer and split it to many smaller chunks, computing the checksum for each smaller chunk.

  In this case the Tx descriptor has one descriptor, and receive would be a chain of descriptors one for each smaller chunk. It is the responsibility of the software to set the buffer sizes correctly for all the smaller chunks as well as the big source data chunk so that the sizes of all the smaller ones match the size of the big source chunk.

  For each smaller buffer, hardware computes the checksum and updates the STATUS field. Because hardware does not update the SOF/EOF fields, it is recommended that software queue desegmentation one chunk at a time. The OFFTY field is set to 0x001.

- Read in many small chunks of data, combine them into one, and compute the checksum of this big chunk.

  Each buffer chunk is associated with a descriptor. If many small pieces are present, the first has the SOF bit in its descriptor set and the last has the EOF bit set in its descriptor. Hardware reads all data from these data buffers and updates checksum in the Rx descriptor. It also writes back the data buffer size in the third word.

Table 3-14 shows the Tx descriptor structure.

Table 3-14 Tx Descriptor Structure

DWord	Bits	Name	Description
0	31:0	BUFFER_ ADDR	Indicates the data buffer start address, supports non-word aligned addresses. The DMA can perform byte-write transactions, which help in segmentation/desegmentation on buffers on any address and any length.
1 (CONTROL)	31	PKTV	Packet void; Software must set PktV to 0, and after the descriptor is processed and checksum is updated, hardware sets it back to 1.
	30:28	OFFTY	Offload type
			0 Compute checksum only. Bytes are not pushed to receive side for segmentation or desegmentation.
			1 Compute checksum and fill up Rx buffers and compute checksum on the Rx side with segmentation or desegmentation.
	27	EOF	End of frame. The frame ends with this buffer. If the frame spans multiple descriptors, the first descriptor should have StartOfFrame set and last descriptor should have EndOfFrame set.
	26	SOF	Start of frame. Should be set on the first descriptor, when more that one buffers are liked though descriptor link pointers.
	25	PKTINTREN	If set, enables generation of interrupt after the descriptor is being processed.
	24:19	RES	Reserved
	18:0	PKTSIZE	Tx buffer size (initialized by the CPU) Supports up to 512 KByte buffers.
1 (STATUS)	31	PKTV	Packet void; After descriptor is processed and checksum is updated, hardware will set this bit to 1.
	30	PKTINTREN	If set, indicates generation of interrupt for the processed descriptor.
	29:16	RES	Reserved
	15:0	CHKSUM	Checksum (written back by hardware); 16-bit checksum computed on bytes in the buffer associated with the descriptor.
2	31:0	NEXTDESC	Next descriptor address; The descriptor chain is traversed until it reaches one with its PktV bit set to 1. If this descriptor is the last descriptor in the chain, point the next descriptor address to the first descriptor in the chain, which will already have PktV set by hardware.
3 (STATUS ONLY)	31:19	RES	Reserved
	18:0	HWPKTSIZE	Hardware Tx packet size; Remains the same as the one in control descriptor.

Table 3-15 shows the Rx descriptor structure.

Table 3-15 Rx Descriptor Structure

DWord	Bits	Name	Description
0	31:0	BUFFER_ ADDR	Buffer address; Indicates the data buffer address. Non-word aligned addresses are supported. The DMA can perform byte-write transactions, which help in segmentation and desegmentation on buffers on any address and on any length.
1 (CONTROL)	31	PKTV	Packet void; Software must set PktV to 0, and after the descriptor is processed and checksum is updated, hardware sets it back to 1.
	30:26	RES	Reserved
	25	PKTINTREN	If set, enables generation of interrupt after the descriptor is being processed.
	24:19	RES	Reserved
	18:0	PKTSIZE	Rx buffer size (initialized by the CPU) Supports up to 512 KByte buffers.
1 (STATUS)	31	PKTV	Packet void
	30	PKTINTREN	If set, indicates generation of interrupt for the processed descriptor.
	29:16	RES	Reserved
	15:0	CHKSUM	Checksum (written back by hardware); 16-bit checksum computed on bytes in the buffer associated with the descriptor.
2	31:0	NEXTDESC	Next descriptor address; The descriptor chain is traversed until it reaches one with its PktV bit set to 1. If this descriptor is the last descriptor in the chain, point the next descriptor address to the first descriptor in the chain, which will already have PktV set by hardware.
3 (STATUS ONLY)	31:19	RES	Reserved
	18:0	PKTLEN	Number of bytes in receive buffer

3.12 GPIO

The GPIO module is structured in such a way that any signal listed in GPIO Output Select Values (Table 3-17) and GPIO Input Select Values (Table 3-18) can be available through any GPIO pin, except for the JTAG signals, which cannot be programmed on any other GPIO pins.

GPIO pins can be configured as input/output by programming the appropriate bits in the GPIO function registers. On reset, GPIO[17:0] are configured with certain default signals, as shown in Table 3-16. Some of these GPIOs will get configured based on the Boot selection in the Boot ROM Mode.

NOTE JTAG pins must use GPIO[3:0]. Apart from JTAG, all signals can use any GPIO and can use GPIO[3:0] by setting the DISABLE_JTAG bit to 1 in the GPIO_OUT_FUNCTIONx register.

Table 3-16 Default GPIO Signals

GPIO	Signal	Direction	During Reset	After Reset	Description
GPIO0	TCK	Input	Input	Input	JTAG Clock
GPIO1	TDI	Input	Input	Input	JTAG data input
GPIO2	TDO	Output	0	0	JTAG data output
GPIO3	TMS	Input	Input	Input	JTAG test mode
GPIO4	CLK_OBS5	Output	Input	Output	Observation Clock - CPU_CLK/4
GPIO5	SPI_CS	Output	1	1	SPI chip select (Default = 1)
GPIO6	SPI_CLK	Output	0	0	SPI clock (Default = 0)
GPIO7	SPI_MOSI	Output	0	0	SPI data output (Default = 0)
GPIO8	SPI_MISO	Input	Input	Input	SPI data input
GPIO9	Software Configured	Input	Input	Input	Software configurable
GPIO10	Software Configured	Input	Input	Input	Software configurable
GPIO11	Software Configured	Input	Input	Input	Software configurable
GPIO12	Software Configured	Input	Input	Input	Software configurable
GPIO13	Software Configured	Input	Input	Input	Software configurable
GPIO14	Software Configured	Input	Input	Input	Software configurable
GPIO15	Software Configured	Input	Input	Input	Software configurable
GPIO16	Software Configured	Input	Input	Input	Software configurable
GPIO17	Software Configured	Input	Input	Input	Software configurable
GPIO18	Software Configured	Input	Input	Input	Software configurable
GPIO19	Software Configured	Input	Input	Input	Software configurable
GPIO20	Software Configured	Input	Input	Input	Software configurable
GPIO21	Software Configured	Input	Input	Input	Software configurable
GPIO22	Software Configured	Input	Input	Input	Software configurable
GPIO23	Software Configured	Input	Input	Input	Software configurable

3.12.1 GPIO Output

GPIO is structured to output one of 128 signal through any GPIO pin. See Figure 3-10.

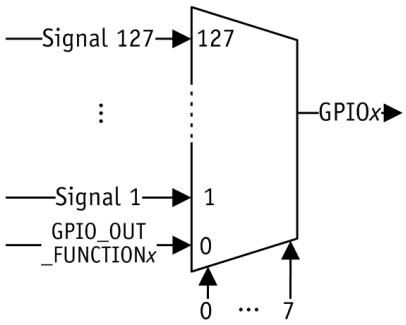


Figure 3-10 GPIO is Structured to Output 1 of 128 Signal Through Any GPIO

Each GPIO output is structured as 128:1 MUX. The MUX select is an 8-bit register that can be programmed with the values 0-127 to allow that particular input signal through the GPIO pin, as shown in Table 3-17. The signal gets the source from the GPIO_OUT_FUNCTIONx registers. Each 32-bit register has select values for four GPIO pins (8 bits each).

Register	Selects values for these GPIO pins
GPIO Function 0 (GPIO_OUT_FUNCTION0)	GPIO pins 0, 1, 2, 3
GPIO Function 1 (GPIO_OUT_FUNCTION1)	GPIO pins 4, 5, 6, 7
GPIO Function 2 (GPIO_OUT_FUNCTION2)	GPIO pins 8, 9, 10, 11
GPIO Function 3 (GPIO_OUT_FUNCTION3)	GPIO pins 12, 13, 14, 15
GPIO Function 4 (GPIO_OUT_FUNCTION4)	GPIO pins 16, 17, 18, 19
GPIO Function 5 (GPIO_OUT_FUNCTION5)	GPIO pins 20, 21, 22, 23

If set to zero, the CPU directly controls the GPIO through the GPIO Per Bit Set (GPIO_SET)/GPIO Per Bit Clear (GPIO_CLEAR) registers, or observes via the GPIO Input Value (GPIO_IN) register.

To output the signal through the GPIO pin, use this register programming:

1. If using a non-JTAG signal on GPIO[3:0], write the bit DISABLE_JTAG of the GPIO_OUT_FUNCTIONx register to 1.
2. Set the corresponding GPIO bit in GPIO Output Enable (GPIO_OE) to 0.
3. Write the particular GPIO field in GPIO_OUT_FUNCTIONx with the corresponding output signal value from Table 3-17.

For example, to drive the SPI_CLK signal through the GPIO4 pin:

1. Set bit[4] of GPIO Output Enable (GPIO_OE) register to 0.
2. Set the 8-bit field ENABLE_GPIO4 (bits [7:0]) of the GPIO Function 1 (GPIO_OUT_FUNCTION1) register to 10.

Table 3-17 GPIO Output Select Values

MUX Select Value	Signal Name	Description
1	MII_EXT_MDI	Boot MDIO MDI signal (MDIO slave for bootup)
2	RES	Reserved
3	SLIC_DATA_OUT	SLIC data out
4	SLIC_PCM_FS	SLIC frame sync
5	SLIC_PCM_CLK	SLIC reference clock
7:6	RES	Reserved
8	SPI_CLK	SPI Clock
9	SPI_CS_0	SPI chip select 0
10	SPI_CS_1	SPI chip select 1
11	SPI_CS_2	SPI chip select 2
12	SPI_MOSI	SPI data output
13	I2S_CLK	I^2S reference clock
14	I2S_WS	I^2S word select for stereo
15	I2S_SD	I^2S serial audio data
16	I2S_MCK	I^2S master clock
17	SPDIF_OUT	SPDIF data output
18	UART1_TD	High-speed UART1 transmit data
19	UART1_RTS	High-speed UART1 request to send output
20	UART1_RD	High-speed UART1 receive data
21	UART1_CTS	High-speed UART1 clear to send input
22	UART0_SOUT	Low-speed UART0 serial data out
23	SPDIF_OUT	SPDIF data output
24	LED_SGMII_SPEED0	SGMII activity LEDs
25	LED_SGMII_SPEED1	
26	LED_SGMII_DUPLEX	
27	LED_SGMII_LINK_UP	
28	LED_SGMII_SPEED0_INVERT	SGMII activity LEDs
29	LED_SGMII_SPEED1_INVERT	
30	LED_SGMII_DUPLEX_INVERT	
31	LED_SGMII_LINK_UP_INVERT	
32	GE1_MII_MDO	GE1 MII media data out
33	GE1_MII_MDC	GE1 MII media data clock
37:34	RES	Reserved

Table 3-17 GPIO Output Select Values

38	SWCOM2	SWCOM bit[2]
39	SWCOM3	SWCOM bit[3]
40	MAC GPIO	Smart antenna control bit [2]
41	MAC GPIO	Smart antenna control bit [3]
42	ATT_LED	External LNA control for chain 0
43	PWR_LED	External LNA control for chain 1
44	TX_FRAME	MAC Tx frame (indicates the MAC is transmitting)
45	RX_CLEAR_EXTERNAL	WLAN active
46	LED_NETWORK_EN	MAC network enable
47	LED_POWER_EN	MAC power LED
67:48	RES	Reserved
68	WMAC_GLUE_WOW	MAC detected a WOW packet
69	RES	Reserved
70	RX_CLEAR_EXTENSION	Medium clear for Rx
71	SHIFT_STROBE	For Smart Antenna
72	SHIFT_DATA	For Smart Antenna
73	CP_NAND_CS1	NAND chip select 1
74	USB_SUSPEND	USB suspend
75	ETH_TX_ERR	MII transmit error
76	DDR_DQ_OE	DDR data output enable
77	CLKREQ_N_EP	Clock request endpoint
78	CLKREQ_N_RC	Clock request root complex
79	CLK_OBS0	Clock observation See the GPIO function registers (GPIO Function 0 (GPIO_OUT_FUNCTION0) through GPIO Function 5 (GPIO_OUT_FUNCTION5)) for clock signals observable through GPIO pins
80	CLK_OBS1	
81	CLK_OBS2	
82	CLK_OBS3	
83	CLK_OBS4	
84	CLK_OBS5	
127:85	RES	Reserved

3.12.2 GPIO Input

GPIO inputs are structured so that any signal listed in Table 3-18 can source from any GPIO pin. See Figure 3-11.

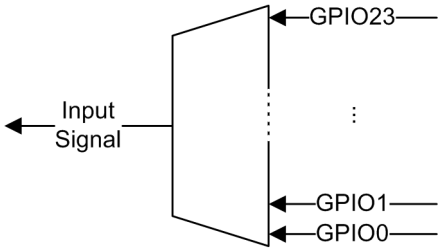


Figure 3-11 Any Signal Can Receive Input From Any GPIO

Each signal can receive its input from GPIO[23:0]. Each signal has an 8-bit register that can be programmed with the GPIO values 0-23; the signal gets its input for the corresponding GPIO pin programmed in the GPIO_IN_ENABLEx registers (GPIO In Signals 0 (GPIO_IN_ENABLE0) through GPIO In Signals 9 (GPIO_IN_ENABLE9)). See Table 3-18.

To route the GPIO input to a particular signal, use this register programming:

1. If using a non-JTAG signal on GPIO[3:0], write the bit DISABLE_JTAG of the GPIO Function (GPIO_FUNCTION) register to 1.
2. Set the corresponding GPIO bit in the GPIO Output Enable (GPIO_OE) register to 1.
3. Write the particular 8-bit GPIO field in the GPIO_IN_ENABLEx registers (GPIO In Signals 0 (GPIO_IN_ENABLE0) through GPIO In Signals 9 (GPIO_IN_ENABLE9)) with the corresponding output signal value from Table 3-17.

   If a value greater than 23 is written, this signal is assigned a default value of 0.

For example, to route the UART0_SIN signal through the GPIO9 signal:

1. Set bit [9] of the GPIO Output Enable (GPIO_OE) register to 1.
2. Set the UART0_SIN field (bits[15:8]) in the GPIO In Signals 0 (GPIO_IN_ENABLE0) register to 0x9.

Table 3-18 shows the GPIO input select values.

Table 3-18 GPIO Input Select Values

Signal Name	Description
UART_SIN	Low speed UART0 serial data in
SPI_MISO	SPI data input
I2S_MCLK	I^2S master clock
I2S_CLK	I^2S reference clock
I2S_MIC_SD	I^2S serial MIC in data
I2S_WS	I^2S word select for stereo
SLIC_MCLK	SLIC master clock
ETH_RX_CRS	MII carrier sense detect
ETH_RX_ERR	MII receive error
ETH_RX_COL	MII receive collision
GE1_MDI	MDI signal of GE1 MDIO
MII_EXT_MDC	External MDIO interface for boot up, management data I/O
MII_EXT_MDO	External MDIO interface for boot up, management data clock
I2C_DATA	I^2C data
I2C_CLK	I^2C reference clock
SLIC PCM FS	SLIC Frame sync
SLIC_DATA_IN	SLIC data input

3.13 Serial Flash SPI/ROM

The SPI controller supports two ways of programming the SPI device:

- The bit blasting method by which data, CLK, and the CS are programmed directly by CPU bit in the controller register SPI_IO_CNTRL_ADDR, which is shifted on to the interface signals.
- Direct programming of the data and the number of bits to shift. The controller takes care of shifting the specified number of bits.

The SPI controller has a dedicated chip select available to an external flash for booting, as well as two more configurable chip selects.

3.13.1 SPI Operations

Before performing any SPI operation, the FUNCTION_SELECT and REMAP_DISABLE bits of the register SPI Controller GPIO Mode Select (FUNCTION_SELECT_ADDR) are set to 1. Any page program or erase operations on the SPI device must enable the write enable latch (WEL).

3.13.2 Write Enable

1. Program the register SPI Controller GPIO Mode Select (FUNCTION_SELECT_ADDR) with the WREN CMD value.
2. Program SPI_SHIFT_CNT_ADDR:

SHIFT_CNT	8	Number of WREN command bits
TENATE	1	After shifting 8-bit deassert chip select
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

3.13.3 Page Program

- Send a **write enable** command before any page program or erase operations.
- Use the **send** command:
  a. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) with the PP CMD value.
  b. Program SPI Content to Shift Out or In (SPI_SHIFT_CNT_ADDR):

SHIFT_CNT	8	Number of command bits
TENATE	0	Do not deassert CS; CMD is followed by address/data
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

- Send the address:
  a. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) with the address to be programmed.
  b. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR):

SHIFT_CNT	24	Number of address command bits
TENATE	0	Do not deassert CS; CMD is followed by address/data
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

- Send the data:
  a. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) with the data to be programmed.
  b. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR):

SHIFT_CNT	32	Number of data bits
TENATE	1	Deassert chip select after programming the data
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

The command and address can be programmed together in SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) in the order: {8'CMD, 24'ADDR}. The SHIFT_CNT field in SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) is set to 32.

3.13.4 Page Read

- Send command and address:
  a. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) with the **read** command and address.
  b. Program SPI Content to Shift Out or In (SPI_SHIFT_CNT_ADDR):

SHIFT_CNT	32	Number of command and address bits
TERMINATE	0	Keep chip select asserted until the data is read
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

- Read the data by programming SPI Content to Shift Out or In (SPI_SHIFT_CNT_ADDR):

SHIFT_CNT	32	Number of bits to be read
TERMINATE	1	Deassert the chip select after the data is read
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

3.14 MDIO Interface

The QCA9558 provides three MDIO interfaces: two MDIO master interfaces and one MDIO slave interface. Due to low number of pads and package pins, one master MDIO interface shares GPIO pins with other functional interfaces.

3.14.1 MDIO Master Interface

- MDIO master interface 0 (associated with RGMII/MII):
  This functionality is available along with RGMII /MII interface where QCA9558 will be the master on the MDIO interface.
- MDIO master interface 1 (associated with SGMII):
  This functionality is available along with the SGMII interface, where QCA9558 will be the master on the MDIO interface.

3.14.2 MDIO Slave Interface

The QCA9558 supports a MDIO Slave interface to allow an external MAC or Host CPU to communicate with the QCA9558 CPU. Typically, an external host processor can download code through this interface to boot the QCA9558 CPU.

A set of eight external registers (MDIO APB Registers (MDIO_REG)) can be accessed and updated by an external MDIO master. The CPU can poll the 8-bit MDIO Interrupt (MDIO_ISR) register (1-bit/MDIO_REG) to show which MDIO_REG register is updated. Typically an external host processor can download code through this MDIO slave interface to boot the CPU.

MDIO Slave PHY Addresses (MDIO_PHY_ADDR) is the PHY address register for MDIO slave. The QCA9558 MIPS 74K CPU must initialize this register with the intended PHY address before initiating any transfer. By default, this PHY address is 7.

3.15 High-Speed UART Interface

The QCA9558 supports a high speed Universal Asynchronous Receive and Transmit (UART) interface for connecting to high speed serial interface devices. This controller supports Tx and Rx speeds of up to 3 Mbps with RTS/CTS flow control. Data and control access is through a APB PIO interface. The UART supports a four-deep, byte-wide FIFO on Tx and Rx interfaces to improve throughput. The controller can be configured for either an RS232 DTE or for DCE equipment.

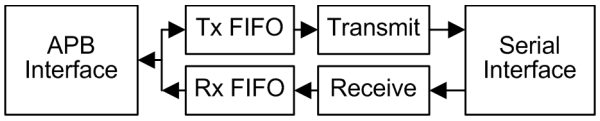


Figure 3-12 UART Block Diagram

The CPU can send and receive data through the UART using a set of control and data registers (see UART1 (High-Speed) Registers on page 431). A FIFO is provided on both the Tx and Rx sides, to synchronize with the remote equipment without loss of data.

The operating mode of the UART is set using the UART1 Configuration and Status (UART1_CS) register for DTE/DCE mode, as is flow control using RTS/CTS. The baud rate for transmit and receive can be set using UART1 Clock (UART1_CLOCK).

3.15.1 Transmit (Tx)

To send data on the serial interface, the CPU checks for Tx busy in the UART1_TX_BUSY bit in the UART1 (High-Speed) Registers. If Tx is idle, the CPU proceeds to write the bytes into the register UART1 Transmit and Rx FIFO Interface (UART1_DATA). The CPU can write data into the Tx FIFO (if enabled) as long as the bit TX_BUSY is reset (idle). The written bytes are sent over the UART0_SOUT pin. The UART1_TX_CSR bit must be set to enable the Tx operation with FIFO.

3.15.2 Receive (Rx)

Received data is available for reading out from the UART1_DATA register. Data availability is indicated by the UART1_RX_BUSY bit being set in the UART1 Configuration and Status (UART1_CS) register. Data can be read from the Rx FIFO (if enabled) as long as the bit RX_ BUSY is set. The UART1_RX_CSR bit must be set to enable the Rx operation with FIFO.

3.15.3 Low-Speed UART Interface

The QCA9558 contains a 16550 equivalent UART controller/port for debug/console monitoring. The UART pins are multiplexed with GPIO pins. GPIO Output describes the multiplexed GPIO options. The UART controller can be programmed through a set of control registers. The UART0 (Low-Speed) Registers defines the required registers and their descriptions for UART. The UART supports programmable baud rates and can support up to 115.2 KBps. This UART does not support hardware flow control.

3.16 USB 2.0 Interface

The USB controller supports a standard USB 2.0 host or device interface, configurable using bootstraps on power-up. In USB host mode, the QCA9558 can support the full number of devices/endpoints allowed in the USB 2.0 specification. It can be connected, either directly or through one or more hubs, at high-speed (480 Mbps) or full-speed (12 Mbps). Besides the standard endpoint 0 for control, the QCA9558 implements four bulk downstream endpoints, one bulk upstream endpoint, and one interrupt upstream endpoint. The USB core acts as a master on the internal AHB bus, maximizing data transfer speeds with the system DDR memory.

In both configurations (host or client) the USB supports low power suspend mode wherein the total power consumed is less than 10 mW. See Figure 3-13.

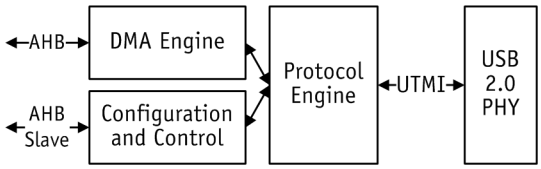


Figure 3-13 USB Interface

Table 3-19 describes the USB interface elements.

Table 3-19 USB Interface Elements

Name	Description
System Interface	The USB controller provides a AHB master interface for DMA transfer of descriptors and endpoint data between the System memory and the USB serial interface. QCA9558 CPU can control the USB controller operation through an AHB Slave interface. In Host Mode, the controller registers and data structures are compliant to Intel EHCI specifications. In Device Mode of operation the controller registers and data structures are implemented as extensions to EHCI programmers interface. QCA9558 software must set the operation mode (host mode or device mode) by writing into the CM bits of the USBMODE register. Also the bootstrap input signal GPIO20 must be set accordingly.
Device Data Interface	The device controller operates to transfer a request in the QCA9558 system memory to and from the Universal Serial Bus. The device controller performs data transfers using a set of linked list transfer descriptors, pointed by a queue head one for each endpoint In and Out directions, The DMA engine performs master operations on the AHB system bus to transfer data to and fro.
Host Data Structure	The host data structures are used to communicate control, status, data and between software and the USB host controller. The data structure is compliant with EHCI specifications. A periodic frame list which is an array of pointers to a transfer list is used. There are asynchronous transfer lists for bulk and control data transfers and Isochronous Transfer list for Isochronous data transfers.
XCVR Interface	The USB Controller interfaces with an on-chip USB 2.0 PHY through the UTMI standard interface.

Table 3-20 shows the USB interface signals.

Table 3-20 USB Interface Elements

Name	Type	Description
USB_DP	IA/OA	USB D+ Signal
USB_DM	IA/OA	USB D– Signal

The QCA9558 has an exclusive USB 2.0 compliant host, that supports High-speed (480 Mbps), full speed (12Mbps) or Low speed (1.5 Mbps) clients. The USB core acts as a master on the internal AHB bus, thus maximizing data transfer speeds with the system DDR memory. The USB Host only interface supports all features of a compliant USB 2.0 host.

3.17 Bootrom

The QCA9558 incorporates 64 KBytes of on-chip read only memory (ROM) for initial booting. A bootstrap option indicates whether CPU will boot from external Flash or internal ROM. If selected for internal boot, Bootrom will map to the highest 64 KBytes of the CPU addressable space.

4 NAND Flash Controller

4.1 Overview

Figure 4-1 shows the NAND flash controller.

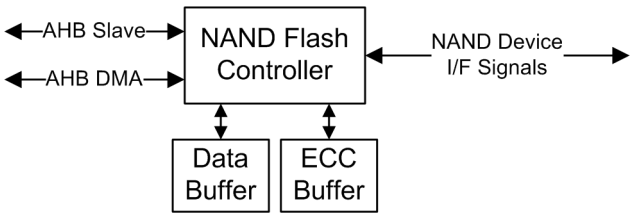


Figure 4-1 NAND Flash Controller

The NAND flash controller includes a configurable instruction mechanism to support a wide spectrum of flash devices with diverse programming requirements. It features:

- Page sizes of 256 Bytes to 16 KBytes
- Block sizes from 32 pages per block to 256 pages per block
- ECC support for error detection and correction; up to 16 bits of error per 512-byte page can be corrected
- 512-Byte data and ECC buffer
- Support for non-ONFI compliant devices through generic command sequences
- 8-bit parallel flash device interface
- Up to two external chip selects support device capacity up to 16 GBytes
- Bus master DMA on the AHB interface
- Programmable CMD/address/data cycles
- Faulty-page-address-remappable; up to 8 page addresses can be remapped
- Interrupts for device ready, command completion, ECC error, and FIFO error
- Sequential page reads within a sector
- Page copy back support (when the device supports it)

4.2 Command Encoding

The NAND flash controller supports many of the NAND flash devices currently in the market. It also includes a configurable instruction set for any new commands that appear with new devices. The command configuration allows defining set of parameters for each supported command sequence.

The 32-bit controller instruction field is constant and contains the command sequence code and these optional parameters:

- Command codes in instruction sequence
- Flag to select the address register used in command sequence
- Flag to select data source/sink for the command sequence (SIU or DMA unit)
- Command sequence code

Any unused fields in a given command sequence are ignored. Table 4-1 shows the instruction encoding scheme.

Table 4-1 Command Encoding

Bits	Name	Description	
31:24	CMD_2	Code for the third command in the sequence	
23:16	CMD_1	Code for the second command in the sequence	
15:8	CMD_0	Code for the first command in the sequence	
7	ADDR_SEL	Address register select flag:	
		0	Selects address register 0
		1	Selects address register 1
6	INPUT_SEL	Input module select flag	
		0	Select the SIU module as input
		1	Selects address register 1
5:0	CMD_SEQ	Sequence code	

4.3 Command Sequence Encoding

The NAND flash controller must be able to support new NAND flash device features with minimum designer effort, so it defines the set of commands, addresses, and data sequences to allow implementation of current and future instructions. Because NAND flash devices use the same set of signals regardless of memory capacity as well as a common I/O bus to transfer commands, addresses, and data, a device can be upgraded without PCB redesign.

This section defines most feature NAND flash device instructions, and Table 4-2 details command sequence encoding.

Table 4-2 Command Sequence Encoding

Symbol	Encoding
SEQ_0	000000
SEQ_1	100001
SEQ_2	100010
SEQ_3	000011
SEQ_4	100100
SEQ_5	100101
SEQ_6	100110
SEQ_7	100111
SEQ_8	001000
SEQ_9	101001
SEQ_10	101010
SEQ_11	101011
SEQ_12	001100
SEQ_13	001101
SEQ_14	001110
SEQ_15	101111
SEQ_16	110000
SEQ_17	010001
SEQ_18 and SEQ_19	SEQ_18: 110010 SEQ_19: 010011

4.3.1 SEQ_0

SEQ_0 is composed from the on command. After the command is written to, the NAND flash controller waits for the device to enter busy state, then it drives RnB low. When the delay (t_{WB}) ends or the device clears RnB, the sequence ends. The command code is encoded in CMD_1 and other fields are ignored.

Because the controller uses an internally generated sequence of read status commands to obtain device busy status instead of polling RnB, t_{WB} can be ignored.

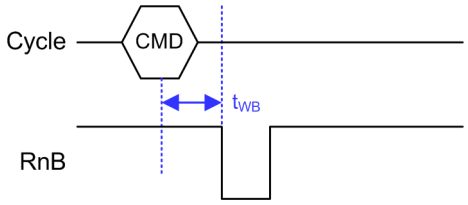


Figure 4-2 SEQ_0 Sequence

4.3.2 SEQ_1

This read sequence composed from the single command cycle, single address cycle, and single data cycle with a programmable number of read sequences. After the address sequence finishes, the controller measures the standard delay of first data read after the last write (t_{WHR}) and the read data words are written to the FIFO module.

The command code is encoded in CMD_1. The ADDR_SEL instruction field selects the address source and the input module is selected by the INPUT_SEL field.

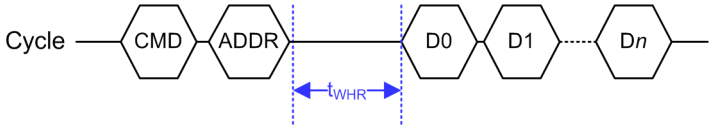


Figure 4-3 SEQ_1 Sequence

4.3.3 SEQ_2

This sequence is similar to SEQ_1, but after the address cycle the controller expects the device to enter busy state. Because the controller uses an internally generated sequence of read status commands to obtain device busy status instead of polling RnB, t_{WB} and t_{RR} can be ignored.

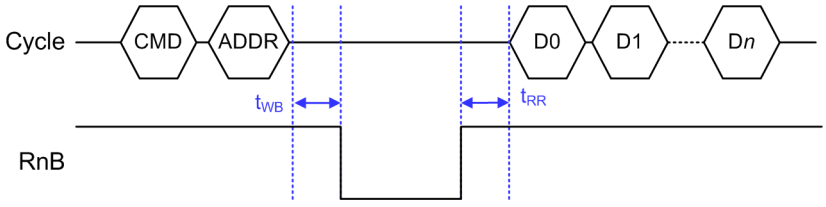


Figure 4-4 SEQ_2 Sequence

4.3.4 SEQ_3

This write sequence is composed from the single command cycle, single address cycle, and single data cycle, with a programmable number of write sequences. After the address sequence completes, the controller measures the standard delay of the first data write after the last address cycle (t_{ADL}). The written words are read from the FIFO module.

Because the controller uses an internally generated sequence of read status commands to obtain device busy status instead of polling RnB, t_{ADL} and t_{WB} can be ignored.

The command code is encoded in CMD_1. The ADDR_SEL instruction field selects the address source and the input module is selected by the INPUT_SEL field.

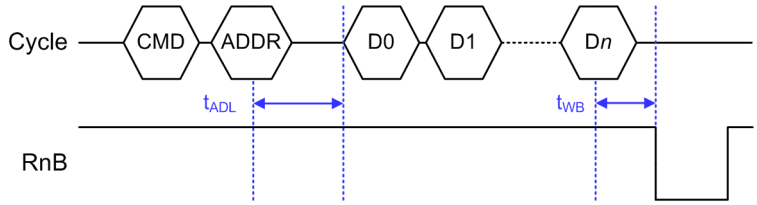


Figure 4-5 SEQ_3 Sequence

4.3.5 SEQ_4

This sequence is used to implement read status command sequences. It is composed from a single command cycle and a single data cycle. Between those cycles the delay (t_{WHR}) is counted. The command code is read from CMD_1; the data is stored in the working register of the NCU module and is accessible by reading the Read Status Command Output Value (READ_STATUS) register.

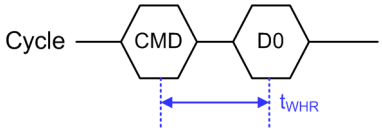


Figure 4-6 SEQ_4 Sequence

4.3.6 SEQ_5

This sequence is similar to SEQ_4, except that after the command cycle, an additional address cycle is performed.

The ADDR_SEL instruction field selects the address register used in the sequence.

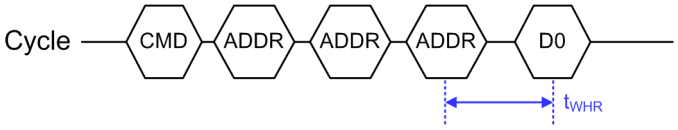


Figure 4-7 SEQ_5 Sequence

4.3.7 SEQ_6

For this read sequence, the delay from the last data cycle to the command cycle (t_{RHW}) is measured. Next the sequence of command cycle, address cycle, and command cycle is executed. Then the delay from the change column to the next operation (t_{CCS}) is measured. Finally the read data cycle is executed.

The first command code is encoded in CMD_1 and the second in CMD_2. The ADDR_SEL instruction field selects the address register used in the sequence and the input module is selected by the INPUT_SEL field.

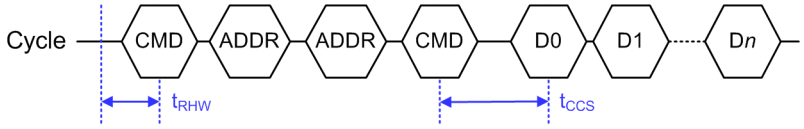


Figure 4-8 SEQ_6 Sequence

4.3.8 SEQ_7

This sequence is similar to the SEQ_6 sequence, except that the address cycle is composed of five bytes rather than three bytes.

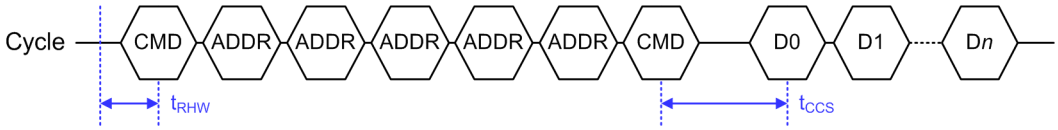


Figure 4-9 SEQ_7 Sequence

4.3.9 SEQ_8

For this write sequence, first the sequence of the command cycle and the two-byte address cycle is executed. Next, the delay after column address changing (t_{CCS}) is measured. Finally, the single data cycle with a programmable number of write sequences is executed.

The command code is encoded in CMD_1. The ADDR_SEL instruction field selects the address register used in the sequence. The input module is selected by the INPUT_SEL field.

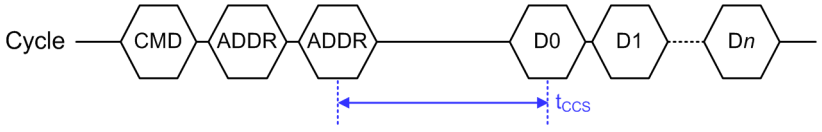


Figure 4-10 SEQ_8 Sequence

4.3.10 SEQ_9

First the sequence of command cycle, five bytes address cycle, and command cycle is executed. Because the controller uses an internally generated sequence of read status commands to obtain device busy status instead of polling RnB, t_{WB} can be ignored.

The first command code is encoded in CMD_1, the second is encoded in CMD_2. The ADDR_SEL instruction field selects the address register used in the sequence.

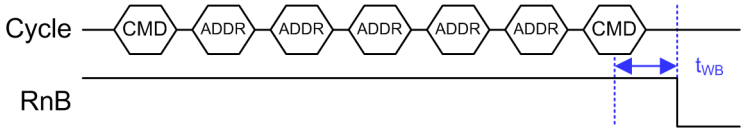


Figure 4-11 SEQ_9 Sequence

4.3.11 SEQ_10

This read sequence is similar to the SEQ_9, except that it is extended by the data read cycle. The input module is selected by the INPUT_SEL field.

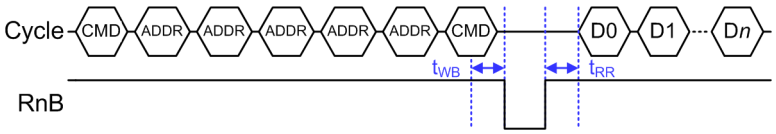


Figure 4-12 SEQ_10 Sequence

4.3.12 SEQ_11

In this read sequence, the first step is to execute the command cycle. Next, the controller waits for the device to go into the busy state. Because the controller uses an internally generated sequence of read status commands to obtain device busy status instead of polling RnB, t_{WB} and t_{RR} can be ignored. Once the device reaches the read state, the write data cycle with configurable read sequences is executed.

The command code is encoded in CMD_1. The ADDR_SEL instruction field selects the address register used in the sequence. The input module is selected by the INPUT_SEL field. The number of transferred bytes can be configured using DATA_SIZE SFR.

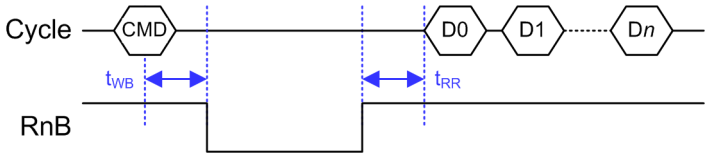


Figure 4-13 SEQ_11 Sequence

4.3.13 SEQ_12

This write sequence is command cycle, address cycle, data cycle with a configurable number of write operations and another command cycle. A delay (t_{ADL}) is measured between the last address cycle and first data cycle, and after the second command cycle (t_{WB}).

The first command code is encoded in CMD_1, and the second in CMD_2. The ADDR_SEL instruction field selects the address register used in the sequence. The input module is selected by the INPUT_SEL field.

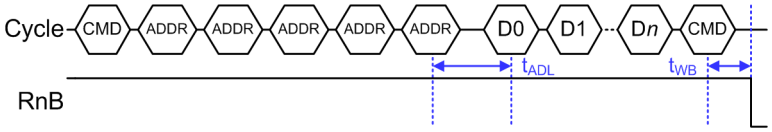


Figure 4-14 SEQ_12 Sequence

4.3.14 SEQ_13

This write sequence is a series of command cycle, address cycle, data cycle with a configurable number of the write operations. Between the last address cycle and first data cycle a delay is measured (t_{ADL}).

The first command code is encoded in CMD_1, and the second in CMD_2. The ADDR_SEL instruction field selects the address register used in the sequence. The input module is selected by the INPUT_SEL field.

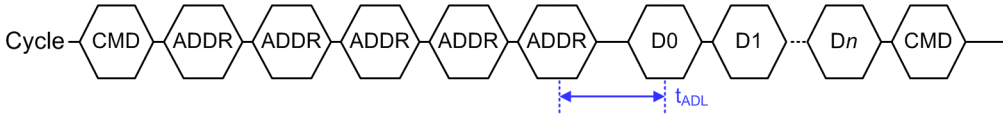


Figure 4-15 SEQ_13 Sequence

4.3.15 SEQ_14

First the series of command cycle, address cycle, command cycle is executed. Because the controller uses an internally generated sequence of read status commands to obtain device busy status instead of polling RnB, t_{WB} can be ignored.

The first command code is encoded in CMD_1, and the second in CMD_2. The ADDR_SEL instruction field selects the address register used in the sequence. The input module is selected by the INPUT_SEL field.

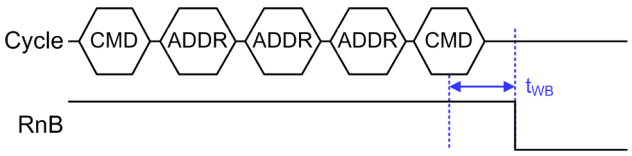


Figure 4-16 SEQ_14 Sequence

4.3.16 SEQ_15

First the series of command cycle, address cycle, second command cycle, second address cycle is executed. Because the controller uses an internally generated sequence of read status commands to obtain device busy status instead of polling RnB, t_{WB} and t_{RR} can be ignored.

Once the NAND flash device is back in ready state the data sequence is executed. The first command code is encoded in the CMD_1 instruction field; the second in CMD_2, the third command code in CMD_3. The first address cycle uses the address selected by the ADDR_SEL instruction field, the second uses the remaining address registers.

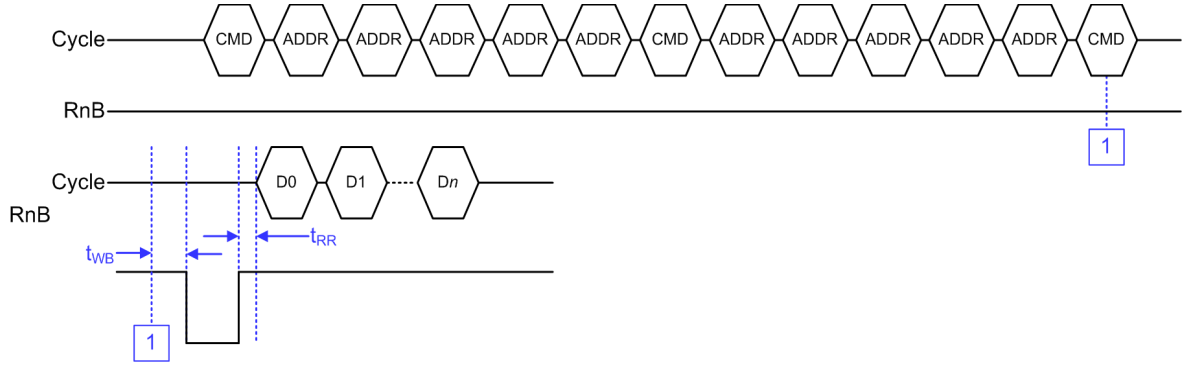


Figure 4-17 SEQ_15 Sequence

4.3.17 SEQ_16

This special sequence is used internally by the controller to detect if selected block is valid during the boot sequence. It allows checking of the selected block status. Each NAND flash device may have some number of bad blocks when it leaves the factory; the erroneous block number can increase as the number of program/erase operations increases.

According to the ONFI standard, the damaged blocks are marked by clearing the first word at the spare area offset in the first or the last page of the block. This sequence implements the page read operation with the read pointer set to the beginning of the page spare area. The single word is read and checked if it is equal to zero; if it is, the boot sequence is continued.

4.3.18 SEQ_17

This sequence is similar to the SEQ_10 sequence, but with no second command cycle.

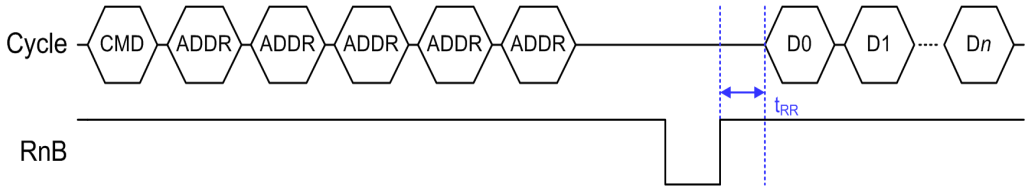


Figure 4-18 SEQ_17 Sequence

4.3.19 SEQ_18 and SEQ_19

SEQ_18 and SEQ_19 are described in Generic Command Sequence (see the DATA step).

4.4 Generic Command Sequence

A generic command sequence is included with the controller to address custom commands created by producers who do not support the ONFI standard or add non-standard commands to their devices. This generic command sequence mimics most commands supported by NAND flash devices. The generic command sequence is executed in these steps:

Step Name	Description
CMD0	This first command step is always present in the sequence. The value of the CMD0 field is sent to the NAND flash device.
ADDR0	The first address sequence (an optional phase). The address of the ADDR0 register is sent to the NAND flash device.
CMD1	The second command sequence (an optional phase). The value of the CMD1 field of the generic command instruction is send to the NAND flash device.
ADDR1	The first address sequence (an optional phase). The address of ADDR1 is sent to the NAND flash device.
CMD2	The third command sequence (an optional phase). The value of the CMD2 field of the generic command instruction is send to the NAND flash device.
DEL0	The wait for the device back from the busy state if the sequence must be continued. The controller waits for the device to back to the ready state and continue the sequence.
DATA	The data phase of the sequence. The transfer direction must be set by the sequence. SEQ_18 reads data from the NAND flash memory, SEQ_19 writes data to NAND flash memory.
CMD3	The fourth command sequence (an optional phase).
DEL1	The wait for the device back from the busy state if the sequence is finished. The controller waits for the device to back to the ready state and finish the sequence.

Figure 4-19 shows the generic sequence composition.

Figure 4-19 Generic Sequence

4.5 Instructions

This implementation of the instruction set is an example of using the instruction encoding scheme presented in Table 4-1, "Command Encoding," on page 83. This section contains the information necessary to implement new commands for NAND flash devices. Table 4-3 contains basic instructions on command sequences assessable in the ONFI standards.

Table 4-3 Instructions Set: Command Sequences Available in ONFI Standards

Instruction	CMD_1	CMD_2	CMD_3	CMD_SEQ	ADDR_ SEL	INPUT_ SEL	Valid Busy
Reset Commands							
RESET	0xFF	—	—	SEQ_0	—	—	Yes
SYNCH_RESET	0xFC	—	—	SEQ_0	—	—	Yes
Identification Commands							
READ_ID	0x90	—	—	SEQ_1	0/1	0/1	No
READ_PARAMETER_PAGE	0xEC	—	—	SEQ_2	0/1	0/1	No
READ_UNIQUE_ID	0xED	—	—	SEQ_2	0/1	0/1	No
Configuration Commands							
GET_FEATURES	0xEE	—	—	SEQ_2	0/1	0/1	No
SET_FEATURES	0xEF	—	—	SEQ_3	0/1	0/1	No
Status Commands							
READ_STATUS	0x70	—	—	SEQ_4	—	—	No
SELECT_LUN_WITH_STATUS	0x78	—	—	SEQ_5	0/1	—	No
Column Address Commands							
CHANGE_READ_COLUMN	0x05	0xE0	—	SEQ_6	0/1	—	No
SELECT_CACHE_REGISTER	0x06	0xE0	—	SEQ_7	0/1	—	No
CHANGE_WRITE_COLUMN	0x85	—	—	SEQ_8	0/1	—	No
CHANGE_ROW_ADDRESS	0x85	—	—	SEQ_12	0/1	—	No
Read Commands							
READ_PAGE	0x00	0x30	—	SEQ_10	0/1	0/1	No
READ_PAGE_CACHE	0x31	—	—	SEQ_11	0/1	0/1	No
READ_PAGE_CACHE_LAST	0x3F	—	—	SEQ_10	0/1	0/1	No
READ_MULTIPANE	0x00	0x32	—	SEQ_16	0/1	—	No
READ_TWO_PLANE	0x00	0x00	0x30	SEQ_12	0/1	0/1	No
Program Commands							
PROGRAM_PAGE	0x80	0x10	—	SEQ_12	0/1	0/1	No
PROGRAM_PAGE_1	0x80	—	—	SEQ_13	0/1	0/1	No
PROGRAM_PAGE_CACHE	0x80	—0x15	—	SEQ_12	0/1	0/1	No
PROGRAM_MULTIPLANE	0x80	0x11	—	SEQ_12	0/1	0/1	No
WRITE_PAGE	0x10	—	—	SEQ_0	—	—	No
WRITE_PAGE_CACHE	0x15	—	—	SEQ_0	—	—	No
WRITE_MULTIPLANE	0x11	—	—	SEQ_0	—	—	No

Table 4-3 Instructions Set: Command Sequences Available in ONFI Standards

Instruction	CMD_1	CMD_2	CMD_3	CMD_SEQ	ADDR_ SEL	INPUT_ SEL	Valid Busy
Erase Commands							
ERASE_BLOCK	0x60	0xD0	—	SEQ_14	0/1	—	No
ERASE_MULTIPLANE	0x60	0xD1	—	SEQ_14	0/1	—	No
Copyback Commands							
COPYBACK_READ	0x00	0x35	—	SEQ_10	0/1	0/1	No
COPYBACK_PROGRAM	0x85	0x10	—	SEQ_9	0/1	—	No
COPYBACK_PROGRAM1	0x85	—	—	SEQ_13	0/1	—	No
COPYBACK_MULTIPLANE	0x85	0x11	—	SEQ_12	0/1	0/1	No
OTP Commands							
PROGRAM_OTP	0xA0	0x10	—	SEQ_12	0/1	0/1	No
DATA_PROTECT_OTP	0xA5	0x10	—	SEQ_9	0/1	—	No
READ_PAGE_OTP	0xAF	0x30	—	SEQ_10	0/1	0/1	No
TWO_PLANE_PAGE_READ	0x00	0x00	0x30	SEQ_15	0/1	0/1	No
SET_FEATURES_2	0xEF	—	—	SEQ_17	0/1	0/1	No

Each instruction goes through defined phases, and the current controller configuration decides whether a given phase is executed:

1. The instruction code is written to the register Controller Commands (COMMAND), which triggers the instruction execution.

   The DCU decodes the instruction and configures the controller to execute it. At this point, the input module for the data FIFO is selected. The NCU module gets the sequence number to execute and the auxiliary parameter for the operation.

2. The command sequence in the instruction is executed in the NCU unit. This process details depends on the controller configuration.

3. If interrupts are enabled, the interrupt will be raised after command execution.

The ADDR_SEL (bit [7]) and INPUT_SEL (bit [6]) fields of the register Controller Commands (COMMAND) are configurable for every instruction that uses them. When an instruction does not use an address SFR or FIFO, these fields are ignored. Ignored fields should have a value of zero.

Command Name	RESET			
Description	This command puts a target into a known condition and aborts command sequences in progress. This command is accepted by all logical unit numbers (LUNs), even when they are busy. It is only issued when the host is configured to the asynchronous data interface. The controller construction does not allow the use of asynchronous commands in synchronous mode; this command should be only used in the asynchronous mode.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0xFF	—	—	SEQ_0

Command Name	SYNCH_RESET			
Description	This command puts a target into a known condition and aborts a command sequence in progress when the synchronous interface is active. It is accepted by all LUNs, even when they are busy. This command is only accepted while the synchronous interface is active. Its use is prohibited when the asynchronous interface is active.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0xFC	—	—	SEQ_0

Command Name	READ_ID			
Description	This command reads identifier codes programmed into the target. It is accepted by the target only when all LUNs on the target are in the IDLE state. When the command is followed by an address cycle of 0x00, the target returns a 5-byte identifier code that includes the manufacturer's ID, device configuration, and part-specific information. When this command is followed by an address cycle of 0x20, the target returns the 4-byte ONFI identifier code.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x90	—	—	SEQ_1

Command Name	READ_PARAMETER_PAGE			
Description	This command reads the ONFI parameter page programmed into the target. It is accepted by the target only when all LUNs on the target are idle. When the command is followed by an address cycle of 0x00, the target goes to busy state. After the read process completes the controller enables data output mode to read the parameter page.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0xEC	—	—	SEQ_2

Command Name	READ_UNIQUE_ID			
Description	This command reads a unique identifier programmed into the target. It is accepted by the target only when all LUNs on the target are idle. When the address cycle of 0x00 is written to the target, then the target goes busy. Once the read process is complete, the controller enables data output mode to read the unique ID. Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes, where the first 16 bytes are unique data and the second 16 bytes are their complement. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of 0xFF, then that copy of the unique ID data is correct. For a non-0xFF result, the host can repeat the XOR operation on a subsequent copy of the unique ID data.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0xED	—	—	SEQ_2

Command Name	GET_FEATURES			
Description	This command reads the sub-feature parameters (P1–P4) from the specified feature address. It is accepted by the target only when all LUNs on the target are idle. When the 0xEE command is followed by a feature address, the target goes busy. After the target's internal read operation completes, the controller enables data output mode to read the sub-feature parameters.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0xEE	—	—	SEQ_2

Command Name	SET_FEATURES			
Description	This command writes the sub-feature parameters (P1–P4) to the specified feature address to enable or disable target-specific features. It is accepted by the target only when all LUNs on the target are idle. The 0xEF command is followed by a valid feature address; the address value depends on the feature set implemented in the target device. The address cycle is followed by the configurable number of data cycles. Allowed values of the address and data encoding scheme can be found in the device vendor documentation.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0xEF	—	—	SEQ_3

Command Name	READ_STATUS			
Description	Each LUN provides its status independently of other LUNs on the same target through its 8-bit target status register. Once this command is issued, the target status register output is enabled, and its contents are returned on DQ[7: 0] for each data output request. This command returns the status of the most recently selected LUN.			
Encoding	This command can be executed when the target is in the BUSY state. The FIFO cannot access the read data because can be occupied by the operation under execution. The special SFR allows immediate access to the status data.			
	CMD_1	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x70	—	—	SEQ_4

Command Name	SELECT_LUN_WITH_STATUS			
Description	Each LUN provides its status independently of other LUNs on the same target through its 8-bit target status register. Once SELECT_LUN_WITH_STATUS is issued, the target status register output is enabled. The contents of the target status register are returned on DQ[7: 0] for each data output request. READ_STATUS returns the status of the selected LUN.			
Encoding	This command can be executed when the target is in the BUSY state. The FIFO cannot access the read data because can be occupied by the operation under execution. The special SFR allows immediate access to the status data.			
	CMD_1	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x78	—	—	SEQ_5

Command Name	CHANGE_READ_COLUMN			
Description	This command changes the column address of the selected target cache register and enables data output of the last selected LUN. It is accepted by the selected LUN when it is ready. Writing 0x05 to the target command register followed by: two column address cycles containing the column address then the 0xE0 command puts the selected LUN into data output mode. The selected LUN stays in data output mode until another valid command is issued.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x05	0xE0	—	SEQ_6

Command Name	SELECT_CACHE_REGISTER			
Description	This command enables data output on the addressed LUN and target cache register at the specified column address. It is accepted by a LUN when it is ready. Writing 0x06 to the target command register followed by two column address cycles, then three row address cycles, then by 0xE0 enables data output mode on the address LUN and target cache register at the specified column address.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x06	0xE0	—	SEQ_7

Command Name	CHANGE_WRITE_COLUMN			
Description	This command changes the column address of the selected target cache register and enables data input on the last selected LUN. Writing the 0x85 to the target command register followed by two column address cycles containing the column address puts the selected LUN into data input mode.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x85	—	—	SEQ_8

Command Name	CHANGE_ROW_ADDRESS			
Description	This command changes the row address (block and page) where the target cache register contents will be programmed in the NAND array. It also changes the column address of the selected target cache register and enables data input on the specified LUN.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x85	—	—	SEQ_12

Command Name	READ_PAGE			
Description	This command copies a page from the NAND flash array to its respective target cache register and enables data output. It is accepted by the LUN when it is ready. To read a page from the NAND flash array, have the controller write 0x00 to the target command register, then write 5 address cycles to the address registers, and conclude with writing 0x30 to the target command register. The selected LUN will go busy as data is transferred. When the LUN is ready data output is enabled for the target cache register linked to the plane addressed in this command. The controller reads the programmed number of bytes to the FIFO.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x00	0x30	—	SEQ_10

Command Name	READ_PAGE_CACHE			
Description	This command reads the next sequential page within a block into the target data register while the previous page is output from the target cache register. To issue this command, the controller writes 0x31 to the target command register. After this command is issued, the RnB goes LOW and the LUN is busy. After RnB goes high and the LUN is busy with a cache operation, indicating that the target cache register is available and that the specified page is copying from the NAND flash array to the target data register. At this point, data is read from the target cache register.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x31	—	—	SEQ_11

Command Name	READ_PAGE_CACHE_LAST			
Description	This command ends the READ_PAGE_CACHE sequence and copies a page from the target data register to the target cache register. This command is accepted by the LUN when it is ready. To issue this command, controller writes the 0x3F to the target command register. After this command is issued, the RnB goes LOW and the LUN is busy. After RnB goes HIGH and the LUN is ready. At this point, data from the target cache register are read in to the FIFO.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x3F	—	—	SEQ_10

Command Name	READ_MULTIPANE			
Description	This command queues a plane to transfer data from the NAND array to its target cache register. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for data transfer. To select the final plane and to begin the read operation for all previously queued planes, issue the READ_PAGE command. All queued planes will transfer data from the NAND array to the target cache registers.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x00	0x32	—	SEQ_16

Command Name	READ_TWO_PLANE			
Description	This command is similar to READ_PAGE. It transfers two pages of data from the NAND flash array to the target data registers. Each page must be from a different plane on the same die. To enter TWO-PLANE PAGE READ mode, controller writes the 0x00 command to the target command register, and then writes 5 ADDRESS cycles for plane 0. Next, writes the 0x00 command to the target command register, then write 5 ADDRESS cycles for plane 1. Finally, controller writes the 0x30 command. The first-plane and second-plane addresses must meet the two-plane addressing requirements and, in addition, they must have identical column addresses. After the 0x30 command is written, page data is transferred from both planes to their respective target data registers. The target device goes to the BUSY state. After the internal read operation is completed the content of the page from the plane 0 is transferred to the FIFO			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x00	0x00	0x30	SEQ_12

Command Name	PROGRAM_PAGE			
Description	This command allows the host to input data to the target cache register and moves the data from the target cache register to the specified block and page address in the array of the selected LUN. It is accepted by the LUN when it is ready. To input a page to the target cache register and move it to the NAND array at the block and page address specified, controller writes the 0x80 to the target command register. Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. When data input is complete, controller writes the 0x10 to the target command register. The selected LUN will go busy.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x80	0x10	—	SEQ_12

Command Name	PROGRAM_PAGE_1			
Description	This command allows the host to input data to a target cache register and moves the data from the target cache register to the specified block and page address in the array of the selected LUN. This command is accepted by the LUN when it is ready. To input a page to the target cache register and move it to the NAND array at the block and page address specified, controller writes the 0x80 to the target command register. Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. When data input is complete, commands sequence ends.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x80	—	—	SEQ_13

Command Name	PROGRAM_PAGE_CACHE			
Description	This command allows the controller to input data to a target cache register, copies the data from the target cache register to the target data register, and then moves the target data register contents to the specified block and page address in the array of the selected LUN. After the data is copied to the target data register the target cache register is available for additional PROGRAM_PAGE and PROGRAM_PAGE_CACHE commands. The PROGRAM_PAGE_CACHE command is accepted by the LUN when it is ready. To input a page to the target cache register to move it to the NAND array at the block and page address specified, controller writes the 0x80 to the target command register. Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. When data input is complete, write 0x15 to the target command register. The selected LUN will go busy to allow the target data register to become available from a previous program cache operation, to copy data from the target cache register to the target data register, and then to begin moving the target data register contents to the specified page and block address.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x80	0x15	—	SEQ_12

Command Name	PROGRAM_MULTIPLANE			
Description	This command allows the controller to input data to the addressed plane's target cache register and queue the target cache register to ultimately be moved to the NAND array. It can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. This command is accepted by the LUN when it is ready. The controller writes 0x80 to the target command register, then writes five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. When data input is complete, the controller writes 0x11 to the target command register.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x80	0x11	—	SEQ_12

Command Name	WRITE_PAGE			
Description	This command allows the controller to move data from the target cache register to the NAND array. It is accepted by the LUN when it is ready. The controller writes the 0x10 to the target command register.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x10	—	—	SEQ_0

Command Name	WRITE_PAGE_CACHE			
Description	This command allows the controller to move data from the target cache register to the target data register. It is accepted by the LUN when it is ready. The controller writes 0x11 to the target command register.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x15	—	—	SEQ_0

Command Name	WRITE_MULTIPLANE			
Description	This command allows the controller to queue data from the target cache register to the NAND array. It is accepted by the LUN when it is ready. The controller writes the 0x15 to the target command register.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x11	—	—	SEQ_0

Command Name	ERASE_BLOCK			
Description	This command erases the specified block in the NAND array. It is accepted by the LUN when it is ready. To erase a block, the controller writes the 0x60 to the target command register, then writes three address cycles containing the row address; the page address is ignored. It concludes by writing 0xD0 to the target command register.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x60	0xD0	—	SEQ_14

Command Name	ERASE_MULTIPLANE			
Description	This command queues a block in the specified plane to be erased from the NAND array. It can be issued one or more times. Each time a new plane address is specified, that plane is also queued for a block to be erased. This command is accepted by the LUN when it is ready. To queue a block to be erased, controller write the 0x60 to the target command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing 0xD1 to the target command register.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x60	0xD1	—	SEQ_0

Command Name	COPYBACK_READ			
Description	This command is functionally identical to the READ_PAGE command, except 0x35 is written to the target command register instead of 0x30.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x00	0x35	—	SEQ_10

Command Name	COPYBACK_PROGRAM			
Description	This command is functionally identical to the PROGRAM_PAGE command, except that when 0x85 is written to the target command register, the target cache register contents are not cleared.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x85	0x10	—	SEQ_9

Command Name	COPYBACK_PROGRAM1			
Description	This command is functionally identical to the PROGRAM_PAGE_1 command, except that when 0x85 is written to the target command register, the target cache register contents are not cleared.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x85	—	—	SEQ_13

Command Name	COPYBACK_MULTIPLANE			
Description	This command is functionally identical to the PROGRAM_MULTIPLANE command, except that when 0x85 is written to the target command register, the target cache register contents are not cleared.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0x85	0x11	—	SEQ_12

Command Name	PROGRAM_OTP			
Description	This command is used to write data to the pages within the OTP area. An entire page can be programmed at one time, or a page can be partially programmed up to four times. OTP pages have no ERASE operation. To use this command, the controller issues the 0xA0 command, then issues 5 address cycles. The address write is followed by programmable number of data cycles. After data input is complete, controller issue the 0x10 command. The internal control logic automatically executes the proper programming algorithm and controls the necessary timing for programming and verification.			
Encoding	CMD_1	CMD_2	CMD_3	CMD_SEQ
	0xA0	0x10	—	SEQ_12

Command Name	DATA_PROTECT_OTP			
Description	This command is used to protect all the data in the OTP area. After the data is protected it cannot be programmed further. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected. To use this command, the controller issues the 0xA5 command. Next, the controller issues the following 5 addresses cycles. Finally, it issues the 0x10 command.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0xA5	0x10	—	SEQ_9

Command Name	READ_PAGE_OTP			
Description	This command reads data from a page within the OTP area. An OTP page within the OTP area is available for reading data whether or not the area is protected. To use this command, the controller issues the 0xAF command. Next, it issues 5 address cycles. Finally, issue the 0x30 command. After internal read from NAND matrix is ended the data is copied to the FIFO.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0xAF	0x30	—	SEQ_10

Command Name	TWO_PLANE_PAGE_READ			
Description	This command was implemented to preserve the compatibility with the ONFI 1.x and some older devices. It is similar to the READ_PAGE command. It transfers two pages of data from the NAND flash array to the target data registers. Each page must be from a different plane on the same die. The software is responsible to generate correct addresses for the requested pages. Both the ADDR0 and ADDR1 addresses registers (see Most Significant Part of the Address 0/1 (ADDR0_0, ADDR0_1, ADDR1_0, ADDR1_1)) are used in this case.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0x00	0x00	0x30	SEQ_15

Command Name	SET_FEATURES_2			
Description	This command writes the sub-feature parameters (P1–P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all LUNs on the target are idle. The 0xEF command is followed by a valid feature address. The possible address value depends on the features set implemented in the target device. The address cycle is followed by the configurable number of data cycles. Allowed values of the address and data encoding scheme can be found in the device vendor documentation. This command must be used to switch from the asynchronous mode to the synchronous mode.			
Encoding	**CMD_1**	**CMD_2**	**CMD_3**	**CMD_SEQ**
	0xEF	—	—	SEQ_17

4.6 NAND Setup and Configuration

The Main Configuration (CONTROL) register is the main control register in the NAND flash controller. To set up the NAND:

1. Configure the basic controller settings:

ADDR_CYCLE	The number of address bytes sent to NAND flash device
ADDRx_AUTO_INCR	Addresses auto increment for address register 0 or 1
BLOCK_SIZE	Bits which configure block size
PAGE_SIZE	Bits which configure page size
IO_WIDTH	Bits which configure width of the I/O bus connected to the PHY module. When the controller works in synchronous mode I/O bus should consist of 16 bits (IO_ WIDTH = 1).
WORK_MODE	Must be set for the controller to work in synchronous mode

2. When NAND flash controller uses DMA to transfer data the software should configure the registers:
   - DMA Module Base Address (DMA_ADDR)
   - DMA Module Counters Initial Value (DMA_CNT)
   - DMA Module Control (DMA_CTRL)
   - DMA Module Address Offset (DMA_ADDR_OFFSET)

   The software can modify these registers before any transfer or during initialization.

   Configure these registers depending on the settings of these bits in the Main Configuration (CONTROL) register:

Bit	Bit Name	Configure:
3	SPARE _EN	If set, software should write the size of the spare area to the NAND Flash Spare Area Size (SPARE_SIZE) register.
4	INT_EN	If set, software should writes the mask into the Interrupt Mask (INT_MASK) register that masks selected interrupt source in the NAND flash controller.
5	ECC_EN	If set, software should configure the ECC module by writing to the register Configuration Parameters for the ECC Module (ECC_CTRL). Additionally, software should configure ECC Offset Value (ECC_OFFSET). The ECC module can be turned on only if the bit CUSTOM_SIZE_EN = 0.
11	CUSTOM_ SIZE_EN	If set, software should write the data transferred by the controller. If this bit is set, the ECC module is disabled.
13	LOOKUP_EN	Software can use remapping using the eight LOOKUP registers.
14	PROT_EN	Software can protect the area space which cannot be erased or overwritten. The Hardware Protect Against the Write/Erase Process Control (PROTECT) register defines the area that will be protected against any modification.

3. Additionally, the software should configure time parameters, which can be found in the Timing Configuration 0 (TIMING_ASYN) register for asynchronous mode and in the Timing Configuration 1 (TIMING_SYN) register for synchronous mode.

5 Ethernet Subsystem

5.1 GMAC0 and GMAC1

The QCA9558 has two independent GB Ethernet MACs.

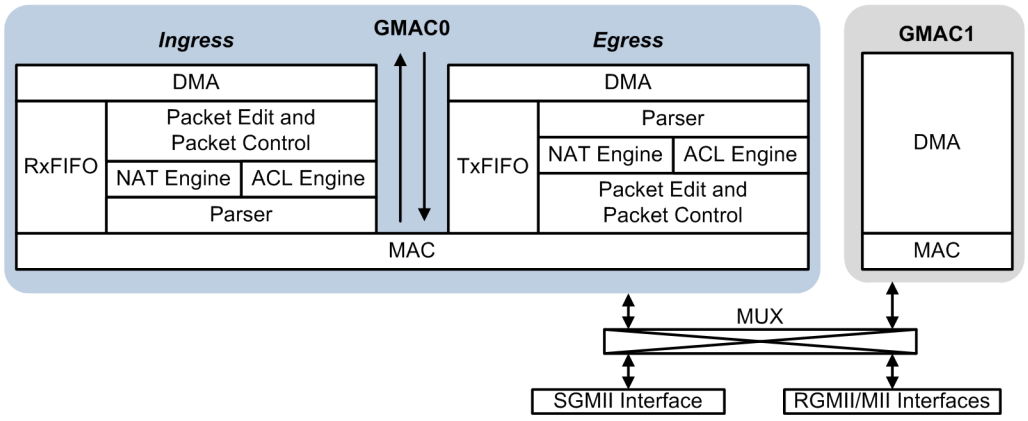


Figure 5-1 Ethernet Subsystem

GMAC0 functions as a WAN post and connects through the MII/RGMII interfaces. Table 5-1 shows the major blocks in GMAC0.

Table 5-1 GMAC0 Blocks

Block	Description
MAC	Detects the SFD, takes care of IFG, Rx/Tx final data in MAC interface format (RGMII/MII, and so on)
Parser	Parses the incoming data (from MAC in the case of ingress, or from DMA in the case of egress), detects the packet type, and isolates all L2, L3, and L4 related fields for NAT and ACL engine
NAT Engine	Creates the lookup table (LUT) and supports entry lookup, addition, and deletion in the LUT for CPU and the parser
ACL Engine	Builds the ACL rule table. From the fields generated by the parser, this block checks the rules and returns with the packet drop or accept decision. If ACL is disabled, then all packets are accepted
Packet Control/ Edit Block	Maintains the packet integrity in the FIFO, takes in the result from both the NAT and ACL engines, edits the packet for NAT, and drops/queues the packet depending on ACL decisions; also takes care of generating control signals to the MAC/DMA, enabling these blocks to transmit the packet from the FIFO

5.1.1 External RGMII/MII Interface

The Ethernet Configuration (ETH_CFG) register determines how GMAC0 is interfaced in the QCA9558:

- In RGMII mode, Tx clock comes from an internal PLL; the exact clock delay with respect to data can be modified using the ETH_TXD_DELAY, and ETH_RXD_DELAY bits.
- In MII master mode, the QCA9558 can source both Tx and Rx clocks. In slave mode, it expects both clocks from external sources.
- MDIO interface to external PHY registers, through dedicated EMDIO and EMDC pins. MDIO interface is controlled through the GMAC0 MII registers described in the MII Configuration through MII Indicators, page 444 through page 446.

5.1.2 SGMII Interface

The SGMII interface provides a high-speed serial interface that connects a GBit MAC and a 10/100/1000 PHY while requiring fewer GMII/RGMII signal pins. It can operate in both half- and full-duplex modes at ports speeds of 10, 100, and 1000 Mbps.

SGMII uses two data signals and two clock signals to convey frame data and link rate information between a 10/100/1000 PHY and an Ethernet MAC. The data signals operate at 1.25 GBaud and the clocks operate at 625 MHz (a DDR interface). Due to operating speed, each of these signals is realized as a differential pair, providing signal integrity while minimizing system noise.

The QCA9558 SGMII interface operates in a mode where the clock is recovered from the received data rather than being provided as a separate pin. SGMII interface pins include:

- SGMII_SIN
- SGMII_SIP
- SGMII_SOP
- SGMII_SON

SGMII supports these operating modes:

- SGMII MAC mode

  In this mode the MAC exchanges capability information across the SGMII interface and sets speeds accordingly as 10, 100, or 1 GBps mode. Either GMAC0 or GMAC1 can be connected to the SGMII physical interface of the QCA9558.
- Auto-negotiation

  In SGMII MAC mode, control information is sent during auto-negotiation. While this exchange is labeled auto-negotiation, it is an information exchange where the PHY passes the copper side auto-negotiation results to the MAC. The MAC responds to the PHY with an acknowledgment.

The MDIO interface is not directly supported through SGMII; use the GPIO-based MDIO master interface 1. See MDIO Master Interface.

5.1.3 GMAC0-Based WLAN Accelerators

GMAC0 is exposed as a separate MAC port on the RGMII or MII interface. It is treated as a WAN port and has several Ethernet-specific accelerators (see Table 5-2). Each accelerator can be separately enabled/disabled by software.

5.1.4 Ingress and Egress Flow of Data and Control Information

Table 5-2 GMAC0 Accelerator Types

Accelerator Type	Rx/Tx	Description
Ingress and Egress NAT Accelerator for IPv4	Rx/Tx	Type II/SNAP-tagged/untagged TCP/UDP/ICMP packets that can support up to 256 entries per direction. Supports hardware-based aging of entries with a different MaxAge timer for TCP, UDP, and ICMP packets. Five tuple information lookup; individual masks to enable each tuple. NAT is performed at wire-speed and is capable of handling GB Ethernet port maximum packet rate. See GMAC Descriptor Structure: Rx through Setup and Data/Packet Flow, page 108 through page 113
Ingress and Egress ACL Accelerator	Rx/Tx	Can support up to 64 entries per direction, with each entry supporting up to five match commands per entry. Supports an ACL accelerator for WAN Rx and Tx traffic. Can be used in accept (default) or reject mode.
QoS	Tx	Supports Tx QoS with different queues: fixed or weighted round-robin algorithms.

The flow of data and control information in the GMAC ingress and egress are detailed in Figure 5-2 and Figure 5-3.

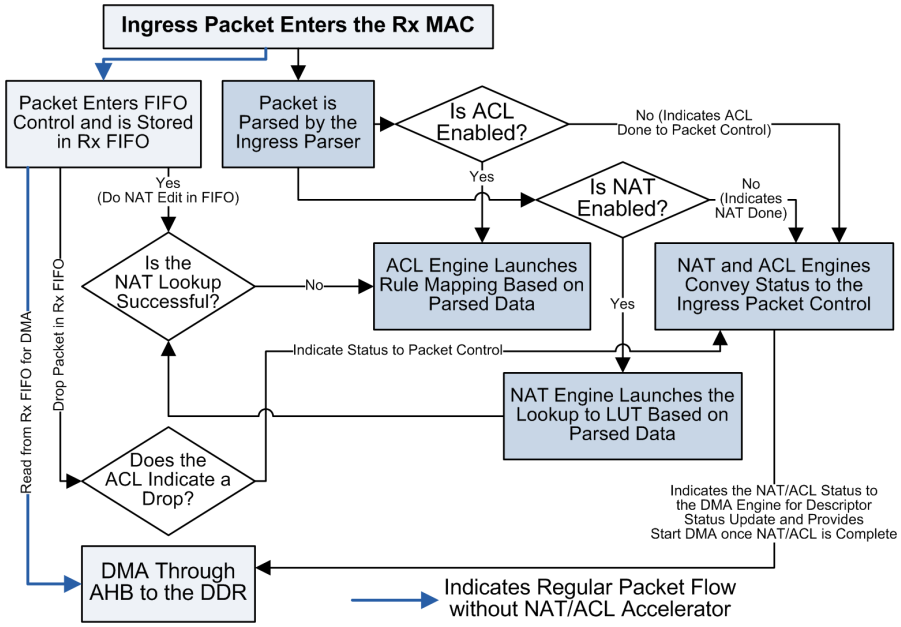


Figure 5-2 Ingress Data and Control in GMAC0

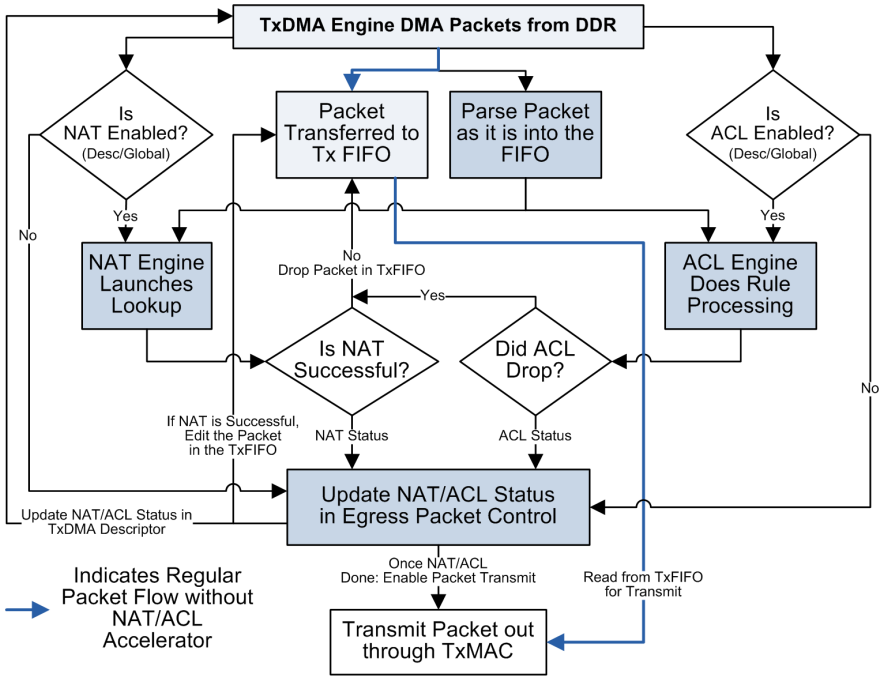


Figure 5-3 Egress Data and Control in GMAC0

5.2 GMAC Descriptor Structure: Rx

In the Rx descriptor, each descriptor comprises a sequence of three 32-bit memory locations:

Table 5-3 Rx Descriptors

Address	Name	Description	Page
0x0	PKT_START_ADDR	Start Address for Packet Data	page 108
0x4	PKT_SIZE	Packet Size and Flags	page 108
0x8	NEXT_DESCRIPTOR	Next Packet Descriptor Address	page 109

5.2.1 Start Address for Packet Data (PKT_START_ADDR)

Address Offset: 0x0
Access: Read/Write

Bit	Name	Description
31:0	PKT_START_ADDR	Packet start address. The built-in DMA controller reads this register to discover the location in host memory of the first byte of data. Note: The start addresses used in any sequence of descriptors must be spaced to add sufficient room in any location for a packet of the maximum size transferred.

5.2.2 Packet Size and Flags (PKT_SIZE)

Address Offset: 0x4
Access: See field descriptions

Bit	Name	Access	Description
31	EMPTY_FLAG	R/W	This bit indicates the availability of the specified location to store the received packet. Setting this flag validates the descriptor. This bit is also called the OWN (ownership) bit. Note: On successful completion of an Rx operation, the DMA controller writes 0 to this location to indicate that this location has been used to store the received packet. This action ensures that received data is not accidentally overwritten by a subsequent packet.
30	NAT_STATUS	RO	Set by the DMA controller indicating the NAT Status for the packet. 0 NAT operation is not done. Valid only if Ingress NAT functionality is enabled. 1 Successfully NAT edit.
29:28	RES	RO	Reserved
27:26	SW_STATUS	RO	Provides the software status bits loaded into the LUT for the connection that the packet belongs to.
25	NAT_UNSUPPORTED	RO	Indicates an ERROR status for NAT because the packet is unsupported 0 Supported packet type 1 Unsupported packet type; valid only if NAT_STATUS is set to 0 and ingress NAT functionality is enabled
24	PER_PKT_INTR_EN	R/W	When set to 1 by software, the DMA controller generates an interrupt to the CPU after successful completion of the packet DMA.
23	FRG	RO	Indicates whether this packet is fragmented
22:14	RES	RO	Reserved
13:0	PKT_SIZE	R/W	Updated by the hardware with the size of the actual packet received.

5.2.3 Next Packet Descriptor Address (NEXT_DESCRIPTOR)

Address Offset: 0x8
Access: Read/Write

Bit	Name	Description
31:2	DESCRIPTOR_ADDR	Top 30 bits of Packet the descriptor address. The built-in DMA controller reads this register to discover the location in host memory of the descriptor for the next packet in the sequence. The descriptors should form a closed linked list.
1:0	RES	Ignored by the DMA controller because it is a requirement of the system that all descriptors are 32-bit aligned in host memory. Default is 0.

5.3 GMAC Descriptor Structure: Tx

In the Tx descriptor, each descriptor comprises a sequence of three 32-bit memory locations:

Table 5-4 Tx Descriptors

Address Offset	Name	Description	Page
0x0	PKT_START_ADDR	Start Address for Packet Data	page 109
0x4	PKT_SIZE	Packet Size and Flags	page 110
0x8	NEXT_DESCRIPTOR	Next Packet Descriptor Address	page 110

5.3.1 Start Address for Packet Data (PKT_START_ADDR)

Address Offset: 0x0
Access: Read/Write

Bit	Name	Description
31:0	PKT_START_ADDR	Packet start address. The built-in DMA controller reads this register to discover the location in host memory of the first byte of data. Note: The start addresses used in any sequence of descriptors must be spaced to add sufficient room in any location for a packet of the maximum size transferred.

5.3.2 Packet Size and Flags (PKT_SIZE)

Address Offset: 0x4
Access: See fields descriptions

Bit	Name	Access	Description	
31	EMPTY_FLAG	R/W	This bit indicates the availability of the specified location to store the received packet. Setting this flag validates the descriptor. Note: On successful completion of an Rx operation, the DMA controller writes 0 to this location to indicate that this location has been used to store the received packet. This action ensures that received data is not accidentally overwritten by a subsequent packet.	
30	PER_PACKET_NAT_ENABLE	R/W	Used to control NAT function for Tx Packets on per-packet basis.	
			0	The Tx packet bypasses the egress NAT Engine. Valid only if egress NAT is enabled.
			1	The Tx packet goes through the egress NAT engine.
29	PER_PACKET_ACL_ENABLE	R/W	Used to control ACL function for Tx Packets on per-packet basis.	
			0	The Tx packet bypasses the egress ACL Engine. Valid only if egress ACL is enabled.
			1	The Tx packet goes through the egress NAT engine.
28	NAT_STATUS	RO	Set by the DMA controller indicating the NAT Status for the packet. '	
			0	NAT unsuccessful. Valid only if the egress NAT functionality is enabled and PER_PACKET_ACL_ENABLE is set.
			1	NAT successful.
27	ACL_STATUS	RO	Set by the DMA controller indicating the ACL Status for the packet.	
			0	ACL allow. Valid only if the egress ACL functionality is enabled and PER_PACKET_ACL_ENABLE is set.
			1	ACL drop
26	FRG	R/W	Indicates whether the current packet is fragmented.	
25	NAT_ UNSUPPORTED	RO	Indicates an ERROR status for NAT because the packet is unsupported	
			0	Supported packet type
			1	Unsupported packet type; valid only if NAT_STATUS is set to 0 and egress NAT functionality is enabled
24	MORE	R/W	Setting this bit indicates that the buffer is only part of the packet and does not contain the end of packet data. This bit should not be set if NAT/ACL are enabled.	
23:14	RES	WO	Reserved; must be set to 0.	
13:0	PKT_SIZE	R/W	Software writes the number of bytes to transmit into this field. The minimum value for this field is 5 bytes. If the MORE bit is set, then the value written should be a multiple of 4.	

5.3.3 Next Packet Descriptor Address (NEXT_DESCRIPTOR)

Address Offset: 0x8
Access: Read/Write

Bit	Name	Description
31:2	DESCRIPTOR_ADDR	Top 30 bits of Packet the descriptor address. The built-in DMA controller reads this register to discover the location in host memory of the descriptor for the next packet in the sequence. The descriptors should form a closed linked list.
1:0	RES	Ignored by the DMA controller because it is a requirement of the system that all descriptors are 32-bit aligned in host memory. Default is 0.

5.4 NAT LUT Structure: Ingress and Egress

The ingress and egress NAT engines contain a lookup table (LUT) supporting up to 512 entries for ingress and 512 entries for egress and built by sets of KEY+INFO fields. Note:

- The CPU can lookup, insert, or delete an LUT entry, or it can initialize the LUT.
- The rising edge of the REQ is recognized as a new request. Setting the INIT bit initializes whole of the ingress LUT.
- The CPU can add or delete an LUT entry. If the INSERT_STATUS bit is set to one, the insert was successful. If it is unsuccessful, the reason for failure is indicated in BUCKET_FULL or BINS_FULL. It is possible for a particular bin to fill, in which case it is unable to add an LUT entry.

If the entry's KEY that they CPU is trying to add is already present in the LUT, only the INFO field is updated and the bit DUPLICATE_KEY is set in IG_CPU_REQ_STATUS.

Table 5-5 NAT LUT Structure

Ingress		
TCP/UDP Key[19:0] + TCP/UDO Info[100:0]		
KEY+INFO Constituent		
		Registers Used to Program KEY+INFO
KEY[19:0]	1:0	L3_DST_ADDR_ID
	1:0	PRTCL
	15:0	L4_SKTNO
INFO[100:0]	1:0	SW_BITS[1]
	2:0	L4_CONN_STATE
	47:0	L2_MAC_ADDR
	15:0	L4_SEQ_ID
	31:0	LCL_IP_ADDR
ICMP Key[19:0] + ICMP Info[100:0]		
KEY[19:0]	1:0	L3_DST_ADDR_ID
	1:0	PRTCL
	15:0	ICMP_SEQ_ID
INFO[100:0]	1:0	SW_BITS[1]
	2:0	L4_CONN_STATE[2]
	47:0	L2_MAC_ADDR
	15:0	L4_SEQ_ID
	31:0	LCL_IP_ADDR
IG Key[19:0] + IG Info[100:0]		
KEY[19:0]	19:0	IG_KEY_DW0
INFO[100:0]	31:0	IG_INFO_DW0
	31:0	IG_INFO_DW1
	31:0	IG_INFO_DW2
	4:0	IG_INFO_DW3

Egress		
TCP/UDP Key[49:0] + TCP/UDO Info[23:0]		
		Registers Used to Program KEY+INFO
KEY[49:0]	31:0	L3_SRC_ADDR
	1:0	PRTC
	15:0	ICMP_DEQ_ID
INFO[23:0]	0:0	SW_BITS[1]
	4:0	L4_CONN_STATE[2]
	1:0	GLOBAL_IP_INDEX
	15:0	L4_DST_SEQ_NUM
ICMP Key[49:0] + ICMP Info[23:0]		
KEY[49:0]	31:0	L3_SRC_ADDR
	1:0	PRTC
	15:0	ICMP_SEQ_ID
INFO[23:0]	0:0	SW_BITS[1]
	4:0	L4_CONN_STATE[2]
	1:0	GLOBAL_IP_INDEX
	15:0	L4_SEQ_ID
IG Key[19:0] + IG Info[100:0]		
KEY[49:0]	17:0	EG_KEY_DW
	31:0	EG_KEY_DW0
INFO[23:0]	23:0	EG_INFO_DW0

1. Software bits: descriptor fields update with these bits if the current packet hits this LUT entry.
2. Used by the ACL engines to realize the rules based on the L4 connection state. Thus states are hot encoded and software can match it on an per-bit basis.

Each entry has an associated free running ager timer's timestamp field. When an entry is hit, the timestamp for that entry is updated with the current timestamp. Timer resolution is software configurable; hardware periodically scans all entries timestamps, and ages out the ones that exceeded their limits. The LUT is totally configured by the CPU. Entries are added by software as sessions are set up (TCP/UDP/ICMP).

- The CPU uses the register IG_CPU_REQ/EG_CPU_REQ for any LUT operation. The CPU operation results to insert/lookup/delete an entry return using the register IG_CPU_REQ_ STATUS/EG_CPU_REQ_STATUS. Once REQ_DONE is set, it implies the other register fields are valid for the request initiated:

COMMAND[2:0]	INIT	REQ	PKT_TYPE
0b2: Lookup	1: Init LUT	New Request	00: TCP
0b3: Insert			01: UDP
0b4: Delete			02: ICMP

5.5 Hardware Ager: Ingress and Egress

The hardware-based ager counter ticks generate periodically. For every tick, all LUT entries are scanned. If any entry's timestamp is off by more than the specified maximum timeout, it deletes the entry. The deleted entry is logged in a FIFO, which is visible to the CPU through IG_AGER_FIFO/EG_AGER_FIFO. If the FIFO is not empty, the CPU can issue a read to delete the entry KEY in IG_AGER_KEY_DW0/EG_AGER_KEY_DW0. Once ager registers are initialized:

- IG_AGER_TICK/EG_AGER_TICK indicate the of REF_CLK (40 MHz) pulses/ms.
- IG_AGER_TIME_OUT/EG_AGER_TIME_OUT defines the maximum timeout for TCP, UDP, and ICMP separately in terms of IG_AGER_TICK/EG_AGER_TICK.
- The hardware-based AGER can be disabled in bit [0] of IG_AGER_FIFO/EG_AGER_FIFO.
- If more than 4 entries are deleted, an interrupt is generated to the CPU.
- Once an entry is deleted from the LUT, all packets for its KEY send with NAT_STATUS=0.

5.6 Setup and Data/Packet Flow

5.6.1 Ingress

IG_NAT_CSR controls ingress NAT as it has ingress NAT enable, per-field edit enable, data swap, and other ACL global matching rules. Pass unedited fragmented packets to the CPU by setting IG_NAT_FRAG_EDIT to 1 (setting to 0 is not recommended). Software creates the LUT when:

- New TCP connections are established
- An ingress UDP data connection is known
- An ICMP ping request is sent out and packets expected at ingress.

Software sets up the descriptors for Rx packets. Upon receiving a packet:

- Hardware parses and extracts packet fields, forms the KEY, and performs a LUT lookup
- If a lookup results in a hit, INFO is retrieved from the LUT. The packet is edited for the fields that are edit enabled.
- If a lookup results in a miss, hardware updates NAT_STATUS to 0.
- If the packet is fragmented, the FRG bit in the descriptor status word is set.
- If NAT is unsuccessful because the packet is not recognized by hardware, the descriptor status word bit NAT_UNSUPPORTED sets.

Software looks at the descriptor status field once it detects the ownership (OWN) bit cleared, it looks at the status fields to decide whether software-based NAT is needed or if hardware has already done NAT for this packet.

- If the NAT_STATUS bit is set, the hardware NAT was successful.
- If the NAT_STATUS bit is not set, software must do the NAT for this packet.
  - If FRG is set, the packet was fragmented.
  - If NAT_UNSUPPORTED is set, hardware did not recognize the packet type. If it is 0, this packet had no NAT entry. The CPU processes the packet then builds the NAT table if necessary (e.g., for unprogrammed entries when too many sessions are in progress).
  - If PER_PKT_INTR_EN is set, it causes an interrupt to the CPU once the packet is sent to the DDR.

5.6.2 Egress

EG_NAT_CSR controls egress NAT as it has ingress NAT enable, per-field edit enable, data swap, and other ACL global matching rules. By default, ingress NAT edits the fields L2_DST_ADDR, L2_SRC_MAC_ADDR, L3_DST_ADDR, and L4_DST_SOCKET. It also computes and updates incremental CHECKSUM. Because L3_SRC_ADDR is the IP address of this WAN port, it is assumed to be only one of the four values set in the Local Global IP Address 0, 1, 2, 3 registers. These addresses index to 0, 1, 2, and 3 and are is populated by the CPU while adding the entry.

Pass unedited fragmented packets to the CPU by setting EG_NAT_FRAG_EDIT_DISABLE to 1 (setting to 0 is not recommended). Software creates the LUT when:

- New TCP connections are established
- An ingress UDP data connection is known
- An ICMP ping request is sent out and packets expected at ingress.
- Software sets up the Tx packet descriptors. If, while deciding whether to forward to the WAN port, software already knows if the packet is unsupported (e.g. a fragmented or IPv6 packet), it can disable the hardware-based NAT for this packet by setting the bit PER_PKT_NAT_ ENABLE to 0. Otherwise software can blindly the packet to transmit.
- Upon receiving a packet from the DDR, if the PER_PKT_NAT_ENABLE is set:
  - Hardware parses and extracts packet fields, forms the KEY, and performs a LUT lookup
  - If a lookup results in a hit, INFO is retrieved from the LUT. The packet is edited for the fields that are edit enabled.
  - If a lookup results in a miss, hardware updates NAT_STATUS to 0.
  - If the packet is fragmented, the FRG bit in the descriptor status word is set.
  - If NAT is unsuccessful because the packet is not recognized by hardware, the descriptor status word bit NAT_UNSUPPORTED sets.

Software could queue the packet to be transmitted out of the WAN port by default. When the ownership (OWN) bit of the descriptor is cleared by hardware, it can look at the descriptor status word to decide whether software-based NAT is required or hardware has already done NAT for this packet.

- If the NAT_STATUS bit is set (and PER_PKT_NAT_ENABLE was set by the CPU for this packet), the hardware NAT was successful and the packet is sent.
- If PER_PKT_NAT_ENABLE is not set by the CPU, hardware unconditionally transmits the packet.
- If the NAT_STATUS bit is not set (and PER_PKT_NAT_ENABLE is set), the packet is not sent. Hardware just updates the status word of the descriptor and proceeds processing the next packet. In this case, software does the appropriate processing.
  - If either NAT_UNSUPPORTED or FRG is set, software must do the NAT for this packet and requeue this packet with PER_PKT_NAT_ENABLE set to 0.
  - If either NAT_UNSUPPORTED or FRG is not set but NAT_STATUS is 0, then hardware LUT lookup failed for this packet. CPU can check whether an entry must be added. After addition it can requeue this packet.

The descriptor has a per-packet interrupt bit which, if set, causes an interrupt to the CPU once the packet is completely fetched from the DDR and processed by hardware. For example, this bit can be sent every 10 descriptors in a ring to indicate the CPU often, but not every packet.

6 Audio Interface

6.1 Overview

The QCA9558 supports an I^{2}S/SPDIF interface to provide audio functionality. It consists of standard two-channel (stereo) I^{2}S out speaker and an I^{2}S in (microphone) interface, as well as an SPDIF speaker out interface. Figure 6-1 shows a block diagram of the QCA9558 audio interface.

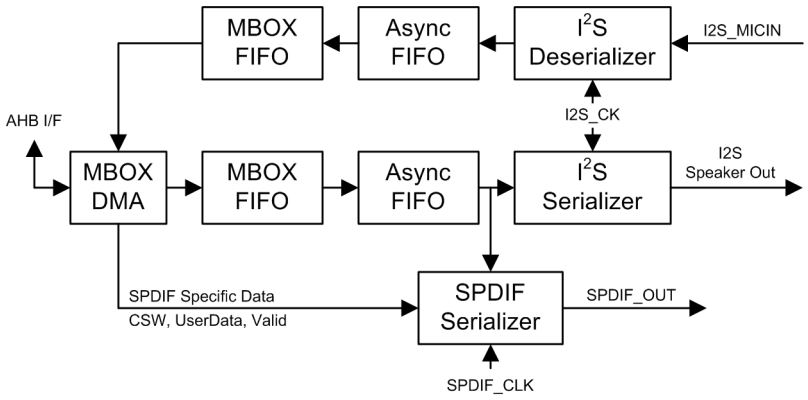


Figure 6-1 Audio Interface

The I^{2}S and SPDIF clocks are generated by the audio PLL block.

6.2 Audio PLL

Figure 6-2 shows the QCA9558 audio PLL block diagram.

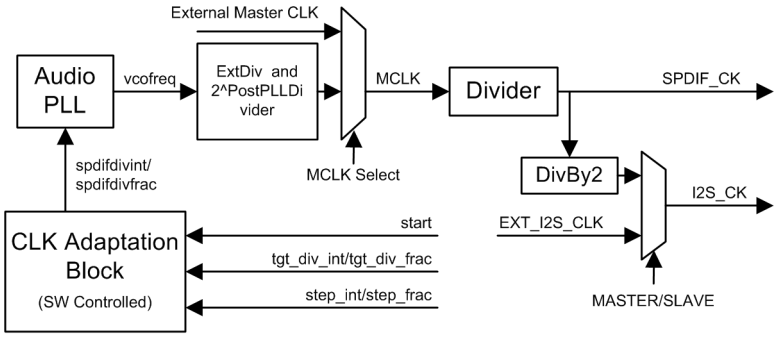


Figure 6-2 Audio PLL Block Diagram

The audio PLL can support generation of all the audio master clock frequencies. It accepts two inputs, SPDIFDIVINT and SPDIFDIVFRAC, which are generated by a clock adaptation module. The clock adaptation module enables slow changing of the audio clock by changing SPDIFDIVINT/SPDIFDIVFRAC in small steps from the current value to a target value. The target TGT_DIV_INT/TGT_DIV_FRAC and step size are software programmable. The clock adaptation module changes the value of the SPDIFDIVINT/SPDIFDIVFRAC values with respect to a slow SPDIFCLKSDM clocks. This small step size ensures that the audio PLL tracks the small variation. The resolution of DIVFRAC ensures that the clock can be varied with steps less than 200 ppb. Following the audio PLL come three dividers: postPLL divider and ExtDiv controlled through the register AUDIO_PLL_CONFIG, PostPLLDivide field, and another posedge divider inside the I^{2}S STEREO_CONFIG register. The final clock relations is:

(40 MHz/3) * (int.frac) = vcofreq
vcofreq/(2^{PostPLLDiv} * ExtDiv) = MCLK
MCLK/posedge = SPDIF_CLK

If the master must be modified from the current value to another value, it is software's responsibility to recompute and program the new TGT_DIV_INT/TGT_DIV_FRAC values.

6.3 I^{2}S Interface

The QCA9558 I^{2}S supports a two-channel digital audio subsystem. This interface uses the I^{2}S pins listed in Table 2-5.

6.3.1 External DAC

An external DAC receives I^{2}S digital audio streams and converts them to analog output to drive speaker or headphones. This stream is PCM data that is serialized and sent with a left channel/right channel select and synchronization signal. The I^{2}S serializer can be set to support a few different I^{2}S data format variants to be compatible with a larger number of external DAC components, including various PCM data word sizes, serialization boundaries, and clocking options.

I^{2}S can also operate in a slave mode where the stereo clock and word select are driven by external master (DAC or external controller). External DAC parts are often controlled by a separate serial 2-wire or 3-wire interface. This interface often controls volume and configuration of the external DAC. This can be attached to the QCA9558 serial interface controllers.

6.3.2 Sample Sizes and Rates

The stereo audio path supports PCM sample sizes of 8, 16, 24, or 32 bits for speaker out and PCM sample sizes of 16 and 32 bits for MICIN. The serializer supports serialization sizes of 16 or 32 bits. The sample size and serialization size need not be the same, LSBs will be padded with 0s. If the QCA9558 is programmed to be a slave, word select and stereo clock (the bit clock) are inputs from the external DAC/ADC.

Along with configuration information, a sample counter provides the number of samples transmitted per second through the I^2S SpeakerOut interface. This sample counter can be used and cleared by software as required.

6.3.3 Stereo Software Interface

To play music, software configures the stereo subsystem and sends interleaved (LRLR....) PCM data to the mailbox DMA. To record music, software configures the stereo subsystem and the PCM samples (interleaved) are written into the memory.

PIO or DMA Mode

To send data PCM samples on the I^2S interface:

1. Program GPIO Function (GPIO_FUNCTION) register to enable I^2S (I2S0, I2S1, or both).
2. Program the Configure Stereo Block (STEREO_CONFIG) register to enable the stereo.
3. Configure other parameters. For example, sample size, word size, mono/stereo mode, master/slave mode, CLK divider (if the QCA9558 is master), and so on.
4. Issue a stereo reset (bit [23] of Configure Stereo Block (STEREO_CONFIG)).
5. Write the PCM samples (a byte per write) to MBOX FIFO (MBOX_FIFO) register if the FIFO is not full. FIFO status can be learned from Non-Destructive FIFO Status Query (MBOX_FIFO_STATUS) register. This data is written into the MBOX FIFO, which is a four-word register where each word corresponds to each channel.

To receive data PCM samples:

1. Program the GPIO Function (GPIO_FUNCTION) register to enable I^2S (I2S0, I2S1, or both).
2. Program Configure Stereo Block (STEREO_CONFIG) register to enable the stereo.
3. Issue a MICIN reset to reset Micin buffers.
4. Configure other parameters. For example, sample size, word size, mono/stereo mode, master/slave mode, CLK divider (if the QCA9558 is master), and so on.
5. Issue a stereo reset (bit [23] of Configure Stereo Block (STEREO_CONFIG)).
6. Read the PCM samples (a byte per read) to MBOX FIFO (MBOX_FIFO) register if the FIFO is not empty. FIFO status can be learnt from Non-Destructive FIFO Status Query (MBOX_FIFO_STATUS) register.

MicIn Slave Mode

- WS is asserted only for the appropriate number of bit-times.
- The stereo block pads the remaining bits of a 32-bit word with all zeros.
- A 32-bit DMA write to memory occurs for each sample irrespective of the sample size used.
- Software must take care of ignoring the padded zeros depending on the sample size.

SpkrOut Slave Mode

- WS is asserted only for the appropriate number of bit-times.
- The stereo block expects samples to be packed in memory without any padded zeros. For example, for an 8-bit sample size, a 32-bit word in memory should contain four 8-bit samples. For a 24-bit sample, a 32-bit word contains the 24 bits of the first sample and 8 bits of the next.
- Software shall provide the packed data in the memory without any padded zeros.

MicIn Master Mode

- WS is always asserted for 32-bit time period irrespective of sample size.
- The stereo block expects the samples to be driven on the I2SMICIN with the padded zeros to form the 32 bit-time of WS line.
- The stereo block performs a DMA write of the entire 32-bit word (with the padded zeros received) to memory.
- Software should unpack and ignore the padded zeros depending on the sample size.

SpkrOut Master Mode

- WS is always asserted for 32-bit time period irrespective of the sample size.
- The stereo block expects the samples to be packed in memory without padded zeros. For example, for an 8-bit sample size, a 32-bit word in memory should contain four 8-bit samples. For a 24-bit sample, a 32-bit word contains the 24 bits of the first sample and 8 bits of the next.
- The stereo block inserts extra zeros in I2S_SD_OUT to make the 32 bit-time of the WS line.
- Software shall provide the packed data in the memory without any padded zeros.

6.4 SPDIF INTERFACE

The SPDIF interface operates on the same sample as I^2S, so it always in sync with audio played on the I^2S interface. All configuration information to the SPDIF block, such as sampling frequency, sample size, word size, and so on, are inherited from the programming of the I^2S interface.

6.5 Mailbox (DMA Controller)

A four channel MBOX DMA controller is used in the QCA9558 for I^2S and SLIC interfaces. All four duplex channels can operate simultaneously. Channels 0 and 2 are dedicated to I^2S0 and I^2S1, respectively. Channels 1 and 3 are dedicated to SLIC slots 0 and 1, respectively.

6.5.1 Mailboxes

The QCA9558 supports four full duplex mailboxes to move data between the QCA9558 and the audio interfaces I^2S and SLIC. Flow control of the four mailboxes must be managed by software.

6.5.2 MBOX DMA Operation

The QCA9558 MBOX DMA engine has four channels for Tx and one channel for Rx. When multiple channels are active, arbitration for the AHB and memory resource is round robin. See Figure 6-3.

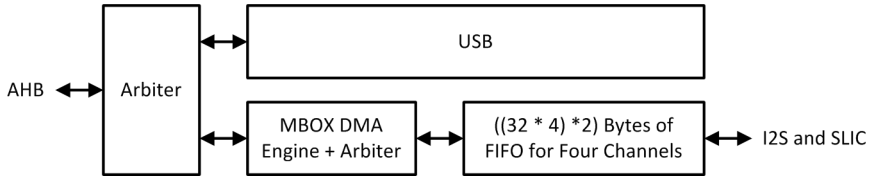


Figure 6-3 MBOX DMA Interface

Each mailbox DMA channel follows a list of linked descriptors, as shown in Figure 6-4 and Table 6-1.

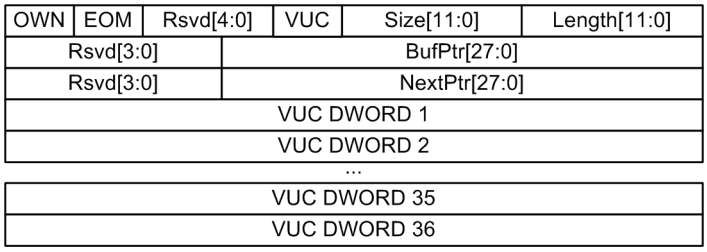


Figure 6-4 DMA Descriptor Structure

Table 6-1 Descriptor Fields

Name	Bits	Description
Length	12	Length of data in memory buffer. If EOM=0, the Length = Size.
Size	12	Size of memory buffer.
VUC	1	When this bit set, the SPDIF block uses the VUC data for the audio block fetched from the previous descriptor.
EOM	1	End of message indicator.
OWN	1	Descriptor is owned by the CPU or DMA engine. (If set, it is owned by the DMA engine).
BufPtr	28	Points to memory buffer pointer. Byte aligned address.
NextPtr	28	Points to next descriptor in the list. Must be word aligned.
VUC DWORD 1 to 36	36 * 32 bits	These are the VUC data for each audio block of the SPDIF. 192 Bits each of Valid, UserData and Channel Status Word for two channels of audio corresponds to 36 Dwords. These data are SPDIF specific and software does not need to provide this data if I^2S is the only active interface and SPDIF is disabled.

Once the DMA engine is started, it follows its descriptor chain until it arrives at a descriptor that has its owner bit set to CPU (bit [31] of the status word is not set). The DMA engine then stops until the CPU restarts it.

The DMA control registers include stop and start commands, a programmable descriptor chain base address, DMA policies to use, and so on. DMA status registers inform the CPU when the engine is running, done, or has encountered an error. See the MBOX Registers.

6.5.3 Software Flow Control

To configure the MBOX channel to send data from the QCA9558 (Rx as referred in MBOX):

1. Set up the MBOX Rx descriptors. Set the owner to indicate it is owned by the DMA controller. Hardware resets this once DMA is complete.
2. Load the corresponding buffers with the data to transmit.
3. Program the register MBOX0 Tx DMA Descriptors Base Address (MBOX0_DMA_TX_DESCRIPTOR_BASE) with the base descriptor address.
4. Reset the corresponding MBOX FIFO.
5. Enable the DMA by setting the START bit in the MBOX0 Rx DMA Control (MBOX0_DMA_RX_CONTROL) register. This register has a provision to stop and resume at any time.
6. On DMA completion, the RX_DMA_COMPLETE interrupt is asserted.

To configure the MBOX channel for the QCA9558 to receive data (Tx as referred in MBOX):

1. Set up the MBOX Tx descriptors. The owner should be set to indicate it is owned by the DMA controller. Hardware resets this once DMA is complete.
2. Program the register MBOX0 Tx DMA Descriptors Base Address (MBOX0_DMA_TX_DESCRIPTOR_BASE) with the base descriptor address.
3. Reset the corresponding MBOX FIFO.
4. Enable the DMA by setting START bit in MBOX0 Tx DMA Control (MBOX0_DMA_TX_CONTROL) register. This register has a provision to stop and resume at any time.
5. On DMA completion, the TX_DMA_COMPLETE interrupt is asserted.

6.5.4 Mailbox Error Conditions

If flow control synchronization is lost for any reason, these mailbox error conditions could arise:

Tx Mailbox Overflow	If no DMA descriptors are available on the QCA9558 Tx side, but an message is coming in from the corresponding interface, the Tx mailbox stalls the host physical interface. If the host interface remains stalled with the Tx FIFO full for a timeout period specified other than FIFO_TIMEOUT, a timeout error occurs. An interrupt is sent to CPU. As long as the host status overflow bit is set, any mailbox Tx bytes that arrive from the host when the mailbox is full are discarded. When the host clears the overflow interrupt, mailbox FIFOs return to normal operation. Software must then either resynchronize flow control state or reset the QCA9558 to recover.
Rx Mailbox Underflow	If I^2S reads a mailbox that does not contain any data and this condition persists for more than a timeout period, the CPU is sent an underflow error interrupt. As long as status underflow bit is set, any mailbox reads which arrive when the mailbox is empty return garbage data. Software must then either resynchronize flow control state or reset the QCA9558 to recover.

6.5.5 MBOX-Specific Interrupts

All MBOX specific interrupts can be masked by control registers (MBOX Related Interrupt Enables (MBOX_INT_ENABLE)).

MBOX sends an interrupt to MIPS in these cases (if they are enabled):

- Tx DMA complete, Rx DMA complete
- Tx overflow, Tx not empty (incoming traffic)
- Rx underflow, Rx not full (outgoing traffic)
- MBOX Tx DMA EOM complete interrupt

The status of these interrupts can be read from the MBOX Related Interrupt Status (MBOX_INT_STATUS) register.

7 WLAN Medium Access Control (MAC)

7.1 Overview

The WLAN MAC consists of the following major functional blocks: 10 queue control units (QCUs), 10 distributed coordination function (DCF) control units (DCUs), a single DMA Rx unit (DRU), and a single protocol control unit (PCU). See Figure 7-1.

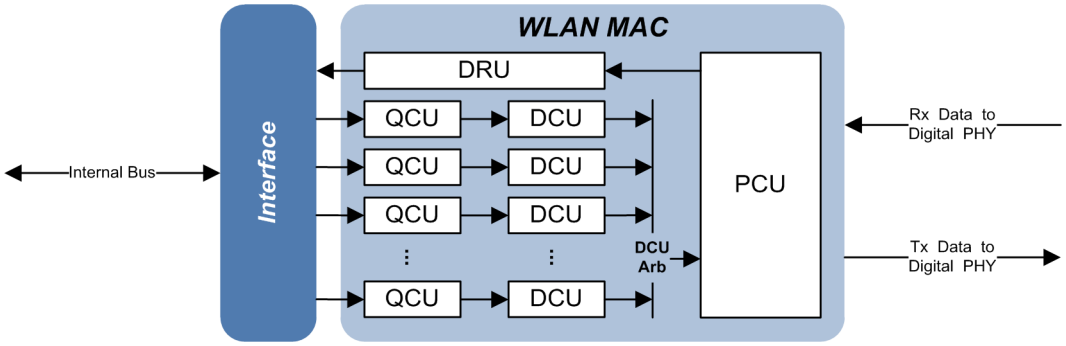


Figure 7-1 WLAN MAC Block Diagram

The WLAN MAC block supports full bus-mastering descriptor-based scatter/gather DMA. Frame transmission begins with the QCUs. QCUs manage the DMA of frame data from the host through the PCIE interface, and determines when a frame is available for transmission.

Each QCU targets exactly one DCU. Ready frames are passed from a QCU to its targeted DCU. The DCU manages the enhanced distributed coordination function (EDCF) channel access procedure on behalf of the QCUs associated with it.

Functionality of the WLAN MAC block includes:

- Tx frame data transfer from the DDR
- Rx frame data transfer to the DDR
- Interrupt generation and reporting
- Sleep-mode sequencing
- Miscellaneous error and status reporting functions

Once the DCU gains access to the channel, it passes the frame to the PCU, which encrypts the frame and sends it to the baseband logic. The PCU handles both processing responses to the transmitted frame, and reporting the transmission attempt results to the DCU.

Frame reception begins in the PCU, which receives the incoming frame bitstream from the digital PHY. The PCU decrypts the frame and passes it to the DRU, which manages Rx descriptors and writes the incoming frame data and status.

7.2 Descriptor

The WLAN MAC is responsible for transferring frames between the DDR and the digital PHY. For all normal frame transmit/receive activity, the CPU provides a series of descriptors to the WLAN MAC, and the WLAN MAC then parses the descriptors and performs the required set of data transfers.

7.3 Descriptor Format

The transmit (Tx) descriptor format contains twenty-three 32-bit words and the receive (Rx) descriptor contains twelve 32-bit words.

A descriptor must be aligned on a 32-bit boundary in host memory, although best performance is achieved if the descriptor is aligned on a cache-line boundary. The MAC uses the final nine words of the Tx descriptor and the twelve words of the Rx descriptor to report status information back to the host.

See these tables for more information:

Table	Words	Description
Table 7-1	0–14	Tx descriptor format
Table 7-4	15–22	Tx descriptor format
Table 7-5	0–8	Tx descriptor status format
Table 7-6	0–11	Rx descriptor format

The Tx descriptor format is described in Table 7-1. With certain exceptions as noted, all Tx descriptor fields must be valid in the first descriptor of a non-aggregate frame. The fields for all following descriptors are ignored. For aggregate frames only the first descriptor of the first frame of the aggregate is valid. The fields for all following descriptors are ignored.

Table 7-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
0	31:16	atheros_id	The unique Qualcomm Atheros identifier of 0x168C is used to visually identify the start of the descriptor.
	15	desc_tx_rx	Indicates whether the descriptor is a transmit or receive descriptor. The value should be set to 1 indicating transmit.
	14	desc_ctrl _stat	Indicates whether the descriptor is a control or status descriptor. The value should be set to 1 indicating control descriptor.
	13:12	RES	Reserved
	11:8	tx_qcu_num	Tx QCU number Indicates which QCU this descriptor is part of.
	7:0	desc_length	Descriptor length Indicates the number of Dwords in this descriptor. The value should be set to 0x17 (23 Dwords).
1	31:0	link_ptr	Link pointer address Contains the 32-bit next descriptor pointer. Must be 32-bit aligned (bits [1:0] must be 0). A null value: (link_ptr= 0x0) is only allowed at the end of a non-aggregate or non-RIFS packet. If the packet is part of an aggregate or RIFS burst, a null is only allowed on the last descriptor of the last packet. A legal null value causes the QCU to stop. Must be valid for all descriptors.
2	31:0	buf_ptr0	Data buffer pointer 0 Contains the 32-bits address of the first data buffer associated with this descriptor. A transmit data buffer may begin at any byte address. Must not be null (buf_ptr0 = 0x0) for all descriptors.
3	31:28	RES	Reserved

	27:16	buf_len0	Data buffer length associated with data buffer pointer 0. Specifies the length, in bytes, of the data buffer associated with buf_ptr0. buf_len0 must not be 0. Note: This field must be valid for all descriptors.
			`case (header_length, qos packet) {`
			`  24, no : pad_length = 0;`
			`  24, yes: pad_length = 2;`
			`  30, no : pad_length = 2;`
			`  30, yes: pad_length = 0;`
			`}`
			`case (encrypt_type) {`
			`  wep  : icv_length = 4;`
			`  tkip nomic : icv_length = 4;`
			`  aes  : icv_length = 8;`
			`  tkip : icv_length = 12;`
			`  wapi : icv_length = 16;`
			`}`
			`fcs_length = 4;`
			`frame_length = buf_len0 + buf_len1 + buf_len2 + buf_len3 +`
			`  icv_length + fcs_length - pad_length`

	15:0	RES	Reserved
4	31:0	buf_ptr1	Data buffer pointer 1 Contains the 32-bits address of the second data buffer associated with this descriptor. A transmit data buffer may begin at any byte address. Only valid if buf_ptr0 is not null.

Table 7-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
5	31:28	RES	Reserved
	27:16	buf_len1	Data buffer length associated with data buffer pointer 1. buf_len1 can only be 0 if and only if buf_ptr1 is null. See buf_len0 for details.
	15:0	RES	Reserved
6	31:0	buf_ptr2	Data buffer pointer 2 Contains the 32-bits address of the third data buffer associated with this descriptor. A transmit data buffer may begin at any byte address. Only valid if buf_ptr0 and buf_ptr1 are not null.
7	31:28	RES	Reserved
	27:16	buf_len2	Data buffer length associated with data buffer pointer 2. buf_len2 can only be 0 if and only if buf_ptr2 is null. See buf_len0 for details.
	15:0	RES	Reserved
8	31:0	buf_ptr3	Data buffer pointer 3 Contains the 32-bits address of the third data buffer associated with this descriptor. A Tx data buffer may begin at any byte address. Only valid if buf_ptr0, buf_ptr1, and buf_ptr2 are not null.
9	31:28	RES	Reserved
	27:16	buf_len3	Data buffer length associated with data buffer pointer 2. buf_len2 can only be 0 if and only if buf_ptr3 is null. See buf_len0 for details.
	15:0	RES	Reserved
10	31:16	tx_desc_id	Tx descriptor sequence number Software will select a unique sequence number associated with this descriptor. This value is copied to the tx_desc_id in the transmit status.

	15:0	ptr_checksum	Memory pointer checksum
			Verifies the integrity of the memory pointers/addresses in this descriptor. The equation looks like this:
			`checksum[31:0] = TXC[0]+TXC[1]+TXC[2]+TXC[3]+TXC[4]+`
			`TXC[5]+TXC[6]+TXC[7]+TXC[8]+TXC[9];`
			`ptr_checksum[15:0] = checksum[31:16] + checksum[15:0];`
			
			The carry bits above the MSB of the checksum or ptr_checksum will disappear.

Table 7-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
11	31	cts_enable	Self-CTS enable Precedes the frame with CTS flag. If set, the PCU first sends a CTS before sending the frame described by the descriptor; used mainly for 802.11g frames to quiet legacy stations before sending a frame the legacy stations cannot interpret, even at the PHY level. At most only one of the rts_enable and cts_ enable bits may be set; it is illegal to set both.
	30	dest_index _valid	Destination index valid flag Specifies whether the contents of the DestIdx field are valid.
	29	int_req	Interrupt request flag Set to one by the driver to request that the DMA engine generate an interrupt upon completion of the frame to which this descriptor belongs. Note: This field must be valid and identical for all descriptors of the frame. That is, all descriptors for the frame must have this flag set, or all descriptors for the frame must have this flag clear.
	28:25	beam_form	Tx beamforming in series 0–3. If this value is set, the current packet carries an array V before MPDU in the current Tx series. Bit [28]: For Tx series 3 Bit [27]: For Tx series 2 Bit [26]: For Tx series 1 Bit [25]: For Tx series 0
	24	clear_dest _mask	Clear destination mask bit flag If set, instructs the DCU to clear the destination mask bit at the index specified by the dest_index field.
	23	VEOL	Virtual end-of-list flag When set, indicates that the QCU should act (mostly) as if this descriptor had a null link_ptr, even though its link_ptr field may be non-null. Note: This field must be valid in the final descriptor of a frame and must be clear for all other descriptors of the frame.
	22	rts_enable	RTS enable If set, the PCU transmits the frame using the RTS/CTS protocol. If clear, the PCU transmits the frame without transmitting a RTS. At most only one of the rts_enable and cts_enable bits may be set; it is illegal to set both.
	21:16	TPC_0	TPC for Tx series 0. These bits pass unchanged to the baseband, where they control Tx power for the frame.
	15	clear_retry	Setting this bit disables the retry bit from being set in the Tx header on a frame retry; applies to both aggregate and non-aggregate frames.
	14	low_rx_chain	When set to 1, indicates that switches the Rx chain mask to low power mode after transmitted this frame.
	13	fast_ant _mode	Fast antenna mode If set to 0, this means that this Tx frame to use the omni antenna mechanism. if set to 1, then the opposite omni antenna should be used.
	12	VMF	Virtual more fragment If this bit is set, bursting is enabled for this frame. If there is no burst in progress, it will initiate a CTS protected burst if cts_enable is set. If there is a previous burst in progress, it ignores the cts_enable bit assuming that this burst is protected.
	11:0	frame_length	Frame length Specifies the length, in bytes, of the entire MAC frame, including the FCS, IC, and ICV fields.

Table 7-1 Tx Descriptor Format: Words 0–14

<table>
<tr><th>Word</th><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="15">12</td><td>31</td><td>MORE_RIFS</td><td>More RIFS burst flag; When set, indicates that the current packet is not the last packet of an aggregate. All descriptors for all packets of a RIFS burst except the descriptors of the last packet must have this bit set. All descriptors of the last packet of a RIFS burst must have this bit clear.</td></tr>
<tr><td>30</td><td>IS_AGG</td><td>This packet is part of an aggregate flag. All descriptors of the all packets in an aggregate must have this bit set.</td></tr>
<tr><td>29</td><td>MORE_AGG</td><td>More aggregate flag; When set, indicates that the current packet is not the last packet of an aggregate. All descriptors for all packets of an aggregate except the descriptors of the last packet must have this bit set. All descriptors of the last packet of an aggregate must have this bit clear.</td></tr>
<tr><td>28</td><td>ext_and_ctl</td><td>Extension and control channel enable
Only four combinations are allowed; otherwise desc_config_error asserts. When neither ext_only nor ext_and_ctl are set, the RTS/CTS and data frame is sent based on the bandwidth: HT20 when 20_40 is set to 0 and HT40 shared when 20_40 is set to 1 (RTS/CTS frames are sent at in HT40 duplicate mode if 20_40 is set to 1). When ext_and_ctl is set the RTS/CTS and data frame is sent at HT40 duplicate. When ext_only is set the RTS/CTS and data frame is sent out in HT20 extension channel mode.
<table>
<tr><th>ETX_AND_CTL</th><th>20_40</th><th>DATA</th><th>RTS/CTS</th></tr>
<tr><td>0</td><td>0</td><td>HT20 Control</td><td>HT20 Control</td></tr>
<tr><td>0</td><td>1</td><td>HT40 Shared</td><td>HT40 Duplicate</td></tr>
<tr><td>1</td><td>1</td><td>HT40 Duplicate</td><td>HT40 Duplicate</td></tr>
</table></td></tr>
<tr><td>27</td><td>RES</td><td>Reserved</td></tr>
<tr><td>26</td><td>corrupt_fcs</td><td>Corrupt packet FCS; When set, the FCS of the packet will be inverted to guarantee the transmitted FCS is incorrect.</td></tr>
<tr><td>25</td><td>RES</td><td>Reserved</td></tr>
<tr><td>24</td><td>NO_ACK</td><td>No ACK flag; When set, indicates to the PCU that it should not expect to receive (and should not wait for) an ACK for the frame. Must be set for any frame with the 802.11 NoACK bit set in the QoS field. Also must be set for all other frame types (such as beacons and other broadcast/multicast frames) that do not receive ACKs.</td></tr>
<tr><td>23:20</td><td>FRAME_TYPE</td><td>Frame type indication; indicates what type of frame is being sent:
<table>
<tr><td>15:5</td><td>Reserved</td></tr>
<tr><td>4</td><td>Probe response</td></tr>
<tr><td>3</td><td>Beacon</td></tr>
<tr><td>2</td><td>PS-Poll</td></tr>
<tr><td>1</td><td>ATIM</td></tr>
<tr><td>0</td><td>Frame type, other than the types listed in [15:1]</td></tr>
</table></td></tr>
<tr><td>19:13</td><td>DEST_INDEX</td><td>Destination table index
Specifies an index into an on-chip table of per-destination information. The PCU fetches the encryption key from the specified index in this table and uses this key to encrypt the frame. The DMA logic uses the index to maintain per-destination transmit filtering status and other related information.</td></tr>
<tr><td>12</td><td>MORE</td><td>More descriptors in this frame flag
Set to one by the driver to indicate that there are additional descriptors (that is, DMA fragments) in the current frame. The last descriptor of a packet must have this bit set to 0. Note: This field must be valid for all descriptors.</td></tr>
<tr><td>11:9</td><td>PA</td><td>Pre-distortion chain mask</td></tr>
<tr><td>8:0</td><td>RES</td><td>Reserved</td></tr>
</table>

Table 7-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
13	31:28	TX_TRIES3	Number of frame data exchange attempts permitted for Tx series 3. A value of zero means skip this transmission series.
	27:24	TX_TRIES2	Number of frame data exchange attempts permitted for Tx series 2. A value of zero means skip this transmission series.
	23:20	TX_TRIES1	Number of frame data exchange attempts permitted for Tx series 1. A value of zero means skip this transmission series.
	19:16	TX_TRIES0	Number of frame data exchange attempts permitted for Tx series 0. A frame data exchange attempt means a transmission attempt in which the actual frame is sent on the air (in contrast to the case in which the frame has RTS enabled and the RTS fails to receive a CTS. In this case, the actual frame is not sent on the air, so this does not count as a frame data exchange attempt. Unlike TX_TRIES1...3, a value of zero is illegal for TX_TRIES0 field.
	15	DUR_UPDATE_EN	Frame duration update control. If set, the MAC updates (overwrites) the duration field in the frame based on the current transmit rate. If clear, the MAC does not alter the contents of the frame duration field.
	14:0	BURST_DURATION	Burst duration value in usec. If this frame is not part of a burst or the last frame in a burst, this value should be zero. In a burst, this value is the amount of time to be reserved (via NAV) after the completion of the current transmit packet sequence (after the ACK if applicable).
14	31:24	tx_rate3	Tx rate for transmission series 3; see Table 7-2 and Table 7-3
	23:16	tx_rate2	Tx rate for transmission series 2; see Table 7-2 and Table 7-3
	15:8	tx_rate1	Tx rate for transmission series 1; see Table 7-2 and Table 7-3
	7:0	tx_rate0	Tx rate for transmission series 0; see Table 7-2 and Table 7-3

Table 7-2 MAC Rate Encodings

MAC Rate Encoding	Protocol
0x01	Reserved
0x02	
0x03	
0x06	
0x07	
0x8	OFDM_48Mb
0x9	OFDM_24Mb
0xA	OFDM_12Mb
0xB	OFDM_6Mb
0xC	OFDM_54Mb
0xD	OFDM_36Mb
0xE	OFDM_18Mb
0xF	OFDM_9Mb
0x18	CCK_11Mb_L
0x19	CCK_5_5Mb_L
0x1A	CCK_2Mb_L
0x1B	CCK_1Mb_L
0x1C	CCK_11Mb_S
0x1D	CCK_5_5Mb_S
0x1E	CCK_2Mb_S

Table 7-3 Tx Rates[1]

Rate	Desc	Stream	HT20; GI= 0 Mbps	HT20; GI = 1 Mbps	HT40; GI= 0 Mbps	HT40; GI= 1 Mbps
0x80	MCS 0	1	6.5	7.2	13.5	15
0x81	MCS 1	1	13	14.4	27	30
0x82	MCS 2	1	19.5	21.7	40.5	45
0x83	MCS 3	1	26	28.9	54	60
0x84	MCS 4	1	39	43.3	81	90
0x85	MCS 5	1	52	57.8	108	120
0x86	MCS 6	1	58.5	65.0	121.5	135
0x87	MCS 7	1	65	72.2	135	150
0x88	MCS 8	2	13	14.4	27	30
0x89	MCS 9	2	26	28.9	54	60
0x8A	MCS 10	2	39	43.3	81	90
0x8B	MCS 11	2	52	57.8	108	120
0x8C	MCS 12	2	78	86.7	162	180
0x8D	MCS 13	2	104	115.6	216	240
0x8E	MCS 14	2	117	130.0	243	270
0x8F	MCS 15	2	130	144.4	270	300
0x90	MCS 16	3	19.5	21.7	40.5	45
0x91	MCS 17	3	39	43.3	81	90
0x92	MCS 18	3	58.5	65	121.5	135
0x93	MCS 19	3	78	86.7	162	180
0x94	MCS 20	3	117	130	243	270
0x95	MCS 21	3	156	173.3	324	360
0x96	MCS 22	3	175.5	195.0	364.5	405
0x97	MCS 23	3	195.0	216.7	405	450

1. All rates not listed are reserved. Note that for short guard interval (GI=1), HT20 mode is allowed.

The Tx descriptor format for words 15 through 22 is described in Table 7-4.

Table 7-4 DMA Tx Descriptor Format for Words 15-22

Word	Bits	Name	Description	
15	31	rts_cts _qual1	Qualifies rts_enable or cts_enable in the Tx descriptor for Tx series 1	
			1	Default behavior with respect to rts_enable and cts_enable
	30:16	PACKET _DURATION1	Packet duration 1 (in µs); Duration of the actual Tx frame associated with TXRate1. This time does not include RTS, CTS, ACK, or any associated SIFS.	
	15	RTS_CTS _QUAL0	Qualifies rts_enable or cts_enable in the Tx descriptor for Tx series 0	
			1	Default behavior with respect to rts_enable and cts_enable
	14:0	PACKET _DURATION0	Packet duration 0 (in µs); Duration of the actual Tx frame associated with TXRate0. This time does not include RTS, CTS, ACK, or any associated SIFS.	
16	31	RTS_CTS _QUAL3	Qualifies rts_enable or cts_enable in the Tx descriptor for Tx series 3	
			1	Default behavior with respect to rts_enable and cts_enable
	30:16	PACKET _DURATION3	Packet duration 3 (in µs); Duration of the actual Tx frame associated with TXRate3. This time does not include RTS, CTS, ACK, or any associated SIFS.	
	15	RTS_CTS _QUAL2	Qualifies rts_enable or cts_enable in the Tx descriptor for Tx series 2	
			1	Default behavior with respect to rts_enable and cts_enable
	14:0	PACKET _DURATION2	Packet duration 2 (in µs); Duration of the actual Tx frame associated with TXRate2. This time does not include RTS, CTS, ACK, or any associated SIFS.	
17	31	RES	Reserved	
	30	CALIBRATING	Calibrating indication; causes the BB to apply the correct MCSD PPDU, which is used for radio calibration.	
	29	DC_AP _STA_SEL	Select for remaining the TBTT between TSF and TSF2, where 0 is from TSF and 1 is from TSF2. Should be used only when both ap_sta_enable and txop_tbtt_limit_ enable are enabled.	
	28:26	ENCRYPT_ TYPE	Encryption type; DMA engine must add the number of necessary extra Dwords at the end of a packet to account for the encryption ICV generated by hardware. The encrypt type fields must be valid for all descriptors.	
			0	None; 0 pad bytes
			1	WEP or TKIP (no MIC); 4 pad bytes
			2	AES; 8 pad bytes
			3	TKIP; 12 pad bytes
			4	WAPI; 16 pad bytes
			7:5	Reserved
	25:18	PAD_DELIM	Pad delimiters; Between each packet of an A-MPDU aggregate the hardware will insert a start delimiter which includes the length of the next frame. Sometimes hardware on the transmitter or receiver requires some extra time between packets which can be satisfied by inserting zero length delimiters. This field indicates the number of extra zero length delimiters to add.	
	17:16	RES	Reserved	

	15:0	AGG_LENGTH	Aggregate (A-MPDU) length; the aggregate length is the number of bytes of the entire aggregate. This length should be computed as:
			`delimiters = start_delim + pad_delim;`
			`frame_pad = (frame_length % 4) ? (4 - (frame_length % 4)) : 0`
			`agg_length = sum_of_all (frame_length + frame_pad + 4 * delimiters)`
			For the last packet of an aggregate the FRAME_PAD = 0 and delimiter= 0, frame_ pad aligns to the next delimiter to be Dword aligned. Each delimiter is 4 bytes long. PAD_DELIM is the number of zero-length delimiters used to introduce an extra time gap between packets. START_DELIM is always 1 and includes the length of the next packet in the aggregate.	

Table 7-4 DMA Tx Descriptor Format for Words 15-22 (cont.)

Word	Bits	Name	Description	
18	31:28	STBC	STBC settings for all four series. If bit [0] is set, STBC is enabled for Tx series 0...3. Only supported for single stream rates, so only the lower bit is set.	
	27:20	RTS_CTS_ RATE	RTS or self-CTS rate selection. Specifies the rate the RTS sends at if rts_enable is set, or self CTS sends at if cts_enable is set; see Table 7-3.	
	19:17	CHAIN_SEL_3	Chain select for Tx series 3. 1 and 3 are the only valid values.	
	16	GI_3	Guard interval control for Tx series 3	
			0	Normal guard interval
			1	Short guard interval
	15	20_40_3	20_40 control for Tx series 3	
			0	HT20 Tx packet
			1	HT40 Tx packet
	14:12	CHAIN_SEL_2	Chain select for Tx series 2; 1, 5, and 7 are the only valid values	
	11	GI_2	Guard interval control for Tx series 2	
	10	20_40_2	20_40 control for Tx series 2	
	9:7	CHAIN_SEL_1	Chain select for Tx series 1; 1, 5, and 7 are the only valid values	
	6	GI_1	Guard interval control for Tx series 1	
	5	20_40_1	20_40 control for Tx series 1	
	4:2	CHAIN_SEL_0	Chain select for Tx series 0; 1, 5, and 7 are the only valid values	
	1	GI_0	Guard interval control for Tx series 0	
	0	20_40_0	20_40 control for Tx series 0	
19	31:30	NESS_0	Number of Extension Spatial Streams (NESS) field of HT-SIG for Tx series 0. This setting is valid when the Tx rate is HT rate.	
			0	No Extension HTLTF is transmitting PPDU
			1	One Extension HTLTF is transmitting PPDU
	29	NOT _SOUNDING	Not sounding HT-SIG field; sends sounding PPDU in explicit feedback as BF. If rts_enable is set to 1, this field affects RTS only, not the next data frame.	
			0	The PPDU is a sounding PPDU
			1	The PPDU is not a sounding PPDU
	28	RTS_HTC_TRQ	Sounding request of RTS frame; available when rts_enable is set to 1.	
			0	The responder is not requested to transmit a sounding PPDU
			1	Request the responder to transmit a sounding PPDU
	27	RTS_HTC_ MRQ	MCS request of RTS frame; available when rts_enable is set to 1	
			0	No MCS feedback is requested
			1	MCS feedback is requested
	26:24	RTS_HTC_MSI	MCS Request Sequence Identifier (MSI) of RTS frame	
			0	Reserved
			1	Contains a sequence number (0–6) to identify the specific request
	23:0	ANTENNA_0	Antenna switch for Tx series 0	
20	31:30	NESS_1	NESS field of HT-SIG for Tx series 1. This setting is valid when the transmission rate is HT rate.	
			0	No Extension HTLTF is transmitting PPDU
			1	One Extension HTLTF is transmitting PPDU
	29:24	TPC_1	TPC for Tx series 1. These bits pass unchanged to the baseband, where they control Tx power for the frame.	
	23:0	ANTENNA_1	Antenna switch for Tx series 1	

Table 7-4 DMA Tx Descriptor Format for Words 15-22 (cont.)

Word	Bits	Name	Description	
21	31:30	NESS_2	NESS field of HT-SIG for Tx series 2. This setting is valid when the transmission rate is HT rate.	
			0	No Extension HTLTF is transmitting PPDU
			1	One Extension HTLTF is transmitting PPDU
	29:24	TPC_2	TPC for Tx series 2. These bits pass unchanged to the baseband, where they control Tx power for the frame.	
	23:0	ANTENNA_2	Antenna switch for Tx series 2	
22	31:30	NESS_3	NESS field of HT-SIG for Tx series 3. This setting is valid when the transmission rate is HT rate.	
			0	No Extension HTLTF is transmitting PPDU
			1	One Extension HTLTF is transmitting PPDU
	29:24	TPC_3	TPC for Tx series 3. These bits pass unchanged to the baseband, where they control Tx power for the frame.	
	23:0	ANTENNA_3	Antenna switch for Tx series 3	

The Tx descriptor status format for words 0 through 8 is described in Table 7-5. The words status is only considered valid when the done bit is set.

Table 7-5 Tx Descriptor Status Format: Words 0-8

Word	Bits	Name	Description
0	31:16	ATHEROS_ID	The unique Qualcomm Atheros identifier of 0x168C is used to visually identify the start of the descriptor.
	15	DESC_TX_RX	Indicates whether the descriptor is a transmit or receive descriptor. The value should be set to 1 indicating transmit.
	14	DESC_CTRL _STAT	Indicates whether the descriptor is a control or status descriptor. The value should be set to 0 indicating status descriptor.
	13:12	RES	Reserved
	11:8	TX_QCU_NUM	Tx QCU number Indicates which QCU this descriptor is part of.
	7:0	DESC_ LENGTH	Descriptor length Indicates the number of Dwords in this descriptor. The value should be set to 0x9 (9 Dwords).
1	31:16	TX_DESC_ID	Tx descriptor sequence number Software will select a unique sequence number associated with this descriptor. This value is copied to the tx_desc_id in the Tx status.
	15:0	RES	Reserved
2	31	RES	Reserved
	30	BA_STATUS	Block ACK status If set, this bit indicates that the BA_BITMAP values are valid.
	29:24	RES	Reserved
	23:16	ACK_RSSI_ ANT02	Rx ACK signal strength indicator of control channel chain 2 A value of 0x80 (–128) indicates an invalid number.
	15:8	ACK_RSSI_ ANT01	Rx ACK signal strength indicator of control channel chain 1 A value of 0x80 (–128) indicates an invalid number.
	7:0	ACK_RSSI_ ANT00	Rx ACK signal strength indicator of control channel chain 0 A value of 0x80 (–128) indicates an invalid number.

Table 7-5 Tx Descriptor Status Format: Words 0-8 (cont.)

Word	Bits	Name	Description
3	31:20	RES	Reserved
	19	TX_TIMER _EXPIRED	Tx timer expired. This bit is set when the Tx frame is taking longer to send to the baseband than is allowed based on the TX_TIMER register. Some regulatory domains require that Tx packets may not exceed a certain amount of Tx time.
	18	RES	Reserved
	17	TX_DATA_ UNDERRUN_ ERR	Tx data underrun error These error conditions occur on aggregate frames when the underrun condition happens while the MAC is sending the data portion of the frame or delimiters.
	16	TX_DELMTR _UNDERRUN_ ERR	Tx delimiter underrun error These error conditions occur on aggregate frames when the underrun conditions happens while the MAC is sending delimiters.
	15:12	VIRTUAL_ RETRY_CNT	Virtual collision count Reports the number of virtual collisions that occurred before transmission of the frame ended. The counter value saturates at 0xF. A virtual collision refers to the case, as described in the 802.11e QoS specification, in which two or more output queues are contending for a TXOP simultaneously. In such cases, all lower-priority output queues experience a virtual collision in which the frame is treated as if it had been sent on the air but failed to receive an ACK.
	11:8	DATA_FAIL_ CNT	Data failure count Reports how many times the actual frame (as opposed to the RTS) was sent but no ACK was received for the final transmission series (see final_tx_index).
	7:4	RTS_FAIL_CNT	RTS failure count Reports the number of times an RTS was sent but no CTS was received for the final transmission series (see the final_tx_index field). For frames that have the rts_enable bit clear, this count always will be zero. Note that this count is incremented only when the RTS/CTS exchange fails. In particular, this count is not incremented if the RTS/CTS exchange succeeds but the frame itself fails because no ACK was received.
	3	FILTERED	Frame transmission filter indication If set, indicates that the frame was not transmitted because the corresponding destination mask bit was set when the frame reached the PCU or if the frame violated TXOP on the first packet of a burst. Valid only if frm_xmit_ok is clear.
	2	FIFO_ UNDERRUN	Tx FIFO underrun flag If set, transmission of the frame failed because the DMA engine was not able to supply the PCU with data as quickly as the baseband was requesting transmit data. Only valid for non-aggregate or non-RIFS underrun conditions unless the underrun occurred on the first packet of the aggregate or RIFS burst. See also the description for tx_delmtr_underrun_err and tx_data_underrun_err. Valid only if frm_xmit_ok is clear.
	1	EXCESSIVE _RETRIES	Excessive tries flag If set, transmission of the frame failed because the try limit was reached before the frame transmitted. Valid only if frm_xmit_ok is clear.
	0	FRM_XMIT_OK	Frame transmission success flag If set, the frame was transmitted successfully. If clear, no ACK or BA was received successfully.
4	31:0	SEND _TIMESTAMP	Timestamp at start of transmit A snapshot of the lower 32 bits of the PCU timestamp (TSF value). This field can be used to aid the software driver in implementing requirements associated with the aMaxTransmitMSDULifetime MAC attribute. The transmit timestamp is sampled on the rising of tx_frame signal which goes from the MAC to the baseband. This value corresponds to the last attempt at packet transmission not the first attempt.

Table 7-5 Tx Descriptor Status Format: Words 0-8 (cont.)

Word	Bits	Name	Description
5	31:0	BA_BITMAP_0-31	Block ACK bitmap 0 to 31 These bits are the values from the block ACK received after the successful transmission of an aggregate frame. If set, bit [0] represents the successful reception of the packet with the sequence number matching the seq_num value.
6	31:0	BA_BITMAP_32-63	Block ACK bitmap 32 to 63 These bits are the values from the block ACK received after the successful transmission of an aggregate frame. If set, bit [32] represents the successful packet reception with the sequence number matching the seq_num value + 32.
7	31:24	ACK_RSSI_COMBINED	Rx ACK signal strength indicator of combination of active chains on the control and extension channels.; a value of 0x80 (-128) indicates an invalid number.
	23:16	ACK_RSSI_ANT12	Rx ACK signal strength indicator of control channel chain 2 A value of 0x80 (–128) indicates an invalid number.
	15:8	ACK_RSSI_ANT11	Rx ACK signal strength indicator of control channel chain 1 A value of 0x80 (-128) indicates an invalid number.
	7:0	ACK_RSSI_ANT10	Rx ACK signal strength indicator of control channel chain 0 A value of 0x80 (-128) indicates an invalid number.
8	31:28	TID	Traffic identifier (TID) of block ACK; indicates the TID of the response block ACK. This field is only valid on the last descriptor of the last packet of an aggregate.
	27:26	RES	Reserved
	25	PWR_MGMT	Power management state; Indicates the value of the PwrMgt bit in the frame control field of the response ACK frame.
	24	TXBF_EXPIRED_MISS	Time expired indication for TXBF; When set, indicates two kinds of status: 1 The left-time of CV for this transmission destination is lower than the threshold set by software 2 CV is expired
	23	TXBF_DEST_MISS	Destination miss indication for TXBF; when set, indicates there is no CV for this destination. The PPDU is transmitted out Tx without beamforming.
	22:21	FINAL_TX_INDEX	Final transmission attempt series index; Specifies the number of the Tx series that caused frame transmission to terminate.
	20	RES	Reserved
	19	TXBF_STREAM_MISS	Stream miss indication for TxBF; When set, indicates that the CV information in CV cache is not enough for transmitting steered PPDU with current Tx rate, but still transmitting this PPDU out without Tx beamforming.
	18	TXBF_BW_MISMATCH	Bandwidth mismatch indication for TxBF If set, shows that the bandwidth of CV data is not same as the bandwidth of transmitting PPDU, then HW will send the PPDU but without Tx beamforming.
	17	TXOP_EXCEEDED	TXOP has been exceeded Indicates that this transmit frame had to be filtered because the amount of time to transmit this packet sequence exceeded the TXOP limit; should only occur when software programs the TXOP limit improperly.
	16:13	RES	Reserved
8 (Cont.)	12:1	SEQ_NUM	Starting sequence number; the value of the block ACK starting sequence control field in the response block ACK. Only consulted for aggregate Tx frames.
	0	DONE	Descriptor completion flag Set to one by the DMA engine when it has finished processing the descriptor and has updated the status information. Valid only for the final descriptor of a non-aggregate frame, regardless of the state of the FrTxOK flag. For an aggregate frame it is valid for only the final descriptor of the final packet of an aggregate. The driver is responsible for tracking what descriptors are associated with a frame. When the DMA engine sets the done flag in the final descriptor of a frame, the driver must be able to determine what other descriptors belong to the same frame and thus also have been consumed.

The DMA Rx logic (the DRU block) manages Rx descriptors and transfers the incoming frame data and status to the host through the PCIE Interface.

Words 0, and 2 are valid for all descriptors. Words 0, 2, and 11 is valid for the last descriptor of each packets. Words 0-11 are valid for the last descriptor of an aggregate or last descriptor of a stand-alone packet. Additional validity qualifiers are described individually. See Table 7-6.

Table 7-6 DMA Rx Descriptor Format for Words 0–11

Word	Bits	Name	Description	
0	31:16	ATHEROS_ID	The unique Qualcomm Atheros identifier of 0x168C is used to visually identify the start of the descriptor.	
	15	DESC_TX_RX	Indicates whether the descriptor is a transmit or receive descriptor. The value should be set to 1 indicating transmit.	
	14	DESC_CTRL_ STAT	Indicates whether the descriptor is a control or status descriptor. The value should be set to 1 indicating status descriptor.	
	13:9	RES	Reserved	
	8	RX_PRIORITY	0	Low priority queue
			1	High priority queue
	7:0	DESC_LENGTH	Descriptor length Indicates the number of Dwords in this descriptor. The value should be set to 0x9 (9 Dwords).	
1	31:24	RX_RATE	Rx rate indication; Indicates the rate at which this frame was transmitted from the source. Encodings match those used for the tx_rate*' field in word 5 of the Tx descriptor. Valid only if the frame_rx_ok flag is set or if the frame_rx_ok flag is clear and the phy_error flag is clear.	
	23:16	RSSI_ANT02	Received signal strength indicator of control channel chain 2; A value of 0x80 (-128) indicates an invalid number.	
	15:8	RSSI_ANT01	Received signal strength indicator of control channel chain 1; A value of 0x80 (-128) indicates an invalid number.	
	7:0	RSSI_ANT00	Received signal strength indicator of control channel chain 0; A value of 0x80 (-128) indicates an invalid number.	
2	31:23	RES	Reserved	
	22	HW_UPLOAD _DATA	Indicates the data carried by current descriptor is that hardware upload for TXBF using (H, V, or CV data). The upload data is valid only when the field hw_upload_ data_valid at RXS 4 bit [7] is set. See RXS 11 bit [26:25] hw_upload_data_type to know which data type is uploaded. Valid for all descriptors.	
	21:14	NUM_DELIM	Number of zero length pad delimiters after current packet This field does not include the start delimiter which is required between each packet in an aggregate. This field is only valid for aggregate packets except for the last packet of an aggregate.	
	13	RES	Reserved	
	12	MORE	More descriptors in this frame flag If set, then this is not the final descriptor of the frame. If clear, then this descriptor is the final one of the frame. Valid for all descriptors.	
	11:0	DATA_LEN	Received data length Specifies the length, in bytes, of the data actually received into the data buffer associated with this descriptor. The actual received data length will be between zero and the total size of the data buffer, as specified originally in this field (see the description for the buf_len field). Valid for all descriptors. See Data Buffer Length (DATABUF).	
3	31:0	RCV _TIMESTAMP	A snapshot of the PCU timestamp (TSF value), expressed in µs (that is, bits [31:0] of the PCU 64-bit TSF). Intended for packet logging and packet sniffing. The timestamp is sampled on the rising edge of rx_clear, which goes from the baseband to the MAC.	

Table 7-6 DMA Rx Descriptor Format for Words 0–11

Word	Bits	Name	Description			
4	31:8	RES	Reserved			
	7	HW_UPLOAD _DATA_VALID	Specifies whether the contents of the hardware upload data are valid			
	6:5	NESS	Receive packet NESS field Shows the number of Rx extension spatial steams.			
	4	NOT _SOUNDING	Rx packet not sounding flag If this value is clear, then the Rx frame is a sounding PPDU. If this value is set, the receive frame is not a sounding PPDU.			
	3	STBC	Rx packet STBC indicator; If this value is set then the baseband has received an STBC frames as indicated in the HT_PLCP.			
	2	DUPLICATE	Rx packet duplicate indicator; If this value is set, the baseband has determined that this packet is a duplicate packet.			
	1	20_40	Rx packet 20 or 40 MHz bandwidth indicator; If this value is clear, then the receive frame was a HT20 packet (20-MHz bandwidth). If this value is set, then the receive frame was a HT40 packet (40-MHz bandwidth).			
	0	GI	Rx packet guard interval If this value is clear, then the Rx frame used a long guard interval. If this value is set, the Rx frame used a short guard interval.			
5	31:24	RX_COMBINED	RSSI of combination of all active chains on the control and extension channels. The value of 0x80 (-128) is used to indicate an invalid number.			
	23:16	RSSI_ANT12	Received signal strength indicator of extension channel chain 2 A value of 0x80 (-128) indicates an invalid number.			
	15:8	RSSI_ANT11	Received signal strength indicator of extension channel chain 1 A value of 0x80 (-128) indicates an invalid number.			
	7:0	RSSI_ANT10	Received signal strength indicator of extension channel chain 0 A value of 0x80 (-128) indicates an invalid number.			
6	31:0	EVM0	Rx packet error vector magnitude 0			
			Bits Mode	**HT20 Mode**	**HT40 Mode**	**Diagnostic**
			evm0[31:24]	pilot1_str0	pilot1_str0	legacy_plcp_byte_1
			evm0[23:16]	RES	RES	legacy_plcp_byte_2
			evm0[15:8]	pilot0_str1	pilot0_str1	legacy_plcp_byte_3
			evm0[7:0]	pilot0_str0	pilot0_str0	service_byte_1
7	31:0	EVM1	Rx packet error vector magnitude 1			
			Bits Mode	**HT20 Mode**	**HT40 Mode**	**Diagnostic**
			evm1[31:24]	pilot2_str1	pilot2_str1	service_byte_2
			evm1[23:16]	pilot2_str0	pilot2_str0	ht_plcp_byte_1
			evm1[15:8]	RES	RES	ht_plcp_byte_2
			evm1[7:0]	pilot1_str1	pilot1_str1	ht_plcp_byte_3
8	31:0	EVM2	Rx packet error vector magnitude 2			
			Bits Mode	**HT20 Mode**	**HT40 Mode**	**Diagnostic**
			evm2[31:24]	RES	RES	service_byte_4
			evm2[23:16]	pilot3_str1	pilot3_str1	ht_plcp_byte_5
			evm2[15:8]	pilot3_str0	pilot3_str0	ht_plcp_byte_6
			evm2[7:0]	RES	RES	0x0

Table 7-6 DMA Rx Descriptor Format for Words 0–11

<table>
<tr><th>Word</th><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="5">9</td><td rowspan="5">31:0</td><td rowspan="5">EVM3</td><td colspan="4">Rx packet error vector magnitude 3</td></tr>
<tr><td>Bits Mode</td><td>HT20 Mode</td><td>HT40 Mode</td><td>Diagnostic</td></tr>
<tr><td>evm3[31:24]</td><td>0x80</td><td>pilot5_str0</td><td>0x0</td></tr>
<tr><td>evm3[23:16]</td><td>0x80</td><td>RES</td><td>0x0</td></tr>
<tr><td>evm3[15:8]</td><td>0x80</td><td>pilot4_str1</td><td>0x0</td></tr>
<tr><td rowspan="6">10</td><td rowspan="2">31:22</td><td rowspan="2">NOISE_FLOOR</td><td colspan="4">For responding CSI report in explicit TXBF procedure; software needs this information to calculate SNR.</td></tr>
<tr><td>evm3[7:0]</td><td>0x80</td><td>pilot4_str0</td><td>0x0</td></tr>
<tr><td>21:16</td><td>RES</td><td colspan="4">Reserved</td></tr>
<tr><td rowspan="4">15:0</td><td rowspan="4">EVM4</td><td colspan="4">Rx packet error vector magnitude 4</td></tr>
<tr><td>Bits Mode</td><td>HT20 Mode</td><td>HT40 Mode</td><td>Diagnostic</td></tr>
<tr><td>evm4[15:8]</td><td>0x80</td><td>RES</td><td>0x0</td></tr>
<tr><td>evm4[7:0]</td><td>0x80</td><td>pilot4_str1</td><td>0x0</td></tr>
<tr><td rowspan="20">11</td><td>31</td><td>KEY_MISS</td><td colspan="4">Key cache miss indication; When set, indicates that the PCU could not locate a valid decryption key for the frame. Valid only if the frame_rx_ok flag is clear.</td></tr>
<tr><td>30</td><td>RES</td><td colspan="4">Reserved</td></tr>
<tr><td>29</td><td>FIRST_AGG</td><td colspan="4">First packet of aggregate; if set, indicates this is the first packet of an aggregate.</td></tr>
<tr><td>28</td><td>HI_RX_CHAIN</td><td colspan="4">If set indicates that the Rx chain control in high power mode.</td></tr>
<tr><td>27</td><td>RES</td><td colspan="4">Reserved</td></tr>
<tr><td rowspan="19">26:25</td><td rowspan="19">HW_UPLOAD_
DATA_TYPE</td><td colspan="4">Indicates the hardware upload data (H, V, or CV). The upload data is valid only when the field hw_upload_data_valid at RXS 4 bit [7] is set:</td></tr>
<tr><td>01</td><td colspan="3">Upload is H</td></tr>
<tr><td>10</td><td colspan="3">Upload is V</td></tr>
<tr><td>11</td><td colspan="3">Upload is CV</td></tr>
<tr><td colspan="4">To support a delay response at explicit TXBF, the upload data (H, V, or CV) at different registers configuration:
<code>regs_config = {MAC_PCU_H_XFER_TIMEOUT_EXTXBF_IMMEDIATE_RESP, MAC_PCU_H_XFER_TIMEOUT_DELAY_EXTXBF_ONLY_UPLOAD_H, MAC_PCU_H_XFER_TIMEOUT_EXTXBF_NOACK_NORPT}</code>
Request report:</td></tr>
<tr><td>regs_config</td><td colspan="2">Request CSI</td><td>Request V/CV</td></tr>
<tr><td>{0,0,x}</td><td colspan="2">HW upload H</td><td>HW upload V/CV</td></tr>
<tr><td>{0,1,x}</td><td colspan="2">HW upload H</td><td>HW upload H</td></tr>
<tr><td colspan="4">If regs_config is {1,x,0}, it means hardware supports immediate response even if it does not need to respond to ACK. Hardware will upload H only when the request report is CSI.
If regs_config is {1,0,1}, it means HW support immediate response but hardware will upload H/V/CV base on request report for delay response if hardware does not need to respond to ACK.
Request Report:</td></tr>
<tr><td>regs_config</td><td colspan="2">Request CSI</td><td>Request V/CV</td></tr>
<tr><td>{0,0,x}</td><td colspan="2">HW upload H</td><td>HW upload V/CV</td></tr>
<tr><td>{0,1,x}</td><td colspan="2">HW upload H</td><td>HW upload H</td></tr>
<tr><td colspan="4">If regs_config is {1,1,1}, hardware supports immediate response but hardware only uploads H for a delay response if it does not need to respond to ACK. For RTS, hardware only supports a delay response and uploads H, V, or CV to software.</td></tr>
<tr><td>24:19</td><td>RES</td><td colspan="4">Reserved</td></tr>
</table>

Table 7-6 DMA Rx Descriptor Format for Words 0–11

Word	Bits	Name	Description
11 (Cont.)	18	post_delim _crc_erR	Delimiter CRC error is detected after this current frame Only occurs when the start delimiter of the last frame in an aggregate is bad.
	17	AGGREGATE	Aggregate flag If set, indicates that this packet is part of an aggregate.
	16	MORE_AGG	More aggregate flag Set to 1 in all packets of an aggregate that have another packet of the current aggregate to follow. If clear, indicates that this packet is the last one of an aggregate.
	15:9	KEY_IDX	If the FrRxOK bit is set, then this field contains the decryption key table index. If KEY_IDX_VALID is set, then this field specifies the index at which the PCU located the frame's destination address in its on-chip decryption key table. If key_ idx_VALID is clear, the value of this field is undefined. If the FrRxOK bit is clear and the PHYErr bit is set, then this field contains bits [7:1] of the PHY error code.
	8	KEY_IDX_VALID	If frame_rx_ok is set, this field contains the decryption key table index valid flag. If set, indicates that the PCU successfully located the frame's source address in its on-chip key table and that the key_idx field reflects the table index at which the destination address was found. If clear, indicates that PCU failed to locate the destination address in the key table and that the contents of key_idx field are undefined. If the frame_rx_ok bit is clear and the phy_error bit is set, then this field contains bit [0] of the PHY error code.
	7	ASPD_TRIG	Received APSD trigger frame The received frame matched the profile of an APSD trigger frame.
	6	PRE_DELIM _CRC_ERR	Delimiter CRC error detected before this current frame. May indicate that an entire packet may have been lost.
	5	MIC_ERROR	Michael integrity check error flag If set, then the frame TKIP Michael integrity check value did not verify correctly. Valid only when all of the following are true: ■ frame_rx_ok bit is set ■ The frame was decrypted using TKIP key type ■ The frame is not a fragment
	4	PHY_ERROR	PHY error flag If set, then reception of the frame failed because the PHY encountered an error. In this case, bits [15:8] of this word indicate the specific type of PHY error; see the baseband specification for details. Valid only if the frame_rx_ok flag is clear.
	3	DECRYPT_ CRC_ERR	Decryption CRC failure flag If set, frame reception failed because the frame was marked as encrypted but the PCU was unable to decrypt the frame properly because the CRC check failed after the decryption process completed. Valid only if the frame_rx_ok flag is clear.
	2	CRC_ERROR	CRC error flag If set, reception of the frame failed because the PCU detected an incorrect CRC value. Valid only if the frame_rx_ok flag is clear.
	1	FRAME_RX_OK	Frame reception success flag. If set, the frame was received successfully. If clear, an error occurred during frame reception.
	0	DONE	Descriptor completion flag Set to one by the DMA engine when it has finished processing the descriptor and has updated the status information. Valid for all descriptors.

7.4 Queue Control Unit (QCU)

The queue control unit performs two tasks:

- Managing the Tx descriptor chain processing for frames pushed to the QCU from the CPU by traversing the linked list of Tx descriptors and transferring frame data from the host to the targeted DCU.
- Managing the queue transmission policy to determine when the frame at the head of the queue should be marked as available for transmission.

The MAC contains ten QCUs. Each QCU contains all the logic and state registers needed to manage a single queue (linked list) of Tx descriptors. A QCU is associated with exactly one DCU. When a QCU prepares a new frame, it signals ready to the DCU. When the DCU accepts the frame, the QCU responds by getting the frame data and passing it to the DCU for eventual transmission to the PCU and on to the air.

The host controls how the QCU performs these tasks by writing to various QCU configuration registers.

7.5 DCF Control Unit (DCU)

Collectively, the ten DCUs implement the EDCF channel access arbitration mechanism defined in the Task Group E (TGe) QoS extension to the 802.11 specification. Each DCU is associated with one of the eight EDCF priority levels and arbitrates with the other DCUs on behalf of all QCUs associated with it. A central DCU arbiter monitors the state of all DCUs and grants one the next access to the PCU (that is, access to the channel).

Because the EDCF standard defines eight priority levels, the first eight DCUs (0-7) map directly to the eight EDCF priority levels. The two additional DCUs handle beacons and beacon-gated frames for a total of ten DCUs.

The mapping of physical DCUs to absolute channel access priorities is fixed and cannot be altered by software: The highest-priority DCU is DCU 9. Typically, this DCU is the one associated with beacons. The next highest priority DCU is DCU 8. Typically, this DCU is the one associated with beacon-gated frames.

The remaining eight DCUs priority levels are filled with DCUs 7 through 0. Among these 8 DCUs, DCU 7 has highest priority, DCU 6 the next highest priority, and so on through DCU 0, which has the lowest priority. Typically, these DCUs are associated with EDCF priorities seven through zero, respectively.

7.6 Protocol Control Unit (PCU)

The PCU is responsible for the details of sending a frame to the baseband logic for transmission, for receiving frames from the baseband logic and passing the frame data to the DRU, including:

- Buffering Tx and Rx frames
- Encrypting and decrypting
- Generating ACK, RTS, and CTS frames
- Maintaining the timing synchronization function (TSF)
- Forming aggregate
- Maintaining sequence state and generating Block ACK.
- Inserting and verifying FCS
- Generating virtual clear channel assessment (CCA)
- Updating and parsing beacons
- The PCU is primarily responsible for buffering outgoing and incoming frames and conducting medium access compatible with the IEEE 802.11 DCF protocol.

Figure 7-1 shows the PCU functional block diagram.

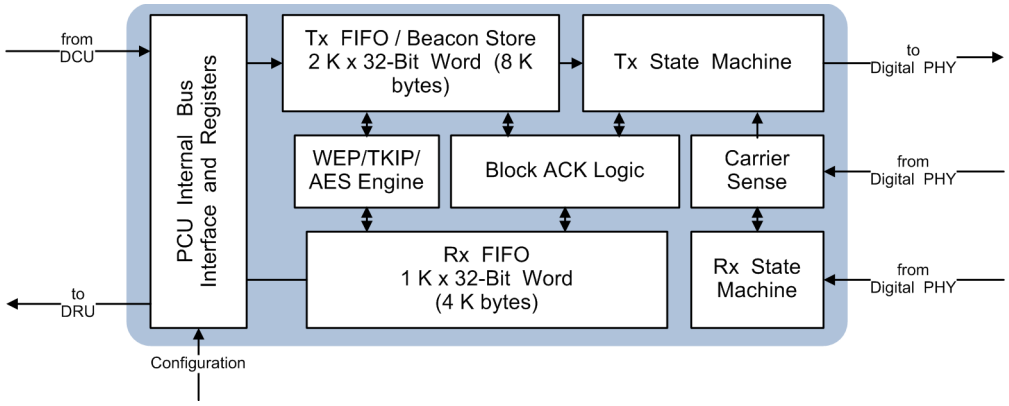


Figure 7-2 PCU Functional Block

7.7 Register Programming Details for Observing WMAC Interrupts

To configure the WMAC glue registers for observing WMAC interrupts:

1. Set bit [1] of these registers to observe MAC interrupts:
   - Synchronous Interrupt Enable (WMAC_GLUE_INTF_INTR_SYNC_ENABLE)
   - Synchronous Interrupt Cause (WMAC_GLUE_INTF_INTR_SYNC_CAUSE)
   - Interface Timeout (WMAC_GLUE_INTF_TIMEOUT)
   - Asynchronous Priority Interrupt Enable (WMAC_GLUE_INTF_INTR_PRIORITY_ASYNC_ENABLE)
2. Write 0xFFFF_FFFF to the Synchronous Interrupt Cause (WMAC_GLUE_INTF_INTR_SYNC_CAUSE) register to clear any pending interrupts.
3. Set bit [0] of the Global Interrupt Status (RST_GLOBAL_INTERRUPT_STATUS) register to enable MAC interrupts.
4. Enable primary MAC interrupts in the Primary Interrupt Mask (IMR_P) register (for example: bit [6] (TXOK), bit [1] (RXOK(LP)), and bit [0] (RXOK(HP)).
5. Enable secondary interrupts by writing to the IMR_S* registers: Secondary Interrupt Mask 0 (IMR_S0) through Secondary Interrupt Mask 5 (IMR_S5).
6. Read bits [3:0] of the register Interrupt Status (RST_EXT_INTERRUPT_STATUS):
   - Bit [0] = 1: Indicates a WMAC interrupt
   - Bit [0] = 1, bit [1] = 1: Indicates a WMAC Tx interrupt
   - Bit [0] = 1, bit [2] = 1: Indicates a WMAC Rx LP interrupt
   - Bit [0] = 1, bit [3] = 1: Indicates a WMAC Rx HP interrupt
7. Read the Primary Interrupt Status (ISR_P) register to find the exact interrupt. Clear the interrupt by writing 1 to the corresponding bit.

8 Digital PHY Block

The digital physical layer (PHY) block is described in 802.11n mode and 802.11 a/b/g legacy mode. Transmit and receive paths are shown as diagrams for 802.11n mode.

8.1 Overview

The digital PHY block is a half-duplex, OFDM, CCK, DSSS baseband processor compatible with IEEE 802.11n and 802.11a/b/g. The QCA9558 supports both 20- and 40-MHz channel modes and data rates up to 300 Mbps defined by the IEEE 802.11a/b/g/n standards. Modulation schemes include BPSK, QPSK, 16-QAM, 64-QAM, and forward error correction coding with rates of 1/2, 2/3, 3/4, and 5/6.

All three 802.11n advanced features, space time block code (STBC), low-density parity check (LDPC), and Tx beamforming are supported in the QCA9558 chip. In addition, many new performance enhancing features are included, such as maximum likelihood (ML) MIMO receiver, and maximum ratio combining (MRC) for OFDM and 802.11b packet detection.

8.2 802.11n (MIMO) Mode

Frames beginning with training symbols are used for signal detection, automatic gain control, frequency offset estimation, symbol timing, and channel estimation. This process uses 56 sub-carriers for 20-MHz HT mode: 52 for data transmission and 4 for pilots. It uses 114 sub-carriers for 40-MHz HT mode: 108 for data transmission and 6 for pilots.

8.2.1 Transmitter (Tx)

Figure 8-1 shows the Tx path digital PHY 802.11n (MIMO mode) block diagram.

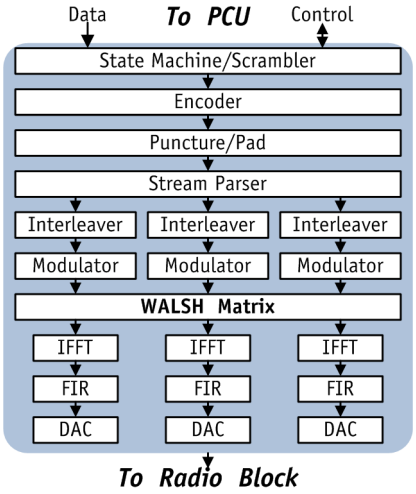


Figure 8-1 Digital PHY 802.11n Tx

The PCU block initiates transmission. The digital PHY powers on the digital to analog converter (DAC) and transmit the training symbol. The training symbols are a fixed waveform and are generated within the digital PHY in parallel with the PCU sending the Tx header (frame length, data rate, etc.). The PCU must send transmitted data quickly enough to prevent buffers in the digital PHY from becoming empty. The PCU is prevented from sending data too quickly by pauses generated within the digital PHY.

Figure 8-1 shows a 3x3 MIMO system with three spatial data streams. The spatial parser splits the coded data into multiple data streams by allocating the proper number of bits to each data stream so that the number of data symbols resulted in each stream is the same. Then it interleaves coded bits across different data subcarriers followed by the modulation. To achieve the maximum spatial diversity for one-stream and two-stream transmission, the Walsh matrix orthogonally spreads the modulated stream(s) into three Tx antennas before undergoing IFFT processing to produce time domain signals.

8.2.2 Receiver (Rx)

Figure 8-2 shows the Rx path digital PHY 802.11n (MIMO mode) block diagram.

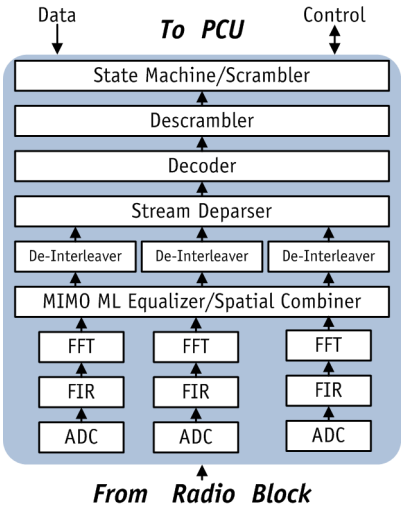


Figure 8-2 Digital PHY 802.11n Rx

The receiver inverts the transmitter's steps, performing a fast Fourier transform (FFT), extracting bits from received constellations, de-interleaving, accounting for puncturing, decoding, and descrambling. The Rx block shows 3x3 MIMO configuration. Figure 8-2 shows a frequency-domain Maximum Likelihood (ML) equalizer handling degradation due to multi-path.

8.3 802.11a/b/g Legacy Mode

8.3.1 Transmitter

The QCA9558 digital PHY incorporates an OFDM and DSSS transceiver that supports all data rates defined by IEEE 802.11a/b/g. Legacy mode is detected on per-frame basis. PLCP frames are detected for legacy network information. The transmitter switches dynamically to generate legacy signals (802.11b/g in 2.4 GHz and 802.11a in 5 GHz).

8.3.2 Receiver

The receiver is capable of dynamically detecting legacy, HT 20 MHz or 40 MHz frames and will demodulate the frame according to the detected frame type. Maximum ratio combining (MRC) is used for OFDM and 802.11b packet detection.

9 Radio Block

The transceiver of the QCA9558 solution consists of these major functional blocks:

- 3 x Receive chain
  Each chain = Radio + BB programmable gain filter
- 3 x Transmit chain
  Each chain = Radio + BB programmable gain filter
- Frequency synthesizer (SYNTH)
- Associated bias/control (BIAS)

See Figure 9-1 [1].

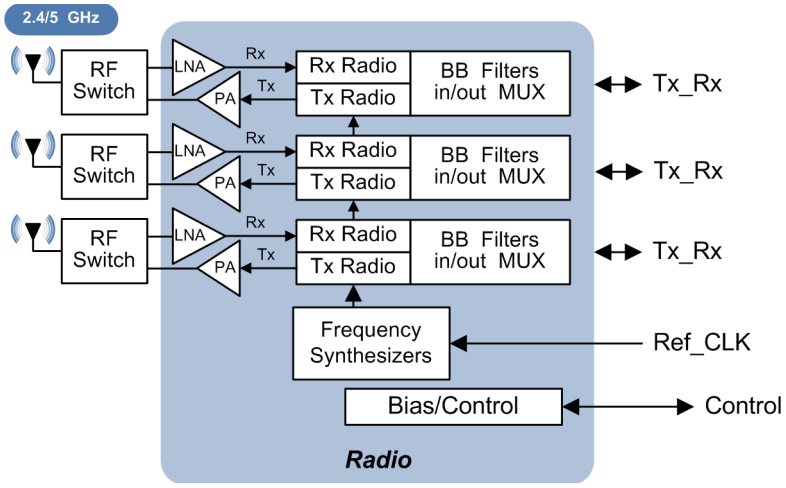


Figure 9-1 Radio Functional Block Diagram

1. Internal PA is only supported for 2.4 GHz, use external PA for 5 GHz operations

9.1 Receiver (Rx) Block

The receiver converts an RF signal (with 20 MHz or 40 MHz bandwidth) to BB I and Q outputs as shown in Figure 9-2. The dual band receiver operates in the 2.4 GHz or 5 GHz bands to support CCK and OFDM signals for 802.11a, 802.11b, 802.11g, and 802.11n. The 2.4 GHz receiver implements a direct-conversion architecture. The 5 GHz receiver implements a dual-conversion architecture that eliminates the need for an external intermediate frequency filter while providing the advantages of traditional heterodyne approaches.

The 2.4 GHz receiver consists of an LNA, a pair of quadrature radio frequency (RF) mixers, and in-phase (I) and quadrature (Q) BB programmable gain filter/amplifiers (PGA). The mixers convert the output of the on-chip LNA to BB I and Q signals. The I and Q signals are low-pass filtered and amplified by a BB programmable gain filter controlled by digital logic. The BB signals are sent to the ADC within the MAC/BB processor.

The 5 GHz receiver consists of an LNA, a RF variable gain amplifier (VGA), quadrature RF and intermediate frequency (IF) mixers, and I and Q BB PGA. Mixer(s) convert the output of the RF VGA to BB I and Q signals. A BB programmable gain filter controlled by digital logic low-pass filters and amplifies the I and Q signals. BB signals are sent to the ADC within the MAC/BB processor. The DC offset of the receive chain is reduced using multiple DACs controlled by the MAC/ BB processor. Additionally, this chain can be digitally powered down to conserve power.

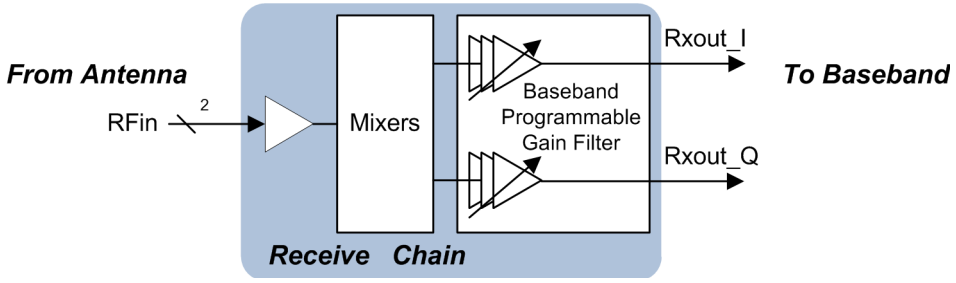


Figure 9-2 Radio Rx Chain Block Diagram

9.2 Transmitter (Tx) Block

The transmitter converts BB I and Q inputs to 2.4/5 GHz RF outputs as shown in Figure 9-3. The inputs to the transmitter are current outputs of the I and Q DAC within the MAC/BB processor. These currents are low-pass filtered through an on-chip reconstruction filter to remove spectral images and out-of-band quantization noise. The I and Q signals are converted to RF signals using an integrated up-conversion architecture.

For the 2.4 GHz transmitter, BB I and Q signals up-convert directly to RF using a pair of quadrature mixers. For 5 GHz, BB I and Q signals up-convert to RF using a pair of IF quadrature mixers and a pair of RF quadrature mixers. A power amplifier drives the up-converted RF signals off-chip. The transmit chain can be digitally powered down to conserve power. To ensure that FCC limits are observed and the output power stays close to the maximum allowed, transmit output power is adjusted by a digitally programmed control loop at the start of each packet. The QCA9558 provides an open loop power control based on an on-chip temperature sensor.

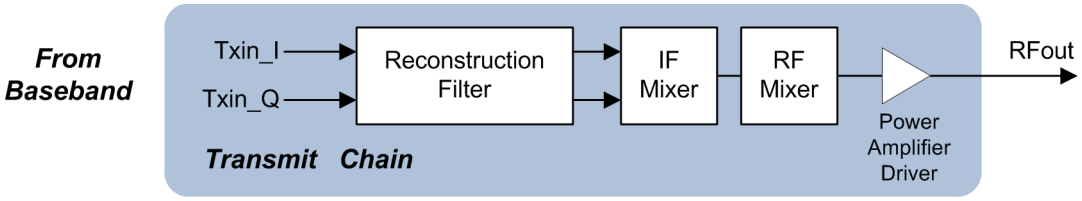


Figure 9-3 Radio Tx Chain Block Diagram

9.3 Synthesizer (SYNTH) Block

The radio supports an on-chip synthesizer to generate local oscillator (LO) frequencies for the receiver and transmitter mixers. The synthesizer has the topology shown in Figure 9-4. The QCA9558 generates the reference input from a 40 MHz crystal for the synthesizer. An on-chip voltage controlled oscillator (VCO) provides the desired LO signal based on a phase locked loop.

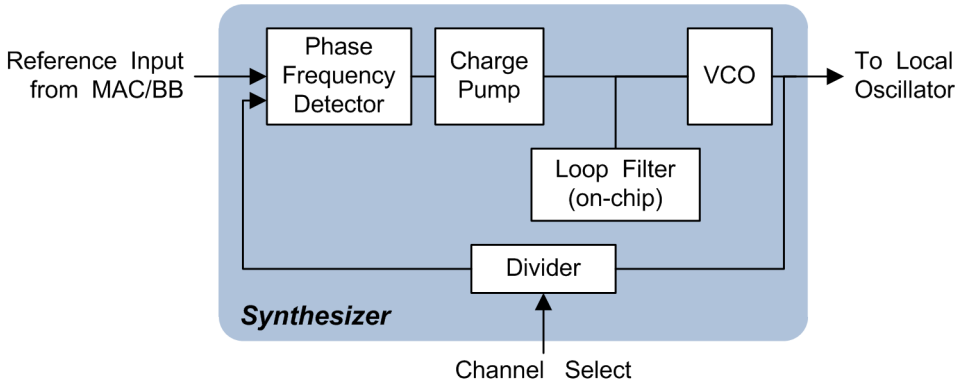


Figure 9-4 Radio Synthesizer Block Diagram

10 Register Descriptions

Table 10-1 summarizes the CPU mapped registers for the QCA9558.

Table 10-1 CPU Mapped Registers Summary

Address	Description	Page
0x18000000-0x1800015C	DDR Registers	page 150
0x18018000-0x18018080	I^2C Registers	page 163
0x18020000-0x18020018	UART0 (Low-Speed) Registers	page 180
0x18030000-0x1803000C	USB Registers	page 187
0x18040000-0x1804006C	GPIO Registers	page 191
0x18050000-0x18050048	PLL Control Registers	page 201
0x18060000-0x1806405C	Reset Registers	page 212
0x18070000–0x18070010	GMAC Interface Registers	page 224
0x18080000-0x1808305C	GMAC0 Ingress NAT/Egress NAT Registers	page 236
0x180A0000-0x180A006C	MBOX Registers	page 254
0x180A9000-0x180A9030	SLIC Registers	page 265
0x180B0000-0x180B0018	Stereo Registers	page 270
0x180B8000-0x180B8024	MDIO Registers	page 275
0x180F0000-0x180F005C 0x18250000-0x182507FF	PCIE RC Control Registers	page 276
0x18100008-0x18100104	WDMA Registers	page 288
0x18100800-0x18100A44	WQCU Registers	page 307
0x18101000-0x18101F04	WDCU Registers	page 314
0x18104000-0x1810409C	WMAC Glue Registers	page 335
0x18107000-0x18107058	RTC Registers	page 345
0x18108000-0x1810E000	WPCU Registers	page 355
0x180C0000-0x180C003E 0x18280000-0x1828005C	PCIE Configuration Space Registers	page 405
0x18116200 -0x18116208 0x18116C80-0x18116C88	PCIE PLL PHY Registers	page 413
0x18116CC0-0x18116CC4	PMU Registers	page 415

Table 10-1 CPU Mapped Registers (cont.)**Summary**

Address	Description	Page
0x18116DC0-0x18116CC8 0x18116E00-0x18116E08	PCIE RC PHY Registers	page 416
0x18116DC0-0x18116DC8	PCIE EP PHY Registers	page 419
0x18400000-0x18400054	Checksum Registers	page 422
0x18500000-0x18500010	UART1 (High-Speed) Registers	page 431
0x19000000-0x190001D8 0x1A000000-0x1A0001D8	GMAC0/GMAC1 Registers	page 435
0x1B000000-0x1B0001FC 0x1B400000-0x1B4001FC	USB Controller Registers	page 503
0x1B000200-0x1B0002B4	NAND Flash Registers	page 534
0x18127800-0x18127D18, 0x00000000-0x00000F18	PCIE EP DMA Registers	page 550
0x1F000000-0x1F000018	Serial Flash SPI Registers	page 559
0x18116180-0x18116188, 0x181161C0-0x181161C8, 0x18116200-0x18116208, 0x18116240-0x18116248, 0x18116C00-0x18116C08	PLL SRIF Registers	page 562

10.1 DDR Registers

Table 10-2 summarizes the DDR registers for the QCA9558.

NOTE The memory controller core clock is twice the frequency of the DDR_CK_P clock.

Table 10-2 DDR Registers Summary

Address	Name	Description	Page
0x18000000	DDR_CONFIG	DDR DRAM Configuration	page 151
0x18000004	DDR_CONFIG2	DDR DRAM Configuration 2	page 152
0x18000008	DDR_MODE_REGISTER	DDR Mode Value	page 153
0x1800000C	DDR_EXTENDED_MODE_REGISTER	DDR Extended Mode Value	page 153
0x18000010	DDR_CONTROL	DDR Control	page 153
0x18000014	DDR_REFRESH	DDR Refresh Control and Configuration	page 154
0x18000018	DDR_RD_DATA_THIS_CYCLE	DDR Read Data Capture Bit Mask	page 154
0x1800001C	TAP_CONTROL_0	DQS Delay Tap Control for Byte 0	page 154
0x18000020	TAP_CONTROL_1	DQS Delay Tap Control for Byte 1	page 155
0x18000024	TAP_CONTROL_2	DQS Delay Tap Control for Byte 2	page 155
0x18000028	TAP_CONTROL_3	DQS Delay Tap Control for Byte 3	page 155
0x1800009C	DDR_WB_FLUSH_GE0	GE0 Interface Write Buffer Flush	page 156
0x180000A0	DDR_WB_FLUSH_GE1	GE1 Interface Write Buffer Flush	page 156
0x180000A4	DDR_WB_FLUSH_USB	USB Interface Write Buffer Flush	page 156
0x180000A8	DDR_WB_FLUSH_PCIE	PCIE Interface Write Buffer Flush	page 156
0x180000AC	DDR_WB_FLUSH_WMAC	WMAC Interface Write Buffer Flush	page 157
0x180000B0	DDR_WB_FLUSH_MISC_SRC1	SRC1 Interface Write Buffer Flush	page 157
0x180000B4	DDR_WB_FLUSH_MISC_SRC2	SRC2 Interface Write Buffer Flush	page 157
0x180000B8	DDR2_CONFIG	DDR2 Configuration	page 158
0x180000BC	DDR_EMR2	DDR Extended Mode 2 Value	page 158
0x180000C0	DDR_EMR3	DDR Extended Mode 3 Value	page 158
0x180000C4	DDR_BURST	DDR Bank Arbiter Per Client Burst Size 1	page 159
0x180000C8	DDR_BURST2	DDR Bank Arbiter Per Client Burst Size 2	page 159
0x180000CC	AHB_MASTER_TIMEOUT_MAX	AHB Master Timeout Control	page 160
0x180000D0	AHB_MASTER_TIMEOUT_CURNT	AHB Timeout Current Count	page 160
0x180000D4	AHB_MASTER_TIMEOUT_SLAVE_ADDR	Timeout Slave Address	page 160
0x18000108	DDR_CTL_CONFIG	DDR Controller Configuration	page 161
0x18000110	DDR_SF_CTL	DDR Self Refresh Control	page 161
0x18000114	SF_TIMER	Self Refresh Timer	page 162
0x18000128	WMAC_FLUSH	WMAC Flush	page 162
0x1800015C	DDR_CONFIG_3	DDR Configuration 3	page 162

10.1.1 DDR DRAM Configuration (DDR_CONFIG)

Address: 0x18000000
Access: Read/Write
Reset: See field description

This register is used to configure the DDR DRAM parameters.

Bit	Bit Name	Reset	Description
31	CAS_ LATENCY_MSB	0x0	DRAM CAS latency parameter MSB rounded up in memory controller core clock cycles
30	OPEN_PAGE	0x1	Controller open page policy. Open page policy increases bus efficiency if accesses are local to a page but increase random read/write latency. 0 Page Open 1 Page Close
29:27	CAS_LATENCY	0x6	DRAM CAS latency parameter (first 3 bits) rounded up in memory controller core clock cycles. CAS_LATENCY is used by the hardware to estimate the internal DDR clock latency of a read. It should be greater than or equal to GATE_OPEN_ LATENCY as specified in the DDR DRAM Configuration 2 (DDR_CONFIG2) register. The value of this register should be memory CAS_LATENCY * 2 or CAS_LATENCY * 2+1/2/3.
26:23	TMRD	0xF	DRAM tMRD parameter rounded up in memory controller core clock cycles
22:17	TRFC	0x1F	DRAM tRFC parameter rounded up in memory controller core clock cycles/4 (if LSB two bits in DDR_CONFIG_3 register are left 0)
16:13	TRRD	0x4	DRAM tRRD parameter rounded up in memory controller core clock cycles
12:9	TRP	0x6	DRAM tRP parameter rounded up in memory controller core clock cycles
8:5	TRCD	0x6	DRAM tRCD parameter rounded up in memory controller core clock cycles
4:0	TRAS	0x10	DRAM tRAS maximum (tRAS minimum+ read latency) parameter rounded up in memory controller core clock cycles

10.1.2 DDR DRAM Configuration 2 (DDR_CONFIG2)

Address: 0x18000004
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31	RES	0x1	Reserved	
30	SWAP_A26_ A27	0x0	This bit gives a choice to drive CPU addresses A26 and A27 on different column lines. This is needed to support different combinations of devices on board. Please refer doc/ddr_init.doc for more details.	
			0	Drives CPU_addr[26] on A11 of COL if DDR_CONFIG_HALF_WIDTH = 1 or on A9 of COL if DDR_CONFIG_HALF_WIDTH = 0. In this case, CPU_ addr[27] will be driven on A12 of COL if DDR_CONFIG_HALF_WIDTH = 1 and A11 of COL if DDR_CONFIG_HALF_WIDTH = 0.
			1	Drives CPU_addr[27] on A11 of COL if DDR_CONFIG_HALF_WIDTH = 1 or on A9 of COL if DDR_CONFIG_HALF_WIDTH = 0. In this case, CPU_ addr[26] will be driven on A12 of COL if DDR_CONFIG_HALF_WIDTH = 1 and A11 of COL if DDR_CONFIG_HALF_WIDTH = 0.
29:26	GATE_OPEN_ LATENCY	0x6	DRAM gate open latency parameter rounded up in memory controller core clock cycles	
25:21	TWTR	0xE	DRAM tWTR parameter rounded up in memory controller core clock cycles	
20:17	TRTP	0x8	DRAM read to precharge parameter rounded up in memory controller core clock cycles. The normal value is two clock cycles.	
16:12	TRTW	0x10	DRAM tRTW parameter rounded up in memory controller core clock cycles. The value should be calculated as CAS_LATENCY + BURST LENGTH + BUS TURNAROUND TIME.	
11:8	TWR	0x6	DRAM tWR parameter rounded up in memory controller core clock cycles	
7	CKE	0x1	DRAM CKE bit	
6:0	RES	0x0	Reserved	

10.1.3 DDR Mode Value (DDR_MODE_REGISTER)

Address: 0x18000008
Access: Read/Write
Reset: See field description

This register is used to set the DDR mode register value. Refer to the DDR memory device datasheet for bit-definitions of this register.

10.1.4 DDR Extended Mode (DDR_EXTENDED_MODE_REGISTER)

Address: 0x1800000C
Access: Read/Write
Reset: See field description

This register is used to set the extended DDR mode register value. Refer to the DDR memory device datasheet for bit-definitions of this register.

10.1.5 DDR Control (DDR_CONTROL)

Address: 0x18000010
Access: Read/Write
Reset: 0x0

This register is used to force update cycles in the DDR control. The CPU first initializes DDR_MODE_REGISTER/DDR_EXTENDED_MODE_REGISTER/DDR_EMR2/DDR_EMR3 register, then writes into DDR_CONTROL. Only one of the bits in this register can be set by the CPU. The bit that is set determines which MR/EMR/EMR2/EMR3 register write command is issued to the DDR device.

Bit	Bit Name	Description
31:6	RES	Reserved
5	EMR3S	Forces an EMR3 update cycle
4	EMR2S	Forces an EMR2 update cycle
3	PREA	Forces a PRECHARGE ALL cycle
2	REF	Forces an AUTO REFRESH cycle
1	EMRS	Forces an EMRS update cycle
0	MRS	Forces an MRS update cycle

10.1.6 DDR Refresh Control and Configuration (DDR_REFRESH)

Address: 0x18000014
Access: Read/Write
Reset: See field description

This register is used to configure the settings to refresh the DDR.

Bit	Bit Name	Reset	Description
31:15	RES	0x0	Reserved
14	ENABLE	0x0	Setting this bit to one will enable a DDR refresh
13:0	PERIOD	0x12C	Sets the refresh period intervals with respect to the REF clock

10.1.7 DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE)

Address: 0x18000018
Access: Read/Write
Reset: See field description

This register is used to set the parameters to read the DDR and capture bit masks.

Bit	Bit Name	Reset	Description
31:0	VEC	0xFF	DDR read and capture bit mask. Each bit represents a cycle of valid data. Set to 0xFF for 32-bit wide memory systems and 0xFFFF for 16-bit wide memory systems.

10.1.8 DQS Delay Tap Control for Byte 0 (TAP_CONTROL_0)

Address: 0x1800001C
Access: Read/Write
Reset: See field description

This register is used along with DQ Lane 0, DQ[7:0], DQS_0.

Controls the delay in the DQS clock path. Used to position the DQS to the center of the EYE of DQ data signal.

Bit	Bit Name	Reset	Description
31:6	RES	0x0	Reserved
5:0	TAP	0x5	Tap setting for the delay chain of this line. 64 TAPS are available and can be set using these 6 bits

10.1.9 DQS Delay Tap Control for Byte 1 (TAP_CONTROL_1)

Address: 0x18000020
Access: Read/Write
Reset: See field description

This register is used along with DQ Lane 1, DQ[15:8], DQS_1.

Controls the delay in the DQS clock path. Used to position the DQS to the center of the EYE of DQ data signal.

Bit	Bit Name	Reset	Description
31:6	RES	0x0	Reserved
5:0	TAP	0x5	Tap setting for the delay chain of this line. 64 TAPS are available and can be set using these 6 bits

10.1.10 DQS Delay Tap Control for Byte 2 (TAP_CONTROL_2)

Address: 0x18000024
Access: Read/Write
Reset: See field description

This register is used along with DQ Lane 2, DQ[23:16], DQS_2.

Controls the delay in the DQS clock path. Used to position the DQS to the center of the EYE of DQ data signal.

Bit	Bit Name	Reset	Description
31:6	RES	0x0	Reserved
5:0	TAP	0x5	Tap setting for the delay chain of this line. 64 TAPS are available and can be set using these 6 bits

10.1.11 DQS Delay Tap Control for Byte 3 (TAP_CONTROL_3)

Address: 0x18000028
Access: Read/Write
Reset: See field description

This register is used along with DQ Lane 3, DQ[31:24], DQS_3.

Controls the delay in the DQS clock path. Used to position the DQS to the center of the EYE of DQ data signal.

Bit	Bit Name	Reset	Description
31:6	RES	0x0	Reserved
5:0	TAP	0x5	Tap setting for the delay chain of this line. 64 TAPS are available and can be set using these 6 bits

10.1.12 GE0 Interface Write Buffer Flush (DDR_WB_FLUSH_GE0)

Address: 0x1800009C
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the GE0 interface.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	Set this bit to 1 to flush the write buffer for the GE0 interface. This bit will reset to 0 when the flush is complete.

10.1.13 GE1 Interface Write Buffer Flush (DDR_WB_FLUSH_GE1)

Address: 0x180000A0
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the GE1 interface.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	Set this bit to 1 to flush the write buffer for the GE1 interface. This bit resets to 0 when the flush is complete.

10.1.14 USB Interface Write Buffer Flush (DDR_WB_FLUSH_USB)

Address: 0x180000A4
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the USB interface.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the USB interface. This bit will reset to 0 when the flush is complete.

10.1.15 PCIE Interface Write Buffer Flush (DDR_WB_FLUSH_PCIE)

Address: 0x180000A8
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the PCIE interface.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the PCIE interface. This bit resets to 0 when the flush is complete.

10.1.16 WMAC Interface Write Buffer Flush (DDR_WB_FLUSH_WMAC)

Address: 0x180000AC
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the WMAC interface.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the WMAC interface. This bit will reset to 0 when the flush is complete.

10.1.17 SRC1 Interface Write Buffer Flush (DDR_WB_FLUSH_MISC_SRC1)

Address: 0x180000B0
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the SRC1 (PCIE EP) interface.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the SRC1 interface. This bit resets to 0 when the flush is complete.

10.1.18 SRC2 Interface Write Buffer Flush (DDR_WB_FLUSH_SRC2)

Address: 0x180000B4
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the SRC2 (checksum engine) interface.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the SRC2 interface. This bit resets to 0 when the flush is complete.

10.1.19 DDR2 Configuration (DDR2_CONFIG)

Address: 0x180000B8
Access: Read/Write
Reset: 0x0858

Bit	Bit Name	Type	RW	Description	
31:14	RES	RO	0x0	Reserved	
13:10	DDR2_TWL	RW	0x1	Delays driving the data signals for writing commands with respect to command issue by TWL DDR clocks	
9:8	RES	RO	0x0	Reserved	
7:2	DDR2_TFAW	RW	0x16	tFAW parameter rounded up in memory core DDR_CLK cycles	
1	RES	RW	0x0	Reserved	
0	ENABLE_DDR2	RW	0x0	0	DDR1
				1	DDR2

10.1.20 DDR Extended Mode Value 2 (DDR_EMR2)

Address: 0x180000BC
Access: Read/Write
Reset: 0x0

This register is used to set the extended mode register 2 value.

Bit	Bit Name	Type	Reset	Description
31:13	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
12:0	VALUE	RW	0x0	See the DDR device data sheet for a detailed description of this register.

10.1.21 DDR Extended Mode Value 3 (DDR_EMR3)

Address: 0x180000C0
Access: Read/Write
Reset: 0x0

This register is used to set the extended mode register 3 value.

Bit	Bit Name	Type	Reset	Description
31:13	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
12:0	VALUE	RW	0x0	See the DDR device data sheet for a detailed description of this register.

10.1.22 DDR Bank Arbiter Per Client Burst Size (DDR_BURST)

Address: 0x180000C4
Access: Read/Write
Reset: See field description

NOTE Changes to this register is not recommended.

Bit	Bit Name	Reset	Description
31	CPU_PRIORITY	0x0	Setting this bit causes the bank arbiters to break current burst and grant CPU
30	CPU_PRIORITY_BE	0x1	Setting this bit causes the bank arbiters to break only at current burst completion and grant CPU
29:24	RES	0x3	Reserved
19:16	CPU_MAX_BL	0x0	CPU burst size
15:12	USB_MAX_BL	0x1	USB burst size
11:8	PCIE_MAX_BL	0x3	PCIE burst size
7:4	GE1_MAX_BL	0x4	GE1 burst size
3:0	GE0_MAX_BL	0x4	Ethernet burst size

10.1.23 DDR Bank Arbiter Per Client Burst Size 2 (DDR_BURST2)

Address: 0x180000C8
Access: Read/Write
Reset: See field description

NOTE Changes to this register is not recommended.

Bit	Bit Name	Reset	Description
31:12	RES	0x0	Reserved
11:8	MISC_SRC2_MAX_BL	0x2	MISC_SRC2 burst size
7:4	MISC_SRC1_MAX_BL	0x2	MISC_SRC1 burst size
3:0	WMAC_MAX_BL	0x2	WMAC burst size

10.1.24 AHB Master Timeout Control (DDR_AHB_MASTER_ TIMEOUT_MAX)

Address: 0x180000CC
Access: Read/Write
Reset: 0x0

This register specifies the maximum timeout value of the AHB master control.

Bit	Bit Name	Type	Reset	Description
31:20	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
19:0	VALUE	RW	0x8000	Maximum time out value

10.1.25 AHB Timeout Current Count (DDR_AHB_MASTER_ TIMEOUT_CURNT)

Address: 0x180000D0
Access: Read/Write
Reset: 0x0

This register specifies the current AHB timeout value.

Bit	Bit Name	Type	Reset	Description
31:20	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
19:0	VALUE	RO	0x0	Current time out value

10.1.26 Timeout Slave Address (AHB_MASTER_TIMEOUT_SLV_ ADDR)

Address: 0x180000D4
Access: Read/Write
Reset: 0x0

This register specifies the maximum timeout value to access the slave address space.

Bit	Bit Name	Type	Reset	Description
31:0	ADDR	RO	0x0	Maximum time out value

10.1.27 DDR Controller Configuration (DDR_CTL_CONFIG)

Address: 0x18000108
Access: Read/Write
Reset: 0x0

This register specifies the control bits for the DDR.

Bit	Bit Name	Type	Reset	Description	
31:30	RES	RW	0x1	Should not be modified	
29:21	CLIENT_ACTIVITY	RO	0x0	Indicates if there is currently any activity in each of the AHB/AXI/OCP clients connected to the DDR	
20:7	RES	RW	0x2	Should not be modified	
6	SEL_18	RW	0x0	Set to one for DDR2 configurations	
5	RES	RW	0x3	Reserved	
4	GATE_SRAM_CLK	RW	0x0	Gating setting for SRAM to clock	
				0	Clock to SRAM does not need to be gated
				1	Clock to SRAM needs to be gated.
3:2	RES	RW	0x3	Reserved	
1	HALF_WIDTH	RW	0x1	Enable to use only 2 DDR lanes	
0	MODE_EN	RW	0x0	Always set to 0 for DDR1 and DDR2 operation	

10.1.28 DDR Self Refresh Control (DDR_SF_CTL)

Address: 0x18000110
Access: Read/Write
Reset: 0x0

This register specifies the settings for the DDR self refresh mode.

Bit	Bit Name	Type	Reset	Description
31	EN_SELF_ REFRESH	RW	0x0	Setting this bit will initiate entering self refresh mode. This bit can be cleared by S/W or H/W if the auto exit is enabled
30	EN_AUTO_SF_ EXIT	RW	0x0	Setting this bit will initiate exiting self refresh mode upon DDR request from any AHB/AXI master
29	CUR_SR_STATE	RO	0x0	Indicates if the DDR is currently in self refresh mode
28	CUR_CKE_STATE	RO	0x0	Indicates if the DDR CKE is high or low
27	EN_SF_CLK_ GATING	RW	0x0	Setting this bit gates CK_P and CK_N during self refresh mode
26:25	CKE_GATE_DLY_ SEL	RW	0x0	Determines the delay of the CKE assertion from CK_P and stops gating when exiting self refresh mode
24:21	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
20:18	NO_ACTIVITY_ CNTR	RO	0x0	Indicates the duration on no activity in the AHB/AXI clients of the DDR in terms of the DDR refresh period
17:8	TXSRD	RW	0x1C2	Indicates XSND parameter of the memory in the number of DDR_CLKs
7:0	TXSNR	RW	0x3C	Indicates XSNR parameter of the memory in the number of DDR_CLKs

10.1.29 Self Refresh Timer (SF_TIMER)

Address: 0x18000114
Access: Read-Only
Reset: 0x0

This register specifies the DDR refresh periods for self refresh mode.

Bit	Bit Name	Description
31:16	RF_OUT_DPR_ COUNT	Indicates the number of DDR_REFRESH_PERIODs for which HW remained out of the self refresh mode
15:0	RES	Reserved

10.1.30 WMAC Flush (WMAC_FLUSH)

Address: 0x18000128
Access: Read/Write
Reset: 0x0

This register specifies the settings for the WMAC Flush.

Bit	Bit Name	Type	Reset	Description
31:10	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
9	DONE	RW	0x0	Set to 1 by HW after the flush is completed and the adapter is ready. SW clears it back to 0.
8:1	DDR_CLK_ CNTR	RW	0x28	Number of DDR clocks to count down after the last grant, ensuring all I/O reads are completed.
0	RES	RW	0x0	Should be left at the default value.

10.1.31 DDR Configuration 3 (DDR_CONFIG_3)

Address: 0x1800015C
Access: Read/Write
Reset: See field description

This register configures the DDR timing parameters.

Bit	Bit Name	Reset	Description
31:0	SPARE	0x0	Spare register bits
3	TWR_MSB	1d0	MSB of the TWR timing parameter expressed as a number of the internal DDR clock
2	TRAS_MSB	1d0	MSB of the TRAS timing parameter expressed as a number of the internal DDR clock
1:0	TRFC_LSB	2d0	TRFC timing parameter, LSB two bits, in terms of the internal DDR clock

10.2 I²C Configuration Registers

Table 10-4 summarizes the I²C configuration registers for the QCA9558.

Table 10-3 CPU Wrapper Registers Summary

Address	Name	Description	Page
0x18018000	IC_CON	I²C Configuration	page 164
0x18018004	IC_TAR	I²C Target Address	page 165
0x18018008	IC_SAR	I²C Slave Address	page 165
0x1801800C	IC_HS_MADDR	I²C HS Mode Master Code	page 165
0x18018010	IC_DATA_CMD	I²C Rx/Tx Data Buffer and Command	page 166
0x18018014	IC_SS_SCL_HCNT	Standard I²C Clock SCL High Count	page 166
0x18018018	IC_SS_SCL_LCNT	Standard I²C Clock SCL Low Count	page 167
0x1801801C	IC_FS_SCL_HCNT	Fast I²C Clock SCL High Count	page 167
0x18018020	IC_FS_SCL_LCNT	Fast I²C Clock SCL Low Count	page 168
0x18018024	IC_HS_SCL_HCNT	High Speed I²C Clock SCL High Count	page 168
0x18018028	IC_HS_SCL_LCNT	High Speed I²C Clock SCL Low Count	page 169
0x1801802C	IC_RAW_INTR_STAT	I²C Raw Interrupt Status	page 169
0x18018030	IC_INTR_MASK	I²C Interrupt Mask	page 171
0x18018034	IC_INTR_STAT	I²C Interrupt Status	page 171
0x18018038	IC_RX_TL	I²C Receive FIFO Threshold	page 173
0x1801803C	IC_TX_TL	I²C Transmit FIFO Threshold	page 173
0x18018040	IC_CLR_INTR	I²C Combined and Individual Interrupts Clear	page 173
0x18018044	IC_CLR_RX_UNDER	I²C Clear RX_UNDER Interrupts	page 174
0x18018048	IC_CLR_RX_OVER	I²C Clear RX_OVER Interrupts	page 174
0x1801804C	IC_CLR_TX_OVER	I²C Clear TX_OVER Interrupts	page 174
0x18018050	IC_CLR_RD_REQ	I²C Clear RD_REQ Interrupts	page 174
0x18018054	IC_CLR_TX_ABRT	I²C Clear TX_ABRT Interrupts	page 175
0x18018058	IC_CLR_RX_DONE	I²C Clear RX_DONE Interrupts	page 175
0x1801805C	IC_CLR_ACTIVITY	I²C Clear ACTIVITY Interrupts	page 175
0x18018060	IC_CLR_STOP_DET	I²C Clear STOP_DET Interrupts	page 175
0x18018064	IC_CLR_START_DET	I²C Clear START_DET Interrupts	page 176
0x18018068	IC_CLR_GEN_CALL	I²C Clear GEN_CALL Interrupts	page 176
0x1801806C	IC_ENABLE	I²C Enable	page 176
0x18018070	IC_STATUS	I²C Transfer and FIFO Status	page 177
0x18018074	IC_TXFLR	I²C Transmit FIFO Level	page 177
0x18018078	IC_RXFLR	I²C Receive FIFO Level	page 178
0x1801807C	IC_SRESET	I²C Soft Reset	page 178
0x18018080	IC_TX_ABRT_SOURCE	I²C TX Abort Source	page 179

10.2.1 I2C Configuration (IC_CON)

Address: 0x18018000
Access: Read-Write
Reset: See field description

This register can be written only when the DW_APB_I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Bit	Bit Name	Type	Reset	Description	
31:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
6	IC_SLAVE_ DISABLE	RW	0x0	Controls whether I2C has its slave disabled after reset. The slave can be disabled by programming a 1 into IC_CON. (Default = Enabled)	
				0	Slave is enabled
				1	Slave is disabled
5	IC_RESTART_EN	RW	0x1	Determines whether restart conditions may be sent when acting as a master. Some older slaves do not support handling restart conditions. Restart conditions are used in several DW_APB_I2C operations. Disabling a restart does not allow the master to perform these functions: 1. Send multiple bytes per transfer (split) 2. Change direction within a transfer (split) 3. Send a start byte 4. Perform any high-speed mode operation 5. Perform combined format transfers in 7- or 10-bit addressing modes (split for 7 bit) 6. Perform a read operation with a 10-bit address. Split operations are broken down into multiple DW_APB_I2C transfers with a stop and start condition in between. The other operations are not performed at all and result in setting TX_ABRT.	
4	IC_10BITADDR_ MASTER	RW	0x1	This bit controls whether the DW_APB_I2C starts its transfers in 10-bit addressing mode when acting as a master.	
				0	7-bit addressing
				1	10-bit addressing
3	IC_10BITADDR_ SLAVE	RW	0x1	When acting as a slave, this bit controls whether the DW_APB_I2C responds to 7- or 10-bit addresses.	
				0	7-bit addressing. The DW_APB_I2C ignores transactions which involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared.
				1	10-bit addressing. The DW_APB_I2C responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register.
2:1	SPEED	RW	0x3	Controls at which speed the DW_APB_I2C operates. If the DW_APB_I2C is configured for fast or standard mode (1 or 2) and a value of 2 or 3 is written, then IC_MAX_SPEED_MODE is stored.	
				0	Illegal; writing a 0 results in setting SPEED to IC_MAX_SPEED_ MODE
				1	Standard mode (100 KBps)
				2	Fast mode (400 KBps)
				3	High speed mode (3.4 MBps)
0	MASTER_MODE	RW	0x1	Controls whether the DW_APB_I2C master is enabled	
				0	Master disabled
				1	Master enabled

10.2.2 I2C Target Address (IC_TAR)

Address: 0x18018004
Access: Read-Write
Reset: See field description

This register can be written only when the DW_APB_I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Bit	Bit Name	Type	Reset	Description	
31:12	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
11	SPECIAL	RW	0x0	This bit indicates whether software would like to perform a general call or start byte I2C command.	
				0	Ignore bit 10 GC_OR_START and use IC_TAR normally
				1	Perform special I2C command as specified in GC_OR_START bit
10	GC_OR_ START	RW	0x0	If bit 11 SPECIAL is set to 1, then this bit indicates whether a general call or start byte command is to be performed by the DW_APB_I2C.	
				0	General Call Address: After issuing a general call, only writes may be performed. Attempting to issue a read sets TX_ABRT. DW_APB_I2C remains in general call mode until the SPECIAL bit value is cleared.
				1	Start Byte
9:0	IC_TAR	RW	0x055	The target address for any master transactions. **The reset value of IC_TAR is equal to IC_DEFAULT_TAR_SLAVE_ADDR which indicates loopback mode.	

10.2.3 I2C Slave Address (IC_SAR)

Address: 0x18018008
Access: Read-Only
Reset: See field description

This register holds the slave address when the I2C is operating as a slave. IC_SAR holds the slave address to which the DW_APB_I2C responds. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ ENABLE register being set to 0. Writes at other times have no effect.

Bit	Bit Name	Type	Reset	Description
31:10	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:0	IC_SAR	RO	0x55	Denotes the I2C slave address

10.2.4 I2C HS Mode Master Code (IC_HS_MADDR)

Address: 0x1801800C
Access: Read-Write
Reset: See field description

This register holds the I2C HS master mode code address.

Bit	Bit Name	Type	Reset	Description
31:3	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
2:0	IC_HS_MADDR	RO/RW	0x1	IC_HS_MAR holds the value of the I2C HS mode master code. Valid values are from 0-7. This register goes away and becomes read-only returning 0 s if IC_MAX_SPEED_MODE = high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect

10.2.5 I2C Rx/Tx Data Buffer and Command (IC_DATA_CMD)

Address: 0x18018010
Access: Read-Write
Reset: See field description

This register contains the data buffer and commands for I2C Rx/Tx.

Bit	Bit Name	Type	Reset	Description
31:9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
8	CMD	RW	0x0	This bit controls whether a read or a write is performed. For reads, the lower 8 (DAT) bits are ignored by the DW_APB_I2C. However, if the APB_DATA_WIDTH is 8, this dummy write is still required as there is coherency in this register. Reading this bit returns 0. Attempting to perform a read operation after a general call command has been sent results in TX_ABRT unless the SPECIAL bit in the IC_TAR register has been cleared. If this bit is written to a 1 after receiving RD_REQ, then a TX_ABRT occurs
				0 Write
				1 Read
7:0	DAT	RO	0x0	This register contains the data to be transmitted or received on the I2C bus. Read these bits to read out the data received on the I2C interface. Write these bits to send data out on the I2C interface.

10.2.6 Standard I2C Clock SCL High Count (IC_SS_SCL_HCNT)

Address: 0x18018014
Access: Read-Write
Reset: See field description

This register holds the standard speed I2C clock SCL high count.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	IC_SS_SCL_HCNT	RW	0x1D6	HCNT COUNT This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted, results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_APB_I2C. The lower byte must be programmed first, then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 6. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read-only.

10.2.7 Standard I2C Clock SCL Low Count (IC_SS_SCL_LCNT)

Address: 0x18018018
Access: Read-Write
Reset: See field description

This register holds the standard speed I2C clock SCL low count.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	IC_SS_SCL_ HCNT	RW	0x3C	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted, results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_ APB_I2C. The lower byte must be programmed first, then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 6. When the configuration parameter IC_HC_COUNT_ VALUES is set to 1, this register is read-only.

10.2.8 Fast I2C Clock SCL High Count (IC_FS_SCL_HCNT)

Address: 0x1801801C
Access: Read-Write
Reset: See field description

This register holds the fast speed I2C clock SCL high count.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	IC_FS_SCL_ HCNT	RW	0x82	This register must be set before any I2C bus transaction can take place to ensure proper I/ O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read only returning 0s if IC_MAX_ SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_APB_I2C. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 6. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

10.2.9 Fast I2C Clock SCL Low Count (IC_FS_SCL_LCNT)

Address: 0x18018020
Access: Read-Write
Reset: See field description

This register holds the fast speed I2C clock SCL low count.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	IC_FS_SCL_ LCNT	RW	0x190	This register must be set before any I2C bus transaction can take place to ensure proper I/ O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_ DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_APB_I2C. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 6. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

10.2.10 High Speed I2C Clock SCL High Count (IC_HS_SCL_HCNT)

Address: 0x18018024
Access: Read-Write
Reset: See field description

This register holds the high speed I2C clock SCL high count.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	IC_SS_SCL_ HCNT	RW	0x000C	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read only returning 0s if IC_MAX_SPEED_MODE = high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_ WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_APB_I2C. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 6. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

10.2.11 High Speed I2C Clock SCL Low Count (IC_HS_SCL_LCNT)

Address: 0x18018028
Access: Read-Write
Reset: See field description

This register holds the high speed I2C clock SCL low count.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	IC_SS_SCL_ HCNT	RW	0x0020	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. The SCL low time depends on the loading of the bus. For 100 pF loading, the SCL low time is 60ns; for 400pF loading, the SCL low time is 120 ns. This register goes away and becomes read only returning 0s if IC_MAX_SPEED_MODE = high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_ WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_APB_I2C. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 6. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

10.2.12 I2C Raw Interrupt Status (IC_RAW_INTR_STAT)

Address: 0x1801802C
Access: Read-Write
Reset: See field description

This register holds the raw internal statistics of the I2C. Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the DW_APB_I2C.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
11	GEN_CALL	RW	0x0	Indicates that a general call request was received. The DW_APB_I2C stores the received data in the RX buffer.
10	START_DET	RW	0x0	Indicates whether a start condition has occurred on the I2C interface
9	STOP_DET	RW	0x0	Indicates whether a stop condition has occurred on the I2C interface
8	ACTIVITY	RW	0x0	This bit captures DW_APB_I2C activity and stays set until it is cleared, regardless of the DW_APB_I2C going idle.
7	RX_DONE	RW	0x0	When the DW_APB_I2C is acting as a slave transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.

6	TX_ABRT	RW	0x0	In general, this bit is set to 1 when the DW_APB_I2C acting as a master is unable to complete a command that the processor has sent. The conditions that set TX_ABRT are: 1. No slave acknowledges after the address is sent. 2. The addressed slave does not acknowledge a byte of data. 3. Arbitration is lost. 4. Attempting to send a master command when configured only to be a slave. 5. IC_RESTART_EN bit in the IC_CON register is set to 0 (restart condition disabled), and the processor attempts to issue an I^2C function that is impossible to perform without using restart conditions, and those conditions are: a. High-speed master code is acknowledge. b. Start byte is acknowledged. c. General call address is not acknowledged. d. When a read request interrupt occurs and the processor has previously placed data in the TX buffer that has not been transmitted yet. This data could have been intended to service a multi-byte RD_REQ that ended up having fewer numbers of bytes requested. Or, if IC_RESTART_EN is disabled and the I2C loses control of the bus between transfers and is then accessed as a slave-transmitter. e. If a read command is issued after a general call command has been issued. Disabling the I^2C reverts it back to normal operation. f. If the processor attempts to issue read command before a RD_ REQ is serviced. Anytime this bit is set, the contents of the transmit and receive buffers are flushed
5	RD_REQ	RW	0x0	This bit is set to 1 when the DW_APB_I2C is acting as slave and another I^2C master is attempting to read data from our module. The DW_APB_I2C holds the I^2C bus in waiting state (SCL=0) until this interrupt is serviced. The processor must acknowledge this interrupt and then write the requested data to the IC_DATA_CMD register.
4	TX_EMPTY	RW	0x0	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. It is automatically cleared by hardware when buffer level goes above the threshold.
3	TX_OVER	RW	0x0	Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_ DEPTH and the processor attempts to issue another I^2C command by writing to the IC_DATA_CMD register.
2	RX_FULL	RW	0x0	Set when the transmit buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold.
1	RX_OVER	RW	0x0	Set if the receive buffer was completely filled to IC_RX_BUFFER_DEPTH and more data arrived. That data is lost.
0	RX_UNDER	RW	0x0	Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

10.2.13 I2C Interrupt Mask (IC_INTR_MASK)

Address: 0x18018030
Access: Read-Write
Reset: See field description

This register's bits mask their corresponding interrupt status bits. They are active high; a value of 0 prevents a bit from generating an interrupt.

Bit	Bit Name	Type	Reset	Description
31:12	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
11	M_GEN_CALL	RW	0x0	Masks this bit in the I2C Interrupt Status (IC_INTR_STAT) register
10	M_START_DET	RW	0x0	Masks this bit in the IC_INTR_STAT register
9	M_STOP_DET	RW	0x0	Masks this bit in the IC_INTR_STAT register
8	M_ACTIVITY	RW	0x0	Masks this bit in the IC_INTR_STAT register
7	M_RX_DONE	RW	0x1	Masks this bit in the IC_INTR_STAT register
6	M_TX_ABRT	RW	0x1	Masks this bit in the IC_INTR_STAT register
5	M_RD_REQ	RW	0x1	Masks this bit in the IC_INTR_STAT register
4	M_TX_EMPTY	RW	0x1	Masks this bit in the IC_INTR_STAT register
3	M_TX_OVER	RW	0x1	Masks this bit in the IC_INTR_STAT register
2	M_RX_FULL	RW	0x1	Masks this bit in the IC_INTR_STAT register
1	M_RX_OVER	RW	0x1	Masks this bit in the IC_INTR_STAT register
0	M_RX_UNDER	RW	0x1	Masks this bit in the IC_INTR_STAT register

10.2.14 I2C Interrupt Status (IC_INTR_STAT)

Address: 0x18018034
Access: Read-Write
Reset: See field description

This register denotes the interrupt status of the I2C.

Bit	Bit Name	Type	Reset	Description
31:12	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
11	R_GEN_CALL	RW	0x0	Indicates that a general call request was received. The DW_APB_I2C stores the received data in the RX buffer
10	R_START_DET	RW	0x0	Indicates whether a start condition has occurred on the I2C interface
9	R_STOP_DET	RW	0x0	Indicates whether a stop condition has occurred on the I2C interface
8	R_ACTIVITY	RW	0x0	This bit captures DW_APB_I2C activity and stays set until it is cleared, regardless of the DW_APB_I2C going idle.
7	R_RX_DONE	RW	0x0	When the DW_APB_I2C is acting as a slave transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.

6	R_TX_ABRT	RW	0x0	In general, this bit is set to 1 when the DW_APB_I2C acting as a master is unable to complete a command that the processor has sent. The conditions that set TX_ABRT are: 1. No slave acknowledges after the address is sent. 2. The addressed slave does not acknowledge a byte of data. 3. Arbitration is lost. 4. Attempting to send a master command when configured only to be a slave. 5. IC_RESTART_EN bit in the I2C Configuration (IC_CON) register is set to 0 (restart condition disabled), and the processor attempts to issue an I^2C function that is impossible to perform without using restart conditions, and those conditions are: a. high-speed master code is acknowledge. b. start byte is acknowledged. c. general call address is not acknowledged. d. when a read request interrupt occurs and the processor has previously placed data in the Tx buffer that has not been transmitted yet. This data could have been intended to service a multi-byte RD_REQ that ended up having fewer numbers of bytes requested. Or, if IC_RESTART_EN is disabled and the I^2C loses control of the bus between transfers and is then accessed as a slave-transmitter. e. if a read command is issued after a general call command has been issued. Disabling the I^2C reverts it back to normal operation. f. if the processor attempts to issue read command before a RD_ REQ is serviced. Anytime this bit is set, the contents of the transmit and receive buffers are flushed.
5	R_RD_REQ	RW	0x0	This bit is set to 1 when the DW_APB_I2C is acting as slave and another I^2C master is attempting to read data from our module. The DW_APB_I2C holds the I^2C bus in waiting state (SCL=0) until this interrupt is serviced. The processor must acknowledge this interrupt and then write the requested data to the I2C Rx/Tx Data Buffer and Command (IC_DATA_ CMD) register.
4	R_TX_EMPTY	RW	0x0	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I2C Transmit FIFO Threshold (IC_TX_TL) register. It is automatically cleared by hardware when buffer level goes above the threshold.
3	R_TX_OVER	RW	0x0	Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_ DEPTH and the processor attempts to issue another I^2C command by writing to the I2C Rx/Tx Data Buffer and Command (IC_DATA_CMD) register.
2	R_RX_FULL	RW	0x0	Set when the transmit buffer reaches or goes above the RX_TL threshold in the I2C Receive FIFO Threshold (IC_RX_TL) register. It is automatically cleared by hardware when buffer level goes below the threshold.
1	R_RX_OVER	RW	0x0	Set if the receive buffer was completely filled to IC_RX_BUFFER_DEPTH and more data arrived. That data is lost.
0	R_RX_UNDER	RW	0x0	Set if the processor attempts to read the receive buffer when it is empty by reading from the I2C Rx/Tx Data Buffer and Command (IC_DATA_CMD) register.

10.2.15 I2C Receive FIFO Threshold (IC_RX_TL)

Address: 0x18018038
Access: Read-Write
Reset: See field description

This register contains the threshold settings for the I2C receive FIFO.

Bit	Bit Name	Type	Reset	Description
31:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	RX_TL	RW	0x0	The receive FIFO Threshold Level controls the level of entries (or above) that triggers the RX_FULL interrupt. The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries. The core, in our case, is configured to use only 0-63

10.2.16 I2C Transmit FIFO Threshold (IC_TX_TL)

Address: 0x18018000
Access: Read-Write
Reset: See field description

This register contains the threshold settings for the I2C transmit FIFO.

Bit	Bit Name	Type	Reset	Description
31:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	TX_TL	RW	0x0	Transmit FIFO Threshold Level Controls the level of entries (or below) that trigger the TX_EMPTY interrupt. The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries. The core, in our case, is configured to use only 0-15

10.2.17 I2C Combined and Individual Interrupts Clear (IC_CLR_INTR)

Address: 0x18018040
Access: Read-Write
Reset: See field description

This register clears the combined and individual I2C interrupts.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_INTR	RW	0x0	Read this register to clear the combined interrupt, all individual interrupts, and the I2C TX Abort Source (IC_TX_ABRT_SOURCE) register.

10.2.18 I²C Clear RX_UNDER Interrupts (IC_CLR_RX_UNDER)

Address: 0x18018044
Access: Read-Only
Reset: See field description

This register clears the RX_UNDER interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_RX_UNDER	RO	0x0	Read this register to clear the RX_UNDER interrupt.

10.2.19 I²C Clear RX_OVER Interrupts (IC_CLR_RX_OVER)

Address: 0x18018048
Access: Read-Only
Reset: See field description

This register clears the RX_OVER interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_RX_OVER	RO	0x0	Read this register to clear the RX_OVER interrupt.

10.2.20 I²C Clear TX_OVER Interrupts (IC_CLR_TX_OVER)

Address: 0x1801804C
Access: Read-Only
Reset: See field description

This register clears the TX_OVER interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_TX_OVER	RO	0x0	Read this register to clear the TX_OVER interrupt.

10.2.21 I²C Clear RD_REQ Interrupts (IC_CLR_RD_REQ)

Address: 0x18018050
Access: Read-Only
Reset: See field description

This register clears the RD_REQ interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_RD_REQ	RO	0x0	Read this register to clear the RD_REQ interrupt.

10.2.22 I2C Clear TX_ABRT Interrupts (IC_CLR_TX_ABRT)

Address: 0x18018054
Access: Read-Only
Reset: See field description

This register clears the TX_ABRT interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_TX_ABRT	RO	0x0	Read this register to clear the TX_ABRT interrupt and IC_TX_ABRT_SOURCE.

10.2.23 I2C Clear RX_DONE Interrupts (IC_CLR_RX_DONE)

Address: 0x18018058
Access: Read-Only
Reset: See field description

This register clears the RX_DONE interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_RX_DONE	RO	0x0	Read this register to clear the RX_DONE interrupt

10.2.24 I2C Clear ACTIVITY Interrupts (IC_CLR_ACTIVITY)

Address: 0x1801805C
Access: Read-Only
Reset: See field description

This register clears the ACTIVITY status interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_ACTIVITY	RO	0x0	Read this register to get the status of the ACTIVITY interrupt. This bit is automatically cleared by hardware

10.2.25 I2C Clear STOP_DET Interrupts (IC_CLR_STOP_DET)

Address: 0x18018060
Access: Read-Only
Reset: See field description

This register clears the STOP_DET interrupts register.

Bit	Bit Name	Type	Reset	Description

31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_STOP_DET	RO	0x0	Read this register to clear the STOP_DET interrupt

10.2.26 I2C Clear START_DET Interrupts (IC_CLR_START_DET)

Address: 0x18018064
Access: Read-Only
Reset: See field description

This register clears the START_DET interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_START_DET	RO	0x0	Read this register to clear the START_DET interrupt

10.2.27 I2C Clear GEN_CALL Interrupts (IC_CLR_GEN_CALL)

Address: 0x18018068
Access: Read-Only
Reset: See field description

This register clears the GEN_CALL interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_GEN_CALL	RO	0x0	Read this register to clear the GEN_CALL interrupt

10.2.28 I2C Enable (IC_ENABLE)

Address: 0x1801806C
Access: Read-Write
Reset: See field description

This registers enables I2C.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	ENABLE	RW	0x0	Controls whether the DW_APB_I2C is enabled. Writing a 1 enables the DW_APB_I2C, and writing a 0 disables it. Software should not disable the DW_APB_I2C while it is active. The ACTIVITY bit can be polled to determine if the DW_APB_I2C is active. If the module was transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module was receiving, the DW_APB_I2C stops the current transfer at the end of the current byte and does not acknowledge the transfer. In systems with asynchronous PCLK and IC_CLK (IC_CLK_TYPE = 1), there is a two IC_CLK delay when enabling or disabling the DW_APB_I2C.

10.2.29 I2C Transfer and FIFO Status (IC_STATUS)

Address: 0x18018070
Access: Read-Write
Reset: See field description

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
4	REF	RW	0x0	Receive FIFO completely Empty. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty locations, this bit is cleared.
			0	Receive FIFO is not full
			1	Receive FIFO is full
3	RFNE	RW	0x0	Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO.
			0	Receive FIFO is empty
			1	Receive FIFO is not empty
2	TFE	RW	0x1	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
			0	Transmit FIFO is not empty
			1	Transmit FIFO is empty
1	TFNF	RW	0x1	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
			0	Transmit FIFO is full
			1	Transmit FIFO is not full
0	ACTIVITY	RW	0x0	I2C activity status

10.2.30 I2C Transmit FIFO Level (IC_TXFLR)

Address: 0x18018074
Access: Read-Only
Reset: See field description

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared when the I2C is disabled, whenever there is a transmit abort, or whenever the Slave Bulk Transfer mode is aborted. It increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Bit	Bit Name	Type	Reset	Description
31:4	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
3:0	TX_FLR	RW	0x0	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

10.2.31 I2C Receive FIFO Level (IC_RXFLR)

Address: 0x18018078
Access: Read-Only
Reset: See field description

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared when the I2C is disabled, whenever there is a transmit abort, or whenever the Slave Bulk Transfer mode is aborted. It increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Bit	Bit Name	Type	Reset	Description
31:4	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
3:0	RX_FLR	RW	0x0	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO

10.2.32 I2C Soft Reset (IC_SRESET)

Address: 0x1801807C
Access: Read-Write
Reset: See field description

This register is used to issue a soft reset to the master and/or the slave state machines. Reading this register does not clear it; it is automatically cleared by hardware.

Bit	Bit Name	Type	Reset	Description
31:3	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
2	IC_SLAVE_SRST	RW	0x0	Issues a soft reset to the slave state machines. 1 = perform the reset
1	IC_MASTER_SRST	RW	0x0	Issues a soft reset to the master state machines. 1 = perform the reset
0	IC_SRST	RW	0x0	Issues a soft reset to the master and slave state machines.

10.2.33 I2C TX Abort Source (IC_TX_ABRT_SOURCE)

Address: 0x18018080
Access: Read-Write
Reset: See field description

This register has 16 bits that indicate the source of the TX_ABRT signal, This register is cleared whenever the processor reads it or when the processor issues a clear signal to all interrupts.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15	ABRT_SLVRD_ INTX	RW	0x0	Writing a 1 to this bit denotes a slave requesting data to TX and the user writing a read command into the TX_FIFO (9th bit is a 1)
14	ABRT_SLV_ ARBLOST	RW	0x0	Writing a 1 to this bit denotes a slave lost the bus while transmitting data to a remote master. IC_TX_ABRT[12] will be set at the same time
13	ABRT_ SLVFLUSH_ TXFIFO	RW	0x0	Writing a 1 to this bit denotes a slave has received a read command and some data exists in the TX_FIFO so the slave issues a TX_ABRT to flush old data in TX_FIFO.
12	ARB_LOST	RW	0x0	Writing a 1 to this bit denotes a Master has lost arbitration, or if TX_ ABRT_SRC[12] is also set, then the slave transmitter has lost arbitration
11	ARB_MASTER_ DIS	RW	0x0	Writing a 1 to this bit denotes a user attempted to use a disabled Master
10	ABRT_10B_RD_ NORSTRT	RW	0x0	Writing a 1 to this bit disables the restart (IC_RESTART_EN bit (ic_ con[5]) = 0) and the Master sends a read command in 10-bit addressing mode.
9	ABRT_SBYTE_ NORSTRT	RW	0x0	Writing a 1 to this bit disables the restart (IC_RESTART_EN bit (ic_ con[5]) = 0) and the user is trying to send a Start Byte.
8	ABRT_HS_ NORSTRT	RW	0x0	Writing a 1 to this bit disables the restart (IC_RESTART_EN bit (ic_ con[5]) = 0) and the user is trying to use the master to send data in High Speed mode.
7	ABRT_SBYTE_ ACKDET	RW	0x0	Writing a 1 to this bit denotes a Master has sent a Start Byte and the Start Byte was acknowledged (wrong behavior)
6	ABRT_HS_ ACKDET	RW	0x0	Writing a 1 to this bit denotes a Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior)
5	ABRT_GCALL_ READ	RW	0x0	Writing a 1 to this bit denotes a Master sent a general call but the user programmed the byte following the G.CALL to be a read from the bus (9th bit is set to 1)
4	ABRT_GCALL_ NOACK	RW	0x0	Writing a 1 to this bit denotes a Master sent a general call and no slave on the bus responded with an acknowledgement
3	ABRT_TX_DATA_ NOACK	RW	0x0	Writing a 1 to this bit denotes a Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	ABRT_10ADDR2_ NOACK	RW	0x0	Writing a 1 to this bit denotes a Master is in 10-bit address mode and the 2nd address byte of the 10-bit address was not acknowledged by any slave.
1	ABRT_10ADDR1_ NOACK	RW	0x0	Writing a 1 to this bit denotes a Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave
0	ABRT_7B_ADDR_ NOACK	RW	0x0	Writing a 1 to this bit denotes a Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

10.3 UART0 (Low-Speed) Registers

Table 10-4 summarizes the UART0 registers for the QCA9558.

Table 10-4 UART0 (Low-Speed) Registers Summary

Address	Name	Description	Page
0x18020000	RBR	Receive Buffer	page 180
0x18020000	THR	Transmit Holding	page 181
0x18020000	DLL	Divisor Latch Low	page 181
0x18020004	DLH	Divisor Latch High	page 181
0x18020004	IER	Interrupt Enable	page 182
0x18020008	IIR	Interrupt Identity	page 182
0x18020008	FCR	FIFO Control	page 183
0x1802000C	LCR	Line Control	page 184
0x18020010	MCR	Modem Control	page 184
0x18020014	LSR	Line Status	page 185
0x18020018	MSR	Modem Status	page 186

10.3.1 Receive Buffer (RBR)

Address: 0x18020000
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description	
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.	
7:0	RBR	Receive buffer register value Contains the data byte received on the serial input port (sin). The data in this register is valid only if the Data Ready (DR) bit in the Line Status (LSR) register is set.	
		Non-FIFO Mode (fifo_mode = 0)	The data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error
		FIFO Mode (fifo_mode = 1)	Accesses the head of the Rx FIFO If the Rx FIFO is full and this register is not read before the next data character arrives, the data already in the FIFO is preserved but any incoming data is lost and an overrun error also occurs.

10.3.2 Transmit Holding (THR)

Address: 0x18020000
Access: Write-Only
Reset: 0x0

Bit	Bit Name	Description	
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.	
7:0	THR	Tx buffer value Contains data to be transmitted on the serial output port (S_{out}). Data can be written to the THR any time that the THR Empty (THRE) bit of the Line Status (LSR) register is set.	
		Non-FIFO Mode (fifo_mode = 0)	If THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.
		FIFO Mode (fifo_mode = 1)	If THRE is set, up to 16 characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

10.3.3 Divisor Latch Low (DLL)

Address: 0x18020000
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Type	Reset	Description
31:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	DLL	RW	0x0	Divisor latch low In conjunction with the Divisor Latch High (DLH) register, forms a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. It is accessed by first setting the DLAB bit (bit [7]) in the Line Control (LCR) register. The output baud rate is equal to the input clock frequency divided by sixteen times the value of the baud rate divisor, shown as follows: baud = (clock freq) /(16 * divisor).

10.3.4 Divisor Latch High (DLH)

Address: 0x18020004
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	DLH	Divisor latch high In conjunction with the Divisor Latch Low (DLL) register, forms a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. It is accessed by first setting the DLAB bit (bit 7) in the Line Control (LCR) register. The output baud rate is equal to the input clock frequency divided by sixteen times the value of the baud rate divisor, shown as follows: baud = (clock freq) /(16 * divisor).

10.3.5 Interrupt Enable (IER)

Address: 0x18020004
Access: Read/Write
Reset: 0x0

This register contains four bits that enable the generation of interrupts.

Bit	Bit Name	Description
31:4	RES	Reserved. Must be written with zero; contains zeros when read
3	EDDSI	Enable modem status interrupt
2	ELSI	Enable receiver line status interrupt
1	ETBEI	Enable register empty interrupt
0	ERBFI	Enable received data available interrupt

10.3.6 Interrupt Identity (IIR)

Address: 0x18020008
Access: Read-Only
Reset: 0x0

This register identifies the source of an interrupt. The two upper bits of the register are FIFO-enabled bits.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7:6	FIFO_STATUS	FIFO enable status bits	
		00	FIFO disabled
		11	FIFO enabled
5:4	RES	Reserved	
3:0	IID	Used to identify the source of the interrupt	
		0000	Modem status changed
		0001	No interrupt pending
		0010	THR empty
		0100	Received data available
		0110	Receiver status
		1100	Character time out

10.3.7 FIFO Control (FCR)

Address: 0x18020008
Access: Write-Only
Reset: 0x0

This register sets the parameters for FIFO control and returns current time values.

- If FIFO mode is 0, this register has no effect.
- If FIFO mode is 1, this register controls the read and write data FIFO operation and the mode of operation for the DMA signals TXRDY_N and RXRDY_N.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7:6	RCVR_TRIG	Sets the trigger level in the receiver FIFO for both the RXRDY_N signal and the Enable received data available interrupt (ERBFI)	
		00	1 byte in FIFO
		01	4 bytes in FIFO
		10	8 bytes in FIFO
		11	14 bytes in FIFO
5:4	RES	Reserved	
3	DMA_MODE	Determines the DMA signalling mode for TXRDY_N and RXRDY_N output signals	
2	XMIT_FIFO_RST	Writing this bit resets and flushes data in the transmit FIFO	
1	RCVR_FIFO_RST	Writing this bit resets and flushes data in the receive FIFO	
0	FIFO_EN	Setting this bit enables the transmit and receive FIFOs. The FIFOs are also reset any time this bit changes its value.	

10.3.8 Line Control (LCR)

Address: 0x1802000C
Access: Read/Write
Reset: 0x0

This register controls the format of the data transmitted and received by the UART controller.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7	DLAB	Divisor latch address bit. Setting this bit enables reading and writing of the Divisor Latch Low (DLL) and Divisor Latch High (DLH) registers to set the baud rate of the UART0. This bit must be cleared after the initial baud rate setup in order to access the other registers.	
6	BREAK	Setting this bit sends a break signal by holding the SOUT line low (when not in loopback mode, as determined by Modem Control (MCR) register bit [4]), until the BREAK bit is cleared. When in loopback mode, the break condition is internally looped back to the receiver.	
5	RES	Reserved	
4	EPS	Used to set the even/odd parity. If parity is enabled, this bit selects between even and odd parity. If this bit is a logic 1, an even number of logic 1s are transmitted or checked. If this bit is a logic 0, an odd number of logic 1s are transmitted or checked.	
3	PEN	Used to enable parity when set	
2	STOP	Used to control the number of stop bits transmitted. If this bit is a logic 0, one-stop bit is transmitted in the serial data. If this bit is a logic 1 and the data bits are set to 5, one and a half stop bits are generated. Otherwise, two stop bits generate and transmit in the serial data out.	
1:0	CLS	Controls the number of bits per character	
		00	5 bits
		01	6 bits
		10	7 bits
		11	8 bits

10.3.9 Modem Control (MCR)

Address: 0x18020010
Access: Read/Write
Reset: See field description

This register controls the interface with the modem.

Bit	Bit Name	Reset	Description
31:6	RES	0x0	Reserved
5	LOOPBACK	0x1	When set, the data on the SOUT line is held HIGH, while the serial data output is looped back to the SIN line, internally. In this mode, all the interrupts are fully functional. This feature is also used for diagnostic purposes. The modem control inputs (DSR_L, CTS_L, RI_L, DCD_L) are disconnected and the four modem control outputs (DTR_L, RTS_L, OUT1_L, OUT1_L) are looped back to the inputs, internally.
4	RES	0x0	Reserved
3	OUT2	0x1	Used to drive the UART output
2	OUT1	0x1	Used to drive the UART output
1	RTS	0x1	Used to drive the UART output RTS_L
0	DTR	0x1	Used to drive the UART output DTR_L. Not supported.

10.3.10 Line Status (LSR)

Address: 0x18020014
Access: Read/Write
Reset: 0x0

This register contains the status of the receiver and transmitter data transfers. This status may be read by the user at any time.

Bit	Bit Name	Description
31:8	RES	Reserved
7	FERR	Error in receiver FIFO. This bit is only active when FIFOs are enabled. It is set with at least one parity error, framing error, or break indication in the FIFO. It is cleared when this register is read, and the character with the error is at the top of the Rx FIFO, and no subsequent errors exist in the FIFO.
6	TEMT	Transmitter empty. In the FIFO mode, this bit is set whenever the transmitter shift register and the FIFO are both empty. In the non-FIFO mode, this bit is set whenever the Transmit Holding (THR) register and the transmitter shift register are both empty.
5	THRE	Transmitter holding register empty. When set, this bit indicates UART controller can accept a new character for transmission. This bit is set whenever data is transferred from the Transmit Holding (THR) register to the transmitter shift register and no new data has been written to the THR. Also causes a THRE interrupt to occur, if the THRE Interrupt is enabled.
4	BI	Break interrupt. This bit is set whenever the serial input (sin) is held in a logic zero state for longer than start time + data bits + parity + stop bits. A break condition on sin causes one and only one character, consisting of all zeros to be received by the UART. In FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading this register clears this bit. In non FIFO mode, the BI indication occurs immediately and persists until LSR is read.
3	FE	Framing error. This bit is set whenever there is a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In FIFO mode, because the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. The OE, PE, and FE bits are reset when a read of LSR is performed.
2	PE	Parity error. This bit is set whenever there is a parity error in the receiver if the PEN bit in the Line Control (LCR) is set. In FIFO mode, because the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO.
1	OE	Overrun error. When set, indicates an overrun error has occurred because a new data character was received before the previous data was read. In non-FIFO mode, this bit is set when a new character arrives in the receiver before the previous character was read from the Receive Buffer (RBR) register. When this happens, the data in the RBR is overwritten. In FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost.
0	DR	Data ready. When set, this bit indicates the receiver contains at least one character in the RBR or the Rx FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty, in the FIFO mode.

10.3.11 Modem Status (MSR)

Address: 0x18020018
Access: Read/Write
Reset: 0x0

This register contains the current status of the modem control input lines and notes whether they have changed.

Bit	Bit Name	Description
31:8	RES	Reserved
7	DCD	Contains information on the current state of the modem control lines; complement of DCD_L
6	RI	Contains information on the current state of the modem control lines; complement of RI_L
5	DSR	Contains information on the current state of the modem control lines; complement of DSR_L
4	CTS	Contains information on the current state of the modem control lines; complement of CTS_L
3	DDCD	Records whether modem control line DCD_L changed since the last time the CPU read the MSR
2	TERI	Indicates whether RI_L changed from an active low to inactive high since MSR was last read
1	DDSR	Records whether the modem control line DSR_L has changed since the last time the CPU read the MSR
0	DCTS	Records whether the modem control line CTS_L has changed since the last time the CPU read the MSR

10.4 USB Registers

Table 10-5 summarizes the USB registers for the QCA9558.

Table 10-5 USB Registers Summary

Address	Name	Description	Page
0x18030000	USB_PWRCTL	USB Power Control	page 187
0x18030004	USB_CONFIG	USB Configuration Control	page 188
0x18030008	USB_DEV_SUSPEND_CTRL	USB Device Suspend Control	page 188
0x1803000C	SUSPEND_RESUME_CNTR	USB Suspend Resume Counters	page 189
0x18030010	USB2_PWRCTL	USB2 Power Control	page 189
0x18030014	USB2_CONFIG	USB2 Configuration Control	page 190
0x1803001C	ARBITER_CONFIG	Arbiter Configuration	page 190

10.4.1 USB Power Control (USB_PWRCTL)

Address: 0x18030000
Access: Read/Write
Reset: 0x0

This register contains status and control bits for USB power control.

Bit	Bit Name	Description
31:7	RES	Reserved
6	WAKEUP_STATUS	Final wakeup status that wakes up the USB core
5	USR_WAKEUP	User wakeup signal. Input that clears suspend output. All suspend outputs are synchronized to the appropriate clock and this input will not propagate to the suspend outputs until the related clock begins running. Thus it must remain asserted until the related suspend output transitions to zero.
4	WAKE_OVRCURR_EN	Wakeup status because of power fault
3	WAKE_DSCNNT_EN	Wakeup status because of a disconnect event
2	WAKE_CNNT_EN	Wakeup status because of connect event
1	SUSPEND_CLR	Output to notify of software commanded wake up; this bit is not synchronized and remains set until the SUSPEND bit (bit [0]) of this register is cleared.
0	SUSPEND	Suspend output synchronized to the XCVR_CLK.

10.4.2 USB Configuration Control (USB_CONFIG)

Address: 0x18030004
Access: Read/Write
Reset: See field description

This register controls the basic configuration for the USB controller.

Bit	Bit Name	Reset	Description	
31:5	RES	0x1	Reserved	
4	HOST_OR_DEVICE	0x1	0	Indicates operation in device mode
			1	Indicates operation in host mode
3	AHB_HRDATA_SWAP	0x1	Swaps the read data on AHB bus	
2	AHB_HWDATA_SWAP	0x1	Swaps the write data on the AHB bus	
1	HS_MODE_EN	0x1	Enables high speed mode	
0	UTMI_PHY_EN	0x1	Asserted when selecting the UTMI mode	

10.4.3 USB Device Suspend Control (USB_DEV_SUSPEND_CTRL)

Address: 0x18030008
Access: Read/Write
Reset: 0x0

This register contains the bits to control the suspend related parameters and enables SUSPEND operation.

Bit	Bit Name	Description	
31:3	RES	Reserved	
2	GPIO_SUSP_POLARITY	Control to determine the polarity of the suspend signal coming on GPIO.	
		0	Suspend is active low
		1	Suspend is active high
1	RESET_ON_RESUME	If set to 1 before USB suspend, then the USB host triggers a FULL_CHIP_ RESET on a RESUME signal	
0	MASTER_SUSP_EN	Master enable for suspend that puts the entire chip in power down mode. The CPU must set this bit as the last operation before moving to suspend/power-down state	

10.4.4 USB Suspend Resume Counters (SUSPEND_RESUME_CNTR)

Address: 0x1803000C
Access: Read/Write
Reset: 0x1F00EA60

This register contains counters that set up timings for suspend entry and exit.

Bit	Bit Name	Description
31:24	SUSP_ENTER_CNTR	Countdown timer. Forces device entry to suspend once the counter reaches zero.
23:18	RES	Reserved
17:0	SUSP_EXIT_CNTR	Countdown timer for suspend exit. Waits until it reaches zero before resume event is signalled to CPU.

10.4.5 USB2 Power Control (USB2_PWRCTL)

Address: 0x18030010
Access: Read/Write
Reset: 0x0

This register contains status and control bits for USB2 power control.

Bit	Bit Name	Description
31:7	RES	Reserved
6	WAKEUP_STATUS	Final wakeup status that wakes up the USB2 core
5	USR_WAKEUP	User wakeup signal. Input that clears suspend output. All suspend outputs are synchronized to the appropriate clock and this input will not propagate to the suspend outputs until the related clock begins running. Thus it must remain asserted until the related suspend output transitions to zero.
4	WAKE_OVRCURR_EN	Wakeup status because of power fault
3	WAKE_DSCNNT_EN	Wakeup status because of a disconnect event
2	WAKE_CNNT_EN	Wakeup status because of connect event
1	SUSPEND_CLR	Output to notify of software commanded wake up; this bit is not synchronized and remains set until the SUSPEND bit (bit [0]) of this register is cleared.
0	SUSPEND	Suspend output synchronized to the XCVR_CLK.

10.4.6 USB2 Configuration Control (USB2_CONFIG)

Address: 0x18030014
Access: Read/Write
Reset: See field description

This register controls the basic configuration for the USB2 controller.

Bit	Bit Name	Reset	Description	
31:5	RES	0x1	Reserved	
4	HOST_OR_DEVICE	0x1	0	Indicates operation in device mode
			1	Indicates operation in host mode
3	AHB_HRDATA_SWAP	0x1	Swaps the read data on AHB bus	
2	AHB_HWDATA_SWAP	0x1	Swaps the write data on the AHB bus	
1	HS_MODE_EN	0x1	Enables high speed mode	
0	UTMI_PHY_EN	0x1	Asserted when selecting the UTMI mode	

10.4.7 Arbiter Configuration (ARBITER_CONFIG)

Address: 0x1803001C
Access: Read/Write
Reset: 0x48

This register contains counters that set up timings for suspend entry and exit.

Bit	Bit Name	Description
31:11	RES	Reserved
10	DISABLE_BURST_CNT	Disables the switching grant feature if the max burst count is crossed
9:0	MAX_BURST_CNT	Indicates the max burst count for one requestor.

10.5 GPIO Registers

Table 10-6 summarizes the GPIO registers for the QCA9558.

Table 10-6 General Purpose I/O (GPIO) Registers Summary

Address	Name	Description	Page
0x18040000	GPIO_OE	GPIO Output Enable	page 192
0x18040004	GPIO_IN	GPIO Input Value	page 192
0x18040008	GPIO_OUT	GPIO Output Value	page 192
0x1804000C	GPIO_SET	GPIO Per Bit Set	page 192
0x18040010	GPIO_CLEAR	GPIO Per Bit Clear	page 193
0x18040014	GPIO_INT	GPIO Interrupt Enable	page 193
0x18040018	GPIO_INT_TYPE	GPIO Interrupt Type	page 193
0x1804001C	GPIO_INT_POLARITY	GPIO Interrupt Polarity	page 193
0x18040020	GPIO_INT_PENDING	GPIO Interrupt Pending	page 194
0x18040024	GPIO_INT_MASK	GPIO Interrupt Mask	page 194
0x18040028	GPIO_SPARE	GPIO Spare bits	page 194
0x1804002C	GPIO_OUT_FUNCTION0	GPIO Pins 0, 1, 2, 3 Output Multiplexing	page 195
0x18040030	GPIO_OUT_FUNCTION1	GPIO Pins 4, 5, 6, 7 Output Multiplexing	page 195
0x18040034	GPIO_OUT_FUNCTION2	GPIO Pins 8, 9, 10, 11 Output Multiplexing	page 196
0x18040038	GPIO_OUT_FUNCTION3	GPIO Pins 12, 13, 14, 15 Output Multiplexing	page 196
0x1804003C	GPIO_OUT_FUNCTION4	GPIO Pins 16, 17, 18, 19 Output Multiplexing	page 197
0x18040040	GPIO_OUT_FUNCTION5	GPIO Pins 20, 21, 22, 23 Output Multiplexing	page 197
0x18040044	GPIO_IN_ENABLE0	UART0_SIN and SPI_DATA_IN Multiplexing	page 197
0x18040048	GPIO_IN_ENABLE1	I^2S Interface Multiplexing	page 198
0x1804004C	GPIO_IN_ENABLE2	ETH_RX related Multiplexing	page 198
0x18040050	GPIO_IN_ENABLE3	External MDIO Multiplexing	page 198
0x18040054	GPIO_IN_ENABLE4	SLIC Interface Multiplexing	page 199
0x18040068	GPIO_IN_ENABLE9	UART1 Multiplexing	page 199
0x1804006C	GPIO_FUNCTION	Controls JTAG, External MDIO in GPIO	page 199

10.5.1 GPIO Output Enable (GPIO_OE)

Address: 0x18040000
Access: Read/Write
Reset: 0xFFFF0B

General Purpose I/O output enable.

Bit	Bit Name	Description
31:0	OE	Per bit output enable.

10.5.2 GPIO Input Value (GPIO_IN)

Address: 0x18040004
Access: Read-Only
Reset: 0x0

General Purpose I/O input value register.

Bit	Bit Name	Description
31:0	IN	Current values of each of the GPIO pins

10.5.3 GPIO Output Value (GPIO_OUT)

Address: 0x18040008
Access: Read-Only
Reset: 0x0

General Purpose I/O output value register.

Bit	Bit Name	Description
31:0	OUT	Driver output value. If the corresponding bit in the GPIO Output Enable (GPIO_OE) register is set to 0, the GPIO pin will drive the value in the corresponding bit of this register.

10.5.4 GPIO Per Bit Set (GPIO_SET)

Address: 0x1804000C
Access: Write-Only
Reset: 0x0

General Purpose I/O per bit set register.

Bit	Bit Name	Description
31:0	SET	On a write, any bit that is set causes the corresponding GPIO bit to be set. Any bit that is not set will have no effect.

10.5.5 GPIO Per Bit Clear (GPIO_CLEAR)

Address: 0x18040010
Access: Write-Only
Reset: 0x0

General Purpose I/O per bit clear register.

Bit	Bit Name	Description
31:23	CLEAR	On a write, any bit that is set causes the corresponding GPIO bit to be cleared. Any bit that is not set will have no effect.

10.5.6 GPIO Interrupt Enable (GPIO_INT)

Address: 0x18040014
Access: Read/Write
Reset: 0x0

General Purpose I/O interrupt enable register.

Bit	Bit Name	Description
31:0	INT	Each bit that is set is considered an interrupt ORd into the GPIO interrupt line.

10.5.7 GPIO Interrupt Type (GPIO_INT_TYPE)

Address: 0x18040018
Access: Read/Write
Reset: 0x0

General Purpose I/O interrupt type register.

Bit	Bit Name	Description	
31:0	TYPE	Interrupt type	
		0	Indicates the bit is an edge-sensitive interrupt
		1	Indicates the bit is a level-sensitive interrupt

10.5.8 GPIO Interrupt Polarity (GPIO_INT_POLARITY)

Address: 0x1804001C
Access: Read/Write
Reset: 0x0

General Purpose I/O interrupt polarity register.

Bit	Bit Name	Description	
31:0	POLARITY	Interrupt polarity	
		0	Indicates that the interrupt is active low (level) or falling edge (edge)
		1	Indicates that the interrupt is active high (level) or rising edge (edge)

10.5.9 GPIO Interrupt Pending (GPIO_INT_PENDING)

Address: 0x18040020
Access: Read/Write (See field description)
Reset: 0x0

General Purpose I/O interrupt pending register.

Bit	Bit Name	Description
31:0	PENDING	For each bit, indicates that an interrupt is currently pending for the particular GPIO. For edge-sensitive interrupts, this register is read-with-clear.

10.5.10 GPIO Interrupt Mask (GPIO_INT_MASK)

Address: 0x18040024
Access: Read/Write
Reset: 0x0

General Purpose I/O interrupt mask.

Bit	Bit Name	Description
31:0	MASK	For each bit that is set, the corresponding interrupt in the register GPIO Interrupt Pending (GPIO_INT_PENDING) is passed on to the central interrupt controller.

10.5.11 GPIO Spare Bits (GPIO_SPARE)

Address: 0x18040028
Access: Read-Only
Reset: 0x0

Spare register bits

Bit	Bit Name	Description
31:0	BITS	Spare register bits

10.5.12 GPIO Function 0 (GPIO_OUT_FUNCTION0)

Address: 0x1804002C
Access: Read/Write
Reset: 0x0

Represents 4 GPIO registers (0, 1, 2, 3), 8 bits each. Each signal to be output through the GPIO pin has a select value. The select value of the signal is programmed in the particular GPIO field through which it is output. (Refer to GPIO_OUTPUT_SELECT_VALUES)

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_3	GPIO3	Reserved	Selected programmed value is available in GPIO3
23:16	ENABLE_GPIO_2	GPIO2	Reserved	Selected programmed value is available in GPIO2
15:8	ENABLE_GPIO_1	GPIO1	Reserved	Selected programmed value is available in GPIO1
7:0	ENABLE_GPIO_0	GPIO0	Reserved	Selected programmed value is available in GPIO0

10.5.13 GPIO Function 1 (GPIO_OUT_FUNCTION1)

Address: 0x18040030
Access: Read/Write
Reset: 0x0

Represents 4 GPIO registers (4, 5, 6, 7), 8 bits each. Each signal to be output through the GPIO pin has a select value. The select value of the signal is programmed in the particular GPIO field through which it is output. (Refer to GPIO_OUTPUT_SELECT_VALUES)

Bit	Bit Name	GPIO	Reset	Default Function	Description
31:24	ENABLE_GPIO_7	GPIO7	0xC	SPI_MOSI	Selected programmed value is available in GPIO7
23:16	ENABLE_GPIO_6	GPIO6	0x8	SPI_CLK	Selected programmed value is available in GPIO6
15:8	ENABLE_GPIO_5	GPIO5	0x9	SPI_CS0	Selected programmed value is available in GPIO5
7:0	ENABLE_GPIO_4	GPIO4	0x54	CLK_OBS5[1]	Selected programmed value is available in GPIO4

1. See GPIO Function (GPIO_FUNCTION) for clock signals that can be observed through GPIO pins.

10.5.14 GPIO Function 2 (GPIO_OUT_FUNCTION2)

Address: 0x18040034
Access: Read/Write
Reset: 0x0

Represents 4 GPIO registers (8, 9, 10, 11), 8 bits each. Each signal to be output through the GPIO pin has a select value. The select value of the signal is programmed in the particular GPIO field through which it is output. (Refer to GPIO_OUTPUT_SELECT_VALUES)

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_11	GPIO11	Reserved	Selected programmed value is available in GPIO11
23:16	ENABLE_GPIO_10	GPIO10	Reserved	Selected programmed value is available in GPIO10
15:8	ENABLE_GPIO_9	GPIO9	Reserved	Selected programmed value is available in GPIO9
7:0	ENABLE_GPIO_8	GPIO8	Reserved	Selected programmed value is available in GPIO8

10.5.15 GPIO Function 3 (GPIO_OUT_FUNCTION3)

Address: 0x18040038
Access: Read/Write
Reset: 0x0

Represents 4 GPIO registers (12, 13, 14, 15), 8 bits each. Each signal to be output through the GPIO pin has a select value. The select value of the signal is programmed in the particular GPIO field through which it is output. (Refer to GPIO_OUTPUT_SELECT_VALUES)

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_15	GPIO15	Reserved	Selected programmed value is available in GPIO15
23:16	ENABLE_GPIO_14	GPIO14	Reserved	Selected programmed value is available in GPIO14
15:8	ENABLE_GPIO_13	GPIO13	Reserved	Selected programmed value is available in GPIO13
7:0	ENABLE_GPIO_12	GPIO12	Reserved	Selected programmed value is available in GPIO12

10.5.16 GPIO Function 4 (GPIO_OUT_FUNCTION4)

Address: 0x1804003C
Access: Read/Write
Reset: 0x0

Represents 4 GPIO registers (16, 17, 18, 19), 8 bits each. Each signal to be output through the GPIO pin has a select value. The select value of the signal is programmed in the particular GPIO field through which it is output. (Refer to GPIO_OUTPUT_SELECT_VALUES).

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_19	GPIO19	Reserved	Selected programmed value is available in GPIO19
23:16	ENABLE_GPIO_18	GPIO18	Reserved	Selected programmed value is available in GPIO18
15:8	ENABLE_GPIO_17	GPIO17	Reserved	Selected programmed value is available in GPIO17
7:0	ENABLE_GPIO_16	GPIO16	Reserved	Selected programmed value is available in GPIO16

10.5.17 GPIO Function 5 (GPIO_OUT_FUNCTION5)

Address: 0x18040040
Access: Read/Write
Reset: 0x0

Represents 4 GPIO registers (20, 21, 22, 23), 8 bits each. Each signal to be output through the GPIO pin has a select value. The select value of the signal is programmed in the particular GPIO field through which it is output. (Refer to GPIO_OUTPUT_SELECT_VALUES)

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_23	GPIO23	Reserved	Selected programmed value is available in GPIO23
23:16	ENABLE_GPIO_22	GPIO22	Reserved	Selected programmed value is available in GPIO22
15:8	ENABLE_GPIO_21	GPIO21	Reserved	Selected programmed value is available in GPIO21
7:0	ENABLE_GPIO_20	GPIO20	Reserved	Selected programmed value is available in GPIO20

The GPIO_IN_ENABLE[9:0] registers, along with the GPIO Output Enable (GPIO_OE) register, drive internal logic. The registers indicate through which GPIO pins the particular input signal is available. Program the GPIO pin number through which these signals are input.

See Table 3-18. Apart from JTAG, all signals listed in Table 3-18 can use any GPIO. GPIO[3:0] can be used by setting the DISABLE_JTAG bit to 1 in the GPIO Function (GPIO_FUNCTION) register.

10.5.18 GPIO In Signals 0 (GPIO_IN_ENABLE0)

Address: 0x18040044
Access: Read/Write
Reset: See field description

Program the GPIO pin number through which these signals are input.

Bit	Bit Name	Reset	Description
31:16	RES	0x0	Reserved
15:8	UART_SIN	0x0	Programmed value indicates the GPIO that inputs UART_SIN
7:0	SPI_DATA_IN	0x8	Programmed value indicates the GPIO pin that inputs SPI_MISO

10.5.19 GPIO In Signals 1 (GPIO_IN_ENABLE1)

Address: 0x18040048
Access: Read/Write
Reset: 0x0

Program the GPIO pin number through which these signals are input.

Bit	Bit Name	Signal	Description
31:24	I2SEXT_MCLK	I2S_MCLK	Programmed value indicates the GPIO pin that inputs I2S_MCLK
23:16	I2SEXTCLK	I2S_CLK	Programmed value indicates the GPIO pin that inputs I2S_CLK
15:8	I2S0_MIC_SD	I2S_SD	Programmed value indicates the GPIO pin that inputs I2S_MIC_SD
7:0	I2S0_WS	I2S_WS	Programmed value indicates the GPIO pin that inputs I2S_WS

10.5.20 GPIO In Signals 2 (GPIO_IN_ENABLE2)

Address: 0x1804004C
Access: Read/Write
Reset: 0x0

Program the GPIO pin number through which these signals are input.

Bit	Bit Name	Signal	Description
31:24	SLICEXT_MCLK	SLICEXT_MCLK	Reserved
23:16	ETH_RX_CRS	ETH_RX_CRS	Programmed value indicates the GPIO pin that inputs ETH_RX_CRS
15:8	ETH_RX_COL	ETH_RX_COL	Programmed value indicates the GPIO pin that inputs ETH_RX_COL
7:0	ETH_RX_ERR	ETH_RX_ERR	Programmed value indicates the GPIO pin that inputs ETH_RX_ERR

10.5.21 GPIO In Signals 3 (GPIO_IN_ENABLE3)

Address: 0x18040050
Access: Read/Write
Reset: 0x0

Program the GPIO pin number through which these signals are input.

Bit	Bit Name	Signal	Description
31:24	RES	—	Reserved
23:16	MII_GE1_MDI	MII_GE1_MDI	Programmed value indicates the GPIO pin through which the boot MII_GE1_MDI signal is input (MDIO slave for boot up)
15:8	BOOT_EXT_MDC	BOOT_EXT_MDC	Programmed value indicates the GPIO pin through which the boot MDIO MDC signal is input (MDIO slave for boot up)
7:0	BOOT_EXT_MDO	BOOT_EXT_MDO	Programmed value indicates the GPIO pin through which the boot MDIO MDO signal is input (MDIO slave for boot up)

10.5.22 GPIO In Signals 4 (GPIO_IN_ENABLE4)

Address: 0x18040054
Access: Read/Write
Reset: 0x0

Program the GPIO pin number through which these signals are input.

Bit	Bit Name	Signal	Description
31:24	I2C_DATA	I2C_DATA	Programmed value indicates the GPIO pin through which I2C_DATA is input
23:16	I2C_CLK	I2C_CLK	Programmed value indicates the GPIO pin through which I2C_CLK is input
15:8	SLIC_PCM_ FS_IN	SLIC_PCM_FS	Programmed value indicates the GPIO pin through which SLIC_PCM_FS is input. Note that the frame sync signal can be used as input or output
7:0	SLIC_DATA_IN	SLIC_DATA_IN	Programmed value indicates the GPIO pin through which SLIC_DATA_IN is input

10.5.23 GPIO In Signals 9 (GPIO_IN_ENABLE9)

Address: 0x18040068
Access: Read/Write
Reset: 0x0

Program the GPIO pin number through which these signals are input.

Bit	Bit Name	Signal	Description
31:24	UART1_CTS	UART1_CTS	Programmed value indicates the GPIO pin that inputs the UART 1 CTS signal
23:16	UART1_RD	UART1_RD	Programmed value indicates the GPIO pin that inputs the UART 1 RD signal
15:8	UART1_RTS	UART1_RTS	Programmed value indicates the GPIO pin that inputs the UART 1 RTS signal
7:0	UART1_TD	UART1_TD	Programmed value indicates the GPIO pin that inputs the UART 1 TD signal

10.5.24 GPIO Function (GPIO_FUNCTION)

Address: 0x1804006C
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:10	RES	0x0	Reserved
9	CLK_OBS7_ENABLE	0x0	Enables observation of audio PLL_CLK
8	CLK_OBS6_ENABLE	0x0	Enables observation of USB_CLK for the first USB instance
7	CLK_OBS5_ENABLE	0x0	Enables observation of CPU_CLK/4
6	CLK_OBS4_ENABLE	0x1	Enables observation of AHB_CLK/2
5	CLK_OBS3_ENABLE	0x0	Enables observation of GE1_TX_CLK
4	CLK_OBS2_ENABLE	0x0	Enables observation of PCIE_EP_CLK
3	CLK_OBS1_ENABLE	0x0	Enables observation of PCIE_RC_CLK
2	RES	0x0	Reserved

1	DISABLE_JTAG	0x0	Disables JTAG port functionality to enable GPIO functionality
0	RES	0x0	Reserved

10.6 PLL Control Registers

Table 10-7 summarizes the QCA9558 PLL control registers.

Table 10-7 PLL Control Registers Summary

Address	Name	Description	Page
0x18050000	CPU_PLL_CONFIG	CPU PLL Configuration	page 202
0x18050004	DDR_PLL_CONFIG	DDR PLL Configuration	page 202
0x18050008	CPU_DDR_CLOCK_CONTROL	CPU DDR Clock Control	page 203
0x1805000C	PCIE_PLL_CONFIG	PCIE RC PLL Configuration	page 204
0x18050010	PCIE_PLL_DITHER_DIV_MAX	PCIE Clock Jitter Max Value Control	page 204
0x18050014	PCIE_PLL_DITHER_DIV_MIN	PCIE Clock Jitter Min Value Control	page 205
0x18050018	PCIE_PLL_DITHER_STEP	PCIE Clock Jitter Step Control	page 205
0x1805001C	LDO_POWER_CONTROL	LDO Power Control	page 205
0x18050020	SWITCH_CLOCK_SPARE	Switch Clock Source Control	page 206
0x18050024	CURRENT_PCIE_PLL_DITHER	Current Dither Logic Output	page 206
0x18050028	ETH_XMII_CONTROL	Ethernet XMII Control	page 207
0x1805002C	AUDIO_PLL_CONFIG	Audio PLL Configuration	page 208
0x18050030	AUDIO_PLL_MODULATION	Audio PLL Modulation Control	page 208
0x18050034	AUDIO_PLL_MOD_STEP	Audio PLL Jitter Control	page 209
0x18050038	CURRENT_AUDIO_PLL_ MODULATION	Current Audio Modulation Output	page 209
0x18050040	DDR_PLL_DITHER	DDR PLL Dither Parameter	page 209
0x18050044	CPU_PLL_DITHER	CPU PLL Dither Parameter	page 210
0x18050048	ETH_SGMII	Ethernet SGMII Control	page 210
0x1805004C	ETH_SGMII_SERDES	SGMII Configuration	page 211
0x18050050	SLIC_PWM_DIV	SLIC PWM Divisor Configuration	page 211

10.6.1 CPU Phase Lock Loop Configuration (CPU_PLL_CONFIG)

Address: 0x18050000
Access: Read/Write
Reset: See field description

This register configures the CPU PLL. $\text{PLL Frequency} = \frac{\text{REFCLK FREQ}}{\text{REFDIV}} \times \left(\frac{\text{NFRAC}}{2^6} + \text{NINT}\right) \times \frac{1}{2^{\text{OUTDIV}}}$

Bit	Bit Name	Type	Reset	Description	
31	UPDATING	RO	0x1	The poll for this bit to become zero to ensure PLL has settled.	
30	PLLPWD	RW	0x1	Write zero to this bit to power up the PLL.	
29:22	RES	RW	0x0	Reserved	
21:19	OUTDIV	RW	0x0	Define the ratio between VCO output and PLL output. OUTDIV > 4 is unsupported.	
18:17	RANGE	RW	0x3	Determines the VCO PLL frequency range of the CPU PLL:	
				0/2	Reflects a PLL frequency range of (580-880) MHz/$2^{(OUTDIV)}$
				1/3	Reflects a PLL frequency range of (400-750) MHz/$2^{(OUTDIV)}$
16:12	REFDIV	RW	0x20	Reference clock divider	
11:6	NINT	RW	0x0	The integer part of the DIV to CPU PLL	
5:0	NFRAC	RO	0x0	Reflects the current NFRAC. Use “CPU PLL Dither Parameter (CPU_PLL_DITHER)” on page 210 to set.	

10.6.2 DDR PLL Configuration (DDR_PLL_CONFIG)

Address: 0x18050004
Access: Read / Write
Reset: See field description

This register is used to configure the DDR PLL. $\text{PLL Frequency} = \frac{\text{REFCLK FREQ}}{\text{REFDIV}} \times \left(\frac{\text{NFRAC}}{2^{10}} + \text{NINT}\right) \times \frac{1}{2^{\text{OUTDIV}}}$

Bit	Bit Name	Type	Reset	Description	
31	UPDATING	RO	0x1	The poll for this bit to become zero to ensure PLL has settled.	
30	PLLPWD	RW	0x1	Write zero to this bit to power up the PLL.	
29:26	RES	RW	0x0	Reserved	
25:23	OUTDIV	RW	0x0	Define the ratio between VCO output and PLL output. OUTDIV > 4 is unsupported.	
22:21	RANGE	RW	0x3	Determines the VCO PLL frequency range of the DDR PLL:	
				0/2	Reflects a PLL frequency range of (580-880) MHz/$2^{(OUTDIV)}$
				1/3	Reflects a PLL frequency range of(400-750) MHz/$2^{(OUTDIV)}$
20:16	REFDIV	RW	0x2	Reference clock divider	
15:10	NINT	RW	0x0	The integer part of the DIV to DDR PLL	
9:0	NFRAC	RO	0x0	Reflects the current NFRAC. Use “DDR PLL Dither Parameter (DDR_PLL_DITHER)” on page 209 to set.	

10.6.3 CPU DDR Clock Control (CPU_DDR_CLOCK_CONTROL)

Address: 0x18050008
Access: Read / Write
Reset: See field description

This register is used to set the CPU and DDR clocks. Any field in this register can be dynamically modified.

Bit	Bit Name	Type	Reset	Description	
31:25	RES	RW	0x0	Reserved	
24	AHBCLK_FROM_ DDRPLL	RW	0x1	AHB_CLK setting	
				0	AHB_CLK is derived from the CPU_PLL
				1	AHB_CLK is derived from the DDR_PLL
23	CPU_RESET_EN_ BP_DEASRT	RW	0x0	Enables reset to the CPU when the CPU_PLL bypass bit is reset	
22	CPU_RESET_EN_ BP_ASRT	RW	0x0	Enables reset to the CPU when the CPU_PLL bypass bit is set	
21	DDRCLK_FROM_ DDRPLL	RW	0x1	DDR_CLK setting. The DDR clock should be a 50% duty cycle clock	
				0	DDR_CLK is derived from the CPU_PLL
				1	DDR_CLK is derived from the DDR_PLL
20	CPUCLK_FROM_ CPUPLL	RW	0x1	CPU_CLK setting. Division of the AHB clock is:	
				0	CPU_CLK is derived from the DDR_PLL
				1	CPU_CLK is derived from the CPU_PLL
19:15	AHB_POST_DIV	RW	0x0	Division of the AHB clock: <AHB frequency> = <PLL or REFCLK frequency> / (AHB_POST_DIV+1)	
14:10	DDR_POST_DIV	RW	0x0	Division of the DDR PLL clock: <DDR frequency> = <PLL frequency> / (DDR_POST_DIV+1) or <REFCLK frequency>	
9:5	CPU_POST_DIV	RW	0x0	Division of the CPU PLL clock: <CPU frequency> = <PLL frequency> / (CPU_POST_DIV+1) or <REFCLK frequency>	
4	AHB_PLL_ BYPASS	RW	0x1	Enables bypassing of the AHB PLL path	
3	DDR_PLL_ BYPASS	RW	0x1	Enables bypassing of the DDR PLL	
2	CPU_PLL_ BYPASS	RW	0x1	Enables bypassing of the CPU PLL	
1	RESET_SWITCH	RW	0x0	Reset during clock switch trigger	
0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	

10.6.4 PCIE RC PLL Configuration (PCIE_PLL_CONFIG)

Address: 0x1805000C
Access: Read / Write
Reset: See field description

Configure the PCIE RC PLL. $$\text{PLL Frequency} = \frac{\text{REFCLK FREQ}}{\text{REFDIV}} \times \left(\frac{\text{DIV FRAC}}{2^{14}} + \text{DIV INT}\right) \times \frac{1}{8}$$

The frequency range is (580-880 MHz)/8. Use the PCIE Clock Jitter Max Value Control (PCIE_PLL_DITHER_DIV_MAX)/PCIE Clock Jitter Min Value Control (PCIE_PLL_DITHER_DIV_MIN) registers to set the DIV_INT and DIV_FRAC.

Bit	Bit Name	Type	Reset	Description
31	UPDATING	RO	0x0	The poll for this bit is to become zero to ensure PLL has settled.
30	PLLPWD	RW	0x1	Power up control for the PLL, write zero to this bit to power up the PLL
29:17	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
16	BYPASS	RW	0x1	Enables bypassing of the PCIE PLL
15	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
14:10	REFDIV	RW	0x1	Reference clock divider
9:0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

10.6.5 PCIE Clock Jitter Max Value Control (PCIE_PLL_DITHER_DIV_MAX)

Address: 0x18050010
Access: Read / Write
Reset: See field description

This register is for the PCIE clock jitter control. The maximum value controls the jitter behavior of the PCIE PLL.

Bit	Bit Name	Type	Reset	Description
31	EN_DITHER	RW	0x1	Enables dither logic
30	USE_MAX	RW	0x1	When the Dither logic is disabled, this maximum value is used
29:21	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
20:15	DIV_MAX_INT	RW	0x0	The maximum limit of the integer part of the divider
14:1	DIV_MAX_FRAC	RW	0x3FFF	The maximum limit of the fractional part of the divider
0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

10.6.6 PCIE Clock Jitter Min Value Control (PCIE_PLL_DITHER_DIV_MIN)

Address: 0x18050014
Access: Read / Write
Reset: See field description

This register is for the PCIE clock jitter control. The minimum value controls the jitter behavior of the PCIE PLL.

Bit	Bit Name	Type	Reset	Description
31:21	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
20:15	DIV_MIN_INT	RW	0x0	The minimum limit of the integer part of the divider
14:1	DIV_MIN_FRAC	RW	0x3FFF	The minimum limit of the fractional part of the divider
0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

10.6.7 PCIE Clock Jitter Step Control (PCIE_PLL_DITHER_STEP)

Address: 0x18050018
Access: Read / Write
Reset: See field description

This register controls the jitter behavior of the PCIE PLL.

Bit	Bit Name	Type	Reset	Description
31:28	UPDATE_CNT	RW	0x0	Sets the frequency of updates. 0 = every clock.
27:25	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
24:15	STEP_INT	RW	0x0	The integer part of the step value of the divider, which should be 0. The integer part cannot be changed during configuration.
14:1	STEP_FRAC	RW	0x0	Fractional Part of the step divider
0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

10.6.8 LDO Power Control (LDO_POWER_CONTROL)

Address: 0x1805001C
Access: Read / Write
Reset: See field description

This register controls and reflects the analog LDO control bits that control the LDO.

Bit	Bit Name	Type	Reset	Description
31:5	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
4	PWDLDO_CPU	RW	0x0	1.2 V signal to power down the DDR regulator
3	PWDLDO_DDR	RW	0x0	1.2 V signal to power down the DDR regulator
2:1	CPU_REFSEL	RW	0x3	Select the CPU regulator output voltage
0	SELECT_DDR1	RW	0x0	Reflects the input in the PC_DDR_SEL pin

10.6.9 Switch Clock Source Control (SWITCH_CLOCK_SPARE)

Address: 0x18050020
Access: Read / Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31:16	RES	RW	0x0	Reserved
15	MDIO_CLK_ SEL1_2	RW	0x0	MDIO master operational clock selection for GMAC1; used with MDIO_ CLK_SEL1_1
			0	REF clock, or 100 MHz clock
			1	50 MHz clock
14	MDIO_CLK_ SEL1_1	RW	0x0	MDIO master operational clock selection for GMAC1; used with MDIO_ CLK_SEL1_2
			0	REF clock, or 100 MHz clock
			1	50 MHz clock
13	MDIO_CLK_ SEL0_2	RW	0x0	MDIO master operational clock selection for GMAC1; used with MDIO_ CLK_SEL0_1
			0	REF clock, or 100 MHz clock
			1	50 MHz clock
12	NANDF_CLK_SEL	RW	0x0	NAND FLASH operational clock selection
			0	REF clock, or 100 MHz clock
			1	50 MHz clock
11:8	USB_REFCLK _FREQ_SEL	RW	0x5	Used to select the REFCLK input of 40 MHz to the USB PLL
7	UART1_CLK_SEL	RW	0x0	Select the clock for UART1 operation
			0	REFCLK
			1	100 MHZ clock
6	MDIO_CLK_ SEL0_1	RW	0x0	MDIO master operational clock selection for GMAC0; used with MDIO_ CLK_SEL0_2
			0	REFCLK
			1	100 MHZ clock
5	I2C_CLK_SEL	RW	0x0	Select the clock for I^2C core clock operation
			0	REFCLK
			1	100 MHZ clock
4:0	SPARE	RW	0x0	Spare CPU configuration bits

10.6.10 Current Dither Logic Output (CURRENT_PCIE_PLL_DITHER)

Address: 0x18050024
Access: Read / Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31:21	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
20:15	INT	RW	0x0	The integer part of the divider
14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	FRAC	RW	0x3FFF	The fractional part of the divider

10.6.11 Ethernet XMII Control (ETH_XMII_CONTROL)

Address: 0x18050028
Access: Read/Write
Reset: See field description

Controls the Tx and Rx clocks for the (MII/GMII/RGMII) master mode of the GMAC. This register should only be changed when GE0 is in reset.

Bit	Bit Name	Type	Reset	Description
31	TX_INVERT	RW	0x0	Decides whether to select the inversion of the GTX clock after the delay line
30	GIGE_QUAD	RW	0x0	Decides whether to allow a 2 ns shift (clock in the middle of a data transfer) to the GTX clock. This bit is only effective when bit [25] is set.
29:28	RX_DELAY	RW	0x0	The delay buffers in the Rx clock path to adjust against the edge/middle-aligned RGMII inputs
27:26	TX_DELAY	RW	0x0	Delay line for the GTX clock that goes along with the data
				00 Minimum delay
				11 Maximum delay
25	GIGE	RW	0x0	Set only after a 1000 MBps connection has been negotiated
24	OFFSET _PHASE	RW	0x0	Used to select if the start is from the positive or negative phase (or whether to have a 180 degree change in addition to the phase-delay in [11:8].
23:16	OFFSET_CNT	RW	0x0	Beginning counter value to phase-delay the GTX clock
15:8	PHASE1_CNT	RW	0x1	Number of 100 clock cycles in the negative cycle of the XMII Tx/Rx clock
7:0	PHASE0_CNT	RW	0x1	Number of 100 clock cycles in the positive cycle of the XMII Tx/Rx clock

10.6.12 Audio PLL Configuration (AUDIO_PLL_CONFIG)

Address: 0x1805002C
Access: Read / Write
Reset: See field description

This register configures the Audio Phase Look Loop.

$$\text{PLL Frequency} = \frac{\text{REFCLK FREQ}}{\text{REFDIV}} \times \left(\frac{\text{DIV FRAC}}{2^{18}} + \text{DIV INT}\right) \times \frac{1}{2^{\text{POSTPLDIV}}}$$

$$\text{MCLK Frequency} = \frac{\text{PLL Frequency}}{\text{EXT DIV}}$$

The frequency range is (400-750 MHz) / $2^{\text{POSTPLLDIV}}$. Use the "Audio PLL Modulation Control (AUDIO_PLL_MODULATION)" on page 208 to set the DIV_INT and DIV_FRAC.

Bit	Bit Name	Type	Reset	Description
31:15	RES	RO	0x0	Reserved. Contains zeros when read.
14:12	EXT_DIV	RW	0x1	Digital divider to derive the MCLK from the PLL output. Use only even values for 50% of the duty cycle
11:10	RES	RO	0x0	Reserved. Contains zeros when read.
9:7	POSTPLLPWD	RW	0x1	Post power up control for the PLL. POSTPLLPWD > 4 is unsupported.
6	RES	RO	0x0	Reserved. Contains zeros when read.
5	PLLPWD	RW	0x1	Write 0 to this bit to power up the PLL
4	BYPASS	RW	0x1	Enables bypassing of the audio PLL
3:0	REFDIV	RW	0x1	Reference clock divider

10.6.13 Audio PLL Modulation Control (AUDIO_PLL_MODULATION)

Address: 0x18050030
Access: Read / Write
Reset: See field description

This register controls the jitter behavior of the audio PLL.

Bit	Bit Name	Type	Reset	Description
31:29	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
28:11	TGT_DIV_FRAC	RW	0x0	Target value of the DIV fractional part for Audio PLL
10:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:1	TGT_DIV_INT	RW	0x0	Target value of the integer part for Audio PLL
0	START	RW	0x0	Starts the audio modulation. If this bit is not set, then the DIV_INT and DIV_FRAC inputs to the PLL are TGT_DIV_INT and TGT_DIV_FRAC fields of this register. Otherwise, the PLL inputs receive the modulated values.

10.6.14 Audio PLL Jitter Control (AUDIO_PLL_MOD_STEP)

Address: 0x18050034
Access: Read/Write
Reset: See field description

Controls the jitter behavior of the AUDIO PLL.

Bit	Bit Name	Type	Reset	Description
31:14	FRAC	RW	0x1	Fractional part of the divider step value
13:4	INT	RW	0x0	Unused
3:0	UPDATE_ CNT	RW	0x0	Update frequency. 0 denotes an update every clock

10.6.15 Current Audio Modulation Output (CURRENT_AUDIO_PLL_ MODULATION)

Address: 0x18050038
Access: Read-Only
Reset: See field description

Sets the current audio modulation logic output.

Bit	Bit Name	Reset	Description
31:28	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
27:10	FRAC	0x1	The fractional part of the divider
9:7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:1	INT	0x0	Integer part of the divider
0	RES	0x0	Reserved

10.6.16 DDR PLL Dither Parameter (DDR_PLL_DITHER)

Address: 0x18050040
Access: Read/Write
Reset: See field description

Controls the FRAC of the DDR PLL. Should be enabled only if the DDR_CLK is from the DDR PLL.

Bit	Bit Name	Type	Reset	Description
31	DITHER_ EN	RW	0x0	The step value which increments every refresh period
30:27	UPDATE_ COUNT	RW	0x0	The number of refresh periods between two updates
26:20	NFRAC_ STEP	RW	0x0	7-bit LSB step value which increments every refresh period
19:10	NFRAC_ MIN	RW	0x0	The minimum NFRAC value
9:0	NFRAC_ MAX	RW	0x0	The maximum NFRAC value

10.6.17 CPU PLL Dither Parameter (CPU_PLL_DITHER)

Address: 0x18050044
Access: Read/Write
Reset: 0x0

Sets the parameters for the CPU PLL dither.

Bit	Bit Name	Description
31	DITHER_ EN	The step value which increments every refresh period
30:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:18	UPDATE_ COUNT	The number of 512 CPU clocks between two updates in NFRAC
17:12	NFRAC_ STEP	The step value increment
11:6	NFRAC_ MIN	The minimum NFRAC value. If DITHER_EN is set to 0, the min would be used.
5:0	NFRAC_ MAX	The maximum NFRAC value

10.6.18 Ethernet SGMII Control (ETH_SGMII)

Address: 0x18050048
Access: Read/Write
Reset: See field description

Controls the Tx and Rx clocks for the GMAC and SDGMII SERDES digital.

Bit	Bit Name	Type	Reset	Description	
31	TX_INVERT	RW	0x0	Decides whether to select the inversion of the GTX clock after the delay line	
30	GIGE_QUAD	RW	0x0	Decides whether to allow a 2 ns shift (clock in the middle of a data transfer) to the GTX clock. This bit is only effective when bit [25] is set.	
29:28	RX_DELAY	RW	0x0	The delay buffers in the Rx clock path to adjust against the edge/middle-aligned RGMII inputs	
27:26	TX_DELAY	RW	0x0	Delay line for the GTX clock that goes along with the data	
				00	Minimum delay
				11	Maximum delay
25	CLK_SEL GIGE	RW	0x1	Set to select between CLK100 and CLK125 for the SGMII source clock	
				0	CLK100
				1	CLK125
24	GIGE	RW	0x1	Select this bit if the GMAC connected to the SGMII is in GIGE mode	
23:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15:8	PHASE1_CNT	RW	0x1	Number of (CLK100/CLK125 + 1) clock cycles in the negative cycle of the SGMII Tx/Rx clock	
7:0	PHASE0_CNT	RW	0x1	Number of (CLK100/CLK125 + 1) clock cycles in the positive cycle of the SGMII Tx/Rx clock	

10.6.19 SGMII Configuration (ETH_SGMII_SERDES)

Address: 0x1805004C
Access: Read/Write
Reset: See field description

This register configures parameters for the SGMII.

Bit	Bit Name	Type	Reset	Description	
31:3	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
2	EN_LOCK_ DETECT	RW	0x0	SGMII VCO control voltage detector	
				0	Lock detector disabled
				1	Lock detector enabled
1	PLL_REFCLK_ SEL	RW	0x0	Must be set to 1 for 40 MHz PLL reference clock	
0	PLL_EN	RW	0x1	Enables the SGMII PLL	
				0	SGMII PLL disabled
				1	SGMII PLL enabled

10.6.20 SLIC PWM Divisor Configuration (SLIC_PWM_DIV)

Address: 0x18050050
Access: Read/Write
Reset: See field description

This register configures the SLIC PWM settings.

Bit	Bit Name	Type	Reset	Description
31	ENABLE	RW	0x0	Enables the extra divider on the SLIC MCLK for PWM
30	REFCLK	RW	0x0	Chooses the REFCLK for divide instead of the audio PLL clock for SLIC PWM
29:16	SPARE	RO	0x0	Spare register bits
15:8	PHASE1_COUNT	RW	0x1	Number of clock cycles in the negative cycle of the output clock
7:0	PHASE0_COUNT	RW	0x1	Number of clock cycles in the positive cycle of the output clock

10.7 Reset Registers

Table 10-8 summarizes the reset registers for the QCA9558.

Table 10-8 Reset Registers

Address	Name	Description	Page
0x18060000	RST_GENERAL_TIMERx	General Purpose Timers	page 212
0x18060004	RST_GENERAL_TIMERx_RELOAD	General Purpose Timers Reload	page 213
0x18060008	RST_WATCHDOG_TIMER_CONTROL	Watchdog Timer Control	page 213
0x1806000C	RST_WATCHDOG_TIMER	Watchdog Timer	page 214
0x18060010	RST_MISC_INTERUPT_STATUS	Miscellaneous Interrupt Status	page 214
0x18060014	RST_MISC_INTERUPT_MASK	Miscellaneous Interrupt Mask	page 216
0x18060018	RST_GLOBAL_INTERUPT_STATUS	Global Interrupt Status	page 217
0x1806001C	RST_RESET	Reset	page 217
0x18060090	RST_REVISION_ID	Chip Revision ID	page 218
0x18060094	RST_GENERAL_TIMER2	General Purpose Timer 2	page 212
0x18060098	RST_GENERAL_TIMER2_RELOAD	General Purpose Timer2 Reload	page 213
0x1806009C	RST_GENERAL_TIMER3	General Purpose Timer 3	page 212
0x180600A0	RST_GENERAL_TIMER3_RELOAD	General Purpose Timer3 Reload	page 213
0x180600A4	RST_GENERAL_TIMER4	General Purpose Timer 4	page 212
0x180600A8	RST_GENERAL_TIMER4_RELOAD	General Purpose Timer4 Reload	page 213
0x180600AC	RST_PCIE_WMAC_INTERRUPT_ STATUS	PCIE, RC and WMAC Interrupt Status	page 219
0x180600B0	RST_BOOTSTRAP	Reset Bootstrap	page 220
0x180600B8	SPARE_STKY_REG[0:0]	Sticky Register Value	page 220
0x180600BC	RST_MISC2	Miscellaneous CPU Control Bits	page 221
0x180600C4	RST_RESET2	Reset Register 2	page 222
0x180600C8	RST_PCIEEP_INTERRUPT_MASK	PCIE EP Interrupt Mask	page 223
0x180600CC	RST_CLKGAT_EN	AHB Clock Gating	page 223

10.7.1 General Purpose Timers (RST_GENERAL_TIMERx)

Timer1 Address: 0x18060000
Timer2 Address: 0x18060094
Timer3 Address: 0x1806009C
Timer4 Address: 0x180600A4
Access: Read/Write
Reset: 0x0

This timer counts down to zero, sets and interrupt, then reloads from the General Purpose Timers Reload (RST_GENERAL_TIMERx_RELOAD) register. The timer operates with REF_CLK as reference input. This definition holds true for timer1, timer2, timer3, and timer4.

Bit	Bit Name	Description
31:0	TIMER	Timer value

10.7.2 General Purpose Timers Reload (RST_GENERAL_TIMERx_RELOAD)

Timer1 Reload Address: 0x18060004
Timer2 Reload Address: 0x18060098
Timer3 Reload Address: 0x180600A0
Timer4 Reload Address: 0x180600A8
Access: Read/Write
Reset: 0x0

This register contains the value that will be loaded into the General Purpose Timers (RST_GENERAL_TIMERx) register when it decrements to zero. The timer operates with REF_CLK as reference input.

This definition holds true for timer1, timer2, timer3, and timer4.

Bit	Bit Name	Description
31:0	RELOAD_VALUE	Timer reload value

10.7.3 Watchdog Timer Control (RST_WATCHDOG_TIMER_CONTROL)

Address: 0x18060008
Access: See field description
Reset: 0x0

Sets the action to take when the watchdog timer reaches zero. The options are reset, non-maskable interrupt and general purpose interrupt after reaching zero.

The timer operates with REF_CLK as reference input.

Bit	Bit Name	Type	Description	
31	LAST	RO	Indicates if the last reset was due to a watchdog timeout	
30:2	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
1:0	ACTION	RW	The action to be taken after the timer reaches zero	
			00	No action
			01	General purpose interrupt
			10	Non-maskable interrupt
			11	Full chip reset, same as power-on reset

10.7.4 Watchdog Timer (RST_WATCHDOG_TIMER)

Address: 0x1806000C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	TIMER	Counts down to zero and stays at zero until the software sets this timer to another value. The timer operates with REF_CLK as reference input. These bits should be set to a non-zero value before updating the Watchdog Timer Control (RST_WATCHDOG_TIMER_CONTROL) register to a non-zero number.

10.7.5 Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_ STATUS)

Address: 0x18060010
Access: Read/Write-to-Clear
Reset: 0x0

Sets the current state of the interrupt lines that are combined to form the MiscInterupt to the processor. All bits of this register need a write to clear.

Bit	Bit Name	Description
31:22	RES	Reserved. Must be written with zero. Contains zeros when read.
21	NANDF_INTR	This interrupt is generated by the NAND_FLASH module. This bit is cleared after a write of this register.
20	WOW_INTR	This interrupt is generated when the MAC detects a WOW event. This bit is cleared after a write of this register.
19	SLIC_INTR	This interrupt is generated from SLIC for an unexpected frame sync in slave mode. This bit is cleared after a write of this register.
18	DDR_ACTIVITY_ IN_ SF	This interrupt is generated when the memory controller detects a DDR request when in self-refresh.
17	DDR_SF_EXIT	This interrupt is generated by the memory controller upon entering self-refresh
16	DDR_SF_ENTRY	This interrupt is generated by the memory controller upon entering self-refresh
15	CHKSUM_ACC_ INT	This interrupt is generated from the checksum accelerator
14	RES	Reserved
13	LUTS_AGER_INT	This interrupt is generated from the ETH_LUT_TOP. This bit is cleared after a write of this register.
12	SGMII_MAC_INT	Interrupt generated from SGMII. This bit is cleared after a write of this register.
11	RES	Reserved
10	TIMER4_INT	The interrupt corresponding to General Purpose Timer4. This bit is cleared after being read. The timer has been immediately reloaded from the General Purpose Timers Reload (RST_GENERAL_TIMERx_RELOAD) register.

9	TIMER3_INT	The interrupt corresponding to General Purpose Timer3. This bit has been cleared after being read. The timer will be immediately reloaded from the General Purpose Timers Reload (RST_GENERAL_TIMERx_RELOAD) register.
8	TIMER2_INT	The interrupt corresponding to General Purpose Timer2. This bit has been cleared after being read. The timer will be immediately reloaded from the General Purpose Timers Reload (RST_GENERAL_TIMERx_RELOAD) register.
7	MBOX_INT	SLIC/I2S/SPDIF/MBOX controller interrupt. The MBOX controller register must be read to clear this interrupt.
6	UART1_INT	This interrupt is generated by UART1. The UART1 (High-Speed) Registers interrupt registers must be read for this bit to be cleared
5	PC_INT	CPU performance counter interrupt. Generated whenever either of the internal CPU performance counters have bit [31] set. The relevant performance counter must be reset to clear this interrupt.
4	WATCHDOG_ INT	The watchdog timer interrupt. This interrupt is generated when the watchdog timer reaches zero and the Watchdog Timer (RST_WATCHDOG_TIMER) register is configured to generate a general-purpose interrupt.
3	UART0_INT	The UART0 interrupt. UART0 interrupt registers must be read before this interrupt can be cleared.
2	GPIO_INT	The GPIO interrupt. Individual lines must be masked before this interrupt can be cleared.
1	ERROR_INT	The error interrupt.
0	TIMER_INT	Interrupt occurring in correspondence to the general purpose timer0. This bit is cleared after being read. The timer has already been reloaded from the General Purpose Timers Reload (RST_GENERAL_TIMERx_RELOAD) register.

10.7.6 Miscellaneous Interrupt Mask (RST_MISC_INTERRUPT_ MASK)

Address: 0x18060014
Access: Read/Write
Reset: 0x0

Enables or disables a propagation of interrupts in the Miscellaneous Interrupt Status (RST_MISC_ INTERRUPT_STATUS) register.

Bit	Bit Name	Description
31:22	RES	Reserved. Must be written with zero. Contains zeros when read.
21	NANDF_INTR_MASK	Enables the NANDF interrupt
20	WOW_INTR_MASK	Enable the WOW interrupt
19	SLIC_INTR_MASK	Enables the SLIC interrupt
18	DDR_ACTIVITY_IN_SF_ MASK	Enables the interrupt generated when the memory controller detects a DDR request when in self-refresh
17	DDR_SF_EXIT_MASK	Enables the interrupt generated when the memory controller enters self-refresh
16	DDR_SF_ENTRY_MASK	Enables the interrupt generated when the memory controller enters self-refresh
15	CHKSUM_ACC_MASK	Enables the checksum interrupt
14	RES	Reserved
13	LUTS_AGER_INT_MASK	Enables the LUT ager interrupt
12	SGMII_MAC_INT_MASK	Enables the SGMII interrupt if set to 1
11	DDR_PERF_MASK	Enables the DDR performance hit interrupt
10	TIMER4_MASK	When set, enables Timer3 interrupt
9	TIMER3_MASK	When set, enables Timer2 interrupt
8	TIMER2_MASK	When set, enables Timer1 interrupt
7	MBOX_MASK	When set, enables MBOX interrupt
6	UART1_MASK	When set, enables the UART1 interrupt
5	PC_MASK	When set, enables CPU performance counter interrupt
4	WATCHDOG_ MASK	When set, enables watchdog interrupt
3	UART0_MASK	When set, enables the UART0 interrupt
2	GPIO_MASK	When set, enables GPIO interrupt
1	ERROR_MASK	When set, enables the error interrupt
0	TIMER_MASK	When set, enables timer interrupt

10.7.7 Global Interrupt Status (RST_GLOBAL_INTERRUPT_STATUS)

Address: 0x18060018
Access: Read-Only
Reset: 0x0

This register indicates the cause of an interrupt to the CPU from various sources.

Bit	Bit Name	Description
31:10	RES	Reserved. Must be written with zero. Contains zeros when read.
9	WMAC_INT	WMAC interrupt
8	PCIE_RC2_INT	Interrupt from second PCIE RC
7	USB2_INT	USB2 interrupt. Information available in the USB register space.
6	PCIE_ HSTDMA_INT	PCIE EP/Host DMA interrupt
5	TIMER_INT	Internal count/compare timer interrupt
4	MISC_INT	Miscellaneous interrupt; source of the interrupt available on the Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS) register
3	GMAC1_INT	Ethernet1 interrupt; information available in the Ethernet1 register space
2	GMAC0_INT	Ethernet0 interrupt; information available in the Ethernet0 register space
1	USB_INT	USB interrupt
0	PCIE_WMAC_INT	PCIE RC/WMAC interrupt

10.7.8 Reset (RST_RESET)

Address: 0x1806001C
Access: See field description
Reset: See field description

This register individually controls the reset to each of the chip's submodules.

Bit	Bit Name	Reset	Type	Description
31	HOST_RESET	0x0	RO	The host DMA reset status
30	SLIC_REST	0x0	RW	The SLIC reset
29	HDMA_RESET	0x1	RW	The host DMA reset
28	EXTERNAL_RESET	0x0	RW	Commands an external reset (SYS_RST_L pin) immediately; inverted before being sent to the pin.
27	RTC_RESET	0x1	RW	The RTC reset
26	PCIEEP_RST_INT	0x0	RW	This interrupt is asserted when the PCIE EP is reset by and external host and cleared on a write to this bit
25	CHKSUM_ACC_ RESET	0x0	RW	Used to reset the checksum
24	FULL_CHIP_RESET	0x0	RW	Used to command a full chip reset. This is the software equivalent of pulling the reset pin. The system will reboot with PLL disabled. Always zero when read.
23	RESET_GE1_MDIO	0x1	RW	Resets the Ethernet 1 MDIO
22	RESET_GE0_MDIO	0x1	RW	Resets the Ethernet 0 MDIO
21	CPU_NMI	0x0	RW	Used to send an NMI to the CPU. Always zero when read. The watchdog timer can also be used to generate NMI/full chip reset.

20	CPU_COLD_RESET	0x0	RW	Used to cold reset the entire CPU. This bit will be cleared automatically immediately after the reset. Always zero when read.
19	HOST_RESET_INT	0x0	RW	Host DMA reset interrupt. Cleared after a write to this bit
18	PCIEEP_RESET	0x0	RO	PCIE endpoint reset status
17	UART1_RESET	0x0	RW	Resets the HS UART
16	DDR_RESET	0x0	RW	Resets the DDR controller. Self-cleared to 0 by hardware
15	USB_PHY_PLL_PWD_EXT	0x0	RW	Used to power down the USB PHY PLL
14	NANDF_RESET	0x1	RW	Resets the NANDF controller
13	GE1_MAC_RESET	0x1	RW	Used to reset the GMAC1 MAC
12	ETH_SGMII_ ARESET	0x1	RW	Resets the SGMII analog and PLL
11	USB_PHY_ARESET	0x1	RW	Resets the USB PHY's analog
10	HOST_DMA_INT	0x0	RO	Host DMA interrupt occurred
9	GE0_MAC_RESET	0x1	RW	Used to reset the GMAC0 MAC
8	ETH_SGMII_ RESET	0x1	RW	Resets the SGMII SERDES
7	PCIE_PHY_RESET	0x1	RW	Used to reset the PCIE PHY
6	PCIE_RESET	0x1	RW	Used to reset the PCIE host controller; this bit will reset the Endpoint as well
5	USB_HOST_RESET	0x1	RW	Used to reset the USB Host Controller
4	USB_PHY_RESET	0x1	RW	Used to reset the USB PHYs
3	USB_PHY_SUSPEND_OVERRIDE	0x0	RW	Used to set the USB suspend state
				0 Used to put the USB PHY in suspend state
				1 Delegates the Core to control the USB PHY suspend state
2	LUT_RESET	0x0	RW	Resets the lookup engine in the GMAC
1	MBOX_RESET	0x0	RW	Resets the MBOX controller
0	I2S_RESET	0x0	RW	Resets the I^2S controller

10.7.9 Chip Revision ID (RST_REVISION_ID)

Address: 0x18060090
Access: Read-Only
Reset: See field description

This register is the revision ID for the chip.

Bit	Bit Name	Reset	Description
31:0	VALUE	0x0130	Revision ID value

10.7.10 Interrupt Status (RST_EXT_INTERRUPT_STATUS)

Address: 0x180600AC
Access: Read-Only
Reset: 0x0

This register is used to read the interrupt statuses for all interrupts.

Bit	Bit Name	Description
31:29	RES	Reserved. Must be written with zero. Contains zeros when read.
28	USB2_INT	USB2 interrupt. See Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS).
27:25	RES	Reserved. Must be written with zero. Contains zeros when read.
24	USB1_INT	USB1 interrupt. See Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS).
23:22	RES	Reserved. Must be written with zero. Contains zeros when read.
21	PCIE_HOSTIF_INT	PCIE host interface interrupt
20	PCIE_HSTDMA_INT	PCIE host DMA interrupt
19:17	RES	Reserved. Must be written with zero. Contains zeros when read.
16	PCIE_RC2_INT3	PCIE R2 multi-MSI interrupt (Vector 3)/INTA interrupt status
15	PCIE_RC2_INT2	PCIE R2 multi-MSI interrupt (Vector 2)/INTA interrupt status
14	PCIE_RC2_INT1	PCIE R2 multi-MSI interrupt (Vector 1)/INTA interrupt status
13	PCIE_RC2_INT0	PCIE R2 multi-MSI interrupt (Vector 0)/INTA interrupt status
12	PCIE_RC2_INT	Master PCIE R2 interrupt
11:9	RES	Reserved. Must be written with zero. Contains zeros when read.
8	PCIE_RC_INT3	PCIE RC Multi-MSI interrupt (vector 3)/INTA interrupt status
7	PCIE_RC_INT2	PCIE RC Multi-MSI interrupt (vector 2)/INTB interrupt status
6	PCIE_RC_INT1	PCIE RC Multi-MSI interrupt (vector 1)/INTC interrupt status
5	PCIE_RC_INT0	PCIE RC Multi-MSI interrupt (vector 0)/INTD interrupt status
4	PCIE_RC_INT	Master PCIE RC interrupt
3	WMAC_RXHP_INT	Interrupt corresponding to the WMAC high priority receive queue
2	WMAC_RXLP_INT	Interrupt corresponding to the WMAC low priority receive queue
1	WMAC_TX_INT	Interrupt corresponding to the WMAC transmission
0	WMAC_MISC_INT	Interrupt corresponding to the WMAC

10.7.11 Reset Bootstrap (RST_BOOTSTRAP)

Address: 0x180600B0
Access: Read-Only
Reset: See field descriptions

This register contains the bootstrap values latched during reset.

Bit	Bit Name	Reset	Description	
31:18	RES	0x0	Reserved	
17:16	BOOT_INTF_SEL	0x0	Selects the boot interface. This bit is only valid if bit one of this register is set to 0	
			0	USB
			01	PCIE
			10	MII
			11	NAND Flash
15:13	RES	0x1	Reserved; Should be set to high	
12	SW_OPTION2	0x0	Software option 2	
11	SW_OPTION1	0x0	Software option 1	
10:8	RES	0x1	Reserved	
7	USB_MODE	0x0	0	Selects USB HOST (Default)
			1	Selects USB DEVICE
6	PCIE_RC_EP_ SELECT	0x0	0	Selects PCIE EP (Default)
			1	Selects PCIE RC
5	JTAG_MODE	0x0	0	Selects JTAG mode (Default)
			1	Selects EJTAG mode
4	REF_CLK	0x0	0	Reserved; must be tied to 1 for 40 MHz REF_CLK operation
			1	Selects REF_CLK 40 MHz
3	DDR_WIDTH	0x0	0	Selects DDR_WIDTH 16 (default)
			1	Selects DDR_WIDTH 32
2	BOOT_SELECT	0x0	0	Selects boot from ROM (default)
			1	Selects boot from SPI
1	RES	0x0	Reserved; should be tied to 1	
0	DDR_SELECT	0x1	0	Selects DDR2
			1	Selects DDR1 (default)

10.7.12 Sticky Register Value (SPARE_STKY_REG)

Address: 0x180600B8
Access: Read/Write
Reset: 0x0

This register is a generic register only affected by power-cycling. This register can be used by the CPU to save and restore critical state bits during a suspend/resume event for example.

Bit	Bit Name	Description
31:0	VALUE	Sticky register value. This value is reset only with power on reset (not on any other reset).

10.7.13 Miscellaneous CPU Control Bits (RST_MISC2)

Address: 0x180600BC
Access: Read/Write
Reset: See field description

This register contains the miscellaneous CPU controllable bits.

Bit	Bit Name	Type	Reset	Description
31	RES	RO	0x0	Reserved
30	PCIEEP_LINK_UP	RW	0x0	PCIE EP XMLH link up status
29	PCIEEP_CLKOBS2	RW	0x0	Select different PCIEEP PHY clocks for observation
28	PCIEEP_CLKOBS1	RW	0x0	Select different PCIEEP common PHY clocks for observation
27	JTAG_EJTAG_SW_ CPU	RW	0x0	JTAG, EJTAG switch through CPU control
26	WOW _STATUS	RW	0x0	WoW status from the host interface
25	PCIEEP_L2_EXIT_ INT	RW	0x0	L2 exit interrupt status for PCIE EP
24	PCIEEP_L2_ENTR_ INT	RW	0x0	L2 entry interrupt status for PCIE EP
23	PCIEEP_L1_EXIT_ INT	RW	0x0	L1 exit interrupt status for PCIE EP
22	PCIEEP_L1_ENTR_ INT	RW	0x0	L1 entry interrupt status for PCIE EP
21	PCIEEP_L0S_EXIT_ INT	RW	0x0	L0S exit interrupt status for PCIE EP
20	PCIEEP_L0S_ENTR_ INT	RW	0x0	L0S entry interrupt status for PCIE EP
19	PCIEEP_REGWR_EN	RW	0x1	CPU enable bit which allows programming of PCIE EP core registers through the DBI
18	EXT_HOST_CHIP_RST_EN	RW	0x0	Mode bit to allow an external host to rest the entire chip through propagation of the PCIE_RST_L through to the chip CPU.
17	PCIE_RST_INT	RW	0x0	Asserted interrupt when PCIE EP is reset by an external host. Cleared on write.
16	HOST_RESET_INT	RW	0x0	Host DMA reset interrupt. Cleared on write.
15	CPU_HOST_WA	RW	0x0	Bit for allowing the host WA register to use the values written by the CPU in the PCIE EP Interrupt Mask (RST_PCIEEP_ INTERRUPT_MASK) register
14	PRESTN_RCPHY2	RW	0x1	The bit which controls the PERTSN of the PCIE RC-only PHY
13	PRESTN_RCPHY	RW	0x1	The bit which controls the PERTSN of the PCIE common PHY
12:8	PCIEEP_LTSSM_STATE	RO	0x0	LTSSM state of the PCIE EP
7:5	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
4	PCIEEP_LINK_STATUS	RO	0x0	The status of the PCIE EP link, whether enabled or in reset
3	WOW_DETECT	RW	0x0	Enable WoW detection
2	PCIEEP_RXDET_DONE	RW	0x0	Indicates that the PCIE EP Rx detection was successful
1	PCIEEP_WOW_INT	RW	0x0	PCIEEP WoW interrupt
0	PCIEEP_CFG_DONE	RW	0x0	Enable bit set by the CPU after it programs the PCIE EP vector/ device ID (once external host interface asserts PCIE_RST_L)

10.7.14 Reset Register 2 (RST_RESET2)

Address: 0x180600C4
Access: Read/Write
Reset: See field description

This register is the reset register 2 and individually controls the reset to the submodules of the chip.

Bit	Bit Name	Type	Reset	Description	
31:19	SPARE	RO	0x0	Spare bits	
18	EP_MODE	RW	0x0	Indicates if the EP is present	
				0	RC
				1	EP
17	USB2_EXT_PWR_SEQ	RW	0x1	External power REQ for second USB PHY	
16	USB1_EXT_PWR_SEQ	RW	0x1	External power REQ for USB PHY	
15	USB_PHY2_PLL_PWD_EXT	RW	0x0	Used to power down the second USB PHY PLL	
14:12	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
11	USB_PHY2_ARESET	RW	0x1	Reset the analog of the second USB PHY	
10:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
7	PCIE2_PHY_RESET	RW	0x1	Reset the second PCIE PHY	
6	PCIE2_RESET	RW	0x1	Reset the second PCIE host controller	
5	USB_HOST2_RESET	RW	0x1	Reset the second USB host controller	
4	USB_PHY2_RESET	RW	0x1	Reset the second USB PHY	
3	USB_PHY2_SUSPEND_OVERRIDE	RW	0x0	0	Second USB PHY is in suspend state
				1	Second USB PHY suspend is controlled from the core
2:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	USB2_MODE	RW	0x0	USB mode	
				0	Host mode
				1	Device mode

10.7.15 PCIE EP Interrupt Mask (RST_PCIEEP_INTERRUPT_MASK)

Address: 0x180600C8
Access: Read/Write
Reset: 0x0

This register is the interrupt mask register for PCIE EP.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PCIEEP_WOW_INT	Mask for PCI EP WoW interrupt
4	PCIEEP_RST_INT	Mas bit for PCIE EP reset interrupt
3	HOST_RESET_INT	Mask bit for host reset interrupt
2	PCIEEP_L2_INT	Mask bit for L2 interrupt status from PCIE EP
1	PCIEEP_L1_INT	Mask bit for L1 interrupt status from PCIE EP
0	PCIEEP_L0S_INT	Mask bit for L0s interrupt status from PCIE EP

10.7.16 AHB Clock Gating (RST_CLKGAT_EN)

Address: 0x180600CC
Access: Read/Write
Reset: 0x1

This register controls the individual AHB clock gating for each interface.

Bit	Bit Name	Description
31:10	SPARE	Spare bits
9	WMAC	Enables AHB CLK to propagate for WMAC
8	USB2	Enables AHB CLK to propagate for USB2
7	USB1	Enables AHB CLK to propagate for USB1
6	GE1	Enables AHB CLK to propagate for GE1
5	GE0	Enables AHB CLK to propagate for GE0
4	CLK100_PCIERC	Enables 100 MHz PCIE REFCLK for first PCIE RC
3	CLK100_PCIERC2	Enables 100 MHz PCIE REFCLK for second PCIE RC
2	PCIE_RC2	Enables AHB CLK to propagate for second PCIE RC
1	PCIE_RC	Enables AHB CLK to propagate for PCIE RC
0	PCIE_EP	Enables AHB CLK to propagate for PCIE EP

10.8 GMAC Interface Registers

Table 10-9 summarizes the GMAC interface registers for the QCA9558.

Table 10-9 GMAC Interface Registers Summary

Address	Name	Description	Page
0x18070000	ETH_CFG	Ethernet Configuration	page 224
0x18070004	LUTS_AGER_INTR	LUTs Ager Interrupt Status	page 225
0x18070008	LUTS_AGER_INTR_MASK	LUTs Ager Interrupt Mask	page 225
0x18070014	SGMII_RESET	SGMII Reset	page 225
0x18070018	SGMII_SERDES	SERDES Control and Status Signals	page 227
0x1807001C	MR_AN_CONTROL	PHY Management Control	page 229
0x18070020	MR_AN_STATUS	PHY Management Status	page 230
0x1807002C	AN_NP_TX	Auto Negotiation Next Page Transmission	page 231
0x18070030	AN_LP_NP_RX	Auto Negotiation Next Page Receive	page 232
0x18070034	SGMII_CONFIG	SGMII Configuration	page 233
0x18070038	SGMII_MAC_RX_CONFIG	SGMII PHY Link Partner Ability	page 234
0x18070054	SGMII_RESOLVE	SGMII Resolution	page 234
0x1807005C	SGMII_INTERRUPT	SGMII Interrupt	page 235
0x18070060	SGMII_INTERRUPT_MASK	SGMII Interrupt Mask	page 235
0x18070064	PRBS_STATUS	PRBS Status	page 235

10.8.1 Ethernet Configuration (ETH_CFG)

Address: 0x18070000
Access: Read/Write
Reset: 0x0

This register determines how GMAC0 is interfaced in the QCA9558.

Bit	Bit Name	Type	Reset	Description
31:22	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
21:20	ETH_TXEN_DELAY	RW	0x0	Specific selection of the delay line for Tx En
19:18	ETH_TXD_ DELAY	RW	0x0	Specific selection of the delay line for Tx Data
17:16	ETH_RXDV_DELAY	RW	0x0	Specific selection of the delay line for Rx DV
15:14	ETH_RXD_DELAY	RW	0x0	Specific selection of the delay line for Rx Data
13:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read
6	GE0_SGMII	RW	0x0	GE0/GE1 connection setting
				0 GMAC0 connects as RGMII/MII. GMAC1 connects as SGMII
				1 GMAC0 connects as SGMII. GMAC1 connects as RGMII/MII
5	GE0_ERR_EN	RW	0x0	Enables ETX_ER and ERX_ER signals
4:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read
0	RGMII_EN	RW	0x0	When set to 1, the RGMII interface is enabled

10.8.2 LUTs Ager Interrupt Status (LUTs_AGER_INT)

Address: 0x18070004
Access: Read/Write
Reset: 0x0

This register configures the interrupt settings for the look up table (LUT).

Bit	Bit Name	Description	
31:4	RES	Reserved. Must be written with zero. Contains zeros when read.	
3:0	INTR	Denotes the interrupt status	
		Bit[0]	Egress fragmentation LUT
		Bit[1]	Egress LUT
		Bit[2]	Ingress fragmentation LUT
		Bit[3]	Ingress LUT

10.8.3 LUTs Ager Interrupt Mask (LUTS_AGER_INTR_MASK)

Address: 0x18070008
Access: Read/Write
Reset: See field description

This register configures the interrupt mask settings for the look up table (LUT).

Bit	Bit Name	Reset	Description		
31:4	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.		
3:0	INTR	0xF	Denotes the interrupt status mask		
			Bit[0]	Egress fragmentation LUT	
			Bit[1]	Egress LUT	
			Bit[2]	Ingress fragmenting LUT	
			Bit[3]	Ingress LUT	
				0	Interrupt masked
				1	Interrupt enabled

10.8.4 SGMII Reset (SGMII_RESET)

Address: 0x18070014
Access: Read/Write
Reset: 0x0

This register sends resets to the SGMII MAC or PHY from the GMII interface.

Bit	Bit Name	Type	Description
31:5	RES	RO	Reserved. Must be written with zero. Contains zeros when read.
4	HW_RX_125M_N	RW	Hardware reset used in registering all control signals programmed through APB registers to the 125 MHz RX_CLK domain
3	TX_125M_N	RW	Reset bit that resets the whole of the Tx 125 MHz domain
2	RX_125M_N	RW	Reset bit that resets the whole of the Rx 125 MHz domain

1	TX_CLK_N	RW	Reset bit for the TX_CLK (2.5, 25, 125 MHz)
0	RX_CLK_N	RW	Reset bit for the RX_CLK (2.5, 25, 125 MHz)

10.8.5 SERDES Control and Status Signals (SGMII_SERDES)

Address: 0x18070018
Access: Read/Write
Reset: See field description

This register comprises of all control/status signals to and from the SERDES.

Bit	Bit Name	Type	Reset	Description	
31:29	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
28:27	VCO_REG	RW	0x3	VCO speed increase	
				00	VCO increase speed by 10%
				01	VCO increased by 5%
				10	
				11	Default setting
26:23	RES_ CALIBRATION	RW	0x0	Resistor calibration from the PHY analog	
22	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
21:20	FIBER_MODE	RW	0x0	Indicates the fiber mode	
				00	Not in fiber mode
				01	100 Base-Tx mode and 1-bit recovered data
				10	Forbidden
				11	1000 Base-Tx mode
19:18	THRESHOLD_ CTRL	RW	0x0	Signal detection threshold setting control	
				00, 01	-2 dB
				10, 11	+2 dB
17	FIBER_SDO	RW	0x0	Fiber signal detection output indicating whether there is any data through the fiber	
				0	Valid data through the fiber
				1	No data through fiber
16	EN_SIGNAL_ DETECT	RW	0x1	SGMII signal detection	
				0	Disabled
				1	Enabled
15	LOCK_DETECT_ STATUS	RW	0x0	SGMII PLL lock status. For testing only.	
				0	PLL lock
				1	PLL not locked
14:11	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
10	VCO_SLOW	RW	0x0	SGMII PLL lock range. For testing only.	
9	VCO_FAST	RW	0x0	SGMII PLL lock range. For testing only.	
8	PLL_BW	RW	0x1	SGMII PLL bandwidth	
				0	Low bandwidth
				1	High bandwidth

7	TX_IMPEDANCE	RW	0x0	Rx output single-ended termination	
				0	50 Ω termination
				1	75 Ω termination
6:4	TX_DR_CTRL	RW	0x1	Driver output VDIFF	
				000	500 mV
				001	600 mV
				010	700 mV
				011	800 mV
				100	900 mV
				101	1 V
				110	1.1 V
				111	1.2 V
3	HALF_TX	RW	0x0	Tx driver amplitude	
				0	Tx driver amplitude normal
				1	Tx driver amplitude is half
2:1	CDR_BW	RW	0x3	CDR digital accumulator length control	
				00	± 0
				01	± 2
				10	± 4
				11	± 8
0	RX_IMPEDANCE	RW	0x0	Rx input single-ended termination	
				0	50 Ω termination
				1	75 Ω termination

10.8.6 PHY Management Control (MR_AN_CONTROL)

Address: 0x1807001C
Access: Read/Write
Reset: See field description

This register contains bit to control the PHY operation.

Bit	Bit Name	Type	Reset	Description	
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15	PHY_RESET	RW	0x0	0	PHY reset
				1	Normal operation
14	LOOPBACK	RW	0x0	0	Enable loopback mode
				1	Disable loopback mode
13	SPEED_SEL0	RW	0x0	LSB bit speed selection	
				00	10 Mb/s
				01	100 Mb/s
				10	1000 Mb/s
				11	Reserved
12	AN_ENABLE	RW	0x1	0	Disable auto-negotiation process
				1	Enable auto-negotiation process
11	POWER_DOWN	RW	0x0	Resets the whole PCS logic	
				0	Normal operation
				1	Power down
10	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
9	RESTART_AN	RW	0x0	0	Normal operation
				1	Restart auto-negotiation process
8	DUPLEX_MODE	RW	0x1	0	Half duplex
				1	Full duplex
7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
6	SPEED_SEL1	RW	0x1	MSB bit of speed selection	
				00	10 Mb/s
				01	100 Mb/s
				10	1000 Mb/s
				11	Reserved
5:0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	

10.8.7 PHY Management Status (MR_AN_STATUS)

Address: 0x18070020
Access: Read/Write
Reset: See field description

This register is for the auto-negotiation status.

Bit	Bit Name	Type	Reset	Description	
31:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
7	BASE_PAGE	RW	0x0	Indicates that the base page during auto-negotiation has been transmitted	
6	NO_PREAMBLE	RW	0x1	0	Indicates that PHY will not accept management frames with preamble pattern suppressed
				1	Indicates that PHY will accept management frames with preamble pattern suppressed
5	AN_COMPLETE	RW	0x0	0	Auto-negotiation incomplete
				1	Auto-negotiation complete
4	REMOTE_FAULT	RW	0x0	0	No remote fault condition detected
				1	Remote fault condition detected
3	AN_ABILITY	RW	0x1	Indicates that the SGMII PHY is capable to perform auto-negotiation	
2	LINK_UP	RW	0x0	0	Link down
				1	Link up
1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	EXT_CAPABILITY	RW	0x1	0	Basic register set capabilities only
				1	Indicates that SGMII PHY provides extended register capabilities

10.8.8 Auto Negotiation Next Page Transmission (AN_NP_TX)

Address: 0x1807002C
Access: Read/Write
Reset: See field description

This register contains the next page link code word to be transmitted when next page ability is supported.

Bit	Bit Name	Type	Reset	Description	
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15	NEXT_PAGE	RW	0x0	0	Next page not available
				1	Request to transmit next page
14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
13	MESSAGE_PAGE	RW	0x0	Differentiates a message page from an unformatted page	
				0	Unformatted page
				1	Message page
12	ACK2	RW	0x0	Acknowledge 2 is used by the NP function to indicate that a device can comply with the message	
				0	Cannot comply with message
				1	Will comply with message
11	TOGGLE	RW	0x0	Used by the arbitration function to synchronize with the link partner during next page exchange	
				0	Previous value of transmitted link code word equalled logic one
				1	previous value of transmitted link code word equalled logic zero
10:0	MSG_UNFORM_CODE	RW	0x0	Depends on bit [13] of this register. Message code field is an 11 bit wide field, encoding 2048 possible messages	

10.8.9 Auto Negotiation Next Page Receive (AN_LP_NP_RX)

Address: 0x18070030
Access: Read/Write
Reset: See field description

This register contains the next page link code word to be transmitted when next page ability is supported.

Bit	Bit Name	Type	Reset	Description	
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15	NEXT_PAGE	RW	0x0	0	Next page not available
				1	Request to transmit next page
14	ACK	RW	0x0	Acknowledge is used by the NP function to indicate that a device can comply with the message	
				0	Cannot comply with message
				1	Will comply with message
13	MESSAGE_PAGE	RW	0x0	Differentiates a message page from an unformatted page	
				0	Unformatted page
				1	Message page
12	ACK2	RW	0x0	Acknowledge 2 is used by the NP function to indicate that a device can comply with the message	
				0	Cannot comply with message
				1	Will comply with message
11	TOGGLE	RW	0x0	Used by the arbitration function to synchronize with the link partner during next page exchange	
				0	Previous value of transmitted link code word equalled logic one
				1	Previous value of transmitted link code word equalled logic zero
10:0	MSG_UNFORM_CODE	RW	0x0	Depends on bit [13] of this register. The message code field is an 11-bit wide field, encoding 2048 possible messages.	

10.8.10 SGMII Configuration (SGMII_CONFIG)

Address: 0x18070034
Access: Read/Write
Reset: See field description

This register contains configuration bits to enable SGMII mode of operation, PRBS, and MDIO.

Bit	Bit Name	Type	Reset	Description	
31:15	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
14	PRBS_BERT_ ENABLE	RW	0x0	Enables the bit error rate feature	
13	PRBS_ENABLE	RW	0x0	Enables the PRBS feature in SGMII	
12	MDIO_ COMPLETE	RW	0x0	Indicates that the MDIO command is completely received	
11	MDIO_PULSE	RW	0x0	Pulse signal to indicate that an MDIO command is ready for transmitting	
10	MDIO_ENABLE	RW	0x0	Enables SGMII-MDIO function	
9	NEXT_PAGE_ LOADED	RW	0x0	0	Next page not loaded
				1	Indicates the next page is loaded for transmitting during auto-negotiation
8	REMOTE_PHY_ LOOPBACK	RW	0x0	0	No remote PHY loopback
				1	Indicates the remote PHY loopback is enabled
7:6	SPEED	RW	0x0	Forces the speed to be a certain level; only valid when bit [5] is set	
				0	10 MBps
				1	100 MBps
				2	1000 MBps
5	FORCE_SPEED	RW	0x0	Indicates the speed selection is forced by CPU, when forced auto-negotiation is disabled	
4	RES	RO	0x0	Reserved	
3	ENABLE_SGMII_ TX_PAUSE	RW	0x0	Enable transmitting pause in the base page when in SGMII PHY mode	
2:0	MODE_CTRL	RW	0x0	SGMII mode control	
				0:1	RES
				2	SGMII_MAC

10.8.11 SGMII PHY Link Partner Ability (SGMII_MAC_RX_CONFIG)

Address: 0x18070038
Access: Read Only
Reset: See field description

This register indicates the SGMII PHY link partners abilities to the SGMII MAC. It is valid only when the MODE_CTRL bits in SGMII Configuration (SGMII_CONFIG) register is set to 0x2.

Bit	Bit Name	Type	Reset	Description	
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15	LINK	RO	0x0	0	Link down
				1	Link up
14	ACK	RO	0x0	Acknowledge is used to indicate that a PHY has also successfully received MAC's configuration information	
				0	Page not received
				1	Page received
13	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
12	DUPLEX_MODE	RO	0x0	Indicates the duplex mode of the LP	
				0	Half duplex
				1	Full duplex
11:10	SPEED_MODE	RO	0x0	The speed of the LP	
				00	10 MBps
				01	100 MBps
				10	1000 MBps
				11	Reserved
9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
8	AYSM_PAUSE	RO	0x0	Indicates device is capable of providing symmetric pause functions.	
7	PAUSE	RO	0x0	Indicates device is capable of providing symmetric pause functions.	
6:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	RES	RO	0x1	Reserved. Should be set to 1.	

10.8.12 SGMII Resolution (SGMII_RESOLVE)

Address: 0x18070054
Access: Read/Write
Reset: See field description

This register indicates the status of the priority resolution for duplex modes, pause capabilities, etc.

Bit	Bit Name	Type	Reset	Description
31:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
6	LINK_FAIL_CFGO	RW	0x0	Indicates a link failure during configuration
5	SYNC_STATUS	RW	0x0	Indicates a sync status
4	AN_SYNC_STATUS	RW	0x0	Indicates a sync status during auto-negotiation
3	RECEIVE_PAUSE_ ENABLE	RW	0x0	Receive pause capability enabled
2	TRANSMIT_PAUSE	RW	0x0	Transmit pause capability enabled
1	DUPLEX_ERROR	RW	0x0	Duplex mode between device and LP does not match
0	DUPLEX_MODE	RW	0x0	Device and LP resolved duplex mode as full duplex

10.8.13 SGMII Interrupt (SGMII_INTERRUPT)

Address: 0x1807005C
Access: Read/Write
Reset: See field description

This register causes an interrupt when there is a change in the link or in duplex modes.

Bit	Bit Name	Type	Reset	Description
31:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:0	INTR	RW	0x0	SGMII interrupt

10.8.14 SGMII Interrupt Mask (SGMII_INTERRUPT_MASK)

Address: 0x18070060
Access: Read/Write
Reset: See field description

This register is the mask to enable or disable SGMII interrupts.

Bit	Bit Name	Type	Reset	Description	
31:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
6:0	MASK	RW	0x0	0	Interrupt masked
				1	Interrupt enabled

10.8.15 PRBS Status (PRBS_STATUS)

Address: 0x18070064
Access: Read/Write
Reset: See field description

This register indicates the status of the PRBS operation.

Bit	Bit Name	Type	Reset	Description
31	BIT_SYNC	RW	0x0	PRBS bit sync from the SGMII interface
30	ERR	RW	0x0	PRBS error status from the SGMII interface
29:0	ERR_CNT	RW	0x0	PRBS error count in the SGMII interface

10.9 GE0 Ingress NAT / Egress NAT Registers

Table 10-10 summarizes the GE0 ingress/egress NAT registers for the QCA9558.

Table 10-10 GMAC0 Ingress NAT /Egress NAT Registers

Address	Name	Description	Page
0x18080000	EG_CPU_REQ	Egress CPU Requested LUT Entry Lookup	page 237
0x18080004	EG_CPU_REQ_STATUS	Egress CPU Request Status	page 238
0x18080008	EG_INFO_DW0	Egress DW0 Information	page 238
0x1808000C	EG_INFO_DW1	Egress DW1 Information	page 238
0x18080010	EG_CPU_REQUESTED_INFO_DW0	Egress CPU Requested DW0 Information	page 239
0x18080014	EG_CPU_REQUESTED_INFO_DW1	Egress CPU Requested DW1 Information	page 239
0x18080018	EG_KEY_DW0	Egress DW0 Key	page 239
0x1808001C	EG_KEY_DW1	Egress DW1 Key	page 239
0x18080020	EG_KEY_DW2	Egress DW2 Key	page 240
0x18080024	EG_KEY_DW3	Egress DW3 Key	page 240
0x18080028	EG_AGER_KEY_DW0	Egress Ageout DW0 Key	page 240
0x1808002C	EG_AGER_KEY_DW1	Egress Ageout DW1 Key	page 240
0x18080030	EG_AGER_KEY_DW2	Egress Ageout DW2 Key	page 241
0x18080034	EG_AGER_KEY_DW3	Egress Ageout DW3 Key	page 241
0x18080038	EG_AGER_INFO	Egress Ager FIFO Signals	page 241
0x1808003C	EG_MEM	Egress Memory	page 242
0x18080040	EG_MEM_DW0	Egress Memory DW0	page 242
0x18080044	EG_MEM_DW1	Egress Memory DW1	page 242
0x18080048	EG_MEM_DW2	Egress Memory DW2	page 242
0x1808004C	EG_MEM_DW3	Egress Memory DW3	page 243
0x18080050	EG_MEM_DW4	Egress Memory DW4	page 243
0x18080054	EG_LINKLIST	Egress Link List	page 243
0x18080058	EG_SUBTABLE	Egress Subtable Data	page 244
0x1808005C	EG_AGER_TICK	Egress Timer Ager Values	page 244
0x18080060	EG_AGER_TIMEOUT	Egress Ager Timeout	page 244
0x18080064	EG_REG	Egress ECO	page 245
0x18081000	IG_CPU_REQ	Ingress CPU Requested LUT Entry Lookup	page 245
0x18081004	IG_CPU_REQ_STATUS	Ingress CPU Request Status	page 246
0x18081008	IG_INFO_DW0	Ingress DW0 Information	page 246
0x1808100C	IG_INFO_DW1	Ingress DW1 Information	page 246
0x18081010	IG_INFO_DW2	Ingress DW2 Information	page 247
0x18081014	IG_INFO_DW3	Ingress DW3 Information	page 247
0x18081018	IG_CPU_REQUESTED_INFO_DW0	Ingress CPU Requested DW0 Information	page 247
0x1808101C	IG_CPU_REQUESTED_INFO_DW1	Ingress CPU Requested DW1 Information	page 247
0x18081020	IG_CPU_REQUESTED_INFO_DW2	Ingress CPU Requested DW2 Information	page 248
0x18081024	IG_CPU_REQUESTED_INFO_DW3	Ingress CPU Requested DW3 Information	page 248
0x18081028	IG_KEY_DW0	Ingress DW0 Key	page 248
0x1808102C	IG_KEY_DW1	Ingress DW1 Key	page 248

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Address	Name	Description	Page
0x18081030	IG_KEY_DW2	Ingress DW2 Key	page 249
0x18081034	IG_AGER_KEY_DW0	Ingress Ageout DW0 Key	page 249
0x18081038	IG_AGER_KEY_DW1	Ingress Ageout DW1 Key	page 249
0x1808103C	IG_AGER_KEY_DW2	Ingress Ageout DW2 Key	page 249
0x18081040	IG_AGER_INFO	Ingress Ager FIFO Signals	page 250
0x18081044	IG_MEM	Ingress Memory	page 250
0x18081048	IG_MEM_DW0	Ingress Memory DW0	page 250
0x1808104C	IG_MEM_DW1	Ingress Memory DW1	page 251
0x18081050	IG_MEM_DW2	Ingress Memory DW2	page 251
0x18081054	IG_MEM_DW3	Ingress Memory DW3	page 251
0x18081058	IG_MEM_DW4	Ingress Memory DW4	page 251
0x1808105C	IG_MEM_DW5	Ingress Memory DW5	page 252
0x18081060	IG_LINKLIST	Ingress Linklist	page 252
0x18081064	IG_SUBTABLE	Ingress Subtable Data	page 252
0x18081068	IG_AGER_TICK	Ingress Timer Ager Values	page 253
0x1808106C	IG_AGER_TIMEOUT	Ingress Ager Timeout	page 253

10.9.1 Egress CPU Requested LUT Entry Lookup (EG_CPU_REQ)

Address: 0x18080000
Access: Read/Write
Reset: See field description

This register denotes the CPU request to insert, delete or lookup an entry in the LUT.

Bit	Bit Name	Reset	Description	
31:7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
6:5	PKT_TYPE	0x1	Type of packet to be inserted into the LUT	
			1	TCP
			2	UDP
			3	ICMP
4	REQ	0x0	This bit is to be asserted to issue any command. Transitioning this bit from 0 to 1 is treated as a new request.	
3	INIT	0x0	Initializes the total LUT	
			0	Out of initialization
			1	Initialize
2:0	COMMAND	0x0	Indicates the type of operation the CPU wants to perform	
			1	Idle
			2	Lookup
			3	Insert
			4	Delete

10.9.2 Egress CPU Request Status (EG_CPU_REQ_STATUS)

Address: 0x18080004
Access: Read/Write
Reset: 0x0

This register denotes and sets status for CPU requests.

Bit	Bit Name	Description	
31:7	RES	Reserved. Must be written with zero. Contains zeros when read.	
6	BUCKET_ FULL	Denotes the status of the insertion request.	
		0	Indifferent
		1	Insertion failed because the bucket is full
5	REQ_ DONE	A one denotes the CPU request was fulfilled. To know the statuses of other commands such as insert_status, bins_full, bucket_full, check their respective statuses.	
4	INSERT_ STATUS	Indicates the status of the insert operation. This can be checked along with the COMMAND_STATUS.	
		0	Insertion not successful
		1	Insertion successful
3	BINS_ FULL	Current entry insertion failed due to bins_full	
2	DUPLICATE_KEY	Denotes the status of the inserted duplicate key.	
		1	Duplicate key inserted using the insert command
		2	Inserted key is not duplicate
1	DATA_ FOUND	This bit is checked when the COMMAND_STATUS or REQ_DONE bit is set to 1.	
		0	Data not found during lookup or deletion
		1	Data found during lookup or deletion
0	COMMAND_STATUS	This bit holds the equivalency of a CPU issued request	

10.9.3 Egress DW0 Information (EG_INFO_DW0)

Address: 0x18080008
Access: Read/Write
Reset: See field description

This register holds 31 bits of Egress information.

Bit	Bit Name	Reset	Description
31:0	DWORD	0x7FFFF	LSB 32 bits of Egress information

10.9.4 Egress DW1 Information (EG_INFO_DW1)

Address: 0x1808000C
Access: Read/Write
Reset: See field description

This register contains the MSB bit of the egress information that will be inserted into the LUT, along with the key.

Bit	Bit Name	Reset	Description
31:1	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	DWORD	0x1	MSB bit of egress information

10.9.5 Egress CPU Related DW0 Information (EG_CPU_ REQUESTED_INFO_DW0)

Address: 0x18080010
Access: Read/Write
Reset: 0x0

This register holds the egress LSB 32 bits found during deletion or lookup procedures.

Bit	Bit Name	Description
31:0	DWORD	32 LSB bits of the Egress key

10.9.6 Egress CPU Related DW1 Information (EG_CPU_ REQUESTED_INFO_DW1)

Address: 0x18080014
Access: Read/Write
Reset: 0x0

This register holds the egress MSB 32 bits found during deletion or lookup procedures.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	DWORD	32 LSB bits of the Egress key

10.9.7 Egress DW0 Key (EG_KEY_DW0)

Address: 0x18080018
Access: Read/Write
Reset: 0x0

This register holds the first LSB 32 bits of the Egress Key.

Bit	Bit Name	Description
31:0	DWORD0	First 32 LSB bits of the Egress key

10.9.8 Egress DW1 Key (EG_KEY_DW1)

Address: 0x1808001C
Access: Read/Write
Reset: 0x0

This register holds the second LSB 32 bits of the Egress Key.

Bit	Bit Name	Description
31:0	DWORD1	Second 32 LSB bits of the Egress key

10.9.9 Egress DW2 Key (EG_KEY_DW2)

Address: 0x18080020
Access: Read/Write
Reset: 0x0

This register holds the third LSB 32 bits of the Egress Key.

Bit	Bit Name	Description
31:0	DWORD2	Third32 LSB bits of the Egress key

10.9.10 Egress DW3 Key (EG_KEY_DW3)

Address: 0x18080024
Access: Read/Write
Reset: 0x0

This register holds MSB 2 bits of the Egress Key.

Bit	Bit Name	Description
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.
1:0	DWORD3	2 MSB bits of the Egress key

10.9.11 Egress Ageout DW0 Key (EG_AGER_KEY_DW0)

Address: 0x18080028
Access: Read-Only
Reset: 0x0

This register holds the first LSB 32 bits of the Egress Key deleted during the ageout process.

Bit	Bit Name	Description
31:0	DWORD0	First 32 LSB bits of the Egress key that were deleted during the ageout process

10.9.12 Egress Ageout DW1 Key (EG_AGER_KEY_DW1)

Address: 0x1808002C
Access: Read/Write
Reset: 0x0

This register holds the second LSB 32 bits of the Egress Key deleted during the ageout process.

Bit	Bit Name	Description
31:0	DWORD1	Second 32 LSB bits of the Egress key that were deleted during the ageout process

10.9.13 Egress Ageout DW2 Key (EG_AGER_KEY_DW2)

Address: 0x18080030
Access: Read/Write
Reset: 0x0

This register holds the third LSB 32 bits of the Egress Key deleted during the ageout process.

Bit	Bit Name	Description
31:0	DWORD2	Third 32 LSB bits of the Egress key that were deleted during the ageout process

10.9.14 Egress Ageout DW3 Key (EG_AGER_KEY_DW3)

Address: 0x18080034
Access: Read/Write
Reset: 0x0

This register holds MSB 2 bits of the key deleted during the ageout process.

Bit	Bit Name	Description
31:0	DWORD2	MSB 2 bits of the key deleted during the ageout process

10.9.15 Egress Ager FIFO Signals (EG_AGER_INFO)

Address: 0x18080038
Access: Read/Write
Reset: 0x0

This register denotes the statuses for the Ager FIFO signals.

Bit	Bit Name	Description	
31:3	RES	Reserved. Must be written with zero. Contains zeros when read.	
2	DISABLE	Denotes the status of the ager	
		0	Ager is active
		1	Ager is inactive
1	EMPTY	Denotes is the ager FIFO is empty or not	
		0	Ager FIFO is not empty
		1	Ager FIFO is empty
0	READ	A rising transition of this signal removes the key from the ager FIFO. This bit can only be read when the previous EMPTY bit is 0.	

10.9.16 Egress Memory (EG_MEM)

Address: 0x1808003C
Access: Read/Write
Reset: 0x0

This register is used to configure the settings for a memory read or write.

Bit	Bit Name	Description	
31:11	RES	Reserved. Must be written with zero. Contains zeros when read.	
10	ACK	Acknowledgement for a read/write	
9:8	RW	Set to read or write to the memory	
		0	Read
		1	Write
7:0	ADDR	Denotes the address of the MAIN_MEMORY for a read/write request	

10.9.17 Egress Memory DW0 (EG_MEM_DW0)

Address: 0x18080040
Access: Read/Write
Reset: 0x0

This register is used to read or write to the main memory.

Bit	Bit Name	Description
31:0	DWORD0	Read/Write the DWORD0 data to the main memory for a read/write request

10.9.18 Egress Memory DW1 (EG_MEM_DW1)

Address: 0x18080044
Access: Read-Only
Reset: 0x0

This register is used to read or write to the main memory.

Bit	Bit Name	Description
31:0	DWORD1	Read/Write the DWORD1 data to the main memory for a read/write request

10.9.19 Egress Memory DW2 (EG_MEM_DW2)

Address: 0x18080048
Access: Read-Only
Reset: 0x0

This register is used to read or write to the main memory.

Bit	Bit Name	Description
31:0	DWORD2	Read/Write the DWORD2 data to the main memory for a read/write request

10.9.20 Egress Memory DW3 (EG_MEM_DW3)

Address: 0x1808004C
Access: Read-Only
Reset: 0x0

This register is used to read or write to the main memory.

Bit	Bit Name	Description
31:0	DWORD3	Read/Write the DWORD3 data to the main memory for a read/write request

10.9.21 Egress Memory DW4 (EG_MEM_DW4)

Address: 0x18080050
Access: Read-Only
Reset: 0x0

This register is used to read or write to the main memory.

Bit	Bit Name	Description
31:0	DWORD4	Read/Write the DWORD4 data to the main memory for a read/write request

10.9.22 Egress Link List (EG_LINKLIST)

Address: 0x18080054
Access: Read/Write
Reset: 0x0

This register is used to read or write to the link list.

Bit	Bit Name	Description	
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.	
12:7	DATA	The Read/Write data of the link list	
6	RW	Link list Read/Write request	
		0	Read
		1	Write
5:0	ADDR	The link list address	

10.9.23 Egress Sub-Table Data (EG_SUBTABLE)

Address: 0x18080058
Access: Read/Write
Reset: 0x0

This register is used to read or write to the sub-table.

Bit	Bit Name	Description	
31:11	RES	Reserved. Must be written with zero. Contains zeros when read.	
10:5	DATA	Holds the Read/Write data related to the subtable	
4	RW	A Read/Write request for the subtable	
		0	Read
		1	Write
3:0	ADDR	The address of the subtable Read/Write address	

10.9.24 Egress Timer Ager Values (EG_AGER_TICK)

Address: 0x1808005C
Access: Read/Write
Reset: See field description

This register denotes the ager timer related values.

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
23:0	TIME	0x100000	A nano-second timer which allows MSECTIMER increment by one when the free running counter reaches the end of the timer value

10.9.25 Egress Ager Timeout (EG_AGER_TIME_OUT)

Address: 0x18080060
Access: Read/Write
Reset: 0x20

This register denotes the ager timeout value.

Bit	Bit Name	Description
31:22	ICMP_ VALUE	The ICMP timeout value which depends on the TIME bit in “Egress Timer Ager Values (EG_AGER_TICK)” on page 244
21:12	UDP_ VALUE	The UDP timeout value which depends on the TIME bit in “Egress Timer Ager Values (EG_AGER_TICK)” on page 244
11:0	TCP_ VALUE	TCP timeout value which depends on the TIME bit in “Egress Timer Ager Values (EG_AGER_TICK)” on page 244

10.9.26 Egress ECOs (EG_REG)

Address: 0x18080064
Access: Read-Only
Reset: 0x0

This register is used to read or write to the main memory.

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	SPARE	For ECOs

10.9.27 Ingress CPU Requested LUT Entry Lookup (IG_CPU_REQ)

Address: 0x18081000
Access: Read/Write
Reset: See field description

This register denotes the CPU request to insert, delete or lookup an entry in the LUT.

Bit	Bit Name	Reset	Description	
31:7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
6:5	PKT_TYPE	0x1	Type of packet to be inserted into the LUT	
			1	TCP
			2	UDP
			3	ICMP
4	REQ	0x0	This bit is to be asserted to issue any command. Transitioning this bit from 0 to 1 is treated as a new request.	
3	INIT	0x0	Initializes the total LUT	
			0	Out of initialization
			1	Initialize
2:0	COMMAND	0x0	Indicates the type of operation the CPU wants to perform	
			1	Idle
			2	Lookup
			3	Insert
			4	Delete

10.9.28 Ingress CPU Request Status (IG_CPU_REQ_STATUS)

Address: 0x18081004
Access: Read/Write
Reset: 0x0

This register denotes and sets status for CPU requests.

Bit	Bit Name	Description	
31:7	RES	Reserved. Must be written with zero. Contains zeros when read.	
6	BUCKET_ FULL	Denotes the status of the insertion request.	
		0	Indifferent
		1	Insertion failed because the bucket is full
5	REQ_ DONE	A one denotes the CPU request was fulfilled. To know the statuses of other commands such as insert_status, bins_full, bucket_full, check their status.	
4	INSERT_ STATUS	Indicates the status of the insert operation. This can be checked along with the COMMAND_STATUS.	
		0	Insertion not successful
		1	Insertion successful
3	BINS_ FULL	Current entry insertion failed due to bins_full	
2	DUPLICATE_KEY	Denotes the status of the inserted duplicate key.	
		1	Duplicate key inserted using the insert command
		2	Inserted key is not duplicate
1	DATA_ FOUND	This bit is checked when the COMMAND_STATUS or REQ_DONE bit is set to 1.	
		0	Data not found during lookup or deletion
		1	Data found during lookup or deletion
0	COMMAND_STATUS	This bit holds the equivalency of a CPU issued request	

10.9.29 Ingress DW0 Information (IG_INFO_DW0)

Address: 0x18081008
Access: Read/Write
Reset: 0xFFFFFFFF

This register holds 32 bits of Ingress information.

Bit	Bit Name	Description
31:0	DWORD0	32 bits of Ingress information which will be inserted into the LUT along with the key DWORD0 from the LSB

10.9.30 Ingress DW1 Information (IG_INFO_DW1)

Address: 0x1808100C
Access: Read/Write
Reset: 0xFFFFFFFF

This register holds 32 bits of Ingress information.

Bit	Bit Name	Description
31:0	DWORD1	32 bits of Ingress information which will be inserted into the LUT along with the key DWORD1 from the LSB

10.9.31 Ingress DW2 Information (IG_INFO_DW2)

Address: 0x18081010
Access: Read/Write
Reset: 0xFFFFFFFF

This register holds 32 bits of Ingress information.

Bit	Bit Name	Description
31:0	DWORD2	32 bits of Ingress information which will be inserted into the LUT along with the key DWORD2 from the LSB

10.9.32 Ingress DW3 Information (IG_INFO_DW3)

Address: 0x18081014
Access: Read/Write
Reset: 0xFFFFFFFF

This register holds 15 bits of Ingress information.

Bit	Bit Name	Description
31:15	RES	Reserved. Must be written with zero. Contains zeros when read.
14:0	DWORD3	15 bits of Ingress information which will be inserted into the LUT along with the key DWORD3 from the LSB

10.9.33 Ingress CPU Related DW0 Information (IG_CPU_ REQUESTED_INFO_DW0)

Address: 0x18081018
Access: Read/Write
Reset: 0xFFFFFFFF

This register holds 32 bits of Ingress information found during deletion or lookup operations.

Bit	Bit Name	Description
31:0	DWORD0	32 bits of Ingress information found during deletion or lookup of the operation DWORD0 from the LSB

10.9.34 Ingress CPU Related DW1 Information (IG_CPU_ REQUESTED_INFO_DW1)

Address: 0x1808101C
Access: Read/Write
Reset: 0xFFFFFFFF

This register holds 32 bits of Ingress information found during deletion or lookup operations.

Bit	Bit Name	Description
31:0	DWORD1	32 bits of Ingress information found during deletion or lookup of the operation DWORD1 from the LSB

10.9.35 Ingress CPU Related DW2 Information (IG_CPU_ REQUESTED_INFO_DW2)

Address: 0x18081020
Access: Read/Write
Reset: 0xFFFFFFFF

This register holds 32 bits of Ingress information found during deletion or lookup operations.

Bit	Bit Name	Description
31:0	DWORD2	32 bits of Ingress information found during deletion or lookup of the operation DWORD2 from the LSB

10.9.36 Ingress CPU Related DW3 Information (IG_CPU_ REQUESTED_INFO_DW3)

Address: 0x18081024
Access: Read/Write
Reset: 0xFFFFFFFF

This register holds 15 bits of Ingress information found during deletion or lookup operations.

Bit	Bit Name	Description
31:0	RES	Reserved. Must be written with zero. Contains zeros when read.
14:0	DWORD3	15 bits of Ingress information found during deletion or lookup of the operation DWORD3 from the LSB

10.9.37 Ingress DW0 Key (IG_KEY_DW0)

Address: 0x18081028
Access: Read/Write
Reset: 0x0

This register holds LSB 32 bits of the Ingress Key. First Dword from the LSB.

Bit	Bit Name	Description
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.
19:0	DWORD	20 LSB bits of the Ingress key

10.9.38 Ingress DW1 Key (IG_KEY_DW1)

Address: 0x1808102C
Access: Read/Write
Reset: 0x0

This register holds LSB 32 bits of the Ingress Key. Second Dword from the LSB.

Bit	Bit Name	Description
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.
19:0	DWORD	20 LSB bits of the Ingress key

10.9.39 Ingress DW2 Key (IG_KEY_DW2)

Address: 0x18081030
Access: Read/Write
Reset: 0x0

This register holds MSB 4 bits of the Ingress Key. Second Dword from the LSB

Bit	Bit Name	Description
31:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3:0	DWORD	4wqqqq MSB bits of the Ingress key

10.9.40 Ingress Ageout DW0 Key (IG_AGER_KEY_DW0)

Address: 0x18081034
Access: Read/Write
Reset: 0x0

This register holds the first Dword LSB bits of the Ingress Key deleted during the ageout process.

Bit	Bit Name	Description
31:0	DWORD0	First Dword LSB bits of the Ingress key deleted during the ageout process

10.9.41 Ingress Ageout DW1 Key (IG_AGER_KEY_DW1)

Address: 0x18081038
Access: Read/Write
Reset: 0x0

This register holds the second Dword LSB bits of the Ingress Key deleted during the ageout process.

Bit	Bit Name	Description
31:0	DWORD0	First Dword LSB bits of the Ingress key deleted during the ageout process

10.9.42 Ingress Ageout DW2 Key (IG_AGER_KEY_DW2)

Address: 0x1808103C
Access: Read/Write
Reset: 0x0

This register holds the first Dword LSB bits of the Ingress Key deleted during the ageout process.

Bit	Bit Name	Description
31:0	DWORD0	First Dword LSB bits of the Ingress key deleted during the ageout process

10.9.43 Ingress Ager FIFO Signals (IG_AGER_FIFO)

Address: 0x18081040
Access: Read/Write
Reset: See field description

This register denotes the statuses for the Ager FIFO signals.

Bit	Bit Name	Reset	Description	
31:3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
2	DISABLE	0x0	Denotes the status of the ager	
			0	Ager is active
			1	Ager is inactive
1	EMPTY	0x1	Denotes is the ager FIFO is empty or not	
			0	Ager FIFO is not empty
			1	Ager FIFO is empty
0	READ	0x0	A rising transition of this signal removes the key from the ager FIFO. This bit can only be read when the previous EMPTY bit is 0.	

10.9.44 Ingress Memory (IG_MEM)

Address: 0x18081044
Access: Read/Write
Reset: 0x0

This register is used to configure the settings for a memory read or write.

Bit	Bit Name	Description	
31:11	RES	Reserved. Must be written with zero. Contains zeros when read.	
10	ACK	Acknowledgement for a read/write	
9:8	RW	Set to read or write to the memory	
		0	Read
		1	Write
7:0	ADDR	Denotes the address of the MAIN_MEMORY for a read/write request	

10.9.45 Ingress Memory DW0 (IG_MEM_DW0)

Address: 0x18081048
Access: Read/Write
Reset: 0x0

This register is used to read or write to the main memory.

Bit	Bit Name	Description
31:0	DWORD0	Read/Write the DWORD0 data to the main memory for a read/write request from the LSB

10.9.46 Ingress Memory DW1 (IG_MEM_DW1)

Address: 0x1808104C
Access: Read/Write
Reset: 0x0

This register is used to read or write to the main memory.

Bit	Bit Name	Description
31:0	DWORD1	Read/Write the DWORD1 data to the main memory for a read or write request from the LSB

10.9.47 Ingress Memory DW2 (IG_MEM_DW2)

Address: 0x18081050
Access: Read/Write
Reset: 0x0

This register is used to read or write to the main memory.

Bit	Bit Name	Description
31:0	DWORD2	Read/Write the DWORD2 data to the main memory for a read or write request

10.9.48 Ingress Memory DW3 (IG_MEM_DW3)

Address: 0x18081054
Access: Read/Write
Reset: 0x0

This register is used to read or write to the main memory.

Bit	Bit Name	Description
31:0	DWORD3	Read/Write the DWORD3 data to the main memory for a read or write request

10.9.49 Ingress Memory DW4 (IG_MEM_DW4)

Address: 0x18081058
Access: Read/Write
Reset: 0x0

This register is used to read or write to the main memory.

Bit	Bit Name	Description
31:0	DWORD4	Read/Write the DWORD3 data to the main memory for a read or write request

10.9.50 Ingress Memory DW5 (IG_MEM_DW5)

Address: 0x1808105C
Access: Read/Write
Reset: 0x0

This register is used to read or write to the main memory.

Bit	Bit Name	Description
31:19	DWORD5	Read/Write the DWORD5 data to the main memory for a read or write request

10.9.51 Ingress Link List (IG_LINKLIST)

Address: 0x18081060
Access: Read/Write
Reset: 0x0

This register is used to read or write to the link list.

Bit	Bit Name	Description	
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.	
12:7	DATA	The Read/Write data of the link list	
6	RW	Link list Read/Write request	
		0	Read
		1	Write
5:0	ADDR	The link list address	

10.9.52 Ingress Sub-Table Data (IG_SUBTABLE)

Address: 0x18081064
Access: Read/Write
Reset: 0x0

This register is used to read or write to the sub-table.

Bit	Bit Name	Description	
31:11	RES	Reserved. Must be written with zero. Contains zeros when read.	
10:5	DATA	Holds the Read/Write data related to the subtable	
4	RW	A Read/Write request for the subtable	
		0	Read
		1	Write
3:0	ADDR	The address of the subtable Read/Write address	

10.9.53 Ingress Timer Ager Values (IG_AGER_TICK)

Address: 0x18081068
Access: Read/Write
Reset: See field description

This register denotes the ager timer related values.

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
23:0	TIME	0x100000	A nano-second timer which allows MSECTIMER increment by one when the free running counter reaches the end of the timer value

10.9.54 Ingress Ager Timeout (IG_AGER_TIMEOUT)

Address: 0x1808106C
Access: Read/Write
Reset: 0x20

This register denotes the ager timeout value.

Bit	Bit Name	Description
31:22	ICMP_ VALUE	The ICMP timeout value which depends on the TIME bit in “Ingress Timer Ager Values (IG_AGER_TICK)” on page 253
21:12	UDP_ VALUE	The UDP timeout value which depends on the TIME bit in “Ingress Timer Ager Values (IG_AGER_TICK)” on page 253
11:0	TCP_ VALUE	TCP timeout value which depends on the TIME bit in “Ingress Timer Ager Values (IG_AGER_TICK)” on page 253

10.10 MBOX Registers

Table 10-9 summarizes the MBOX registers for the QCA9558.

Table 10-11 MBOX Registers

Address	Name	Description	Page
0x180A0000	MBOX_FIFO	MBOX FIFO	page 255
0x180A0008	MBOX_FIFO_STATUS	Non-Destructive FIFO Status Query	page 255
0x180A000C	SLIC_MBOX_FIFO_STATUS	Non-Destructive SLIC FIFO Status Query	page 256
0x180A0010	MBOX_DMA_POLICY	Mailbox DMA Engine Policy Control	page 256
0x180A0014	SLIC_MBOX_DMA_POLICY	SLIC Mailbox DMA Engine Policy Control	page 257
0x180A0018	DMA_RX_DESCRIPTOR_BASE	Mailbox Rx DMA Descriptors Base Address	page 257
0x180A001C	MBOX_DMA_RX_CONTROL	Mailbox Rx DMA Control	page 258
0x180A0020	MBOX_DMA_TX_DESCRIPTOR_BASE	Mailbox Tx DMA Descriptors Base Address	page 258
0x180A0024	MBOX_DMA_TX_CONTROL	Mailbox Tx DMA Control	page 259
0x180A0028	SLIC_DMA_RX_DESCRIPTOR_BASE	Mailbox Rx DMA Descriptors Base Address	page 259
0x180A002C	MBOX1_DMA_RX_CONTROL	Mailbox Rx DMA Control	page 260
0x180A0030	MBOX1_DMA_TX_DESCRIPTOR_BASE	Mailbox Tx DMA Descriptors Base Address	page 260
0x180A0034	SLIC_DMA_TX_CONTROL	SLIC Tx DMA Control	page 261
0x180A0038	MBOX_FRAME	Mailbox FIFO Status	page 261
0x180A0040	FIFO_TIMEOUT	FIFO Timeout Period	page 261
0x180A0044	MBOX_INT_STATUS	MBOX Related Interrupt Status	page 262
0x180A0048	SLIC_MBOX_INT_STATUS	SLIC_MBOX Related Interrupt Status	page 262
0x180A004C	MBOX_INT_ENABLE	MBOX Related Interrupt Enables	page 263
0x180A0050	SLIC_MBOX_INT_ENABLE	SLIC_MBOX Related Interrupt Enables	page 263
0x180A0058	MBOX_FIFO_RESET	Reset and Clear MBOX FIFOs	page 264
0x180A005C	SLIC_MBOX_FIFO_RESET	SLIC Reset and Clear MBOX FIFOs	page 264

10.10.1 MBOX FIFO (MBOX_FIFO)

Address: 0x180A0000
Access: Read-Write
Reset: See field description

Mailbox PIO access registers This register provides PIO access to the mailbox FIFO. An individual mailbox should either be accessed via PIO or DMA, accessing the same mailbox via both PIO and DMA will cause undefined results.

Bit	Bit Name	Reset	Description	
31:20	RES	0x0	Reserved	
19:0	DATA	0x1	Maps to individual fields as follows:	
			Bit [19:17]	Reserved
			Bit [16]	FIFO Empty indication for the corresponding mailbox. This bit is a mirror of bit 2 of the Non-Destructive FIFO Status Query (MBOX_FIFO_STATUS) register. Gives an empty status before the actual read operation of the FIFO
			Bit [15:13]	Reserved
			Bit [12]	FIFO Full indication for the corresponding mailbox. This bit is a mirror of bit 0 of Non-Destructive FIFO Status Query (MBOX_FIFO_STATUS) register. Gives full indication before actual read operation of FIFO
			Bit [11:9]	Reserved
			Bit [8]	EOM: 1 bit EOM for the mailbox can be read or written here. This is just an additional bit of storage and can be treated as 9th bit of data
			Bit [7:0]	8 bit data for corresponding Mailbox can be read or written here

10.10.2 Non-Destructive FIFO Status Query (MBOX_FIFO_STATUS)

Address: 0x180A0008
Access: Read-Only
Reset: See field description

This register returns the status of the mailbox FIFOs. This register may be read at any time without changing the mailbox state.

Bit	Bit Name	Reset	Description
31:3	RES	0x0	Reserved
2	EMPTY	0x1	MBOX 0 Tx FIFO is empty (I^2S)
1	RES	0x0	Reserved
0	FULL	0x0	MBOX 0 Tx FIFO is full (I^2S)

10.10.3 Non-Destructive SLIC FIFO Status Query (SLIC_MBOX_FIFO_STATUS)

Address: 0x180A000C
Access: Read-Only
Reset: See field description

This register returns the status of the SLIC mailbox FIFOs. This register may be read at any time without changing the SLIC mailbox state.

Bit	Bit Name	Reset	Description
31:2	RES	0x0	Reserved
1	EMPTY	0x1	SLIC MBOX TX FIFO is empty (I^2S)
0	FULL	0x0	MBOX 0 Tx FIFO is full (I^2S0)

10.10.4 Mailbox DMA Engine Policy Control (MBOX_DMA_POLICY)

Address: 0x180A0010
Access: Read/Write
Reset: See field description

Controls when a trigger is generated for the MBOX DMA to start. Also contains the 16-bit and 32-bit byte swap settings for both Tx and Rx.

Bit	Bit Name	Reset	Description
31	SW_RESET	0x0	When set to 1, provides a soft reset to the I^2S MBOX DMA Engine. Software need to clear this bit after being set for the normal operation.
30:13	RES	0x0	Reserved
12	SRAM_AC	0x0	When set to 1, for HADDR from MBOX, the MSNibble is prefixed with 0x1. This enables access to the SRAM space from MBOX
11	TX_16BIT_SWAP	0x0	If set, transmit data will be swapped in 16-bit sub-words within a 32-bit word before being transmitted onto the interface.
10	RX_16BIT_SWAP	0x0	If this bit is set, data received from the interface will be swapped in 16bit sub-words within a 32bit word before DMA onto the system memory.
9	TX_END_SWAP	0x0	When set, transmit data will be byte swapped (Endian) across a 32-bit word before being transmitted onto the interface.
8	RX_END_SWAP	0x0	When set, data received from the interface will be byte swapped (Endian) across a 32-bit word before DMA onto the system memory
7:4	TX_FIFO_ THRESH0	0x4	Threshold for MBOX Tx FIFO in units of words (0 maps to 0 bytes, 1 maps to 4 bytes, etc). Reaching this threshold is a trigger for MBOX TX DMA to start.
3:0	RES	0x0	Reserved

10.10.5 SLIC Mailbox DMA Engine Policy Control (SLIC_MBOX_DMA_POLICY)

Address: 0x180A0014
Access: Read/Write
Reset: See field description

Controls when a trigger is generated for MBOX DMA to start. Also contains the 16-bit byte swap and 32-bit byte swap settings for both Tx and Rx.

Bit	Bit Name	Reset	Description
31	SW_RESET	0x0	When set to '1', provides a soft reset to the SLIC MBOX DMA Engine. Software need to clear this bit after being set for the normal operation.
30:13	RES	0x0	Reserved
12	SRAM_AC	0x0	When set to '1', for HADDR from MBOX, the MSNibble is prefixed with 0x1. This enables access to the SRAM space from MBOX
11	TX_16BIT_SWAP	0x0	If set, transmit data will be swapped in 16-bit sub-words within a 32-bit word before being transmitted onto the interface.
10	RX_16BIT_SWAP	0x0	If this bit is set, data received from the interface will be swapped in 16bit sub-words within a 32bit word before DMA onto the system memory.
9	TX_END_SWAP	0x0	When set, transmit data will be byte swapped (Endian) across a 32-bit word before being transmitted onto the interface.
8	RX_END_SWAP	0x0	When set, data received from the interface will be byte swapped (Endian) across a 32-bit word before DMA onto the system memory
7:4	TX_FIFO_THRESH0	0x4	Threshold for MBOX Tx FIFO in units of words (0 maps to 0 bytes, 1 maps to 4 bytes, etc). Reaching this threshold is a trigger for MBOX TX DMA to start.
3:0	RES	0x0	Reserved

10.10.6 MBOX0 Rx DMA Descriptors Base Address (MBOX0_DMA_RX_DESCRIPTOR_BASE)

Address: 0x180A0018
Access: Read/Write
Reset: 0x0

Holds the starting address of the descriptor chain for mailbox 0's Rx direction transfers. The DMA engine starts by fetching a descriptor from this address when the START bit in the MBOX0 Rx DMA Control (MBOX0_DMA_RX_CONTROL) register is set. All DMA descriptors must be 4-byte aligned, so the register's bottom two bits of the contents, as well as the bottom two bits of the next descriptor field of the individual descriptors are ignored and assumed to be zeros by the DMA engine.

For the purposes of the DMA engine, the Rx direction is defined to be transfers from the chip to the external interface and Tx to be transfers from external interface to the chip.

Bit	Bit Name	Description
31:28	RES	Reserved
27:2	ADDRESS	Most significant 26 bits of the 4-byte-aligned address of the first descriptor in the DMA chain
1:0	RES	Reserved

10.10.7 MBOX0 Rx DMA Control (MBOX0_DMA_RX_CONTROL)

Address: 0x180A001C
Access: Read/Write
Reset: 0x0

Controls the operational state of the DMA engine for mailbox 0's Rx direction transfers. The register should always be written in a one shot manner (only one of the operations should be specified) and can be polled to see if the desired operation has taken effect (indicated by the clearing of the corresponding bit). The DMA engine starts out stopped and must be kicked off for the first time with a START operation. The START operation causes the DMA engine to start fetching a descriptor at the address specified by the MBOX0 Rx DMA Descriptors Base Address (MBOX0_DMA_RX_DESCRIPTOR_BASE) register. Once this first descriptor has been fetched, if the DMA engine ever catches up with a CPU-owned descriptor, it can be requested to re-fetch the descriptor that it stalled on by programming the RESUME operation. Software can stop the operation of the DMA engine by programming the STOP operation. When the STOP operation is programmed, the DMA engine stops transfers immediately if it was already idle or at the end of the transfer of the current descriptor it is working on if it was busy. Note that this may leave incomplete messages in the mailbox FIFOs if the message in progress is scattered or gathered across multiple descriptors.

Bit	Bit Name	Description
31:3	RES	Reserved
2	RESUME	Programming a 1 to this field causes a potentially stalled (due to having caught up with CPU-owned descriptors) DMA engine to resume its transfers by refetching the last descriptor it had fetched and found to be CPU-owned. Software can use RESUME operations to add descriptors to the end of the descriptor chain (only modifying CPU-owned descriptors) in a race-free atomic manner. If the RESUME operation is programmed and the DMA engine is not stalled, it has no effect and is automatically cleared.
1	START	Programming a one to this field causes the DMA engine to start transferring data by fetching the descriptor pointed to by the MBOX0 Rx DMA Descriptors Base Address (MBOX0_DMA_RX_DESCRIPTOR_BASE) register. The START operation should usually be used only when the DMA engine is known to be stopped (after power-on or SOC reset) or after an explicit STOP operation.
0	STOP	Programming a one to this field causes the DMA engine to stop transferring any more data from this descriptor chain (after the current descriptor is completed, if a transfer is already in progress).

10.10.8 MBOX0 Tx DMA Descriptors Base Address (MBOX0_DMA_TX_DESCRIPTOR_BASE)

Address: 0x180A0020
Access: Read/Write
Reset: 0x0

See the description for the MBOX0 Rx DMA Descriptors Base Address (MBOX0_DMA_RX_DESCRIPTOR_BASE) register, as applied to mailbox 0's Tx direction transfers.

Bit	Bit Name	Description
31:28	RES	Reserved
27:2	ADDRESS	Most significant 26 bits of the 4-byte-aligned address of the first descriptor in the DMA chain
1:0	RES	Reserved

10.10.9 MBOX0 Tx DMA Control (MBOX0_DMA_TX_CONTROL)

Address: 0x180A0024
Access: Read/Write
Reset: 0x0

See the description for the MBOX0 Rx DMA Control (MBOX0_DMA_RX_CONTROL) register.

Bit	Bit Name	Description
31:3	RES	Reserved
2	RESUME	Programming a one to this field causes a potentially stalled (due to having caught up with CPU-owned descriptors) DMA engine to resume its transfers by re-fetching the last descriptor it had fetched and found to be CPU-owned. Software can use RESUME operations to keep adding descriptors to the end of the descriptor chain (only modifying CPU-owned descriptors) in a race free atomic manner. If the RESUME operation is programmed and the DMA engine is not stalled, it has no effect and is automatically cleared.
1	START	Programming a one to this field causes the DMA engine to start transferring data by fetching the descriptor pointed to by the MBOX0 Tx DMA Descriptors Base Address (MBOX0_DMA_TX_DESCRIPTOR_BASE) register. The START operation should usually be used only when the DMA engine is known to be stopped (after power-on or SOC reset) or after an explicit STOP operation.
0	STOP	Programming a one to this field causes the DMA engine to stop transferring any more data from this descriptor chain (after the current descriptor is completed, if a transfer is already in progress).

10.10.10 MBOX1 Rx DMA Descriptors Base Address (MBOX1_DMA_RX_DESCRIPTOR_BASE)

Address: 0x180A0028
Access: Read/Write
Reset: 0x0

This register holds the starting address of the descriptor chain for mailbox #1's RX direction transfers. The DMA engine starts by fetching a descriptor from this address when the START bit in the MBOX1 Rx DMA Control (MBOX1_DMA_RX_CONTROL) register is set. All DMA descriptors must be 4-byte aligned, so the bottom two bits of this register's contents, as well as the bottom two bits of the next descriptor field of the individual descriptors are ignored and assumed to be zeros by the DMA engine. For the purposes of the DMA engine, RX direction is defined to be transfers from Scorpion to the Interface say I^2S, and the TX direction is defined to be transfers from the Interface say I^2S to Scorpion.

Bit	Bit Name	Description
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.
27:2	ADDRESS	Most significant 26 bits of the 4-byte-aligned address of the first descriptor in the DMA chain
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

10.10.11 MBOX1 Rx DMA Control (MBOX1_DMA_RX_CONTROL)

Address: 0x180A002C
Access: Read/Write
Reset: 0x0

This register controls the operational state of the DMA engine for mailbox #1's RX direction transfers. The register should always be written in a one-hot manner, that is, only one of the operations should be specified. The bits can be polled to see if the desired operation has taken effect (indicated by the clearing of the corresponding bit). The basic operational states are Start indicating start of a DMA operation, Stop, indicating termination of a DMA operation, Stalled, which does not have a separate bit, and Resume, indicating resuming a stalled DMA operation.

Bit	Bit Name	Description
31:3	RES	Reserved. Must be written with zero. Contains zeros when read.
2	RESUME	Programming a 1 to this field causes a potentially stalled (due to having caught up with CPU-owned descriptors) DMA engine to resume its transfers by refetching the last descriptor it had fetched and found to be CPU-owned. Software can use RESUME operations to add descriptors to the end of the descriptor chain (only modifying CPU-owned descriptors) in a race-free atomic manner. If the RESUME operation is programmed and the DMA engine is not stalled, it has no effect and is automatically cleared.
1	START	Programming a one to this field causes the DMA engine to start transferring data by fetching the descriptor pointed to by the MBOX1 Rx DMA Descriptors Base Address (MBOX1_DMA_RX_DESCRIPTOR_BASE) register. The START operation should usually be used only when the DMA engine is known to be stopped (after power on or SOC reset) or after an explicit STOP operation.
0	STOP	Programming a one to this field causes the DMA engine to stop transferring any more data from this descriptor chain (after the current descriptor is completed, if a transfer is already in progress).

10.10.12 MBOX1 Tx DMA Descriptors Base Address (MBOX1_DMA_TX_DESCRIPTOR_BASE)

Address: 0x180A0030
Access: Read/Write
Reset: 0x0

See the description for the MBOX0 Rx DMA Descriptors Base Address (MBOX0_DMA_RX_DESCRIPTOR_BASE) register, as applied to mailbox 0's Tx direction transfers.

Bit	Bit Name	Description
31:28	RES	Reserved
27:2	ADDRESS	Most significant 26 bits of the 4-byte-aligned address of the first descriptor in the DMA chain
1:0	RES	Reserved

10.10.13 SLIC Tx DMA Control (SLIC_DMA_TX_CONTROL)

Address: 0x180A0034
Access: Read/Write
Reset: 0x0

See the description for the MBOX0 Rx DMA Control (MBOX0_DMA_RX_CONTROL) register.

Bit	Bit Name	Description
31:3	RES	Reserved
2	RESUME	Programming a one to this field causes a potentially stalled (due to having caught up with CPU-owned descriptors) DMA engine to resume its transfers by re-fetching the last descriptor it had fetched and found to be CPU-owned. Software can use RESUME operations to keep adding descriptors to the end of the descriptor chain (only modifying CPU-owned descriptors) in a race free atomic manner. If the RESUME operation is programmed and the DMA engine is not stalled, it has no effect and is automatically cleared.
1	START	Programming a one to this field causes the DMA engine to start transferring data by fetching the descriptor pointed to by the MBOX1 Tx DMA Descriptors Base Address (MBOX1_DMA_TX_DESCRIPTOR_BASE) register. The START operation should be used only when the DMA engine is known to be stopped (after power on or SOC reset) or after an explicit STOP operation.
0	STOP	Programming a one to this field causes the DMA engine to stop transferring any more data from this descriptor chain (after the current descriptor is completed, if a transfer is already in progress).

10.10.14 Mailbox FIFO Status (MBOX_FRAME)

Address: 0x180A0038
Access: Read-Only
Reset: See field description

Bit	Bit Name	Reset	Description
31:3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
2	RX_EOM	0x0	Rx FIFO contains a data byte with the EOM end of message marker set in the corresponding mailbox
1	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	RX_SOM	0x1	Rx FIFO contains a data byte with the SOM start of message marker set in the corresponding mailbox; a SOM byte always follows an EOM byte from the previous message

10.10.15 FIFO Timeout Period (FIFO_TIMEOUT)

Address: 0x180A0040
Access: Read/Write
Reset: See field description

If an MBOX RX FIFO is empty and an interface read arrives, or an MBOX TX FIFO is full and an interface write arrives, the DMA controller waits for the timeout period before declaring an error state. After an error is declared, all writes to full FIFOs are dropped and all reads from empty FIFO returns garbage data instead of a wait. After the error condition is cleared a write to ERROR_INT_STATUS will clear the error condition and the FIFOs will return to normal operation.

Bit	Bit Name	Reset	Description	
31:9	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
8	ENABLE	0x1	0	FIFO timeouts are disabled
			1	FIFO timeouts are enabled
7:0	VALUE	0xFF	Timeout value (in ms) when CORE_CLK = 40 MHz, or in 0.5 ms when CORE_CLK=80 MHz; should never be set to 0	

10.10.16 MBOX Related Interrupt Status (MBOX_INT_STATUS)

Address: 0x180A0044
Access: Read/Write-1-to-Clear
Reset: 0x0

This register contains the status of all the CPU directed Interrupt sources from the Mailbox #0.

Bit	Bit Name	Description
31:11	RES	Reserved. Must be written with zero. Contains zeros when read.
10	RX_DMA_COMPLETE	MBOX Rx DMA completion (one descriptor completed) interrupts
9	RES	Reserved. Must be written with zero. Contains zeros when read.
8	TX_DMA_EOM_ COMPLETE	MBOX Tx DMA completion of EOM (descriptor with EOM flag completed) interrupts
7	RES	Reserved. Must be written with zero. Contains zeros when read.
6	TX_DMA_COMPLETE	MBOX Tx DMA completion (one descriptor completed) interrupts
5	TX_OVERFLOW	MBOX Tx overflow error; the overflow condition is the same as the host interface overflow error
4	RX_UNDERFLOW	MBOX Rx underflow error; the underflow condition is the same as the host interface underflow error
3	RES	Reserved. Must be written with zero. Contains zeros when read.
2	TX_NOT_EMPTY	TX_NOT_EMPTY pending interrupt for Tx mailboxes; bit sets when the MBOX FIFO has insufficient space
1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	RX_NOT_FULL	RX_NOT_FULL pending interrupt for Rx mailboxes; bit sets when one or more exist

10.10.17 SLIC MBOX Related Interrupt Status (SLIC_MBOX_INT_ STATUS)

Address: 0x180A0048
Access: Read/Write-1-to-Clear
Reset: 0x0

This register contains the status of all the CPU directed Interrupt sources from the Mailbox #1 used by SLIC.

Bit	Bit Name	Description
31:7	RES	Reserved. Must be written with zero. Contains zeros when read.
6	RX_DMA_ COMPLETE	SLIC mailbox Rx DMA completion (one descriptor completed) interrupts
5	TX_DMA_EOM_ COMPLETE	SLIC mailbox Tx DMA completion of EOM (descriptor with EOM flag completed) interrupts
4	TX_DMA_COMPLETE	SLIC mailbox Tx DMA completion (one descriptor completed) interrupts
3	TX_OVERFLOW	SLIC MBOX Tx overflow error; the overflow condition is the same as the host interface overflow error
2	RX_UNDERFLOW	SLIC MBOX Rx underflow error; the underflow condition is the same as the host interface underflow error
1	TX_NOT_EMPTY	TX_NOT_EMPTY pending interrupt for SLIC Tx mailboxes; bit sets when the MBOX FIFO has no room
0	RX_NOT_FULL	RX_NOT_FULL pending interrupt for SLIC Rx mailboxes; bit sets when one or more exist

10.10.18 MBOX Related Interrupt Enables (MBOX_INT_ENABLE)

Address: 0x180A0028
Access: Read/Write
Reset: 0x0

This register is used to mask/enable interrupts to the CPU from Mailbox #0.

Bit	Bit Name	Description	
31:12	RES	Reserved	
11:10	RX_DMA_COMPLETE	Enable per mailbox Rx DMA completion interrupts	
9:8	TX_DMA_EOM_COMPLETE	Enable per mailbox Tx DMA completion of end of message interrupts	
7:6	TX_DMA_COMPLETE	Enable per mailbox Tx DMA completion interrupts	
5	TX_OVERFLOW	Enable MBOX Tx overflow error	
4	RX_UNDERFLOW	Enable MBOX Rx overflow error	
3:2	TX_NOT_EMPTY	Enable TX_NOT_EMPTY interrupts from MBOX Tx FIFOs	
		Bit [0]	Enable MBOX 0 TX_NOT_EMPTY interrupt
		Bit [1]	Enable MBOX 1 TX_NOT_EMPTY interrupt
1:0	RX_NOT_FULL	Enable RX_NOT_EMPTY interrupts from MBOX RX FIFOs	
		Bit [0]	Enable MBOX 0 RX_NOT_EMPTY interrupt
		Bit [1]	Enable MBOX 1 RX_NOT_EMPTY interrupt

10.10.19 SLIC MBOX Interrupt Enable (SLIC_MBOX_INT_ENABLE)

Address: 0x180A0050
Access: Read/Write
Reset: 0x0

This register is used to mask/enable interrupts to the CPU.

Bit	Bit Name	Description
31:7	RES	Reserved. Must be written with zero. Contains zeros when read.
6	RX_DMA_COMPLETE	SLIC mailbox Rx DMA completion interrupts
5	TX_DMA_EOM_COMPLETE	Enable SLIC mailbox Tx DMA completion of end of message interrupts
4	TX_DMA_COMPLETE	Enable SLIC mailbox Tx DMA completion interrupts
3	TX_OVERFLOW	Enable SLIC MBOX Tx overflow error
2	RX_UNDERFLOW	Enable SLIC MBOX Rx overflow error
1	TX_NOT_EMPTY	Enable TX_NOT_EMPTY interrupts from SLIC MBOX Tx FIFOs
0	RX_NOT_FULL	Enable RX_NOT_EMPTY interrupts from SLIC MBOX RX FIFOs

10.10.20 Reset and Clear MBOX FIFOs (MBOX_FIFO_RESET)

Address: 0x180A0058
Access: Read/Write
Reset: 0x0

Resets and clears data from MBOX0 FIFOs. This register should only be written to when no DMAs are in progress. For stereo applications, MBOX0 FIFOs should be reset at the beginning of each new audio stream (new VoIP call, etc.) The stereo block should also be reset when FIFOs are reset to maintain byte alignment.

Bit	Bit Name	Description	
31:3	RES	Reserved	
2	RX_INIT	Writing a 1 causes a Rx FIFO reset. The register is automatically reset to 0, and will always return 0 on a read.	
		RX_INIT[0]	Resets MBOX 0
		RX_INIT[1]	Resets MBOX 1
1	RES	Reserved	
1:0	TX_INIT	Writing a 1 will cause a TX FIFO reset. The register is automatically reset to 0, and will always return 0 on a read.	
		TX_INIT[0]	Resets MBOX 0
		TX_INIT[1]	Resets MBOX 1

10.10.21 SLIC Reset and Clear MBOX FIFOs (SLIC_MBOX_FIFO_RESET)

Address: 0x180A005C
Access: Read/Write
Reset: 0x0

Resets and clears data from SLIC MBOX1 FIFOs. This register should only be written to when no DMAs are in progress.

Bit	Bit Name	Description
31:3	RES	Reserved. Must be written with zero. Contains zeros when read.
1	RX_INIT	Writing a 1 causes a Rx FIFO reset; register resets to 0, and always returns 0 on a read.
0	TX_INIT	Writing a 1 will cause a Tx FIFO reset; register resets to 0, and always returns 0 on a read.

10.11 SLIC Registers

Table 10-12 summarizes the SLIC registers for the QCA9558.

Table 10-12 SLIC Registers

Address	Name	Description	Page
0x180A9000	SLIC_SLOT	SLIC Slots	page 265
0x180A9004	SLIC_CLOCK_CONTROL	SLIC Clock Control	page 265
0x180A9008	SLIC_CTRL	SLIC Control	page 266
0x180A900C	SLIC_TX_SLOTS1	SLIC Tx Slots1 Control	page 266
0x180A9010	SLIC_TX_SLOTS2	SLIC Tx Slots2 Control	page 267
0x180A9014	SLIC_RX_SLOTS1	SLIC Rx Slots1 Control	page 267
0x180A9018	SLIC_TX_SLOTS2	SLIC Tx Slots2 Control	page 267
0x180A901C	SLIC_TIMING_CTRL	SLIC Timing Control	page 268
0x180A9020	SLIC_INTR	SLIC Interrupt	page 269
0x180A9024	SLIC_SWAP	SLIC Swaps	page 269
0x180A9028	PWM_CTL	Pulse Width Modulation Control	page 269
0x180A9030	PWM_DATA	PWM Data	page 269

10.11.1 SLIC Slots (SLIC_SLOT)

Address: 0x180A9000
Access: Read/Write
Reset: See field description

This register indicates the maximum number of time slots supported by the connected SLIC device. The QCA9558 supports 1 to 64 slots, each one has a duration of 8 bits.

Bit	Bit Name	Reset	Description
31:7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:0	SEL	0x20	The number of SLIC slots

10.11.2 SLIC Clock Control (SLIC_CLOCK_CONTROL)

Address: 0x18090004
Access: Read/Write
Reset: 0x0

This register defines the divider value of AUDIO_PLL_CLK. A value of 1 indicates division by 2, 2 indicates division by 4, and so on. This value needs to be programmed based on the PLL_CLK frequency and maximum number of slots programmed using SLIC Slots (SLIC_SLOT).

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	DIV	Defines the divider value of AUDIO_PLL_CLK.

10.11.3 SLIC Control (SLIC_CTRL)

Address: 0x18090008
Access: Read/Write
Reset: See field description

This register defines the various control signals of the SLIC controller.

Bit	Bit Name	Reset	Description	
31:6	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
5:4	PLL_SOURCE_SEL	0x0	Master clock source	
			0	Master clock source is AUDIOPLL
			1	Master clock source is REF_CLK
			2	Master clock source is CLK100
			3	Master clock source is CLK125
3	CLK_EN	0x0	Acts as a clock gate enable. It gates the AUDIO_PLL/external clock.	
2	MASTER_SLAVE	0x1	Used to select the mode for SLIC control functionality	
			0	Slave mode. Indicates that the QCA9558 is a device on the PCM Highway and FS and SLIC_PCM_CLK are inputs.
			1	Master mode. Indicates that the QCA9558 is the master on the PCM highway and will drive the Frame Sync and SLIC_PCM_CLK signal.
1	SLIC_EN	0x0	Enables the total SLIC controller functionality either in master or slave mode	
0	RES	0x0	Reserved	

10.11.4 SLIC Tx Slots 1 (SLIC_TX_SLOTS1)

Address: 0x1809000C
Access: Read/Write
Reset: 0x0

This register defines the LSB 32 Tx slots, each bit corresponds to one of the 64 slots. Write a 1 to enable a particular slot.

Bit	Bit Name	Description
31:0	ONEHOT	Slots to be enabled. A 1 in any bit indicates the corresponding time slot is enabled.

10.11.5 SLIC Tx Slots 2 (SLIC_TX_SLOTS2)

Address: 0x18090010
Access: Read/Write
Reset: 0x0

This register defines the MSB 32 Tx slots, each bit corresponds to one of the 64 slots. Write a 1 to enable a particular slot.

Bit	Bit Name	Description
31:0	ONEHOT	Slots to be enabled. A 1 in any bit indicates the corresponding time slot is enabled.

10.11.6 SLIC Rx Slots 1 (SLIC_RX_SLOTS1)

Address: 0x18090014
Access: Read/Write
Reset: 0x0

This register defines the LSB 32 Rx slots, each bit corresponds to one of the 64 slots. Write a 1 to enable a particular slot.

Bit	Bit Name	Description
31:0	ONEHOT	Slots to be enabled. A 1 in any bit indicates the corresponding time slot is enabled.

10.11.7 SLIC Rx Slots 2 (SLIC_RX_SLOTS2)

Address: 0x18090018
Access: Read/Write
Reset: 0x0

This register defines the MSB 32 Rx slots, each bit corresponds to one of the 64 slots. Write a 1 to enable a particular slot.

Bit	Bit Name	Description
31:0	ONEHOT	Slots to be enabled. A 1 in any bit indicates the corresponding time slot is enabled.

10.11.8 SLIC Timing Control (SLIC_TIMING_CTRL)

Address: 0x1809001C
Access: Read/Write
Reset: See field description

This register sets the timing control related bits for FRAME_SYNC and data.

Bit	Bit Name	Reset	Description	
31:12	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
12:11	RXDATA_ SAMPLE_ POS_ EXTENDED	0x0	This bit, along with RX_DATA_SAMPLE_POS, provides a 3-bit field which controls when data will be sampled with respect to the frame sync posedge.	
			000	Rx Data sampled at the second posedge of the BIT_CLK after the framesync
			001	Rx Data sampled at the second negedge of BIT_CLK after framesync
			010	Rx Data sampled at the third negedge of BIT_CLK after framesync
			011	Rx Data sampled at the third posedge of BIT_CLK after framesync
			100	Rx Data will be sampled at the fourth posedge of BIT_CLK after framesync
			101	Rx Data will be sampled at the first posedge of BIT_CLK framesync
10	TXDATA_ FS_SYNC_ EXTEND	0x0	This bit (MSB), along with TXDATA_FS_SYNC field, provides a 3-bit field which controls software when Tx data will be shifted out with respect to the frame sync posedge.	
			000	Tx data will be sent at the first posedge of BIT_CLK after frame sync
			001	Tx data will be sent at the first negedge of BIT_CLK after frame sync
			010	Tx data will be sent in the second posedge of BIT_CLK after frame sync
			011	Tx data will be sent at the second negedge of BIT_CLK after frame sync
			100	Tx data will be sent in the third posedge of BIT_CLK after frame sync
			101	Tx data will be sent in the third posedge of BIT_CLK after frame sync
9	DATAOEN_ ALWAYS	0x0	0	The DATA_OEN is present for enabled slots
			1	The DATA_OEN is high for all slots
8:7	RXDATA_ SAMPLE_ POS	0x0	This field, along with the RXDATA_SAMPLE_POS_EXTEND bit, provides a 3-bit field which controls when data will be sampled with respect to frame sync posedge. See the descriptions for RXDATA_SAMPLE_POS_EXTEND.	
6:5	TXDATA_ FS_SYNC	0x1	This field, along with the TXDATA_FS_SYNC_EXTEND bit, provides a 3-bit field which controls when data will be sampled with respect to frame sync posedge. See the descriptions for TXDATA_FS_SYNC_EXTEND.	
4:2	LONG_ FSCLKS	0x0	This field depends on the LONG_FS. If the LONG_FS = 1, then this field specifies then number of BIT_CLKs for which FS is high.	
			0	1 BIT_CLK
			...	...
			7	8 BIT_CLKs
1	FS_POS	0x1	This field determines the relation between BIT_CLK and Framesync when the QCA9558 is in master mode	
			0	Send FS at the negative edge of the BIT_CLK
			1	Send FS at the positive edge of the BIT_CLK
0	LONG_FS	0x1	0	FS is high for a half bit clock
			1	FS is high for more than 1 BIT_CLK duration

10.11.9 SLIC Interrupt (SLIC_INTR)

Address: 0x18090020
Access: Read/Write
Reset: See field description

This register controls the SLIC interrupt and SLIC status registers.

Bit	Bit Name	Reset	Description	
31:6	RES	0x0	Reserved	
5	STATUS	0x0	Indicates unexpected Framesync received interrupt	
4:1	RES	0xF	Reserved	
0	MASK	0x1	0	Indicates the unexpected Framesync interrupt is MASKED
			1	Indicates the interrupt is enabled

10.11.10 SLIC Swap (SLIC_SWAP)

Address: 0x18090024
Access: Read/Write
Reset: 0x0

This register denotes the bit level swap registers at byte boundary for both Tx and Rx data.

Bit	Bit Name	Description	
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.	
1	RX_DATA	0	Do not swap the Rx byte
		1	Swap the Rx byte
0	TX_DATA	0	Do not swap the Tx byte
		1	Swap the Tx byte

10.11.11 Pulse Width Modulation Control (PWM_CTL)

Address: 0x1809002C
Access: Read/Write
Reset: 0x0

This is the control register for enabling Pulse Width Modulation.

Bit	Bit Name	Description
31	PWM_EN	Enables PWM output on SLIC data out
30	CONTINUOUS	Enables continuous shift of PWM data
29	START	When set to 1, the command to start shift is issued. When read as 0, the shift has started.
28	PWM_STOP	When set to 1, the command to stop shift is issued. When read as 0, the shift has stopped.
27:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:0	RPT_COUNT	Counter to shift PWM data. Tells the number of iterations.

10.11.12 PWM Data (PWM_DATA)

Address: 0x18090030
Access: Read/Write
Reset: 0x0

This is the control register for enabling Pulse Width Modulation.

Bit	Bit Name	Description
31:0	DATA32	Enables PWM output on SLIC data out

10.12 Stereo Registers

Table 10-13 summarizes the stereo registers for the QCA9558.

Table 10-13 Stereo Registers Summary

Address	Name	Description	Page
0x180B0000	STEREO_CONFIG	Configure Stereo Block	page 270
0x180B0004	STEREO_VOLUME	Set Stereo Volume	page 272
0x180B0008	STEREO_MASTER_CLOCK	Stereo Master Clock	page 273
0x180B000C	STEREO_TX_SAMPLE_CNT_LSB	Tx Sample Counter	page 273
0x180B0010	STEREO_TX_SAMPLE_CNT_MSB	Tx Sample Counter	page 273
0x180B0014	STEREO_RX_SAMPLE_CNT_LSB	Rx Sample Counter LSB	page 274
0x180B0018	STEREO_RX_SAMPLE_CNT_MSB	Rx Sample Counter MSB	page 274

10.12.1 Configure Stereo Block (STEREO_CONFIG)

Address: 0x180B0000
Access: Read/Write
Reset: See field description

This register controls the basic configuration of the stereo block.

Bit	Bit Name	Reset	Description	
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.		
23	SPDIF_ENABLE	0x0	Enables the SPDIF stereo block for operation	
22	REFCLK_SEL	0x0	Enables stereo to choose from external reference clock through a GPIO input or internal REF_CLK from crystal	
			0	Internal through crystal
			1	External through GPIO
21	ENABLE	0x0	Enables operation of the I^2S stereo block	
20	MIC_RESET	0x0	Resets the MIC buffers	
19	RESET	0x0	Resets the stereo buffers and I^2S state; Should be written to 1 when any of the data word sizes change, or if data synchronization is lost. Hardware will automatically clear to 0.	
18	I2S_DELAY	0x1	No delay: I2S_WS is available one clock cycle before data	
			0	No delay
			1	One I2S_CK delay: I2S_WS is asserted on the same CLK edge as the data
17	PCM_SWAP	0x0	This bit is used for swapping byte order of PCM samples	
16	MIC_WORD_SIZE	0x0	Causes configures microphone word size:	
			0	16-bit PCM words
			1	32-bit PCM words

15:14	STEREO_ MONO	0x0	Causes configures stereo or mono	
			0x0	Stereo
			0x1	Mono from channel 0
			0x2	Mono from channel 1
			0x3	Reserved
13:12	DATA_WORD_ SIZE	0x0	Controls the word size loaded into the PCM register from the MBOX FIFO. Data word size:	
			0x0	8 bits/word
			0x1	16 bits/word
			0x2	24 bits/word
			0x3	32 bits/word
11	I2S_WORD_ SIZE	0x0	Controls the word size sent to the external I^2S DAC. When set to 32 bit words, the PCM data will be left justified in the I^2S word. I^2S word size:	
			0	16 bits per I^2S word
			1	32 bits per I^2S word
10	MCK_SEL	0x0	When a DAC master clock is required, this field selects the raw clock source between divided audio clock and input master clock (MCLK_IN)	
			0	Raw master clock is divided audio PLL clock
			1	Raw master clock is MCLK_IN
9	SAMPLE_CNT _CLEAR_TYPE	0x0	Indicates the strategy used to clear the sample counter Tx and Rx registers	
			0	Write an explicit zero data through software to the Tx and Rx sample counter registers
			1	A software read of the Tx and Rx sample counter registers clears the counter registers
8	MASTER	0x1	This field controls the I2S_CK and I2S_WS master	
			0	External DAC is the master and drives I2S_CK and I2S_WS
			1	The QCA9558 is the master and drives I2S_CK and I2S_WS
7:0	POSEDGE	0x2	Counts in units of MCLK and can be calculated as follows: ■ Identify the relationship between MCLK and I^2S bit clock (I2S_SCK): I2S_SCK = MCLK / DIV Where DIV = MCLK/(SAMPLE_RATE * I2S_WORD_SIZE * 2 channels); a common example, a 44.1 KSps sample rate with 32 bits/word and a 11.2896 MHz MCLK would yield: DIV = 11.2896MHz/(44.1 KSps * 32 bits/word * 2) = 4 ■ Identify the relationship between I2S_SCK and SPDIF_SCK: If I2S_WORD_SIZE=16, then I2S_SCK = SPDIF_SCK / 4 If I2S_WORD_SIZE=32, then I2S_SCK = SPDIF_SCK / 2 Note that SPDIF is always 32 bits per word. ■ Determine the value of this register (POSEDGE): SPDIF_SCK = MCLK/POSEDGE	

10.12.2 Set Stereo Volume (STEREO_VOLUME)

Address: 0x180B0004
Access: Read/Write
Reset: 0x0

This register digitally attenuates or increases the volume level of the stereo output. Volume is adjusted in 6-dB steps. If the gain is set too high, the PCM values saturate and waveform clipping occurs.

Bit	Bit Name	Description	
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.	
12:8	CHANNEL1	Channel 1 gain/attenuation. Setting the gain above +7 is not supported. A 5 bit number; the MSB is a sign bit, the others are magnitude:	
		Binary (Decimal)	**Result**
		11111 (–16)	Maximum attenuation
		11110 (–14)	–84 dB
		...	...
		10001 (–1)	–6 dB
		10000 (0)	0 dB
		00000 (0)	0 dB
		00001 (+1)	+6 dB
		...	...
		00111 (+7)	+42 dB (maximum gain)
		01000 (+8)	Reserved
		...	...
		01111 (+15)	Reserved
7:5	RES	Reserved. Must be written with zero. Contains zeros when read.	
4:0	CHANNEL0	Channel 0 gain/attenuation. Setting the gain above +7 is not supported. A 5 bit number; the MSB is a sign bit, the others are magnitude:	
		Binary (Decimal)	**Result**
		11111 (–16)	Maximum attenuation
		11110 –14)	–84 dB
		...	...
		10001 (–1)	–6 dB
		10000 (0)	0 dB
		00000 (0)	0 dB
		00001 (+1)	+6 dB
		...	...
		00111 (+7)	+42 dB (maximum gain)
		01000 (+8)	Reserved
		...	...
		01111 (+15)	Reserved

10.12.3 Stereo Master Clock (STEREO_MASTER_CLOCK)

Address: 0x180B0008
Access: Read/Write
Reset: 0x0

This register is used to configure the stereo block.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	MCK_SEL	Master clock select

10.12.4 Tx Sample Counter (STEREO_TX_SAMPLE_CNT_LSB)

Address: 0x180B000C
Access: Read/Write
Reset: 0x0

This register counts the number of Tx samples transmitted by stereo. This register holds the 16 LSBs of the sample counter.

Bit	Bit Name	Description
31:16	CH1	Holds the 16 LSBs of Tx CH1 sample counter
15:0	CH0	Holds the 16 LSBs of Tx CH0 sample counter; also, these are the 16 LSBs of the sample counter

10.12.5 Tx Sample Counter (STEREO_TX_SAMPLE_CNT_MSB)

Address: 0x180B0010
Access: Read/Write
Reset: 0x0

This register counts the number of Tx samples transmitted by stereo. This register holds only the 16 MSBs of the sample counter.

Bit	Bit Name	Description
31:16	CH1	Holds the 16 MSBs of Tx CH1 sample counter
15:0	CH0	Holds the 16 MSBs of Tx CH0 sample counter; also, these are the 16 LSBs of the sample counter

10.12.6 Rx Sample Counter (STEREO_RX_SAMPLE_CNT_LSB)

Address: 0x180B0014
Access: Read/Write
Reset: 0x0

This register counts the number of Rx samples transmitted by stereo. This register holds only the 16 LSBs of the sample counter.

Bit	Bit Name	Description
31:16	CH1	Holds the 16 LSBs of Rx CH1 sample counter
15:0	CH0	Holds the 16 LSBs of Rx CH0 sample counter

10.12.7 Rx Sample Counter (STEREO_RX_SAMPLE_CNT_MSB)

Address: 0x180B0018
Access: Read/Write
Reset: 0x0

This register counts the number of Rx samples transmitted by stereo. This register holds only the 16 MSBs of the sample counter.

Bit	Bit Name	Description
31:16	CH1	Holds the 16 MSBs of Rx CH1 sample counter
15:0	CH0	Holds the 16 MSBs of Rx CH0 sample counter

10.13 MDIO Registers

Table 10-14 summarizes the BOOT MDIO registers for the QCA9558. Please note that these registers are not IEEE-compliant MDIO registers, but are generic register space accessible to the external host through the MDIO interface.The host can use them to download target firmware.

Table 10-14 BOOT MDIO Registers Summary

Address	Name	Description	Page
0x180B8000 - 0180B801C	MDIO_REG	MDIO APBs	page 275
0x180B8020	MDIO_ISR	MDIO Interrupt	page 275
0x180B8024	MDIO_PHY_ADDR	MDIO Slave PHY Addresses	page 275

10.13.1 MDIO APB Registers (MDIO_REG)

MDIO_REG0 Address: 0x180B8000
MDIO_REG1 Address: 0x180B8004
MDIO_REG2 Address: 0x180B8008
MDIO_REG3 Address: 0x180B800C
MDIO_REG4 Address: 0x180B8010
MDIO_REG5 Address: 0x180B8014
MDIO_REG6 Address: 0x180B8018
MDIO_REG7 Address: 0x180B801C
Access: Read/Write
Reset: 0x0

Each register contains MDIO master data.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	VALUE	RW	0x0	MDIO master data

10.13.2 MDIO Interrupt (MDIO_ISR)

Address: 0x180B8020
Access: Read to clear
Reset: 0x0

This register denotes the registers modified by the external host.

Bit	Bit Name	Type	Reset	Description
31:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	REGS	RCLR	0x0	Registers modified by the external host. One bit per register. (individual bits)

10.13.3 MDIO Slave PHY Addresses (MDIO_PHY_ADDR)

Address: 0x180B8024
Access: Read/Write
Reset: 0x0

This register denotes the address of the MDIO slave.

Bit	Bit Name	Type	Reset	Description
31:3	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
2:0	VALUE	RW	0x7	Address of the MDIO Slave

10.14 PCIE RC Control Registers

Table 10-15 summarizes the PCIE RC control registers for the QCA9558.

Table 10-15 PCIE RC Control Registers

RC1 Address	RC1 Address	Name	Description	Page
0x180F0000	0x18250000	PCIE_APP	PCIE Application Control	page 277
0x180F0004	0x18250004	PCIE_AER	PCIE Interrupt and Error	page 278
0x180F0008	0x18250008	PCIE_PWR_MGMT	PCIE Power Management	page 278
0x180F000C	0x1825000C	PCIE_ELEC	PCIE Electromechanical	page 279
0x180F0010	0x18250010	PCIE_CFG	PCIE Configuration	page 279
0x180F0014	0x18250014	PCIE_RX_CNTL	PCIE Receive Completion	page 280
0x180F0018	0x18250018	PCIE_RESET	PCIE Reset	page 280
0x180F001C	0x1825001C	PCIE_DEBUG	PCIE Debug and Control	page 281
0x180F0024	0x18250024	PCIE_PHY_RW_DATA	PCIE PHY Read/Write Data	page 281
0x180F0028	0x18250028	PCIE_PHY_TRG_RD_LOAD	PCIE PHY Serial Interface Load/Read Trigger	page 282
0x180F002C	0x1825002C	PCIE_PHY_CFG_DATA	PCIE PHY Configuration Data	page 282
0x180F0030	0x18250030	PCIE_MAC_PHY	PCIE MAC-PHY Interface Signals	page 282
0x180F0034	0x18250034	PCIE_PHY_MAC	PCIE PHY-MAC Interface Signals	page 283
0x180F0038	0x18250038	PCIE_SIDEBAND1	PCIE Sideband Bus1	page 283
0x180F003C	0x1825003C	PCIE_SIDEBAND2	PCIE Sideband Bus2	page 283
0x180F0040	0x18250040	PCIE_SPARE	PCIE Spare	page 284
0x180F0044	0x18250044	PCIE_MSI_ADDR	PCIE MSI Lower Address	page 284
0x180F0048	0x18250048	PCIE_MSI_DATA	PCIE MSI Data Value	page 284
0x180F004C	0x1825004C	PCIE_INT_STATUS	PCIE Interrupt Status	page 284
0x180F0050	0x18250050	PCIE_INT_MASK	PCIE Interrupt Mask	page 286
0x180F0054	0x18250054	PCIE_ERR_CNT	PCIE Error Counter	page 287
0x180F0058	0x18250058	PCIE_REQ_LATENCY_W_INT	PCIE AHB Latency Interrupt Counter	page 287
0x180F005C	0x1825005C	PCIE_MISC	Miscellaneous PCIE Bits	page 287

10.14.1 PCIE Application Control (PCIE_APP)

RC1 Address: 0x180F0000
RC2 Address: 0x18250000
Access: Read/Write
Reset: See field description

This register provides various control and status bits to configure the PCIE RC core from the application side.

Bit	Bit Name	Reset	Description	
31:22	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
21:20	CFG_TYPE	0x0	0	Sending a configuration transaction to the immediate downstream component (switch, endpoint) (Default)
			1	Sending a type 1 configuration transaction to multiple endpoints via a switch.
19:16	PCIE_BAR_MSN	0x1	Most significant nibble of the register PCIE Interrupt and Error (PCIE_AER).	
15:12	CFG_BE	0xF	Used as the byte enable of the next configuration request sent out on the PCIE interface.	
11:6	SLV_RESP_ ERR_MAP	0x3F	AHB slave response for a previous PCIE transaction. THe response bits are mapped as: 6 bits == {completion_tlp_abort, completion_ecrc, completion_ep, completion_crs, completion_ca, completion_ur}, where:	
			0	SLVERR
			1	DECERR
5:4	MSTR_RESP_ ERR_MAP	0x0	AHB master response error map. This signal allows the application to select a master response error report mechanism received from an AHB response channel to the CPL status of native PCIE core transmissions. MSB is not currently used. ■ When the LSB is set to 0, it will set an AHB response error to a CA of a PCIE completion: 2 bits == {decerr, slverr} ■ When the LSB is set to 1, it will set an AHB response error to a UR of a PCIE completion.	
3	INIT_RST	0x0	Application request to initiate a training reset	
2	PM_XMT_ TURNOFF	0x0	Application signal to generate PM turnoff messages for power management	
1	UNLOCK_MSG	0x0	Wakeup status because of power fault	
0	LTSSM_ENABLE	0x0	Application signal to enable the LTSSM. If set to zero, it indicates that the application is not ready.	

10.14.2 PCIE Interrupt and Error (PCIE_AER)

RC1 Address: 0x180F0004
RC1 Address: 0x18250004
Access: Read-Only
Reset: 0x0

This register contains common transmit and receive advanced error (AER) counters, such as bad DLLP, BAD TLP, NAKS, REPLAY TIMEOUTS, and so on.

Bit	Bit Name	Description
31:24	ERR_CNT4	Counter for replay timeouts/replay rollover
23:16	ERR_CNT3	Counter for receive errors (coding and disparity errors)
15:8	ERR_CNT2	Counter for transmit NAKs
7:0	ERR_CNT1	Counter for bad TLP and DLLP errors

10.14.3 PCIE Power Management (PCIE_PWR_MGMT)

RC1 Address: 0x180F0008
RC2 Address: 0x18250008
Access: Read/Write
Reset: 0x0

This register controls application control and status signals needed for power management.

Bit	Bit Name	Description
31:9	RES	Reserved
8	PME_INT	Interrupt caused by PME
7	ASSERT_CLKREQ	Signal to enable the common PHY in RC mode to turn off clocks to the EP; set after the EP has asserted PCIE1_CLKOUT_N to indicate readiness for clock removal (tracked through a GPIO interrupt).
6	RADM_PM_TO_ACK	Receipt of a PME turnoff acknowledgement message (the signal that indicates that the RC received a PME_TO_ACK message)
5	RADM_PM_PME	Receipt of a PME message (the signal that indicates that the RC received a PM_PME message)
4	AUX_PM_EN	AUX power PM enable; enable device to draw auxiliary power independent of PME AUX power
3	READY_ENTR_L23	Indication from the application that it is ready to enter the L2/L3 state
2	REQ_EXIT_L1	Request from the application to exit ASPM state L1, only effective if L1 is enabled
1	REQ_ENTRY_L1	Capability for applications to request PM state to enter L1; only effective if ASPM of L1 is enabled
0	AUX_PWR_DET	Auxiliary power detected; indicates that auxiliary power (VAUX) is present

10.14.4 PCIE Electromechanical (PCIE_ELEC)

RC1 Address: 0x180F000C
RC2 Address: 0x1825000C
Access: See field description
Reset: 0x0

Bit	Bit Name	Access	Description
31:3	RES	RW	Reserved
2	SYS_ATTEN_ BUTTON_PRESSED	RW	Attention button pressed. Indicates that the system attention button was pressed, sets the attention button pressed bit in the Slot Status register
1	CLK_REQ_N	RO	Clock enable Allows the application clock generation module to turn off CORE_CLK based on the current power management state:
			0 CORE_CLK must be active for the current power state
			1 Current power state allows CORE_CLK to be shut down
0	WAKE_N	RO	Wake up from power management unit. PCIE RC core generates WAKE_L to request the system to restore power and clock when a beacon has been detected. Assertion of WAKE_L could be a clock or multiple clock cycles.

10.14.5 PCIE Configuration (PCIE_CFG)

RC1 Address: 0x180F0010
RC1 Address: 0x18250010
Access: Read/Write
Reset: 0x0

This registers controls application control and status signals to configure core behavior.

Bit	Bit Name	Description
31	RES	Reserved. Must be written with zero. Contains zeros when read.
30:26	INT_MSG_NUM	Advanced error interrupt message number Used when MSI or MSI-X is enabled. Assertion of CFG_AER_RC_ERR_MSI along with a value on CFG_AER_INT_MSG_NUM is equivalent to the RC core receiving an MSI with the CFG_AER_INT_MSG_NUM value as the MSI vector.
25	EML_CONTROL	Electromechanical interlock control; this bit denotes the state of the electromechanical interlock control bit in PCIE Electromechanical (PCIE_ELEC) register.
24	PWR_CTRLER_ CTRL	Power controller control; this bit controls the system power controller (from bit [10] of the PCIE Receive Completion (PCIE_RX_CNTL) register).
23:22	ATTEN_IND	Attention indicator control; these bits control the system attention indicator) from bits [7:6] of the PCIE Receive Completion (PCIE_RX_CNTL) register).
21:17	PBUS_DEV_NUM	Configured device number; denotes the device number assigned to the device.
16:9	PBUS_NUM	The configured primary bus number. These bits denote the primary bus number assigned to the device.
8	RCB	The read completion boundary (RCB). This bit denotes the value of the RCB bit in the Link Control register in the PCIE RC.
7:5	MAX_PAYLOAD_ SIZE	The maximum payload size. This bit denotes the value of the MAX_PAYLOAD_SIZE field in the Device Control register in the PCIE RC.
4:2	MAX_RDREQ_ SIZE	The maximum read request size. This bit denotes the value of the MAX_READ_ REQUEST_SIZE field in the Device Control register in the PCIE RC.
1	MEM_SPACE_EN	Memory space enable; this bit denotes the state of the Memory Space Enable bit in the PCI-compatible Command register in the PCIE RC.
0	BUS_MASTER_ EN	Bus master enable; this bit denotes the state of the Bus Master Enable bit in the PCI-compatible Command register in the PCIE RC.

10.14.6 PCIE Receive Completion (PCIE_RX_CNTL)

RC1 Address: 0x180F0014
RC2 Address: 0x18250014
Access: Read-Only
Reset: 0x0

This register is used to denote the field values related to the completion timeout of the PCIE.

Bit	Bit Name	Description
31:29	RES	Reserved. Must be written with zero. Contains zeros when read.
28:21	TIMEOUT_CPL_ TAG	The tag field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted
20:9	TIMEOUT_CPL_ LEN	The length field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted.
8:7	TIMEOUT_CPL _ATTR	The attributes field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted.
6:4	TIMEOUT_CPL_ TC	The traffic class of the timed out completion. This bit is valid when the PCIE core Rx timeout signal is asserted.
3:1	TIMEOUT_FN_ NUM	The function number of the timed out completion. This bit is valid when the PCIE core Rx timeout signal is asserted.
0	CPL_TIMEOUT	The completion timeout. This bit indicates that the completion TLP for a request has not been received within the expected time window.

10.14.7 PCIE Reset (PCIE_RESET)

RC1 Address: 0x180F0018
RC2 Address: 0x18250018
Access: Read/Write
Reset: See field description

This register is used to set the bits for the PCIE reset.

Bit	Bit Name	Reset	Description	
31:3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
2	EP_RESET_L	0x1	The reset bit for indicating an endpoint reset through the PCIE PHY	
1	LINK_REQ_ RESET	0x0	The reset request due to a link down status. A high-to-low transition indicates that the RC Core is requesting external logic to reset the RC Core because the PHY link is down.	
0	LINK_UP	0x0	Indicates if the PHY link is up or down	
			0	Link is down
			1	Link is up

10.14.8 PCIE Debug and Control (PCIE_DEBUG)

RC1 Address: 0x180F001C
RC2 Address: 0x1825001C
Access: Read/Write
Reset: See field description

This register controls application and status signals for additional debug and configuration of the core behavior.

Bit	Bit Name	Reset	Description
31:18	RES	0x0	Reserved
17	AHB_MSTR_DATA_SWAP_EN	0x0	AHB master: byte swap configuration option
16	PCIE_PHY_READY	0x0	PCIE PHy's ready signal
15	RXVALID_EXT_ENABLE	0x0	Enable bit for extending rxvalid from PHY by three clocks
14	BYTESWAP	0x1	AHB slave: byte swap configuration option
13	PM_STATUS	0x0	Power management status: PME status bit from the PMCSR
12	PM_PME_EN	0x0	Power management event (PME) enable: PME enable bit in the PMCSR
11:9	PM_DSTATE	0x0	Current power management D-state of the function
8:4	XMLH_LTSSM_STATE	0x0	Current LTSSM state
3:1	PM_CURNT_STATE	0x0	Current power state
0	RDLH_LINK_UP	0x0	DATA link layer up/down indicator This status from the flow control initialization state machine indicates that flow control has been initiated and the data link Layer is ready to transmit and receive packets.
			0 Link is down
			1 Link is up

10.14.9 PCIE PHY Read/Write Data (PCIE_PHY_RW_DATA)

RC1 Address: 0x180F0024
RC2 Address: 0x18250024
Access: Read/Write
Reset: 0x0

This register would trigger a read and a write to the PCIE PHY Serial Interface.

Bit	Bit Name	Description
31:0	PHY_DATA	PCIE PHY data read/write

10.14.10 PCIE PHY Serial Interface Load/Read Trigger (PCIE_PHY_TRG_RD_LOAD)

RC1 Address: 0x180F0028
RC2 Address: 0x18250028
Access: Read-Only
Reset: 0x0

This register triggers a read or a load for the PCIE PHY serial interface.

Bit	Bit Name	Description	
31:0	PARALLEL_LOAD_OP_DONE	Bit 0	Parallel Load: Trigger a Parallel Load to the PCIE PHY - Would be cleared on Operation Complete
		Bit 31	OP_DONE: Indicates that the previous Operation is completed. Read / Write - Gets cleared on read/write to PCIE_PHY_RW_DATA register

10.14.11 PCIE PHY Configuration Data (PCIE_PHY_CFG_DATA)

RC1 Address: 0x180F002C
RC2 Address: 0x1825002C
Access: Read-Only
Reset: 0x0 (32'd5)

Bit	Bit Name	Description
31:0	PHY_CFG_DATA	PCIE PHY configuration data

10.14.12 PCIE MAC-PHY Interface Signals (PCIE_MAC_PHY)

RC1 Address: 0x180F0030
RC2 Address: 0x18250030
Access: Read-Only
Reset: See field description

This register is used to denote the interface signals for the MAC-PHY interface.

Bit	Bit Name	Description	
31:24	RES	Reserved	
23:22	PWRDOWN	The power control. Power control bits to the PHY. The MAC_PHY_POWERDOWN is a 2-bit signal that is shared by all Lanes.	
		00	P0 (normal operation)
		01	P0s (Low power, small latency for recovery)
		10	P1 (Much lower power but longer latency for recovery)
		11	P2 (Lowest power state)
21	RXPOLARITY	Inverted polarity on receive	
20	TXCOMPLIANCE	MAC_PHY_TX compliance status	
19	TXELECIDLE	Transmit electrical idle status	
18	TXDETRX_LOOPBACK	Status of MAC_PHY_TXDETECTRX from RC	
17:16	TXDATAK	Data/control indication for transmit data symbols. When set to 1, indicates a "K" or control symbol.	
15:0	TXDATA	PCIE RC transmit data from MAC to PHY	

10.14.13 PCIE PHY-MAC Interface Signals (PCIE_PHY_MAC)

RC1 Address: 0x180F0034
RC2 Address: 0x18250034
Access: Read-Only
Reset: 0x0

This register is used to denote the interface signals for the PHY-MAC interface.

Bit	Bit Name	Description
31:26	RES	Reserved. Must be written with zero. Contains zeros when read.
25	RXDETECT_DONE	Indicated a successful receiver detection
24	PHYSTATUS_ASSERTED	Indicates that PHYSTATUS (bit [22])has been asserted
23	RXVALID	Indicates PIPE Rx data valid
22	PHYSTATUS	Indicates PIPE PHY status
21:19	RXSTATUS	Indicates PIPE Rx status
18	RXELECIDLE	Indicates PIPE electrical idle
17:16	RXDATAK	Data/control for the receive data symbols
15:0	RXDATA	PIPE receive data

10.14.14 PCIE Sideband Bus1 (PCIE_SIDEBAND1)

RC1 Address: 0x180F0038
RC2 Address: 0x18250038
Access: Read-Only
Reset: 0x0

This register is used to control additional PHY purposes.

Bit	Bit Name	Description
31:0	CFG_PHY_CONTROL	The output bus that can be used for additional PHY control purposes. The CFG_ PHY_CONTROL bus maps to the PHY control register.

10.14.15 PCIE Sideband Bus2 (PCIE_SIDEBAND2)

RC1 Address: 0x180F003C
RC2 Address: 0x1825003C
Access: Read-Only
Reset: 0x0

This register is used to control additional PHY purposes.

Bit	Bit Name	Description
31:0	CFG_PHY_CONTROL	The output bus that can be used for additional PHY control purposes. The CFG_ PHY_CONTROL bus maps to the PHY control register.

10.14.16 PCIE Spare (PCIE_SPARE)

RC1 Address: 0x180F0040
RC2 Address: 0x18250040
Access: Read-Only
Reset: 0x0

This register is contains spare bits for the PCIE.

Bit	Bit Name	Description
31:0	BITS	Spare bits for the PCIE

10.14.17 PCIE MSI Lower Address (PCIE_MSI_ADDR)

RC1 Address: 0x180F0044
RC2 Address: 0x18250044
Access: Read/Write
Reset: 0x0

This register holds the lower address for the MSI.

Bit	Bit Name	Description
31:0	LADDR	The lower address register for the MSI

10.14.18 PCIE MSI Data Value (PCIE_MSI_DATA)

RC1 Address: 0x180F0048
RC2 Address: 0x18250048
Access: Read/Write
Reset: 0x0

This register is used to hold the data for the MSI including vector.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	VALUE	These bits hold the data for the MSI including vector [4:0]. The pattern assigned by the system software.

10.14.19 PCIE Interrupt Status (PCIE_INT_STATUS)

RC1 Address: 0x180F004C
RC2 Address: 0x1825004C
Access: Read/Write
Reset: 0x0

This register reflects the status of currently active interrupts. A 1 in a bit position indicates the corresponding interrupt is active.

Bit	Bit Name	Description
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.
27	LINK_DOWN	XMLH link down interrupt
26	LINK_REQ_RST	Request for reset from the PCIE RC core to the application.
25:22	MSI_VEC	Indicates which MSI interrupt has happened
21	CPU_INTD	The status bit to indicate that an INTD assertion has occurred and the client needs to send a deassert interrupt

20	CPU_INTC	The status bit to indicate that an INTC assertion has occurred and the client needs to send a deassert interrupt
19	CPU_INTB	The status bit to indicate that an INTB assertion has occurred and the client needs to send a deassert interrupt
18	CPU_INTA	The status bit to indicate that an INTA assertion has occurred and the client needs to send a deassert interrupt
17	INTDL	PCI 3.0 compatible, level triggered INTD virtual wire interrupt. This interrupt is ON on reception of INTD assertion message and stays on till the corresponding deassertion message is received.
16	INTCL	PCI 3.0 compatible, level triggered INTC virtual wire interrupt. This interrupt is ON on reception of INTC assertion message and stays on till the corresponding deassertion message is received.
15	INTBL	PCI 3.0 compatible, level triggered INTB virtual wire interrupt. This interrupt is ON on reception of INTB assertion message and stays on till the corresponding deassertion message is received.
14	INTAL	PCI 3.0 compatible, level triggered INTA virtual wire interrupt. This interrupt is ON on reception of INTA assertion message and stays on till the corresponding deassertion message is received.
13	SYS_ERR	A system error. The RC Core asserts CFG_SYS_ERR_RC if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL.
12	AER_MSI	Advanced error MSI or MSI-X indication; CFG_AER_RC_ERR_MSI is set when: ■ MSI or MSI-X is enabled ■ A reported error condition causes a bit to be set in the Root Error Status register. ■ The associated error message reporting enable bit is set in the Root Error Command register.
11	AER_INT	Advanced error reporting interrupt; This interrupt is set when an internally generated error message is to be propagated to the software by PCIE root complex.
10	MSI_ERR	Error MSI interrupt Interrupt is set whenever an MSI error message is received by the PCIE root complex.
9	MSI	The interrupt caused by the MSI
8	INTD	PCI 3.0 compatible, edge triggered INTD virtual wire interrupt This interrupt is set on reception of INTD assertion message; software must explicitly write a 0 to this bit to clear the interrupt condition.
7	INTC	PCI 3.0 compatible, edge triggered INTC virtual wire interrupt This interrupt is set on reception of INTC assertion message; software must explicitly write a 0 to this bit to clear the interrupt condition.
6	INTB	PCI 3.0 compatible, edge triggered INTB virtual wire interrupt This interrupt is set on reception of INTB assertion message; software must explicitly write a 0 to this bit to clear the interrupt condition.
5	INTA	PCI 3.0 compatible, edge triggered INTA virtual wire interrupt This interrupt is set on reception of INTA assertion message; software must explicitly write a 0 to this bit to clear the interrupt condition.
4	RADMX_COMP_ LOOKUP_ERR	The RADMX response composer TAG lookup error. This is a fatal error condition.
3	GM_COMP_ LOOKUP_ERR	GM response composer TAG lookup error. This is a fatal error condition.
2	FATAL_ERR	The received fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_FATAL message
1	NONFATAL_ERR	The received non-fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_NONFATAL message
0	CORR_ERR	The received correctable error message. One clock cycle pulse that indicates that the RC core received an ERR_COR message.

10.14.20 PCIE Interrupt Mask (PCIE_INT_MASK)

RC1 Address: 0x180F0050
RC2 Address: 0x18250050
Access: Read/Write
Reset: 0x0

Selectively enables or disables propagation of interrupts. A “1” in a bit position enables the corresponding interrupt being asserted. A “0” in a bit position disables the corresponding interrupt being asserted.

Bit	Bit Name	Description
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.
27	LINK_DOWN	XMLH link down interrupt mask
26	LINK_REQ_RST	PCIE RC link reset link request int mask
25:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17	INTDL	Mask for the assertion+deassertion of the INTD virtual wire level-triggered interrupt.
16	INTCL	Mask for the assertion+deassertion of the INTC virtual wire level-triggered interrupt.
15	INTBL	Mask for the assertion+deassertion of the INTB virtual wire level-triggered interrupt.
14	INTAL	Mask for the assertion+deassertion of the INTA virtual wire level-triggered interrupt.
13	SYS_ERR	System error interrupt mask
12	AER_MSI	Mask for advanced error (AER) MSI or MSI-X indication interrupt
11	AER_INT	AER interrupt mask
10	MSI_ERR	MSI error interrupt
9	MSI	Interrupt caused by the MSI
8	INTD	INTD virtual wire edge triggered interrupt mask
7	INTC	INTC virtual wire edge triggered interrupt mask
6	INTB	INTB virtual wire edge triggered interrupt mask
5	INTA	INTA virtual wire edge triggered interrupt mask
4	RADMX_COMP_ LOOKUP_ERR	RADMX response composer TAG lookup error mask
3	GM_COMP_ LOOKUP_ERR	GM response composer TAG lookup error mask
2	FATAL_ERR	Received fatal error message interrupt (RADM_FATAL_ERR) mask
1	NONFATAL_ERR	Received non-fatal error message (RADM_NONFATAL_ERR) mask
0	CORR_ERR	Received correctable error message interrupt (RADM_CORRECTABLE_ERR) mask

10.14.21 PCIE Error Counter (PCIE_ERR_CNT)

RC1 Address: 0x180F0054
RC2 Address: 0x18250054
Access: Read/Write
Reset: 0x0

This register keeps a count of the number of errors related to PCIE RC.

Bit	Bit Name	Description
31:0	VALUE	Indicates the number of errors related to PCIE RC; can include: bad DLLP, bad TLP, NAKS, REPLAY TIMEOUTS, and so on.

10.14.22 PCIE AHB Latency Interrupt Counter (PCIE_REQ_LATENCY_W_INT)

RC1 Address: 0x180F0058
RC2 Address: 0x18250058
Access: Read/Write
Reset: 0x0

This register is a counter to indicate the AHB Request to AHB Ready Latency of PCIE when an interrupt is asserted.

Bit	Bit Name	Description
31	ENABLE	Counter enable
30:0	VALUE	Indicates the latency

10.14.23 Miscellaneous PCIE Bits (PCIE_MISC)

RC1 Address: 0x180F005C
RC2 Address: 0x1825005C
Access: Read/Write
Reset: 0x0

This register contains miscellaneous spare CPU writable bits.

Bit	Bit Name	Description
31:0	BITS	Spare bits for the PCIE

10.15 WDMA Registers

Table 10-16 shows the mapping of the general DMA and Rx-related (WMAC interface) registers.

Table 10-16 WDMA Registers

Offset	Name	Description	Page
0x18100008	CR	Command	page 289
0x18100014	CFG	Configuration and Status	page 289
0x18100018	RXBUFPTR_THRESH	Rx DMA Data Buffer Pointer Threshold	page 290
0x1810001C	TXDPPTR_THRESH	Tx DMA Descriptor Pointer Threshold	page 290
0x18100020	MIRT	Maximum Interrupt Rate Threshold	page 290
0x18100024	IER	Interrupt Global Enable	page 291
0x18100028	TIMT	Tx Interrupt Mitigation Thresholds	page 291
0x1810002C	RIMT	Rx Interrupt Mitigation Thresholds	page 291
0x18100030	TXCFG	Transmit Configuration	page 292
0x18100034	RXCFG	Receive Configuration	page 293
0x18100040	MIBC	MIB Control	page 293
0x18100060	DATABUF	Data Buffer Length	page 294
0x18100064	GTT	Global Transmit Timeout	page 294
0x18100068	GTTM	Global Transmit Timeout Mode	page 294
0x1810006C	CST	Carrier Sense Timeout	page 295
0x18100070	RXDP_SIZE	Size of High and Low Priority	page 295
0x18100074	RX_QUEUE_HP_RXDP	Lower 32 bits of MAC Rx High Priority Queue RXDP Pointer	page 295
0x18100078	RX_QUEUE_LP_RXDP	Lower 32 bits of MAC Rx Low Priority Queue RXDP Pointer	page 295
0x18100080	ISR_P	Primary Interrupt Status	page 296
0x18100084	ISR_S0	Secondary Interrupt Status 0	page 297
0x18100088	ISR_S1	Secondary Interrupt Status 1	page 298
0x1810008C	ISR_S2	Secondary Interrupt Status 2	page 298
0x18100090	ISR_S3	Secondary Interrupt Status 3	page 299
0x18100094	ISR_S4	Secondary Interrupt Status 4	page 299
0x18100098	ISR_S5	Secondary Interrupt Status 5	page 300
0x181000A0	IMR_P	Primary Interrupt Mask	page 301
0x181000A4	IMR_S0	Secondary Interrupt Mask 0	page 302
0x181000A8	IMR_S1	Secondary Interrupt Mask 1	page 302
0x181000AC	IMR_S2	Secondary Interrupt Mask 2	page 303
0x181000B0	IMR_S3	Secondary Interrupt Mask 3	page 303
0x181000B4	IMR_S4	Secondary Interrupt Mask 4	page 304
0x181000B8	IMR_S5	Secondary Interrupt Mask 5	page 304
0x181000C0	ISR_P_RAC	Primary Interrupt Status Read-and-Clear	page 305
0x181000C4	ISR_S0_S	Secondary Interrupt Status 0 (Shadow Copy)	page 305
0x181000C8	ISR_S1_S	Secondary Interrupt Status 1 (Shadow Copy)	page 305
0x181000D0	ISR_S2_S	Secondary Interrupt Status 2 (Shadow Copy)	page 305
0x181000D4	ISR_S3_S	Secondary Interrupt Status 3 (Shadow Copy)	page 306
0x181000D8	ISR_S4_S	Secondary Interrupt Status 4 (Shadow Copy)	page 306
0x181000DC	ISR_S5_S	Secondary Interrupt Status 5 (Shadow Copy)	page 306

10.15.1 Command (CR)

Offset: 0x18100008
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:11	RES	Reserved
10:7	SPARE	Spare bits
6	SWI	Software interrupt; this bit is one-shot/auto-cleared, so it always reads as 0
5	RXD	Rx disabled
4	RES	Reserved
3	RXE_HP	Receive enabled; this read-only bit indicates RxDMA status for HP frames. Set when SW writes to the RxBP register and cleared when RxDMA runs out of RxBP or RxD is asserted.
2	RXE_LP	Receive enabled; this read-only bit indicates RxDMA status for LP frames. Set when software writes to RXBUFPTR_THRESH register and cleared when RxDMA runs out of RXBUFPTR_THRESH or when RxD is asserted.
1:0	RES	Reserved

10.15.2 Configuration and Status (CFG)

Offset: 0x18100014
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31:19	RES	0x0	Reserved	
18:17	FULL_THRESHOLD	0x0	PCIE core master request queue full threshold	
			0	Use default value of 4
			3:1	Use indicated value
16:13	RES	0x0	Reserved	
12	CFG_HALT_ACK	0x0	DMA halt status	
			0	DMA has not yet halted
			1	DMA has halted
11	CFG_HALT_REQ	0x0	DMA halt in preparation for reset request	
			0	DMA logic operates normally
			1	Request DMA logic to stop so software can reset the MAC; Bit [12] indicates when the halt has taken effect; the DMA halt is not recoverable; once software sets bit [11] to request a DMA halt, software must wait for bit [12] to be set and reset the MAC.
10	CFG_CLKGATE_DIS	0x0	0	Allow clock gating in all DMA blocks to operate normally
			1	Disable clock gating in all DMA blocks (for debug use)
9:6	RES	0x0	Reserved	
5	REG_CFG_ADHOC	0x0	0	AP mode: MAC is operating either as an AP or as a STA in a BSS
			1	Ad hoc mode: MAC is operating as a STA in an IBSS
4	MODE_MMR	0x0	Byteswap register access (MMR) data words	
3	MODE_RCV_DATA	0x0	Byteswap Rx data buffer words	
2	MODE_RCV_DESC	0x0	Byteswap Rx descriptor words	
1	MODE_XMIT_DATA	0x0	Byteswap Tx data buffer words	
0	MODE_XMIT_DESC	0x0	Byteswap Tx descriptor words	

10.15.3 Rx DMA Data Buffer Pointer Threshold (RXBUFPTR_ THRESH)

Offset: 0x18100018
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:15	RES	Reserved
14:8	LP_DATA	Indicates the Rx DMA data buffer pointer threshold. An interrupt will be asserted (if enabled) if the number of available data buffer pointers is less than this threshold. There is a separate threshold for high and low priority buffers.
7:4	RES	Reserved
3:0	HP_DATA	Indicates the Rx DMA data buffer pointer threshold. An interrupt will be asserted (if enabled) if the number of available data buffer pointers is less than this threshold. The high and low priority buffers have separate thresholds.

10.15.4 Tx DMA Descriptor Pointer Threshold (TXDPPTR_THRESH)

Offset: 0x1810001C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:4	RES	Reserved
3:0	DATA	Indicates the Tx DMA descriptor pointer threshold. An interrupt will be asserted (if enabled) if the number of available descriptor pointers for any of the 10 queues is less than this threshold.

10.15.5 Maximum Interrupt Rate Threshold (MIRT)

Offset: 0x18100020
Access: Read/Write
Reset: 0x0

This register is described in ms up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The maximum interrupt rate timer is started when either the TXINTM or RXIMTM status bits are set. TXMINTR or RXMINTR are asserted at this time. No future TXINTM or RXINTM events can cause the TXMINTR or TXMINTR to be asserted until this timer has expired. If both the TXINTM and RXINTM status bits are set while the timer is expired then the TXMINTR and RXMINTR will round robin between the two.

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	INTR_RATE_THRESH	Maximum interrupt rate threshold

10.15.6 Interrupt Global Enable (IER)

Offset: 0x18100024
Access: Read/Write
Reset: 0x0

Enables hardware signalling of interrupts.

Bit	Bit Name	Description
31:1	RES	Reserved
0	ENABLE	Writing a 0 enables hardware signaling of interrupts

10.15.7 Tx Interrupt Mitigation Thresholds (TIMT)

Offset: 0x18100028
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:16	TX_FIRST_ PKT_THRESH	Tx first packet threshold This register is in µs up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The Tx first packet timer starts counting after any Tx completion. If the timer is still counting when the next Tx completion occurs, it resets and starts over. The first Tx packet timer expires when either the last Tx packet threshold equals the last Tx packet timer count or the first Tx packet threshold equals the first Tx packet timer count.
15:0	TX_LAST_ PKT_THRESH	Tx last packet threshold This register is in µs up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The Tx last packet timer starts counting after any Tx completion. If the timer is still counting when the next Tx completion occurs, it resets and starts over. The last Tx packet timer expires when either the last Tx packet threshold equals the last Tx packet timer count or the first Tx packet threshold equals the first Tx packet timer count.

10.15.8 Rx Interrupt Mitigation Thresholds (RIMT)

Offset: 0x1810002C
Access: Read/Write
Reset: Undefined

This register is in ms up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The Rx last packet timer starts counting after any receive completion. If the timer is still counting when the next receive completion occurs, it resets and starts over. The last receive packet timer expires when either the last receive packet threshold equals the last receive packet timer count or the first receive packet threshold equals the first receive packet timer count.

Bit	Bit Name	Description
31:16	RX_FIRST_PKT_THRESH	Receive first packet threshold
15:0	RX_LAST_PKT_THRESH	Receive last packet threshold

10.15.9 Tx Configuration (TXCFG)

Offset: 0x18100030
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31:18	RES	0x0	Reserved	
17	DIS_RETRY _UNDERRUN	0x1	Disable retry of underrun packets	
			0	Underrun packets will retry indefinitely
			1	Underrun packets will quit after first underrun attempt and write status indicating underrun
16:15	RES	0x0	Reserved	
14	RTCI_DIS	0x0	ReadyTime/CBR disable for QCUs 8-9. When the MAC is running at a clock rate ≤ 32 MHz, this bit must be set and only the ASAP frame scheduling policy may be selected for QCUs 8-9. QCUs 0-7 may continue to use any frame scheduling policy. Since in normal operation the MAC clock rate is at least 40 MHz, this is meant as a debugging mode only. Resets to 0x0.	
			0	MAC clock rate at least 33 MHz; enable all frame scheduling policies for all QCUs.
			1	MAC clock rate is ≤ 32 MHz. Disable non-ASAP FSP for QCUs 8-9 so that CBR and ReadyTime logic will continue to operate correctly for QCUs 0-7.
13	RES	0x0	Reserved	
12	ATIM_DEFER_DIS	0x0	Fragment burst vs. ATIM window defer disable. Note: PCU does not currently support ATIM	
			0	In ad hoc mode only, if the ATIM window starts in the middle of a fragment burst, halt the burst and allow frames from other DCUs (e.g., DCUs generating beacon and CAB traffic) to proceed. Resume fragment burst after the ATIM window ends and after following normal DCF channel access procedures.
			1	Pause the fragment burst for the duration of the ATIM window, but do not allow frames from other DCUs to appear on the air; meant for debugging mode or if a problem is suspected with the fragment burst deferral logic.
11	BCN_PAST_ATIM_DIS	0x0	Ad hoc beacon ATIM window transmission policy. Note: PCU does not currently support ATIM.	
			0	If the ATIM window ends before the station can send its beacon, the station cancels its beacon transmission.
			1	The station continues to attempt to send its beacon until it is able to do so, regardless of the status of the ATIM window.
10	RES	0x0	Reserved	
9:4	TXCFG_TRIGLVL	0x1	Frame trigger level; Specifies the minimum number (in units of 64 bytes) to DMA into the PCU TXFIFO before the PCU initiates sending the frame on the air. Resets to 0x1 (meaning 64 Bytes or a full frame, whichever occurs first).	
3	RES	0x0	Reserved	
2:0	TXCFG_DMA_SIZE	0x5	Maximum DMA request size for master reads	
			0	4 B
			1	8 B
			2	16 B
			3	32 B
			4	64 B
			5	128 B
			6	256 B
			7	Reserved

10.15.10 Rx Configuration (RXCFG)

Offset: 0x18100034
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:8	RES	0x0	Reserved
7	SLEEP_RX_ PEND_EN	0x0	Sleep entry policy when frames are pending in the PCU RX FIFO.
		0	The DMA receive logic requires all frames to be drained from the PCU RX FIFO before allowing the chip to sleep (the desired and default setting)
		1	The DMA receive logic will allow the chip to sleep even when frames are pending in the PCU Rx FIFO. This setting should not be needed in normal use and is meant primarily as a debugging mode or if a bug is suspected in the DMA tracking of the PCU RX FIFO frame count.
6	JUMBO_ WRAP_EN	0x0	Jumbo descriptor wrap mode.
		0	After reaching end of the jumbo descriptor's data buffer, go to next descriptor
		1	After reaching end of the jumbo descriptor's data buffer, retransfer into the same descriptor's data buffer again. This means the descriptor's data buffer will be overwritten with data from the PCU repeatedly in an infinite loop.
5	RES	0x0	Reserved
4:3	ZERO_LEN_ DMA_EN	0x0	Zero-length frame DMA enable
		0	Disable DMA of all zero-length frames. In this mode, the DMA logic suppresses all zero-length frames. Reception of zero-length frames is invisible to the host (they neither appear in host memory nor consume a Rx descriptor).
		1	Reserved
		2	Enable DMA of all zero-length frames. In this mode, all zero-length frames (chirps, double-chirps, and non-chirps) are DMAed into host memory just like normal (non-zero-length) frames.
		3	Reserved
2:0	DMA_SIZE	0x4	Maximum DMA size for master writes; (See the encodings for the register “Tx Configuration (TXCFG)” on page 292)

10.15.11 MIB Control (MIBC)

Offset: 0x18100040
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:4	RES	0x0	Reserved
3	STROBE	0x0	MIB counter strobe. This bit is a one-shot and always reads as zero. For writes:
		0	No effect
		1	Causes every MIB counter to increment by one
2	CLEAR	0x1	Clear all counters
1	FREEZE	0x1	Freeze all counters
0	RES	0x0	Reserved

10.15.12 Data Buffer Length (DATABUF)

Offset: 0x18100060
Access: Read/Write
Reset: 0xFFF

Bit	Name	Description
31:12	RES	Reserved
11:0	BUF_LEN	Data buffer length; specifies the maximum size of the frame (4 KBytes) that can be written to this buffer (in bytes). The first 48 bytes of the 4 KBytes are for Rx status, the rest are for payload.

10.15.13 Global Tx Timeout (GTT)

Offset: 0x18100064
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:16	LIMIT	Timeout limit (in TU: 1024 μs); on reset, this value is set to 25 TU.
15:0	COUNT	Timeout counter (in TU: 1024 μs). The current value of the timeout counter that is reset on every transmit. If no Tx frame is queued up and ready to transmit, the timeout counter stays at 0 or else the counter increments every 1024 μs. If the timeout counter is equal to or greater than the timeout limit, the global transmit timeout interrupt is set in the ISR. This mechanism can be used to detect whether a Tx frame is ready and is unable to be transmitted.

10.15.14 Global Tx Timeout Mode (GTTM)

Offset: 0x18100068
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:5	RES	Reserved
4	DISABLE_QCU_FR_ ACTIVE_GTT	Before the GTT logic was using the PCI_TX_QCU_STATUS signal for GTT. It didn't seem to cover all the cases such as retry. If this bit is set then the original functionality will be enabled. If this bit is clear then QCU_FR_ACTIVE is used instead.
3	CST_USEC_STROBE	CST μs strobe; if this bit is set, then the CST timer will not use the TU based strobe but rather use the μs strobe to increment the timeout counter.
2	RESET_ON_CHAN_IDLE	Reset count on chan idle low. Reset count every time channel idle is low.
1	IGNORE_CHAN_IDLE	Ignore channel idle; if this bit is set then the GTT timer does not increment if the channel idle indicates the air is busy or NAV is still counting down.
0	USEC_STROBE	μs strobe; if this bit is set then the GTT timer will not use the TU based strobe but rather use a μs strobe to increment the timeout counter.

10.15.15 Carrier Sense Timeout (CST)

Offset: 0x1810006C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:16	LIMIT	Timeout limit (in TU: 1024 µs). On reset, this value is set to 0 TU.
15:0	COUNT	Timeout counter (in TU: 1024 µs). The current value of the timeout counter that is reset on every transmit. If no Tx frame is queued up and ready to transmit, the timeout counter stays at 0 or the counter increments every 1024 µs. If the timeout counter is equal to or greater than the timeout limit then carrier sense timeout (CST) interrupt is set in the ISR. This counter starts counting if any queues are ready for Tx. It continues counting when RX_CLEAR is low, which is useful to determine whether the transmit is stuck because RX_CLEAR is low for a long time.

10.15.16 Size of High and Low Priority (RXDP_SIZE)

Offset: 0x18100070
Access: Read-Only
Reset: 0x0Indicates the size of high and low priority RXDP FIFOs.

Bit	Bit Name	Description
31:12	RES	Reserved
12:8	HP	Indicates the size of high priority RXDP FIFO
7:0	LP	Indicates the size of low priority RXDP FIFO

10.15.17 MAC Rx High Priority Queue RXDP Pointer (RX_QUEUE_HP_RXDP)

Offset: 0x18100074
Access: Read/Write
Reset: 0x0

Lower 32 bits of the MAC Rx high priority queue RXDP pointer.

Bit	Bit Name	Description
31:0	ADDR	MAC Rx high priority queue RXDP pointer

10.15.18 MAC Rx Low Priority Queue RXDP Pointer (RX_QUEUE_LP_RXDP)

Offset: 0x18100078
Access: Read/Write
Reset: 0x0

Lower 32 bits of MAC Rx Low Priority Queue RXDP pointer.

Bit	Bit Name	Description
31:0	ADDR	MAC Rx low priority queue RXDP pointer for the lower 32 bits

10.15.19 Primary Interrupt Status (ISR_P)

Offset: 0x18100080
Access: Read/Write-One-to-Clear
Reset: 0x0

NOTE

- The bits that are logical ORs of bits in the secondary ISRs are generated by logically ORing the secondary ISR bits after the secondary ISR bits have been masked with the appropriate bits from the corresponding secondary interrupt mask register.
- A write of one to a bit that is a logical OR of bits in a secondary ISR clears the secondary ISR bits from which the primary ISR bit is generated. E.g.: A write of a one to TXOK (bit [6]) in ISR_P clears all 10 TXOK bits in ISR_S0 (bits [9:0] of Secondary Interrupt Status 0 (ISR_S0), page 10-297).
- Only the bits in this register (ISR_P) and the primary interrupt mask register (Primary Interrupt Mask (IMR_P), page 10-301) control whether the MAC's interrupt output is asserted. The bits in the several secondary interrupt status/mask registers control what bits are set in the primary interrupt status register; however, the IMR_S* registers do not determine whether an interrupt is asserted. That is, an interrupt is asserted only when the logical AND of ISR_P and IMR_P is non-zero. The secondary interrupt mask/status registers affect which bits are set in ISR_P, but do not directly affect whether an interrupt is asserted.

Bit	Bit Name	Description
31	RXINTM	Rx completion interrupt after mitigation; either the first Rx packet or last Rx packet interrupt mitigation count has reached its threshold (see the register "Rx Interrupt Mitigation Thresholds (RIMT)" on page 291)
30	TXINTM	Tx completion interrupt after mitigation; either the first Tx packet or last Tx packet interrupt mitigation count has reached its threshold (see the register "Tx Interrupt Mitigation Thresholds (TIMT)" on page 291)
29	RES	Reserved
28	GENTMR	Logical OR of all GENERIC TIMER bits in the secondary ISR 5 which include the GENERIC_TIMER_TRIGGER[7:0], GENERIC_TIMER_THRESH[7:0], GENERIC_TIMER_OVERFLOW
27	QTRIG	Logical OR of all QTRIG bits in secondary ISR 4; indicates that at least one QCU's frame scheduling trigger event has occurred
26	QCBRURN	Logical OR of all QCBRURN bits in secondary ISR 3; indicates that at least one QCU's frame scheduling trigger event occurred when no frames were present on the queue
25	QCBROVF	Logical OR of all QCBROVF bits in secondary ISR 3; indicates that at least one QCU's CBR expired counter has reached the value of the QCU's CBR_OVR_THRESH parameter (see CBR Configuration (Q_CBRCFG), page 10-309 register bits [31:24])
24	RXMINTR	RXMINTR maximum receive interrupt rate; same as RXINTM with the added requirement that maximum interrupt rate count has reached its threshold; this interrupt alternates with TXMINTR.
23	BCNMISC	Miscellaneous beacon-related interrupts This bit is the Logical OR of the CST, GTT, TIM, CABEND, DTIMSYNC, BCNTO, CABTO, TSFOOR, DTIM, and TBTT_TIME bits in secondary ISR 2.
22:21	RES	Reserved
20	BNR	Beacon not ready Indicates that the QCU marked as being used for beacons received a DMA beacon alert when the queue contained no frames.
19	TXMINTR	TXMINTR maximum Tx interrupt rate

Bit	Bit Name	Description
18	BMISS	The PCU indicates that is has not received a beacon during the previous *N* (*N* is programmable) beacon periods
17	BRSSI	The PCU indicates that the RSSI of a beacon it has received has fallen below a programmable threshold
16	SWBA	The PCU has signalled a software beacon alert
15	RXKCM	Key cache miss; a frame was received with a set key cache miss Rx status bit
14	RXPHY	The PHY signalled an error on a received frame
13	SWI	Software interrupt signalled; see the register “Command (CR)” on page 289
12	MIB	One of the MIB regs has reached its threshold
11	TXURN	Logical OR of all TXURN bits in secondary ISR 2. Indicates that the PCU reported a txfifo underrun for at least one QCU’s frame
10	TXEOL	Logical OR of all TXEOL bits in secondary ISR 1; indicates that at least one Tx desc fetch state machine has no more Tx descs available
9	RES	Reserved
8	TXERR	Logical OR of all TXERR bits in secondary ISR 1; indicates that at least one frame was completed with an error, regardless of whether the InterReq bit was set
7	RES	Reserved
6	TXOK	Logical OR of all TXOK bits in secondary ISR 0; indicates that at least one frame was completed with no errors and at the requested rate, regardless of whether the InterReq bit was set.
5	RXORN	RxFIFO overrrun
4	RXEOL	Rx descriptor fetch logic has no more Rx descs available
3	RXNOFR	No frame was received for RXNOFR timeout clocks
2	RXERR	The frame was received with errors
1	RXOK_LP	Low priority frame was received with no errors
0	RXOK_HP	High priority frame was received with no errors

10.15.20 Secondary Interrupt Status 0 (ISR_S0)

Offset: 0x18100084
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	TXOK[9]	TXOK for QCU 9
...	...	...
1	TXOK[1]	TXOK for QCU 1
0	TXOK[0]	TXOK for QCU 0

10.15.21 Secondary Interrupt Status 1 (ISR_S1)

Offset: 0x18100088
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25	TXEOL[9]	TXEOL for QCU 9
...	...	...
17	TXEOL]1]	TXEOL for QCU 1
16	TXEOL[0]	TXEOL for QCU 0
15:10	RES	Reserved
9	TXERR[9]	TXERR for QCU 9
...	...	...
1	TXERR[1]	TXERR for QCU 1
0	TXERR[0]	TXERR for QCU 0

10.15.22 Secondary Interrupt Status 2 (ISR_S2)

Offset: 0x1810008C
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31	TBTT_TIME	TBTT-referenced timer interrupt; indicates the PCU's TBTT-referenced timer has elapsed.
30	TSFOOR	TSF out of range; indicates that the corrected TSF received from a beacon differs from the PCU's internal TSF by more than a (programmable) threshold
29	DTIM	A beacon was received with the DTIM bit set and a DTIM count value of zero. Beacons with a set DTIM bit but a non-zero DTIM count do not generate it.
28	CABTO	CAB timeout; a beacon was received that indicated that the STA should expect to receive CAB traffic. However, the PCU's CAB timeout expired either because the STA received no CAB traffic, or because the STA received some CAB traffic but never received a CAB frame with the more data bit clear in the frame control field (which would indicate the final CAB frame).
27	BCNTO	Beacon timeout; a TBTT occurred and the STA began waiting to receive a beacon, but no beacon was received before the PCU's beacon timeout expired
26	DTIMSYNC	DTIM synchronization lost; a beacon was received that was expected to be a DTIM but was not, or a beacon was received that was not expected to be a DTIM but was
25	CABEND	End of CAB traffic; a CAB frame was received with the more data bit clear in the frame control field
24	TIM	A beacon was received with the local STA's bit set in the TIM element
23	GTT	Global Tx timeout; indicates the GTT count ≥ than the GTT limit
22	CST	Carrier sense timeout; indicates the CST count ≥ than the CST limit
21:10	RES	Reserved
9	TXURN[9]	TXURN for QCU 9
...	...	...
1	TXURN[1]	TXURN for QCU 1
0	TXURN[0]	TXURN for QCU 0

10.15.23 Secondary Interrupt Status 3 (ISR_S3)

Offset: 0x18100090
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25	QCBRURN[9]	QCBRURN for QCU 9
...	...	...
17	QCBRURN[1]	QCBRURN for QCU 1
16	QCBRURN[0]	QCBRURN for QCU 0
15:10	RES	Reserved
9	QCBROVF[9]	QCBROVF for QCU 9
1	QCBROVF[1]	QCBROVF for QCU 1
...	...	...
0	QCBROVF[0]	QCBROVF for QCU 0

10.15.24 Secondary Interrupt Status 4 (ISR_S4)

Offset: 0x18100094
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	QTRIG[9]	QTRIG for QCU 9
...	...	...
1	QTRIG[1]	QTRIG for QCU 1
0	QTRIG[0]	QTRIG for QCU 0

10.15.25 Secondary Interrupt Status 5 (ISR_S5)

Offset: 0x18100098
Access: Read/Write-One-to-Clear
Reset: 0x0

NOTE The trigger indicates that the TSF matched or exceeded the timer. The threshold is set when the TSF exceeds the timer by the GENERIC_TIMER_THRESH value. The GENERIC_TIMER overflow occurs when the TSF exceeds the timer by such a large amount that TSF ≥ Timer + Period, indicating incorrect software programming. The GENERIC_TIMER 0 threshold was removed because timer 0 is special and does not generate threshold event.

Bit	Bit Name	Description
31	GENERIC_TIMER[15]	GENERIC_TIMER 15 threshold
...	...	...
17	GENERIC_TIMER[11]	GENERIC_TIMER 1 threshold
16	GENERIC_TIMER_OVERFLOW	GENERIC_TIMER overflow
15	GENERIC_TIMER_TRIGGER[15]	GENERIC_TIMER 15 trigger
...	...	...
1	GENERIC_TIMER_TRIGGER[1]	GENERIC_TIMER 1 trigger
0	GENERIC_TIMER_TRIGGER[0]	GENERIC_TIMER 0 trigger

10.15.26 Primary Interrupt Mask (IMR_P)

Offset: 0x181000A0
Access: Read/Write
Reset: 0x0

NOTE Only the bits in this register control whether the MAC's interrupt outputs are asserted. The bits in the secondary interrupt mask registers control what bits are set in the Primary Interrupt Mask (IMR_P), page 10-301 register; however, the IMR_S* registers do not determine whether an interrupt is asserted.

Bit	Bit Name	Description
31	RXINTM	RXINTM interrupt enable
30	TXINTM	TXINTM interrupt enable
29	RES	Reserved
28	GENTMR	GENTMR interrupt enable
27	QTRIG	QTRIG interrupt enable
26	QCBRURN	QCBRURN interrupt enable
25	QCBROVF	QCBROVF interrupt enable
24	RXMINTR	RXMINTR interrupt enable
23	BCNMISC	BCNMISC interrupt enable
22:21	RES	Reserved
20	BNR	BNR interrupt enable
19	TXMINTR	TXMINTR interrupt enable
18	BMISS	BMISS interrupt enable
17	BRSSI	BRSSI interrupt enable
16	SWBA	SWBA interrupt enable
15	RXKCM	RXKCM interrupt enable
14	RXPHY	RXPHY interrupt enable
13	SWI	SWI interrupt enable
12	MIB	MIB interrupt enable
11	TXURN	TXURN interrupt enable
10	TXEOL	TXEOL interrupt enable
9	TXNOFR	TXNOFR interrupt enable
8	TXERR	TXERR interrupt enable
7	RES	Reserved
6	TXOK	TXOK interrupt enable
5	RXORN	RXORN interrupt enable
4	RXEOL	RXEOL interrupt enable
3	RXNOFR	RXNOFR interrupt enable
2	RXERR	RXERR interrupt enable
1	RXOK_LP	RXOK_LP interrupt enable
0	RXOK_HP	RXOK_HP interrupt enable

10.15.27 Secondary Interrupt Mask 0 (IMR_S0)

Offset: 0x181000A4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	TXOK[9]	TXOK for QCU 9 interrupt enable
...	...	...
1	TXOK[1]	TXOK for QCU 1 interrupt enable
0	TXOK[0]	TXOK for QCU 0 interrupt enable

10.15.28 Secondary Interrupt Mask 1 (IMR_S1)

Offset: 0x181000A8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25	TXEOL[9]	TXEOL for QCU 9 interrupt enable
...	...	...
17	TXEOL[1]	TXEOL for QCU 1 interrupt enable
16	TXEOL[0]	TXEOL for QCU 0 interrupt enable
15:10	RES	Reserved
9	TXERR[9]	TXERR for QCU 9 interrupt enable
...	...	...
1	TXERR[1]	TXERR for QCU 1 interrupt enable
0	TXERR[0]	TXERR for QCU 0 interrupt enable

10.15.29 Secondary Interrupt Mask 2 (IMR_S2)

Offset: 0x181000AC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31	TBTT_TIME	TBTT_TIME interrupt enable
30	TSFOOR	TSFOOR interrupt enable
29	DTIM	DTIM interrupt enable
28	CABTO	CABTO interrupt enable
27	BCNTO	BCNTO interrupt enable
26	DTIMSYNC	DTIMSYNC interrupt enable
25	CABEND	CABEND interrupt enable
24	TIM	TIM interrupt enable
23	GTT	GTT interrupt enable
22	CST	CST interrupt enable
21:10	RES	Reserved
9	TXURN[9]	TXURN for QCU 9 interrupt enable
...	...	...
1	TXURN[1]	TXURN for QCU 1 interrupt enable
0	TXURN[0]	TXURN for QCU 0 interrupt enable

10.15.30 Secondary Interrupt Mask 3 (IMR_S3)

Offset: 0x181000B0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25	QCBRURN[9]	QCBRURN for QCU 9 interrupt enable
...	...	...
17	QCBRURN[1]	QCBRURN for QCU 1 interrupt enable
16	QCBRURN[0]	QCBRURN for QCU 0 interrupt enable
15:10	RES	Reserved
9	QCBROVF[9]	QCBROVF for QCU 9 interrupt enable
...	...	...
1	QCBROVF[1]	QCBROVF for QCU 1 interrupt enable
0	QCBROVF[0]	QCBROVF for QCU 0 interrupt enable

10.15.31 Secondary Interrupt Mask 4 (IMR_S4)

Offset: 0x181000B4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	QTRIG[9]	QTRIG for QCU 9 interrupt enable
...	...	...
1	QTRIG[1]	QTRIG for QCU 1 interrupt enable
0	QTRIG[0]	QTRIG for QCU 0 interrupt enable

10.15.32 Secondary Interrupt Mask 5 (IMR_S5)

Offset: 0x181000B8
Access: Read/Write-One-to-Clear
Reset: 0x0

NOTE The trigger indicates the TSF matched or exceeded the timer; threshold is set when the TSF exceeds the timer by the GENERIC_TIMER_THRESH value. The GENERIC_TIMER overflow occurs when the TSF exceeds the timer by such a large amount that TSF ≥ Timer + Period, indicating incorrect software programming. The threshold GENERIC_TIMER 0 was removed because timer 0 is special and does not generate a threshold event.

Bit	Bit Name	Description
31	GENERIC_TIMER_THRESHOLD[15]	GENERIC_TIMER_THRESHOLD 15
30	GENERIC_TIMER_THRESHOLD[14]	GENERIC_TIMER_THRESHOLD 14
...	...	...
18	GENERIC_TIMER_THRESHOLD[2]	GENERIC_TIMER_THRESHOLD 2
17	GENERIC_TIMER_THRESHOLD[1]	GENERIC_TIMER_THRESHOLD 1
16	GENERIC_TIMER_OVERFLOW	GENERIC_TIMER overflow enable
15	GENERIC_TIMER_TRIGGER[15]	GENERIC_TIMER 15 trigger enable
...	...	...
1	GENERIC_TIMER_TRIGGER[1]	GENERIC_TIMER 1 trigger enable
0	GENERIC_TIMER_TRIGGER[0]	GENERIC_TIMER 0 trigger enable

10.15.33 Primary Interrupt Status Read and Clear (ISR_P_RAC)

Offset: 0x181000C0
Access: Read-and-Clear (No Write Access)
Reset: 0x0

NOTE A read from this location atomically:

- Copies all secondary ISRs into the corresponding secondary ISR shadow registers (ISR_S0 is copied to ISR_S0_S, etc.)
- Clears all bits of the primary ISR (ISR_P) and all bits of all secondary ISRs (ISR_S0–ISR_S4)
- Returns the contents of the primary ISR (ISR_P)

Bit	Bit Name	Description
31:0	ISR_P	Same format as Primary Interrupt Status (ISR_P)

10.15.34 Secondary Interrupt Status 0 (ISR_S0_S)

Offset: 0x181000C4
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 0 (ISR_S0)

10.15.35 Secondary Interrupt Status 1 (ISR_S1_S)

Offset: 0x181000C8
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 1 (ISR_S1)

10.15.36 Secondary Interrupt Status 2 (ISR_S2_S)

Offset: 0x181000D0
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 2 (ISR_S2)

10.15.37 Secondary Interrupt Status 3 (ISR_S3_S)

Offset: 0x181000D4
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 3 (ISR_S3)

10.15.38 Secondary Interrupt Status 4 (ISR_S4_S)

Offset: 0x181000D8
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 4 (ISR_S4)

10.15.39 Secondary Interrupt Status 5 (ISR_S5_S)

Offset: 0x181000DC
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 5 (ISR_S5)

10.16 WQCU Registers

The WQCU registers occupy the offset range 0x18100800-0x18100A40 in the QCA9558 address space. The QCA9558 has ten QCUs, numbered from 0 to 9.

Table 10-17 WQCU Registers

Offset	Name	Description	Page
0x18100800 + (*Q* << 2)[1]	Q_TXDP	Tx Queue Descriptor Pointer	page 307
0x18100830	Q_STATUS_RING_START	QCU_STATUS_RING_START_ ADDRESS Lower 32 bits of Address	page 308
0x18100834	Q_STATUS_RING_END	QCU_STATUS_RING_END_ADDR Lower 32 Bits of Address	page 308
0x18100838	Q_STATUS_RING_CURRENT	QCU_STATUS_RING_CURRENT Address	page 308
0x18100840	Q_TXE	Tx Queue Enable	page 308
0x18100880	Q_TXD	Tx Queue Disable	page 309
0x181008C0 + (*Q* << 2)[1]	Q_CBRCFG	CBR Configuration	page 309
0x18100900 + (*Q* << 2)[1]	Q_RDYTIMECFG	ReadyTime Configuration	page 309
0x18100940	Q_ONESHOTARM_SC	OneShotArm Set Control	page 310
0x18100980	Q_ONESHOTARM_CC	OneShotArm Clear Control	page 310
0x181009C0 + (*Q* << 2)[1]	Q_MISC	Miscellaneous QCU Settings	page 311
0x18100A00 + (*Q* << 2)[1]	Q_STS	Miscellaneous QCU Status	page 312
0x18100A40	Q_RDYTIMESHDN	ReadyTimeShutdown Status	page 313
0x18100A44	Q_MAC_QCU_DESC_CRC_ CHK	Descriptor CRC Check	page 313

1. The variable Q in the register addresses refers to the QCU number.

10.16.1 Tx Queue Descriptor (Q_TXDP)

Offset: 0x18100800 + (*Q* < 2)
Access: Read/Write
Cold Reset: Undefined
Warm Reset: Unaffected

Bit	Bit Name	Description
31:2	TXDP	Tx descriptor pointer
1:0	RES	Reserved

10.16.2 QCU_STATUS_RING_START_ADDRESS Lower 32 bits of Address (Q_STATUS_RING_START)

Offset: 0x18100830
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	ADDR	Lower 32 bits of QCU_STATUS_RING_START_ADDR

10.16.3 QCU_STATUS_RING_END_ADDR Lower 32 Bits of Address (Q_STATUS_RING_END)

Offset: 0x18100834
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	ADDR	Lower 32 bits of QCU_STATUS_RING_END_ADDR

10.16.4 QCU_STATUS_RING_CURRENT Address (Q_STATUS_RING_CURRENT)

Offset: 0x18100838
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	ADDR	MAC_QCU_STATUS_RING_CURRENT_ADDRESS

10.16.5 Tx Queue Enable (Q_TXE)

Offset: 0x18100840
Access: Read/Write
Reset: 0x0

NOTE Writing a 1 in bit position *N* sets the TXE bit for QCU *N*. Writing a 0 in bit position *N* has no effect; in particular, it does not clear the TXE bit for the QCU.

Bit	Bit Name	Description
31:10	RES	Reserved
9	QCU_EN[9]	Enable QCU 9
...	...	...
1	QCU_EN[1]	Enable QCU 1
0	QCU_EN[0]	Enable QCU 0

10.16.6 Tx Queue Disable (Q_TXD)

Offset: 0x18100880
Access: Read/Write
Reset: 0x0

NOTE To stop transmission for QCU *Q*:

1. Write a 1 to QCU Q's TXD bit
2. Poll the Tx Queue Enable (Q_TXE), page 10-308 register until QCU *Q*'s TXE bit is clear
3. Poll QCU *Q*'s Misc. QCU Status (Q_STS), page 10-312 register until its pending frame count (Q_STS bits [1:0]) is zero
4. Write a 0 to QCU *Q*'s TXD bit

NOTE At this point, QCU *Q* has shut down and has no frames pending in its associated DCU.

NOTE Software must not write a 1 to a QCU's TXE bit when that QCU's TXD bit is set; an undefined operation will result. Software must ensure that it sets a QCU's TXE bit only when the QCU's TXD bit is clear. It is fine to write a 0 to TXE when TXD is set, but this has no effect on the QCU.

Bit	Bit Name	Description
31:10	RES	Reserved
9	QCU_DIS[9]	Disable QCU 9
...	...	...
1	QCU_DIS[1]	Disable QCU 1
0	QCU_DIS[0]	Disable QCU 0

10.16.7 CBR Configuration (Q_CBRCFG)

Offset: 0x181008C0 + (*Q* < 2)
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:24	CBR_OVF_THRESH	CBR overflow threshold
23:0	CBR_INTV	CBR interval in µs

10.16.8 ReadyTime Configuration (Q_RDYTIMECFG)

Offset: 0x18100900 + (*Q* < 2)
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:25	RES	Reserved	
24	RDYTIME_EN	ReadyTime enable	
		0	Disable ReadyTime use
		1	Enable ReadyTime use
23:0	RDYTIME_DUR	ReadyTime duration in µs	

10.16.9 OneShotArm Set Control (Q_ONESHOTARM_SC)

Offset: 0x18100940
Access: Read/Write
Reset: 0x0

NOTE A read to this register returns the current state of all OneShotArm bits (QCU *Q*'s OneShotArm bit is returned in bit position *Q*).

Bit	Bit Name	Description	
31:10	RES	Reserved	
9	ONESHOTARM[9]	0	No effect
		1	Set OneShot arm bit for QCU 9
...	...	...	
1	ONESHOTARM[1]	0	No effect
		1	Set OneShot arm bit for QCU 1
0	ONESHOTARM[0]	0	No effect
		1	Set OneShot arm bit for QCU 0

10.16.10 OneShotArm Clear Control (Q_ONESHOTARM_CC)

Offset: 0x18100980
Access: Read/Write
Reset: 0x0

NOTE A read to this register returns the current state of all OneShotArm bits (QCU *Q*'s OneShotArm bit is returned in bit position *Q*).

Bit	Bit Name	Description	
31:10	RES	Reserved	
9	ONESHOT_CLEAR[9]	0	No effect
		1	Clear OneShot arm bit for QCU 9
...	...	...	
1	ONESHOT_CLEAR[1]	0	No effect
		1	Clear OneShot arm bit for QCU 1
0	ONESHOT_CLEAR[0]	0	No effect
		1	Clear OneShot arm bit for QCU 0

10.16.11 Misc. QCU Settings (Q_MISC)

Offset: 0x181009C0 + (Q < 2)
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31:12	RES	0x0	Reserved	
11	QCU_FR_ABORT_REQ_EN	0x1	DCU frame early termination request control	
			0	Never request early frame termination. Once a frame enters the DCU, it will remain active until its normal retry count has been reached or the frame succeeds.
			1	Allow this QCU to request early frame termination. When requested, the DCU attempts to complete processing the frame more quickly than it normally would.
10	CBR_EXP_CNT_CLR_EN	0x0	CBR expired counter force-clear control. Write-only (always reads as zero). Write of:	
			0	No effect
			1	Resets the CBR expired counter to zero
9	TXE_CLR_ON_CBR_END	0x0	ReadyTime expiration and VEOL handling policy	
			0	On expiration of ReadyTime or on VEOL, the TXE bit is not cleared. Only reaching the physical end-of-queue (that is, a NULL LinkPtr) will clear TXE
			1	The TXE bit is cleared on expiration of ReadyTime, on VEOL, and on reaching the physical end-of-queue
8	CBR_EXP_INC_LIMIT	0x0	CBR expired counter limit enable	
			0	The maximum CBR expired counter value is 255, but a CBROVF interrupt is generated when the counter reaches the value set in the CBR overflow threshold field of the CBR Configuration (Q_CBRCFG) register.
			1	The maximum CBR expired counter is limited to the value of the CBR overflow threshold field of the CBR Configuration (Q_CBRCFG) register. Note that in addition to limiting the maximum CBR expired counter to this value, a CBROVF interrupt is also generated when the CBR expired counter reaches the CBR overflow threshold.
7	QCU_IS_BCN	0x0	Beacon use indication. Indicates whether the QCU is being used for beacons	
			0	QCU is being used for non-beacon frames only
			1	QCU is being used for beacon frames (and possibly for non-beacon frames)
6	CBR_EXP_INC_DIS_NOBCNFR	0x0	Disable the CBR expired counter increment if the frame scheduling trigger occurs and the QCU marked as being used for beacon transmission (i.e., the QCU that has bit [7] set in its Misc. QCU Settings (Q_MISC) register) contains no frames	
			0	Increment the CBR expired counter each time the frame scheduling trigger occurs, regardless of whether the beacon queue contains frames
			1	Increment the CBR expired counter only when both the frame scheduling trigger occurs and the beacon queue is valid (the beacon queue is valid whenever its TXE is asserted)
5	CBR_EXP_INC_DIS_NOFR	0x0	Disable the CBR expired counter increment if the frame scheduling trigger occurs and the queue contains no frames	
			0	Increment the CBR expired counter each time the frame scheduling trigger occurs, regardless of whether the queue contains frames
			1	Increment the CBR expired counter only when both the frame scheduling trigger occurs and the queue is valid (the queue is valid whenever TXE is asserted)
4	ONESHOT_EN	0x0	OneShot enable	
			0	Disable OneShot function
			1	Enable OneShot function - Note that OneShot must not be enabled when the QCU is set to an ASAP frame scheduling policy.

Bit	Bit Name	Reset	Description	
3:0	FSP	0x0	Frame scheduling policy setting	
			0	ASAP- The QCU is enabled continuously.
			1	CBR - The QCU is enabled under control of the settings in the CBR Configuration (Q_CBRCFG) register.
			2	DBA-gated; the QCU is enabled at each occurrence of a DMA beacon alert.
			3	TIM-gated - The QCU will be enabled whenever: ■ In STA mode, the PCU indicates that a beacon frame has been received with the local STA's bit set in the TIM element ■ In IBSS mode, the PCU indicates that an ATIM frame has been received
			4	Beacon-sent-gated - The QCU will be enabled when the DCU that is marked as being used for beacon transmission (see bit [16] of the QCU Tx Filter DCU0 127-96 (D_TXFILTER_DCU0_127_96) register) indicates that it has sent the beacon frame on the air
			5	Beacon-received-gated - The QCU will be enabled when the PCU indicates that it has received a beacon.
			6	HCF Poll gated - The QCU will be enabled whenever the Rx HCF poll event occurs; the signals come from the PCU when a directed HCF poll frame type is received with valid FCS.
			15:7	Reserved

10.16.12 Misc. QCU Status (Q_STS)

Offset: 0x18100A00 + ($Q < 2$)
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:16	RES	Reserved
15:8	CBR_EXP	Current value of the CBR expired counter
7:2	RES	Reserved
1:0	FC	Pending frame count; the number of frames this QCU has pending in its associated DCU.

10.16.13 ReadyTimeShutdown Status (Q_RDYTIMESHDN)

Offset: 0x18100A40
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:10	RES	Reserved	
9	READYTIME_SHUTDOWN[9]	ReadyTimeShutdown status for QCU 9	
...	...	...	
1	READYTIME_SHUTDOWN[1]	ReadyTimeShutdown status for QCU 1	
0	READYTIME_SHUTDOWN[0]	ReadyTimeShutdown status for QCU 0 On read, returns ReadyTimeShutdown indication. Write of:	
		0	No effect
		1	Set OneShot arm bit for QCU 0

10.16.14 Descriptor CRC Check (MAC_QCU_DESC_CRC_CHK)

Offset: 0x18100A44
Access: Read/Write
Reset: 0x1

Bit	Bit Name	Description	
31:1	RES	Reserved	
0	EN	QCU frame descriptor CRC check	
		0	Disable CRC check on the descriptor fetched from HOST
		1	Enable CRC check on the descriptor fetched from HOST

10.17 WDCU Registers

The WDCU registers occupy the offset range 0x18101000-0x181012F0 in the QCA9558 address space. The QCA9558 has ten DCUs, numbered from 0 to 9.

Table 10-18 WLAN DCU Registers

Offset	Name	Description	Page
0x18101000 + (*D* << 2)[1]	D_QCUMASK	QCU Mask	page 315
0x18101030	D_GBL_IFS_SIFS	DCU-Global SIFS	page 316
0x18101038	D_TXFILTER_DCU0_0_31	QCU Tx Filter DCU0 0-31	page 316
0x1810103C	D_TXFILTER_DCU8_0_31	QCU Tx Filter DCU8 0-31	page 316
0x18101040 + (*D* << 2)[1]	D_LCL_IFS	DCU-Specific IFS Settings	page 317
0x18101070	D_GBL_IFS_SLOT	DCU-Global IFS Settings: Slot Duration	page 317
0x18101078	D_TXFILTER_DCU0_63_32	QCU Tx Filter DCU0 63-32	page 317
0x1810107C	D_TXFILTER_DCU8_63_32	QCU Tx Filter DCU8 63-32	page 318
0x18101080 + (*D* << 2)[1]	D_RETRY_LIMIT	Retry Limits	page 318
0x181010B0	D_GBL_IFS_EIFS	DCU-Global IFS Settings: EIFS Duration	page 318
0x181010B8	D_TXFILTER_DCU0_95_64	QCU Tx Filter DCU0 95-64	page 318
0x181010B	D_TXFILTER_DCU8_95_64	QCU Tx Filter DCU8 95-64	page 319
0x181010C0 + (*D* << 2)[1]	D_CHNTIME	ChannelTime Settings	page 319
0x181010F0	D_GBL_IFS_MISC	QCU Global IFS Miscellaneous	page 319
0x181010F8	D_TXFILTER_DCU0_127_96	QCU Tx Filter DCU0 127-96	page 320
0x181010FC	D_TXFILTER_DCU8_127_96	QCU Tx Filter DCU8 127-96	page 321
0x18101100 + (*D* << 2)[1]	D_MISC	Miscellaneous DCU-Specific Settings	page 321
0x18101138	D_TXFILTER_DCU1_31_0	QCU Tx Filter DCU1 31-0	page 323
0x1810113C	D_TXFILTER_DCU9_31_0	QCU Tx Filter DCU9 31-0	page 324
0x18101140	D_SEQ	DCU Sequence	page 324
0x18101178	D_TXFILTER_DCU1_63_32	QCU Tx Filter DCU1 63-32	page 324
0x1810117C	D_TXFILTER_DCU9_63_32	QCU Tx Filter DCU9 63-32	page 324
0x181011B8	D_TXFILTER_DCU1_95_64	QCU Tx Filter DCU1 95-64	page 325
0x181011BC	D_TXFILTER_DCU9_95_64	QCU Tx Filter DCU9 95-64	page 325
0x181011F8	D_TXFILTER_DCU1_127_96	QCU Tx Filter DCU1 127-96	page 325
0x181011FC	D_TXFILTER_DCU9_127_96	QCU Tx Filter DCU9 127-96	page 325
0x18101238	D_TXFILTER_DCU2_31_0	QCU Tx Filter DCU2 31-0	page 326
0x18101270	D_PAUSE	DCU Pause	page 326
0x18101278	D_TXFILTER_DCU2_63_32	QCU Tx Filter DCU2 63-32	page 326
0x181012B0	DCU_WOW_KEEP_ALIVE	DCU WOW Keep-Alive	page 327
0x181012B8	D_TXFILTER_DCU2_95_64	QCU Tx Filter DCU2 95-64	page 327
0x181012F0	D_TXSLOTMASK	DCU Transmission Slot Mask	page 328
0x181012F8	D_TXFILTER_DCU2_127_96	QCU Tx Filter DCU2 127-96	page 328
0x18101338	D_TXFILTER_DCU3_31_0	QCU Tx Filter DCU3 31-0	page 329

Table 10-18 WLAN DCU Registers (cont.)

Offset	Name	Description	Page
0x18101378	D_TXFILTER_DCU3_63_32	QCU Tx Filter DCU3 63-32	page 329
0x181013B8	D_TXFILTER_DCU3_95_64	QCU Tx Filter DCU3 95-64	page 329
0x181013F8	D_TXFILTER_DCU3_127_96	QCU Tx Filter DCU3 127-96	page 329
0x18101438	D_TXFILTER_DCU4_31_0	QCU Tx Filter DCU4 31-0	page 330
0x1810143C	D_TXFILTER_CLEAR	QCU-DCU Tx Filter Clear	page 330
0x18101478	D_TXFILTER_DCU4_63_32	QCU Tx Filter DCU4 63-32	page 330
0x1810147C	D_TXFILTER_SET	QCU-DCU Tx Filter Set	page 330
0x18101478	D_TXFILTER_DCU4_95_64	QCU Tx Filter DCU4 95-64	page 331
0x181014F8	D_TXFILTER_DCU4_127-96	QCU Tx Filter DCU4 127-96	page 331
0x18101538	D_TXFILTER_DCU5_31_0	QCU Tx Filter DCU5 31-0	page 331
0x18101578	D_TXFILTER_DCU5_63_32	QCU Tx Filter DCU5 63-32	page 331
0x181015B8	D_TXFILTER_DCU5_95_64	QCU Tx Filter DCU5 95_64	page 332
0x181015F8	D_TXFILTER_DCU5_127_96	QCU Tx Filter DCU5 127-96	page 332
0x18101638	D_TXFILTER_DCU6_31_0	QCU Tx Filter DCU6 31-0	page 332
0x18101678	D_TXFILTER_DCU6_63_32	QCU Tx Filter DCU6 63-32	page 332
0x181016B8	D_TXFILTER_DCU6_95_64	QCU Tx Filter DCU6 95_64	page 333
0x181016F8	D_TXFILTER_DCU6_127_96	QCU Tx Filter DCU6 127-96	page 333
0x18101738	D_TXFILTER_DCU7_31_0	QCU Tx Filter DCU7 31-0	page 333
0x18101778	D_TXFILTER_DCU7_63_32	QCU Tx Filter DCU7 63-32	page 333
0x181017B8	D_TXFILTER_DCU7_95_64	QCU Tx Filter DCU7 95_64	page 334
0x181017F8	D_TXFILTER_DCU7_127_96	QCU Tx Filter DCU7 127-96	page 334
0x18101F00	SLEEP_STATUS	MAC Sleep Status	page 334
0x18101F04	LED_CONFIG	MAC LED Configuration	page 334

1. The variable *D* in the register addresses refers to the DCU number.

10.17.1 QCU Mask (D_QCUMASK)

Offset: 0x18101000 + (*D* < 2)
Access: Read/Write
Cold Reset: 0x0
Warm Reset: Unaffected

NOTE To achieve lowest power consumption, software should set this register to 0x0 for all DCUs that are not in use. The hardware detects that the QCU mask is set to zero and shuts down certain logic in response, helping to save power.

Bit	Bit Name	Description
31:10	RES	Reserved
9:0	QCU_MASK	Setting bit *Q* means that QCU *Q* is associated with (i.e., feeds into) this DCU. These register have reset values which corresponding to a 1 to 1 mapping between QCUs and DCUs. A register offset of 0x1000 maps to 0x1, 0x1004 maps to 0x2, 0x1008 maps to 0x4, etc.

10.17.2 DCU-Global SIFS (D_GBL_IFS_SIFS)

Offset: 0x18101030
Access: Read/Write
Reset: 0x640

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DURATION	SIFS duration in core clocks (40 MHz in non turbo mode, 80 MHz in turbo mode

10.17.3 QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31)

Offset: 0x18101038
Access: Read/Write
Reset: 0x0000

Each DCU has 128 transmit filter bits, for a total of 10*128=1280 transmit filter bits for all 10 DCUs. For reads of the transmit filter bits, the 1280 bits are accessed via reads within a range of 64 32-bit register locations.For writes of the transmit filter bits, only three of the 64 register locations are used. One location allows specific bits of a specific DCU transmit filter bits to be set or cleared. Two other locations allow all 128 transmit filter bits for any subset of the 10 DCUs to be set or cleared atomically. For both reads and writes, the PCI offset issued by the host is mapped to one of the 64 register locations. The 6-bit internal address that results from this mapping is called 'mmr_addr', and its value controls what portion of the transmit filter bits is affected by the host's register read or write. In general, the PCI offset that maps to the internal 'mmr_addr' is given by the equation: PCI offset = 0x1038 + ((mmr_addr & 0x1f) << 6) + ((mmr_addr & 0x20) >> 3).
Thus the proper PCI offset can be determined from the desired mmr_addr.

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCUO

10.17.4 QCU Tx Filter DCU8 0-31 (D_TXFILTER_DCU8_0_31)

Offset: 0x1810103C
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31), page 10-316.

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCUO

10.17.5 DCU-Specific IFS Settings (D_LCL_IFS)

Offset: 0x18101040 + ($D < 2$)
Access: Read/Write
Cold Reset: See field description
Warm Reset: Unaffected

Bit	Bit Name	Reset	Description
When Long AIFS is 0:			
31:28	RES	0x0	Reserved
27:20	DATA_AIFS_D[7:0]	0x2	AIFS value, in slots beyond SIFS; e.g., a setting of 2 (the reset value) means AIFS is equal to DIFS. **NOTE** This field is 17 bits wide (including the 9 MSBs accessed using the AIFS field), but the maximum supported AIFS value is 0x1FFFC. Setting AIFS to 0x1FFFD, 0x1FFFE, or 0x1FFFF causes the DCU to hang.
19:10	DATA_CW_MAX	0x3FF	CW_MAX value; must be equal to a power of 2, minus 1
9:0	DATA_CW_MIN	0xF	CW_MIN value; must be equal to a power of 2, minus 1
When Long AIFS is 1:			
31:29	RES	0x0	Reserved
28	LONG_AIFS [DCU_IDX_D]	0x0	Long AIFS bit; used to read or write to the nine MSBs of the AIFS value
27:9	RES	0x0	Reserved
8:0	DATA_AIFS_D[16:8]	0x2	Upper nine bits of the AIFS value (see bits [27:20] listed in this register)

10.17.6 QCU Global IFS Slots (D_GBL_IFS_SLOT)

Offset: 0x18101070
Access: Read/Write
Reset: 0x360

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DURATION	Slot duration in core clocks (40 MHz in non turbo mode, 80 MHz in turbo mode)

10.17.7 QCU Tx Filter DCU0 63-32 (D_TXFILTER_DCU0_63_32)

Offset: 0x18101078
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU0

10.17.8 QCU Tx Filter DCU8 63-32 (D_TXFILTER_DCU8_63_32)

Offset: 0x1810107C
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31), page 10-316.

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.9 Retry Limits (D_RETRY_LIMIT)

Offset: 0x18101080 + ($D < 2$)
Access: Read/Write
Cold Reset: See field description
Warm Reset: Unaffected

Bit	Bit Name	Reset	Description
31:20	RES	0x20	Reserved
19:14	SDFL	0x20	STA data failure limit: Specifies the number of times a frame's data exchange may fail before CW is reset to CW_MIN. Note: A value of 0x0 is unsupported.
13:8	SRFL	0x20	STA RTS failure limit: Specifies the number of times a frame's RTS exchange may fail before the CW is reset to CW_MIN. Note: A value of 0x0 is unsupported.
7:4	RES	0x0	Reserved
3:0	FRFL	0x4	Frame RTS failure limit: Specifies the number of times a frame's RTS exchange may fail before the current transmission series is terminated. A frame's RTS exchange fails if RTS is enabled for the frame, but when the MAC sends the RTS on the air, no CTS is received. Note: A value of 0x0 is unsupported.

10.17.10 QCU Global IFS EIFS (D_GBL_IFS_EIFS)

Offset: 0x18101070
Access: Read/Write
Reset: 0x3480

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DURATION	EIFS duration in core clocks (40 MHz in non turbo mode, 80 MHz in turbo mode)

10.17.11 QCU Tx Filter DCU0 95-64 (D_TXFILTER_DCU0_95_64)

Offset: 0x181010B8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCUO

10.17.12 QCU Tx Filter DCU8 95-64 (D_TXFILTER_DCU8_95_64)

Offset: 0x181010BC
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.13 ChannelTime Settings (D_CHNTIME)

Offset: 0x181010C0 + ($D < 2$)
Access: Read/Write
Cold Reset: 0x0
Warm Reset: Unaffected

Bit	Bit Name	Description
31:21	RES	Reserved
20	CHANNEL_TIME_EN	ChannelTime enable
19:0	DATA_CT_MMR	ChannelTime duration in µs

10.17.14 QCU Global IFS Miscellaneous (D_GBL_IFS_MISC)

Offset: 0x181010F0
Access: Read/Write
Reset: See field description

Determines which slice of the internal LFSR will be used to generate the random sequence used to determine backoff counts in the DCUs and scrambler seeds in the PCU. The intent is to have different stations have different LFSR slice values (perhaps by using some bits from the MAC address) to minimize the random sequence correlations among stations in the same BSS IBSS.

NOTE This field affects the MAC only when LFSR_SLICE_RANDOM_DIS (bit [24] of this register) is set. When random LFSR slice selection is enabled (default), it is ignored.

Bit	Bit Name	Reset	Description
31:30	RES	0x0	Reserved
29	SLOT_COUNT_ RST_UNCOND	0x0	Slot count reset policy. If set, slot count gets reset as soon as channel gets busy. If clear, slot count gets reset only after transmitting or receiving frame. Setting this bit will be helpful if performance is degraded by spur.
28	IGNORE_ BACKOFF	0x0	Ignore Back Off. Setting this bit will allow the DCU to ignore any backoff as well as EIFS. This should be set during fast channel change to guarantee low latency to flush the transmit pipe.

Bit	Bit Name	Reset	Description
27	CHAN_SLOT_ ALWAYS	0x0	Force transmission always on slot boundaries. When bits [26:25] of this register are non-zero, the MAC will transmit on slot boundaries when the 802.11 spec requires it to do so. When bits [26:25] are not equal to 0x0 and this bit is non-zero, then the MAC will attempt to transmit on slot boundaries all the time, not just when the spec requires. This mainly affects the case in which a frame becomes available when the channel has been idle for an AIFS. If this bit is clear in this case, then the MAC will transmit immediately. If this bit is set, then the MAC will wait for the next slot boundary before transmitting. Note that the setting of this bit has no effect unless bits [26:25] are non-zero.
26:25	CHAN_SLOT_ WIN_DUR	0x0	Slot transmission window length. Under certain corner cases (most related to very slow PCI DMA), the MAC could send a frame not on a slot boundary, thus deslotting the network. The value in this field specifies the number of core clocks after a slot boundary during which the MAC is permitted to send a frame. Specified in units of 8 core clocks; if set to 0x0 (the reset value), the MAC is permitted to send at any point in the slot.
24	LFSR_SLICE_ RANDOM_DIS	0x0	Random LFSR slice selection disable. 0 Allow the IFS logic to randomly generate the LFSR slice select value (see bits [2:0] of this register). The random selection method is meant to ensure independence of the LFSR output values both for nodes on different PCI busses but on the same network as well as for multiple nodes connected to the same physical PCI bus. 1 Disable random LFSR slice selection. Instead, the value programmed into LFSR_SLICE_SEL (bits [2:0] of this register) will be used.
23:10	RES	0x0	Reserved
9:4	SIFS_DUR_ USEC	0x10	SIFS duration in Microseconds
3	TURBO_MODE	0x0	Turbo mode indication. Software is required to keep this register consistent with the turbo non-turbo state of the overall system. In other words, this IS NOT a status bit generated by the MAC. Rather it is a control bit that must be maintained by software so that certain parts of the MAC that are sensitive to whether the system is in turbo mode will operate correctly. 0 Station is operating in non-turbo mode 1 Station is operating in turbo mode
2:0	LFSR_SLICE_ SEL	0x0	LFSR slice select. Determines which slice of the internal LFSR generates the random sequence used to determine backoff counts in the DCUs and scrambler seeds in the PCU. The intent is to have different stations have different LFSR slice values (perhaps by using some bits from the MAC address) to minimize the random sequence correlations among stations in the same BSS IBSS. **NOTE** This field affects the MAC only when LFSR_SLICE_RANDOM_DIS (bit [24] of this register) is set. When random LFSR slice selection is enabled (the default), this field is ignored.

10.17.15 QCU Tx Filter DCU0 127-96 (D_TXFILTER_DCU0_127_96)

Offset: 0x181010F8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCUO

10.17.16 QCU Tx Filter DCU8 127-96 (D_TXFILTER_DCU8_127_96)

Offset: 0x181010FC
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.17 Misc. DCU-Specific Settings (D_MISC)

Offset: 0x18101100 + ($D < 2$)
Access: Read/Write
Cold Reset: See field description
Warm Reset: Unaffected

Bit	Bit Name	Reset	Description	
31:25	RES	0x0	Reserved	
24	SIFS_BURST_CHAN_BUSY_IGNORE	0x1	SIFS burst medium sense policy.	
			0	MAC obeys medium busy during SIFS burst
			1	MAC ignore medium busy during SIFS burst
23	RETRY_ON_BLOWN_IFS_EN	0x0	Blown IFS handling policy. This setting controls how the DCU handles the case in which the DMA of a frame takes so long that the IFS spacing is met before the frame trigger level is reached.	
			0	Send the frame on the air anyway (ignore the IFS violation); causes the frame to be sent on the air at a time that is later than called for in the 802.11 spec
			1	Do not send the frame on the air. Instead, act as if the frame had been sent on the air but failed and initiate the retry procedure. A retry will be charged against the frame. If more retries are permitted, the frame will be retried. If the retry limit has been reached, the frame will fail.
22	VIRT_COLL_CW_INC_EN	0x0	Post-frame backoff disable.	
			0	DCU performs a backoff after each frame finishes, as required by the 11a spec
			1	DCU skips the post-frame backoff (or, equivalently, acts as if it always selects a post-frame backoff count of zero)
21	POST_BKOFF_SKIP	0x0	Post-frame backoff disable.	
			0	DCU performs a backoff after each frame finishes, as required by the 11a spec
			1	DCU skips the post-frame backoff (or, equivalently, acts as if it always selects a post-frame backoff count of zero)
20	SEQNUM_FREEZE	0x0	Sequence number increment disable.	
			0	Allow the DCU to use a normal sequence number progression (the DCU increments the sequence number for each new frame)
			1	Force the sequence number to be frozen at its current value
19	LOCKOUT_IGNORE	0x0	DCU arbiter lockout ignore control.	
			0	Obey DCU arbiter lockouts from higher-priority DCUs
			1	Ignore DCU arbiter lockouts from higher-priority DCUs (that is, allow the current DCU to arbitrate for access to the PCU even if one or more higher-priority DCUs is asserting a DCU arbiter lockout)

Bit	Bit Name	Reset	Description	
18	LOCKOUT_ GBL_EN	0x0	DCU arbiter lockout control	
			0	No lockout. Allows lower-priority DCUs to arbitrate for access to the PCU concurrently with this DCU.
			1	Intra-frame lockout only. Forces all lower-priority DCUs to defer arbitrating for access to the PCU while the current DCU arbitrates for access to the PCU or doing an intra-frame backoff.
			2	Global lockout. Forces all lower-priority DCUs to defer arbitration for access to the PCU when: ■ At least one QCU feeding to the current DCU has a frame ready ■ The DCU is actively processing a frame, including arbitrating for PCU access, performing intra- or post-frame backoff, DMAing frame data to the PCU, or waiting for the PCU to complete the frame.
			3	Reserved
17	ARB_ LOCKOUT_IF_ EN	0x0	DCU arbiter lockout control	
16	DCU_IS_BRN	0x0	Beacon use indication. Indicates whether the DCU is being used for beacons.	
			0	DCU is being used for non-beacon frames only
			1	DCU is being used for beacon frames only
15:14	VIRT_COL_ POLICY	0x0	Virtual collision handling policy. Resets to 0x0. 0 - 1 - 2 - Reserved 3 - Reserved	
			3:2	Reserved
			1	Ignore. Virtual collisions are ignored (i.e., the DCU immediately re-arbitrates for access to the PCU without doing a backoff and without incrementing the retry count)
			0	Default handling. A virtual collision is processed like a collision on the air except that the retry count for the frame is not incremented (that is, just do the backoff)
13	RES	0x0	Reserved	
12	BKOFF_PF	0x0	Backoff persistence factor setting.	
			0	New CW equals old CW
			1	Use binary-exponential CW progression
11	HCF_POLL_EN	0x0	HCF poll enable.	
			0	DCU operates in VDCF mode
			1	DCU operates in HCF mode
10	RES	0x0	Reserved	
9	FRAG_ BURST_ BKOFF_EN	0x0	Fragment burst backoff policy. This bit controls whether the DCU performs a backoff after each transmission of a fragment (that is, a frame with the MoreFrag bit set in the frame control field).	
			0	The DCU handles fragment bursts normally -- no backoff is performed after a successful transmission, and the next fragment is sent at SIFS.
			1	Modified handling. The DCU performs a backoff after all fragments, even those transmitted successfully. In addition, after the backoff count reaches zero, the DCU then follows the normal channel access procedure and sends at AIFS rather than at SIFS. This setting is intended to ease the use of fragment bursts in XR mode see bug 4454 for more details.

Bit	Bit Name	Reset	Description	
18	LOCKOUT_ GBL_EN	0x0	DCU arbiter lockout control	
			0	No lockout. Allows lower-priority DCUs to arbitrate for access to the PCU concurrently with this DCU.
			1	Intra-frame lockout only. Forces all lower-priority DCUs to defer arbitrating for access to the PCU while the current DCU arbitrates for access to the PCU or doing an intra-frame backoff.
			2	Global lockout. Forces all lower-priority DCUs to defer arbitration for access to the PCU when: ■ At least one QCU feeding to the current DCU has a frame ready ■ The DCU is actively processing a frame, including arbitrating for PCU access, performing intra- or post-frame backoff, DMAing frame data to the PCU, or waiting for the PCU to complete the frame.
			3	Reserved
17	ARB_ LOCKOUT_IF_ EN	0x0	DCU arbiter lockout control	
16	DCU_IS_BRN	0x0	Beacon use indication. Indicates whether the DCU is being used for beacons.	
			0	DCU is being used for non-beacon frames only
			1	DCU is being used for beacon frames only
15:14	VIRT_COL_ POLICY	0x0	Virtual collision handling policy. Resets to 0x0. 0 - 1 - 2 - Reserved 3 - Reserved	
			3:2	Reserved
			1	Ignore. Virtual collisions are ignored (i.e., the DCU immediately re-arbitrates for access to the PCU without doing a backoff and without incrementing the retry count)
			0	Default handling. A virtual collision is processed like a collision on the air except that the retry count for the frame is not incremented (that is, just do the backoff)
13	RES	0x0	Reserved	
12	BKOFF_PF	0x0	Backoff persistence factor setting.	
			0	New CW equals old CW
			1	Use binary-exponential CW progression
11	HCF_POLL_EN	0x0	HCF poll enable.	
			0	DCU operates in VDCF mode
			1	DCU operates in HCF mode
10	RES	0x0	Reserved	
9	FRAG_ BURST_ BKOFF_EN	0x0	Fragment burst backoff policy. This bit controls whether the DCU performs a backoff after each transmission of a fragment (that is, a frame with the MoreFrag bit set in the frame control field).	
			0	The DCU handles fragment bursts normally -- no backoff is performed after a successful transmission, and the next fragment is sent at SIFS.
			1	Modified handling. The DCU performs a backoff after all fragments, even those transmitted successfully. In addition, after the backoff count reaches zero, the DCU then follows the normal channel access procedure and sends at AIFS rather than at SIFS. This setting is intended to ease the use of fragment bursts in XR mode see bug 4454 for more details.

Bit	Bit Name	Reset	Description	
8	FRAG_ BURST_WAIT_ QCU_EN	0x0	Fragment burst frame starvation handling policy. This bit controls the DCU operation when the DCU is in the middle of a fragment burst and finds that the QCU sourcing the fragments does not have the next fragment available.	
			0	The DCU terminates the fragment burst. Note that when this occurs, the remaining fragments (when the QCU eventually has them available) will be sent as a separate fragment burst with a different sequence number
			1	The DCU waits for the QCU to have the next fragment available. While doing so, all other DCUs will be unable to transmit frames.
7	CW_RST_AT_ TS_END)DIS	0x0	End of transmission series CW reset policy. Note that this bit controls only whether the contention window is reset when transitioning from one transmission series to the next *within* a single frame. The CW is reset per the 802.11 spec when the entire frame attempt terminates (either because the frame was sent successfully or because all transmission series failed).	
			0	Reset the CW to CW_MIN at the end of each intraframe transmission series.
			1	Do not reset the CW at the end of each intraframe transmission series.
6	SFC_RST_AT_ TS_END_EN	0x0	End of transmission series station RTS data failure count reset policy. Note that this bit controls only whether the two station failure counts are reset when transitioning from one transmission series to the next *within* a single frame. The counts are reset per the 802.11 spec when the entire frame attempt terminates (either because the frame was sent successfully or because all transmission series failed).	
			0	Do not reset the station RTS failure count or the station data failure count at the end of each transmission series.
			1	Reset both the station RTS failure count and the station data failure count at the end of each transmission series
5:0	DATA_BKOFF _THRESH	0x2	Backoff threshold setting. Determines the backoff count at which the DCU will initiate arbitration for access to the PCU and commit to sending the frame.	

10.17.18 QCU Tx Filter DCU1 31-0 (D_TXFILTER_DCU1_31_0)

Offset: 0x18101138
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCUO

10.17.19 QCU Tx Filter DCU9 31-0 (D_TXFILTER_DCU9_31_0)

Offset: 0x1810113C
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.20 DCU Sequence (D_SEQ)

Offset: 0x18101140
Access: Read/Write
Reset: 0x0

MAC DCU sequence number register.

Bit	Bit Name	Description
31:12	RES	Reserved
11:0	NUM	Value of the sequence number to be inserted into the next frame. Shared across all DCUs.

10.17.21 QCU Tx Filter DCU1 63-32 (D_TXFILTER_DCU1_63_32)

Offset: 0x18101178
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCUO

10.17.22 QCU Tx Filter DCU9 63-32 (D_TXFILTER_DCU9_63_32)

Offset: 0x1810117C
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.23 QCU Tx Filter DCU1 95-64 (D_TXFILTER_DCU1_95_64)

Offset: 0x181011B8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCUO

10.17.24 QCU Tx Filter DCU9 95-64 (D_TXFILTER_DCU9_95_64)

Offset: 0x181011BC
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.25 QCU Tx Filter DCU1 127-96 (D_TXFILTER_DCU1_127_96)

Offset: 0x181011F8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCUO

10.17.26 QCU Tx Filter DCU9 127-96 (D_TXFILTER_DCU9_127_96)

Offset: 0x181011FC
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.27 QCU Tx Filter DCU2 31-0 (D_TXFILTER_DCU2_31_0)

Offset: 0x18101238
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.28 DCU Pause (D_PAUSE)

Offset: 0x18101270
Access: Read/Write
Reset: See field description

MAC DCU pause register.

Bit	Bit Name	Reset	Description	
31:21	RES	0x0	Reserved	
20:17	SPARE	0x0	Spare bits	
16	STATUS	0x1	Transmit pause status. Resets to 0x1. 0 - 1 -	
			0	Transmit pause request has not yet taken effect. This means that some of the DCUs for which a transmission pause request has been issued via bits [9:0] of this register still are transmitting and have not yet paused.
			1	All DCUs for which a transmission pause request has been issued via bits [9:0] of this register, if any, have in fact paused their transmissions. Note that if no transmission pause request is pending (that is, bits [9:0] of this register are all set to 0), then this transmit pause status bit will be set to one.
15:10	RES	0x0	Reserved	
9:0	REQUEST	0x0	Request that some subset of the DCUs pause transmission. For bit D of this field (9<=D<=0.	
			0	Allow DCU D to continue to transmit normally
			1	Request that DCU D pause transmission as soon as it is able to do so.
11:0	NUM	Value of the sequence number to be inserted into the next frame. Shared across all DCUs.		

10.17.29 QCU Tx Filter DCU2 63-32 (D_TXFILTER_DCU2_63_32)

Offset: 0x18101278
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.30 DCU WOW Keep-Alive (DCU_WOW_KEEP_ALIVE)

Offset: 0x181012B0
Access: Read/Write
Reset: 0x0

WOW keep-alive transmission enable.

Bit	Bit Name	Description	
31:24	RES	Reserved	
23:12	RX_TIMEOUT_CNT	Keep-alive receive frame timeout. This field specifies the minimum amount of time after a keep-alive frame is sent for which the MAC will remain awake so that it can receive a response frame from the AP. Specified in units of 4096 core clocks (40 80 MHz). Resets to 0x0, which allows the MAC to return to sleep immediately after sending the keep-alive frame.	
11:4	BCN_CNT	Beacon interval. The WoW keep-alive frame normally is transmitted in response to the receipt of every Nth beacon, regardless of the beacon's contents. This field specifies the value of N. Setting this field to a value of 0 disables WoW keep-alive transmission in response to received beacons. Setting this field to a value from 1-255 enables WoW keep-alive transmission in response to received beacons and establishes the value of N.	
3:2	RES	Reserved	
1	TIME_EN	TIM-triggered transmission enable. This field controls whether the WoW keep-alive frame is transmitted in response to received beacons in which the local station's TIM bit is set.	
		0	The WoW keep-alive frame is not transmitted in response to such beacons
		1	The WoW keep-alive frame is transmitted each time such a beacon is received
0	TX_EN	WoW keep-alive transmission enable.	
		0	WoW keep-alive transmission is disabled. The DCUs and QCUs operate normally
		1	WoW keep-alive transmission is enabled. DCU0 will be used as the source of the periodic WoW keep-alive frame. No other DCUs may be used.

10.17.31 QCU Tx Filter DCU2 95-64 (D_TXFILTER_DCU2_95_64)

Offset: 0x181012B8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.32 DCU Transmission Slot Mask (D_TXSLOTMASK)

Offset: 0x181012F0
Access: Read/Write
Cold Reset: 0x0
Warm Reset: Unaffected

NOTE When bits [26:25] of the QCU Tx Filter DCU2 95-64 (D_TXFILTER_DCU2_95_64) register are non-zero, D_TXSLOTMASK controls the slots DCUs can start frame transmission on. The slot occurring coincident with SIFS elapsing is slot 0. Slot numbers increase thereafter, whether the channel was idle or busy during the slot. If bits [26:25] of D_GBL_IFS_MISC are zero, this register has no effect.

Bit	Bit Name	Description	
31:16	RES	Reserved	
15	SLOT_TX[15]	Specifies whether transmission may start on slot numbers that are congruent to 15 (mod 16)	
		0	Transmission may start on such slots
		1	Transmission may not start on such slots
...	...	...	
1	SLOT_TX[1]	Specifies whether transmission may start on slot numbers that are congruent to 1 (mod 16)	
		0	Transmission may start on such slots
		1	Transmission may not start on such slots
0	SLOT_TX[0]	Specifies whether transmission may start on slot numbers that are congruent to 0 (mod 16)	
		0	Transmission may start on such slots
		1	Transmission may not start on such slots

10.17.33 QCU Tx Filter DCU2 127-96 (D_TXFILTER_DCU2_127_96)

Offset: 0x181012F8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.34 QCU Tx Filter DCU3 31-0 (D_TXFILTER_DCU3_31_0)

Offset: 0x18101338
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.35 QCU Tx Filter DCU3 63-32 (D_TXFILTER_DCU3_63_32)

Offset: 0x18101378
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.36 QCU Tx Filter DCU3 95-64 (D_TXFILTER_DCU3_95_64)

Offset: 0x181013B8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.37 QCU Tx Filter DCU3 127-96 (D_TXFILTER_DCU3_127_96)

Offset: 0x181013F8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.38 QCU Tx Filter DCU4 31-0 (D_TXFILTER_DCU4_31_0)

Offset: 0x18101438
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.39 QCU-DCU Tx Filter Clear (D_TXFILTER_CLEAR)

Offset: 0x1810143C
Access: Read/Write
Reset: 0x0000

This register is used to clear the TX filter

Bit	Bit Name	Description
31:0	DATA	Transmit filter clear

10.17.40 QCU Tx Filter DCU4 63-32 (D_TXFILTER_DCU4_63_32)

Offset: 0x18101478
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.41 QCU-DCU Tx Filter Set (D_TXFILTER_SET)

Offset: 0x1810147C
Access: Read/Write
Reset: 0x0000

This register is used to set the TX filter

Bit	Bit Name	Description
31:0	DATA	Transmit filter set

10.17.42 QCU Tx Filter DCU4 95-64 (D_TXFILTER_DCU4_95_64)

Offset: 0x18101478
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.43 QCU Tx Filter DCU4 127-96 (D_TXFILTER_DCU4_127-96)

Offset: 0x181014F8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.44 QCU Tx Filter DCU5 31-0 (D_TXFILTER_DCU5_31_0)

Offset: 0x18101538
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.45 QCU Tx Filter DCU5 63-32 (D_TXFILTER_DCU5_63_32)

Offset: 0x18101578
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.46 QCU Tx Filter DCU5 95_64 (D_TXFILTER_DCU5_95_64)

Offset: 0x181015B8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.47 QCU Tx Filter DCU5 127-96 (D_TXFILTER_DCU5_127_96)

Offset: 0x181015F8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.48 QCU Tx Filter DCU6 31-0 (D_TXFILTER_DCU6_31_0)

Offset: 0x18101638
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.49 QCU Tx Filter DCU6 63-32 (D_TXFILTER_DCU6_63_32)

Offset: 0x18101678
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.50 QCU Tx Filter DCU6 95_64 (D_TXFILTER_DCU6_95_64)

Offset: 0x181016B8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.51 QCU Tx Filter DCU6 127-96 (D_TXFILTER_DCU6_127_96)

Offset: 0x181016F8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.52 QCU Tx Filter DCU7 31-0 (D_TXFILTER_DCU7_31_0)

Offset: 0x18101738
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.53 QCU Tx Filter DCU7 63-32 (D_TXFILTER_DCU7_63_32)

Offset: 0x18101778
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.54 QCU Tx Filter DCU7 95_64 (D_TXFILTER_DCU7_95_64)

Offset: 0x181017B8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.55 QCU Tx Filter DCU7 127-96 (D_TXFILTER_DCU7_127_96)

Offset: 0x181017F8
Access: Read/Write
Reset: 0x0000

See the register description for QCU Tx Filter DCU0 0-31 (D_TXFILTER_DCU0_0_31).

Bit	Bit Name	Description
31:0	DATA	Transmit filter bits for DCU8

10.17.56 MAC Sleep Status (SLEEP_STATUS)

Offset: 0x18101F00
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Sleep status

10.17.57 MAC LED Configuration (LED_CONFIG)

Offset: 0x18101F04
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	LED Configuration

10.18 WMAC Glue Registers

Table 10-19 summarizes the WMAC glue control registers.

Table 10-19 WMAC Glue Registers

Offset	Name	Description	Page
0x18104000	WMAC_GLUE_INTF_RESET_CONTROL	Interface Reset Control	page 336
0x18104004	WMAC_GLUE_INTF_PM_CTRL	Power Management Control	page 336
0x18104008	WMAC_GLUE_INTF_INTR_SYNC_ENABLE	Synchronous Interrupt Enable	page 336
0x18104018	WMAC_GLUE_INTF_TIMEOUT	Interface Timeout	page 336
0x18104028	WMAC_GLUE_INTF_INTR_SYNC_CAUSE	Synchronous Interrupt Cause	page 337
0x1810402C	WMAC_GLUE_INTF_INTR_SYNC_ENABLE	Synchronous Interrupt Enable	page 337
0x18104030	WMAC_GLUE_INTF_INTR_ASYNC_MASK	Asynchronous Interrupt Mask	page 337
0x18104034	WMAC_GLUE_INTF_INTR_SYNC_MASK	Synchronous Interrupt Mask	page 337
0x18104038	WMAC_GLUE_INTF_INTR_ASYNC_ CAUSE	Asynchronous Interrupt Cause	page 338
0x1810403C	WMAC_GLUE_INTF_INTR_ASYNC_ ENABLE	Asynchronous Interrupt Enable	page 338
0x18104048	WMAC_GLUE_INTF_GPIO_IN	GPIO Input	page 338
0x1810404C	WMAC_GLUE_INTF_GPIO_INPUT_VALUE	WMAC Glue GPIO Input Value	page 338
0x18104050	WMAC_GLUE_INTF_SWCOM_GPIO_ FUNC_ENABLE	GPIO SWCOM Enable Function	page 339
0x1810405C	WMAC_GLUE_INTF_GPIO_INPUT_VALUE	WMAC Glue GPIO Input Value	page 339
0x18104074	WMAC_GLUE_INTF_GPIO_INPUT_STATE	Output Values from MAC to GPIO Pins	page 340
0x18104088	WMAC_GLUE_INTF_OBS_CRTL	WMAC Glue Observation Control	page 341
0x181040A0	WMAC_GLUE_INTF_MISC	WMAC Glue Miscellaneous	page 341
0x181040B4	WMAC_GLUE_INTF_MAC_TXAPSYNC	Synchronous AP Transmit	page 342
0x181040B8	WMAC_GLUE_INTF_MAC_TXSYNC_ INITIAL_SYNC_TMR	Synchronous Initial Timer	page 342
0x181040BC	WMAC_GLUE_INTF_INTR _PRIORITY_SYNC_CAUSE	Synchronous Priority Interrupt Cause	page 342
0x181040C0	WMAC_GLUE_INTF_INTR _PRIORITY_SYNC_ENABLE	Synchronous Priority Interrupt Enable	page 343
0x181040C4	WMAC_GLUE_INTF_INTR _PRIORITY_ASYNC_MASK	Asynchronous Priority Interrupt Mask	page 343
0x181040C8	WMAC_GLUE_INTF_INTR _PRIORITY_SYNC_MASK	Synchronous Priority Interrupt Mask	page 343
0x181040CC	WMAC_GLUE_INTF_INTR _PRIORITY_ASYNC_CAUSE	Asynchronous Priority Interrupt Cause	page 344
0x181040D4	WMAC_GLUE_INTF_INTR _PRIORITY_ASYNC_ENABLE	Asynchronous Priority Interrupt Enable	page 344
0x181040F0	WMAC_GLUE_INTF_AXI_BYTE_SWAP	AXI to MAC and MAC to AXI Byte Swap Enable	page 344

10.18.1 Interface Reset Control (WMAC_GLUE_INTF_RESET_CONTROL)

Offset: 0x18104000
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:2	RES	Reserved	
1	APB_RESET	0	Normal operation of the MAC APB interface
		1	Hold the MAC APB interface in reset
0	RES	Reserved	

10.18.2 Power Management Control (WMAC_GLUE_INTF_PM_CTRL)

Offset: 0x18104004
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:23	RES	Reserved
22	WMAC_GLUE_PME_ENABLE	Enable WOW detect interrupt from MAC
21	WMAC_GLUE_MAC_WOW_CLEAR	WOW clear signal going to the MAC
20:0	RES	Reserved

10.18.3 Synchronous Interrupt Enable (WMAC_GLUE_INTF_INTR_SYNC_ENABLE)

Offset: 0x18104008
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Writing a 1 to any bit in this register will allow the corresponding interrupt signal to set its corresponding bit in the synchronous interrupt cause register.

10.18.4 Interface Timeout (WMAC_GLUE_INTF_TIMEOUT)

Offset: 0x18104018
Access: Read/Write
Reset: 0x0

APB and AXI timeout counter.

Bit	Bit Name	Description
31:16	AXI_TIMEOUT_VAL	AXI timeout counter for DMA success
15:0	RES	Reserved

10.18.5 Synchronous Interrupt Cause (WMAC_GLUE_INTF_INTR_SYNC_CAUSE)

Offset: 0x18104028
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in the synchronous mode. In order for any bit to be set in this register, the corresponding bit in the synchronous interrupt enable register must also be set.

10.18.6 Synchronous Interrupt Enable (WMAC_GLUE_INTF_INTR_SYNC_ENABLE)

Offset: 0x1810402C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the synchronous interrupt cause register.

10.18.7 Asynchronous Interrupt Mask (WMAC_GLUE_INTF_INTR_ASYNC_MASK)

Offset: 0x18104030
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	A bit set to 1 in this register allows the corresponding interrupt signal to trigger a PCI/PCIE interrupt provided that the corresponding Async Interrupt cause register bit is set. Note that for the Async Interrupt Cause register bit to be set, the corresponding Async Interrupt Enable register bit must also be set by the software

10.18.8 Synchronous Interrupt Mask (WMAC_GLUE_INTF_INTR_SYNC_MASK)

Offset: 0x18104034
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	A bit set to 1 in this register allows the corresponding interrupt signal to trigger a PCI/PCIE interrupt provided that the corresponding Sync Interrupt cause register bit is set. Note that for the Sync Interrupt Cause register bit to be set, the corresponding Sync Interrupt Enable register bit must also be set by the software

10.18.9 Asynchronous Interrupt Cause (WMAC_GLUE_INTF_INTR_ASYNC_CAUSE)

Offset: 0x18104038
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in the asynchronous mode. In order for any bit to be set in this register, the corresponding bit in the asynchronous interrupt enable register must also be set.

10.18.10 Asynchronous Interrupt Enable (WMAC_GLUE_INTF_INTR_ASYNC_ENABLE)

Offset: 0x1810403C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the asynchronous interrupt cause register.

10.18.11 GPIO Output (WMAC_GLUE_INTF_GPIO_OUT)

Offset: 0x18104048
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:4	RES	Reserved
3:0	OUT	Output value of each GPIO. This value is only used if the corresponding GPIO enable bits and GPIO output MUX registers are set correctly.

10.18.12 GPIO Input (WMAC_GLUE_INTF_GPIO_IN)

Offset: 0x1810404C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:11	RES	Reserved
10:0	IN	Input value of each GPIO. This value is only used if the corresponding GPIO enable bits and GPIO output MUX registers are set correctly.

10.18.13 GPIO SWCOM Enable Function (WMAC_GLUE_INTF_SWCOM_GPIO_FUNC_ENABLE)

Offset: 0x18104050
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:4	RES	Reserved
3:0	OUT	Enables GPIO output signals on SWCOM pins

10.18.14 WMAC Glue GPIO Input Value (WMAC_GLUE_INTF_GPIO_INPUT_VALUE)

Offset: 0x1810405C
Access: Read/Write
Reset: 0x0

WMAC Glue GPIO input value

Bit	Bit Name	Description	
31:22	RES	Reserved	
21	BT_PRIORITY_3_ENABLE	0	Set BT_PRIORITY_3 to default value
		1	Connect BT_PRIORITY_3 to GPIO input
20	BT_PRIORITY_3_VAL	0	Set BT_PRIORITY_2 to default value
		1	Connect BT_PRIORITY_2 to GPIO input
19	BT_PRIORITY_2_ENABLE	0	Set BT_PRIORITY_2 to default value
		1	Connect BT_PRIORITY_2 to GPIO input
18	BT_PRIORITY_2_VAL	Default value of BT_PRIORITY_2 input	
17	RES	Reserved	
16	RTC_RESET_OVRD_ENABLE	0	RTC reset is entirely controlled by software
		1	RTC reset is controlled by GPIO input as well as software
15	RFSILENT_BB_L_ENABLE	0	Set RFSILENT_BB_L to default value
		1	Connect RFSILENT_BB_L to GPIO input
14	CLK25_ENABLE	0	Set CLK25 to default value
		1	Connect CLK25 to GPIO input
13	RES	Reserved	
12	BT_ACTIVE_ENABLE	0	Set BT_ACTIVE to default value
		1	Connect BT_ACTIVE to GPIO input
11	BT_FREQUENCY_ENABLE	0	Set BT_FREQUENCY to default value
		1	Connect BT_FREQUENCY to GPIO input
10	BT_PRIORITY_ENABLE	0	Set BT_PRIORITY to default value
		1	Connect BT_PRIORITY to GPIO input
9	RES	Reserved	
8	GPIO_RST_TSF_ENABLE	0	Set RST_TSF to default value
		1	Connect RST_TSF to GPIO input
7	RFSILENT_BB_L_VAL	Default value of RFSILENT_BB_L input	
6	CLK25_VAL	Default value of CLK25 input	
5	RES	Reserved	
4	BT_ACTIVE_VAL	Default value of BT_ACTIVE input	
3	BT_FREQUENCY_VAL	Default value of BT_FREQUENCY input	
2	BT_PRIORITY_VAL	Default value of BT_PRIORITY input	
1:0	RES	Reserved	

10.18.15 Output Values from MAC to GPIO Pins (WMAC_GLUE_INTF_GPIO_INPUT_STATE)

Offset: 0x18104074
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:7	RES	Reserved
6	TX_FRAME	Tx frame
5	RX_CLEAR_EXTERNAL	Rx clear external
4	LED_POWER_EN	LED power
3	LED_NETWORK_EN	LED network
2	RES	Reserved
1	PWR_LED	LED power
0	ATT_LED	ATT LED

10.18.16 WMAC Glue Observation Control (WMAC_GLUE_INTF_OBS_CRTL)

Offset: 0x18104088
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:8	RES	Reserved
7:6	OBS_MODE	OBS mode
5:4	ANT_SEL	Antenna select
3:0	OBS_SEL	OBS select

10.18.17 WMAC Glue Miscellaneous (WMAC_GLUE_INTF_MISC)

Offset: 0x181040A0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	AT_SPEED_EN	WMAC glue miscellaneous

10.18.18 Synchronous AP Transmit (WMAC_GLUE_INTF_MAC_TXAPSYNC)

Offset: 0x181040B8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	DATA	

10.18.19 Synchronous Initial Timer (WMAC_GLUE_INTF_MAC_TXSYNC_INITIAL_SYNC_TMR)

Offset: 0x181040BC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DATA	

10.18.20 Synchronous Priority Interrupt Cause (WMAC_GLUE_INTF_INTR_PRIORITY_SYNC_CAUSE)

Offset: 0x181040C0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in synchronous mode. For any bit to be set in this register, the corresponding bit in the synchronous priority interrupt enable register must also be set by software:	
		Bit[0]	Tx interrupt triggered
		Bit[1]	Rx low priority interrupt triggered
		Bit[2]	Rx high priority interrupt triggered

10.18.21 Synchronous Priority Interrupt Enable (WMAC_GLUE_INTF_INTR_PRIORITY_SYNC_ENABLE)

Offset: 0x181040C4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the asynchronous priority interrupt cause register:	
		Bit[0]	Tx interrupt enable
		Bit[1]	Rx low priority interrupt enable
		Bit[2]	Rx high priority interrupt enable

10.18.22 Asynchronous Priority Interrupt Mask (WMAC_GLUE_INTF_INTR_PRIORITY_ASYNC_MASK)

Offset: 0x181040C8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	A bit set to 1 in this register allows the corresponding interrupt signal to trigger a CPU interrupt provided that the corresponding synchronous priority interrupt cause register bit is set. For the priority asynchronous interrupt cause register bit to be set, the corresponding asynchronous priority interrupt enable register bit must also be set by software:	
		Bit[0]	Tx interrupt mask
		Bit[1]	Rx low priority interrupt mask
		Bit[2]	Rx high priority interrupt mask

10.18.23 Synchronous Priority Interrupt Mask (WMAC_GLUE_INTF_INTR_PRIORITY_SYNC_MASK)

Offset: 0x181040CC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	A bit set to 1 in this register allows the corresponding interrupt signal to trigger a CPU interrupt provided that the corresponding synchronous priority interrupt cause register bit is set. For the priority asynchronous interrupt cause register bit to be set, the corresponding asynchronous priority interrupt enable register bit must also be set by software:	
		Bit[0]	Tx interrupt mask
		Bit[1]	Rx low priority interrupt mask
		Bit[2]	Rx high priority interrupt mask

10.18.24 Asynchronous Priority Interrupt Cause (WMAC_GLUE_INTF_INTR_PRIORITY_ASYNC_CAUSE)

Offset: 0x181040D0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in asynchronous mode. For any bit to be set in this register, the corresponding bit in the asynchronous priority interrupt enable register must also be set by software:	
		Bit[0]	Tx interrupt triggered
		Bit[1]	Rx low priority interrupt triggered
		Bit[2]	Rx high priority interrupt triggered

10.18.25 Asynchronous Priority Interrupt Enable (WMAC_GLUE_INTF_INTR_PRIORITY_ASYNC_ENABLE)

Offset: 0x181040D4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the asynchronous priority interrupt cause register:	
		Bit[0]	Tx interrupt enable
		Bit[1]	Rx low priority interrupt enable
		Bit[2]	Rx high priority interrupt enable

10.18.26 AXI to MAC and MAC to AXI Byte Swap Enable (WMAC_GLUE_INTF_AXI_BYTE_SWAP)

Offset: 0x181040F0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:1	RES	Reserved	
0	ENABLE	0	Do not swap data bytes of a 32-bit word, transferred between Memory and MAC (Default)
		1	Swap data bytes of a 32-bit word, transferred between Memory and MAC

10.19 RTC Registers

RTC registers occupy the offset range 0x18107000-0x18107FFC in the QCA9558 address space. Within this address range, the 0x18107040-0x18107058 registers are always on and available for software access regardless of whether the RTC is asleep. Table 10-20 summarizes the RTC registers for the QCA9558.

Table 10-20 RTC Summary

Address	Name	Description	Page
0x18107000	RESET_CONTROL	Reset Control	page 345
0x18107004	XTAL_CONTROL	XTAL Control	page 346
0x18107014	WLAN_PLL_CONTROL	WLAN PLL Control Settings	page 347
0x18107018	PLL_SETTLE	PLL Settling Time	page 348
0x1810701C	XTAL_SETTLE	Crystal Settling Time	page 348
0x18107020	CLOCK_OUT	Pin Clock Speed Control	page 349
0x18107028	RESET_CAUSE	Reset Cause	page 350
0x1810702C	SYSTEM_SLEEP	System Sleep Status	page 350
0x18107034	KEEP_AWAKE	Keep Awake Timer	page 351
0x18107038	DERIVED_RTC_CLK	Derived RTC Clock	page 351
0x1810703C	PLL_CONTROL2	PLL Control	page 352
0x18107040	RTC_SYNC_REGISTER	RTC Sync Reset	page 352
0x18107044	RTC_SYNC_STATUS	RTC Sync Status	page 352
0x18107048	RTC_SYNC_DERIVED	RTC Derived	page 353
0x1810704C	RTC_SYNC_FORCE_WAKE	RTC Force Wake	page 353
0x18107050	RTC_SYNC_INTR_CAUSE	RTC Interrupt Cause	page 353
0x18107054	RTC_SYNC_INTR_ENABLE	RTC Interrupt Enable	page 354
0x18107058	RTC_SYNC_INTR_MASK	RTC Interrupt Mask	page 354

10.19.1 Reset Control (RESET_CONTROL)

Address: 0x18107000
Access: Read/Write
Reset: 0x0

This register is used to control individual reset pulses to functional blocks. Software can hold any target block in reset by writing a 1 to the corresponding bit in this register. Reset will be held asserted to the target block as long as the corresponding bit is set. Multiple blocks may be held in reset simultaneously.

Bit	Bit Name	Description
31:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	COLD_RST	Cold reset
2	WARM_ RESET	Warm reset
1	MAC_COLD_RST	Holds MAC block in cold reset, including BB and Radio. To clear this reset, SW must write a 0 and poll (for 62-92 µsecs) till this bit returns a 0.
0	MAC_WARM_RST	Holds MAC block in warm reset, including BB and radio

10.19.2 XTAL Control (XTAL_CONTROL)

Address: 0x18107004
Access: Read/Write
Reset: See field description

This register controls the analog crystal interface, the regulator and the clock source selection between an TCXO and a crystal.

Bit	Bit Name	Reset	Description
31:1	RES	0x0	Reserved
0	TXCO	0x0	When a TCXO device is used, software should set this field to 1 **WARNING** If this field is set to 1 when a crystal is being used, the high speed clock will stop and the chip will hang. 0 The chip is being driven by a crystal. 1 The chip is being driven by a TCXO device

10.19.3 Switching Regulator Control Bits 0 (REG_CONTROL0)

Address: 0x18107008
Access: Read/Write
Reset: See field description

This register contains the regulator control bits for switching.

Bit	Bit Name	Reset	Description
31:0	SWREG_BITS	0x0	Switching regulator control bits

10.19.4 WLAN PLL Control Settings (WLAN_PLL_CONTROL)

Address: 0x18107014
Access: Read/Write
Reset: See field description

Control settings for the PLL.: This register provides access to the PLL setup control signals. Any write to this register will freeze all high speed clocks for 61 µsec. The clock select lines and PLL control lines will change after 30.5 µsec, then another 30.5 µsec passes before enable to allow the clocks to settle.

PLL freq = (refclk/refdiv) * (div_int + div_frac*2^4/(2^18-1)) * (1/f(clk_sel)).

Before applying f(clk_sel) frequency range is 530 ~ 830 MHz.

NOTE This reset values of some fields in this register must be kept in sync with the corresponding fields in bb reg 31

Bit	Bit Name	Type	Reset	Description	
31	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
30	MAC_ OVERRIDE	RW	0x0	When set, a MAC clock request will deassert PLLBYPASS even if the BYPASS field is set to 1. This can be set when its the preferable time to select the ON state to use the PLL, instead of the SOC_ON state.	
29	NOPWD	RW	0x0	Prevents the PLL from being powered down when the PLLBYPASS is asserted or when in light sleep	
28	UPDATING	RO	0x0	This bit is set during the PLL update process. After software writes to the PLL_CONTROL, it takes about 45 secs for the update to occur. Software may poll this bit to see if the update has taken place.	
				0	PLL update is complete
				1	PLL update is pending
27	BYPASS	RW	0x00000001	Bypass PLL. This defaults to 1 for test purposes. Software must enable the PLL for normal operation.	
26:25	CLK_SEL	RW	0x0	Controls the final PLL select.	
				00	1
				01	2
				10	4
				11	Bypass
24:20	REFDIV	RW	0x00000005	Reference clock divider	
19:6	DIV_FRAC	RW	0x0	Primary multiplier	
5:0	DIV_INT	RW	0x2C	Primary multiplier	

10.19.5 PLL Settling Time (PLL_SETTLE)

Address: 0x18107018
Access: Read/Write
Reset: See field description

This register sets the PLL settling time. The PLL requires some time to settle once it is powered up or reprogrammed. Each time the PLL parameters change due to a write to the PLL register or a system event which changes the PLL control, hardware will gate off the clocks for PLL_SETTLE time while the PLL stabilizes. Units are in REFCLK periods.

NOTE The reset values of this register must be kept in sync with the corresponding field in the baseband register 31.

Bit	Bit Name	Reset	Description
31:11	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
10:0	TIME	0x00000400	Time required for the PLL to settle. Units are in REFCLK periods, so the default value of 1024 will result in a 25.6 µsec settling time. This register should never be set less than 100.

10.19.6 Crystal Settling Time (XTAL_SETTLE)

Address: 0x1810701C
Access: Read/Write
Reset: See field description

This register sets the crystal settling time. The external crystal requires some time to settle once it is powered up. The power occurs as chip passes through the WAKEUP state, between OFF and ON or between SLEEP an ON. This exact time will vary and must be characterized, so this register is provided to allow the XTAL power up FSM to transition in the minimal correct time. The default value of 63 will always allow the XTAL to be fully settled before clocks are enabled, but this value can be set to a smaller value if hardware characterization approves. The timer will expire in (XTAL_SETTLE + 1) clocks. Unlike most registers, XTAL_SETTLE will retain its programmed value in the RTC block during reset. The value programmed in this register should be matched to the MAC register Sleep Clock 32 KHz Wake, field 'SLEEP32_WAKE_XTL_TIME'. Note that the MAC register value is in microseconds.

Bit	Bit Name	Reset	Description
31:7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:0	TIME	0x00000001	Time required for the XTAL to settle. Units are in 30 µsecs, so the default value of 66 will result in 2.0 msec settling time. this register should never be set to 0.

10.19.7 Pin Clock Speed Control (CLOCK_OUT)

Address: 0x18107020
Access: Read/Write
Reset: See field description

This register controls the CLK_OUT pin clock speed. The output clock can be used for testing or to drive external components.

Bit	Bit Name	Reset	Description	
31:7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
6:4	DELAY	0x00000000	Controls the tap selection point for CLK_OUT on a delay line when SELECT[2] is set. 000 corresponds to the least delay while 111 corresponds to the maximum display (100 to 180 degree delay).	
3:0	SELECT	0x00000000	Controls the CLK_OUT speed. The binary MUX select decode is as follows:	
			0000	Low
			0001	CLKOBSOUT (from the PCIE PHY)
			0010	CLK80_ADC
			0011	CLK160_DAC
			0100	LCL20A (delayed as specified by the DELAY field)
			0101	LCL40A (delayed as specified by the DELAY field)
			0110	LCL80A (delayed as specified by the DELAY field)
			0111	LCL160A (delayed as specified by the DELAY field)
			1000	CLK128
			1001	XTLCLK
			1010	CLK80_ADC
			1011	CLK160_DAC
			1100	RTC_CLK_W (delayed as specified by the DELAY field)
			1101	REFCLK_W (delayed as specified by the DELAY field)
			1110	PCI_CLK_W (delayed as specified by the DELAY field)
			1111	PCIE_CORE_CLK_W (delayed as specified by the DELAY field)

10.19.8 Reset Cause (RESET_CAUSE)

Address: 0x18107028
Access: Read/Write
Reset: See field description

This register holds the cause of the last reset event.

Bit	Bit Name	Reset	Description	
31:2	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
1:0	LAST	0x00000000	The value of this register holds the cause of the last reset, as stated:	
			0	Hard reset of the RTC
			1	Software wrote to the RTC_CONTOL_COLD_RST register
			2	Software wrote to the RTC_CONTOL_WARM_RST register
			3	Reserved

10.19.9 System Sleep Status (SYSTEM_SLEEP)

Address: 0x1810702C
Access: Read/Write
Reset: See field description

This register contains the system sleep status bits. System sleep state is entered when all high frequency clocks are gated and the high frequency crystal is shut down. This register is used to indicate the status of each sleep control interface. If any bit in this control register is 0, sleep is not permitted. If all bits are 1, sleep is permitted. The system will enter sleep as soon as the CPU executes a WAIT instruction. The LIGHT field will gate clocks off in SLEEP, but will keep the crystal running for faster wakeup. The DISABLE field will prevent the chip from entering SLEEP.

Bit	Bit Name	Reset	Description	
31:3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
2	MAC_IF	0x00000001	THE MAC block sleep state	
			0	The MAC block will not allow a sleep state
			1	The MAC block has enabled the sleep state
1	LIGHT	0x00000000	Controls whether or not the crystal is turned off during SLEEP. If the crystal is turned off, power consumption is lowered during sleep but the wakeup time is controlled by XTAL_SETTLE. If the crystal remains on, power consumption is higher but the wakeup time is about 45 µs.	
			0	System sleep is DEEP, resulting in minimal power consumption
			1	System sleep will be LIGHT
0	DISABLE	0x0000000	Enables or disables the system sleep	
			0	System sleep is enabled
			1	System sleep is disabled

10.19.10 Keep Awake Timer (KEEP_AWAKE)

Address: 0x18107034
Access: Read/Write
Reset: See field description

This register ensures that the chip does not enter the SLEEP state until at least the COUNT cycles have passed from the time of the last CLK_REQ event.

Bit	Bit Name	Reset	Description
31:8	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	COUNT	0x00000000	The keep awake timer measured in 32 KHz (30.5 µsecs) cycles

10.19.11 Derived RTC Clock (DERIVED_RTC_CLK)

Address: 0x18107038
Access: Read/Write
Reset: See field description

This register creates a 32 KHz clock, derived from the HF. This register controls a scaled output clock which can be used to generate lower frequency clocks based on the reference clock. For example, a 32.768 KHz clock can be generated by setting the divisor of the high speed clock accordingly. The accuracy will depend on how the divisors align with this integer count. RTC will start up normally using the derived RTC_CLK, and will switch to the LF_XTAL if it detects an LF_XTAL (this behavior can be modified using the fields in the RTC_SYNC_DERIVED register) since the external LF_XTAL is mostly unsupported.

Bit	Bit Name	Type	Reset	Description	
31:19	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
18	EXTERNAL_DETECT	RO	0x0	Detects external 32 KHz XTALs; if a LF XTAL is detected and RTC_SYNC_DERIVED clear, the RTC automatically uses the external XTAL.	
				0	No XTAL is detected
				1	LFXTAL not detected
17:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15:1	PERIOD	RW	0x262	The period of the derived clock is 2 * (PERIOD + 1). The reset value creates a 30.55 sec clock if the REFCLK is 40 MHz. The 30.5 µs value is closer to 32.768 KHz. To set it to 30.5 µs, the PERIOD value should be 0x261. To set to 30.48 µs, the PERIOD should be 0x17C. HALF_CLK_LATENCY and TSF_INC fields in MAC PCU should also be set appropriately.	
0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	

10.19.12 PLL Control (PLL_CONTROL2)

Address: 0x1810703C
Access: Read/Write
Reset: See field description

This register provides access to the PLL setup control signals for the additional bits required for the PLL.

Bit	Bit Name	Type	Reset	Description
31:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:3	DIV_FRAC	RW	0x0	Additional fractional bits
2:0	DIV_INT	RW	0x0	Additional int bits

10.19.13 RTC Sync Reset (RTC_SYNC_RESET)

Address: 0x18107040
Access: Read/Write
Reset: See field description

This register sets the RTC reset, force sleep and force wakeup.

Bit	Bit Name	Type	Reset	Description	
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	RESET	RW	0x0	Active low signal setting	
				0	RTC is currently resetting
				1	RTC is not currently resetting

10.19.14 RTC Sync Status (RTC_SYNC_STATUS)

Address: 0x18107044
Access: Read-Only
Reset: 0x0

This register denotes the current use of RTC.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PLL_ CHANGING	PLL_CHANGING signal from RTC
4	WRESET	Denotes the RTC was accessed while the MAC is asleep
3	WAKEUP_STATE	RTC is in the wakeup state
2	SLEEP_STATE	RTC is in the sleep state
1	ON_STATE	RTC is in the on state
0	SHUTDOWN_STATE	RTC is in the shutdown state

10.19.15 RTC Derived (RTC_SYNC_DERIVED)

Address: 0x18107048
Access: Read/Write
Reset: See field description

This register is for the Derived RTC.

Bit	Bit Name	Reset	Description
31:2	RSVD	0x0	Reserved
1	FORCE	0x0	Force Derived RTC
0	BYPASS	0x0	Bypass the Derived RTC

10.19.16 RTC Force Wake (RTC_SYNC_FORCE_WAKE)

Address: 0x1810704C
Access: Read/Write
Reset: See field description

This register enables a Force Wake to the MAC.

Bit	Bit Name	Reset	Description
31:2	RSVD	0x0	Reserved
1	INTR	0x1	Allows a MAC interrupt to assert a force wake enable
0	ESABLE	0x1	Enables a Force Wake to the MAC

10.19.17 RTC Interrupt Cause (RTC_SYNC_INTR_CAUSE)

Address: 0x18107050
Access: Read/Write
Reset: 0x0

This register is a controller that works the same way as the host interface interrupt controller. Each bit in the interrupt cause register pertains to an event as described here. A write of 1 to any bit in this register will clear that bit in the interrupt cause register until the corresponding event occurs again.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PLL_CHANGING	PLL_CHANGING signal received from RTC
4	SLEEP_ACCESS	RTC accessed while MAC is asleep
3	WAKEUP_STATE	RTC is in wakeup state
2	SLEEP_STATE	RTC is in sleep state
1	ON_STATE	RTC is in on state
0	SHUTDOWN_STATE	RTC is in shutdown state

10.19.18 RTC Interrupt Enable (RTC_SYNC_INTR_ENABLE)

Address: 0x18107054
Access: Read/Write
Reset: 0x0

This register is used for the RTC interrupts. Writing a 1 to any bit in this register allows that bit in the interrupt cause register to be set when the corresponding event occurs. Writing a 0 to any bit in this register will automatically clear the corresponding bit in the interrupt cause register regardless of the corresponding event.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PLL_CHANGING	PLL_CHANGING signal received from RTC
4	SLEEP_ACCESS	RTC accessed while MAC is asleep
3	WAKEUP_STATE	RTC is in wakeup state
2	SLEEP_STATE	RTC is in sleep state
1	ON_STATE	RTC is in on state
0	SHUTDOWN_STATE	RTC is in shutdown state

10.19.19 RTC Interrupt Mask (RTC_SYNC_INTR_MASK)

Address: 0x18107058
Access: Read/Write
Reset: 0x0

This register is the mask for RTC interrupts. Writing a 1 to any bit in this register will allow the corresponding event to generate an RTC Interrupt to the host interface, which can be programmed to generate a system interrupt. The corresponding bit in the RTC Interrupt Enable register must also be set.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PLL_CHANGING	PLL_CHANGING signal received from RTC
4	SLEEP_ACCESS	RTC accessed while MAC is asleep
3	WAKEUP_STATE	RTC is in wakeup state
2	SLEEP_STATE	RTC is in sleep state
1	ON_STATE	RTC is in on state
0	SHUTDOWN_STATE	RTC is in shutdown state

10.20 WPCU Registers

Table 10-21 shows the mapping of the WPCU registers.

Table 10-21 WPCU Registers

Address	Name	Description	Page
0x18108000	WMAC_PCU_STA_ADDR_L32	STA Address Lower 32 Bits	page 358
0x18108004	WMAC_PCU_STA_ADDR_U16	STA Address Upper 16 Bits	page 358
0x18108008	WMAC_PCU_BSSID_L32	BSSID Lower 32 Bits	page 359
0x1810800C	WMAC_PCU_BSSID_U16	BSSID Upper 16 Bits	page 359
0x18108010	WMAC_PCU_BCN_RSSI_AVE	Beacon RSSI Average	page 359
0x18108014	WMAC_PCU_ACK_CTS_TIMEOUT	ACK and CTS Timeout	page 360
0x18108018	WMAC_PCU_BCN_RSSI_CTL	Beacon RSSI Control	page 360
0x1810801C	WMAC_PCU_USEC_LATENCY	Millisecond Counter and Rx/Tx Latency	page 360
0x18108020	WMAC_PCU_RESET_TSF	Reset TSF	page 361
0x18108038	WMAC_PCU_MAX_CFP_DUR	Maximum CFP Duration	page 361
0x1810803C	WMAC_PCU_RX_FILTER	Rx Filter	page 362
0x18108040	WMAC_PCU_MCAST_FILTER_L32	Multicast Filter Mask Lower 32 Bits	page 363
0x18108044	WMAC_PCU_MCAST_FILTER_U32	Multicast Filter Mask Upper 32 Bits	page 363
0x18108048	WMAC_PCU_DIAG_SW	Diagnostic Switches	page 364
0x1810804C	WMAC_PCU_TSF_L32	TSF Lower 32 Bits	page 365
0x18108050	WMAC_PCU_TSF_U32	TSF Upper 32 Bits	page 365
0x1810805C	WMAC_PCU_AES_MUTE_MASK_0	AES Mute Mask 0	page 365
0x18108060	WMAC_PCU_AES_MUTE_MASK_1	AES Mute Mask 1	page 365
0x18108064	MAC_PCU_GATED_CLKS	Gated Clocks	page 366
0x18108070	DYM_MIMO_PWR_SAVE	Dynamic MIMO Power Save	page 366
0x18108080	WMAC_PCU_LAST_BEACON_TSF	Last Receive Beacon TSF	page 366
0x18108084	WMAC_PCU_NAV	Current NAV	page 367
0x18108088	WMAC_PCU_RTS_SUCCESS_CNT	Successful RTS Count	page 367
0x1810808C	WMAC_PCU_RTS_FAIL_CNT	Failed RTS Count	page 367
0x18108090	WMAC_PCU_ACK_FAIL_CNT	FAIL ACK Count	page 367
0x18108094	WMAC_PCU_FCS_FAIL_CNT	Failed FCS Count	page 368
0x18108098	WMAC_PCU_BEACON_CNT	Beacon Count	page 368
0x181080A0	MAC_PCU_BASIC_SET	BASIC MCS Set	page 368
0x181080A4	MGMT_SEQ	Management Sequence Threshold	page 369
0x181080D4	WMAC_PCU_SLP1	Sleep 1	page 369
0x181080D8	WMAC_PCU_SLP2	Sleep 2	page 370
0x181080E0	WMAC_PCU_ADDR1_MASK_L32	Address 1 Mask Lower 32 Bits	page 370
0x181080E4	WMAC_PCU_ADDR1_MASK_U16	Address 1 Mask Upper 16 Bits	page 370
0x181080E8	WMAC_PCU_TPC	Tx Power Control	page 371
0x181080EC	WMAC_PCU_TX_FRAME_CNT	Tx Frame Counter	page 371
0x181080F0	WMAC_PCU_RX_FRAME_CNT	Rx Frame Counter	page 371
0x181080F4	WMAC_PCU_RX_CLEAR_CNT	Rx Clear Counter	page 372

Table 10-21 WPCU Registers (cont.)

Address	Name	Description	Page
0x181080F8	WMAC_PCU_CYCLE_CNT	Cycle Counter	page 372
0x181080FC	WMAC_PCU_QUIET_TIME_1	Quiet Time 1	page 372
0x18108100	WMAC_PCU_QUIET_TIME_2	Quiet Time 2	page 373
0x18108108	WMAC_PCU_QOS_NO_ACK	QoS NoACK	page 373
0x1810810C	WMAC_PCU_PHY_ERROR_MASK	PHY Error Mask	page 374
0x18108114	WMAC_PCU_RXBUF	Rx Buffer	page 374
0x18108118	WMAC_PCU_MIC_QOS_CONTROL	QoS Control	page 375
0x1810811C	WMAC_PCU_MIC_QOS_SELECT	Michael QoS Select	page 375
0x18108120	WMAC_PCU_MISC_MODE	Miscellaneous Mode	page 376
0x18108124	WMAC_PCU_FILTER_OFDM_CNT	Filtered OFDM Counter	page 377
0x18108128	WMAC_PCU_FILTER_CCK_CNT	Filtered CCK Counter	page 378
0x1810812C	WMAC_PCU_PHY_ERR_CNT_1	PHY Error Counter 1	page 378
0x18108130	WMAC_PCU_PHY_ERR_CNT_1_MASK	PHY Error Counter 1 Mask	page 378
0x18108134	WMAC_PCU_PHY_ERR_CNT_2	PHY Error Counter 2	page 379
0x18108138	WMAC_PCU_PHY_ERR_CNT_2_MASK	PHY Error Counter 2 Mask	page 379
0x1810813C	WMAC_PCU_TSF_THRESHOLD	TSF Threshold	page 379
0x18108144	WMAC_PCU_PHY_ERROR_EIFS_MASK	PHY Error EIFS Mask	page 380
0x18108168	WMAC_PCU_PHY_ERR_CNT_3	PHY Error Counter 3	page 380
0x1810816C	WMAC_PCU_PHY_ERR_CNT_3_MASK	PHY Error Counter 3 Mask	page 380
0x18108180	WMAC_PCU_GENERIC_TIMERS2	MAC PCU Generic Timers 2	page 380
0x181081C0	WMAC_PCU_GENERIC_TIMERS2_MODE	MAC PCU Generic Timers Mode 2	page 381
0x181081D0	WMAC_PCU_TXSIFS	SIFS, Tx Latency and ACK Shift	page 381
0x181081EC	WMAC_PCU_TXOP_X	TXOP for Non-QoS Frames	page 382
0x181081F0	WMAC_PCU_TXOP_0_3	TXOP for TID 0 to 3	page 382
0x181081F4	WMAC_PCU_TXOP_4_7	TXOP for TID 4 to 7	page 382
0x181081F8	WMAC_PCU_TXOP_8_11	TXOP for TID 8 to 11	page 383
0x181081FC	WMAC_PCU_TXOP_12_15	TXOP for TID 0 to 3	page 383
0x18108200	WMAC_PCU_GENERIC_TIMERS[0:15]	Generic Timers	page 384
0x18108240	WMAC_PCU_GENERIC_TIMERS_MODE	Generic Timers Mode	page 384
0x18108244	WMAC_PCU_SLP32_MODE	32 KHz Sleep Mode	page 385
0x18108248	WMAC_PCU_SLP32_WAKE	32 KHz Sleep Wake	page 385
0x1810824C	WMAC_PCU_SLP32_INC	32 KHz Sleep Increment	page 386
0x18108250	WMAC_PCU_SLP_MIB1	Sleep MIB Sleep Count	page 386
0x18108254	WMAC_PCU_SLP_MIB2	Sleep MIB Cycle Count	page 387
0x18108258	WMAC_PCU_SLP_MIB3	Sleep MIB Control Status	page 387
0x1810825C	WMAC_PCU_WOW1	MAC PCU Wake-on-Wireless (WoW) 1	page 388
0x18108260	WMAC_PCU_WOW2	MAC PCU WOW 2	page 388
0x18108270	WMAC_PCU_WOW3_BEACON_FAIL	MAC PCU WoW Beacon Fail Enable	page 388
0x18108274	WMAC_PCU_WOW3_BEACON	MAC PCU WoW Beacon Fail Timeout	page 389
0x18108278	WMAC_PCU_WOW3_KEEP_ALIVE	MAC PCU WoW Keep Alive Timeout	page 389

Table 10-21 WPCU Registers (cont.)

Address	Name	Description	Page
0x1810827C	WMAC_PCU_WOW_KA	MAC PCU WoW Automatic Keep Alive Disable	page 389
0x18108294	PCU_WOW4	WoW Offset 1	page 389
0x18108288	KA	WoW Keep-Alive Frames Delay	page 390
0x1810828C	WOW_EXACT	WoW Exact Length and Offset	page 390
0x18108294	PCU_WOW4	WoW Offset 1	page 390
0x18108298	PCU_WOW5	WoW Offset 2	page 391
0x1810829C	PHY_ERR_CNT_MASK_CONT	PHY Error Counter Continued	page 391
0x18108318	WMAC_PCU_20_40_MODE	Global Mode	page 392
0x18108328	WMAC_PCU_RX_CLEAR_DIFF_CNT	Difference RX_CLEAR Counter	page 392
0x1810832C	SELF_GEN_ANTENNA_MASK	Self Generated Antenna Mask	page 393
0x18108330	WMAC_PCU_BA_BAR_CONTROL	Control Registers for Block BA Control Fields	page 393
0x18108334	WMAC_PCU_LEGACY_PLCP_SPOOF	Legacy PLCP Spoof	page 394
0x18108338	WMAC_PCU_PHY_ERROR_MASK_CONT	PHY Error Mask and EIFS Mask	page 394
0x1810833C	WMAC_PCU_TX_TIMER	Tx Timer	page 395
0x18108340	TXBUF_CTRL	Transmit Buffer Control	page 395
0x18108348	ALT_AES_MUTE_MASK	Alternate AES QoS Mute Mask	page 396
0x1810834C	WMAC_PCU_WOW6	MAC PCU WoW 6	page 396
0x1810835C	WMAC_PCU_WOW5	MAC PCU WoW 5	page 396
0x18108360	WMAC_PCU_WOW_LENGTH1	Length of Pattern Match for Pattern 0	page 397
0x18108364	WMAC_PCU_WOW_LENGTH2	Length of Pattern Match for Pattern 1	page 397
0x18108368	WOW_PATTERN_MATCH_LESS_THAN_256_BYTES	Enable Control for Pattern Match Feature of WOW	page 397
0x18108370	WMAC_PCU_WOW4	MAC PCU WoW 4	page 398
0x18108374	WOW2_EXACT	Exact Length and Offset Requirement Flag for WoW Patterns	page 398
0x18108378	PCU_WOW6	WoW Offset 2	page 398
0x1810837C	PCU_WOW7	WoW Offset 3	page 398
0x18108380	WMAC_PCU_WOW_LENGTH3	Length of Pattern Match for Pattern 0	page 399
0x18108384	WMAC_PCU_WOW_LENGTH4	Length of Pattern Match for Pattern 0	page 399
0x1810838C	MAC_PCU_LOCATION_MODE_TIMER	MAC PCU TIMER for Location Mode	page 399
0x18108390	TSF2_L32	TSF 2 Lower 32	page 399
0x18108394	TSF2_U32	TSF 2 Upper 32	page 400
0x18108398	BSSID2_L32	BSSID 2 Lower 32	page 400
0x1810839C	BSSID2_U16	BSSID 2 Upper 16	page 400
0x181083A4	WMAC_PCU_TID_TO_AC	TID Value Access Category	page 400
0x181083A8	WMAC_PCU_HP_QUEUE	High Priority Queue Control	page 401
0x181083C8	WMAC_PCU_HW_BCN_PROC1	Hardware Beacon Processing 1	page 402
0x181083CC	WMAC_PCU_HW_BCN_PROC2	Hardware Beacon Processing 2	page 402
0x18108800	WMAC_PCU_KEY_CACHE[0:1023]	Key Cache	page 403

10.20.1 STA Address Lower 32 Bits (WMAC_PCU_STA_ADDR_L32)

Offset: 0x18108000

Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	ADDR_31_0	Lower 32 bits of STA MAC address (PCU_STA_ADDR[31:0])

10.20.2 STA Address Upper 16 Bits (WMAC_PCU_STA_ADDR_U16)

Offset: 0x18108004
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

This register contains the lower 32 bits of the STA address.

Bit	Name	Reset	Description
31	REG_ADHOC_MCAST_SEARCH	0x0	Enables the key cache search for ad hoc MCAST packets
30	PCU_CBCIV_ENDIAN	0x0	Endianess of IV in CBC nonce
29	REG_PRESERVE_SEQNUM	0x1	Stops PCU from replacing the sequence number
28	PCU_KSRCH_MODE	0x0	Search key cache first. If not, match use offset for IV = 0, 1, 2, 3. ■ If KSRCH_MODE = 0 then do not search ■ If IV = 1, 2, or 3, then search ■ If IV = 0, do not search
27	REG_CRPT_MIC_ENABLE	0x0	Enables the checking and insertion of MIC in TKIP
26	SECTOR_SELF_GEN	0x0	Use the default antenna for self-generated frames
25	PCU_BSRATE_11B	0x0	802.11b base rate 0 Use all rates 1 Use only 1–2 MBps
24	PCU_ACKCTS_6MB	0x0	Use 6 MBps rate for ACK and CTS
23	RTS_USE_DEF	0x0	Use the default antenna to send RTS
22	DEFANT_UPDATE	0x0	Update the default antenna with the Tx antenna
21	USE_DEFANT	0x0	When the descriptor chooses auto-select mode (0000), use the default antenna to transmit
20	PCU_PCF	0x0	Set if associated AP is PCF capable
19	KEYSRCH_DIS	0x0	Disable key search
18	PW_SAVE	0x0	Set if STA is in power-save mode
17	PCU_ADHOC	0x0	Set if STA is in an ad hoc network
16	PCU_AP	0x0	Set if STA is an AP
15:0	PCU_STA_ADDR[47:32]	0x0	Upper 16 bits of STA MAC address

10.20.3 BSSID Lower 32 Bits (WMAC_PCU_BSSID_L32)

Offset: 0x18108008
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

This register contains the lower 32 bits of the BSS identification information.

Bit	Name	Description
31:0	pcu_bssid[31:0]	Lower 32 bits of BSSID

10.20.4 BSSID Upper 16 Bits (WMAC_PCU_BSSID_U16)

Offset: 0x1810800C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0
This register contains the upper 32 bits of the BSS identification information.

Bit	Name	Description
31:17	RES	Reserved
26:16	PCU_AID	Association ID
15:0	PCU_BSSID[47:32]	Upper 16 bits of BSSID

10.20.5 Beacon RSSI Average (WMAC_PCU_BCN_RSSI_AVE)

Offset: 0x18108010
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x800
BCN_RSSI_AVE

Bit	Name	Description
31:12	RES	Reserved
11:0	REG_BCN_RSSI_AVE	Holds the average RSSI with 1/16 dB resolution. The RSSI is averaged over multiple beacons which matched our BSSID. AVE_VALUE is 12 bits with 4 bits below the normal 8 bits. These lowest 4 bits provide for a resolution of 1/16 dB. The averaging function is depends on the BCN_RSSI_WEIGHT; determines the ratio of weight given to the current RSSI value compared to the average accumulated value.

10.20.6 ACK and CTS Timeout (WMAC_PCU_ACK_CTS_TIMEOUT)

Offset: 0x18108014
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:30	RES	Reserved
29:16	PCU_CTS_TIMEOUT	Timeout while waiting for CTS (in cycles)
15:14	RES	Reserved
13:0	PCU_ACK_TIMEOUT	Timeout while waiting for ACK (in cycles)

10.20.7 Beacon RSSI Control (WMAC_PCU_BCN_RSSI_CTL)

Offset: 0x18108018
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:30	RES	Reserved
29	REG_BCN_RSSI_RST_ STROBE	The BCN_RSSI_RESET clears BCN_RSSI_AVE, page 10-359 to aid in changing channels
28:24	REG_BCN_RSSI_WEIGHT	Used to calculate BCN_RSSI_AVE, page 10-359
23:16	RES	Reserved
15:8	PCU_BCN_MISS_THR	Threshold at which the beacon miss interrupt asserts. Because the beacon miss counter increments at TBTT, it increments to 1 before the first beacon.
7:0	PCU_RSSI_THR	The threshold at which the beacon low RSSI interrupt is asserted when the average RSSI (BCN_RSSI_AVE, page 10-359) below this level

10.20.8 Ms Counter and Rx/Tx Latency (WMAC_PCU_USEC_ LATENCY)

Offset: 0x1810801C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Description
31:29	RES	Reserved
28:23	PCU_RXDELAY	Baseband Rx latency to start of SIGNAL (in µs)
22:14	PCU_TXDELAY	Baseband Tx latency to start of timestamp in beacon frame (in µs)
13:8	RES	Reserved
7:0	USEC	USEC defines the number of clock cycles minus 1 in 1 microsecond. For example, 40 cycles of a 40 MHz clock is 1 µsec, so this register would be programmed to be 39. If the clock frequency is 40 5/9 MHz, the fractional components need to be defined. In this case the numerator (register: MAC_PCU_MAX_CFP_DUR, field: USEC_FRAC_ NUMERATOR) should be set to 5 and the denominator (register: MAC_PCU_MAX_CFP_ DUR, field: USEC_FRAC_DENOMINATOR) should be set to 9. The USEC field would still be 39. Note that the D_GBL_IFS_MISC register, microsecond duration field in the DMA block has been removed and the function is now shared with the PCU logic.

10.20.9 Reset TSF (WMAC_PCU_RESET_TSF)

Offset: 0x18108020
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Controls beacon operation by the PCU.

Bit	Name	Description
31:26	RES	Reserved
25	ONE_SHOT2	Setting this bit causes the TSF2 to reset. This register clears immediately after reset.
24	ONE_SHOT	Setting this bit causes the TSF to reset. This register clears immediately after reset.
23:0	RES	Reserved

10.20.10 Maximum CFP Duration (WMAC_PCU_MAX_CFP_DUR)

Offset: 0x18108038
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Contains the maximum time for a contention free period.

Bit	Name	Description
31:28	RES	Reserved
27	USEC_FRAC _DENOMINATOR[27:24]	See description for USEC[7:0] in Ms Counter and Rx/Tx Latency (WMAC_ PCU_USEC_LATENCY)
23:20	RES	Reserved
16:16	USEC_FRAC _DENOMINATOR[19:16]	See description for USEC[7:0] in Ms Counter and Rx/Tx Latency (WMAC_ PCU_USEC_LATENCY)
15:0	VALUE[15:0]	Maximum contention free period duration (in µs)

10.20.11 Rx Filter (WMAC_PCU_RX_FILTER)

Offset: 0x1810803C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

This register determines Rx frame filtering.

NOTE If any bit is set, the corresponding packet types pass the filter and DMA. All filter conditions except the promiscuous setting rely on the no early PHY error and protocol version being checked to ensure it is version 0.

Bit	Name	Reset	Description
31:20	RES	0x0	Reserved
19	CONTROL_ WRAPPER	0x1	Enable receiving directed frames for control wrapper frames
18	MGMT_ACTION_ MCAST	0x0	Enable receive of multicast frames for management action frames
17	HW_BCN_PROC _ENABLE	0x0	If set, the beacon frame with matching BSSID is filtered per hardware beacon processing logic. See the HW_BCN_PROC register.
16	RST_DLMTR_CNT _DISABLE	0x0	Clearing this bit resets the ST_DLMTR_CNT to 0 when RXSM.STATE leaves the START_DELIMITER state.
15	MCAST_BCAST_ALL	0x0	Enables receipt of all multicast and broadcast frames
14	PS_POLL	0x0	Enables receipt of PS-POLL
13	ASSUME_RADAR	0x1	If set, a legacy PLCP rate of 0 indicates a radar packet that will not be filtered
12	UNCOMPRESSED_ BA_BAR	0x0	Uncompressed directed block ACK request or block ACK
11	COMPRESSED_BA	0x0	Compressed directed block ACK
10	COMPRESSED_BAR	0x0	Compressed directed block ACK request
9	MY_BEACON	0x0	Retrieves any beacon frame with matching SSID
8	RES	0x0	Reserved
7	PROBE_REQ	0x0	Probe request enable; enables reception of all probe request frames
6	XR_POLL	0x0	Any multicast or broadcast frame with a frame type matching the XR_POLL_ TYPE register
5	PROMISCUOUS	0x0	Promiscuous Rx enable; enables reception of all frames, including errors
4	BEACON	0x0	Beacon frame enable; enables reception of beacon frames.
3	CONTROL	0x0	Control frame enable; enables reception of control frames
2	BROADCAST	0x0	Broadcast frame enable; enables reception of non beacon broadcast frames that originate from the BSS whose ID matches BSSID
1	MULTICAST	0x0	Multicast frame enable; enables reception of multicast frames that match the multicast filter
0	UNICAST	0x0	Unicast frame enable; enables reception of unicast (directed) frames that match the STA address

10.20.12 Multicast Filter Mask Lower 32 Bits (WMAC_PCU_MCAST_FILTER_L32)

Offset: 0x18108040
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PCU_MCAST_MASK	Multicast filter mask low. Lower 32 bits of multicast filter mask.

10.20.13 Multicast Filter Mask Upper 32 Bits (WMAC_PCU_MCAST_FILTER_U32)

Offset: 0x18108044
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PCU_MCAST_MASK	Multicast filter mask high. Upper 32 bits of multicast filter mask.

10.20.14 Diagnostic Switches (WMAC_PCU_DIAG_SW)

Offset: 0x18108048

Access: Hardware = Read-Only

Software = Read/Write

Reset Value: 0x0

Controls the operation of the PCU, including enabling/disabling acknowledgements, CTS, transmission, reception, encryption, loopback, FCS, channel information, and scrambler seeds.

Bit	Name	Description
31:30	RES	Reserved
29	RX_CLEAR_EXT_LOW	Force the RX_CLEAR_EXT signal to appear to the MAC as being low
28	RX_CLEAR_CTL_LOW	Force the RX_CLEAR_CTL signal to appear to the MAC as being low
27	OBS_SEL_2	Observation point select.
26	SATURATE_CYCLE_CNT	The saturate cycle count bit, if set, causes the Cycle Counter (WMAC_PCU_CYCLE_CNT) register to saturate instead of shifting to the right by 1 every time the count reaches 0xFFFFFFFF. This saturate condition also holds the RX_CLEAR, RX_FRAME, and TX_FRAME counts.
25	FORCE_RX_ABORT	Force Rx abort bit in conjunction with Rx block aids quick channel change to shut down Rx. The force Rx abort bit kills with the Rx_abort any frame currently transferring between the MAC and baseband. while the RX block bit prevents any new frames from getting started.
24	DUAL_CHAIN_CHAN_INFO	Dual chain channel information
23	PHYERR_ENABLE_EIFS_CTL	Used frame and WAIT_WEP in the PCU_RX_ERR logic if this bit is set to 0
22	CHAN_IDLE_HIGH	Force channel idle high
21	IGNORE_NAV	Ignore virtual carrier sense (NAV)
20	RX_CLEAR_HIGH	Force RX_CLEAR high
19:18	OBS_SEL_1	Observation point select
17	ACCEPT_NON_V0	Enable or disable protocol field
16:9	RES	Reserved
8	DUMP_CHAN_INFO	Dump channel information
7	CORRUPT_FCS	Corrupt FCS
6	LOOP_BACK	Enable or disable Tx data loopback
5	HALT_RX	Enable or disable reception
4	NO_DECRYPT	Enable or disable decryption
3	NO_ENCRYPT	Enable or disable encryption
2	NO_CTS	Enable or disable CTS generation
1	NO_ACK	Enable or disable acknowledgement generation for all frames
0	PCU_INVALKEY_NOACK	Enable or disable acknowledgement when a valid key is not found for the received frames in the key cache.

10.20.15 TSF Lower 32 Bits (WMAC_PCU_TSF_L32)

Offset: 0x1810804C

Access: Hardware = Read/Write

Software = Read/Write

Reset Value: 0xFFFFFFF

Bit	Name	Description
31:0	VALUE	The timestamp value in µs. Writes to this register do not cause the TSF to change. Rather, the value is held in a temporary staging area until this register is written, at which point both the lower and upper parts of the TSF are loaded. A read result of 0xFFFFFFFF indicates that the read occurred before TSF logic came out of sleep. It may take up to 45 µs after the chip is brought out of sleep for the TSF logic to wake.

10.20.16 TSF Upper 32 Bits (WMAC_PCU_TSF_U32)

Offset: 0x18108050

Access: Hardware = Read/Write

Software = Read/Write

Reset Value: 0xFFFFFFF

Bit	Name	Description
31:0	VALUE	The timestamp value in µs

10.20.17 AES Mute Mask 0 (WMAC_PCU_AES_MUTE_MASK_0)

Offset: 0x1810805C

Access: Hardware = Read-Only

Software = Read/Write

Reset Value: See field description

Bit	Name	Reset	Description
31:16	QOS_MUTEMASK	0xFFFF	AES mute mask for TID field
15:0	FC_MUTEMASK	0x478F	AES mute mask for frame control field

10.20.18 AES Mute Mask 1 (WMAC_PCU_AES_MUTE_MASK_1)

Offset: 0x18108060

Access: Hardware = Read-Only

Software = Read/Write

Reset Value: See field description

Bit	Name	Reset	Description
31:16	FC_MGMT	0xE7FF	AES mute mask for management frame control field
15:0	SEQ_MUTEMASK	0x000F	AES mute mask for sequence number field

10.20.19 Gated Clocks (MAC_PCU_GATED_CLKS)

Address: 0x18108064
Access: Read/Write
Reset: 0x0

This register forces enabling a clock domain to be on. Clearing these bits causes the interface to use the existing enable logic.

Bit	Bit Name	Description
31:4	RES	Reserved
3	GATED_REG	Controls clock enable for PCU_OCBINT which is normally controlled by PCU_ REGCLKEN
2	GATED_RX	Controls clock enable for PCU_RXSM which is normally controlled by PCU_RXCLKEN
1	GATED_TX	Controls clock enable for PCU_TXSM which is normally controlled by PCU_TXCLKEN
0	RES	Reserved

10.20.20 Dynamic MIMO Power Save (DYM_MIMO_PWR_SAVE)

Address: 0x18108070
Access: Read/Write
Reset: See field description

This register is for the MAC PCU dynamic MIMO power save.

Bit	Bit Name	Reset	Description
31:11	RES	0x0	Reserved
10:8	HI_PWR_CHAIN_MASK	0x3	The high power setting of the Rx chain mask
7	RES	0x0	Reserved
6:4	LOW_PWR_CHAIN_ MASK	0x1	The low power setting of the Rx chain mask
3	RES	0x0	Reserved
2	SW_CHAIN_MASK_SEL	0x0	The software selection of the dynamic MIMO power save
1	HW_CTRL_EN	0x0	Enable the hardware control of the dynamic MIMO power save
0	USE_MAC_CTRL	0x0	The Rx chain mask will be controlled by MAC

10.20.21 Last Receive Beacon TSF (MAC_PCU_LAST_BEACON_TSF)

Offset: 0x18108080
Access: Hardware = Write-only
Software = Read-Only
Reset Value: 0x0

This threshold register indicates the minimum amount of data required before initiating a transmission.

Bit	Name	Description
31:0	LAST_TSTP	Beacon timestamp. Lower 32 bits of timestamp of the last beacon received.

10.20.22 Current NAV (WMAC_PCU_NAV)

Offset: 0x18108084
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:26	RES	Reserved
25:0	CS_NAV	Current NAV value (in µs)

10.20.23 Successful RTS Count (WMAC_PCU_RTS_SUCCESS_CNT)

Offset: 0x18108088
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of successful RTS exchanges. The counter stops at 0xFFFF. After a read, automatically resets to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	RTS_OK	RTS/CTS exchange success counter

10.20.24 Failed RTS Count (WMAC_PCU_RTS_FAIL_CNT)

Offset: 0x1810808C
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of failed RTS exchanges. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	RTS_FAIL	RTS/CTS exchange failure counter

10.20.25 FAIL ACK Count (WMAC_PCU_ACK_FAIL_CNT)

Offset: 0x18108090
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of failed acknowledgements. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	ACK_FAIL	DATA/ACK failure counter

10.20.26 Failed FCS Count (WMAC_PCU_FCS_FAIL_CNT)

Offset: 0x18108094
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of failed frame check sequences. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	FCS_FAIL	FCS failure counter

10.20.27 Beacon Count (WMAC_PCU_BEACON_CNT)

Offset: 0x18108098
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of valid beacon frames received. The counter stops at 0xFFFF. After a read, automatically resets to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	BEACONCNT	Valid beacon counter

10.20.28 BASIC MCS Set (MAC_PCU_BASIC_SET)

Address: 0x181080A0
Access: Read/Write
Reset: 0x0

This register is the basic set from MCS0 to MCS31.

Bit	Bit Name	Description
31:0	MCS	The basic set for MCS 0 to 31. Bit [0] is for MCS0, Bit [1] is for MCS1, etc. Each bit is individually set for each MCS

10.20.29 Management Sequence Threshold (MGMT_SEQ)

Address: 0x181080A4
Access: Read/Write
Reset: See field description

This register configures the threshold of minimum and maximum values for inserting sequence numbers into management packets (ie. V/CV report of Action No ACK frame) which is self-generated by HW. For example, MAC_PCU_MGMT_SEQ_MIN= 0x20 and MAC_PCU_MGMT_SEQ_MAX= 0x60, so the sequence number will be inserted cyclically as 0x20, 0x21..., 0x60, and so on.

Bit	Bit Name	Reset	Description
31:28	RES	0x0	Reserved
27:16	MAX	0x2FF	Maximum value for inserting sequence numbers into management packets
15:12	RES	0x0	Reserved
11:0	MAX	0x0	Maximum value for inserting sequence numbers into management packets

10.20.30 MAC PCU Sleep 1 (SLP1)

Offset: 0x181080D4
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

The Sleep 1 register in conjunction with the Sleep 2 (WMAC_PCU_SLP2) register, controls when the QCA9558 should wake when waiting for AP Rx traffic. Sleep registers are only used when the QCA9558 is in STA mode.

Bit	Name	Reset	Description
31:21	CAB_TIMEOUT	0x5	Time in 1/8 TU the PCU waits for CAB after receiving the beacon or the previous CAB; insures that if no CAB is received after the beacon or if a long gap occurs between CABs, CAB powersave state returns to idle.
20	RES	0x0	Reserved
19	ASSUME_DTIM	0x0	A mode bit which indicates whether to assume a beacon was missed when the SLP_BEACON_TIMEOUT occurs with no received beacons, in which case is assumes the DTIM was missed, and waits for CAB.
18:0	RES	0x0	Reserved

10.20.31 Sleep 2 (WMAC_PCU_SLP2)

Offset: 0x181080D8
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x2

Bit	Name	Description
31:21	BEACON_TIMEOUT	Time in 1/8 TU that the PCU waits for a beacon after waking up. If this time expires, the PCU woke due to SLP_NEXT_DTIM, and SLP_ASSUME_DTIM is active, then it assumes the beacon was missed and goes directly to watching for CAB. Otherwise when this time expires, the beacon powersave state returns to idle.
20:0	RES	Reserved

10.20.32 Address 1 Mask Lower 32 Bits (WMAC_PCU_ADDR1_MASK_L32)

Offset: 0x181080E0

Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0xFFFFFFFF

This STA register provides multiple BSSID support when the QCA9558 is in AP mode.

Bit	Name	Description
31:0	STA_MASK_L	STA address mask lower 32-bit register. Provides multiple BSSID support.

10.20.33 Address 1 Mask Upper 16 Bits (WMAC_PCU_ADDR1_MASK_U16)

Offset: 0x181080E4

Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0xFFFF

This STA register provides multiple BSSID support when the QCA9558 is in AP mode.

Bit	Name	Description
31:16	RES	Reserved
15:0	STA_MASK_L	STA address mask upper 16-bit register. Provides multiple BSSID support.

10.20.34 Tx Power Control (WMAC_PCU_TPC)

Offset: 0x181080E8

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x3F

The 6-bit Tx power control sent from the MAC to the baseband is typically controlled using the Tx descriptor field. But self-generated response frames such as ACK, CTS, and chirp that do not have a Tx descriptor use the values in the Tx power control register instead.

Bit	Name	Description
31:30	RES	Reserved
29:24	RPT_PWR	Tx power control for self-generated action/NoACK frame
23:22	RES	Reserved
21:16	CHIRP_PWR	Tx power control for chirp
15:14	RES	Reserved
13:8	CTS_PWR	Tx power control for CTS
7:6	RES	Reserved
5:0	ACK_PWR	Tx power control for ACK

10.20.35 Tx Frame Counter (WMAC_PCU_TX_FRAME_CNT)

Offset: 0x181080EC

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

The Tx frame counter counts the number of cycles the TX_FRAME signal is active.

Bit	Name	Description
31:0	TX_FRAME_CNT	Counts the number of cycles the TX_FRAME signal is active

10.20.36 Rx Frame Counter (WMAC_PCU_RX_FRAME_CNT)

Offset: 0x181080F0

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

The receive frame counter counts the number of cycles the RX_FRAME signal is active.

Bit	Name	Description
31:0	RX_FRAME_CNT	Counts the number of cycles the RX_FRAME signal is active

10.20.37 Rx Clear Counter (WMAC_PCU_RX_CLEAR_CNT)

Offset: 0x181080F4

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

The receive clear counter counts the number of cycles the RX_CLEAR signal is not active.

Bit	Name	Description
31:0	RX_CLEAR_CNT	Counts the number of cycles the RX_CLEAR signal is low (not active)

10.20.38 Cycle Counter (WMAC_PCU_CYCLE_CNT)

Offset: 0x181080F8

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

The cycle counter counts the number of clock cycles.

Bit	Name	Description
31:0	CYCLE_CNT	Counts the number of clock cycles

10.20.39 Quiet Time 1 (WMAC_PCU_QUIET_TIME_1)

Offset: 0x181080FC

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: See field description

The Quiet Time registers implement the quiet time function specified in the proposed 802.11h extension supporting radar detection.

Bit	Name	Reset	Description
31:18	RES	0x0	Reserved
17	QUIET_ACK_CTS_ENABLE	0x1	If set, then the MAC sends an ACK or CTS in response to a received frame
16:0	RES	0x0	Reserved

10.20.40 Quiet Time 2 (WMAC_PCU_QUIET_TIME_2)

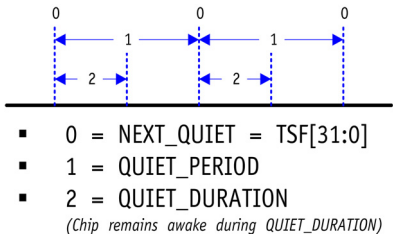
Offset: 0x18108100

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

The Quiet Time registers implement the quiet time function specified in the proposed 802.11h extension supporting radar detection.

NOTE QUIET_ENABLE is implemented as GENERIC_TIMER_ENABLE and NEXT_QUIET as GENERIC_TIMER_NEXT. QUIET_PERIOD is implemented as GENERIC_TIMER_PERIOD.



Bit	Name	Description
31:16	QUIET_DURATION	The length of time in TUs (TU = 1024 µs) that the chip is required to be quiet
15:0	RES	Reserved

10.20.41 QoS NoACK (WMAC_PCU_QOS_NO_ACK)

Offset: 0x18108108

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x52

This register provides a mechanism to locate the NoACK information in the QoS field and determine which encoding means NoACK.

Bit	Name	Reset	Description	
31:9	RES	0x0	Reserved	
8:7	NOACK_ BYTE_ OFFSET	0x0	Number of bytes from the byte after end of the header of a data packet to the byte location where NoACK information is stored. (The end of the header is at byte offset 25 for 3-address packets and 31 for 4-address packets.)	
6:4	NOACK_BIT_ OFFSET	0x5	Offsets from the byte where the NoACK information should be stored; offset can range from 0 to 6 only	
3:0	NOACK_2_ BIT_VALUES	0x2	These values are of a two bit field that indicate NoACK	
			NOACK_2_BIT_VALUE	**Encoding Matching NoACK**
			xxx1	00
			xx1x	01
			x1xx	10
			1xxx	11

10.20.42 PHY Error Mask (WMAC_PCU_PHY_ERROR_MASK)

Offset: 0x1810810C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x2

NOTE Provides the ability to choose which PHY errors to filter from the BB; the number offsets into this register. If the mask value at the offset is 0, the error filters and does not show on the Rx queue.

Bit	Name	Description
31	ERROR CCK RESTART	CCK restart error
30	ERROR CCK SERVICE	CCK service error
29:28	RES	Reserved
27	ERROR CCK RATE_ILLEGAL	CCK illegal rate error
26	ERROR CCK HEADER_CRC	CCK CRC header error
25	ERROR CCK TIMING	False detection for CCK
24	RES	Reserved
23	ERROR OFDM RESTART	OFDM restart error
22	ERROR OFDM SERVICE	OFDM service error
21	ERROR OFDM POWER_DROP	OFDM power drop error
20	ERROR OFDM LENGTH_ILLEGAL	OFDM illegal length error
19	ERROR OFDM RATE_ILLEGAL	OFDM illegal rate error
18	ERROR OFDM SIGNAL_PARITY	OFDM signal parity error
17	ERROR OFDM TIMING	False detection for OFDM
16:8	RES	Reserved
7	ERROR TX_INTERRUPT_RX	Transmit interrupt
6	ERROR ABORT	Abort error
5	ERROR RADAR_DETECT	Radar detect error
4	ERROR PANIC	Panic error
3:1	RES	Reserved
0	ERROR TRANSMIT_UNDERRUN	Transmit underrun error

10.20.43 Rx Buffer (WMAC_PCU_RXBUF)

Offset: 0x18108114
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:12	RES	0x0	Reserved
11	REG_RD _ENABLE	0x0	When reading WMAC_PCU_BUF with this bit set, hardware returns the contents of the receive buffer.
10:0	HIGH_PRIORITY_ THRSHD	0x7FF	When number of valid entries in the receive buffer is larger than this threshold, the host interface logic gives the higher priority to receive side to prevent receive buffer overflow.

10.20.44 QoS Control (WMAC_PCU_MIC_QOS_CONTROL)

Offset: 0x18108118
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0xAA

Bit	Name	Description	
31:17	RES	Reserved	
16	MIC_QOS_ENABLE	Enable MIC QoS control	
		0	Disable hardware Michael
		1	Enable hardware Michael
15:14	MIC_QOS_CONTROL [7]	MIC QoS control [7]. See options for MIC_QOS_CONTROL [0], page 10-375.	
13:12	MIC_QOS_CONTROL [6]	MIC QoS control [6]. See options for MIC_QOS_CONTROL [0], page 10-375.	
11:10	MIC_QOS_CONTROL [5]	MIC QoS control [5]. See options for MIC_QOS_CONTROL [0], page 10-375.	
9:8	MIC_QOS_CONTROL [4]	MIC QoS control [4]. See options for MIC_QOS_CONTROL [0], page 10-375.	
7:6	MIC_QOS_CONTROL [3]	MIC QoS control [3]. See options for MIC_QOS_CONTROL [0], page 10-375.	
5:4	MIC_QOS_CONTROL [2]	MIC QoS control [2]. See options for MIC_QOS_CONTROL [0], page 10-375.	
3:2	MIC_QOS_CONTROL [1]	MIC QoS control [1]. See options for MIC_QOS_CONTROL [0], page 10-375.	
1:0	MIC_QOS_CONTROL [0]	MIC QoS control [0]	
		0	Use 0 when calculating Michael
		1	Use 1 when calculating Michael
		2	Use MIC_QOS_SELECT when calculating Michael
		3	Use inverse of MIC_QOS_SELECT when calculating Michael

10.20.45 Michael QoS Select (WMAC_PCU_MIC_QOS_SELECT)

Offset: 0x1810811C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x3210

Bit	Name	Description
31:28	MIC_QOS_SELECT [7]	MIC QoS select [7]. Select the OOS TID bit when calculating Michael.
27:24	MIC_QOS_SELECT [6]	MIC QoS select [6]. Select the OOS TID bit when calculating Michael.
23:20	MIC_QOS_SELECT [5]	MIC QoS select [5]. Select the OOS TID bit when calculating Michael.
19:16	MIC_QOS_SELECT [4]	MIC QoS select [4]. Select the OOS TID bit when calculating Michael.
15:12	MIC_QOS_SELECT [3]	MIC QoS select [3]. Select the OOS TID bit when calculating Michael.
11:8	MIC_QOS_SELECT [2]	MIC QoS select [2]. Select the OOS TID bit when calculating Michael.
7:4	MIC_QOS_SELECT [1]	MIC QoS select [1]. Select the OOS TID bit when calculating Michael.
3:0	MIC_QOS_SELECT [0]	MIC QoS select [0]. Select the OOS TID bit when calculating Michael.

10.20.46 Miscellaneous Mode (WMAC_PCU_MISC_MODE)

Offset: 0x18108120
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:30	RES	0x0	Reserved
29	USE_EOP_PTR_ FOR_DMA_WR	0x0	When this bit is set, use LAST_EOP_PTR as an indication for DMA write When this bit is clear, use RD_PTR_TO_DMA instead.
28	ALWAYS_ PERFORM_KEY_ SEARCH	0x0	If this bit is set, key search is performed for every frame in an aggregate. If this bit is cleared, key search is only performed for the first frame of an aggregate. Unless the transmitter address is different between the frames in an aggregate. This bit has no effect on non-aggregate frame packets.
27	SEL_EVM	0x1	If set, the EVM field of the Rx descriptor status contains the EVM data received from the BB. If cleared, the EVM field of the Rx descriptor status contains 3 bytes of Legacy PLCP, 2 service bytes, and 6 bytes of HP PLCP.
26	CLEAR_BA_VALID	0x0	If set, the state of the block ACK storage is invalidated.
25	CLEAR_FIRST_HCF	0x0	If the CLEAR_FIRST_HCF bit is set then the FIRST_HCF state will be cleared. This should be set to enter fast channel change mode and cleared once fast channel change is over.
24	CLEAR_VMF	0x0	If the CLEAR_VMF bit is set then the VMF mode in the transmit state machine will be cleared. This should be set to enter fast channel change mode and cleared once fast channel change is over.
23	RX_HCF_POLL_ ENABLE	0x1	If the RX_HCF_POLL_ENABLE bit is set then the MAC is enabled to receive directed HCF polls. If this bit is not set the receive state machine will not tell the rest of the MAC that it has received a directed HCF poll.
22	HCF_POLL_ CANCELS_NAV	0x1	If the HCF_POLL_CANCELS_NAV bit is set, when a directed HCF poll is received, the current NAV is cancelled and HCF data burst can proceed at SIFS.
21	TBTT_PROTECT	0x1	If set, then the time from TBTT to 20 μs after TBTT is protected from transmit. Turn this off in ad hoc mode or if this MAC is used in the AP.
20:19	RES	0x0	Reserved
18	FORCE_QUIET_ COLLISION	0x0	If set, the PCU thinks that it is in quiet collision period, kills any transmit frame in progress, and prevents any new frame from starting.
17:15	RES	0x0	Reserved
14	MISS_BEACON_IN_ SLEEP	0x1	If the MISS_BEACON_IN_SLEEP bit is set, the missed beacon logic will not clear the missed beacon count when the chip is in sleep.
13	RES	0x0	Reserved
12	TXOP_TBTT _LIMIT_ENABLE	0x0	If this limit is set, then logic to limit the value of the duration to fit the time remaining in TXOP and time remaining until TBTT is turned on. This logic will also filter frames, which will exceed TXOP.
11	KC_RX_ANT	0x1	If KC_RX_ANT_UPDATE bit is set, the transmit antenna information in the key cache is updated based on the receive antenna results from baseband. Updates only occur when the selected antenna does not match the requested antenna which only occurs when the receive diversity is turned on in the baseband. This bit is only used with the dual chain antenna feature. The DUAL_CHAIN_ANT_MODE needs to be set to enable the KC_RX_ANT_ UPDATE.
10:7	RES	0x0	Reserved

Bit	Name	Reset	Description
6	RCV_DELAY_ SOUNDING_IM_ TXBF	0x0	If set to high, RXSM triggers SVD+ to update the CVCache when receiving a delay sounding for implicit TXBF.
5	RXSM2SVD_PRE_ RST	0x0	If set to high when packets are received, SVD is always reset.
4	CCK_SIFS_MODE	0x0	If set, the chip assumes that it is using 802.11g mode where SIFS is set to 10 μs and non-CCK frames must add 6 to SIFS to make it CCK frames. This bit is needed in duration calculation, as is the SIFS_TIME register.
3	TX_ADD_TSF	0x0	If the TX_ADD_TSF bit is set, the TSF in the transmit packet will be added to the internal TSF value for transmit beacons and prob_response frames.
2	MIC_NEW_ LOCATION_ENABLE	0x0	If MIC_NEW_LOCATION_ENABLE is set, the Tx Michael Key is assumed to be co-located in the same entry where the Rx Michael key is.
1	RES	0x0	Reserved
0	BSSID_MATCH _FORCE	0x0	If the BSSID_MATCH_FORCE bit is set, all logic based on matching the BSSID thinks that the BSSID matches.

10.20.47 Filtered OFDM Counter (WMAC_PCU_FILTER_OFDM_CNT)

Offset: 0x18108124
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The filtered OFDM counters use the MIB control signals.

Bit	Name	Description
31:24	RES	Reserved
23:0	FILTOFDM _CNT	Counts the OFDM frames that were filtered using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

10.20.48 Filtered CCK Counter (WMAC_PCU_FILTER_CCK_CNT)

Offset: 0x18108128
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:0	FILTCCK_CNT	Counts the CCK frames that were filtered using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

10.20.49 PHY Error Counter 1 (WMAC_PCU_PHY_ERR_CNT_1)

Offset: 0x1810812C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The PHY error counters count any PHY error matching the respective mask. The bits of 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to provide flexibility in counting. For example, if setting the mask bits to 0xFF0000FF, then all PHY errors from 0-7 and 24-31 are counted.

Bit	Name	Description
31:24	RES	Reserved
23:0	PHY_ERROR_CNT1	Counts any PHY error1 using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. Counter saturates at the highest value and is writable. If the upper two counter bits are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

10.20.50 PHY Error Counter 1 Mask (WMAC_PCU_PHY_ERR_CNT_1_MASK)

Offset: 0x18108130
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PHY_ERROR_CNT_MASK1	Counts any error that matches the PHY error1 mask. The values of any 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to allow counting flexibility (e.g., setting the mask to 0xFF0000FF means all PHY errors from [7:0] and [31:24] are counted).

10.20.51 PHY Error Counter 2 (WMAC_PCU_PHY_ERR_CNT_2)

Offset: 0x18108134
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:0	PHY_ ERROR_ CNT	Counts any error that matches the PHY error2 mask. The values of any 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to allow counting flexibility (e.g., setting the mask to 0xFF0000FF means all PHY errors from 0:7 and 24:31 are counted).

10.20.52 PHY Error Counter 2 Mask (WMAC_PCU_PHY_ERR_CNT_2_ MASK)

Offset: 0x18108138
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PHY_ ERROR_ CNT_MASK2	Counts any PHY error2 using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted, generating an interrupt.

10.20.53 TSF Threshold (WMAC_PCU_TSF_THRESHOLD)

Offset: 0x1810813C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0xFFFF

Bit	Name	Description
31:16	RES	Reserved
15:0	TSF_THRESHOLD	Asserts the PCU_TSF_OUT_OF_RANGE_INTER if the corrected receive TSF in a beacon is different from the internal TSF by more than this threshold.

10.20.54 PHY Error EIFS Mask (WMAC_PCU_PHY_ERROR_EIFS_MASK)

Offset: 0x18108144

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:0	VALUE	This mask provides the ability to choose which PHY errors from the baseband cause EIFS delay. The error number is used as an offset into this mask. If the mask value at the offset is 1, then this error will not cause EIFS delay.

10.20.55 PHY Error Counter 3 (WMAC_PCU_PHY_ERR_CNT_3)

Offset: 0x18108168

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:0	PHY_ERROR_CNT3	Count of PHY errors that pass the PHY_ERR_CNT_3_MASK filter

10.20.56 PHY Error Counter 3 Mask (WMAC_PCU_PHY_ERR_CNT_3_MASK)

Offset: 0x1810816C

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:0	PHY_ERROR_CNT_MASK3	Mask of the PHY error number allowed to be counted

10.20.57 MAC PCU Generic Timers 2 (WMAC_PCU_GENERIC_TIMERS2)

Offset: 0x18108180

Access: Read/Write

Reset Value: Undefined

Bit	Name	Description
31:0	DATA	WMAC_PCU_GENERIC_TIMERS

10.20.58 MAC PCU Generic Timers Mode 2 (WMAC_PCU_GENERIC_TIMERS2_MODE)

Offset: 0x181081C0
Access: See field description
Reset Value: Undefined

Bit	Name	Access	Description
31:11	RES	RO	Reserved
10:8	OVERFLOW_INDEX	RO	Overflow index
7:0	ENABLE	RW	Enable

10.20.59 SIFS, Tx Latency and ACK Shift (WMAC_PCU_TXSIFS)

Offset: 0x181081D0
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:15	RES	Reserved	
14:12	ACK_SHIFT	ACK_SHIFT is used to generate the ACK_TIME, which is used to generate the ACK_SIFS_TIME. The ACK_TIME table in the hardware assumes a channel width of 2.5 MHz. This value should be 3 for CCK rates.	
		0	2.5 MHz
		1	5 MHz
		2	10 MHz (11j)
		3	20 MHz (Standard 11a/11g)
		4	40 MHz (turbo mode)
11:8	TX_LATENCY	TX_LATENCY is the latency in µs from TX_FRAME being asserted by the MAC to when the energy of the frame is on the air. This value is used to decrease the time to TBTT and time remaining in TXOP in the calculation to determine quiet collision.	
7:0	SIFS_TIME	SIFS_TIME is the number of µs in SIFS. For example, in 802.11a, SIFS_TIME would be set to 16. This value is used to determine quiet collision and filtering due to TBTT and TXOP limits.	

10.20.60 TXOP for Non-QoS Frames (WMAC_PCU_TXOP_X)

Offset: 0x181081EC
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:8	RES	Reserved
7:0	SIFS_TIME	TXOP in units of 32 µs. A TXOP value exists for each QoS TID value. When a new burst starts, the TID is used to select one of the 16 TXOP values. This TXOP decrements until the end of the burst to make sure that the packets are not sent out by the time TXOP expires. This register is used for legacy non QoS frames.

10.20.61 TXOP for TID 0 to 3 (WMAC_PCU_TXOP_0_3)

Offset: 0x181081F0
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_3	Value in units of 32 µs
23:16	VALUE_2	Value in units of 32 µs
15:8	VALUE_1	Value in units of 32 µs
7:0	VALUE_0	Value in units of 32 µs

10.20.62 TXOP for TID 4 to 7 (WMAC_PCU_TXOP_4_7)

Offset: 0x181081F4
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_7	Value in units of 32 µs
23:16	VALUE_6	Value in units of 32 µs
15:8	VALUE_5	Value in units of 32 µs
7:0	VALUE_4	Value in units of 32 µs

10.20.63 TXOP for TID 8 to 11 (WMAC_PCU_TXOP_8_11)

Offset: 0x181081F8
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_11	Value in units of 32 µs
23:16	VALUE_10	Value in units of 32 µs
15:8	VALUE_9	Value in units of 32 µs
7:0	VALUE_8	Value in units of 32 µs

10.20.64 TXOP for TID 0 to 3 (WMAC_PCU_TXOP_12_15)

Offset: 0x181081FC
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_15	Value in units of 32 µs
23:16	VALUE_14	Value in units of 32 µs
15:8	VALUE_13	Value in units of 32 µs
7:0	VALUE_12	Value in units of 32 µs

10.20.65 Generic Timers (WMAC_PCU_GENERIC_TIMERS[0:15])

Offset: 0x18108200
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Address	Default	Description
0x8200–0x821C	0x0	GENERIC_TIMER_NEXT
0x8220–0x823C	0x0	GENERIC_TIMER_PERIOD

NOTE GENERIC _TIMER_0, unlike other generic timers, does not wake the MAC before timer expiration and its overflow mechanism does not generate an interrupt. Instead, it silently adds this period repeatedly until the next timer advances past the TSF. Thus when MAC wakes after sleeping for multiple TBTTs, the TGBTT does not assert repeatedly or cause the beacon miss count to jump.

Generic Timer	Function
0	TBTT
1	DMA beacon alert
2	SW beacon alert
3	Reserved
4	NEXT_TIM
5	NEXT_DTIM
6	Quiet time trigger
7	No dedicated function

10.20.66 Generic Timers Mode (WMAC_PCU_GENERIC_TIMERS_MODE)

Offset: 0x18108240
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: See Field Description

Bit	Name	Reset	Description
31:12	THRESH	0x100	Number of µs that generate a threshold interrupt if exceeded in TSF comparison
11	RES	0x0	Reserved
10:8	OVERFLOW_INDEX	UND	Indicates the last generic timer that overflowed
7:0	ENABLE	0x0	Timer enable

10.20.67 32 KHz Sleep Mode (WMAC_PCU_SLP32_MODE)

Offset: 0x18108244
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:25	RES	0x0	Reserved
24	TSF2_WRITE_ STATUS	0x1	This bit has the same function as TSF_WRITE_STATUS but this bit is the indication for TSF2.
23	FORCE_BIAS_ BLOCK_ON	0x0	When set, indicates that the Bias block is turned on and generating the reference current for PCIE PHY.
22	DISABLE_32KHZ	0x0	Indicates the 32 KHz clock is not used to control the TSF, but the MAC clock increments the TSF. Only used on AP class devices that do not go to sleep.
21	TSF_WRITE_STATUS	0x1	Since it takes such a long time to write the TSF, the effect of the TSF change may not occur until 10 µsec intervals after the write. Make sure that the write completes before the next read/write of the TSF is initiated. If the data is not stale, it may be read out. The SLEEP32_TSF_WRITE_STAT if set indicates that a configuration write or TSF reset (see register BEACON_PERIOD 0x8020) is in progress. Immediately after writing or resetting the TSF, this bit should be set between 15 to 45 µsec. If it does not get set, it may be because the TSF is being updated from a receive beacon and the writing or reset of the TSF will be lost. This is a read only register.
20	ENABLE	0x1	When set, indicates that the TSF should be allowed to increment on its own
19:0	HALF_CLK_LATENCY	0xF424	Defines the time in µsec from the detection of the falling edge of the 32 KHz clock to the rising edge of the 32 KHz clock. Whenever the TSF is updated by the configuration interface or by a receive beacon, the time in µsec is incremented until the falling edge of the 32 KHz clock then this time is added to the value of this register and is then is used to update the TSF. Since the 32 KHz clock is slow, if this modification is not done, the TSF will be off by 10s of µsecs. When there is no 32 KHz crystal the edges will be separated by 15.250 µsec which corresponds to the HALK_CLK_ LATENCY of 0xF400 for a 40 MHz reference clock.

10.20.68 32 KHz Sleep Wake (WMAC_PCU_SLP32_WAKE)

Offset: 0x18108248
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x800

Bit	Name	Description
31:16	RES	Reserved
15:0	XTL_TIME	Time in µs before a generic timer should expire that the wake signal asserts to the crystal wake logic. Add an extra 31 µs due to 32 KHz clock resolution.

10.20.69 32 KHz Sleep Increment (WMAC_PCU_SLP32_INC)

Offset: 0x1810824C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x1E848

Bit	Name	Description
31:20	RES	Reserved
19:0	TSF_INC	Time in $1/2^{12}$ of a µs the TSF increments on the rising edge of the 32 KHz clk (30.5176 µs period). The upper 8 bits are at µs resolution. The lower 12 bits are the fractional portion. $\frac{1 \text{ unit}}{1/212 \text{ ms}} = \frac{X}{30.5176 \text{ ms}}$ Where *X* = 125000, or 0x1E848 is the default setting for 32.768 MHz clock. The TSF_INC value needs to be programmed differently if there is no 32.768 KHz crystal and the 32 KHz clock is approximated using the 40 MHz reference clock. This is actually a more common system configuration. The closest to 30.5176 µsec using a divider on a 40 MHz reference clock is 30.500 µsec which corresponds to TSF_INC of 0x1E800. The HALF_CLK_LATENCY will then be 15.250 µsec which corresponds to 0x0F400.

10.20.70 Sleep MIB Sleep Count (WMAC_PCU_SLP_MIB1)

Offset: 0x18108250
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	SLEEP_CNT	Counts the number of 32 KHz clock cycles that the MAC has been asleep

10.20.71 Sleep MIB Cycle Count (WMAC_PCU_SLP_MIB2)

Offset: 0x18108254
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The SLEEP_CNT counts the number of 32 KHz clock cycles that the MAC has been asleep. The CYCLE_CNT counts the absolute number of 32 KHz clock cycles. When the CYCLE_CNT bit 31 is 1, the MIB interrupt will be asserted. The SLEEP_CNT and CYCLE_CNT are saturating counters when the value of CYCLE_CNT reaches 0xFFFF_FFFF both counters will stop incrementing. The CLR_CNT will clear both the SLEEP_CNT and CYCLE_CNT. During the time that the clearing of these register are pending the PENDING will be asserted. SLEEP_CNT, CYCLE_CNT, and CLR_CNT are writable for diagnostic purposes. Before every read/write, the PENDING bit should be polled to verify any pending write has cleared.

Bit	Name	Description
31:0	CYCLE_CNT	Counts the absolute number of 32KHz clock cycles. When CYCLE_CNT bit 31 is 1, the MIB interrupt will be asserted. SLEEP_CNT and CYCLE_CNT are saturating counters when the value of CYCLE_CNT reaches 0xFFFF_FFFF both counters will stop incrementing.

10.20.72 Sleep MIB Control Status (WMAC_PCU_SLP_MIB3)

Offset: 0x18108258
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

See Sleep MIB Cycle Count (WMAC_PCU_SLP_MIB2).

Bit	Name	Description
31:2	RES	Reserved
1	PENDING	SLEEP_CNT, CYCLE_CNT, and CLR_CNT are writable for diagnostic purposes. Before every read/write, the pending bit should be polled to verify any pending write has cleared.
0	CLR_CNT	CLR_CNT clears both SLEEP_CNT and CYCLE_CNT. Pending is asserted while the clearing of these registers is pending.

10.20.73 MAC PCU WoW 1 (WMAC_PCU_WOW1)

Offset: 0x1810825C
Access: See field description
Reset Value: See field description

See Sleep MIB Cycle Count (WMAC_PCU_SLP_MIB2).

Bit	Name	Access	Reset	Description
31:28	CW_BITS	RW	0x4	Indicates the number of bits used in the contention window. If = N, the random backoff is selected between 0 and (2^N) – 1. For example, if CS_BITS = 4, the random backoff is selected between 0 and 15. Values larger than 10 are assumed to be 10.
27:22	RES	RO	0x0	Reserved
21	BEACON_FAIL	RO	0x0	Beacon receive timeout
20	KEEP_ALIVE_FAIL	RO	0x0	Indicates excessive retry or other problems which cause the keep alive packet from transmitting successfully
19	INTR_DETECT	RO	0x0	Set when an interrupt was detected
18	INTR_ENABLE	RW	0x0	When set, indicates that MAC interrupts that are not masked cause WoW detection
17	MAGIC_DETECT	RO	0x0	Set when a magic packet has been detected
16	MAGIC_ENABLE	RW	0x0	When set, indicates the magic packet detection has been enabled
15:8	PATTERN_DETECT	RO	0x0	Indicate the which of the 8 patterns were matched a receive packet
7:0	PATTERN_ENABLE	RW	0x0	Indicate the which of the 8 patterns are enabled for compare

10.20.74 PCU WoW 2 (WMAC_PCU_WOW2)

Offset: 0x18108260
Access: Read/Write
Reset Value: See field description

See Sleep MIB Cycle Count (WMAC_PCU_SLP_MIB2).

Bit	Name	Reset	Description
31:24	RES	0x0	Reserved
23:16	TRY_CNT	0x00000008	Time in µs for TRY_CNT
15:8	SLOT	0x00000009	Time in µs for SLOT
7:0	AIFS	0x000000CC	Time in µs for AIFS

10.20.75 MAC PCU WoW Beacon Fail Enable (WMAC_PCU_WOW3_BEACON_FAIL)

Offset: 0x18108270
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:1	RES	Reserved
0	ENABLE	Enable WoW if the AP fails to send a beacon

10.20.76 MAC PCU WoW Beacon Fail Timeout (WMAC_PCU_WOW3_BEACON)

Offset: 0x18108274
Access: Read/Write
Reset Value: 0x40000000

Bit	Name	Description
31:0	TIMEOUT	WoW beacon fail timeout value (REFCLK cycles)

10.20.77 MAC PCU WoW Keep Alive Timeout (WMAC_PCU_WOW3_KEEP_ALIVE)

Offset: 0x18108278
Access: Read/Write
Reset Value: 0x3E4180

Bit	Name	Description
31:0	TIMEOUT	WoW keep alive timeout value (REFCLK cycles)

10.20.78 MAC PCU WoW Automatic Keep Alive Disable (WMAC_PCU_WOW_KA)

Offset: 0x1810827C
Access: Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:3	RES	0x0	Reserved
2	BKOFF_CS_ENABLE	0x00000001	Enable carrier sense during KEEPALIVEBACKOFF state
1	FAIL_DISABLE	0x00000000	Disable WoW If there is a failure in sending keep-alive frames
0	AUTO_DISABLE	0x00000000	Disable automatic transmission of keep-alive frames

10.20.79 1 µS Clocks (1US)

Address: 0x18108284
Access: Read/Write
Reset: See field description

This register sets the number of clocks in one micro-second. See Sleep MIB Sleep Count (WMAC_PCU_SLP_MIB1) for more information.

Bit	Bit Name	Reset	Description
31:7	RES	0x0	Reserved
6:0	SCALER	0x2C	The number of MAC clocks in one µs

10.20.80 WoW Keep-Alive Frames Delay (KA)

Address: 0x18108288
Access: Read/Write
Reset: See field description

See Sleep MIB Sleep Count (WMAC_PCU_SLP_MIB1) for more information.

Bit	Bit Name	Reset	Description
31:12	RES	0x0	Reserved
11:0	DEL	0x2C	Delay between WoW keep-alive frames

10.20.81 WoW Exact Length and Offset (WOW_EXACT)

Address: 0x1810828C
Access: Read/Write
Reset: See field description

This register contains the exact length and offset requirement Flag for WoW patterns. See Sleep MIB Sleep Count (WMAC_PCU_SLP_MIB1) for more information.

Bit	Bit Name	Reset	Description
31:16	RES	0x0	Reserved
15:8	OFFSET	0x00000000	Exact offset requirement flag for WoW patterns, 1 bit for each pattern.
7:0	LENGTH	0x00000000	Exact length requirement flag for WoW patterns, 1 bit for each pattern.

10.20.82 WoW Offset 1 (PCU_WOW4)

Offset: 0x18108294
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	OFFSET3	Offset for pattern 3
23:16	OFFSET2	Offset for pattern 2
15:8	OFFSET1	Offset for pattern 1
7:0	OFFSET0	Offset for pattern 0

10.20.83 WoW Offset 2 (PCU_WOW5)

Offset: 0x18108298
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	OFFSET7	Offset for pattern 7
23:16	OFFSET6	Offset for pattern 6
15:8	OFFSET5	Offset for pattern 5
7:0	OFFSET4	Offset for pattern 4

10.20.84 PHY Error Counter Continued (PHY_ERR_CNT_MASK_CONT)

Address: 0x1810829C
Access: Read/Write
Reset: 0x0

This register is the MAC PCU PHY error counter 1, 2, and 3 continued. See PHY Error Counter 1 (WMAC_PCU_PHY_ERR_CNT_1).

Bit	Bit Name	Description
31:24	RES	Reserved
23:16	MASK3	Mask for PHY error count #1 for PHY errors 35 to 32 which correspond to the MASK3 bits 39 to 32. PHY errors above 39 will not be counted.
15:8	MASK2	Mask for PHY error count #1 for PHY errors 39 to 32 which correspond to the MASK3 bits 39 to 32. PHY errors above 39 will not be counted.
17:0	MASK1	Mask for PHY error count #1 for PHY errors 39 to 32 which correspond to the MASK3 bits 39 to 32. PHY errors above 39 will not be counted.

10.20.85 Global Mode (WMAC_PCU_20_40_MODE)

Offset: 0x18108318

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

MAC PCU global mode register. There are only 4 allowable modes of operation:
A: Current HT2040 joined mode.
B: Current static HT20 mode.
C: Spec compliant mode.
D: Spec compliant but HT20 can Tx even when extension channel is busy mode.

Bit	Name	Description
31:16	RES	Reserved
15:4	PIFS_CYCLES	When EXT_PIFS_ENABLE is enabled, the PIFS_CYCLES register needs to be set to the appropriate value. In 11g mode PIFS is 10 μsec for SIFS and 9 μsec for slot. In 11a mode PIFS is 16 μsec for SIFS and 9 μsec for slot. This register defines the number of clock cycles per PIFS. For HT2040 mode the number of cycles should be 1672 for 11g mode and 2000 cycles for 11a mode. For HT20 mode the number of cycles should be 836 for 11g mode and 1000 for 11a mode.
3	SWAMPED_ FORCES_RX_ CLEAR_CTL_IDLE	Indicates that the baseband sees a strong signal on the extension channel and a weak signal on the control channel. This is likely caused by a transmitter on the extension channel that is so close that the spectral leakage onto the control channel is strong enough to cause RX_CLEAR on the control channel to indicate a busy signal.
2	TX_HT20_ON_ EXT_BUSY	When set, HT20 frames are permitted to be transmitted even when the extension channel has not been idle for PIFS. In fact it is permitted to transmit even if the extension channel is busy as long as the control channel is idle. The HT40 frames still depend on being idle for PIFS. This mode should only be enabled when capable of meeting the spectral mask requirement on the extension channel. To use this bit the JOINED_RX_CLEAR bit must be clear.
1	EXT_PIFS_ ENABLE	Enables the chips to be 802.11n compliant. The JOINED_RX_CLEAR must be clear to use this mode. When this bit is set, only the control channel RX_CLEAR is used to count down backoff. The only time that the extension channel is consulted is immediately prior to transmitting a frame. The PCU verifies that the extension channel has been clear for at least PIFS. See also PIFS_CYCLES register.
0	JOINED_RX_ CLEAR	Setting this bit causes the RX_CLEAR used in the MAC to be the AND of the control channel RX_CLEAR and the extension channel RX_CLEAR. If this bit is clear then the MAC will use only the control channel RX_CLEAR.

10.20.86 Difference RX_CLEAR Counter (WMAC_PCU_RX_CLEAR_ DIFF_CNT)

Offset: 0x18108328

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:0	RX_CLEAR_DIFF_ CNT	A cycle counter MIB register. On every cycle of the MAC clock, this counter increments every time the extension channel RX_CLEAR is low when the MAC is not actively transmitting or receiving. Due to a small lag between TX_FRAME and RX_CLEAR as well as between RX_CLEAR and RX_FRAME, the count may have some residual value even when no activity is on the extension channel.

10.20.87 Self Generated Antenna Mask (SELF_GEN_ANTENNA_MASK)

Address: 0x1810832C
Access: Read/Write
Reset: See field description

The antenna mask normally comes from the transmit descriptor. For self generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

Bit	Bit Name	Reset	Description
31:5	RES	0x0	Reserved
4	FORCE_CHAIN	0x0	Forces the SELF_GEN frame to be sent by chain 0 when location mode is on
3	ONE_RESP_EN	0x1	Forces the SELF_GEN frame to be sent by only one antenna when location mode is on
2:0	VALUE	0x7	

10.20.88 Control Registers for Block BA Control Fields (WMAC_PCU_BA_BAR_CONTROL)

Offset: 0x18108330
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

The MAC PCU control registers for block BA control fields. The antenna mask normally comes from the transmit descriptor. For self generated frames, this register will provide the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Reset	Description
31:13	RES	0x0	Reserved
12	UPDATE_BA_BITMAP_QOS_NULL	0x0	When set, it enables the update of BA_BITMAP on a QoS Null frame
11	TX_BA_CLEAR_BA_VALID	0x0	When set, enables the BA_VALID bits to be cleared upon transmit of the block ACK for an aggregate frame or on receiving a BAR
10	FORCE_NO_MATCH	0x0	Causes the BA logic to never find a match of previous saved bitmap in the memory
9	ACK_POLICY_VALUE	0x1	The value of the ACK policy bit
8	COMPRESSED_VALUE	0x1	The value of the compressed bit
7:4	ACK_POLICY_OFFSET	0x0	Indicates the bit offset in the block ACK or block ACK request control field which defines the location of the ACK policy bit.
3:0	COMPRESSED_OFFSET	0x2	Indicates the bit offset in the block ACK or block ACK request control field which defines the location of the COMPRESSED bit.

10.20.89 Legacy PLCP Spoof (WMAC_PCU_LEGACY_PLCP_SPOOF)

Offset: 0x18108334
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

The MAC PCU legacy PLCP spoof. The antenna mask normally comes from the transmit descriptor. For self generated frames, this register will provide the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Reset	Description
31:13	RES	0x0	Reserved
12:8	MIN_LENGTH	0xE	Defines the minimum spoofed legacy PLCP length
7:0	EIFS_MINUS _DIFS	0x0	Defines the number of µs to be subtracted from the transmit packet duration to provide fairness for legacy devices as well as HT devices.

10.20.90 PHY Error Mask and EIFS Mask (WMAC_PCU_PHY_ ERROR_MASK_CONT)

Offset: 0x18108338
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

MAC PCU PHY error mask and EIFS mask continued. The antenna mask normally comes from the transmit descriptor. For self-generated frames, this register will provide the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Description
31:24	AIFS_VALUE	This is a continuation of register MAC_PCU_PHY_ERROR_AIFS_MASK_VALUE. Bits [31] to [24] correspond to PHY errors 39 to 32. All others PHY errors above 39 will cause AIFS delay. Currently the baseband does not generate PHY errors above 39
23:16	EIFS_VALUE	Continuation of PHY Error Counter 1 Mask (WMAC_PCU_PHY_ERR_CNT_1_MASK), page 10-378. Bits [2], [1], and [0] correspond to PHY errors 34, 33, and 32. All PHY errors above 39 cause EIFS delay.
15:8	RES	Reserved
7:0	MASK_VALUE	Continuation of PHY Error Counter 1 Mask (WMAC_PCU_PHY_ERR_CNT_1_MASK), page 10-378. Bits [2], [1], and [0] correspond to PHY errors 34, 33, and 32. All PHY errors above 39 are filtered.

10.20.91 Tx Timer (WMAC_PCU_TX_TIMER)

Offset: 0x1810833C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: See field description

The MAC PCU transmit timer. The antenna mask normally comes from the transmit descriptor. For self-generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Reset	Description
31:26	RES	0x0	Reserved
25	QUIET_TIMER_ ENABLE	0x1	The quiet timer is enabled when this bit is set to 1.
24:20	QUIET_TIMER	0x4	This timer is used to guarantee the transmit frame does not take less time than the values programmed in this timer in case a quiet collision occurs. The unit for this timer is µsecs.
19:16	RIFS_TIMER	0x0	This timer defines the RIFS interval in the unit of µsecs
15	TX_TIMER_ ENABLE	0x0	Enabled when this bit is set to 1
14:0	TX_TIMER	0x0	Guarantees the transmit frame does not take more time than the values programmed in this timer. The unit for this timer is in µsecs.

10.20.92 Transmit Buffer Control (TXBUF_CTRL)

Address: 0x18108340
Access: Read/Write
Reset: See field description

The MAC PCU transmit buffer control. The antenna mask normally comes from the transmit descriptor. For self- generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

Bit	Bit Name	Reset	Description
31:17	RES	0x0	Reserved
16	TX_FIFO_WRAP_ ENABLE	0x1	Set to 1 to enable a fix to allow the Tx buffer to wrap correctly without overwriting previous data.
15:12	RES	0x0	Reserved
11:0	USABLE_ENTRIES	0x7FF	Controls how full the Tx buffer can be. The default is to use all the entries in the Tx buffer.

10.20.93 Alternate AES QoS Mute Mask (ALT_AES_MUTE_MASK)

Address: 0x18108348
Access: Read/Write
Reset: See field description

The antenna mask normally comes from the transmit descriptor. For self-generated frames, this register will provide the antenna mask to the baseband via the MAC/baseband interface.

Bit	Bit Name	Reset	Description
31:16	QOS	0x008F	Used to mask off sections of the MAC header for use in the AES algorithm. The QoS control fields are bytes 25 and 26 of the three-address frame and bytes 31 and 32 of the 4 address frame. This alternate QoS mute mask is needed to support changes in 802.11n related to the setting the mask of bit 7 of the QoS field. For APs, the client device must allow selection of the QoS mute mask. Some may support this new mute mask and others will not.
15:0	RES	0x0	Reserved

10.20.94 MAC PCU WoW 6 (WMAC_PCU_WOW6)

Offset: 0x1810834C
Access: Read-Only
Reset Value: 0x0

Indicates the start address of the frame in RxBUF which caused the WoW event.

Bit	Name	Description
31:16	RES	Reserved
15:0	RXBUF_START_ADDR	Indicates the start address of the frame in RxBUF that caused the WoW event

10.20.95 MAC PCU WoW 5 (WMAC_PCU_WOW5)

Offset: 0x1810835C
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:16	RES	Reserved
15:0	RX_ABORT_ENABLE	Enables generation of RX_ABORT when a pattern is matched

10.20.96 Length of Pattern Match for Pattern 0 (WMAC_PCU_WOW_LENGTH1)

Offset: 0x18108360
Access: Read/Write
Reset Value: 0xFF

The antenna mask normally comes from the Tx descriptor. For self generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Description
31:24	PATTERN_0	Used for pattern matching length of the WoW feature
23:16	PATTERN_1	Used for pattern matching length of the WoW feature
15:8	PATTERN_2	Used for pattern matching length of the WoW feature
7:0	PATTERN_3	Used for pattern matching length of the WoW feature

10.20.97 Length of Pattern Match for Pattern 1 (WMAC_PCU_WOW_LENGTH2)

Offset: 0x18108364
Access: Read/Write
Reset Value: 0xFF

The antenna mask normally comes from the Tx descriptor. For self generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Description
31:24	PATTERN_4	Used for pattern matching length of the WoW feature
23:16	PATTERN_5	Used for pattern matching length of the WoW feature
15:8	PATTERN_6	Used for pattern matching length of the WoW feature
7:0	PATTERN_7	Used for pattern matching length of the WoW feature

10.20.98 Enable Control for Pattern Match Feature of WOW (WOW_PATTERN_MATCH_LESS_THAN_256_BYTES)

Offset: 0x18108368
Access: Read/Write
Reset Value: 0x0

The antenna mask normally comes from the Tx descriptor. For self generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Description
31:16	RES	Reserved
15:0	EN	Used for turning on the feature of pattern matching length (<256 bytes) of the WOW feature

10.20.99 PCU WoW 4 (WMAC_PCU_WOW4)

Offset: 0x18108370
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:16	RES	Reserved
15:8	PATTERN_DETECT	Indicates the which of the 8 patterns were matched a receive packet
7:0	PATTERN_ENABLE	Indicates the which of the 8 patterns are enabled for compare

10.20.100 Exact Length and Offset Requirement Flag for WoW Patterns (WOW2_EXACT)

Offset: 0x18108374
Access: Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:16	RES	0x0	Reserved
15:8	OFFSET	0x0	Exact offset requirement flag for WoW patterns; 1 bit for each pattern
7:0	LENGTH	0xFF	Exact length requirement flag for WoW patterns;1 bit for each pattern

10.20.101 WoW Offset 2 (PCU_WOW6)

Offset: 0x18108378
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	OFFSET11	Offset for pattern 11
23:16	OFFSET10	Offset for pattern 10
15:8	OFFSET9	Offset for pattern 9
7:0	OFFSET8	Offset for pattern 8

10.20.102 WoW Offset 3 (PCU_WOW7)

Offset: 0x1810837C
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	OFFSET15	Offset for pattern 15
23:16	OFFSET14	Offset for pattern 14
15:8	OFFSET13	Offset for pattern 13
7:0	OFFSET12	Offset for pattern 12

10.20.103 Length of Pattern Match for Pattern 0 (WMAC_PCU_WOW_LENGTH3)

Offset: 0x18108380
Access: Read/Write
Reset Value: 0xFF

The antenna mask normally comes from the Tx descriptor. For self generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Description
31:24	PATTERN_8	Used for pattern matching length of the WoW feature
23:16	PATTERN_9	Used for pattern matching length of the WoW feature
15:8	PATTERN_10	Used for pattern matching length of the WoW feature
7:0	PATTERN_11	Used for pattern matching length of the WoW feature

10.20.104 Length of Pattern Match for Pattern 0 (WMAC_PCU_WOW_LENGTH4)

Offset: 0x18108384
Access: Read/Write
Reset Value: 0x0

The antenna mask normally comes from the Tx descriptor. For self generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Description
31:24	PATTERN_12	Used for pattern matching length of the WoW feature
23:16	PATTERN_13	Used for pattern matching length of the WoW feature
15:8	PATTERN_14	Used for pattern matching length of the WoW feature
7:0	PATTERN_15	Used for pattern matching length of the WoW feature

10.20.105 MAC PCU Timer for Location Mode (MAC_PCU_LOCATION_MODE_TIMER)

Offset: 0x838C
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	VALUE	The unit of timestamp value is MAC clock so it increments every MAC clock.

10.20.106 TSF 2 Lower 32 (TSF2_L32)

Address: 0x18108390
Access: Read/Write
Reset: See field description

This register holds the lower 32 bits of the MAC PCU TSF2.

Bit	Bit Name	Reset	Description
31:0	VALUE	0xFFFFFFF	Same function as TSF and added support for dual BSSID/TSF which is needed for DirectConnect or Mesh networking

10.20.107 TSF 2 Upper 32 (TSF2_U32)

Address: 0x18108394
Access: Read/Write
Reset: See field description

This register holds the upper32 bits of the MAC PCU TSF2.

Bit	Bit Name	Reset	Description
31:0	VALUE	0xFFFFFFF	The upper 32 bits of the local clock

10.20.108 BSSID 2 Lower 32 (BSSID2_L32)

Address: 0x18108398
Access: Read/Write
Reset: 0x0

This register holds the lower 32 bits for the MAC PCU BSSID2.

Bit	Bit Name	Description
31:0	ADDR	Lower 32 bits of BSSID2 (PCU_BSSID2[31:0]) Added to support dual BSSID/TSF which is needed for Mesh networking. Note that the only function added with this BSSID2 is to receive multicast/broadcast information from BSSID2 as well.

10.20.109 BSSID 2 Upper 16 (BSSID2_U16)

Address: 0x1810839C
Access: Read/Write
Reset: 0x0

This register holds the upper 16 bits of the MAC PCU BSSID2.

Bit	Bit Name	Description
31:17	RES	Reserved
16	ENABLE	Enables BSSID2
15:0	ADDR	The upper 16 bits of BSSID2 (PCU_BSSID2[47:32])

10.20.110 TID Value Access Category (WMAC_PCU_TID_TO_AC)

Offset: 0x181083A4
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:0	DATA	Maps the 16 user priority TID values to corresponding access category (AC). Two bits denote the AC for each TID. Bits [1:0] define the AC for TID 0 and next two bits are used for AC of TID 1, and finally bits [31:30] define the AC for TID 15. Default values are as specified in the 11e specification: TID 1 and 2 are BK, TID 0 and 3 are BK, TID 4 and 5 are VI, and TID 6 and 7 are V0. ACs:	
		00	BE
		01	BK
		10	VI
		11	VO

10.20.111 High Priority Queue Control (WMAC_PCU_HP_QUEUE)

Offset: 0x181083A8
Access: Read/Write
Reset Value: 0x0

Bit	Name	Reset	Description
31:23	RES	0x0	Reserved
22	NON_UAPSD_EN	0x1	If this bit is not set, only frames from UAPSD enabled devices having power management changes are placed into the HP QUEUE on power management change. Otherwise, all frames with power management changes are placed into the HP QUEUE. This bit is valid only if PM_ CHANGE bit is 1
21	PM_CHANGE	0x1	Place all frames which have power management state changes of a station into the HP QUEUE
20	UAPSD_EN	0x0	Enable detection and reporting in the Rx status of the UAPSD trigger frames and enable update of the PowerMgt bit in the key cache on error-free Rx-directed frames. If UAPSD enable is set for the AC of an error-free Rx directed QoS frame with the power management bit set, and the key cache entry of the sender has the PowerMgt bit set, it will be detected as a UAPSD trigger.
19:16	FRAME_SUBTYPE_ MASK0	0x0	Frame subtype mask for FRAME_SUBTYPE0, to be matched for the frame to be placed in high priority receive queue
15:12	FRAME_SUBTYPE0	0x0	Frame sub type to be matched for the frame to be placed in high priority receive queue
11:10	FRAME_TYPE_MASK0	0x3	Frame type mask for FRAME_TYPE0, to be matched for the frame to be placed in high priority receive queue
9:8	FRAME_TYPE0	0x0	Frame type to be matched for the frame to be placed in high priority receive queue
7	FRAME_BSSID_ MATCH0	0x0	If set to 1, frames with matching BSSID are only moved to high priority receive queue on a frame type match
6	FRAME_FILTER_ ENABLE0	0x0	Enables the mode where a frame is moved to high priority receive queue based on frame type
5	HPQON_UAPSD	0x0	Set to 1 if the Rx UAPSD trigger frame must be placed in the high priority Rx queue. Any frame that has a STA power management state change is also placed in the HP queue. HPQON_UAPSD = 1 with UAPSD_EN = 0 is not supported.
4	AC_MASK_VO	0x0	Set to 1 if BK traffic needs to be placed in high priority Rx queue
3	AC_MASK_VI	0x0	Set to 1 if VI traffic needs to be placed in high priority Rx queue
2	AC_MASK_BK	0x0	Set to 1 if BK traffic needs to be placed in high priority Rx queue
1	AC_MASK_BE	0x0	Set to 1 if BE traffic needs to be placed in high priority Rx queue
0	ENABLE	0x0	Enables high priority Rx queue

10.20.112 Hardware Beacon Processing 1 (HW_BCN_PROC1)

Address: 0x181083C8
Access: Read/Write
Reset: 0x0

This register is for Hardware Beacon Processing register 1.

Bit	Bit Name	Description
31:24	ELM2_ID	Element ID 2
23:16	ELM1_ID	Element ID 1
15:8	ELM0_ID	Element ID 0
7	EXCLUDE_ELM2	Exclude information with element ID ELM2 in CRC calculations
6	EXCLUDE_ELM1	Exclude information with element ID ELM1 in CRC calculations
5	EXCLUDE_ELM0	Exclude information with element ID ELM0 in CRC calculations
4	EXCLUDE_TIM_ELM	Exclude beacon TIME element in CRC calculations
3	EXCLUDE_CAP_INFO	Exclude beacon capability information in CRC calculations
2	EXCLUDE_BCN_INTVL	Exclude beacon intervals in CRC calculations
1	RESET_CRC	Reset the last beacon CRC calculated
0	CRC_ENABLE	Enables hardware beacon processing

10.20.113 Hardware Beacon Processing 2 (HW_BCN_PROC2)

Address: 0x181083CC
Access: Read/Write
Reset: See field description

This register is for Hardware Beacon Processing register 2.

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved
23:16	ELM3_ID	0x0	Element ID 3
15:8	FILTER_INTERVAL	0x2	Filter interval for beacons
7:3	RES	0x0	Reserved
2	EXCLUDE_ELM3	0x0	Exclude information with element ID ELM3 in CRC calculations
1	RESET_INTERVAL	0x0	Reset internal interval counter
0	FILTER_INTERVAL_ENABLE	0x0	Enable filtering beacons based on filter intervals

10.20.114 Key Cache (WMAC_PCU_KEY_CACHE[0:1023])

Offset: 0x18108800
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Table 10-22 Offset to First Dword of *N*th Key [1]

Intra Key	Offset Bits	Description	
8*N* + 00	31:0	Key[31:0]	
8*N* + 04	15:0	Key[47:32]	
8*N* + 08	31:0	Key[79:48]	
8*N* + 0C	15:0	Key[95:79]	
8*N* + 10	31:0	Key[127:96]	
8*N* + 14	14:3	Reserved	
	9	Power Mgt bit of last error-free directed Rx frame (only if UAPSD = 1)	
	8:5	UAPSD mask for the four ACs.	
		8	UAPSD enabled for BE
		7	UAPSD enabled for BK
		6	UAPSD enabled for VI
		5	UAPSD enabled for VO
	2:0	Key type:	
		0	40b
		1	104b
		2	TKIP without MIC
		3	128b
		4	TKIP
		5	Reserved
		6	AES_CCM
		7	Do nothing
8*N* + 18	31:0	Addr[32:1]	
8*N* + 1C	17:16	Key ID for multicast keys	
	15	Key valid	
		0	Entry has multi/broadcast key
		1	Entry has unicast key
	14:0	Addr[47:33]	

1. Key = (Address: 8800 + 20 * *N*)

When the key type is 4 (TKIP) and key is valid, this entry + 64 contains the Michael key. TKIP keys may not reside in the entries 64-127 because they require the Michael key. Entries 64-67 are always reserved for Michael.

Table 10-23 Offset to First Dword of *N*th Key (Continued)

Intra Key	Offset Bits	Description
8*N + 800	31:0	Rx Michael Key 0
8*N + 804	15:0	Tx Michael Key 0 [31:16]
8*N + 808	31:0	Rx Michael Key 1
8*N + 80C	15:0	Tx Michael Key 0 [15:0]
8*N + 810	31:0	Tx Michael Key 1
8*N + 814	RES	Reserved
8*N + 818	RES	Reserved
8*N + 81C	RES	Reserved
	15	Key Valid = 0

NOTE Internally the memory is 50 bits wide, thus writing a line of the memory requires two 32-bit writes. All writes to registers with an offset of 0x0 or 0x8 actually write to a temporary holding register. A write to registers with an offset of 0x4 or 0xC writes to memory.

10.21 PCIE Configuration Space Registers

Table 10-24 shows the PCI Express configuration space registers for the QCA9558.

Table 10-24 PCI Configuration Space Registers

RC1 Address	RC2 Address	Description	Page
0x180C0000	0x18280000	Vendor ID	page 405
0x180C0002	0x18280002	Device ID	page 405
0x180C0004	0x18280004	Command	page 406
0x180C0006	0x18280006	Status	page 406
0x180C0008	0x18280008	Revision ID	page 407
0x180C0009	0x18280009	Class Code	page 407
0x180C000C	0x1828000C	Cache Line Size	page 407
0x180C000D	0x1828000D	Master Latency Timer	page 407
0x180C000E	0x1828000E	Header Type	page 408
0x180C0010	0x18280010	Base Address 0 (Read-Only)	page 408
0x180C0010	0x18280010	BAR0 Mask (Write-Only)	page 409
0x180C0018	0x18280018	Bus Number	page 409
0x180C001E	0x1828001E	Secondary Status	page 410
0x180C0020	0x18280020	Memory Base	page 410
0x180C0022	0x18280022	Memory Limit	page 410
0x180C0024	0x18280024	Prefetchable Memory Base	page 411
0x180C0026	0x18280026	Prefetchable Memory Limit	page 411
0x180C0034	0x18280034	Capability Pointer	page 411
0x180C003C	0x1828003C	Interrupt Line	page 411
0x180C003D	0x1828003D	Interrupt Pin	page 412
0x180C003E	0x1828003E	Bridge Control	page 412

10.21.1 Vendor ID

RC1 Address: 0x180C0000
RC2 Address: 0x18280000
Access: Read-Only

The default value is the hardware configuration parameter.

Bit	Bit Name	Description
15:0	CX_VENDOR_ID_0	Vendor ID

10.21.2 Device ID

RC1 Address: 0x180C0002
RC2 Address: 0x18280002
Access: Read-Only

The default value is the hardware configuration parameters.

Bit	Bit Name	Description
15:0	CX_DEVICE_ID_0	Device ID

10.21.3 Command

RC1 Address: 0x180C0004
RC2 Address: 0x18280004
Access: See field description
Reset: 0

Bit	Access	Description
15:11	RO	Reserved
10	R/W	INTx assertion disable
9	RO	Fast back-to-back enable. Not applicable for PCIE. Hard-wired to 0.
8	R/W	SERR# enable
7	RO	IDSEL stepping/wait cycle control. Not applicable for PCIE. Hard-wired to 0.
6	R/W	Parity error response
5	RO	VGA palette snoop. Not applicable for PCIE. Hard-wired to 0.
4	RO	Memory write and invalidate. Not applicable for PCIE. Hard-wired to 0.
3	RO	Special cycle enable. Not applicable for PCIE. Hard-wired to 0.
2	R/W	Bus master enable
1	R/W	Memory space enable
0	R/W	I/O space enable

10.21.4 Status

RC1 Address: 0x180C0006
RC2 Address: 0x18280006
Access: See field description
Reset: See field description

Bit	Access	Reset	Description
15	RW1C	0	Detected parity error
14	RW1C	0	Signalled system error
13	RW1C	0	Received master abort
12	RW1C	0	Received target abort
11	RW1C	0	Signalled target abort
10:9	RO	0x0	DEVSEL timing; not applicable for PCIE. Hard-wired to 0.
8	RW1C	0	Master data parity error
7	RO	0	Fast back-to-back capable; not applicable for PCIE. Hard-wired to 0.
6	RO	0	Reserved
5	RO	0	66 MHz capable; not applicable for PCIE. Hardwired to 0.
4	RO	1	Capabilities list. Indicates presence of an extended capability item. Hard-wired to 1.
3	RO	0	INTx status
2:0	RO	0x0	Reserved

10.21.5 Revision ID

RC1 Address: 0x180C0008
RC2 Address: 0x18280008
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
7:0	CX_REVISION_ID_0	Revision ID

10.21.6 Class Code

RC1 Address: 0x180C0009
RC2 Address: 0x18280009
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
23:16	BASE_CLASS_CODE_0	Base class code
15:8	SUB_CLASS_CODE_0	Sub class code
7:0	IF_CODE_0	Programming interface

10.21.7 Class Line Size

RC1 Address: 0x180C000C
RC2 Address: 0x1828000C
Access: Read/Write
Reset: 0x0

Bit	Description
7:0	Cache line size This register is R/W for legacy compatibility purposes and is not applicable to PCI Express device functionality. Writing to the Cache Line Size register does not impact functionality of the RC.

10.21.8 Master Latency Timer

RC1 Address: 0x180C000D
RC2 Address: 0x1828000D
Access: Read-Only
Reset: 0x0

Bit	Description
7:0	Master latency timer; not applicable to PCIE. Hardwired to 0.

10.21.9 Header Type

RC1 Address: 0x180C000E
RC2 Address: 0x1828000E
Access: Read-Only
Reset: See field descriptions

Bit	Reset	Description
7	0x0	Multi-function device
6:0	0x01	Configuration header format. Hardwired to 0x01.

10.21.10 Base Address 0 (BAR0)

RC1 Address: 0x180C0010
RC2 Address: 0x18280010
Access: Read-Only
Reset: See field descriptions

The RC Core provides one 32-bit base address register.

Bit	Reset	Description	
31:4	0x0000000	BAR0 base address bits. The BAR0 mask value determines which address bits are masked.	
3	PREFETCHABLE0_0 for memory BAR	If BAR0 is a memory BAR, indicates if the memory region is prefetchable:	
		0	Non-prefetchable
		1	Prefetchable
2:1	BAR0_TYPE_0 for memory BAR	If BAR 0 is a memory BAR, bits [2:1] determine the BAR type:	
		00	32-bit BAR
		10	Unused
0	MEM0_SPACE_DECODER_0	0	BAR0 is a memory BAR
		1	Unused

10.21.11 BAR0 Mask

RC1 Address: 0x180C0010 (same as Base Address 0 (BAR0), page 10-408)
RC2 Address: 0x18280010
Access: Write-Only
Reset: See field descriptions

Determines the BAR bits non-writable by host software, which determines the address space size claimed by the BAR. This register only exists if the corresponding BAR*n*_MASK_WRITABLE_0 value is 1. Otherwise, the BAR*n*_MASK_0 value sets the BAR Mask value in hardware.

BAR Mask values indicate the range of low-order bits in each implemented BAR to not use for address matching. The BAR Mask value also indicates the range of low-order bits in the BAR that cannot be written from the host. The application can write to all BAR bits to set memory, I/O, and other BAR options. To disable a BAR, the application can write a 0 to bit [0] of the BAR Mask register. To change the BAR Mask value for a disabled BAR, the application must first enable the BAR by writing 1 to bit [0]. After enabling the BAR, the application can write a new value to the BAR Mask register. If the BAR Mask value for a BAR is less than that required for the BAR type, the RC Core uses the minimum BAR type value:

- BAR bits [11:0] are always masked for a memory BAR. The RC Core requires each memory BAR to claim at least 4 KB
- BAR bits [7:0] are always masked for an I/O BAR. The RC Core requires each I/O BAR to claim at least 256 bytes

Bit	Bit Name	Description	
31:1	BAR0 _MASK_0	Indicates which BAR0 bits to mask (make nonwritable) from host software, which in turn determines the size of the BAR. For example, writing 0xFFF to the BAR0 Mask register claims a 4096-byte BAR by masking bits 11:0 of the BAR from writing by host software. Application write access depends on the value of BAR0_MASK_WRITABLE_0: ■ If BAR0_MASK_WRITABLE_0 = 1, the BAR0 Mask register is writable ■ If BAR0_MASK_WRITABLE_0 = 0, BAR0 Mask is not writable	
0	BAR0 _ENABLED _0	Bit [0] is interpreted as BAR enable when writing to the BAR Mask register rather than as a mask bit because bit [0] of a BAR is always masked from writing by host software.	
		0	BAR0 is disabled
		1	BAR0 is enabled

10.21.12 Bus Number

RC1 Address: 0x180C0018
RC2 Address: 0x18280018
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
31:24	RO	Secondary latency timer; not applicable to PCI Express, hardwired to 0x00.
23:16	R/W	Subordinate bus number
15:8	R/W	Secondary bus number
7:0	R/W	Primary bus number

10.21.13 Secondary Status

RC1 Address: 0x180C001E
RC2 Address: 0x1828001E
Access: See field descriptions
Reset: 0

Bit	Access	Description
15	RW1C	Detected parity error
14	RW1C	Received system error
13	RW1C	Received master abort
12	RW1C	Received target abort
11	RW1C	Signalled timer abort
10:9	RO	DEVSEL timing; not applicable to PCIE. Hardwired to 0.
8	RW1C	Master data parity error
7	RO	Fast back-to-back capable; not applicable to PCIE. Hardwired to 0.
6	RO	Reserved
5	RO	66 MHz; not applicable to PCIE. Hardwired to 0.
4:0	RO	Reserved

10.21.14 Memory Base

RC1 Address: 0x180C0020
RC2 Address: 0x18280020
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
15:4	R/W	Memory base address
3:0	RO	Reserved

10.21.15 Memory Limit

RC1 Address: 0x180C0022
RC2 Address: 0x18280022
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
15:5	R/W	Memory limit address
4:0	RO	Reserved

10.21.16 Prefetchable Memory Base

RC1 Address: 0x180C0024
RC2 Address: 0x18280024
Access: See field descriptions
Reset: See field descriptions

Bit	Access	Default	Description	
15:4	R/W	0x000	Upper 12 bits of 32-bit prefetchable memory start address	
3:1	RO	0x0	Reserved	
0	RO	MEM_DECODE_64_0	64-bit memory addressing	
			0	32-bit memory addressing
			1	Unused

10.21.17 Prefetchable Memory Limit

RC1 Address: 0x180C0026
RC2 Address: 0x18280026
Access: See field descriptions
Reset: See field descriptions

Bit	Access	Default	Description	
15:4	R/W	0x000	Upper 12 bits of 32-bit prefetchable memory end address	
3:1	RO	0x0	Reserved	
0	RO	MEM_DECODE_64_0	64-bit memory addressing	
			0	32-bit memory addressing
			1	Unused

10.21.18 Capability Pointer

RC1 Address: 0x180C0034
RC2 Address: 0x18280034
Access: Read-Only
Reset: 0x40

Bit	Description
7:0	First capability pointer. Points to power management capability structure by default.

10.21.19 Interrupt Line

RC1 Address: 0x180C003C
RC2 Address: 0x1828003C
Access: Read/Write
Reset: 0xFF

Bit	Description
7:0	Interrupt line

10.21.20 Interrupt Pin

RC1 Address: 0x180C003D
RC2 Address: 0x1828003D
Access: Read-Only
Reset: 0x1

Bit	Description	
7:0	Interrupt pin. Identifies the legacy interrupt Message that the device uses. Valid values are:	
	00	The device does not use legacy interrupt
	01	The device uses INTA

10.21.21 Bridge Control

RC1 Address: 0x180C003E
RC2 Address: 0x1828003E
Access: See field descriptions
Reset: 0x0

Bit	Access	Description
15:12	RO	Reserved
11	RO	Discard timer SERR enable status; not applicable to PCIE. Hardwired to 0.
10	RO	Discard timer status; not applicable to PCIE. Hardwired to 0.
9	RO	Secondary discard timer; not applicable to PCIE. Hardwired to 0.
8	RO	Primary discard timer; not applicable to PCIE. Hardwired to 0.
7	RO	Fast back-to-back transactions enable; not applicable to PCIE. Hardwired to 0.
6	R/W	Secondary bus reset
5	RO	Master abort mode; not applicable to PCIE. Hardwired to 0.
4	R/W	VGA 16-bit decode
3	R/W	VGA enable
2	R/W	ISA enable
1	R/W	SERR enable
0	R/W	Parity error response enable

10.22 PCIE PLL PHY Registers

Table 10-25 summarizes the PCIE PLL PHY registers for the QCA9558.

Table 10-25 PCIE PLL PHY Registers

Address		Name	Description	Page
0x18116200	0x18116C80	PLL Division	DPLL	page 413
0x18116204	0x18116C84	PLL Division 2	DPLL2	page 414
0x18116208	0x18116C88	PLL Division 3	DPLL3	page 414

10.22.1 PLL Division (DPLL)

Address: 0x18116200
: 0x18116C80
Access: Read/Write
Reset: See field description

This register manually overrides the PLL divide ratio calculations.

Bit	Bit Name	Reset	Description
31:27	REFDIV	0x1	Manual override of the PLL reference divide ratio
26:18	NINT	0x10	Manual override of the PLL feedback divide ratio
17:0	NFRAC	0x0	Manual override of the PLL fractional value of the PLL divide ratio, requires PWD_PLLSDM=0 to be effective

10.22.2 PLL Division 2 (DPLL2)

Address: 0x18116204
: 0x18116C84
Access: Read/Write
Reset: See field description

This register holds the control bits for DPLL.

Bit	Bit Name	Reset	Description	
31	RANGE	0x0	Manual override for bias current control bits inside the DPLL to cover the required frequency range	
30	LOCAL_PLL	0x0	Chooses to manually set PLL control bits or not	
29:26	KI	0x6	Integral path gain of loop filter in DPLL	
25:19	KD	0x7F	Proportional gain of loop filter in DPLL	
18	EN_NEGTRIG	0x0	Enables the negative trigger for the DPLL digital engine. Only use half cycles for computations.	
17	SEL_1SDM	0x0	Sets the DPLL SDM order.	
			0	Second SDM order
			1	First SDM order
16	PLL_PWD	0x1	Manual override for PWD	
15:13	OUTDIV	0x0	Manual override to divide output of VCO in DPLL by 2^out_div[2:0].	
12:0	RES	0x0	Reserved	

10.22.3 PLL Division 3 (DPLL3)

Address: 0x18116208
: 0x18116C88
Access: Read/Write
Reset: 0x0

This register holds the EVM estimation bits.

Bit	Bit Name	Description
31:30	RES	Reserved
29:23	PHASE_SHIFT	Programmable phase shift for DPLL
22:0	RES	Reserved

10.23 PMU Registers

Table 10-26 summarizes the PCIE RC PHY registers for the QCA9558.

Table 10-26 PCIE RC PHY Registers

Address	Name	Description	Page
0x18116CC0	PMU1	PMU Configuration	page 415
0x18116CC4	PMU2	PMU Configuration 2	page 415

10.23.1 PMU Configuration (PMU1)

Address: 0x18116CC0
Access: Read/Write
Reset: 0x3009D8D0

This register is for configuring PMU.

Bit	Bit Name	Description
31:0	SWREG	CTRL bits for SWREG

10.23.2 PMU Configuration 2 (PMU2)

Address: 0x18116CC4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:22	SWREGMSB	MSB CTRL bits for SWREG
21	PGM	PGM
20:19	LDO_TUNE	DDR LDO TUNE
18	PWDLDO_DDR	PWD DDR LDO
17	LPOPWD	PWD DDR LDO
16:0	SPARE	Spare bits

10.24 PCIE RC PHY Registers

Table 10-27 summarizes the PCIE RC PHY registers for the QCA9558.

Table 10-27 PCIE RC PHY Registers

RC0 Address	RC1 Address	Name	Description	Page
0x18116DC0	0x18116E00	PCIE_PHY_REG_1	PCIE PHY 1	page 416
0x18116CC4	0x18116E04	PCIE_PHY_REG_2	PCIE PHY 2	page 417
0x18116CC8	0x18116E08	PCIE_PHY_REG_3	PCIE PHY 3	page 418

10.24.1 PCIE PHY 1 (PCIE_PHY_REG_1)

RC0 Address: 0x18116DC0
RC1 Address: 0x18116E00
Access: Read/Write
Reset: See field description

This register is the PCIE PHY long shift register.

Bit	Bit Name	Reset	Description	
31	SERDES_DIS_RXIMP	0x0	Disable the receiver impedance in SERDES	
30:29	SERDES_TXDR_CTRL	0x0	Transmit Amplitude control for the SERDES (used in conjunction with SERDES_HALFTXDR)	
28:27	PERSTDELAY	0x2	Controls delay of PERSTN_DIGITAL WRT PERSTN_SERDES	
			00	10 µs
			01	12 µs
			10	15 µs
			11	20 µs
26:25	CLKOBSSEL	0x0	Select different clocks for observation.	
			00	No clock
			01	CLK125M_TX
			10	CLK125M_RX
			11	CLK_PCIEREF
24	DATAOBSEN	0x0	Enables the receive Data Observe bus	
23	FUNCTEST_EN	0x0	Enables the low-speed functional test mode of the PCIE interface	
22	SERDES_DISABLE	0x0	Forces the SERDES into power down mode. Used during ATE testing of other interfaces	
21	RXCLKINV	0x1	Invert the CLK125M_RX before using for receive data latching	
20	FUNCTESTRXCLKINV	0x0	Invert the Functional Test Clock for receive latching	
19	FUNCTESTTXCLKINV	0x0	Invert the Functional Test Clock for Transmit latching	
18	ENABLECLKREQ	0x0	Enables assertion/deassertion of CLKREQ# pin upon L1-Entry/Exit	
17	FLORCELOOPBACK	0x0	Force PCIE PHY into looping back its Rx data back to Tx	
16:15	SEL_CLK	0x2	Overclock control	

14	SERDES_RX_EQ	0x0	Enables receiver equalization	
13	SERDES_EN_LCKDT	0x1	Enables the lock detect circuit	
12	SERDES_PLL_ DISABLE	0x0	When this bit is set the PLL is disabled in L1 state	
11	SERDES_POWER_ SAVE	0x0	When set, enables additional power saving of SERDES in L0s and L1 states	
10:9	SERDES_CDR_BW	0x3	CDR digital accumulator length control	
8:7	SERDES_TH_LOS	0x0	Threshold selection for RX loss-of-signal detection	
			00	Normal
			01	-2dB
			10, 11	+2dB
6	SERDESEN_DEEMP	0x1	Enable TX de-emphasis when high	
5	SERDES_HALFTXDR	0x0	Tx driver output amplitude is reduced to 500 mVppd when high	
4	SERDES_SEL_HSP	0x1	VCO frequency adjust	
3:0	SWITCH_CTRL	0xE	Resistor calibration switch control	

10.24.2 PCIE PHY 2 (PCIE_PHY_REG_2)

RC0 Address: 0x18116DC4
RC1 Address: 0x18116E04
Access: Read/Write
Reset: See field description

This register is the PCIE PHY long shift register.

Bit	Bit Name	Reset	Description
31:24	PRBS_ERROR_COUNT	0x0	PRBS error count
23	SDS_SDM_RXELECIDLE	0x0	SERDES Rx electrical idle status
22	SDS_SDM_RXDETECTED	0x0	SERDES receiver detect status
21	PRBS_SCRAMBLE	0x0	Scramble during PRBS pattern
20	PRBS_START	0x0	Start the PRBS testing
19:13	PRBS_TS_NUM	0x40	Number of TS preceding PRBS
12	TXDETRXOVREN	0x0	Enable bit for overriding and controlling the TxDetRx trigger
11	TXDETRXOVRVALUE	0x0	Override value for TxDetRx trigger
10	DATAOBSPRBSERR	0x0	Enables observation of PRBS Error Count of the 20-bit observation bus
9:6	CDRREADYTIMER	0x7	RX_CLOCK ready timer in units of 8*8ns. Triggered by an exit from RXELECIDLE
5:1	TXDETRXTARGETDELAY	0xC	Programmable timer that gets enabled after assertion of Tx Elecidle and MAC-PHY TxDetRx trigger . Receiver detection status is checked after the completion of this timer.
0	FORCEDETECT	0x0	Overrides the PHY_MAC_RXSTATUS to 0x3 (successful receiver detection) on occurence of PHY_MAC_PHYSTATUS pulse and mac_ PHY_XDETECTRX (receiver detection request). Overrides the originial receiver detection indication.

10.24.3 PCIE PHY 3 (PCIE_PHY_REG_3)

RC0 Address: 0x18116DC8
RC1 Address: 0x18116E08
Access: Read/Write
Reset: See field description

This register is the PCIE PHY long shift register.

Bit	Bit Name	Reset	Description
31:28	PRBS_COMMA_STATUS	0x0	PRBS Rx comma status
27:11	SPARE	0x00A0B	Spare bits
10	SEL_CLK100	0x0	Enable/disable for 100 MHz reference clock input to analog (used when serdes_disable is set)
9	EN_BEACONGEN	0x0	Enable SERDES beacon generation Controllability used in SRIF mode (pipe_mode = 0)
8	TXELECIDLE	0x0	Controllability for transmit electrical idle
7:6	SEL_CLK	0x0	Overclock control Controllability used in SRIF mode (pipe_mode = 0)
5	RX_DET_REQ	0x0	Receiver detection TxDetRx trigger - controllability used in SRIF mode (pipe_mode = 0)
4	MODE_OCLK_IN	0x0	Overclocking control 0 Non-overclocking 1 Overclocking
3	EN_PLL	0x0	Enable/disable SERDES PLL Controllability used in SRIF mode (pipe_mode = 0)
2	EN_LCKDT	0x1	Enable lock detect circuit Controllability used in SRIF mode (pipe_mode = 0)
1	EN_BUFS_RX	0x0	Enable SERDES Rx buffers Controllability used in SRIF mode (pipe_mode = 0)
0	EN	0x0	SERDES enable Controllability used in SRIF mode (pipe_mode = 0)

10.25 PCIE EP PHY Registers

Table 10-28 summarizes the PCIE EP PHY registers for the QCA9558.

Table 10-28 PCIE EP PHY Registers Summary

Address	Name	Description	Page
0x18116DC0	PCIE_EP_PHY_REG_1	PCIE EP PHY 1	page 419
0x18116DC4	PCIE_EP_PHY_REG_2	PCIE EP PHY 2	page 420
0x18116DC8	PCIE_EP_PHY_REG_3	PCIE EP PHY 3	page 421

10.25.1 PCIE EP PHY 1 (PCIE_EP_PHY_REG_1)

Address: 0x18116DC0
Access: Read/Write
Reset: 0x1021265E

This register contains bits to control the PCIE EP PHY long shift register 1.

Bit	Bit Name	Description	
31	SERDES_DIS_RXIMP	Disable the receiver impedance in SERDES	
30:29	SERDES_TXDR_CTRL	Transmit amplitude control for SERDES; used with SERDES_HALFTXDR)	
28:27	PERSTDELAY	Controls the delay of PERSTN_DIGITAL respecting PERSTN_SERDES	
		00	10 µs
		01	12 µs
		10	15 µs
		11	20 µs
26:25	CLKOBSSEL	Selects different clocks for observation	
		00	No clock
		01	CLK125M_TX
		10	CLK125M_RX
		11	CLK_PCIEREF
24	DATAOBSEN	Enable the receive data observe bus	
23	FUNCTESTEN	Enables the low-speed functional test mode of the PCIE interface	
22	SERDES_DISABLE	Force SERDES into power down mode; used during ATE testing of other interfaces	
21	RXCLKINV	Invert the CLK125M_RX before using for receive data latching	
20	FUNCTESTRXCLKINV	Invert the functional test clock for receive latching	
19	FUNCTESTTXCLKINV	Invert the functional test clock for transmit latching	
18	ENABLECLKREQ	Enable assertion/deassertion of the CLKREQ pin upon L1 entry/exit	
17	FORCELOOPBACK	Force PCIE PHY into looping Rx data back to Tx	
16:15	SEL_CLK	Overclock control	

14	SERDES_RX_EQ	Receiver equalization enable	
13	SERDES_EN_LCKDT	Enable lock detect circuit	
12	SERDES_PLL_DISABLE_L1	When this bit is set the PLL is disabled in L1 state	
11	SERDES_POWER_SAVE	When set, enables additional power saving of SERDES in L0s and L1 states	
10:9	SERDES_CDR_BW	CDR digital accumulator length control	
8:7	SERDES_TH_LOS	Threshold selection for Rx loss-of-signal detection	
		00	Normal
		01	–2 dB
		10/11	+2 dB
6	SERDES_EN_DEEMP	Enable Tx de-emphasis when high	
5	SERDES_HALFTXDR	Tx driver output amplitude is reduced to 500 mVppd when high	
4	SERDES_SEL_HSP	VCO frequency adjust	
3:0	SWITCH_CTRL	Resistor calibration switch control	

10.25.2 PCIE EP PHY 2 (PCIE_EP_PHY_REG_2)

Address: 0x18116DC4
Access: Read/Write
Reset: 0x000801D8

This register contains bits to control the PCIE EP PHY long shift register 2.

Bit	Bit Name	Description
31:24	PRBS_ERROR_COUNT	Indicates errors PRBS loopback Increments when the required number of comma symbols have not been received; reaches 0xAA when at timeout.
23	SDS_SDM_RXELECIDLE	SERDES Rx electrical idle status
22	SDS_SDM_RXDETECTED	SERDES RX detect result
21	PRBS_SCRAMBLE	Scramble during PRBS pattern
20	PRBS_START	Start the PRBS testing
19:13	PRBS_TS_NUM	Number of training sequences preceding PRBS
12	TXDETRXOVRVALUE	Value for Rx detection TXDETRX trigger when in override mode (pipe mode = 0)
11	TXDETRXOVREN	Used to enable Rx detection TXDETRX triggering; used when pipe mode=0
10	DATAOBSPRBSERR	Enables observation of the PRBS error count of the 20-bit observation bus
9:6	CDRREADYTIMER	RX_CLOCK ready timer in units of 8 * 8 ns; triggered by exit from RXELECIDLE
5:1	TXDETRXTARGETDELAY	Programmable delay for receiver detection operation
0	FORCEDETECT	Force receiver detection

10.25.3 PCIE EP PHY 3 (PCIE_EP_PHY_REG_3)

Address: 0x18116DC8
Access: Read/Write
Reset: 0x0000580C

This register contains bits to control the PCIE EP PHY long shift register 3.

Bit	Bit Name	Description	
31:16	RES	Reserved	
15:11	SPARE	Spare	
10	SEL_CLK100	Enable for CLK100M. Applicable for common PHY. Selects the source of the common PHY: internally generated or derived from Rx.	
9	EN_BEACONGEN	Enable beacon generation from the SERDES	
8	TXELECIDLE	Tx electric idle. Controllability for Tx electric idle; used when pipe mode = 0	
7:6	SEL_CLK	Select clock; overclock control	
5	RX_DET_REQ	Receive detect request: TXDETRX trigger	
4	MODE_OCLK_IN	Clock mode input to analog circuit.	
3	EN_PLL	Enables SERDES PLL	
		0	Disable
		1	Enable
2	EN_LCKDT	Enable lock detect circuit	
1	EN_BUFS_RX	Enable SERDES Rx buffers	
0	EN	SERDES enable; used when pipe mode = 0.	

10.26 Checksum Registers

Table 10-29 summarizes the Checksum registers for the QCA9558.

Table 10-29 Checksum Registers

Address	Name	Description	Page
0x18400000	DMATX_CONTROL	Checksum Transmit Control	page 422
0x18400004	DMATX_CONTROL1	Checksum Transmit Control 1	page 423
0x18400008	DMATX_CONTROL2	Checksum Transmit Control 2	page 423
0x1840000C	DMATX_CONTROL3	Checksum Transmit Control 3	page 423
0x18400010	DMATX_DESC0	First Tx Descriptor Address	page 424
0x18400014	DMATX_DESC1	First Tx Descriptor Address 1	page 424
0x18400018	DMATX_DESC2	First Tx Descriptor Address 2	page 424
0x1840001C	DMATX_DESC3	First Tx Descriptor Address 3	page 424
0x18400020	DMATX_DESC_STATUS	DMA Tx Descriptor Status	page 425
0x18400024	DMATX_ARB_CFG	DMA Tx Arbitration Configuration	page 425
0x18400028	RR_PKTCNT01	Channel 0 and 1 Round Robin Packet Count	page 426
0x1840002C	RR_PKTCNT23	Channel 2 and 3 Round Robin Packet Count	page 426
0x18400030	TXST_PKTCNT	Tx Packet Count	page 426
0x18400034	DMARX_CONTROL	DMA Rx Transmit Control	page 427
0x18400038	DMARX_DESC	DMA Rx Descriptor	page 427
0x1840003C	DMARX_DESC_STATUS	DMA Rx Descriptor Status	page 427
0x18400040	INTR	Checksum Interrupt	page 428
0x18400044	IMASK	Checksum Interrupt Mask	page 429
0x18400048	ARB_BURST	Checksum Burst Control	page 429
0x18400050	RESET_DMA	DMA Reset	page 430
0x18400054	CONFIG	Checksum Configuration	page 430

10.26.1 Checksum Transmit Control (DMATX_CONTROL)

Address: 0x18400000
Access: Read/Write
Reset: 0x0

This register is used to enable DMA transmit packet transfers for channel 0.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TXEN	Setting this bit enables DMA transmit packet transfers for channel 0. This bit is cleared by the built-in DMA controller whenever it encounters a Tx Underrun or Bus Error state.

10.26.2 Checksum Transmit Control1 (DMATX_CONTROL1)

Address: 0x18400004
Access: Read/Write
Reset: 0x0

This register is used to enable DMA transmit packet transfers for channel 1.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TXEN	Setting this bit enables DMA transmit packet transfers for channel 1. This bit is cleared by the built-in DMA controller whenever it encounters a Tx Underrun or Bus Error state.

10.26.3 Checksum Transmit Control2 (DMATX_CONTROL2)

Address: 0x18400008
Access: Read/Write
Reset: 0x0

This register is used to enable DMA transmit packet transfers for channel 2.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TXEN	Setting this bit enables DMA transmit packet transfers for channel 2. This bit is cleared by the built-in DMA controller whenever it encounters a Tx Underrun or Bus Error state.

10.26.4 Checksum Transmit Control3 (DMATX_CONTROL3)

Address: 0x1840000C
Access: Read/Write
Reset: 0x0

This register is used to enable DMA transmit packet transfers for channel 3.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TXEN	Setting this bit enables DMA transmit packet transfers for channel 3. This bit is cleared by the built-in DMA controller whenever it encounters a Tx Underrun or Bus Error state.

10.26.5 First Tx Descriptor Address (DMATX_DESC0)

Address: 0x18400010
Access: Read/Write
Reset: 0x0

This register contains the first Tx descriptor address for channel 0.

Bit	Bit Name	Description
31:0	ADDR	The address of the first Tx descriptor in the chain for channel 0

10.26.6 First Tx Descriptor Address 1 (DMATX_DESC1)

Address: 0x18400014
Access: Read/Write
Reset: 0x0

This register contains the first Tx descriptor address for channel 1.

Bit	Bit Name	Description
31:0	ADDR	The address of the first Tx descriptor in the chain for channel 1

10.26.7 First Tx Descriptor Address 2 (DMATX_DESC2)

Address: 0x18400018
Access: Read/Write
Reset: 0x0

This register contains the first Tx descriptor address for channel 2.

Bit	Bit Name	Description
31:0	ADDR	The address of the first Tx descriptor in the chain for channel 2

10.26.8 First Tx Descriptor Address 3 (DMATX_DESC3)

Address: 0x1840001C
Access: Read/Write
Reset: 0x0

This register contains the first Tx descriptor address for channel 3.

Bit	Bit Name	Description
31:0	ADDR	The address of the first Tx descriptor in the chain for channel 3

10.26.9 DMA Tx Descriptor Status (DMATX_DESC_STATUS)

Address: 0x18400020
Access: Read/Write
Reset: 0x0

This register reflects the status of the DMA Tx descriptor.

Bit	Bit Name	Description
31:26	RES	Reserved. Must be written with zero.
25:24	CHAIN_NUM	Denotes an active chain
23:16	PKTCNT	Packet count for channel 0
15:9	RES	Reserved. Must be written with zero.
8:5	DESC_INTR	When set, indicates that a Tx descriptor interrupt is pending for a corresponding chain (Ex. chain3, chain2, etc.)
4	BUSERROR	When set, indicates that a host slave split, retry, or error response was received by the DMA controller
3	UNDERRUN3	Set when the DMA controller reads a descriptor for channel 3 for each packet with PKTV set to 1
2	UNDERRUN2	Set when the DMA controller reads a descriptor for channel 2 for each packet with PKTV set to 1
1	UNDERRUN1	Set when the DMA controller reads a descriptor for channel 1 for each packet with PKTV set to 1
0	UNDERRUN0	Set when the DMA controller reads a descriptor for channel 0 for each packet with PKTV set to 1

10.26.10 DMA Tx Arbitration Configuration (DMATX_ARB_CFG)

Address: 0x18400024
Access: Read/Write
Reset: See field description

This register configures the Tx arbitration.

Bit	Bit Name	Reset	Description
31:26	WGT3	0x8	Weight for channel 3
25:20	WGT2	0x4	Weight for channel 2
19:14	WGT1	0x2	Weight for channel 1
13:8	WGT0	0x1	Weight for channel 0
7:1	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	RRMODE	0x1	Round robin mode

10.26.11 Channel 0 and 1 Round Robin Packet Count (RR_ PKTCNT01)

Address: 0x18400028
Access: Read/Write
Reset: 0x0

This register contains the round-robin packet count for channels 0 and 1.

Bit	Bit Name	Reset	Description
31:25	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
24:16	PKTCNT1	0x0	Packet count for channel 1
15:9	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
8:0	PKTCNT0	0x0	Packet count for channel 0

10.26.12 Channel 2 and 3 Round Robin Packet Count (RR_ PKTCNT23)

Address: 0x1840002C
Access: Read/Write
Reset: 0x0

This register contains the round-robin packet count for channels 2 and 3.

Bit	Bit Name	Description
31:25	RES	Reserved. Must be written with zero. Contains zeros when read.
24:16	PKTCNT3	Packet count for channel 3
15:9	RES	Reserved. Must be written with zero. Contains zeros when read.
8:0	PKTCNT2	Packet count for channel 2

10.26.13 Tx Packet Count (TXST_PKTCNT)

Address: 0x18400030
Access: Read/Write
Reset: 0x0

This register contains the packet count for channels 3, 2, and 1.

Bit	Bit Name	Description
31:24	PKTCNT3	Packet count for channel 3
23:16	PKTCNT2	Packet count for channel 2
15:8	PKTCNT1	Packet count for channel 1
7:0	RES	Reserved. Must be written with zero. Contains zeros when read.

10.26.14 DMA Rx Transmit Control (DMARX_CONTROL)

Address: 0x18400034
Access: Read/Write
Reset: 0x0

This register enables DMA receive packets transfers.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	RXEN	Setting this bit enables DMA receive packets transfers. When set, the built-in DMA controller will start to receive a new packet whenever the FIFO indicates that a new packet is available (FRSOF asserted). This bit is cleared by the built-in DMA controller whenever it encounters an Rx overflow or bus error.

10.26.15 DMA Rx Descriptor (DMARX_DESC)

Address: 0x18400038
Access: Read/Write
Reset: 0x0

This register contains the first Rx descriptor address.

Bit	Bit Name	Description
31:0	ADDR	When RXENABLE is set by the host, the built-in DMA controller reads this register to discover the location in the host memory of the first receive packet descriptor

10.26.16 DMA Rx Descriptor Status (DMARX_DESC_STATUS)

Address: 0x1840003C
Access: Read/Write
Reset: 0x0

This register sets the status for various DMA Rx descriptor functions.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:16	PKTCNT	An 8-bit transmit packet counter that is incremented whenever the built-in DMA controller successfully transfers a packet, and decremented whenever the host writes a “1” to bit 0 (OVERFLOW) of this register.
15:3	RES	Reserved. Must be written with zero. Contains zeros when read.
2	DESC_INTR	When set, indicates that an Rx descriptor interrupt is pending
1	BUSERROR	When set, indicates that a host slave split, retry or error response was received by the DMA controller
0	OVERFLOW	Set whenever the DMA controller reads a set 1 Empty Flag in the descriptor it is processing

10.26.17 Checksum Interrupt (INTR)

Address: 0x18400040
Access: Read/Write
Reset: 0x0

This register reflects the status of checksum interrupts.

Bit	Bit Name	Description	
31:17	RES	Reserved. Must be written with zero. Contains zeros when read.	
16:4	TX_VAL	Status of Tx interrupts	
		16:13	Per-chain TxPktIntr[3:0]
		12	TxPktCnt > 0 on chain 3
		11	TxPktCnt > 0 on chain 2
		10	TxPktCnt > 0 on chain 1
		9	TxUnderrun on chain 3
		8	TxUnderrun on chain 2
		7	TxUnderrun on chain 1
		6	BusError
		5	TxUnderrun on chain 0
		4	TxPktCnt > 0 on chain 0
3:0	RX_VAL	Status of Rx interrupts	
		3	RxPktIntr
		2	BusError
		1	RxOverflow
		0	RxPktCnt > 0

10.26.18 Checksum IMask (IMASK)

Address: 0x18400044
Access: Read/Write
Reset: 0x0

This register is used to set the Checksum interrupt mask.

Bit	Bit Name	Description	
31:17	RES	Reserved. Must be written with zero. Contains zeros when read.	
16:4	TX_VAL	Mask for Tx interrupts	
		16:13	Per-chain TxPktIntr[3:0]
		12	TxPktCnt > 0 on chain 3
		11	TxPktCnt > 0 on chain 2
		10	TxPktCnt > 0 on chain 1
		9	TxUnderrun on chain 3
		8	TxUnderrun on chain 2
		7	TxUnderrun on chain 1
		6	BusError
		5	TxUnderrun on chain 0
		4	TxPktCnt > 0 on chain 0
3:0	RX_VAL	Mask for Rx interrupts	
		3	RxPktIntr
		2	BusError
		1	RxOverflow
		0	RxPktCnt > 0

10.26.19 Checksum Burst Control (ARB_BURST)

Address: 0x18400048
Access: Read/Write
Reset: See field description

This register is used to set the maximum burst size for Rx and Tx.

Bit	Bit Name	Reset	Description
31:26	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
25:16	MAX_RX	0x42	Rx Maximum burst size
15:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:0	MAX_TX	0x42	Tx Maximum Burst Size

10.26.20 DMA Reset (RESET_DMA)

Address: 0x18400050
Access: Read/Write
Reset: 0x0

This register is used to reset parts of the DMA engine.

Bit	Bit Name	Description
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	RX	Resets the Rx portion of the DMA engine
0	TX	Resets the Tx portion of the DMA engine

10.26.21 Checksum Configuration (CONFIG)

Address: 0x18400054
Access: Read/Write
Reset: See field description

This register configures the checksum settings.

Bit	Bit Name	Reset	Description
31:22	SPARE	0x16	Spare registers
21:16	TXFIFO_MIN_TH	0x16	Restarts the Tx DMA when the number of words are less than this value
15:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:4	TXFIFO_MAX_TH	0x19	Stops the Tx DMA and waits for the FIFO to be flushed when the number of words are greater than this value
3:1	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CHKSUM_SWAP	0x0	Swap checksum computation

10.27 UART1 (High-Speed) Registers

Table 10-30 summarizes the UART1 registers for the QCA9558.

Table 10-30 UART1 Registers

Address	Name	Description	Page
0x18500000	UART1_DATA	UART1 Transmit and Rx FIFO	page 431
0x18500004	UART1_CS	UART1 Configuration and Status	page 432
0x18500008	UART1_CLOCK	UART1 Clock	page 433
0x1850000C	UART1_INT	UART1 Interrupt	page 433
0x18500010	UART1_INT_EN	UART1 Interrupt Enable	page 434

10.27.1 UART1 Transmit and Rx FIFO Interface (UART1_DATA)

Address: 0x18500000
Access: Read/Write
Reset: 0x0

This register pushes data on the Tx FIFO and pop data off the Rx FIFO. This interface can be used only if all other interfaces are disabled in the UART1 Configuration and Status (UART1_CS).

Bit	Bit Name	Description
31:10	RES	Reserved. Must be written with zero. Contains zeros when read.
9	UART1_TX_CSR	Read returns the status of the Tx FIFO. If set, the Tx FIFO can accept more transmit data. Setting this bit will push UART1_TX_RX_DATA on the Tx FIFO. Clearing this bit has no effect.
8	UART1_RX_CSR	Read returns the status of the Rx FIFO. If set, the receive data in UART1_TX_RX_DATA is valid. Setting this bit will pop the Rx FIFO if there is valid data. Clearing this bit has no effect.
7:0	UART1_TX_RX_DATA	Read returns receive data from the Rx FIFO, but leaves the FIFO unchanged. The receive data is valid only if UART1_RX_CSR is also set. Write pushes the transmit data on the Tx FIFO if UART1_TX_CSR is also set.

10.27.2 UART1 Configuration and Status (UART1_CS)

Address: 0x18500004
Access: Read/Write
Reset: 0x0

This register configures the UART1 operation and reports the operating status.

Bit	Bit Name	Type	Description	
31:16	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
15	UART1_RX_ BUSY	RO	This bit is set whenever there is receive data or data is being received. It is clear when receive is completely idle.	
14	UART1_TX_ BUSY	RO	This bit is set whenever there is data ready to transmit or being transmitted. It is clear when transmit is completely idle.	
13	UART1_ HOST_INT_ EN	RW	Enables an interrupt on the UART1 host	
12	UART1_HOST_ INT	RO	This bit will be set while the host interrupt is being asserted and will clear when host interrupt is deasserted.	
11	UART1_TX_ BREAK	RW	This bit blocks the Tx FIFO and causes a break to be continuously transmitted. The Tx FIFO will resume normal operation when this bit is clear.	
10	UART1_RX_ BREAK	RO	This bit will be set while a break is being received. It will clear when the receive break stops.	
9	UART1_SERIAL_TX_ READY	RO	This bit will be set while Serial Tx Ready is asserted and is cleared when Serial Tx Ready is deasserted.	
8	UART1_TX_ READY_ ORIDE	RW	This bit overrides the transmit ready flow control. If clear, transmit ready is controlled by UART1_FLOW_CONTROL_MODE. If set, then transmit ready will be true.	
7	UART1_RX_ READY_ORIDE	RW	This bit overrides the receive ready flow control. If clear, receive ready is controlled by UART1_FLOW_CONTROL_MODE. If set, then receive ready will be true.	
6	RES	RO	Reserved	
5:4	UART1_FLOW_ CONTROL_ MODE	RW	Select which hardware flow control to enable	
			00	No flow control. Disable hardware flow control. Serial Transmit Ready and Serial Receive Ready are controlled by UART1_RX_READY_ ORIDE and UART1_TX_READY_ORIDE.
			10	Hardware flow control. Enable standard RTS/CTS flow control to control Serial Transmit Ready and Serial Receive Ready.
			11	Inverted Flow Control. Enable inverted RTS/CTS flow control to control Serial Transmit Ready and Serial Receive Ready
3:2	UART1_ INTERFACE_ MODE	RW	Select which serial port interface to enable	
			00	No interface. Disable serial port.
			01	DTE interface. Configure serial port for DTE (Data Terminal Equipment) operation. Transmit on TD, receive on RD, flow control out on RTS, flow control in on CTS.
			10	DCE interface. Configure serial port for DCE (Data Communication Equipment) operation. Transmit on RD, receive on TD, flow control out on CTS, flow control in on RTS.
1:0	UART1_PARITY_ MODE	RW	Select the parity mode for transmit and receive data	
			00	No parity. Parity is not transmitted or received
			10	Odd parity. Odd parity is transmitted and checked on receive
			11	Even parity. Even parity is transmitted and checked on receive

10.27.3 UART1 Clock (UART1_CLOCK)

Address: 0x18500008
Access: Read/Write
Reset: 0x0

This register sets the scaling factors use by the serial clock interpolator to create the transmit bit clock and receive sample clock.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:16	UART1_ CLOCK_ SCALE	The serial clock divisor used to create a scaled Serial Clock. This is used to bring the serial clock into a range that can be interpolated by UART1_CLOCK_STEP. The actual divisor is (1 + UART1_CLOCK_SCALE). Use the formula: UART1_CLOCK_SCALE = truncate(((1310*serialClockFreq)/(131072*baudClockFreq)))
15:0	UART1_ CLOCK_STEP	The ratio of the scaled serial clock to the baud clock, as expressed by a 17-bit fraction. This value should range between 1310–13107 to maintain a better than ±5% accuracy. Smaller is generally better, because interpolation errors caused by a small value are far less than quantization errors caused by a large value. Use the formula: UART1_CLOCK_STEP = round((131072*baudClockFreq)/(serialClockFreq/(UART1ClockScale+1)))

10.27.4 UART1 Interrupt/Control Status (UART1_INT)

Address: 0x1850000C
Access: Read/Write
Reset: 0x0

This register when read, returns the current interrupt status. Setting a bit will clear the individual attempt. Clearing a bit has no effect.

Bit	Bit Name	Description
31:10	RES	Reserved. Must be written with zero. Contains zeros when read.
9	UART1_TX_ EMPTY_INT	This bit will be high while the Tx FIFO is almost empty. Setting this bit will clear this interrupt. Clearing this bit has no effect.
8	UART1_RX_FULL_ INT	This bit will be high while the Rx FIFO is almost full, triggering hardware flow control, if enabled. Setting this bit will clear this interrupt. Clearing this bit has no effect.
7	UART1_RX_ BREAK_OFF_INT	This bit will be high while a break is not received. Setting this bit will clear this interrupt. Clearing this bit has no effect.
6	UART1_RX_ BREAK_ON_INT	This bit will be high while a break is received. Setting this bit will clear this interrupt. Clearing this bit has no effect.
5	UART1_RX_ PARITY_ERR_INT	This bit will be high if receive parity checking is enabled and the receive parity does not match the value configured by UART1_PARITY_EVEN. Setting this bit will clear this interrupt. Clearing this bit has no effect.
4	UART1_TX_ OFLOW_ERR_INT	This bit will be high if the Tx FIFO overflowed. Setting this bit will clear this interrupt. Clearing this bit has no effect.
3	UART1_RX_ OFLOW_ERR_INT	This bit will be high if the Rx FIFO overflowed. Setting this bit will clear this interrupt. Clearing this bit has no effect.
2	UART1_RX_ FRAMING_ERR_ INT	This bit will be high if a receive framing error was detected. Setting this bit will clear this interrupt. Clearing this bit has no effect
1	UART1_TX_ READY_INT	Will be high if there is room for more data in the Tx FIFO. Setting this bit will clear this interrupt if there is room for more data in the Tx FIFO. Clearing this bit has no effect.
0	UART1_RX_ VALID_INT	This bit will be high while there is data in the Rx FIFO. Setting this bit will clear this interrupt if there is no more data in the Rx FIFO. Clearing this bit has no effect.

10.27.5 UART1 Interrupt Enable (UART1_INT_EN)

Address: 0x18500010
Access: Read/Write
Reset: 0x0

This register enables interrupts in the UART1 Interrupt register.

Bit	Bit Name	Description
31:10	RES	Reserved. Must be written with zero. Contains zeros when read.
9	UART1_TX_ EMPTY_INT_EN	Enables UART1_TX_EMPTY_INT in UART1 Interrupt/Control Status (UART1_INT).
8	UART1_RX_FULL_ INT_EN	Enables UART1_RX_FULL_INT in UART1 Interrupt/Control Status (UART1_INT).
7	UART1_RX_BREAK_OFF_INT_EN	Enables UART1_RX_BREAK_OFF_INT in UART1 Interrupt/Control Status (UART1_INT).
6	UART1_RX_BREAK_ON_INT_EN	Enables UART1_RX_BREAK_ON_INT in UART1 Interrupt/Control Status (UART1_INT).
5	UART1_RX_PARITY_ERR_INT_EN	Enables UART1_PARITY_ERR_INT in UART1 Interrupt/Control Status (UART1_INT).
4	UART1TX_OFLOW_ERR_INT_EN	Enables UART1_TX_OFLOW_ERR_INT in UART1 Interrupt/Control Status (UART1_INT).
3	UART1_RX_OFLOW_ERR_INT_EN	Enables UART1_RX_OFLOW_ERR_INT in UART1 Interrupt/Control Status (UART1_INT).
2	UART1_RX_ FRAMING_ERR_ INT_ EN	Enables UART1_RX_FRAMING_ERR_INT in UART1 Interrupt/Control Status (UART1_INT).
1	UART1_TX_READY_INT_EN	Enables UART1_TX_READY_INT in UART1 Interrupt/Control Status (UART1_INT).
0	UART1_RX_VALID_ INT_EN	Enables UART1_RX_VALID_INT in UART1 Interrupt/Control Status (UART1_INT).

10.28 GMAC Registers

Table 10-31 summarizes the GMAC0/GMAC1 registers for the QCA9558.

10.28.1 MAC Configuration 1

Table 10-31 Ethernet Registers Summary

GMAC0 Address	GMAC1 Address	Description		Page
0x19000000	0x1A000000	MAC Configuration 1		page 436
0x19000004	0x1A000004	MAC Configuration 2		page 441
0x19000008	0x1A000008	IPG/IFG		page 442
0x1900000C	0x1A00000C	Half-Duplex		page 443
0x19000010	0x1A000010	Maximum Frame Length		page 443
0x19000020	0x1A100020	MII Configuration		page 445
0x19000024	0x1A000024	MII Command		page 445
0x19000028	0x1A000028	MII Address		page 445
0x1900002C	0x1A00002C	MII Control		page 445
0x19000030	0x1A000030	MII Status		page 446
0x19000034	0x1A000034	MII Indicators		page 446
0x19000038	0x1A000038	Interface Control		page 447
0x1900003C	0x1A00003C	Interface Status		page 448
0x19000040	0x1A000040	STA Address 1		page 449
0x19000044	0x1A000044	STA Address 2		page 449
0x19000048	0x1A000048	ETH Configuration 0		page 450
0x1900004C	0x1A00004C	ETH Configuration 1		page 451
0x19000050	0x1A000050	ETH Configuration 2		page 451
0x19000054	0x1A000054	ETH Configuration 3		page 452
0x19000058	0x1A000058	ETH Configuration 4		page 452
0x1900005C	0x1A00005C	ETH Configuration 5		page 453
0x19000080	0x1A000080	TR64	Tx/Rx 64 Byte Frame Counter	page 453
0x19000084	0x1A000084	TR127	Tx/Rx 65-127 Byte Frame Counter	page 453
0x19000088	0x1A000088	TR255	Tx/Rx 128-255 Byte Frame Counter	page 454
0x1900008C	0x1A00008C	TR511	Tx/Rx 256-511 Byte Frame Counter	page 454
0x19000090	0x1A000090	TR1K	Tx/Rx 512-1023 Byte Frame Counter	page 454
0x19000094	0x1A000094	TRMAX	Tx/Rx 1024-1518 Byte Frame Counter	page 455
0x19000098	0x1A000098	TRMGV	Tx/Rx 1519-1522 Byte VLAN Frame Counter	page 455
0x1900009C	0x1A00009C	RBYT	Receive Byte Counter	page 455
0x190000A0	0x1A0000A0	RPKT	Receive Packet Counter	page 456
0x190000A4	0x1A0000A4	RFCS	Receive FCS Error Counter	page 456
0x190000A8	0x1A0000A8	RMCA	Receive Multicast Packet Counter	page 456
0x190000AC	0x1A0000AC	RBCA	Receive Broadcast Packet Counter	page 457
0x190000B0	0x1A0000B0	RXCF	Receive Control Frame Packet Counter	page 457
0x190000B4	0x1A0000B4	RXPF	Receive Pause Frame Packet Counter	page 457
0x190000B8	0x1A0000B8	RXUO	Receive Unknown OPCode Packet Counter	page 458
0x190000BC	0x1A0000BC	RALN	Receive Alignment Error Counter	page 458
0x190000C0	0x1A0000C0	RFLR	Receive Frame Length Error Counter	page 458
0x190000C4	0x1A0000C4	RCDE	Receive Code Error Counter	page 459
0x190000C8	0x1A0000C8	RCSE	Receive Carrier Sense Error Counter	page 459
0x190000CC	0x1A0000CC	RUND	Receive Undersize Packet Counter	page 459

Table 10-31 Ethernet Registers Summary (cont.)

GMAC0 Address	GMAC1 Address	Description		Page
0x190000D0	0x1A0000D0	ROVR	Receive Oversize Packet Counter	page 460
0x190000D4	0x1A0000D4	RFRG	Receive Fragments Counter	page 460
0x190000D8	0x1A0000D8	RJBR	Receive Jabber Counter	page 460
0x190000DC	0x1A0000DC	RDRP	Receive Dropped Packet Counter	page 461
0x190000E0	0x1A0000E0	TBYT	Transmit Byte Counter	page 461
0x190000E4	0x1A0000E4	TPKT	Transmit Packet Counter	page 461
0x190000E8	0x1A0000E8	TMCA	Transmit Multicast Packet Counter	page 462
0x190000EC	0x1A0000EC	TBCA	Transmit Broadcast Packet Counter	page 462
0x190000F0	0x1A0000F0	TXPF	Transmit Pause Control Frame Counter	page 462
0x190000F4	0x1A0000F4	TDFR	Transmit Deferral Packet Counter	page 463
0x190000F8	0x1A0000F8	TEDF	Transmit Excessive Deferral Packet Counter	page 463
0x190000FC	0x1A0000FC	TSCL	Transmit Single Collision Packet Counter	page 463
0x19000100	0x1A000100	TMCL	Transmit Multiple Collision Packet	page 463
0x19000104	0x1A000104	TLCL	Transmit Late Collision Packet Counter	page 464
0x19000108	0x1A000108	TXCL	Transmit Excessive Collision Packet Counter	page 464
0x1900010C	0x1A00010C	TNCL	Transmit Total Collision Counter	page 464
0x19000110	0x1A000110	TPFH	Transmit Pause Frames Honored Counter	page 465
0x19000114	0x1A000114	TDRP	Transmit Drop Frame Counter	page 465
0x19000118	0x1A000118	TJBR	Transmit Jabber Frame Counter	page 465
0x1900011C	0x1A00011C	TFCS	Transmit FCS Error Counter	page 466
0x19000120	0x1A000120	TXCF	Transmit Control Frame Counter	page 466
0x19000124	0x1A000124	TOVR	Transmit Oversize Frame Counter	page 466
0x19000128	0x1A000128	TUND	Transmit Undersize Frame Counter	page 467
0x1900012C	0x1A00012C	TFRG	Transmit Fragment Counter	page 467
0x19000130	0x1A000130	CAR1	Carry 1	page 468
0x19000134	0x1A000134	CAR2	Carry 2	page 469
0x19000138	0x1A000138	CAM1	Carry Mask 1	page 470
0x1900013C	0x1A00013C	CAM2	Carry Mask 2	page 471
0x19000180	0x1A000180	DMATXCNTRL_Q0	DMA Transfer Control for Queue 0	page 471
0x19000184	0x1A000184	DMATXDESCR_Q0	Descriptor Address for Queue 0 Tx	page 472
0x19000188	0x1A000188	***DMA Tx Status***		page 472
0x1900018C	0x1A00018C	DMARXCTRL	Rx Control	page 472
0x19000190	0x1A000190	DMARXDESCR	Pointer to Rx Descriptor	page 473
0x19000194	0x1A000194	DMARXSTATUS	Rx Status	page 473
0x19000198	0x1A000198	DMAINTRMASK	Interrupt Mask	page 474
0x1900019C	0x1A00019C	***Interrupts***		page 475
0x190001A0	0x1A0001A0	ETH_TX_BURST	Ethernet Tx burst	page 476
0x190001A4	0x1A0001A4	ETH_XFIFO_DEPTH	Current Tx and Rx FIFO Depth	page 476
0x190001A8	0x1A0001A8	ETH_TXFIFO_TH	Ethernet Transmit FIFO Throughput	page 477
0x190001AC	0x1A0001AC	ETH_RXFIFO_TH	Ethernet Rx FIFO	page 477

Table 10-31 Ethernet Registers Summary (cont.)

GMAC0 Address	GMAC1 Address	Description		Page
0x190001B8	0x1A0001B8	ETH_FREE_TIMER	Ethernet Free Timer	page 478
0x190001C0	0x1A0001C0	DMATXCNTRL_Q1	DMA Transfer Control for Queue 1	page 478
0x190001C4	0x1A0001C4	DMATXDESCR_Q1	Descriptor Address for Queue 1 Tx	page 479
0x190001C8	0x1A0001C8	DMATXCNTRL_Q2	DMA Transfer Control for Queue 2	page 479
0x190001CC	0x1A0001CC	DMATXDESCR_Q2	Descriptor Address for Queue 2 Tx	page 479
0x190001D0	0x1A0001D0	DMATXCNTRL_Q3	DMA Transfer Control for Queue 3	page 479
0x190001D4	0x1A0001D4	DMATXDESCR_Q3	Descriptor Address for Queue 3 Tx	page 480
0x190001D8	0x1A0001D8	DMATXARBCFG	DMA Tx Arbitration Configuration	page 480
0x190001E4	0x1A0001E4	DMATXSTATUS_123	Tx Status and Packet Count for Queues 1-3	page 481
0x19000200	—	LCL_MAC_ADDR_DW0	Local MAC Address Dword0	page 481
0x19000204	—	LCL_MAC_ADDR_DW1	Local MAC Address Dword1	page 481
0x19000208	—	NXT_HOP_DST_ADDR_ DW0	Next Hop Router MAC Address Dword0	page 482
0x1900020C	—	NXT_HOP_DST_ADDR_ DW1	Next Hop Router MAC Destination Address Dword1	page 482
0x19000210	—	GLOBAL_IP_ADDR0	Local Global IP Address 0	page 482
0x19000214	—	GLOBAL_IP_ADDR1	Local Global IP Address 1	page 482
0x19000218	—	GLOBAL_IP_ADDR2	Local Global IP Address 2	page 483
0x1900021C	—	GLOBAL_IP_ADDR3	Local Global IP Address 3	page 483
0x19000228	—	EG_NAT_CSR	Egress NAT Control and Status	page 483
0x1900022C	—	EG_NAT_CNTR	Egress NAT Counter	page 484
0x19000230	—	IG_NAT_CSR	Ingress NAT Control and Status	page 484
0x19000234	—	IG_NAT_CNTR	Ingress NAT Counter	page 485
0x19000238	—	EG_ACL_CSR	Egress ACL Control and Status	page 485
0x1900023C	—	IG_ACL_CSR	Ingress ACL Control and Status	page 485
0x19000240	—	EG_ACL_CMD0_AND_ ACTION	Egress ACL CMD0 and Action	page 486
0x19000244	—	EG_ACL_CMD1234	Egress ACL CMD1, CMD2, CMD3, CMD4	page 486
0x19000248	—	EG_ACL_OPERAND0	Egress ACL OPERAND 0	page 487
0x1900024C	—	EG_ACL_OPERAND1	Egress ACL OPERAND 1	page 487
0x19000250	—	EG_ACL_MEM _CONTROL	Egress ACL Memory Control	page 488
0x19000254	—	IG_ACL_CMD0_AND_ ACTION	Ingress ACL CMD0 and Action	page 489
0x19000258	—	IG_ACL_CMD1234	Ingress ACL CMD1, CMD2, CMD3,CMD4	page 490
0x1900025C	—	IG_ACL_OPERAND0	Ingress ACL OPERAND 0	page 490
0x19000260	—	IG_ACL_OPERAND1	Ingress ACL OPERAND 1	page 490
0x19000264	—	IG_ACL_MEM _CONTROL	Ingress ACL Memory Control	page 491
0x19000268	—	IG_ACL_COUNTER_GRP0	Ingress ACL Counter Group 0	page 492
0x1900026C	—	IG_ACL_COUNTER_GRP1	Ingress ACL Counter Group 1	page 492
0x19000270	—	IG_ACL_COUNTER_GRP2	Ingress ACL Counter Group 2	page 492
0x19000274	—	IG_ACL_COUNTER_GRP3	Ingress ACL Counter Group 3	page 493

Table 10-31 Ethernet Registers Summary (cont.)

GMAC0 Address	GMAC1 Address	Description		Page
0x19000278	—	IG_ACL_COUNTER_GRP4	Ingress ACL Counter Group 4	page 493
0x1900027C	—	IG_ACL_COUNTER_GRP5	Ingress ACL Counter Group 5	page 493
0x19000280	—	IG_ACL_COUNTER_GRP6	Ingress ACL Counter Group 6	page 494
0x19000284	—	IG_ACL_COUNTER_GRP7	Ingress ACL Counter Group 7	page 494
0x19000288	—	IG_ACL_COUNTER_GRP8	Ingress ACL Counter Group 8	page 494
0x1900028C	—	IG_ACL_COUNTER_GRP9	Ingress ACL Counter Group 9	page 495
0x19000290	—	IG_ACL_COUNTER_GRP10	Ingress ACL Counter Group 10	page 495
0x19000294	—	IG_ACL_COUNTER_GRP11	Ingress ACL Counter Group 11	page 495
0x19000298	—	IG_ACL_COUNTER_GRP12	Ingress ACL Counter Group 12	page 496
0x1900029C	—	IG_ACL_COUNTER_GRP13	Ingress ACL Counter Group 13	page 496
0x190002A0	—	IG_ACL_COUNTER_GRP14	Ingress ACL Counter Group 14	page 496
0x190002A4	—	IG_ACL_COUNTER_GRP15	Ingress ACL Counter Group 15	page 497
0x190002A8	—	EG_ACL_COUNTER_GRP0	Egress ACL Counter Group 0	page 497
0x190002AC	—	EG_ACL_COUNTER_GRP1	Egress ACL Counter Group 1	page 497
0x190002B0	—	EG_ACL_COUNTER_GRP2	Egress ACL Counter Group 2	page 498
0x190002B4	—	EG_ACL_COUNTER_GRP3	Egress ACL Counter Group 3	page 498
0x190002B8	—	EG_ACL_COUNTER_GRP4	Egress ACL Counter Group 4	page 498
0x190002BC	—	EG_ACL_COUNTER_GRP5	Egress ACL Counter Group 5	page 499
0x190002C0	—	EG_ACL_COUNTER_GRP6	Egress ACL Counter Group 6	page 499
0x190002C4	—	EG_ACL_COUNTER_GRP7	Egress ACL Counter Group 7	page 499
0x190002C8	—	EG_ACL_COUNTER_GRP8	Egress ACL Counter Group 8	page 500
0x190002CC	—	EG_ACL_COUNTER_GRP9	Egress ACL Counter Group 9	page 500
0x190002D0	—	EG_ACL_COUNTER_GRP10	Egress ACL Counter Group 10	page 500
0x190002D4	—	EG_ACL_COUNTER_GRP11	Egress ACL Counter Group 11	page 501
0x190002D8	—	EG_ACL_COUNTER_GRP12	Egress ACL Counter Group 12	page 501
0x190002DC	—	EG_ACL_COUNTER_GRP13	Egress ACL Counter Group 13	page 501
0x190002E0	—	EG_ACL_COUNTER_GRP14	Egress ACL Counter Group 14	page 502
0x190002E4	—	EG_ACL_COUNTER_GRP15	Egress ACL Counter Group 15	page 502
0x190002E8	—	CLEAR_ACL_COUNTERS	Clear ACL Counters	page 502

GMAC0 Address: 0x19000000
GMAC1 Address: 0x1A000000
Access: See field description
Reset: See field description

This register is used to set the actions for transmitting and receiving frames.

Bit	Bit Name	Type	Reset	Description
31	SOFT_RESET	RW	0x1	Setting this bit resets all modules except the host interface. The host interface is reset via HRST.
30	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
29:20	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

19	RESET_RX_MAC_ CONTROL	RW	0x0	Resets the receive (Rx) MAC control block
18	RESET_TX_MAC_ CONTROL	RW	0x0	Resets the transmit (Tx) MAC control
17	RESET_RX_ FUNCTION	RW	0x0	Resets the Rx function
16	RESET_TX_FUNCTION	RW	0x0	Resets the Tx function
15:9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
8	LOOP_BACK	RW	0x0	Setting this bit causes MAC Rx outputs to loop back to the MAC Rx inputs. Clearing this bit results in normal operation.
7:6	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
5	RX_FLOW _CONTROL	RW	0x0	Setting this bit causes the Rx MAC control to detect and act on pause flow control frames.
4	TX_FLOW_ CONTROL	RW	0x0	Setting this bit causes the Tx MAC control to send requested flow control frames. Clearing this bit prevents the MAC from sending flow control frames. The default is 0.
3	SYNCHRONIZED_RX	RO	0x0	Rx enable synchronized to the receive stream
2	RX_ENABLE	RW	0x0	Setting this bit will allow the MAC to receive frames from the PHY. Clearing this bit will prevent the reception of frames.
1	SYNCHRONIZED_TX	RO	0x0	Tx enable synchronized to the Tx stream
0	TX_ENABLE	RW	0x0	Allows the MAC to transmit frames from the system. Clearing this bit will prevent the transmission of frames.

10.28.2 MAC Configuration 2

GMAC0 Address: 0x19000004
GMAC1 Address: 0x1A000004
Access: Read/Write
Reset: See field description

This register is used to set the parameters relating to the MAC, including duplex, CRC, and oversized frames.

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:16</td><td>RES</td><td>0x0</td><td>Reserved. Must be written with zero. Contains zeros when read.</td></tr>
<tr><td>15:12</td><td>PREAMBLE_ LENGTH</td><td>0x7</td><td>Determines the length of the preamble field of the packet, in bytes.</td></tr>
<tr><td>11:10</td><td>RES</td><td>0x0</td><td>Reserved. Must be written with zero. Contains zeros when read.</td></tr>
<tr><td rowspan="6">9:8</td><td rowspan="6">INTERFACE_ MODE</td><td rowspan="6">0x0</td><td>Determines the type of interface to which the MAC is connected.</td></tr>
<tr><td><table>
<tr><th>Interface Mode</th><th>Bit [9]</th><th>Bit [8]</th></tr>
<tr><td>RESERVED</td><td>0</td><td>0</td></tr>
<tr><td>Nibble Mode (10/100 MBps MII/SMII...)</td><td>0</td><td>1</td></tr>
<tr><td>Byte Mode (GMII/RGMII)</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>7:6</td><td>RES</td><td>0x0</td><td>Reserved. Must be written with zero. Contains zeros when read.</td></tr>
<tr><td>5</td><td>HUGE_FRAME</td><td>0x0</td><td>Set this bit to allow frames longer than the MAXIMUM FRAME LENGTH to be transmitted and received. Clear this bit to have the MAC limit the length of frames at the MAXIMUM FRAME LENGTH value, which is contained in the Maximum Frame Length, page 10-443 register.</td></tr>
<tr><td>4</td><td>LENGTH_FIELD</td><td>0x0</td><td>Set this bit to cause the MAC to check the frame’s length field to ensure it matches the data field length. Clear this bit for no length field checking.</td></tr>
<tr><td>3</td><td>RES</td><td>0x0</td><td>Reserved. Must be written with zero. Contains zeros when read.</td></tr>
<tr><td>2</td><td>PAD/CRC ENABLE</td><td>0x0</td><td>Set this bit to have the MAC pad all short frames and append a CRC to every frame whether or not padding was required. Clear this bit if frames presented to the MAC have a valid length and contain a CRC.</td></tr>
<tr><td>1</td><td>CRC_ENABLE</td><td>0x0</td><td>Set this bit to have the MAC append a CRC to all frames. Clear this bit if frames presented to the MAC have a valid length and contain a valid CRC.</td></tr>
<tr><td>0</td><td>FULL_DUPLEX</td><td>0x0</td><td>Setting this bit configures the MAC to operate in full-duplex mode. Clearing this bit configures the MAC to operate in half-duplex mode only.</td></tr>
</table>

10.28.3 IPG/IFG

GMAC0 Address: 0x19000008
GMAC1 Address: 0x1A000008
Access: Read/Write
Reset: See field description

This register is used to configure settings for the inter-packet gap and the inter-frame gap.

Bit	Bit Name	Reset	Description
31	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
30:24	NON_BACK_TO_ BACK_INTER _PACKET_GAP1	0x40	Represents the carrier sense window. If a carrier is detected, MAC defers to the carrier. If the carrier becomes active, MAC continues timing and Tx, knowingly causing a collision to ensure fair access to the medium.
23	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
22:16	NON_BACK_TO_ BACK_INTER_ PACKET_GAP2	0x60	This programmable field represents the non-back-to-back inter-packet gap in bit times
15:8	MINIMUM_IFG_ ENFORCEMENT	0x50	Represents the minimum IFG size to enforce between frames (expressed in bit times). Frames with a IFG of less than programmed are dropped.
7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:0	BACK_TO_BACK_ INTER_PACKET_GAP	0x60	Represents the IPG between back-to-back packets (expressed in bit times). This IPG parameter is used in full- duplex mode when two Tx packets are sent back-to-back. Set this field to the desired number of bits.

10.28.4 Half-Duplex

GMAC0 Address: 0x1900000C
GMAC1 Address: 0x1A00000C
Access: Read/Write
Reset: See field description

This register is used to configure the settings for half-duplex, including back pressure, excessive defer and collisions.

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
23:20	ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION	0xA	Used when bit [19] is set. The value programmed is substituted for the Ethernet standard value of ten.
19	ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE	0x0	Setting this bit will configure the Tx MAC to use the setting of bits [23:20] instead of the tenth collision. Clearing this bit will cause the TX MAC to follow the standard binary exponential backoff rule, which specifies that any collision after the tenth uses 210-1 as the maximum backoff time.
18	BACKPRESSURE_ NO_BACKOFF	0x0	Setting this bit will configure the Tx MAC to immediately retransmit following a collision during backpressure operation. Clearing this bit will cause the Tx MAC to follow the binary exponential backoff rule.
17	NO_BACKOFF	0x0	Setting this bit will configure the Tx MAC to immediately retransmit following a collision. Clearing this bit will cause the Tx MAC to follow the binary exponential backoff rule.
16	EXCESSIVE_ DEFER	0x1	Setting this bit will configure the Tx MAC to allow the transmission of a packet that has been excessively deferred. Clearing this bit will cause the Tx MAC to abort the transmission of a packet that has been excessively deferred.
15:12	RETRANSMISSION_ MAXIMUM	0xF	This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The maximum number of attempts is defined by 802.11 standards as 0xF.
11:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:0	COLLISION_ WINDOW	0x37	This programmable field represents the slot time or collision window during which collisions might occur in a properly configured network. Since the collision window starts at the beginning of a transmission, the preamble and SFD are included. The reset value (0x37) corresponds to the count of frame bytes at the end of the window. If the value is larger than 0x3F the TPST single will no longer work correctly.

10.28.5 Maximum Frame Length

GMAC0 Address: 0x19000010
GMAC1 Address: 0x1A000010
Access: Read/Write
Reset: 0x600

This register is used to set the maximum allowable frame length.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	MAX_FRAME_LENGTH	This programmable field sets the maximum frame size in both the Tx and Rx directions

10.28.6 MII Configuration

GMAC0 Address: 0x19000020
GMAC1 Address: 0x1A000020
Access: Read/Write
Reset: 0x0

This register is used to set the MII management parameters.

Bit	Bit Name	Description
31	RESET_MII_ MGMT	Setting this bit resets the MII management. Clearing this bit allows MII management to perform management read/write cycles as requested by the host interface.
30:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	SCAN_AUTO_ INCREMENT	Setting this bit causes MII Management to continually read from a set of contiguous PHYs. The starting address of the PHY is specified by the PHY address field recorded in the MII address register. The next PHY to be read will be PHY address + 1. The last PHY to be queried in this read sequence will be the one residing at address 0x31, after which the read sequence will return to the PHY specified by the PHY address field.
4	PREAMBLE_ SUPRESSION	Setting this bit causes MII management to suppress preamble generation and reduce the management cycle from 64 clocks to 32 clocks. Clearing this bit causes MII management to perform Management read/write cycles with the 64 clocks of preamble.
3:0	MGMT_CLOCK_ SELECT	This field determines the clock frequency of the management clock (MDC).

Management Clock Select	3	2	1	0
Source clock divided by 4	0	0	0	0
Source clock divided by 4	0	0	0	1
Source clock divided by 6	0	0	1	0
Source clock divided by 8	0	0	1	1
Source clock divided by 10	0	1	0	0
Source clock divided by 14	0	1	0	1
Source clock divided by 20	0	1	1	0
Source clock divided by 28	0	1	1	1
Source clock divided by 34	1	0	0	0
Source clock divided by 42	1	0	0	1
Source clock divided by 50	1	0	1	0
Source clock divided by 58	1	0	1	1
Source clock divided by 66	1	1	0	0
Source clock divided by 74	1	1	0	1
Source clock divided by 82	1	1	1	0
Source clock divided by 98	1	1	1	1

10.28.7 MII Command

GMAC0 Address: 0x19000024
GMAC1 Address: 0x1A000024
Access: Read/Write
Reset: 0x0

This register is used to cause MII management to perform read cycles.

Bit	Bit Name	Description
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	SCAN_CYCLE	Causes MII management to perform read cycles continuously (e.g. to monitor link fail).
0	READ_CYCLE	Causes MII management to perform a single read cycle.

10.28.8 MII Address

GMAC0 Address: 0x19000028
GMAC1 Address: 0x1A000028
Access: Read/Write
Reset: 0x0

All MAC/PHY registers are accessed via the MII address and MII control registers of GMAC0 only. GMAC1 MII address and control registers are not used. The details of the Ethernet MAC/PHY that are accessible through the MAC 0 MII address.

Bit	Bit Name	Description
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.
12:8	PHY_ADDRESS	Represents the five-bit PHY address field used in management cycles. Up to 31 PHYs can be addressed (0 is reserved).
7:5	RES	Reserved. Must be written with zero. Contains zeros when read.
4:0	REGISTER ADDRESS	Represents the five-bit register address field used in management cycles. Up to 32 registers can be accessed.

10.28.9 MII Control

GMAC0 Address: 0x1900002C
GMAC1 Address: 0x1A00002C
Access: Write-Only
Reset: 0x0

All MAC/PHY registers are accessed via the MII address and MII control registers. This register is used to perform write cycles using the information in the MII address register.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	MII_MGMT_ CONTROL	When written, an MII management write cycle is performed using the 16-bit data and the pre-configured PHY and register addresses from "MII Address, page 10-445" (0x0A).

10.28.10 MII Status

GMAC0 Address: 0x19000030
GMAC1 Address: 0x1A000030
Access: Read-Only
Reset: 0x0

This register is used to read information following an MII management read cycle.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	MII_MGMT_ STATUS	After an MII management read cycle, 16-bit data can be read from this register.

10.28.11 MII Indicators

GMAC0 Address: 0x19000034
GMAC1 Address: 0x1A000034
Access: Read-Only
Reset: 0x0

This register is used indicate various functions of the MII management are currently being performed.

Bit	Bit Name	Description
31:3	RES	Reserved. Must be written with zero. Contains zeros when read.
2	NOT_VALID	When a 1 is returned, this bit indicates that the MII management read cycle has not yet completed and that the read data is not yet valid
1	SCANNING	When a 1 is returned, this bit indicates that a scan operation (continuous MII management read cycles) is in progress
0	BUSY	When a 1 is returned, this bit indicates that the MII management block is currently performing an MII management read or write cycle

10.28.12 Interface Control

GMAC0 Address: 0x19000038
GMAC1 Address: 0x1A000038
Access: Read/Write
Reset: 0x0

This register is used to configure and set the interface modules.

Bit	Bit Name	Description	
31	RESET_ INTF_ MODULE	Setting this bit resets the interface module, clearing it allows for normal operation. This bit can be used in place of bits [23], [15], and [7] when an interface module is connected.	
30:28	RES	Reserved. Must be written with zero. Contains zeros when read.	
27	TBIMODE	Setting this bit configures the A-RGMII module to expect TBI signals at the GMII interface. This bit should not be asserted unless this mode is being used.	
26	GHDMODE	Setting this bit configures the A-RGMII to expect half-duplex at the GMII interface. It also enables the use of CRS and COL signals.	
25	LHDMODE	Setting this bit configures the A-RGMII module to expect 10 or 100 MBps half-duplex MII at the GMII interface and will enable the use of CRS and COL signals. This bit should not be asserted unless this mode is being used.	
24	PHY_MODE	Setting this bit configures the serial MII module to be in PHY Mode. Link characteristics are taken directly from the RX segments supplied by the PHY.	
23	RESET_PERMII	Setting this bit resets the PERMII module. Clearing this bit allows for normal operation.	
22:17	RES	Reserved. Must be written with zero. Contains zeros when read.	
16	SPEED	This bit configures the reduced MII module with the current operating speed.	
		0	Selects 10 MBps mode
		1	Selects 100 MBps mode
15	RESET_PE100X	Resets the PE100X module, which contains the 4B/5B symbol encipher/decipher code.	
14:11	RES	Reserved. Must be written with zero. Contains zeros when read.	
10	FORCE_QUIET	Affects PE100X module only.	
		0	Normal operation
		1	Tx data is quiet, allowing the contents of the cipher to be output
9	NO_CIPHER	Affects PE100X module only.	
		0	Normal ciphering occurs
		1	The raw transmit 5B symbols are transmitting without ciphering
8	DISABLE_LINK_ FAIL	Affects PE100X module only.	
		0	Normal Operation
		1	Disables the 330-ms link fail timer, allowing shorter simulations. Removes the 330-ms link-up time before stream reception is allowed.
7	RESET GPSI	This bit resets the PE10T module which converts MII nibble streams to the serial bit stream of ENDEC PHYs. Affects PE10T module only.	
6:1	RES	Reserved. Must be written with zero. Contains zeros when read.	
0	EN_ JABBER_ PROTECTION	This bit enables the jabber protection logic within the PE10T in ENDEC mode. Jabber is the condition where a transmitter is on for longer than 50 ms preventing other STAs from transmitting. Affects PE10T module only.	

10.28.13 Interface Status

GMAC0 Address: 0x1900003C
GMAC1 Address: 0x1A00003C
Access: Read-Only
Reset: 0x0

Identifies the interface statuses. The range of bits that are active are dependant upon the optional interfaces connected at the time.

Bit	Bit Name	Description	
31:10	RES	Reserved. Must be written with zero. Contains zeros when read.	
9	EXCESS_DEFER	This bit sets when the MAC excessively defers a transmission. It clears when read. This bit latches high.	
8	CLASH	Used to identify the SGMII module mode	
		0	In PHY mode or in a properly configured MAC-to-MAC mode
		1	MAC-to-MAC mode with the partner in 10 MBps and/or half-duplex mode indicative of a configuration error
7	JABBER	Used to identify a jabber condition as detected by the SGMII PHY	
		0	No jabber condition detected
		1	Jabber condition detected
6	LINK_OK	Used to identify the validity of a SGMII PHY link	
		0	No valid link detected
		1	Valid link detected
5	FULL_DUPLEX	Used to identify the current duplex of the SGMII PHY	
		0	Half-duplex
		1	Full-duplex
4	SPEED	Used to identify the current running speed of the SGMII PHY	
		0	10 MBps
		1	100 MBps
3	LINK_FAIL	Used to read the PHY link fail register. For asynchronous host accesses, this bit must be read at least once every scan read cycle of the PHY.	
		0	The MII management module has read the PHY link fail register to be 0
		1	The MII management module has read the PHY link fail register to be 1
2	CARRIER_LOSS	Carrier status. This bit latches high.	
		0	No carrier loss detection
		1	Loss of carrier detection
1	SQE_ERROR	0	Has not detected an SQE error. Latches high.
		1	Has detected an SQE error.
0	JABBER	0	Has not detected a Jabber condition. Latches high.
		1	Has detected a Jabber condition

10.28.14 STA Address 1

GMAC0 Address: 0x19000040
GMAC1 Address: 0x1A000040
Access: Read/Write
Reset: 0x0

This register holds the first four octets of the station address.

Bit	Bit Name	Description
31:24	STATION_ ADDRESS_1	This field holds the first octet of the station address
23:16	STATION_ ADDRESS_2	This field holds the second octet of the station address
15:8	STATION_ ADDRESS_3	This field holds the third octet of the station address
7:0	STATION_ ADDRESS_4	This field holds the fourth octet of the station address

10.28.15 STA Address 2

GMAC0 Address: 0x19000044
GMAC1 Address: 0x1A000044
Access: Read/Write
Reset: 0x0

This register holds the last two octets of the station address.

Bit	Bit Name	Description
31:24	STATION_ ADDRESS_5	This field holds the fifth octet of the station address
23:16	STATION_ ADDRESS_6	This field holds the sixth octet of the station address
15:0	RES	Reserved

10.28.16 ETH_FIFO RAM Configuration 0

GMAC0 Address: 0x19000048
GMAC1 Address: 0x1A000048
Access: See field description
Reset: 0x0

This register is used to assert and negate functions concerning the ETH module.

Bit	Bit Name	Access	Description	
31:21	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
20	FTFENRPLY	RO	Asserted	The eth_fab module is enabled
			Negated	The eth_fab module is disabled
19	STFENRPLY	RO	Asserted	The eth_sys module is enabled
			Negated	The eth_sys module is disabled
18	FRFENRPLY	RO	Asserted	The eth_fab module is enabled
			Negated	The eth_fab module is disabled
17	SRFENRPLY	RO	Asserted	The eth_sys module is enabled
			Negated	The eth_sys module is disabled
16	WTMENRPLY	RO	Asserted	The eth_wtm module is enabled
			Negated	The eth_wtm module is disabled
15:13	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
12	FTFENREQ	RW	Asserted	Requests enabling of the eth_fab module
			Negated	Requests disabling of the eth_fab module
11	STFENREQ	RW	Asserted	Requests enabling of the eth_sys module
			Negated	Requests disabling of the eth_sys module
10	FRFENREQ	RW	Asserted	Requests enabling of the eth_fab module
			Negated	Requests disabling of the eth_fab module
9	SRFENREQ	RW	Asserted	Requests enabling of the eth_sys module
			Negated	Requests disabling of the eth_sys module
8	WTMENREQ	RW	Asserted	Requests enabling of the eth_wtm module
			Negated	Requests disabling of the eth_wtm module
7:5	RES	RW	Reserved. Must be written with zero. Contains zeros when read.	
4	HSTRSTFT	RW	When asserted, this bit places the eth_fab module in reset	
3	HSTRSTST	RW	When asserted, this bit places the eth_sys module in reset	
2	HSTRSTFR	RW	When asserted, this bit places the eth_fab module in reset	
1	HSTRSTSR	RW	When asserted, this bit places the eth_sys module in reset	
0	HSTRSTWT	RW	When asserted, this bit places the eth_wtm module in reset	

10.28.17 ETH Configuration 1

GMAC0 Address: 0x1900004C
GMAC1 Address: 0x1A00004C
Access: Read/Write
Reset: 0xFFFF

This register is used to configure the ETH storage area.

Bit	Bit Name	Description
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.
27:16	CFGFRTH [11:0]	This hex value represents the minimum number of 4-byte locations to store simultaneously in the receive RAM, relative to the beginning of the frame being input, before FRRDY may be asserted. Note that FRRDY will be latent a certain amount of time due to fabric transmit clock to system transmit clock time domain crossing, and conditional on FRACPT assertion. When set to the maximum value, FRRD may be asserted only after the completion of the input frame. The value of this register must be greater than 18D when HSTDRPLT64 is asserted.
15:0	CFGXOFFRTX	This hexadecimal value represents the number of pause quanta (64-bit times) after an XOFF pause frame has been acknowledged until the ETH reasserts TCRQ if the ETH receive storage level has remained higher than the low watermark.

10.28.18 ETH Configuration 2

GMAC0 Address: 0x19000050
GMAC1 Address: 0x1A000050
Access: Read/Write
Reset: See field description

This register is used to number the minimum amount of 8-byte words in the Rx RAM before pause frames are transmitted.

Bit	Bit Name	Reset	Description
31:29	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
28:16	CFGHWM [12:0]	0xAAA	This hex value represents the maximum number of 8-byte words to store simultaneously in the Rx RAM before TCRQ and PSVAL facilitates an XOFF pause control frame.
15:13	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
12:0	CFGLWM [12:0]	0x555	This hex value represents the minimum number of 8-byte words to store simultaneously in Rx RAM before TCRQ and PSVAL facilitate an XON pause control frame in response to a transmitted XOFF pause control frame.

10.28.19 ETH Configuration 3

GMAC0 Address: 0x19000054
GMAC1 Address: 0x1A000054
Access: Read/Write
Reset: See field description

This register is used denote the minimum number of 4-byte locations to simultaneously store in the Tx RAM before assertion.

Bit	Bit Name	Reset	Description
31:28	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
27:16	CFGHWMFT [11:0]	0x555	This hex value represents the maximum number of 4-byte locations to store simultaneously in Tx RAM before FTHWM is asserted. Note that FTHWM has two FTCLK clock periods of latency before assertion or negation, as should be considered when calculating required headroom for maximum size packets.
15:12	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
11:0	CFGFTTTH [11:0]	0xFFF	This hex value represents the minimum number of 4-byte locations to store simultaneously in the Tx RAM, relative to the beginning of the frame being input, before TPSF is asserted. Note that TPSF is latent for a certain amount of time due to fabric Tx clock system Tx clock time domain crossing. When set to the maximum value, TPSF asserts only after the completion of the input frame.

10.28.20 ETH Configuration 4

GMAC0 Address: 0x19000058
GMAC1 Address: 0x1A000058
Access: Read/Write
Reset: 0x0

This register is used to signal drop frame conditions internal to the Ethernet.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17	Unicast MAC address match	In combination with ETH Configuration 5, page 10-453, bits [17:0] of this register control which frames are dropped and which are sent to the DMA engine. If the bit is set in ETH Configuration 5, page 10-453 and it does not match the value in this bit, then the frame is dropped. For example, for a current packet, if the L2 DA address matches the STA address, a ucastMatch is set. This packet is dropped if (ucastMatch^eth_cfg_4[17]) & ~eth_cfg_5[17] == 1
16	Truncated frame	
15	Long event	
14	VLAN tag detected	
13	Unsupported op. code	
12	Pause frame	
11	Control frame	
10	Dribble nibble	
9	Broadcast	
8	Multicast	
7	OK	
6	Out of range	
5	Length mismatch	
4	CRC error	
3	Code error	
2	False carrier	
1	RX_DV event	
0	Drop event	

10.28.21 ETH Configuration 5

GMAC0 Address: 0x1900005C
GMAC1 Address: 0x1A00005C
Access: Read/Write
Reset: See field description

This register is used to assert or negate bits of the ETH component.

Bit	Bit Name	Reset	Description
31:20	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
19	Byte/Nibble	0x0	This bit should be set to 1 for 1000 MBps, else set to 0.
18	Short Frame	0x0	If set to 1, all frames under 64 bytes are dropped.
17:0	Rx Filter[17:0]	0x3FFFF	If set in this vector, the corresponding field must match exactly in ETH Configuration 4, page 10-452 for the packet to pass on to the DMA engine.

10.28.22 Tx/Rx 64 Byte Frame Counter (TR64)

GMAC0 Address: 0x19000080
GMAC1 Address: 0x1A000080
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were up to 64 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR64	The transmit and receive 64 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which is 64 bytes in length inclusive (excluding framing bits but including FCS bytes).

10.28.23 Tx/Rx 65-127 Byte Frame Counter (TR127)

GMAC0 Address: 0x19000084
GMAC1 Address: 0x1A000084
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 65-127 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR127	The transmit and receive 65–127 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 65-127 bytes in length inclusive (excluding framing bits but including FCS bytes).

10.28.24 Tx/Rx 128-255 Byte Frame Counter (TR255)

GMAC0 Address: 0x19000088
GMAC1 Address: 0x1A000088
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 128-255 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR255	The transmit and receive 128-255 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 128-255 bytes in length inclusive (excluding framing bits but including FCS bytes).

10.28.25 Tx/Rx 256-511 Byte Frame Counter (TR511)

GMAC0 Address: 0x1900008C
GMAC1 Address: 0x1A00008C
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 256-511 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR511	The transmit and receive 256–511 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 256–511 bytes in length inclusive (excluding framing bits but including FCS bytes).

10.28.26 Tx/Rx 512-1023 Byte Frame Counter (TR1K)

GMAC0 Address: 0x19000090
GMAC1 Address: 0x1A000090
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 512-1023 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR1K	The transmit and receive 512–1023 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 512–1023 bytes in length inclusive (excluding framing bits but including FCS bytes).

10.28.27 Tx/Rx 1024-1518 Byte Frame Counter (TRMAX)

GMAC0 Address: 0x19000094
GMAC1 Address: 0x1A000094
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 1024-1518 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TRMAX	The transmit and receive 1024-1518 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 1024-1518 bytes in length inclusive (excluding framing bits but including FCS bytes).

10.28.28 Tx/Rx 1519-1522 Byte VLAN Frame Counter (TRMGV)

GMAC0 Address: 0x19000098
GMAC1 Address: 0x1A000098
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 1519-1522 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TRMGV	The transmit and receive 1519–1522 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 1519–1522 bytes in length inclusive (excluding framing bits but including FCS bytes).

10.28.29 Receive Byte Counter (RXBT)

GMAC0 Address: 0x1900009C
GMAC1 Address: 0x1A00009C
Access: Read/Write
Reset: 0x0

This register is used to count incoming frames and then increment this register accordingly.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:0	RBYT	The receive byte counter. This statistic count register is incremented by the byte count of all frames received, including bad packets but excluding framing bits but including FCS bytes.

10.28.30 Receive Packet Counter (RPKT)

GMAC0 Address: 0x190000A0
GMAC1 Address: 0x1A0000A0
Access: Read/Write
Reset: 0x0

This register is used to count packets received.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	RPKT	The receive packet counter. This register is incremented for each received packet (including bad packets, all Unicast, broadcast and Multicast packets).

10.28.31 Receive FCS Error Counter (RFCS)

GMAC0 Address: 0x190000A4
GMAC1 Address: 0x1A0000A4
Access: Read/Write
Reset: 0x0

This register is used to count frames received between 64-1518 in length and has a FCS error.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RFCS	The received FCS error counter. This register is incremented for each frame received that has an integral 64–1518 length and contains a frame check sequence error.

10.28.32 Receive Multicast Packet Counter (RMCA)

GMAC0 Address: 0x190000A8
GMAC1 Address: 0x1A0000A8
Access: Read/Write
Reset: 0x0

This register is used to count received good standard multicast packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	RMCA	The receive multicast packet counter. This register is incremented for each multicast good frame of lengths smaller than 1518 (non-VLAN) or 1522 (VLAN) excluding broadcast frames. This does not include range/length errors.

10.28.33 Receive Broadcast Packet Counter (RBCA)

GMAC0 Address: 0x190000AC
GMAC1 Address: 0x1A0000AC
Access: Read/Write
Reset: 0x0

This register is used to count received good broadcast frames.

Bit	Bit Name	Description
31:22	RES	Reserved. Must be written with zero. Contains zeros when read.
21:0	RBCA	The receive broadcast packet counter. This register is incremented for each broadcast good frame of lengths smaller than 1518 (non-VLAN) or 1522 (VLAN) excluding multicast frames. This does not include range or length errors.

10.28.34 Receive Control Frame Packet Counter (RXCF)

GMAC0 Address: 0x190000B0
GMAC1 Address: 0x1A0000B0
Access: Read/Write
Reset: 0x0

This register is used to count received MAC control frames.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	RXCF	The receive control frame packet counter. This register is incremented for each MAC control frame received (pause and unsupported).

10.28.35 Receive Pause Frame Packet Counter (RXPF)

GMAC0 Address: 0x190000B4
GMAC1 Address: 0x1A0000B4
Access: Read/Write
Reset: 0x0

This register is used to count received pause frame packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RXPF	The receive pause frame packet counter. This register is incremented each time a valid pause MAC control frame is received.

10.28.36 Receive Unknown OPCode Packet Counter (RXUO)

GMAC0 Address: 0x190000B8
GMAC1 Address: 0x1A0000B8
Access: Read/Write
Reset: 0x0

This register is used to count received MAC control frames that contain an OPCode.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RXUO	The receive unknown OPcode counter. This bit is incremented each time a MAC control frame is received which contains an opcode other than a pause.

10.28.37 Receive Alignment Error Counter (RALN)

GMAC0 Address: 0x190000BC
GMAC1 Address: 0x1A0000BC
Access: Read/Write
Reset: 0x0

This register is used to count received packets with an alignment error.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RALN	The receive alignment error counter. This register is incremented for each received frame from 64–1518 bytes that contains an invalid FCS and is not an integral number of bytes.

10.28.38 Receive Frame Length Error Counter (RFLR)

GMAC0 Address: 0x190000C0
GMAC1 Address: 0x1A0000C0
Access: Read/Write
Reset: 0x0

This register is used to count received frames that have a length error.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	RFLR	The received frame length error counter. this register is incremented for each received frame in which the 802.3 length field did not match the number of data bytes actually received (46–1500 bytes). The counter is not incremented if the length field is not a valid 802.3 length, such as an EtherType value.

10.28.39 Receive Code Error Counter (RCDE)

GMAC0 Address: 0x190000C4
GMAC1 Address: 0x1A0000C4
Access: Read/Write
Reset: 0x0

This register is used to count the number of received frames that had a code error counter.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RCDE	The receive code error counter. This register is incremented each time a valid carrier was present and at least one invalid data symbol was detected.

10.28.40 Receive Carrier Sense Error Counter (RCSE)

GMAC0 Address: 0x190000C8
GMAC1 Address: 0x1A0000C8
Access: Read/Write
Reset: 0x0

This register is used to count the number of frames received that had a false carrier.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RCSE	The receive false carrier counter. This register is incremented each time a false carrier is detected during idle, as defined by a 1 on RX_ER and an 0xE on RXD. This event is reported along with the statistics generated on the next received frame. Only one false carrier condition can be detected and logged between frames.

10.28.41 Receive Undersize Packet Counter (RUND)

GMAC0 Address: 0x190000CC
GMAC1 Address: 0x1A0000CC
Access: Read/Write
Reset: 0x0

This register is used to count the number of received packets that were undersized.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RUND	The receive undersize packet counter. This register is incremented each time a frame is received which is less than 64 bytes in length and contains a valid FCS and were otherwise well formed. This does not include Range Length errors

10.28.42 Receive Oversize Packet Counter (ROVR)

GMAC0 Address: 0x190000D0
GMAC1 Address: 0x1A0000D0
Access: Read/Write
Reset: 0x0

This register is used to count received packets that were oversized.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	ROVR	The receive oversize packet counter., This register is incremented each time a frame is received which exceeded 1518 (non-VLAN) or 1522 (VLAN) and contains a valid FCS and were otherwise well formed. This does not include Range Length errors.

10.28.43 Receive Fragments Counter (RFRG)

GMAC0 Address: 0x190000D4
GMAC1 Address: 0x1A0000D4
Access: Read/Write
Reset: 0x0

This register is used to count received fragmented frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RFRG	The receive fragments counter. This register is incremented for each frame received which is less than 64 bytes in length and contains an invalid FCS. This includes integral and non-integral lengths.

10.28.44 Receive Jabber Counter (RJBR)

GMAC0 Address: 0x190000D8
GMAC1 Address: 0x1A0000D8
Access: Read/Write
Reset: 0x0

This register is used to count received jabber frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RJBR	The received jabber counter. This register is incremented for frames which exceed 1518 (non-VLAN) or 1522 (VLAN) bytes and contains an invalid FCS, including alignment errors.

10.28.45 Receive Dropped Packet Counter (RDRP)

GMAC0 Address: 0x190000DC
GMAC1 Address: 0x1A0000DC
Access: Read/Write
Reset: 0x0

This register is used to count received dropped packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RDRP	The received dropped packets counter. this register is incremented for frames received which are streamed to the system but are later dropped due to a lack of system resources.

10.28.46 Transmit Byte Counter (TXBT)

GMAC0 Address: 0x190000E0
GMAC1 Address: 0x1A0000E0
Access: Read/Write
Reset: 0x0

This register is used to count transmitted bytes.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:0	TXBT	The transmit byte counter. This register is incremented by the number of bytes that were put on the wire including fragments of frames that were involved with collisions. This count does not include preamble/SFD or jam bytes.

10.28.47 Transmit Packet Counter (TPKT)

GMAC0 Address: 0x190000E4
GMAC1 Address: 0x1A0000E4
Access: Read/Write
Reset: 0x0

This register is used to count transmitted packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TPKT	The transmit packet counter. This register is incremented for each transmitted packet (including bad packets, excessive deferred packets, excessive collision packets, late collision packets, all Unicast, Broadcast and Multicast packets.

10.28.48 Transmit Multicast Packet Counter (TMCA)

GMAC0 Address: 0x190000E8
GMAC1 Address: 0x1A0000E8
Access: Read/Write
Reset: 0x0

This register is used to count transmitted multicast packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TMCA	Transmit multicast packet counter. Incremented for each multicast valid frame transmitted (excluding broadcast frames).

10.28.49 Transmit Broadcast Packet Counter (TBCA)

GMAC0 Address: 0x190000EC
GMAC1 Address: 0x1A0000EC
Access: Read/Write
Reset: 0x0

This register is used to count transmitted broadcast packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TBCA	Transmit broadcast packet counter. Incremented for each broadcast frame transmitted (excluding multicast frames).

10.28.50 Transmit Pause Control Frame Counter (TXPF)

GMAC0 Address: 0x190000F0
GMAC1 Address: 0x1A0000F0
Access: Read/Write
Reset: 0x0

This register is used to count transmitted pause control frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TXPF	Transmit pause frame packet counter. Incremented each time a valid pause MAC control frame is transmitted.

10.28.51 Transmit Deferral Packet Counter (TDFR)

GMAC0 Address: 0x190000F4
GMAC1 Address: 0x1A0000F4
Access: Read/Write
Reset: 0x0

This register is used to count transmitted deferral packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TDFR	Transmit deferral packet counter. Incremented for each frame that was deferred on its first transmission attempt. Does not include frames involved in collisions.

10.28.52 Transmit Excessive Deferral Packet Counter (TEDF)

GMAC0 Address: 0x190000F8
GMAC1 Address: 0x1A0000F8
Access: Read/Write
Reset: 0x0

This register is used to count excessive transmitted deferral packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TEDF	Transmit excessive deferral packet counter. Incremented for frames aborted that were deferred for an excessive period of time (3036 byte times).

10.28.53 Transmit Single Collision Packet Counter (TSCL)

GMAC0 Address: 0x190000FC
GMAC1 Address: 0x1A0000FC
Access: Read/Write
Reset: 0x0

This register is used to count transmitted single collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TSCL	Transmit single collision packet counter. Incremented for each frame transmitted that experienced exactly one collision during transmission.

10.28.54 Transmit Multiple Collision Packet (TMCL)

GMAC0 Address: 0x19000100
GMAC1 Address: 0x1A000100
Access: Read/Write
Reset: 0x0

This register is used to count transmitted multiple collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TMCL	Transmit multiple collision packet counter. Incremented for each frame transmitted that experienced 2–15 collisions (including any late collisions) during transmission as defined using the RETRY[3:0] field of the Tx function control register.

10.28.55 Transmit Late Collision Packet Counter (TLCL)

GMAC0 Address: 0x19000104
GMAC1 Address: 0x1A000104
Access: Read/Write
Reset: 0x0

This register is used to count transmitted late collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TLCL	Transmit late collision packet counter. Incremented for each frame transmitted that experienced a late collision during a transmission attempt. Late collisions are defined using the LCOL[5:0] field of the Tx function control register.

10.28.56 Transmit Excessive Collision Packet Counter (TXCL)

GMAC0 Address: 0x19000108
GMAC1 Address: 0x1A000108
Access: Read/Write
Reset: 0x0

This register is used to count excessive transmitted collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TXCL	Transmit excessive collision packet counter. Incremented for each frame that experienced 16 collisions during transmission and was aborted.

10.28.57 Transmit Total Collision Counter (TNCL)

GMAC0 Address: 0x1900010C
GMAC1 Address: 0x1A00010C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted total collision packets.

Bit	Bit Name	Description
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.
12:0	TNCL	Transmit total collision counter. Incremented by the number of collisions experienced during the transmission of a frame as defined as the simultaneous presence of signals on the DO and RD circuits (i.e., transmitting and receiving at the same time). Note, this register does not include collisions that result in an excessive collision condition).

10.28.58 Transmit Pause Frames Honored Counter (TPFH)

GMAC0 Address: 0x19000110
GMAC1 Address: 0x1A000110
Access: Read/Write
Reset: 0x0

This register is used to count honored transmitted pause frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TPFH	Transmit pause frames honored counter. Incremented each time a valid pause MAC control frame is transmitted and honored.

10.28.59 Transmit Drop Frame Counter (TDRP)

GMAC0 Address: 0x19000114
GMAC1 Address: 0x1A000114
Access: Read/Write
Reset: 0x0

This register is used to count transmitted drop frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TDRP	Transmit drop frame counter. Incremented each time input PFH is asserted.

10.28.60 Transmit Jabber Frame Counter (TJBR)

GMAC0 Address: 0x19000118
GMAC1 Address: 0x1A000118
Access: Read/Write
Reset: 0x0

This register is used to count transmitted jabber frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TJBR	Transmit jabber frame counter. Incremented for each oversized transmitted frame with an incorrect FCS value.

10.28.61 Transmit FCS Error Counter (TFCS)

GMAC0 Address: 0x1900011C
GMAC1 Address: 0x1A00011C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted FCS errors.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TFCS	Transmit FCS error counter. Incremented for every valid sized packet with an incorrect FCS value.

10.28.62 Transmit Control Frame Counter (TXCF)

GMAC0 Address: 0x19000120
GMAC1 Address: 0x1A000120
Access: Read/Write
Reset: 0x0

This register is used to count transmitted control frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TXCF	Transmit control frame counter. Incremented for every valid size frame with a type field signifying a control frame.

10.28.63 Transmit Oversize Frame Counter (TOVR)

GMAC0 Address: 0x19000124
GMAC1 Address: 0x1A000124000128
Access: Read/Write
Reset: 0x0

This register is used to count transmitted oversize frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TOVR	Transmit oversize frame counter. Incremented for each oversized transmitted frame with an correct FCS value.

10.28.64 Transmit Undersize Frame Counter (TUND)

GMAC0 Address: 0x19000128
GMAC1 Address: 0x1A000128
Access: Read/Write
Reset: 0x0

This register is used to count transmitted undersize frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TUND	Transmit undersize frame counter. Incremented for every frame less then 64 bytes, with a correct FCS value.

10.28.65 Transmit Fragment Counter (TFRG)

GMAC0 Address: 0x1900012C
GMAC1 Address: 0x1A00012C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted fragments.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TFRG	Transmit fragment counter. Incremented for every frame less then 64 bytes, with an incorrect FCS value.

10.28.66 Carry 1 (CAR1)

GMAC0 Address: 0x19000130
GMAC1 Address: 0x1A000130
Access: Read-Only
Reset: 0x0

Carry register bits are cleared on carry register write while the respective bit is asserted.

Bit	Bit Name	Description
31	C1_64	Carry register 1 TR64 counter carry bit
30	C1_127	Carry register 1 TR127 counter carry bit
29	C1_255	Carry register 1 TR255 counter carry bit
28	C1_511	Carry register 1 TR511 counter carry bit
27	C1_1K	Carry register 1 TR1K counter carry bit
26	C1_MAX	Carry register 1 TRMAX counter carry bit
25	C1_MGV	Carry register 1 TRMGV counter carry bit
24:17	RES	Reserved. Must be written with zero. Contains zeros when read.
16	C1_RBY	Carry register 1 RBYT counter carry bit
15	C1_RPK	Carry register 1 RPKT counter carry bit
14	C1_RFC	Carry register 1 RFCS counter carry bit
13	C1_RMC	Carry register 1 RMCA counter carry bit
12	C1_RBC	Carry register 1 RBCA counter carry bit
11	C1_RXC	Carry register 1 RXCF counter carry bit
10	C1_RXP	Carry register 1 RXPF counter carry bit
9	C1_RXU	Carry register 1 RXUO counter carry bit
8	C1_RAL	Carry register 1 RALN counter carry bit
7	C1_RFL	Carry register 1 RFLR counter carry bit
6	C1_RCD	Carry register 1 RCDE counter carry bit
5	C1_RCS	Carry register 1 RCSE counter carry bit
4	C1_RUN	Carry register 1 RUND counter carry bit
3	C1_ROV	Carry register 1 ROVR counter carry bit
2	C1_RFR	Carry register 1 RFRG counter carry bit
1	C1_RJB	Carry register 1 RJBR counter carry bit
0	C1_RDR	Carry register 1 RDRP counter carry bit

10.28.67 Carry 2 (CAR2)

GMAC0 Address: 0x19000134
GMAC1 Address: 0x1A000134
Access: Read-Only
Reset: 0x0

Carry register bits are cleared on carry register write while the respective bit is asserted.

Bit	Bit Name	Description
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.
19	C2_TJB	Carry register 2 TJBR counter carry bit
18	C2_TFC	Carry register 2 TFCS counter carry bit
17	C2_TCF	Carry register 2 TXCF counter carry bit
16	C2_TOV	Carry register 2 TOVR counter carry bit
15	C2_TUN	Carry register 2 TUND counter carry bit
14	C2_TFG	Carry register 2 TFRG counter carry bit
13	C2_TBY	Carry register 2 TBYT counter carry bit
12	C2_TPK	Carry register 2 TPKT counter carry bit
11	C2_TMC	Carry register 2 TMCA counter carry bit
10	C2_TBC	Carry register 2 TBCA counter carry bit
9	C2_TPF	Carry register 2 TXPF counter carry bit
8	C2_TDF	Carry register 2 TDFR counter carry bit
7	C2_TED	Carry register 2 TEDF counter carry bit
6	C2_TSC	Carry register 2 TSCL counter carry bit
5	C2_TMA	Carry register 2 TMCL counter carry bit
4	C2_TLC	Carry register 2 TLCL counter carry bit
3	C2_TXC	Carry register 2 TXCL counter carry bit
2	C2_TNC	Carry register 2 TNCL counter carry bit
1	C2_TPH	Carry register 2 TPFH counter carry bit
0	C2_TDP	Carry register 2 TDRP counter carry bit

10.28.68 Carry Mask 1 (CAM1)

GMAC0 Address: 0x19000138
GMAC1 Address: 0x1A000138
Access: Read/Write
Reset: 0x1

When one of these mask bits is set to zero, the corresponding interrupt bit is allowed to cause interrupt indications on output CARRY.

Bit	Bit NaM1e	Description
31	M1_64	Mask register 1 TR64 counter carry bit
30	M1_127	Mask register 1 TR127 counter carry bit
29	M1_255	Mask register 1 TR255 counter carry bit
28	M1_511	Mask register 1 TR511 counter carry bit
27	M1_1K	Mask register 1 TR1K counter carry bit
26	M1_MAX	Mask register 1 TRMAX counter carry bit
25	M1_MGV	Mask register 1 TRMGV counter carry bit
24:17	RES	Reserved. Must be written with zero. Contains zeros when read.
16	M1_RBY	Mask register 1 RBYT counter carry bit
15	M1_RPK	Mask register 1 RPKT counter carry bit
14	M1_RFC	Mask register 1 RFCS counter carry bit
13	M1_RMC	Mask register 1 RMCA counter carry bit
12	M1_RBC	Mask register 1 RBCA counter carry bit
11	M1_RXC	Mask register 1 RXCF counter carry bit
10	M1_RXP	Mask register 1 RXPF counter carry bit
9	M1_RXU	Mask register 1 RXUO counter carry bit
8	M1_RAL	Mask register 1 RALN counter carry bit
7	M1_RFL	Mask register 1 RFLR counter carry bit
6	M1_RCD	Mask register 1 RCDE counter carry bit
5	M1_RCS	Mask register 1 RCSE counter carry bit
4	M1_RUN	Mask register 1 RUND counter carry bit
3	M1_ROV	Mask register 1 ROVR counter carry bit
2	M1_RFR	Mask register 1 RFRG counter carry bit
1	M1_RJB	Mask register 1 RJBR counter carry bit
0	M1_RDR	Mask register 1 RDRP counter carry bit

10.28.69 Carry Mask 2 (CAM2)

GMAC0 Address: 0x1900013C
GMAC1 Address: 0x1A00013C
Access: Read/Write
Reset: 0x1

When one of these mask bits is set to zero, the corresponding interrupt bit is allowed to cause interrupt indications on output CARRY.

Bit	Bit Name	Description
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.
19	M2_TJB	Mask register 2 TJBR counter carry bit
18	M2_TFC	Mask register 2 TFCS counter carry bit
17	M2_TCF	Mask register 2 TXCF counter carry bit
16	M2_TOV	Mask register 2 TOVR counter carry bit
15	M2_TUN	Mask register 2 TUND counter carry bit
14	M2_TFG	Mask register 2 TFRG counter carry bit
13	M2_TBY	Mask register 2 TBYT counter carry bit
12	M2_TPK	Mask register 2 TPKT counter carry bit
11	M2_TMC	Mask register 2 TMCA counter carry bit
10	M2_TBC	Mask register 2 TBCA counter carry bit
9	M2_TPF	Mask register 2 TXPF counter carry bit
8	M2_TDF	Mask register 2 TDFR counter carry bit
7	M2_TED	Mask register 2 TEDF counter carry bit
6	M2_TSC	Mask register 2 TSCL counter carry bit
5	M2_TMA	Mask register 2 TMCL counter carry bit
4	M2_TLC	Mask register 2 TLCL counter carry bit
3	M2_TXC	Mask register 2 TXCL counter carry bit
2	M2_TNC	Mask register 2 TNCL counter carry bit
1	M2_TPH	Mask register 2 TPFH counter carry bit
0	M2_TDP	Mask register 2 TDRP counter carry bit

10.28.70 DMA Transfer Control for Queue 0 (DMATXCNTRL_Q0)

GMAC0 Address: 0x19000180
GMAC1 Address: 0x1A000180
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 0

10.28.71 Descriptor Address for Queue 0 Tx (DMATXDESCR_Q0)

GMAC0 Address: 0x19000184
GMAC1 Address: 0x1A000184
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 0
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

10.28.72 Transmit Status (DMATXSTATUS)

GMAC0 Address: 0x19000188
GMAC1 Address: 0x1A000188
Access: Read/Write
Reset: 0x0

This register is used to set the bits and flags regarding the DMA controller and its transferring status.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:16	TXPKTCOUNT	This 8-bit Tx packet counter increments when the DMA controller transfers a packet successfully, and decrements when the host writes a 1 to TXPKTSENT (bit [0]).
15:12	RES	Reserved.
11	TX_UNDERRUN_Q3	Indicates TXUNDERRUN_Q3 as an interrupt source
10	TX_UNDERRUN_Q2	Indicates TXUNDERRUN_Q2 as an interrupt source
9	TX_UNDERRUN_Q1	Indicates TXUNDERRUN_Q1 as an interrupt source
8:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	BUS_ERROR	Indicates that the DMA controller received a host/slave split, error, or retry response
2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	TXUNDERRUN_Q0	This bit is set when the DMA controller reads a set (1) empty flag in the descriptor it is processing
0	TXPKTSENT	Indicates one or more packets transferred successfully. Cleared when TXPKTCOUNT (bits [23:16]) is zero. Writing a 1 to this bit reduces TXPKTCOUNT by one.

10.28.73 Receive Control (DMARXCTRL)

GMAC0 Address: 0x1900018C
GMAC1 Address: 0x1A00018C
Access: Read/Write
Reset: 0x0

This register is used to enable the DMA to receive packets.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	RXENABLE	Allows the DMA to receive packet transfers. When set, the built-in DMA controller begins receiving packets as the FIFO indicates they are available (FRSOF asserted). The DMA controller clears this bit when it encounters an RX overflow or bus error state.

10.28.74 Pointer to Receive Descriptor (DMARXDESCR)

GMAC0 Address: 0x19000190
GMAC1 Address: 0x1A000190
Access: Read/Write
Reset: 0x0

This register is used to find the location of the first TX packet descriptor in the memory.

Bit	Bit Name	Description
31:2	DESCRIPTOR_ ADDRESS	The descriptor address. When the RXENABLE (bit [0] of the Receive Control (DMARXCTRL), page 10-472 register) is set by the host, the DMA controller reads this register to find the host memory location of the first receive packet descriptor.
1:0	RES	Ignored by the DMA controller, because it is a requirement of the system that all descriptors are 32-bit aligned in the host memory.

10.28.75 Receive Status (DMARXSTATUS)

GMAC0 Address: 0x19000194
GMAC1 Address: 0x1A000194
Access: Read/Write
Reset: 0x0

This register is used to set the bits and flags regarding the DMA controller and its receiving status.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:16	RXPKTCOUNT	This 8-bit receive packet counter increments when the DMA controller transfers a packet successfully, and decrements when the host writes a 1 to RXPKTRECEIVED (bit [0]).
15:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	BUSERROR	Indicates that the DMA controller received a host/slave split, error, or retry response
2	RXOVERFLOW	This bit is set when the DMA controller reads a set empty flag in the descriptor it is processing
1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	RXPKT RECEIVED	Indicates that one or more packets were received successfully. This bit is cleared when the RXPKTCOUNT (bits [23:16]) is zero. Writing a 1 to this bit reduces RXPKTCOUNT by one.

10.28.76 Interrupt Mask (DMAINTRMASK)

GMAC0 Address: 0x19000198
GMAC1 Address: 0x1A000198
Access: Read/Write
Reset: 0x0

This register is used to configure interrupt masks for the DMA. Setting a bit to 1 enables the corresponding status signal as an interrupt source. The register DMA Interrupts is the AND of DMA status bits with this register.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11	TX_UNDERRUN_Q3_MASK	Setting this bit 1 enables TXUNDERRUN_Q3(bit [11] in the Transmit Status (DMATXSTATUS) register) as an interrupt source
10	TX_UNDERRUN_Q2_MASK	Setting this bit 1 enables TXUNDERRUN_Q2 (bit [10] in the Transmit Status (DMATXSTATUS) register) as an interrupt source
9	TX_UNDERRUN_Q1_MASK	Setting this bit 1 enables TXUNDERRUN_Q1 (bit [9] in the Transmit Status (DMATXSTATUS) register) as an interrupt source
8	RES	Reserved. Must be written with zero. Contains zeros when read.
7	BUS_ERROR_MASK	Setting this bit to 1 enables BUSERROR (bit [3] in the Receive Status (DMARXSTATUS) register) as an interrupt source
6	RX_OVERFLOW_MASK	Setting this bit to 1 enables RXOVERFLOW (bit [1] in the Receive Status (DMARXSTATUS) register) as in interrupt source
5	RES	Reserved. Must be written with zero. Contains zeros when read.
4	RXPKTRECEIVED_MASK	Enables RXPKTRECEIVED (bit [0] in the Receive Status (DMARXSTATUS) register) as an interrupt source
3	BUSERROR_MASK	Setting this bit to 1 enables BUSERROR (bit [3] in the Transmit Status (DMATXSTATUS) register) as an interrupt source
2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	TX_UNDERRUN_Q0_MASK	Setting this bit 1 enables TXUNDERRUN_Q0 (bit [1] in the Transmit Status (DMATXSTATUS) register) as an interrupt source
0	TXPKTSENT_MASK	Setting this bit to 1 enables TXPKTSENT (bit [0] in the Transmit Status (DMATXSTATUS) register) as an interrupt source

10.28.77 Interrupts (DMAINTERRUPT)

GMAC0 Address: 0x1900019C
GMAC1 Address: 0x1A00019C
Access: Read/Write
Reset: 0x0

This register is used to configure interrupts for the DMA. Flags in this register clear when their corresponding Status bit is cleared.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11	TX_UNDERRUN_Q3	Setting this bit 1 enables TXUNDERRUN_Q3(bit [11] in the Transmit Status (DMATXSTATUS) register) as an interrupt source
10	TX_UNDERRUN_Q2	Setting this bit 1 enables TXUNDERRUN_Q2 (bit [10] in the Transmit Status (DMATXSTATUS) register) as an interrupt source
9	TX_UNDERRUN_Q1	Setting this bit 1 enables TXUNDERRUN_Q1 (bit [9] in the Transmit Status (DMATXSTATUS) register) as an interrupt source
8	RES	Reserved. Must be written with zero. Contains zeros when read.
7	BUS_ERROR_MASK	Setting this bit to 1 records an Rx bus error interrupt when BUS_ERROR (bit [3] in the Receive Status (DMARXSTATUS) register) and BUS_ERROR_MASK (bit [7] of the Interrupt Mask (DMAINTRMASK) register) are both set
6	RX_OVERFLOW_MASK	Setting this bit to 1 records an Rx overflow error interrupt when RX_OVERFLOW (bit [1] in the Receive Status (DMARXSTATUS) register) and RX_OVERFLOW_MASK (bit [6] of the Interrupt Mask (DMAINTRMASK) register) are both set
5	RES	Reserved. Must be written with zero. Contains zeros when read.
4	RXPKT_RECEIVED_MASK	Records a RX_PKT_RECEIVED error interrupt when RX_PKT_RECEIVED (bit [0] in the Receive Status (DMARXSTATUS) register) and RXPKT_RECEIVED_MASK (bit [4] of the Interrupt Mask (DMAINTRMASK) register) are both set
3	BUS_ERROR	Setting this bit to 1 enables BUSERROR (bit [3] in the Transmit Status (DMATXSTATUS) register) and BUSERROR_MASK (bit [3] of the Interrupt Mask (DMAINTRMASK) register) are both set
2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	TX_UNDERRUN_Q0	Setting this bit to 1 enables TX_UNDERRUN (bit [1] in the Transmit Status (DMATXSTATUS) register) and TX_UNDERRUN_MASK (bit [1] of the Interrupt Mask (DMAINTRMASK) register) are both set
0	TXPKTSENT	Set this bit to 1 enables TXPKTSENT (bit [0] in the Transmit Status (DMATXSTATUS) register) and TXPKTSENT_MASK (bit [0] of the Interrupt Mask (DMAINTRMASK) register) are both set

10.28.78 Ethernet TX Burst (ETH_ARB_TX_BURST)

GMAC0 Address: 0x190001A0
GMAC1Address: 0x1A0001A0
Access: Read/Write
Reset: 0x48

Tx and Rx requests are arbitrated based on these parameters. These parameters ensure DDR bandwidth is available to both Tx and Rx until the specified number of DWs transfer. Note that this affects the bandwidth/latency of the data for transmit and receive.

Bit	Bit Name	Description
31:26	RES	Reserved
25:16	MAX_RCV_BURST	Maximum number of DWs to be continuously allowed for Rx
15:10	RES	Reserved
9:0	MAX_TX_BURST	Maximum number of DWs to be continuously allowed for Tx

10.28.79 Current Tx and Rx FIFO Depth (ETH_XFIFO_DEPTH)

GMAC0 Address: 0x190001A8
GMAC1Address: 0x1A0001A8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25:16	CURRENT_RX_FIFO_DEPTH	Current Rx FIFO depth
15:10	RES	Reserved
9:0	CURRENT_TX_FIFO_DEPTH	Current Tx FIFO depth

10.28.80 Ethernet Transmit FIFO Throughput (ETH_TXFIFO_TH)

GMAC0 Address: 0x190001A4
GMAC1 Address: 0x1A0001A4
Access: Read/Write
Reset: See field description

This Ethernet register has a 2 KB Tx FIFO. It is use to determine the minimum and maximum levels of the transfer FIFO and correspondingly keep the transmit levels within the range to keep a continuous data transfer flowing.

Bit	Bit Name	Reset	Description
31:26	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
25:16	TXFIFO_MAXTH	0x1D8	This bit represents the maximum number of double words in the Tx FIFO, and once this limit is surpassed, this bit should be de-asserted
15:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:0	TXFIFO_MINTH	0x160	This bit specifies the minimum number of double words in the Tx FIFO, and if it is less than this value, this bit needs to be asserted.

10.28.81 Ethernet Receive FIFO Threshold (ETH_RXFIFO_TH)

GMAC0 Address: 0x190001AC
GMAC1 Address: 0x1A0001AC
Access: Read/Write
Reset: See field description

This Ethernet register has a 2 KB Rx FIFO. It is used to determine the minimum and maximum levels of the transfer FIFO and correspondingly keep the transmit levels within the range to keep a continuous data transfer flowing.

Bit	Bit Name	Reset	Description
31:10	SCRATCHREG_0	0x28	This bit is a pure scratch pad register that can be used by the CPU for any general purpose.
9:0	RCVFIFO_MINTH	0x0	The minimum number of double words in the receive FIFO. Once this number is reached, this bit needs to be asserted.

10.28.82 Ethernet Free Timer (ETH_FREE_TIMER)

GMAC0 Address: 0x190001B8
GMAC1 Address: 0x1A0001B8
Access: Read/Write
Reset: See field description

This register updates the Ethernet descriptors with time stamps.

Bit	Bit Name	Reset	Description	
31	TIMER_UPDATE	0x1	0	Timer update at the AHB_CLK
			1	Free timer at the AHB_CLK/4
30:21	SCRATCHREG_1	0x0	The pure general purpose register for use by the CPU	
20:0	FREE_TIMER	0x3FFFFF	Free timer	

10.28.83 DMA Transfer Control for Queue 1 (DMATXCNTRL_Q1)

GMAC0 Address: 0x190001C0
GMAC1 Address: 0x1A0001C0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 1

10.28.84 Descriptor Address for Queue 1 Tx (DMATXDESCR_Q1)

GMAC0 Address: 0x190001C4
GMAC1 Address: 0x1A0001C4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 1
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

10.28.85 DMA Transfer Control for Queue 2 (DMATXCNTRL_Q2)

GMAC0 Address: 0x190001C8
GMAC1 Address: 0x1A0001C8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 2

10.28.86 Descriptor Address for Queue 2 Tx (DMATXDESCR_Q2)

GMAC0 Address: 0x190001CC
GMAC1 Address: 0x1A0001CC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 2
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

10.28.87 DMA Transfer Control for Queue 3 (DMATXCNTRL_Q3)

GMAC0 Address: 0x190001D0
GMAC1 Address: 0x1A0001D0 Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 3

10.28.88 Descriptor Address for Queue 3 Tx (DMATXDESCR_Q3)

GMAC0 Address: 0x190001D4
GMAC1 Address: 0x1A0001D4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 3
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

10.28.89 DMA Transfer Arbitration Configuration (DMATXARBCFG)

GMAC0 Address: 0x190001D8
GMAC1 Address: 0x1A0001D8
Access: Read/Write
Reset: See field description

This register is used to select the type of arbitration used for the QoS feature and the weight to be assigned to a particular queue. Note that a weight of zero is not permitted and causes the hardware to misbehave.

Bit	Bit Name	Reset	Description	
31:26	WGT3	0x1	The weight for Queue 3, if WRR has been selected	
25:20	WGT2	0x2	The weight for Queue 2, if WRR has been selected	
19:14	WGT1	0x4	The weight for Queue 1, if WRR has been selected	
13:8	WGT0	0x8	The weight for Queue 0, if WRR has been selected	
7:1	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	RRMODE	0x4	Round robin mode	
			0	Simple priority (Q0 highest priority)
			1	Weighted round robin (WRR)

10.28.90 Tx Status and Packet Count for Queues 1 to 3 (DMATXSTATUS_123)

GMAC0 Address: 0x190001E4
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	RES	Reserved
23:16	TXPKTCOUNT_CH3	8-bit Tx packet counter that increments when the built-in DMA controller successfully transfers a packet for queue 3, and decrements when the host writes a 1 to bit TXPKTSENT for chain 3 in the Transmit Status (DMATXSTATUS) register. Default is 0.
15:8	TXPKTCOUNT_CH2	8-bit Tx packet counter that increments when the built-in DMA controller successfully transfers a packet for queue 2, and decrements when the host writes a 1 to bit TXPKTSENT for chain 2 in the Transmit Status (DMATXSTATUS) register. Default is 0.
7:0	TXPKTCOUNT_CH1	8-bit Tx packet counter that increments when the built-in DMA controller successfully transfers a packet for queue 1, and decrements when the host writes a 1 to bit TXPKTSENT for chain 1 in the Transmit Status (DMATXSTATUS) register. Default is 0.

10.28.91 Local MAC Address Dword0 (LCL_MAC_ADDR_DW0)

GMAC0 Address: 0x19000200
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_MAC_ADDR_DW0	Bits [31:0] of the local L2 MAC address

10.28.92 Local MAC Address Dword1 (LCL_MAC_ADDR_DW1)

GMAC0 Address: 0x19000204
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	LOCAL_MAC_ADDR_DW1	Bits [47:32] of the local L2 MAC address

10.28.93 Next Hop Router MAC Address Dword0 (NXT_HOP_DST_ADDR_DW0)

GMAC0 Address: 0x19000208
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_MAC_DST_ADDR_DW0	Bits [31:0] of the next hop router's local L2 MAC address

10.28.94 Next Hop Router MAC Destination Address Dword1 (NXT_HOP_DST_ADDR_DW1)

GMAC0 Address: 0x1900020C
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	LOCAL_MAC_DST_ADDR_DW1	Bits [47:32] of the local L2 MAC address

10.28.95 Local Global IP Address 0 (GLOBAL_IP_ADDR0)

GMAC0 Address: 0x19000210
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_GLOBAL_IP_ADDR0	Local IP address 0 (up to 4 global IP addresses are supported)

10.28.96 Local Global IP Address 1 (GLOBAL_IP_ADDR1)

GMAC0 Address: 0x19000214
GMAC1 Address: 0x1A000214
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_GLOBAL_IP_ADDR1	Local IP address 1 (up to 4 global IP addresses are supported)

10.28.97 Local Global IP Address 2 (GLOBAL_IP_ADDR2)

GMAC0 Address: 0x19000218
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_GLOBAL_IP_ADDR2	Local IP address 2 (up to 4 global IP addresses are supported)

10.28.98 Local Global IP Address 3 (GLOBAL_IP_ADDR3)

GMAC0 Address: 0x1900021C
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_GLOBAL_IP_ADDR3	Local IP address 3 (up to 4 global IP addresses are supported)

10.28.99 Egress NAT Control and Status (EG_NAT_CSR)

GMAC0 Address: 0x19000228
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Reset	Description	
31:7	RES	0x0	Reserved	
6	EG_NAT_FRAG_ EDIT_DISABLE	0x0	Egress NAT fragmentation packet edit disable; Disables NAT editing of the egress fragmented packet	
5:2	EG_FIELD_EDIT_ MASK	0x0	Egress field edit mask; Setting these bits disables the edit of each field in the egress packet.	
			Bit [0]	Disables NAT Edit of L2 DA field in the packet
			Bit [1]	Disables NAT Edit of L2 SA field in the packet
			Bit [2]	Disables NAT Edit of IP SA field in the packet
			Bit [3]	Disables NAT Edit of L4 source port field in the packet
1	EG_LOOKUP _DATA_SWAP	0x0	Egress lookup data swap; Enables byte swapping of the data given by the lookup table before editing the egress packet	
0	EG_NAT _DISABLE	0x1	Egress NAT disable; Disables the egress NAT engine. Packets that are Tx DMAed transmit without going through the NAT engine.	

10.28.100 Egress NAT Counter (EG_NAT_CNTR)

GMAC0 Address: 0x1900022C
Access: Read-Only
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:16	EG_NAT_ERR_COUNTER	Counter indicating the number of packets that were not NAT edited on egress.
15:0	EG_NAT_DONE_COUNTER	Counter indicating the number of packets successfully NAT edited on egress.

10.28.101 Ingress NAT Control and Status (IG_NAT_CSR)

GMAC0 Address: 0x19000230
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Reset	Description
31:14	RES	0x0	Reserved
13	IG_NAT_GLBL_ICMP_REQ_DRP_EN	0x0	Ingress NAT global rule ICMP request packet drop enable; When set to 1, ICMP request packets are dropped. Effective only if bit [8] of this register is set to 1.
12	IG_NAT_GLBL_ICMP_RPLY_DRP_EN	0x0	Ingress NAT global rule ICMP reply packet drop enable; When set to 1, ICMP packets that are neither request nor reply are dropped. Effective only if bit [8] of this register is set to 1.
11	IG_NAT_GLBL_TCP_ACK_DRP_EN	0x0	Ingress NAT global rule TCP SYN/ACK packet drop enable; When set to 1, any TCP packet received that fails NAT and has both the SYN and ACK flags set to 1 are dropped. Effective only if bit [8] of this register is set to 1.
10	IG_NAT_GLBL_TCP_SYN_DRP_EN	0x0	Ingress NAT global rule TCP SYN packet drop enable; When set to 1, any TCP packet received that fails NAT and has the SYN flag set to 1 are dropped. Effective only if bit [8] of this register is set to 1.
9	IG_NAT_GLBL_L2_DROP_EN	0x0	Ingress NAT global rule L2 drop enable; When set to 1, packets that do not match the L2 LOCAL_MAC_ADDR programmed in the Local MAC Address Dword0 (LCL_MAC_ADDR_DW0) and Local MAC Address Dword1 (LCL_MAC_ADDR_DW1) registers are dropped. Effective only if bit [8] of this register is set to 1.
8	IG_NAT_GLBL_RULE_EN	0x0	Ingress NAT global rule enable; Enables the basic firewall to drop packets for certain global rules based on bits [13:9] of this register
7	IG_NAT_FRAG_EDIT_DISABLE	0x0	Ingress NAT fragmentation packet edit disable; Disables NAT editing of the ingress fragmented packet
6	IG_L4CKSUM_EN	0x0	Ingress L4 checksum; Disables NAT editing of ingress fragmented packet
5:2	IG_FIELD_EDIT_MASK[3:0]	0x0	Ingress field edit mask; setting the bits disables the edit of each of the fields in the ingress packet.
			Bit [0] Disables NAT edit of L2 DA field in the packet
			Bit [1] Disables NAT edit of L2 SA field in the packet
			Bit [2] Disables NAT edit of IP DA field in the packet
			Bit [3] Disables NAT edit of L4 dest port field in the packet
1	IG_LOOKUP_DATA_SWAP	0x0	Ingress lookup data swap; Enables byte swapping of the data given by the lookup table before editing the ingress packet
0	IG_NAT_DISABLE	0x1	Ingress NAT disable; Disables the ingress NAT engine. Packets that are received are DMAed without going through the NAT engine.

10.28.102 Ingress NAT Counter (IG_NAT_CNTR)

GMAC0 Address: 0x19000234
Access: Read-Only
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:16	IG_NAT_ERR_COUNTER [EG_NAT_ERR_COUNTER]	Ingress NAT error counter; Counter indicating the number of packets that were not NAT edited on ingress.
15:0	IG_NAT_DONE_COUNTER [EG_NAT_DONE_COUNTER]	Ingress NAT done counter; Counter indicating the number of packets successfully NAT edited on ingress.

10.28.103 Egress ACL Control and Status (EG_ACL_CSR)

GMAC0 Address: 0x19000238
Access: Read-Only
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Reset	Description
31:1	RES	0x0	Reserved
0	EG_ACL_DISABLE	0x1	Egress ACL disable; Disables the egress ACL functionality. Default is 1.

10.28.104 Ingress ACL Control and Status (IG_ACL_CSR)

GMAC0 Address: 0x1900023C
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Reset	Description
31:1	RES	0x0	Reserved
0	iG_ACL_DISABLE	0x1	Ingress ACL disable; Disables the ingress ACL functionality. Default is 1.

10.28.105 Egress ACL CMD0 and Action (EG_ACL_CMD0_AND_ ACTION)

GMAC0 Address: 0x19000240
Access: Read/Write
Reset: 0x0

This register is used to program the ACL table.

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:21	RES	Reserved
20:16	EG_ACL_CMD0	Egress ACL command 0; The CMD0 field of the entry in ACL table.
15:14	RES	Reserved
13:8	EG_ACL_NEP	Egress ACL next entry pointer. Points to the next entry in the ACL Table this entry is linked to. Valid only if bit [1] of this register is set to 1.
7:4	RES	Reserved
3	EG_ACL_ALLOW	Egress ACL allow; When set, the action associated with this entry/rule in the ACL table is to allow the packet.
2	EG_ACL_REJECT	Egress ACL reject; When set, the action associated with this entry/rule in the ACL table is to reject the packet.
1	EG_ACL_LINKED	Egress ACL linked; When set, this entry in the ACL table is linked to another entry in the table.
0	EG_ACL_RULE_HD	Egress ACL rule head; When set, this entry in the ACL table is considered the head of the rule.

10.28.106 Egress ACL CMD1, CMD2, CMD3 and CMD4 (EG_ACL_ CMD1234)

GMAC0 Address: 0x19000244
Access: Read/Write
Reset: 0x0

This register is used to program the ACL table.

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:29	RES	Reserved
28:24	EG_ACL_CMD4	Egress ACL command 4: the CMD4 field of the entry in ACL table
23:21	RES	Reserved
20:16	EG_ACL_CMD3	Egress ACL command 3: the CMD4 field of the entry in ACL table
15:13	RES	Reserved
12:8	EG_ACL_CMD2	Egress ACL command 2: the CMD4 field of the entry in ACL table
7:5	RES	Reserved
4:0	EG_ACL_CMD1	Egress ACL command 1: the CMD4 field of the entry in ACL table

10.28.107 Egress ACL OPERAND 0 (EG_ACL_OPERAND0)

GMAC0 Address: 0x19000248
Access: Read/Write
Reset: 0x0

This register is used to program the ACL table.

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	EG_ACL_OPERAND0	Egress ACL operand 0; The lower order [31:0] bits of the Operand field of the entry in ACL table.

10.28.108 Egress ACL OPERAND 1 (EG_ACL_OPERAND1)

GMAC0 Address: 0x1900024C
Access: Read/Write
Reset: 0x0

This register is used to program the ACL table.

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	EG_ACL_OPERAND0	Egress ACL operand 1; The higher order [63:32] bits of the operand field of the entry in ACL table.

10.28.109 Egress ACL Memory Control (EG_ACL_MEM_CONTROL)

GMAC0 Address: 0x19000250
Access: See field description
Reset: 0x0

This register is used to control the ACL table operations.

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Access	Description
31:15	RES	RO	Reserved
14	EG_ACL_INIT	RW	Egress ACL initialization; When set to 1, the ACL table is initialized to all 0s. Software should always initialize the ACL table before loading entries into the ACL table. This bit clears itself once initialization is done.
13	EG_ACL _GLOBAL_RULE_ VALID	RW	Egress ACL global rule valid
			0 Only individual rules determine the allow/drop of the packets
			1 Bit [12] of this register is valid
12	EG_ACL _GLOBAL_DROP	RW	Egress ACL global drop
			0 The global rule indicates whether to allow the packet, and individual rules drop the packets
			1 The global rule is to drop the packets, and individual rules indicate whether to allow the packet
11	EG_ACL_RULE_ MAP_DONE	RO	Egress ACL rule map done; After the last entry is loaded, when hardware sets this bit to 1, it indicates that the rule mapping is done. Only when hardware sets this bit to 1, the ACL_DISABLE bit in the Egress ACL Control and Status (EG_ACL_CSR) register shall be set to 0 (ACL shall be enabled).
10	EG_ACL_LAST _ENTRY	RW	Egress ACL last entry; Indicates if this is the last entry to write to the ACL table.
9	EG_ACL_ACK _REG	RO	Egress ACL acknowledge; When this bit is ready by software as 1, it indicates that the write or read operation to the ACL table is done.
8	EG_ACL_TABLE_ WR	RW	Egress ACL register write; When software sets this bit to 1 during a write to this register, the entry as pointed by the entry address is written to the ACL table with the fields taken from the earlier registers (e.g., commands or operands). When software sets this bit to 0 during a write to this register, a read from the ACL table is initiated to the entry pointed by the entry address and the entry fields are available in these registers after the ACK bit is set to 1. For write operations, software ensure all these registers and the fields of this register are correctly written.
7:6	RES	RO	Reserved
5:0	EG_ACL_ENTRY_ ADDR	RW	Egress ACL entry addr; The entry address where this entry is to be loaded in the ACL table.

10.28.110 Ingress ACL CMD0 and Action (IG_ACL_CMD0_AND_ ACTION)

GMAC0 Address: 0x19000254
Access: Read/Write
Reset: 0x0

This register is used to program the ACL table.

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:21	RES	Reserved
20:16	IG_ACL_CMD0	Ingress ACL command 0; The CMD0 field of the entry in ACL table.
15:14	RES	Reserved
13:8	IG_ACL_NEP	Ingress ACL next entry pointer; Points to the Next Entry in the ACL Table to which this entry is linked to. Valid only if bit [1] of this register is set to 1.
7:4	RES	Reserved
3	IG_ACL_ALLOW	Ingress ACL allow; When set, the action associated with this entry/rule is to allow the packet.
2	IG_ACL_REJECT	Ingress ACL reject; When set, the action associated with this entry/rule is to reject the packet.
1	IG_ACL_LINKED	Ingress ACL linked; When set, this entry in the ACL table is linked to another entry in the table.
0	IG_ACL_RULE _HD	Ingress ACL rule head; When set, this entry in the ACL table is considered the head of the rule.

10.28.111 Ingress ACL CMD1, CMD2, CMD3 and CMD4 (IG_ACL_ CMD1234)

GMAC0 Address: 0x19000258
Access: Read/Write
Reset: See field description

This register is used to program the ACL table.This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:29	RES	Reserved
28:24	IG_ACL_CMD4	Ingress ACL command 4: the CMD4 field of the entry in ACL table
23:21	RES	Reserved
20:16	IG_ACL_CMD3	Ingress ACL command 3: the CMD4 field of the entry in ACL table
15:13	RES	Reserved
12:8	IG_ACL_CMD2	Ingress ACL command 2: the CMD4 field of the entry in ACL table
7:5	RES	Reserved
4:0	IG_ACL_CMD1	Ingress ACL command 1: the CMD4 field of the entry in ACL table

10.28.112 Ingress ACL OPERAND 0 (IG_ACL_OPERAND0)

GMAC0 Address: 0x1900025C
Access: Read/Write
Reset: See field description

This register is used to program the ACL table.

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	IG_ACL _OPERAND0	Ingress ACL operand 0; The lower order [31:0] bits of the operand field of the entry in ACL table.

10.28.113 Ingress ACL OPERAND 1 (IG_ACL_OPERAND1)

GMAC0 Address: 0x19000260
Access: Read/Write
Reset: See field description

This register is used to program the ACL table.

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	IG_ACL _OPERAND0	Ingress ACL operand 1; The higher order [63:32] bits of the operand field of the entry in ACL table.

10.28.114 Ingress ACL Memory Control (IG_ACL_MEM_CONTROL)

GMAC0 Address: 0x19000264
Access: Read/Write
Reset: See field description

This register is used to control the ACL table operations.

This register is available only for GE0 MAC.

Bit	Bit Name	Access	Description
31:15	RES	RO	Reserved
14	IG_ACL_INIT	RW	Ingress ACL initialization; When set to 1, the ACL table is initialized to all 0s. Software should always initialize the ACL table before loading entries into the ACL table. This bit clears itself once initialization is done.
13	IG_ACL _GLOBAL_RULE_ VALID	RW	Ingress ACL global rule valid 0 Only individual rules determine the allow/drop of the packets 1 Bit [12] of this register is valid
12	IG_ACL _GLOBAL_DROP	RW	Ingress ACL global drop 0 The global rule indicates whether to allow the packet, and individual rules drop the packets 1 The global rule is to drop the packets, and individual rules indicate whether to allow the packet
11	IG_ACL_RULE_ MAP_DONE	RO	Ingress ACL rule map done; After the last entry is loaded, when hardware sets this bit to 1, it indicates that the rule mapping is done. Only when hardware sets this bit to 1, the ACL_DISABLE bit in the Egress ACL Control and Status (EG_ACL_CSR) register shall be set to 0 (ACL shall be enabled).
10	IG_ACL_LAST _ENTRY	RW	Ingress ACL last entry; Indicates if this is the last entry to write to the ACL table.
9	IG_ACL_ACK _RIG	RO	Ingress ACL acknowledge; When this bit is ready by software as 1, it indicates that the write or read operation to the ACL table is done.
8	IG_ACL_TABLE_ WR	RW	Ingress ACL register write; When software sets this bit to 1 during a write to this register, the entry as pointed by the entry address is written to the ACL table with the fields taken from the earlier registers (e.g., commands or operands). When software sets this bit to 0 during a write to this register, a read from the ACL table is initiated to the entry pointed by the entry address and the entry fields are available in these registers after the ACK bit is set to 1. For write operations, software ensure all these registers and the fields of this register are correctly written.
7:6	RES	RO	Reserved
5:0	IG_ACL_ENTRY_ ADDR	RW	Ingress ACL entry addr; The entry address where this entry is to be loaded in the ACL table.

10.28.115 Ingress ACL Counter Group 0 (IG_ACL_COUNTER_GRP0)

GMAC0 Address: 0x19000268
Access: Read-Only
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE3	Counter indicating the number of ingress packets that hit rule 3
23:16	COUNT_IG_RULE2	Counter indicating the number of ingress packets that hit rule 2
15:8	COUNT_IG_RULE1	Counter indicating the number of ingress packets that hit rule 1
7:0	COUNT_IG_RULE0	Counter indicating the number of ingress packets that hit rule 0

10.28.116 Ingress ACL Counter Group 1 (IG_ACL_COUNTER_GRP1)

GMAC0 Address: 0x1900026C
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	BIT NAME	Description
31:24	COUNT_IG_RULE7	Counter indicating the number of ingress packets that hit rule 7
23:16	COUNT_IG_RULE6	Counter indicating the number of ingress packets that hit rule 6
15:8	COUNT_IG_RULE5	Counter indicating the number of ingress packets that hit rule 5
7:0	COUNT_IG_RULE4	Counter indicating the number of ingress packets that hit rule 4

10.28.117 Ingress ACL Counter Group 2 (IG_ACL_COUNTER_GRP2)

GMAC0 Address: 0x19000270
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE11	Counter indicating the number of ingress packets that hit rule 11
23:16	COUNT_IG_RULE10	Counter indicating the number of ingress packets that hit rule 10
15:8	COUNT_IG_RULE9	Counter indicating the number of ingress packets that hit rule 9
7:0	COUNT_IG_RULE8	Counter indicating the number of ingress packets that hit rule 8

10.28.118 Ingress ACL Counter Group 3 (IG_ACL_COUNTER_GRP3)

GMAC0 Address: 0x19000274
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE15	Counter indicating the number of ingress packets that hit rule 15
23:16	COUNT_IG_RULE14	Counter indicating the number of ingress packets that hit rule 14
15:8	COUNT_IG_RULE13	Counter indicating the number of ingress packets that hit rule 13
7:0	COUNT_IG_RULE12	Counter indicating the number of ingress packets that hit rule 12

10.28.119 Ingress ACL Counter Group 4 (IG_ACL_COUNTER_GRP4)

GMAC0 Address: 0x19000278
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE19	Counter indicating the number of ingress packets that hit rule 19
23:16	COUNT_IG_RULE18	Counter indicating the number of ingress packets that hit rule 18
15:8	COUNT_IG_RULE17	Counter indicating the number of ingress packets that hit rule 17
7:0	COUNT_IG_RULE16	Counter indicating the number of ingress packets that hit rule 16

10.28.120 Ingress ACL Counter Group 5 (IG_ACL_COUNTER_GRP5)

GMAC0 Address: 0x1900027C
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE23	Counter indicating the number of ingress packets that hit rule 23
23:16	COUNT_IG_RULE22	Counter indicating the number of ingress packets that hit rule 22
15:8	COUNT_IG_RULE21	Counter indicating the number of ingress packets that hit rule 21
7:0	COUNT_IG_RULE20	Counter indicating the number of ingress packets that hit rule 20

10.28.121 Ingress ACL Counter Group 6 (IG_ACL_COUNTER_GRP6)

GMAC0 Address: 0x19000280
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE27	Counter indicating the number of ingress packets that hit rule 27
23:16	COUNT_IG_RULE26	Counter indicating the number of ingress packets that hit rule 26
15:8	COUNT_IG_RULE25	Counter indicating the number of ingress packets that hit rule 25
7:0	COUNT_IG_RULE24	Counter indicating the number of ingress packets that hit rule 24

10.28.122 Ingress ACL Counter Group 7 (IG_ACL_COUNTER_GRP7)

GMAC0 Address: 0x19000284
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE31	Counter indicating the number of ingress packets that hit rule 31
23:16	COUNT_IG_RULE30	Counter indicating the number of ingress packets that hit rule 30
15:8	COUNT_IG_RULE29	Counter indicating the number of ingress packets that hit rule 29
7:0	COUNT_IG_RULE28	Counter indicating the number of ingress packets that hit rule 28

10.28.123 Ingress ACL Counter Group 8 (IG_ACL_COUNTER_GRP8)

GMAC0 Address: 0x19000288
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE35	Counter indicating the number of ingress packets that hit rule 35
23:16	COUNT_IG_RULE34	Counter indicating the number of ingress packets that hit rule 34
15:8	COUNT_IG_RULE33	Counter indicating the number of ingress packets that hit rule 33
7:0	COUNT_IG_RULE32	Counter indicating the number of ingress packets that hit rule 32

10.28.124 Ingress ACL Counter Group 9 (IG_ACL_COUNTER_GRP9)

GMAC0 Address: 0x1900028C
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE39	Counter indicating the number of ingress packets that hit rule 39
23:16	COUNT_IG_RULE38	Counter indicating the number of ingress packets that hit rule 38
15:8	COUNT_IG_RULE37	Counter indicating the number of ingress packets that hit rule 37
7:0	COUNT_IG_RULE36	Counter indicating the number of ingress packets that hit rule 36

10.28.125 Ingress ACL Counter Group 10 (IG_ACL_COUNTER_ GRP10)

GMAC0 Address: 0x19000290
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE43	Counter indicating the number of ingress packets that hit rule 43
23:16	COUNT_IG_RULE42	Counter indicating the number of ingress packets that hit rule 42
15:8	COUNT_IG_RULE41	Counter indicating the number of ingress packets that hit rule 41
7:0	COUNT_IG_RULE40	Counter indicating the number of ingress packets that hit rule 40

10.28.126 Ingress ACL Counter Group 11 (IG_ACL_COUNTER_ GRP11)

GMAC0 Address: 0x19000294
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE47	Counter indicating the number of ingress packets that hit rule 47
23:16	COUNT_IG_RULE46	Counter indicating the number of ingress packets that hit rule 46
15:8	COUNT_IG_RULE45	Counter indicating the number of ingress packets that hit rule 45
7:0	COUNT_IG_RULE44	Counter indicating the number of ingress packets that hit rule 44

10.28.127 Ingress ACL Counter Group 12 (IG_ACL_COUNTER_GRP12)

GMAC0 Address: 0x19000298
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE51	Counter indicating the number of ingress packets that hit rule 51
23:16	COUNT_IG_RULE50	Counter indicating the number of ingress packets that hit rule 50
15:8	COUNT_IG_RULE49	Counter indicating the number of ingress packets that hit rule 49
7:0	COUNT_IG_RULE48	Counter indicating the number of ingress packets that hit rule 48

10.28.128 Ingress ACL Counter Group 13 (IG_ACL_COUNTER_GRP13)

GMAC0 Address: 0x1900029C
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE55	Counter indicating the number of ingress packets that hit rule 55
23:16	COUNT_IG_RULE54	Counter indicating the number of ingress packets that hit rule 54
15:8	COUNT_IG_RULE53	Counter indicating the number of ingress packets that hit rule 53
7:0	COUNT_IG_RULE52	Counter indicating the number of ingress packets that hit rule 52

10.28.129 Ingress ACL Counter Group 14 (IG_ACL_COUNTER_GRP14)

GMAC0 Address: 0x190002A0
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE59	Counter indicating the number of ingress packets that hit rule 59
23:16	COUNT_IG_RULE58	Counter indicating the number of ingress packets that hit rule 58
15:8	COUNT_IG_RULE57	Counter indicating the number of ingress packets that hit rule 57
7:0	COUNT_IG_RULE56	Counter indicating the number of ingress packets that hit rule 56

10.28.130 Ingress ACL Counter Group 15 (IG_ACL_COUNTER_ GRP15)

GMAC0 Address: 0x190002A4
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_IG_RULE63	Counter indicating the number of ingress packets that hit rule 63
23:16	COUNT_IG_RULE62	Counter indicating the number of ingress packets that hit rule 62
15:8	COUNT_IG_RULE61	Counter indicating the number of ingress packets that hit rule 61
7:0	COUNT_IG_RULE60	Counter indicating the number of ingress packets that hit rule 60

10.28.131 Egress ACL Counter Group 0 (EG_ACL_COUNTER_GRP0)

GMAC0 Address: 0x190002A8
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE3	Counter indicating the number of egress packets that hit rule 3
23:16	COUNT_EG_RULE2	Counter indicating the number of egress packets that hit rule 2
15:8	COUNT_EG_RULE1	Counter indicating the number of egress packets that hit rule 1
7:0	COUNT_EG_RULE0	Counter indicating the number of egress packets that hit rule 0

10.28.132 Egress ACL Counter Group 1 (EG_ACL_COUNTER_GRP1)

GMAC0 Address: 0x190002AC
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE7	Counter indicating the number of egress packets that hit rule 7
23:16	COUNT_EG_RULE6	Counter indicating the number of egress packets that hit rule 6
15:8	COUNT_EG_RULE5	Counter indicating the number of egress packets that hit rule 5
7:0	COUNT_EG_RULE4	Counter indicating the number of egress packets that hit rule 4

10.28.133 Egress ACL Counter Group 2 (EG_ACL_COUNTER_GRP2)

GMAC0 Address: 0x190002B0
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE11	Counter indicating the number of egress packets that hit rule 11
23:16	COUNT_EG_RULE10	Counter indicating the number of egress packets that hit rule 10
15:8	COUNT_EG_RULE9	Counter indicating the number of egress packets that hit rule 9
7:0	COUNT_EG_RULE8	Counter indicating the number of egress packets that hit rule 8

10.28.134 Egress ACL Counter Group 3 (EG_ACL_COUNTER_GRP3)

GMAC0 Address: 0x190002B4
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE15	Counter indicating the number of egress packets that hit rule 15
23:16	COUNT_EG_RULE14	Counter indicating the number of egress packets that hit rule 14
15:8	COUNT_EG_RULE13	Counter indicating the number of egress packets that hit rule 13
7:0	COUNT_EG_RULE12	Counter indicating the number of egress packets that hit rule 12

10.28.135 Egress ACL Counter Group 4 (EG_ACL_COUNTER_GRP4)

GMAC0 Address: 0x190002B8
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE19	Counter indicating the number of egress packets that hit rule 19
23:16	COUNT_EG_RULE18	Counter indicating the number of egress packets that hit rule 18
15:8	COUNT_EG_RULE17	Counter indicating the number of egress packets that hit rule 17
7:0	COUNT_EG_RULE16	Counter indicating the number of egress packets that hit rule 16

10.28.136 Egress ACL Counter Group 5 (EG_ACL_COUNTER_GRP5)

GMAC0 Address: 0x190002BC
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE23	Counter indicating the number of egress packets that hit rule 23
23:16	COUNT_EG_RULE22	Counter indicating the number of egress packets that hit rule 22
15:8	COUNT_EG_RULE21	Counter indicating the number of egress packets that hit rule 21
7:0	COUNT_EG_RULE20	Counter indicating the number of egress packets that hit rule 20

10.28.137 Egress ACL Counter Group 6 (EG_ACL_COUNTER_GRP6)

GMAC0 Address: 0x190002C0
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE27	Counter indicating the number of egress packets that hit rule 27
23:16	COUNT_EG_RULE26	Counter indicating the number of egress packets that hit rule 26
15:8	COUNT_EG_RULE25	Counter indicating the number of egress packets that hit rule 25
7:0	COUNT_EG_RULE24	Counter indicating the number of egress packets that hit rule 24

10.28.138 Egress ACL Counter Group 7 (EG_ACL_COUNTER_GRP7)

GMAC0 Address: 0x190002C4
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE31	Counter indicating the number of egress packets that hit rule 31
23:16	COUNT_EG_RULE30	Counter indicating the number of egress packets that hit rule 30
15:8	COUNT_EG_RULE29	Counter indicating the number of egress packets that hit rule 29
7:0	COUNT_EG_RULE28	Counter indicating the number of egress packets that hit rule 28

10.28.139 Egress ACL Counter Group 8 (EG_ACL_COUNTER_GRP8)

GMAC0 Address: 0x190002C8
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE35	Counter indicating the number of egress packets that hit rule 35
23:16	COUNT_EG_RULE34	Counter indicating the number of egress packets that hit rule 34
15:8	COUNT_EG_RULE33	Counter indicating the number of egress packets that hit rule 33
7:0	COUNT_EG_RULE32	Counter indicating the number of egress packets that hit rule 32

10.28.140 Egress ACL Counter Group 9 (EG_ACL_COUNTER_GRP9)

GMAC0 Address: 0x190002CC
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE39	Counter indicating the number of egress packets that hit rule 39
23:16	COUNT_EG_RULE38	Counter indicating the number of egress packets that hit rule 38
15:8	COUNT_EG_RULE37	Counter indicating the number of egress packets that hit rule 37
7:0	COUNT_EG_RULE36	Counter indicating the number of egress packets that hit rule 36

10.28.141 Egress ACL Counter Group 10 (EG_ACL_COUNTER_ GRP10)

GMAC0 Address: 0x190002D0
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE43	Counter indicating the number of egress packets that hit rule 43
23:16	COUNT_EG_RULE42	Counter indicating the number of egress packets that hit rule 42
15:8	COUNT_EG_RULE41	Counter indicating the number of egress packets that hit rule 41
7:0	COUNT_EG_RULE40	Counter indicating the number of egress packets that hit rule 40

10.28.142 Egress ACL Counter Group 11 (EG_ACL_COUNTER_GRP11)

GMAC0 Address: 0x190002D4
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE47	Counter indicating the number of egress packets that hit rule 47
23:16	COUNT_EG_RULE46	Counter indicating the number of egress packets that hit rule 46
15:8	COUNT_EG_RULE45	Counter indicating the number of egress packets that hit rule 45
7:0	COUNT_EG_RULE44	Counter indicating the number of egress packets that hit rule 44

10.28.143 Egress ACL Counter Group 12 (EG_ACL_COUNTER_GRP12)

GMAC0 Address: 0x190002D8
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE51	Counter indicating the number of egress packets that hit rule 51
23:16	COUNT_EG_RULE50	Counter indicating the number of egress packets that hit rule 50
15:8	COUNT_EG_RULE49	Counter indicating the number of egress packets that hit rule 49
7:0	COUNT_EG_RULE48	Counter indicating the number of egress packets that hit rule 48

10.28.144 Egress ACL Counter Group 13 (EG_ACL_COUNTER_GRP13)

GMAC0 Address: 0x190002DC
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE55	Counter indicating the number of egress packets that hit rule 55
23:16	COUNT_EG_RULE54	Counter indicating the number of egress packets that hit rule 54
15:8	COUNT_EG_RULE53	Counter indicating the number of egress packets that hit rule 53
7:0	COUNT_EG_RULE52	Counter indicating the number of egress packets that hit rule 52

10.28.145 Egress ACL Counter Group 14 (EG_ACL_COUNTER_ GRP14)

GMAC0 Address: 0x190002E0
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE59	Counter indicating the number of egress packets that hit rule 59
23:16	COUNT_EG_RULE58	Counter indicating the number of egress packets that hit rule 58
15:8	COUNT_EG_RULE57	Counter indicating the number of egress packets that hit rule 57
7:0	COUNT_EG_RULE56	Counter indicating the number of egress packets that hit rule 56

10.28.146 Egress ACL Counter Group 15 (EG_ACL_COUNTER_ GRP15)

GMAC0 Address: 0x190002E4
Access: Read/Write
Reset: See field description

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	COUNT_EG_RULE63	Counter indicating the number of egress packets that hit rule 63
23:16	COUNT_EG_RULE62	Counter indicating the number of egress packets that hit rule 62
15:8	COUNT_EG_RULE61	Counter indicating the number of egress packets that hit rule 61
7:0	COUNT_EG_RULE60	Counter indicating the number of egress packets that hit rule 60

10.28.147 Clear ACL Counters (CLEAR_ACL_COUNTERS)

GMAC0 Address: 0x190002E8
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:2	RES	Reserved
1	CLEAR_EG_COUNTERS	Set to clear all the egress ACL counters. Software must write a 0 to enable the ACL counters
0	CLEAR_IG_COUNTERS	Set to clear all the ingress ACL counters. Software must write a 0 to enable the ACL counters

10.29 USB Controller Registers

Table 10-32 summarizes the USB controller registers and the modes they support.

Table 10-32 USB Controller Registers [1]

USB1 Address	USB2 Address	Access	Name	Description	DEV	SPH	Page
Identification Registers Declare the slave interface presence							
0x1B000000	0x1B400000	RO	ID	Identification	X	X	page 504
0x1B000004	0x1B400004	RO	HWGENERAL	General Hardware Parameters	X	X	page 505
0x1B000008	0x1B400008	RO	HWHOST	Host Hardware Parameters		X	page 505
0x1B00000C	0x1B40000C	RO	HWDEVICE	Device Hardware Parameters	X		page 505
0x1B000010	0x1B400010	RO	HWTXBUF	Tx Buffer Hardware Parameters	X	X	page 506
0x1B000014	0x1B400014	RO	HWRXBUF	Rx Buffer Hardware Parameters	X	X	page 506
Device/Host Timer Registers Measure time-related activities							
0x1B000080	0x1B400080	RW	GPTIMER0LD	General Purpose Timer 0 Load	X	X	page 506
0x1B000084	0x1B400084	Varies	GPTIMER0CTRL	General Purpose Timer 0 Control	X	X	page 507
0x1B000088	0x1B400088	RW	GPTIMER1LD	General Purpose Timer 1 Load	X	X	page 507
0x1B00008C	0x1B40008C	RW	GPTIMER1CTRL	General Purpose Timer 1 Control	X	X	page 508
Device/Host Capability Registers Specify the software limits, restrictions, and capabilities of the host/device controller implementation							
0x1B000100	0x1B400100	RO	CAPLENGTH	Capability Register Length	X	X	page 508
0x1B000102	0x1B400102	RO	HCIVERSION	Host Interface Version Number		X	page 509
0x1B000104	0x1B400104	RO	HCSPARAMS	Host Control Structural Parameters		X	page 509
0x1B000108	0x1B400108	RO	HCCPARAMS	Host Control Capability Parameters		X	page 510
0x1B000120	0x1B400120	RO	DCIVERSION	Device Interface Version Number	X		page 510
0x1B000122	0x1B400122	RO	DCCPARAMS	Device Control Capability Parameters	X		page 511
Device/Host Operational Registers							
0x1B000140	0x1B400140	Varies	USBCMD	USB Command	X	X	page 511
0x1B000144	0x1B400144	Varies	USBSTS	USB Status	X	X	page 511
0x1B000148	0x1B400148	RW	USBINTR	USB Interrupt Enable	X	X	page 517
0x1B00014C	0x1B40014C	Varies	FRINDEX	USB Frame Index	X	X	page 519
0x1B000154	0x1B400154	RW	PERIODICLISTBASE	Frame List Base Address		X	page 520
—	—	RW	DEVICEADDR	USB Device Address	X		page 520
0x1B000158	0x1B400158	RW	ASYNCLISTADDR	Next Asynchronous List Address		X	page 520
—	—	RW	Endpointlist_Addr	Address at Endpoint List in Memory	X		page 521
0x1B00015C	0x1B40015C	RW	TTCTRL	TT Status and Control		X	page 521
0x1B000160	0x1B400160	RW	BURSTSIZE	Programmable Burst Size	X	X	page 521
0x1B000164	0x1B400164	RW	TXFILLTUNING	Host Tx Pre-Buffer Packet Tuning		X	page 522
0x1B000178	0x1B400178	RWC	ENDPTNAK	Endpoint NAK	X		page 523

Table 10-32 USB Controller Registers (cont.)[1]

USB1 Address	USB2 Address	Access	Name	Description	DEV	SPH	Page
0x1B00017C	0x1B40017C	RW	ENDPTNAKEN	Endpoint NAK Enable	X		page 523
0x1B000184	0x1B400184	Varies	PORTSC0	Port/Status Control	X	X	page 524
0x1B0001A8	0x1B4001A8	RW	USBMODE	USB Mode	X	X	page 528
0x1B0001AC	0x1B4001AC	RWC	ENDPTSETUPSTAT	Endpoint Setup Status	X		page 530
0x1B0001B0	0x1B4001B0	RWC	ENDPTPRIME	Endpoint Initialization	X		page 530
0x1B0001B4	0x1B4001B4	WC	ENDPTFLUSH	Endpoint De-Initialization	X		page 531
0x1B0001B8	0x1B4001B8	RO	ENDPTSTATUS	Endpoint Status	X		page 531
0x1B0001BC	0x1B4001BC	RWC	ENDPTCOMPLETE	Endpoint Complete	X		page 532
0x1B0001C0	0x1B4001C0	RW	ENDPTCTRL0	Endpoint Control 0	X		page 532
0x1B0001C4	0x1B4001C4	RW	ENDPTCTRL1	Endpoint Control 1	X		page 533
0x1B0001C8	0x1B4001C8	RW	ENDPTCTRL2	Endpoint Control 2	X		page 533
0x1B0001CC	0x1B4001CC	RW	ENDPTCTRL3	Endpoint Control 3	X		page 533
0x1B0001D0	0x1B4001D0	RW	ENDPTCTRL4	Endpoint Control 4	X		page 533
0x1B0001D4	0x1B4001D4	RW	ENDPTCTRL5	Endpoint Control 5	X		page 533

1. DEV = Device Mode
   SPH = Single-Port Host

10.29.1 Identification (ID)

USB1 Address: 0x1B000000
USB2 Address: 0x1B400000
Access: Read-Only
Reset Value: 0x42FA05

Provides a simple way to determine whether the system provides the USB-HS USB 2.0 core and identifies the USB-HS USB 2.0 core and revision number.

Bit	Name	Description
31:24	RES	Reserved. Must be set to 0.
23:16	REVISION[7:0]	Core revision number
15:14	RES	Reserved. Must be set to 1.
13:8	NID[5:0]	Complement version of ID bits [5:0]
7:6	RES	Reserved. Must be set to 0.
5:0	ID	Configuration number; Set to 0x05. Indicates that the peripheral is the USB-HS USB 2.0 core.

10.29.2 General Hardware Parameters (HWGENERAL)

USB1 Address: 0x1B000004
USB2 Address: 0x1B400004
Access: Read-Only
Reset Value: 0x22

Bit	Name	Description
31:10	RES	Reserved. Must be set to 0.
9	SM	VUSB_HS_PHY_SERIAL
8:6	PHYM	VUSB_HS_PHY_TYPE
5:4	PHYW	VUSB_HS_PHY16_8
3	RES	Reserved
2:1	CLKC	VUSB_HS_CLOCK_CONFIGURATION
0	RT	VUSB_HS_RESET_TYPE

10.29.3 Host Hardware Parameters (HWHOST)

USB1 Address: 0x1B000008
USB2 Address: 0x1B400008
Access: Read-Only
Reset Value: 0x1002001

Bit	Name	Description
31:24	TTPER	VUSB_HS_TT_PERIODIC_CONTEXTS
23:16	TTASY	VUSB_HS_TT_ASYNC_CONTEXTS
15:4	RES	Reserved. Must be set to 0.
3:1	NPORT	VUSB_HS_NUM_PORT – 1
0	HC	VUSB_HS_HOST

10.29.4 Device Hardware Parameters (HWDEVICE)

USB1 Address: 0x1B00000C
USB2 Address: 0x1B40000C
Access: Read-Only
Reset Value: 0xD

Bit	Name	Description
31:6	RES	Reserved. Must be set to 0.
5:1	DEVEP	VUSB_HS_DEV_EP
0	DC	Device capable; [0 ≥ VUSB_HS_DEV]

10.29.5 Tx Buffer Hardware Parameters (HWTXBUF)

USB1 Address: 0x1B000010
USB2 Address: 0x1B400010
Access: Read-Only
Reset Value: 0x80060908

Bit	Name	Description
31:24	RES	Reserved. Must be set to 0.
23:16	TXCHANADD	VUSB_HS_TX_CHAN_ADD
15:8	TXADD	VUSB_HS_TX_ADD
7:0	TXBURST	VUSB_HS_TX_BURST

10.29.6 Rx Buffer Hardware Parameters (HWRXBUF)

USB1 Address: 0x1B000014
USB2 Address: 0x1B400014
Access: Read-Only
Reset Value: 0x608

Bit	Name	Description
31:16	RES	Reserved. Must be set to 0.
15:8	RXADD	VUSB_HS_RX_ADD
7:0	RXBURST	VUSB_HS_RX_BURST

10.29.7 General Purpose Timer 0 Load (GPTIMER0LD)

USB1 Address: 0x1B000080
USB2 Address: 0x1B400080
Access: Read/Write
Reset Value: 0

Contains the timer duration or load value.

Bit	Name	Description
31:24	RES	Reserved. Must be set to 0.
23:0	GPTLD	General purpose timer load value. The value to load into the GPTCNT countdown timer on a reset action. This value in this register represents the time (in ms minus 1) for the timer duration.

10.29.8 General Purpose Timer 0 Control (GPTIMER0CTRL)

USB1 Address: 0x1B000084
USB2 Address: 0x1B400084
Access: Read/Write
Reset Value: 0

Contains the timer control. A data field can be queried to determine the running count value. This timer has granularity on 1 µs and can be programmed to over 16 s. This timer supports two modes: a one-shot and a looped count. When the timer counter value goes to zero an interrupt can be generated using the timer interrupts in the USBSTS and USBINTR registers.

Bit	Name	Description	
31	GPTRUN	General purpose timer run (read/write). Enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.	
		0	Timer stop
		1	Timer run
30	GPTRST	General purpose timer reset (write-only)	
		0	No action
		1	Load counter value. Writing a one to this bit reloads GPTCNT with the value in GPTLD.
29:25	RES	Reserved. Must be set to 0.	
24	GPTMODE	General purpose timer mode (read/write). Selects between a single-timer (one-shot) countdown and a looped countdown.	
		0	One-shot. The timer counts down to zero, generates an interrupt, and stops until the counter is reset by software.
		1	Repeat. The timer counts down to zero, generates an interrupt, and automatically reloads the counter to restart.
23:0	GPTCNT	General purpose timer counter (read-only). The running timer value.	

10.29.9 General Purpose Timer 1 Load (GPTIMER1LD)

USB1 Address: 0x1B000088
USB2 Address: 0x1B400088
Access: Read/Write
Reset Value: 0

See also “General Purpose Timer 0 Load (GPTIMER0LD)” on page 506.

Bit	Name	Description
31:24	RES	Reserved. Must be set to 0.
23:0	GPTLD	General purpose timer load value. The value to load into the GPTCNT countdown timer on a reset action. This value in this register represents the time (in ms minus 1) for the timer duration.

10.29.10 General Purpose Timer 1 Control (GPTIMER1CTRL)

USB1 Address: 0x1B00008C
USB2 Address: 0x1B40008C
Access: Read/Write
Reset Value: 0

See also "General Purpose Timer 0 Control (GPTIMER0CTRL)" on page 507.

Bit	Name	Description	
31	GPTRUN	General purpose timer run (read/write). Enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.	
		0	Timer stop
		1	Timer run
30	GPTRST	General purpose timer reset (write-only)	
		0	No action
		1	Load counter value. Writing a one to this bit reloads GPTCNT with the value in GPTLD.
29:25	RES	Reserved. Must be set to 0.	
24	GPTMODE	General purpose timer mode (read/write). Selects between a single-timer (one-shot) countdown and a looped countdown.	
		0	One-shot. The timer counts down to zero, generates an interrupt, and stops until the counter is reset by software.
		1	Repeat. The timer counts down to zero, generates an interrupt, and automatically reloads the counter to restart.
23:0	GPTCNT	General purpose timer counter (read-only). The running timer value.	

10.29.11 Capability Length (CAPLENGTH)

USB1 Address: 0x1B000100
USB2 Address: 0x1B400100
Access: Read-Only
Reset Value: 0x40

Bit	Name	Description
31:8	RES	Reserved. Must be set to 0.
7:0	CAPLENGTH	Capability register length Indicates which offset to add to the beginning of the register base address of the operational registers (see Table 10-32, Device/Host Operational Registers).

10.29.12 Host Interface Version Number (HCIVERSION)

USB1 Address: 0x1B000102
USB2 Address: 0x1B400102
Access: Read-Only

Bit	Name	Description
31:16	RES	Reserved. Must be set to 0.
15:0	HCIVERSION	This two-byte register contains a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision, and the least significant byte is the minor revision.

10.29.13 Host Control Structural Parameters (HCSPARAMS)

USB1 Address: 0x1B000104
USB2 Address: 0x1B400104
Access: Read-Only

Bit	Name	Description	
31:28	RES	Reserved. Must be set to 0.	
27:24	N_TT	Number of transaction translators. Indicates the number of embedded transaction translators associated with the USB2.0 host controller. Always set to 0.	
23:20	N_PTT	Number of ports per transaction translator. Indicates the number of ports assigned to each transaction translator within the USB2.0 host controller.	
19:17	RES	Reserved. Must be set to 0.	
16	PI	Port indicator. Indicates whether ports support port indicator control. This field is always set to 1, so the port status and control registers include a read/writable field for controlling the port indicator state.	
15:12	N_CC	Number of companion controllers. Indicates the number of companion controllers associated with this USB 2.0 host controller. A value larger than zero in this field indicates there are companion USB1.1 host controller(s) and port-ownership hand-offs are supported. High, Full- and Low-speed devices are supported on the host controller root ports.	
11:8	N_PCC	Number of ports per companion controller. Indicates the number of ports supported per internal companion controller; used to indicate the port routing configuration to the system software.	
7:5	RES	Reserved. Must be set to 0.	
4	PPC	Port power control Indicates whether the host controller implementation includes port power control.	
		0	Indicates the ports do not have port power switches. The value of this field affects the functionality of the port power field in each port status and control register.
		1	Indicates the ports have port power switches
3:0	N_PORTS	Number of downstream ports Specifies the number of physical downstream ports implemented on this host controller. The value determines how many port registers are addressable in the operational registers (see Table 10-32, “Device/Host Operational Registers” on page 503). Valid values range from 0x1-0xF. A zero in this field is undefined.	

10.29.14 Host Control Capability Parameters (HCCPARAMS)

USB1 Address: 0x1B000108
USB2 Address: 0x1B400108
Access: Read-Only
Reset Value: 0x0006

Identifies multiple mode control addressing capability.

Bit	Name	Description	
31:16	RES	Reserved. Must be set to 0.	
15:8	EECP	EHCI extended capabilities pointer (default = 0) This optional field indicates the existence of a capabilities list.	
7:4	IST	Isochronous scheduling threshold; Indicates where software can reliably update the isochronous schedule relative to the current position of the executing host controller.	
		bit [7] = 0	The value of the least significant three bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures (one or more) before flushing the state
		bit [7] = 1	Host software assumes the host controller may cache an isochronous data structure for an entire frame
3	RES	Reserved. Must be set to 0.	
2	ASP	Asynchronous schedule park capability (default = 1) The feature can be disabled or enabled and set to a specific level by using the asynchronous schedule park mode enable and asynchronous schedule park mode count fields in the register “USB Command (USBCMD)” on page 511.	
		1	The host controller supports the park feature for high-speed queue heads in the asynchronous schedule
1	PFL	Programmable frame list flag	
		0	System software must use a frame list length of 1024 elements with this host controller. The frame list size field in the register USB Command (USBCMD), page 10-511 is read-only and must be set to zero.
		1	System software can specify and use a smaller frame list and configure the host controller via the frame list size field in the register USB Command (USBCMD), page 10-511. The frame list must always be aligned on a 4K-page boundary, ensuring the frame list is always physically contiguous.
0	ADC	64-bit addressing capability; must be set to 0. 64-bit addressing capability is not supported.	

10.29.15 Device Interface Version Number (DCIVERSION)

USB1 Address: 0x1B000120
USB2 Address: 0x1B400120
Access: Read-Only

Bit	Name	Description
31:16	RES	Reserved. Must be set to 0.
15:0	DCIVERSION	The device controller interface conforms to the two-byte BCD encoding of the interface version number contained in this register.

10.29.16 Device Control Capability Parameters (DCCPARAMS)

USB1 Address: 0x1B000124
USB2 Address: 0x1B400124
Access: Read-Only

Bit	Name	Description
31:9	RES	Reserved. Must be set to 0.
8	HC	Host capable; the controller can operate as an EHCI-compatible USB 2.0 host controller.
7	DC	Device capable; when set to 1, this controller is capable of operating as a USB 2.0 device.
6:5	RES	Reserved. Must be set to 0.
4:0	DEN	Device endpoint number. Indicates the number of endpoints (0-16) built into the device controller. If this controller is not device capable, this field is zero.

10.29.17 USB Command (USBCMD)

USB1 Address: 0x1B000140
USB2 Address: 0x1B400140
Access: See field description
Reset Value: 00080B00h (host mode)
00080000h (device mode)

Bit	Name	Access	Description	
31:24	RES	R	Reserved. Must be set to zero.	
23:16	ITC	RW	Interrupt threshold control. System software uses this field to set the max. rate the host/device controller issues interrupts at. ITC contains the maximum interrupt interval measured in micro-frames.	
			0x0	Immediate (no threshold)
			0x1	1 micro-frame
			0x2	2 micro-frames
			0x4	4 micro-frames
			0x8	8 micro-frames
			0x10	16 micro-frames
			0x20	32 micro-frames
			0x40	64 micro-frames

Bit	Name	Access	Description	
15	FS2	RW/RO	Frame list size Read/write if programmable frame list flag in the register “Host Control Structural Parameters (HCSPARAMS)” on page 509 is set to one. Specifies the size of the frame list that controls which bits in the register “USB Frame Index (FRINDEX)” on page 519 to use for the frame list current index. This field is made up of bits [15, 3:2] of this register.	
			000	1024 elements (4096 bytes) (default)
			001	512 elements (2048 bytes)
			010	256 elements (1024 bytes)
			011	128 elements (512 bytes)
			100	64 elements (256 bytes)
			101	32 elements (128 bytes)
			110	16 elements (64 bytes)
			111	8 elements (32 bytes)
14	ATDTW	RW	Add dTD tripwire (device mode only) Used as a semaphore to ensure the to proper addition of a new dTD to an active (primed) endpoint’s linked list. This bit is set and cleared by software. This bit shall also be cleared by hardware when its state machine is hazard region for which adding a dTD to a primed endpoint may go unrecognized.	
13	SUTW	RW	Setup tripwire (device mode only) Used as a semaphore to ensure the 8-byte setup data payload is extracted from a QH by the DCD without being corrupted. If the setup lockout mode is off, a hazard exists when new setup data arrives while the DCD is copying the setup data payload from the QH for a previous setup packet. This bit is set and cleared by software and cleared by hardware when a hazard exists.	
12	RES	R	Reserved. Must be set to zero.	
11	ASPE	RW/RO	Asynchronous schedule park mode enable (Host mode only) If the asynchronous park capability bit in the register Host Control Structural Parameters (HCSPARAMS) is a one, this bit defaults to 0x1 and is read/write. Otherwise the bit must be a zero and is RO. Software uses this bit to enable or disable park mode.	
			0	Park mode is disabled
			1	Park mode is enabled
10	RES	R	Reserved. Must be set to zero.	
9	ASP1	RW/RO	Asynchronous schedule park mode count (optional) If the asynchronous park capability bit in the register Host Control Structural Parameters (HCSPARAMS) is a one, this field defaults to 0x3 and is read/write. Otherwise it defaults to zero and is RO. Contain a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule before continuing traversal of the asynchronous schedule. Valid values are 0x1–0x3. Software should not write a zero to this bit when park mode is enabled.	
8	ASP0			
7	RES	Reserved. Must be set to zero.		

Bit	Name	Access	Description	
6	IAA	RW	Interrupt on asynchronous advance doorbell (host mode only) Used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule states, it sets the interrupt on the asynchronous advance status bit in the register USB Status (USBSTS). If the interrupt on synchronous advance enable bit in the register USB Interrupt Enable (USBINTR) is set to one, the host controller asserts an interrupt at the next interrupt threshold. The host controller sets this bit to zero after setting the interrupt on the synchronous advance status bit in the register USB Status (USBSTS) to one. Software should not write a one to this bit if asynchronous schedule is inactive.	
5	ASE	RW	Asynchronous schedule enable (host mode only)	
			0	Do not process the asynchronous schedule (default)
			1	Use the register Next Asynchronous List Address (ASYNCLISTADDR) to access the asynchronous schedule
4	PSE	RW	Periodic schedule enable (host mode only)	
			0	Do not process the periodic schedule (default)
			1	Use the register “Frame List Base Address (PERIODICLISTBASE)” on page 520 to access the asynchronous schedule
3	FS1	RW/RO	Frame list size. See bit [15], FS2, for description.	
2	FS0			
1	RST	RW	Controller reset (RESET). Software uses this bit to reset the controller. This bit is set to zero by the host/device controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register.	
			Host	When this bit is set by software, the host controller resets internal pipelines, timers, etc. to the initial values. Any transaction in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. SW should not set this bit to 1 when HCHalted in the register USB Status (USBSTS) is set to 0.
			Device	When software writes a 1 to this bit, the device controller resets internal pipelines, timers, etc. to the initial values. Writing a 1 to this bit when the device is in the attached state is not recommended. To ensure the device is not in attached state before initiating a device controller reset, primed endpoints must be flushed and the run/stop bit [0] set to 0.
0	RS	RW	Run/Stop (1 = Run, 0 = stop (default))	
			Host	When set to a 1, the host controller proceeds with the schedule and continues as long as this bit is set to 1. When this bit is set to 0, the host controller completes the current transaction on the USB then halts. The HCHalted bit in the register USB Status (USBSTS) indicates when the host controller has completed the transaction and stopped. Software should not write a one to this field unless the host controller is stopped.
			Device	Writing a 1 to this bit causes the device controller to enable a pull-up on D+ and initiates an attach event. This bit is not connected to pull-up enable, as the pull-up becomes disabled on transitioning to high-speed mode. This bit to prevents an attach event before the device controller is properly initialized. Writing a 0 causes a detach event.

10.29.18 USB Status (USBSTS)

USB1 Address: 0x1B000144
USB2 Address: 0x1B400144
Access: See field description
Reset Value: 0

Indicates various states of the host/device controller and pending interrupts. This register does not indicate status resulting from a transaction on the serial bus. Software clears some bits in this register by writing a 1 to them.

Bit	Name	Access	Description
31:26	RES	R	Reserved. Must be set to zero.
25	TI	RWC	General purpose timer interrupt 1. Set when the counter in the register “General Purpose Timer 1 Control (GPTIMER1CTRL)” on page 508 transitions to zero. Write-one-to-clear.
24	TI0	RWC	General purpose timer interrupt 0. Set when the counter in the register “General Purpose Timer 0 Control (GPTIMER0CTRL)” on page 507 transitions to zero. Write-one-to-clear.
23:20	RES	R	Reserved. Must be set to zero.
19	UPI	RWC	USB host periodic interrupt. Set by the host controller when the cause of an interrupt is a completion of a USB transaction where the transfer descriptor (TD) has an interrupt on complete (IOC) bit set and the TD was from the periodic schedule. This bit is also set by the host controller when a short packet (the actual number of bytes received was less than the expected number of bytes) is detected and the packet is on the periodic schedule. Write-one-to-clear.
18	UAI	RWC	USB host asynchronous interrupt. Set by the host controller when the cause of an interrupt is a completion of a USB transaction where the TD has an interrupt on complete (IOC) bit set AND the TD was from the asynchronous schedule. This bit is also set by the host controller when a short packet (the actual number of bytes received was less than the expected number of bytes) is detected and the packet is on the asynchronous schedule. Write-one-to-clear.
17	RES	R	Reserved. Must be set to zero.
16	NAKI	RO	Set by hardware when for one endpoint, both the Tx/Rx endpoint NAK bit and the corresponding Tx/Rx endpoint NAK enable bit are set. Automatically cleared by hardware when the all enabled Tx/Rx endpoint NAK bits are cleared.
15	AS	RO	Reports the real status of the asynchronous schedule (host mode only). The host controller is not required to immediately disable or enable the asynchronous schedule when software transitions the asynchronous schedule enable bit in the register “USB Command (USBCMD)” on page 511. When this bit and the asynchronous schedule enable bit are the same value, the asynchronous schedule is either enabled (1) or disabled (0 = Default).
14	PS	RO	Reports the real status of the periodic schedule (host mode only). The host controller is not required to immediately disable or enable the periodic schedule when software transitions the periodic schedule enable bit in the register USB Command (USBCMD). When this bit and the periodic schedule enable bit are the same value, the periodic schedule is either enabled (1) or disabled (0 = Default).
13	RCL	RO	Reclamation (host mode only) Used to detect an empty asynchronous schedule.
12	HCH	RO	HCHalted (host mode only). This bit is a zero whenever the run/stop bit in the register USB Command (USBCMD) is set to one. The host controller sets this bit to one (default setting) after it has stopped executing because the run/stop bit is set to 0, either by software or by the host controller hardware.
11	RES	R	Reserved. Must be set to zero.

Bit	Name	Access	Description	
10	ULPII	RWC	ULPI interrupt. Only present in designs where the configuration constant VUSB_HS_PHY_ULPI = 1.	
9	RES	Reserved. Must be set to zero.		
8	SLI	RWC	DCSuspend. When a device controller enters a suspend state from an active state, this bit is set to 1. Cleared by the device controller upon exiting from a suspend state. Write-one-to-clear.	
7	SRI	RWC	Start-of-(micro-)frame (SOF) received. When the device controller detects a SOF, this bit is set to 1. When a SOF is late, the device controller automatically sets this bit to indicate that an SOF was expected, thus this bit is set about every 1 ms in device FS mode and every 125 ms in HS mode, and synchronized to the received SOF. Because the device controller initializes to FS before connect, this bit is set at an interval of 1 ms during the prelude to connect and chirp. Write-one-to-clear.	
6	URI	RWC	USB reset received (device controller only). When the device controller detects a USB Reset and enters the default state (0), this bit is set to 1. Write-one-to-clear.	
5	AAI	RWC	Interrupt on asynchronous advance (Host mode only). System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a 1 to the interrupt on asynchronous advance doorbell bit in the register USB Command (USBCMD). Indicates the assertion of that interrupt source. Write-one-to-clear.	
4	RES	R	Reserved. Must be set to zero.	
3	FRI	RWC	Frame list rollover (Host mode only). The host controller sets this bit to a 1 when the frame list index rolls over from its maximum value to 0. The exact value at which the rollover occurs depends on frame list size, e.g, if the size (as programmed in the frame list size field of the register USB Command (USBCMD)) is 1024, the frame index register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the host controller sets this bit to 1 every time FHINDEX [12] toggles. Write-one-to-clear.	
2	PCI	RWC	Port change detect	
			Host	The host controller sets this bit to 1 when on any port, a connect status or a port enable/disable change occurs, or the force port resume bit is set as the result of a transition on the suspended port.
			Device	The device controller sets this bit to1 when the port controller enters full- or high-speed operational state. When the port controller exits full- or high-speed operation states due to reset or suspend events, the notification mechanisms are the USB Reset Received bit and the DCSuspend bits respectively. Write-one-to-clear.
1	UEI	RWC	USB error interrupt. When completion of a USB transaction results in an error condition, this bit along with the USBINT bit is set by the host/device controller if the TD on which the error interrupt occurred also had its interrupt on complete (IOC) bit set. Write-one-to-clear.	
0	UI	RWC	USB interrupt. Set by the host/device controller when the cause of an interrupt is a completion of a USB transaction where the TD has an interrupt on complete (IOC) bit set. Also set by the host/device controller when a short packet (the actual number of bytes received was less than the expected number of bytes) is detected. Write-one-to-clear.	

10.29.19 USB Interrupt Enable (USBINTR)

USB1 Address: 0x1B000148
USB2 Address: 0x1B400148
Access: Read/Write
Reset Value: 0

Interrupts to software are enabled with this register. An interrupt is generated when a bit is set and the corresponding interrupt is active. The register still shows interrupt sources even if they are disabled by this register, allowing polling of interrupt events by software.

Bit	Name	Description		
31:26	RES	Reserved. Must be set to zero.		
25	TIE1	General purpose timer interrupt enable 1; when enabled:		
		This bit:	**USBSTS bit:**	**Controller:**
		= 1	GPTINT1 = 1	Issues an interrupt at acknowledged by software clearing the general purpose timer interrupt 1 bit.
24	TIE0	General purpose timer interrupt enable 0; when enabled:		
		This bit:	**USBSTS bit:**	**Controller:**
		= 1	GPTINT0 = 1	Issues an interrupt at acknowledged by software clearing the general purpose timer interrupt 0 bit.
23:20	RES	Reserved. Must be set to zero.		
19	UPIE	USB host periodic interrupt enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host controller:**
		= 1	USBHSTPERINT = 1	Issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USB host periodic interrupt bit.
18	UAIE	USB host asynchronous interrupt enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host controller:**
		= 1	USBHSTASYNCINT = 1	Issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USB host asynchronous interrupt bit.
17	RES	Reserved. Must be set to zero.		
16	NAKE	NAK interrupt enable. Set by software if it wants to enable the hardware interrupt for the NAK interrupt bit. When enabled:		
		This bit:	**USBSTS bit:**	**Interrupt:**
		= 1	NAKI = 1	A hardware interrupt is generated.
15:11	RES	Reserved. Must be set to zero.		
10	ULPIE	ULPI enable; when enabled:		
		This bit:	**USBSTS bit:**	**Device Controller:**
		= 1	ULPII = 1	Issues an interrupt acknowledged by software writing a one to the ULPI interrupt bit.
9	RES	Reserved. Must be set to zero.		

Bit	Name	Description		
8	SLE	DC suspend interrupt enable; when enabled: When this bit is 1, and the bit in the register transitions, the device controller issues an interrupt acknowledged by software DCSuspend bit.		
		This bit:	**USBSTS bit:**	**Device Controller:**
		= 1	SLI = 1	Issues an interrupt acknowledged by software writing a one to the DCSuspend bit.
7	SRE	SOF received enable; when enabled:		
		This bit:	**USBSTS bit:**	**Device Controller:**
		= 1	SRI = 1	Issues an interrupt acknowledged by software clearing the interrupt on the SOF received bit.
6	URE	USB reset enable; when enabled:		
		This bit:	**USBSTS bit:**	**Device Controller:**
		= 1	URI = 1	Issues an interrupt acknowledged by software clearing USB reset received bit.
5	AAE	Interrupt on asynchronous advance enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host Controller:**
		= 1	AAI = 1	Issues an interrupt acknowledged by software clearing the interrupt on the asynchronous advance bit.
4	SEE	System error enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host/Device Controller:**
		= 1	SEI = 1	Issues an interrupt acknowledged by software clearing the system error bit.
3	FRE	Frame list rollover enable (host controller only); when enabled:		
		This bit:	**USBSTS bit:**	**Host Controller:**
		= 1	FRI = 1	Issues an interrupt acknowledged by software clearing the frame list rollover bit.
2	PCE	Port change detect enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host/Device Controller:**
		= 1	PCE = 1	Issues an interrupt acknowledged by software clearing the port change detect bit.
1	UEE	USB error interrupt enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host/Device Controller:**
		= 1	USBERRINT = 1	Issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USB error interrupt bit.
0	UE	USB interrupt enable; when enabled:		
		This bit:	**USBSTS bit:**	**Host/Device Controller:**
		= 1	USBINT = 1	Issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USB interrupt bit.

10.29.20 USB Frame Index (FRINDEX)

USB1 Address: 0x1B00014C
USB2 Address: 0x1B40014C
Access: Read/Write (host mode)
Read-Only (device mode)
Reset Value: Undefined (free-running counter)

Used by the host controller to index the periodic frame list. The register updates every 125 ms (once each micro-frame). Bits [*N*:3] are used to select a particular entry in the periodic frame list during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by system software in the frame list size field in the register "USB Command (USBCMD)" on page 511. This register must be written as a DWord. Byte writes produce-undefined results. This register cannot be written unless the Host Controller is in the halted state. A write to this register while the run/stop hit is set to a one produces undefined results. Writes to this register also affect the SOF value.

In device mode this register is read only and, the device controller updates the FRINDEX [13:3] register from the frame number indicated by the SOF marker. Whenever a SOF is received by the USB bus, FRINDEX [13:3] is checked against the SOF marker. If FRINDEX [13:3] is different from the SOF marker, FRINDEX [13:3] is set to the SOF value and FRINDEX [2:0] is set to 0 (i.e., SOF for 1 ms frame). If FRINDEX [13:3] is equal to the SOF value, FRINDEX [2:0] increments (i.e., SOF for 125-µs micro-frame.)

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>31:14</td><td>RES</td><td>Reserved. Must be written to 0.</td></tr>
<tr><td>13:0</td><td>FRINDEX</td><td>Frame index. The value, in this register, increments at the end of each time frame (micro-frame). Bits [N:3] are used for the frame list current index, thus each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index.
In device mode the value is the current frame number of the last frame transmitted. It is not used as an index.
In either mode bits 2:0 indicate the current micro-frame.
The values of N are based on the value of the frame list size field in the register USB Command (USBCMD) when used in host mode:
<table>
<tr><th>USBCMD</th><th>[Frame Size List] Number</th><th>Elements N</th></tr>
<tr><td>000</td><td>1024</td><td>12</td></tr>
<tr><td>001</td><td>512</td><td>11</td></tr>
<tr><td>010</td><td>256</td><td>10</td></tr>
<tr><td>011</td><td>128</td><td>9</td></tr>
<tr><td>100</td><td>64</td><td>8</td></tr>
<tr><td>101</td><td>32</td><td>7</td></tr>
<tr><td>110</td><td>16</td><td>6</td></tr>
<tr><td>111</td><td>8</td><td>5</td></tr>
</table>
</td></tr>
</table>

10.29.21 Frame List Base Address (PERIODICLISTBASE)

USB1 Address: 0x1B000154
USB2 Address: 0x1B400154
Access: Read/Write (writes must be DWord)
Reset Value: 0

Bit	Name	Description
31:12	PERBASE	Contains the beginning address of the periodic frame list in the system memory. HCD loads this register prior to starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kb aligned. The contents of this register are combined with the frame index register (FRINDEX) to enable the host controller to step through the periodic frame list in sequence. (Host mode only)
11:0	RES	Reserved. Must be written to zero.

10.29.22 USB Device Address (DEVICEADDR)

Access: Read/Write
Reset Value: 0

Bit	Name	Description
31:25	USBADR	USB device address After any controller reset or a USB reset, the device address is set to the default address (0). The default address will match all incoming addresses. Software shall reprogram the address after receiving a SET_ADDRESS descriptor.
24	USBADRA	Device address advance (default=0) When written to 0, any writes to USBADR are instantaneous. When this bit is written to 1 at the same time or before USBADR (bits [31:25]) is written, the write to the USBADR field is staged and held in a hidden register. After an IN occurs on endpoint 0 and is ACKed, USBADR is loaded from the holding register. Hardware will automatically clear this bit if: ■ IN is ACKed to endpoint 0 (USBADR is updated from staging register) ■ OUT/SETUP occur to endpoint 0 (USBADR is not updated) ■ Device reset occurs (USBADR is reset to 0) Note: After the status phase of the SET_ADDRESS descriptor, the DCD has 2 ms to program the USBADR field. This mechanism ensures this specification is met when the DCD can not write of the device address within 2ms from the SET_ADDRESS status phase. If the DCD writes the USBADR with USBADRA = 1 after the SET_ADDRESS data phase (before the prime of the status phase), the USBADR is programmed instantly at the correct time and meets the 2 ms USB requirement.
23:0	RES	Reserved. Must be written to zero.

10.29.23 Next Asynchronous List Address (ASYNCLISTADDR)

USB1 Address: 0x1B000158
USB2 Address: 0x1B400158
Access: Read/Write (writes must be DWord)
Reset Value: 0

Bit	Name	Description
31:5	ASYBASE	LPL (host mode only). Corresponds to memory address signals [31:5], respectively.
4:0	RES	Reserved. Must be written to zero.

10.29.24 Address at Endpointlist in Memory (ENEDPOINTLIST_ ADDR)

Access: Read/Write
Reset Value: 0

Bit	Name	Description
31:11	EPBASE	Endpoint list pointer (low). These bits correspond to memory address signals [31:11], respectively. This field references a list of up to 32 queue heads, i.e., one queue head per endpoint and direction. In device mode, this register contains the address of the top of the endpoint list in system memory. Bits [10:0] of this register cannot be modified by the system software and will always return a zero when read.The memory structure referenced by this physical memory pointer is assumed 64-byte.
10:0	RES	Reserved. Must be written to zero.

10.29.25 TT Status and Control (TTCTRL)

USB1 Address: 0x1B00015C
USB2 Address: 0x1B40015C
Access: Read/Write (writes must be DWord)
Reset Value: 0

Bit	Name	Description
31	RES	Reserved. Must be written to zero.
30:24	TTHA	Internal TT hub address representation. Used to match against the hub address field in queue head and SITD to determine whether the packet is routed to the internal TT for directly attached FS/LS devices. If the hub address in the queue head or SITD does not match this address, the packet is broadcast on the high speed ports destined for a downstream high speed hub with the address in the queue head or SITD. This register contains parameters needed for internal TT operations. This register is not used in the device controller operation.
23:0	RES	Reserved. Must be written to zero.

10.29.26 Programmable Burst Size (BURSTSIZE)

USB1 Address: 0x1B000160
USB2 Address: 0x1B400160
Access: Read/Write (writes must be DWord)
Reset Value: 0

Bit	Name	Description
31:16	RES	Reserved. Must be written to zero.
15:8	TXPBURST	Programmable Tx burst length. Represents the maximum length of the burst in 32-bit words while moving data from system memory to the USB bus. The default is the constant VUSB_HS_TX_BURST.
7:0	RXPBURST	Programmable Rx burst length. Represents the maximum length of the burst in 32-bit words while moving data from the USB bus to system memory. The default is the constant VUSB_HS_RX_BURST.

10.29.27 Host Tx Pre-Buffer Packet Tuning (TXFILLTUNING)

USB1 Address: 0x1B000164
USB2 Address: 0x1B400164
Access: Read/Write (writes must be DWord)
Reset Value: See field description

Definitions:

T_0	Standard packet overload
T_1	Time for send data payload
T_{FF}	Time to fetch a packet into Tx FIFO up to specified level
T_S	Total packet flight time (send-only) packet = $T_0 + T_1$
T_P	Total packet time (fetch-and-send) packet = $T_{FF} + T_0 + T_1$

Controls performance tuning associated with how the host controller posts data to the Tx latency FIFO before moving the data to the USB bus. The specific areas of performance include how much data to post into the FIFO and an estimate of how long the operation will take in the target system.

On discovery of a Tx packet (OUT/SETUP) in the data structures, the host controller checks whether T_P remains before the end of the (micro-)frame. If so, it pre-fills the Tx FIFO. If during the pre-fill operation the time remaining in the (micro-)frame is < T_S, the packet attempt ceases and the packet is tried at a later time. This condition is not an error and the host controller eventually recovers, but a note of a "back-off" occurrence is made on the scheduler health counter. When a back-off event is detected, the partial packet fetched may need to be discarded from the latency buffer to make room for periodic traffic that begins after the next SOF. Excessive back-off events can waste bandwidth and power on the system bus and thus should be minimized. Back-offs can be minimized with use of the TSCHHEALTH (T_{FF}).

Bit	Name	Reset	Description
31:22	RES	0x0	Reserved. Must be written to zero.
21:16	TXFIFOTHRES	0x2	FIFO burst threshold. Controls the number of data bursts posted to the Tx latency FIFO in host mode before the packet begins on to the bus. The minimum value is 2; this value should be a low as possible to maximize USB performance. A higher value can be used in systems with unpredictable latency and/or insufficient bandwidth where the FIFO may underrun because the data transferred from the latency FIFO to USB occurs before it can be replenished from system memory.
15:13	RES	0x0	Reserved. Must be written to zero.
12:8	TXSCHEALTH	0x0	Scheduler health counter. Increments when the host controller fails to fill the Tx latency FIFO to the level programmed by TXFIFOTHRES before running out of time to send the packet before the next SOF. This health counter measures how many times this occurs to aid in selecting a proper TXSCHOH. Writing to this register clears the counter and this counter maxes out at 31.
7	RES	0x0	Reserved. Must be written to zero.
6:0	TXSCHOH	0x0	Scheduler overload. This register adds an additional fixed offset to the schedule time estimator (T_{FF}). As an approximation, the value chosen for the register should limit the number of back-off events captured in TXSCHHEALTH to less than 10 per second in a highly utilized bus. Choosing a value that is too high for this register is not desired as it can needlessly reduce USB utilization.

10.29.28 Endpoint NAK (ENDPTNAK)

USB1 Address: 0x1B000178
USB2 Address: 0x1B400178
Access: Read/Write-to-Clear
Reset Value: 0

Bit	Name	Description	
31:16	EPTN	Tx endpoint NAK. Each Tx endpoint has 1 bit in this field. The bit is set when the device sends a NAK handshake on a received IN token for the corresponding endpoint.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0
15:0	EPRN	Rx endpoint NAK. Each Rx endpoint has 1 bit in this field. The bit is set when the device sends a NAK handshake on a received OUT or PING token for the corresponding endpoint.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0

10.29.29 Endpoint NAK Enable (ENDPTNAKEN)

USB1 Address: 0x1B00017C
USB2 Address: 0x1B40017C
Access: Read/Write
Reset Value: 0

Bit	Name	Description	
31:16	EPTNE	Tx endpoint NAK enable. Each bit is an enable bit for the corresponding Tx endpoint NAK bit. If this bit is set and the corresponding Tx endpoint NAK bit is set, the NAK interrupt bit is set.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0
15:0	EPRNE	Rx endpoint NAK enable. Each bit is an enable bit for the corresponding Rx endpoint NAK bit. If this bit is set and the corresponding Rx endpoint NAK bit is set, the NAK interrupt bit is set.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0

10.29.30 Port/Status Control (PORTSC0)

USB1 Address: 0x1B000184
USB2 Address: 0x1B400184
Access: See field description
Reset Value: 0x0

- Host Controller
  A host controller must implement one to eight port registers; the number is implemented by a instantiation of a host controller (see the register Host Control Structural Parameters (HCSPARAMS)). Software uses this information as an input parameter to determine how many ports need service. This register is only reset when power is initially applied or in response to a controller reset. The initial conditions of a port are:
  - No device connected
  - Port disabled

  If the port has port power control, this state remains until software applies power to the port by setting port power to one.
- Device Controller
  A device controller must implement only port register one and does not support power control. Port control in device mode is only used for status port reset, suspend, and current connect status. It also initiates test mode or forces signaling and allows software to place the PHY into low power suspend mode and disable the PHY clock.

Bit	Name	Access	Description		
31:30	PTS	RW/RO	Parallel transceiver select; register bit pair used in conjunction with the configuration constant VUSB_HS_PHY_TYPE to control which parallel Tx interface is selected. ■ If VUSB_HS_PHY_TYPE is set for 0-3 then this bit is read only ■ If VUSB_HS_PHY_TYPE is set for 4-7, this bit is read/write This field resets to:		
			00	UTMI/UTMI	If VUSB_HS_PHY_TYPE = 0, 4
			01	RES	Reserved
			10	ULPI	If VUSB_HS_PHY_TYPE = 2, 6
			11	Serial/1.1 PHY	If VUSB_HS_PHY_TYPE = 3, 7 (FS Only)
29	RES	RO	Reserved		
28	PTW	RW/RO	Parallel transceiver width Used in conjunction with the configuration constant VUSB_HS_PHY16_8 to control the data bus width of the UTMI transceiver interface. ■ If VUSB_HS_PHY16_8 is set for 0 or 1, this bit is read-only ■ If VUSB_HS_PHY16_8 is 2 or 3, this bit is read/write This bit resets to 1 if VUSB_HS_PHY16_8 selects a default UTMI interface width of 16-bits else it is reset to 0. This bit has no effect if the serial interface is selected.		
			0	Writing this bit to 0 selects the 8-bit [60 MHz] UTMI interface	
			1	Writing this bit to 1 selects the 16-bit [30 MHz] UTMI interface	
27:26	PSPD	RO	Port speed Indicates the speed at which the port is operating. For HS mode operation in the host controller and HS/FS operation in the device controller the port routing steers data to the protocol engine. For FS and LS mode operation in the host controller, the port routing steers data to the Protocol Engine with the embedded transaction translator.		
			00	Full speed	
			01	Low speed	
			10	High speed	
			11	Not used	

Bit	Name	Access	Description	
25	RES	RO	Reserved. Must be set to zero.	
24	PFSC	RW	Port force full speed connect; Default = 0 (debug mode only) Setting this bit to 1 forces the port to only connect at Full Speed and disables the chirp sequence, allowing the port to identify itself as High Speed (useful for testing FS configurations with a HS host, hub or device).	
23	PHCD	RW	PHY low power suspend: clock disable (PLPSCD)	
			0	Disables the PHY clock (Default)
			1	Enables the PHY clock
			Reading this bit indicates the status of the PHY clock. NOTE: The PHY clock cannot be disabled if it is being used as the system clock.	
			Device Mode	The PHY can be put into Low Power Suspend – Clock Disable when the device is not running (USBCMD Run/Stop = 0) or the host has signaled suspend (PORTSC SUSPEND = 1). Low power suspend clears automatically when the host has signaled resume if using a circuit similar to that in 10. Before forcing a resume from the device, the device controller driver must clear this bit.
			Host Mode	The PHY can be put into Low Power Suspend – Clock Disable when the downstream device has been put into suspend mode or when no downstream device is connected. Low power suspend is completely under the control of software.
22	WKOC	RW	Wake on over-current enable (WKOC_E) (Host mode only)	
			0	This field is zero if Port Power (PP) is zero (Default)
			1	Sensitizes the port to over-current conditions as wake-up events
21	WKDS	RW	Wake on Disconnect Enable (WKDSCNNT_E) (Host mode only)	
			0	This field is zero if Port Power (PP) is zero or in device mode (Default)
			1	Sensitizes the port to device disconnects as wake-up events
20	WKCN	RW	Wake on connect enable (WKCNNT_E) (Host mode only)	
			0	This field is zero if Port Power (PP) is zero or in device mode (Default)
			1	Sensitizes the port to device connects as wake-up events
19:16	PTC[3:0]	RW	Port test control. The FORCE_ENABLE_FS and FORCE ENABLE_LS are extensions to the test mode support. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values forces the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. Note: Low speed operations are not supported as a peripheral device. Any other value than zero indicates that the port is operating in test mode.	
			Value	**Specific Test**
			0000	TEST_MODE_DISABLE (Default)
			0001	J_ STATE
			0010	K_STATE
			0011	SE0 (host) / NAK (device)
			0100	Packet
			0101	FORCE_ENABLE_HS
			0110	FORCE_ENABLE_FS
			0111	FORCE_ENABLE_LS
			1111:1000	Reserved

Bit	Name	Access	Description	
15:14	PIC	RW	Port indicator control. Writes to this field have no effect if the P_INDICATOR bit in the HCSPARAMS register is a zero. If P_INDICATOR bit is a one, then the bit is:	
			Value	**Specific Test**
			00	Port indicators off (Default)
			01	Amber
			10	Green
			11	Undefined
13	PO	RO	Port owner; default = 0. Port owner hand-off is not implemented in this design, therefore this bit always reads back as 0. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device.	
12	RES	RW	Reserved	
11:10	LS	RO	Line status; bit encoding is:	
			Setting	**Meaning**
			00	SE0
			01	J_ STATE
			10	K_STATE
			11	Undefined
			These bits show the current logical levels of the D+ (bit [11]) and D– (bit [10]) signal lines.	
			Device Mode	In device mode, the use of line-state by the device controller driver is not necessary.
			Host Mode	In host mode, the use of line-state by the host controller driver is not necessary (unlike EHCI), because the port controller state machine and the port routing manage the connection of LS and FS.
9	HSP	RO	High-speed port; see also bits [27:26], PSPD	
			0	Connected host/device is not in a high-speed mode (Default)
			1	The host/device connected to the port is in high-speed mode
8	PR	RW/RO	Port reset ■ This field is zero if Port power (PP) is zero ■ When software writes a one to this bit, the bus-reset sequence as defined in USB2.0 is started. This bit automatically changes to zero after reset.	
			Device Mode: Read-Only	
			Host Mode: Read/Write	
			0	Port is not in reset (Default)
			1	Port is in reset

Bit	Name	Access	Description		
7	SUSP	RW/RO	Suspend. Port Enabled Bit and Suspend bit of this register define the port states:		
			Bits	**Port State**	
			0*x*	Disable	
			10	Enable	
			11	Suspend	
			This field is zero if Port Power (PP) is zero in host mode.		
			Device Mode	Read-Only	
				0	Port not in suspend state (Default)
				1	Port in suspend state
			Host Mode	Read/Write In suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. The host controller unconditionally sets this bit to zero when software sets the force port resume bit to zero. The host controller ignores a write of zero to this bit. If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined.	
				0	Port not in suspend state (Default)
				1	Port in suspend state
6	FPR	RW	Force port resume		
			0	No resume (K-state) detected/driven on port (Default)	
			1	Resume detected/driven on port	
			This field is zero if Port Power (PP) is zero in host mode.		
			Device Mode	After the device has been in suspend state for 5 ms or more, software must set this bit to 1 to drive resume signaling before clearing. The device controller sets this bit to one if a J-to-K transition is detected while the port is in the suspend state. The bit will be cleared when the device returns to normal operation. Also, when this bit transitions to a one because a J-to-K transition detected, the port change detect bit in the register USB Status (USBSTS) is also set to one.	
			Host Mode	Software sets this bit to one to drive resume signaling. The host controller sets this bit to one if a J-to-K transition is detected while the port is in the suspend state. When this bit transitions to a one because a J-to-K transition is detected, the port change detect bit in the register USB Status (USBSTS) is also set to one. This bit automatically changes to zero after the resume sequence is complete. This behavior is different from EHCI where the host controller driver is required to set this bit to a zero after the resume duration is timed in the driver.	
5	OCC	RWC	Over-current change. For device-only implementations this bit shall always be 0.		
			0	(Default)	
			1	This bit is set to 1 when there is a change to over-current active. Software clears this bit by writing a one to this bit position.	
4	OCA	RO	Over-current active. For device-only implementations this bit shall always be 0.		
			0	This port does not have an over-current condition. This bit automatically transitions from one to zero when the over-current condition is removed. (Default)	
			1	This port currently has an over-current condition	

Bit	Name	Access	Description		
3	PEC	RWC	Port enable/disable change		
			0	No change (Default)	
			1	Port enabled/disabled status has changed	
			This field is zero if Port Power (PP) is zero.		
			Device Mode	The device port is always enabled (this bit will be zero)	
			Host Mode	For the root hub, this bit gets set to a one only when a port is disabled due to disconnect on the port or due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification). Software clears this by writing a one to it.	
2	PE	RW	Port enabled/disabled		
			0	Disabled (Default)	
			1	Enabled	
			This field is zero if Port Power (PP) is zero in host mode.		
			Device Mode	The device port is always enabled (this bit will be one)	
			Host Mode	Ports can only be enabled by the host controller as a part of reset and enable. Software cannot enable a port by writing a one to this field. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by the host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, (0b) downstream propagation of data is blocked except for reset.	
1	CSC	RWC	Connect status change		
			0	No change (Default)	
			1	Change in current connect status. Software clears this bit by writing a 1 to it.	
			This field is zero if Port Power (PP) is zero in host mode.		
			Device Mode	This bit is undefined in device controller mode.	
			Host Mode	Indicates a change has occurred in the port's current connect status. The host/device controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be setting an already-set bit (that is, the bit will remain set).	
0	CCS	RO	Current connect status		
			Device Mode	0	Not attached (Default); Indicates that the device did not attach successfully or was forcibly disconnected by the software writing a zero to the Run bit in the register USB Command (USBCMD). It does not state the device being disconnected or suspended.
				1	Attached; Indicates that the device successfully attached and is operating in either high speed or full speed as indicated by the high speed port bit in this register.
			Host Mode	This value reflects the current state of the port, and may not correspond directly to the event that caused the connect status change bit to be set. This field is zero if port power (PP) is zero in host mode.	
				0	No device is present. (Default)
				1	Device is present on port.

10.29.31 USB Mode (USBMODE)

USB1 Address: 0x1B0001A8
USB2 Address: 0x1B4001A8

Access: Read/Write
Reset Value: 0

Bit	Name	Description	
31:5	RES	Reserved. Must be written to zero.	
4	SDIS	Stream disable mode ■ 0 = Inactive (Default) ■ 1 = Active	
		Device Mode	Setting to a 1 disables double priming on both Rx and Tx for low bandwidth systems. This mode, when enabled, ensures that the Rx and Tx buffers are sufficient to contain an entire packet, so the usual double buffering scheme is disabled to prevent overruns/underruns in bandwidth limited systems.
		Host Mode	Setting to a 1 ensures that overruns/underruns of the latency FIFO are eliminated for low bandwidth systems where the Rx and Tx buffers are sufficient to contain the entire packet. Enabling stream disable also has the effect of ensuring the Tx latency is filled to capacity before the packet is launched onto the USB.
3	SLOM	Setup lockout mode In device mode, this bit controls behavior of the setup lock mechanism.	
		0	Setup lockouts on (Default)
		1	Setup lockouts off
2	ES	Endian select Can change the byte ordering of transfer buffers to match the host microprocessor bus architecture. The bit fields in the microprocessor interface and the DMA data structures (including the setup buffer within the device QH) are unaffected by the value of this bit, because they are based upon 32-bit words.	
		Bit	**Meaning**
		0	Little Endian (Default). First byte referenced in least significant byte of 32-bit word
		1	Big Endian First byte referenced in most significant byte of 32-bit word
1:0	CM	Controller mode Controller mode is defaulted to the proper mode for host only and device only implementations. For those designs that contain both host and device capability, the controller will default to an idle state and will need to be initialized to the desired operating mode after reset. For combination host/device controllers, this register can only be written once after reset. If it is necessary to switch modes, software must reset the controller by writing to the RESET bit in the register USB Command (USBCMD) before reprogramming this register.	
		Bit	**Meaning**
		00	Idle (Default for combination host/device)
		01	Reserved
		10	Device Controller (Default for device-only controller)
		11	Host Controller (Default for host-only controller)

10.29.32 Endpoint Setup Status (ENDPTSETUPSTAT)

USB1 Address: 0x1B0001AC
USB2 Address: 0x1B4001AC
Access: Read/Write-One-to-Clear
Reset Value: 0x00000000

Bit	Name	Description
31:16	RES	Reserved
15:0	ENDPTSETUPSTAT	Setup endpoint status (Device mode only) For every setup transaction received, a corresponding bit in this register is set to 1. Software must clear or acknowledge the setup transfer by writing a one to a respective bit after it has read the setup data from Queue head. The response to a setup packet as in the order of operations and total response time is crucial to limit bus time outs while the setup lock our mechanism is engaged.

10.29.33 Endpoint Initialization (ENDPTPRIME)

USB1 Address: 0x1B0001B0
USB2 Address: 0x1B4001B0
Access: Read/Write-One-to-Clear
Reset Value: 0x00000000

Bit	Name	Description	
31:16	PETB	Prime endpoint Tx buffer (Device mode only). For each endpoint a corresponding bit is used to request that a buffer prepared for a Tx operation in order to respond to a USB IN/INTERRUPT transaction. Software should write a 1 to the corresponding bit when posting a new transfer descriptor to an endpoint. Hardware automatically uses this bit to begin parsing for a new transfer descriptor from the queue head and prepare a Tx buffer. Hardware clears this bit when the associated endpoint(s) are successfully primed.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0
15:0	PERB	Prime endpoint Rx buffer. For each endpoint a corresponding bit is used to request that a buffer prepared for a Rx operation in order to respond to a USB IN/INTERRUPT transaction. Software should write a 1 to the corresponding bit when posting a new transfer descriptor to an endpoint. Hardware automatically uses this bit to begin parsing for a new transfer descriptor from the queue head and prepare a Rx buffer. Hardware clears this bit when the associated endpoint(s) are successfully primed.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0

10.29.34 Endpoint De-Initialization (ENDPTFLUSH)

USB1 Address: 0x1B0001B4
USB2 Address: 0x1B4001B4
Access: Writing a 1 to a bit causes associated endpoint(s) to clear any primed buffers.
Reset Value: 0This register is for device mode only.

Bit	Name	Description	
31:16	FETB	Flush endpoint Tx buffer. If a packet is in progress for one of the associated endpoints, that transfer continues until completion. Hardware clears this register after the endpoint flush operation.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0
15:0	FERB	Flush endpoint Rx buffer. If a packet is in progress for one of the associated endpoints, that transfer continues until completion. Hardware clears this register after the endpoint flush operation.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0

10.29.35 Endpoint Status (ENDPTSTATUS)

USB1 Address: 0x1B0001B8
USB2 Address: 0x1B4001B8
Access: Read-Only
Reset Value: 0

This register is for device mode only.

Bit	Name	Description	
31:16	ETBR	Endpoint Tx buffer ready One bit for each endpoint indicates status of the respective endpoint buffer. This bit is set to a 1 by the hardware as a response to a command from a corresponding bit in the register Endpoint Initialization (ENDPTPRIME). A delay always occurs between setting a bit in the ENDPTPRIME register and endpoint indicating ready. This delay time varies based upon the current USB traffic and the number of bits set in the ENDPTPRIME register. Buffer ready is cleared by USB reset, by the USB DMA system, or through the ENDPTFLUSH register.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0
15:0	ERBR	Endpoint Rx buffer ready One bit for each endpoint indicates status of the respective endpoint buffer. This bit is set to a 1 by the hardware as a response to a command from a corresponding bit in the register Endpoint Initialization (ENDPTPRIME). A delay always occurs between setting a bit in the ENDPTPRIME register and endpoint indicating ready. This delay time varies based upon the current USB traffic and the number of bits set in the ENDPTPRIME register. Buffer ready is cleared by USB reset, by the USB DMA system, or through the ENDPTFLUSH register.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0

10.29.36 Endpoint Complete (ENDPTCOMPLETE)

USB1 Address: 0x1B0001BC
USB2 Address: 0x1B4001BC
Access: Read/Write-One-to-Clear
Reset Value: 0

This register is for device mode only.

Bit	Name	Description	
31:16	ETCE	Endpoint Tx complete event. Indicates a Tx event (IN/INTERRUPT) occurred and software should read the corresponding endpoint queue to determine the endpoint status. If the corresponding IOC bit is set in the transfer descriptor, this bit is set simultaneously with the register USBINTR.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0
15:0	ERCE	Endpoint Rx complete event. Indicates a Rx event (IN/INTERRUPT) occurred and software should read the corresponding endpoint queue to determine the endpoint status. If the corresponding IOC bit is set in the transfer descriptor, this bit is set simultaneously with the register USBINTR.	
		Bit [15]	Endpoint 15
		...	...
		Bit [1]	Endpoint 1
		Bit [0]	Endpoint 0

10.29.37 Endpoint Control 0 (ENDPTCTRL0)

USB1 Address: 0x1B0001C0
USB2 Address: 0x1B4001C0
Access: Read/Write
Reset Value: 0x0080008

Every device implements Endpoint0 as a control endpoint.

Bit	Name	Description	
31:24	RES	Reserved. Must be written to zero.	
23	TXE	Tx endpoint enable. Endpoint 0 is always enabled; this bit is always 1.	
22:20	RES	Reserved. Must be written to zero.	
19:18	TXT	Tx endpoint type (0 = Control). Endpoint 0 is always 0; this bit is always 0.	
17	RES	Reserved. Must be written to zero.	
16	TXS	Tx endpoint stall	
		0	Endpoint OK (Default)
		1	Endpoint stalled
15:8	RES	Reserved. Must be written to zero.	
7	RXE	Rx endpoint enable. Endpoint 0 is always enabled; this bit is always 1.	
6:4	RES	Reserved. Must be written to zero.	
3:2	RXT	Rx endpoint type (0 = Control). Endpoint 0 is fixed as a control endpoint; this bit is always 0	
1	RES	Reserved. Must be written to zero.	
0	RXS	Rx endpoint stall	
		0	Endpoint OK (Default)
		1	Endpoint stalled

10.29.38 Endpoint Control 1 (ENDPTCTRL1)

USB1 Address: 0x1B0001C4 (Endpoint Control 1)
0x1B0001C8 (Endpoint Control 2)
0x1B0001CC (Endpoint Control 3)
0x1B0001D0 (Endpoint Control 4)
0x1B0001D4 (Endpoint Control 5)
USB2 Address: 0x1B4001C4 (Endpoint Control 1)
0x1B4001C8 (Endpoint Control 2)
0x1B4001CC (Endpoint Control 3)
0x1B4001D0 (Endpoint Control 4)
0x1B4001D4 (Endpoint Control 5)
Access: Read/Write
Reset Value: 0

Bit	Name	Description	
31:24	RES	Reserved. Must be written to zero.	
23	TXE	Tx endpoint enable. An Endpoint should be enabled only after it has been configured	
22	TXR	Tx data toggle reset. When a configuration event is received for this Endpoint, software must write a 1 to this bit in order to synchronize the data PIDs between the host and device.	
21	TXI	Tx data toggle inhibit	
		0	PID sequencing enabled (Default)
		1	PID sequencing disabled
20	RES	Reserved. Must be written to zero.	
19:18	TXT	Tx endpoint type	
		00	Control
		01	Isochronous
		10	Bulk
		11	Interrupt
17	TXD	Tx endpoint data source; should always be written to zero	
16	TXS	Tx endpoint stall	
		0	Endpoint OK (Default)
		1	Endpoint stalled
15:8	RES	Reserved. Must be written to zero.	
7	RXE	Rx endpoint enable. An Endpoint should be enabled only after it has been configured	
6	RXR	Rx data toggle reset. When a configuration event is received for this Endpoint, software must write a 1 to this bit in order to synchronize the data PIDs between the host and device.	
5	RXI	Rx data toggle inhibit	
		0	PID sequencing enabled (Default)
		1	PID sequencing disabled
4:3	RES	Reserved. Must be written to zero.	
2	RXT	Rx endpoint type	
		00	Control
		01	Isochronous
		10	Bulk
		11	Interrupt
1	RXD	Rx endpoint data source; should always be written to zero	
0	RXS	Rx endpoint stall	
		0	Endpoint OK (Default)
		1	Endpoint stalled

10.30 NAND Flash Registers

Table 10-33 summarizes the NAND flash registers.

Table 10-33 NAND Flash Registers

Offset	Name	Description	Page
0x1B000200	COMMAND	Controller Commands	page 535
0x1B000204	CONTROL	Main Configuration	page 535
0x1B000208	STATUS	Controller Status	page 537
0x1B00020C	INT_MASK	Interrupt Mask	page 538
0x1B000210	INT_STATUS	Interrupt Status	page 539
0x1B000214	ECC_CTRL	Configuration Parameters for the ECC Module	page 540
0x1B000218	ECC_OFFSET	Stores the ECC Offset Value	page 540
0x1B00021C	ADDR0_0	Most Significant Part of the Address 0	page 541
0x1B000224	ADDR0_1		
0x1B000220	ADDR1_0	Most Significant Part of the Address 1	page 541
0x1B000228	ADDR1_1		
0x1B000230	SPARE_SIZE	Stores the Value of the NAND Flash Spare Area Size	page 541
0x1B000238	PROTECT	Hardware Protect Against the Write/Erase Process Control	page 542
0x1B000240	LOOKUP_EN	Enables Look-Up During NAND Flash Memory Address	page 542
0x1B000244	LOOKUP0	Lookup Table 0	page 543
0x1B000248	LOOKUP1	Lookup Table 1	
0x1B00024C	LOOKUP2	Lookup Table 2	
0x1B000250	LOOKUP3	Lookup Table 3	
0x1B000254	LOOKUP4	Lookup Table 4	
0x1B000258	LOOKUP5	Lookup Table 5	
0x1B00025C	LOOKUP6	Lookup Table 6	
0x1B000260	LOOKUP7	Lookup Table 7	
0x1B000264	DMA_ADDR	DMA Module Base Address	page 544
0x1B000268	DMA_CNT	DMA Module Counters Initial Value	page 544
0x1B00026C	DMA_CTRL	DMA Module Control	page 545
0x1B000280	MEM_CTRL	Memory Device Control	page 546
0x1B000284	DATA_SIZE	Custom Page Size Value	page 546
0x1B000288	READ_STATUS	Read Status Command Output Value	page 547
0x1B00028C	TIME_SEQ	Command Sequence Timings Configuration	page 547
0x1B000290	TIMING_ASYN	Timing Configuration 0	page 547
0x1B000294	TIMING_SYN	Timing Configuration 1	page 548
0x1B000298	FIFO_DATA	FIFO Module Interface	page 548
0x1B00029C	TIME_MODE	DQS Signal Delay Effect	page 548
0x1B0002A0	DMA_ADDR_ OFFSET	DMA Module Address Offset	page 549
0x1B0002B0	FIFO_INIT	Control for the FIFO Module	page 549
0x1B0002B4	GENERIC_SEQ_ CTRL	Stores Configuration for the Two Generic Sequences	page 549

10.30.1 Controller Commands (COMMAND)

Address Offset: 0x1B000200

The write of the command sequence code to this register triggers the programmed command sequence execution as soon as possible. If execution cannot be done immediately then the transfer to this register is prolonged by the series of the WAIT responses best suited for the selected system bus. For the AHB it is the series of the RETRY responses. Each command sequence can trigger the interrupt when it is completed.

Bit	Bit Name	Description	
31:24	CMD_2	Code of the third command in a sequence	
23:16	CMD_1	Code of the second command in a sequence	
15:8	CMD_0	Code of the first command in a sequence	
7	ADDR_SEL	Address register select flag	
		0	Select address register 0
		1	Select address register 1
6	INPUT_SEL	Input module select flag	
		0	Select the SIU module as input
		1	Select the DMA module as input
5:0	CMD_SEQ	Command code	

10.30.2 Main Configuration (CONTROL)

Address Offset: 0x1B000204

This register stores the configuration parameters that are common to all controller modules.

Bit	Bit Name	Description	
31:22	RES	Reserved	
21	SMALL_BLOCK_EN	Enable small block mode. In this mode controller sends only the single byte as the column address instead of the two bytes as it is done for the big block NAND flash devices.	
20:18	ADDR_CYCLE1	Address cycles: number of address bytes sent to the NAND flash device.	
		000	0 address cycles
		001	1 address cycle
		010	2 address cycles
		011	3 address cycles
		100	4 address cycles
		101	5 address cycles
17	ADDR1_AUTO_INCR	Address auto increment for address register 0	
		0	Auto-increment disabled
		1	Auto-increment enabled
16	ADDR0_AUTO_INCR	Address auto increment for address register 1	
15	WORK_MODE	Controller work mode	
		0	Asynchronous mode
		1	Source synchronous mode

Bit	Bit Name	Description	
14	PROT_EN	Protect mechanism enable	
		0	Protect disable
		1	Protect enable
13	LOOKUP_EN	Lookup enable	
12	IO_WIDTH	NAND flash input/output width. Must be additionally set when the controller is in synchronous mode	
		0	8 bits
		1	16 bits
11	CUSTOM_SIZE_EN	Custom page size enable flag	
		0	Transfer full data page
		1	Transfer custom data block
10:8	PAGE_SIZE	000	256 bytes
		001	512 bytes
		010	1024 bytes
		011	2048 bytes
		100	4096 bytes
		101	8192 bytes
		110	8192 bytes
		111	0 bytes
7:6	BLOCK_SIZE	00	32 pages per block
		01	64 pages per block
		10	128 pages per block
		11	256 pages per block
5	ECC_EN	Hardware ECC support enable	
		0	ECC disabled
		1	ECC enabled
4	INT_EN	Global interrupt enable	
		0	Interrupt disabled
		1	Interrupt enabled
3	SPARE_EN	Spare area enable signal	
		0	Spare area enabled for the given command sequence
		1	Spare area disabled for the given command sequence
2:0	ADDR_CYCLE0	Address cycles: Number of address bytes sent to NAND flash	
		000	0 address cycles
		001	1 address cycle
		010	2 address cycles
		011	3 address cycles
		100	4 address cycles
		101	5 address cycles

10.30.3 Controller Status (STATUS)

Address Offset: 0x1B000208

This register stores the NAND flash controller and connected devices status flags. Those flags can be used by the host controller to implement interleaved devices access.

Bit	Bit Name	Description	
31:10	RES	Reserved	
9	SYN_STAT	Mode busy synchronous bit. Set after the controller change the NAND flash device work mode from the asynchronous to the source synchronous mode.	
		0	Controller ready
		1	Controller busy
8	CTRL_STAT	Main controller status bit. Set after the controller starts to execute the requested command for the selected NAND flash device and is prolonged to the moment when the command sequence part to the moment when the NAND flash device goes to the busy state is finished. As long as this flag is set controller did not accept new command.	
		0	Controller ready
		1	Controller busy
7	MEM7_ST	Device 7 status flag. Corresponds to the NAND flash device with the same index value. The flag gives information about the NAND flash device state.	
		0	Device ready
		1	Device busy
6	MEM6_ST	Device 6 status flag	
5	MEM5_ST	Device 5 status flag	
4	MEM4_ST	Device 4 status flag	
3	MEM3_ST	Device 3status flag	
2	MEM2_ST	Device 2 status flag	
1	MEM1_ST	Device 1 status flag	
0	MEM0_ST	Device 0 status flag	

10.30.4 Interrupt Mask (INT_MASK)

Address Offset: 0x1B00020C

This register allows masking the selected interrupts source in the NAND flash controller. The masked interrupts still sets appropriate bits in the status register, but those changes do not trigger the interrupt.

Bit	Bit Name	Description	
31:13	RES	Reserved	
12	FIFO_ERROR_EN	FIFO error	
		0	Interrupt disabled
		1	Interrupt enabled
11	MEM7_RDY_INT_EN	Memory device 7 is ready for the new command	
		0	Interrupt disabled
		1	Interrupt enabled
10	MEM6_RDY_INT_EN	Memory device 6 is ready for the new command	
9	MEM5_RDY_INT_EN	Memory device 5 is ready for the new command	
8	MEM4_RDY_INT_EN	Memory device 4 is ready for the new command	
7	MEM3_RDY_INT_EN	Memory device 3 is ready for the new command	
6	MEM2_RDY_INT_EN	Memory device 2 is ready for the new command	
5	MEM1_RDY_INT_EN	Memory device 1 is ready for the new command	
4	MEM0_RDY_INT_EN	Memory device 0 is ready for the new command	
3	ECC_TRSH_ERR_EN	The ECC module detected that the error level sat by the ECC_CTRL.ERR_ THRESHOLD was exceeded	
2	ECC_FATAL_ERR_EN	The ECC module detected uncorrectable errors number during read operation	
1	CMD_END_INT_EN	Command sequence ended	
0	PROT_INT_EN	Erase/write protected area attempt interrupt enable	

10.30.5 Interrupt Status (INT_STATUS)

Address Offset: 0x1B000210

This register stores the NAND flash controller interrupt flags. If a bit is set to 0, the corresponding interrupt condition is not met. If set to 1, that interrupt condition is met.

Bit	Bit Name	Description
31:13	RES	Reserved
12	FIFO_ERROR_FL	FIFO error
11	MEM7_RDY_INT_FL	Memory device 7 is ready for the new command
10	MEM6_RDY_INT_FL	Memory device 6 is ready for the new command
9	MEM5_RDY_INT_FL	Memory device 5 is ready for the new command
8	MEM4_RDY_INT_FL	Memory device 4 is ready for the new command
7	MEM3_RDY_INT_FL	Memory device 3 is ready for the new command
6	MEM2_RDY_INT_FL	Memory device 2 is ready for the new command
5	MEM1_RDY_INT_FL	Memory device 1 is ready for the new command
4	MEM0_RDY_INT_FL	Memory device 0 is ready for the new command
3	ECC_TRSH_ERR_FL	The ECC module detected that the error level sat by the ECC_CTRL.ERR_ THRESHOLD was exceeded
2	ECC_FATAL_ERR_FL	The ECC module detected uncorrectable errors number during read operation
1	CMD_FLD_INT_FL	Command sequence ended
0	PROT_INT_FL	Erase/write protected area attempt interrupt enable

10.30.6 Configuration Parameters for the ECC Module (ECC_CTRL)

Address Offset: 0x1B000214

This register stores all configuration parameters required by the ECC module, and stores the ECC module status information. The status fields of the register are ignored during the write process.

Bit	Bit Name	Description	
31:13	RES	Reserved	
12:8	ERR_THRESHOLD	Acceptable errors level. Contains the number of errors acceptable for the host system. This field must be initialized by the host system.	
7:5	ECC_CAP	ECC module correction ability	
		000	2
		001	4
		010	6
		011	8
		100	10
		101	12
		110	14
		111	16
4:3	RES	Reserved	
2	ERR_OVER	Acceptable errors level overflow. Set when the number of errors is greater than the value ERR_THRESHOLD (bits [12:8]).	
1	ERR_UNCORRECT	Uncorrectable error flag. Set when during the read operation the uncorrectable errors occur.	
0	ERR_CORRECT	Correctable error flag. Set when correctable errors occur during the read operation.	

10.30.7 ECC Offset Value (ECC_OFFSET)

Address Offset: 0x1B000218

This register stores the offset value from beginning of the page to the place where correction words will be stored. The register value is valid only if ERR_WORD_POS field of the Configuration Parameters for the ECC Module (ECC_CTRL) register chose the correction words location in the spare area.

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	ECC_OFFSET	Correction words block offset

10.30.8 Most Significant Part of the Address 0/1 (ADDR0_0, ADDR0_1, ADDR1_0, ADDR1_1)

Address Offset: ADDR0_0: 0x1B00021C
ADDR0_1: 0x1B000224
ADDR1_0: 0x1B000220
ADDR1_1: 0x1B000228

The ADDR*x*_0 and ADDR*x*_1 registers store the packaged version of the address that will be used by the next command sequence during access to the NAND flash device.

Bit	Bit Name	Description
ADDRx_0		
31:24	ADDRx_0_3	Fourth address byte; A31–A24 address bits
23:16	ADDRx_0_2	Third address byte; A23–A16 address bits
15:8	ADDRx_0_1	Second address byte; A15–A8 address bits
7:0	ADDRx_0_0	First address byte; A7–A0 address bits
ADDRx_1		
31:8	ADDRx_1_1	Reserved
7:0	ADDRx_1_0	Complete block address to 40 bits

No register defines the total memory size of the NAND flash memory chip, so the controller is not able to determine which address bits in the ADDR*x* registers are important and which have been set to zero. Therefore software must take care about the values written to the ADDR*x* registers. Incorrect values of unused address bits can cause errors in memory access.

A relationship between the ADDR*x* registers and the memory device address width is configured in the ADDR_CYCLE field of the Main Configuration (CONTROL) register. This field determines a number of address bytes that are used when addressing a NAND flash device. If the ADDR_CYCLE field is cleared (the four-address cycle mode is used), the last byte (fifth cycle) is omitted.

The address written to the address register must be aligned in the way that is required by the NAND flash device. Unused bits must be padded with zeros.

Table 10-34 Relationship of Address Register and Address Bytes

Address Cycle	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7
First Cycle	A0	A1	A2	A3	A4	A5	A6	A7
Second Cycle	A8	A9	A10	A11	A12	A13	A14	A15
Third Cycle	A16	A17	A18	A19	A20	A21	A22	A23
Fourth Cycle	A24	A25	A26	A27	A28	A29	A30	A31
Fifth Cycle	A32	A33	A34	A35	A36	A37	A38	A39

10.30.9 NAND Flash Spare Area Size (SPARE_SIZE)

Address Offset: 0x1B000230

This register stores the actual value of the NAND flash device spare area size. The size value is aligned to the NAND flash word size.

Bit	Bit Name	Description
31:9	RES	Reserved
8:0	SPARE_CNT	Spare area size value

10.30.10 Hardware Protect Against the Write/Erase Process Control (PROTECT)

Address Offset: 0x1B000238

The NAND flash controller allows defining the area that will be protected against any modifications. The protected area is a space that cannot be erased or overwritten. An attempt to erase/overwrite this space causes an error. Because write and erase process have constraints (only page can be written and only block can be erased), the protected area can be defined with block-size precision.

The lower [15:0] bits of this register define the beginning address of the protected area and are related to the NAND Flash memory block address bits of ADDR*x*_0/ADDR*x*_1 registers. The higher bits [31:16] of this register define the ending address of the protected area and are related to the NAND Flash memory block address bits of ADDR*x* registers. Independent of the memory type, the block address always has 16 bits. For 16-bit devices the column address width has one byte less, contrary to the 8-bit devices, so to keep constant block address width the most significant address bit is ignored for these devices.

Figure 10-1 shows the how these register fields are used to define the protected area.

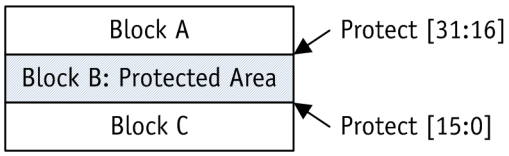


Figure 10-1 Write/Erase Protected Area Definition

Bit	Bit Name	Description
31:16	PROT_UP	Protected area upper limit
15:0	PROT_DOWN	Protected area lower limit

10.30.11 Enables Look-Up Register During NAND Flash Memory Address (LOOKUP_EN)

Address Offset: 0x1B000240

This register enables LOOKUP*x* registers during the remapping process. Each LOOKUP*x* register has an appropriate bit in this register. The asserted bit means that the contents of the associated LOOKUP*x* register is valid. Each LOOKUP*x* register has two fields the first one stores the address of the block that must be remapped, the second one stores the address of block that will replace the one from the first field. After the controllers LOOKUP initialization the bits corresponding to the initialized registers must be set in this register.

Bit	Bit Name	Description
31:8	RES	Reserved
7:0	LUT_EN	Enable bits. Every bit of this field corresponds to the LOOKUP register. If the bit is asserted, the given LOOKUP register is used during the remapping process.

10.30.12 Lookup Table [7:0] (LOOKUP[7:0])

Address Offset:
LOOKUP0: 0x1B000244
LOOKUP1: 0x1B000248
LOOKUP2: 0x1B00024C
LOOKUP3: 0x1B000250
LOOKUP4: 0x1B000254
LOOKUP5: 0x1B000258
LOOKUP6: 0x1B00025C
LOOKUP7: 0x1B000260

The LOOKUP*x* registers can be treated as rows in the bad blocks remapping table. The remapping table has two columns: the first column stores an address of the block that will be replaced; the second column stores an address of the block that will be replacing the block from the first column.

By default, the controller has eight LOOKUP registers. Each register can be separately enabled or disabled, or can also be completely removed to save chip area. The register amount can be easily extended to meet application requirements.

Bit	Bit Name	Description
31:16	DST_ADDR	Destination address. Contains an address of the block that replaces the bad one in the remapping process.
15:0	SRC_ADDR	Source address. The field contains an address of the block that will be replaced in the remapping process.

10.30.13 DMA Module Base Address (DMA_ADDR)

Address Offset: 0x1B000264

Contains the address of the first data in the data block written to the NAND flash device. The DMA module can read data from the memory location set by this register and write it to the FIFO module, or read data from the FIFO module and write it to the memory starting from the location indicated.

Bit	Bit Name	Description
31:24	DMA_ADDR3	Fourth DMA address byte; A31–A24 address bits
23:16	DMA_ADDR2	Third DMA address byte; A23–A16 address bits
15:8	DMA_ADDR1	Second DMA address byte; A15–A8 address bits
7:0	DMA_ADDR0	First DMA address byte; A7–A0 address bits

10.30.14 DMA Module Counters Initial Value (DMA_CNT)

Address Offset: 0x1B000268

This register defines the number of the bytes transferred by the DMA module. It remains unchanged during the transfer process.

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	CNT_INIT	Bytes counter initial value; The field contains data page length in bytes (0x0000–0xFFFD). The number of the bytes must be divided by 4.

10.30.15 DMA Module Control (DMA_CTRL)

Address Offset: 0x1B00026C

This control register for the DMA channel defines the parameters of the DMA transfer.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7	DMA_START	DMA start; set this bit to start DMA when the command sequence will be sent to NAND flash memory.	
6	DMA_DIR	Defines the DMA transfer (transmission) direction	
		0	Write data from AHB to the internal buffer (FIFO)
		1	Read from internal buffer (FIFO) and write to AHB
5	DMA_MODE	DMA work mode	
		0	Register-managed mode
		1	Scatter-gather mode
4:2	DMA_BURST	Burst type; These bits define the main transfer type used by the DMA to precede the requested transfer.	
		000	Incrementing precise burst of precisely four transfers
		001	Steam burst (address constant)
		010	Single transfer (address increment)
		011	Burst of unspecified length (address increment)
		100	Incrementing precise burst of precisely eight transfers
		101	Incrementing precise burst of precisely sixteen transfers
1	ERR_FLAG	DMA error flag; Set when a Tx error occurs during the DMA transfer. Set when the logical 1 value on the SERROR line was set.	
0	DMA_READY	DMA ready flag. The flag is set transfer is completed.	

10.30.16 Memory Device Control (MEM_CTRL)

Address Offset: 0x1B000280

This register stores the set of configuration parameters used to select the destination NAND flash device for the current transfer and state of the write protect bit for each device.

Bit	Bit Name	Description
31:16	RES	Reserved
15	MEM7_WP	WP line state of the eighth device in the selected bank
14	MEM6_WP	WP line state of the seventh device in the selected bank
13	MEM5_WP	WP line state of the sixth device in the selected bank
12	MEM4_WP	WP line state of the fifth device in the selected bank
11	MEM3_WP	WP line state of the fourth device in the selected bank
10	MEM2_WP	WP line state of the third device in the selected bank
9	MEM1_WP	WP line state of the second device in the selected bank
8	MEM0_WP	WP line state of the first device in the selected bank
7:3	RES	Reserved
2:0	MEM0_CE	The memory selection field. The number of selected memory is binary coded.

10.30.17 Custom Page Size Value (DATA_SIZE)

Address Offset: 0x1B000284

Stores the size of the data block. It is used only when the CUSTOM_SIZE_EN field of Main Configuration (CONTROL) chooses the custom size, otherwise the fixed value is used. The data size value is the number of bytes per transferred block, but its size must be declared as the multiple of the chosen NAND flash word size. Unused bits for the word size configuration are replaced with 0. When a non-custom data size is selected, the register value is overwritten by the value decoded from the PAGE_SIZE field of the CONTROL register.

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DATA_SIZE	Defines the data size

10.30.18 Read Status Command Output Value (READ_STATUS)

Address Offset: 0x1B000288

Stores the value of the Controller Status (STATUS) register that was a result of the latest READ STATUS command. A read of this register must be preceded by sending the READ STATUS command to the device requiring the status. This register is valid as soon as the destination device status is in the STATUS register back to ready state after command execution.

Bit	Bit Name	Description
31:16	RES	Reserved
15:8	STATE_MASK	Marks the ready/busy bits in the NAND flash device status byte. This field is used during internal read status operation.
7:0	STATUS	The READ STATUS command output value.

10.30.19 Command Sequence Timings Configuration (TIME_SEQ)

Address Offset: 0x1B00028C

The NAND flash controller is intended to be used with a wide range of host clock rates. To maximize flexibility, some timing parameters are configurable. This register defines some of the waveform configuration parameters.

Bit	Bit Name	Description
7:15	RES	Reserved
14:12	TWB	Busy time for interface change. The busy time when the interface changes from asynchronous to synchronous using the SET FEATURES command or synchronous to asynchronous using the RESET command.
11:9	TWHR	Command cycle to data output time for synchronous interface. NAND_WE_L high to NAND_RE_L low time for asynchronous interface.
8:6	TRHW	Data output to command, address, or data input time for synchronous interface. NAND_RE_L high to NAND_WE_L low time for asynchronous interface.
5:3	TADL	NAND_ALE to data loading time for synchronous interface. NAND_ALE to data start time for asynchronous interface.
2:0	TCCS	Change column setup.

10.30.20 Timing Configuration 0 (TIMING_ASYN)

Address Offset: 0x1B000290

The NAND flash controller is intended to be used with a wide range of host clock rates. To maximize flexibility, some timing parameters are configurable. Two waveform configuration parameters are defined in this register.

Bit	Bit Name	Description
31:8	RES	Reserved
7:4	TRHW	NAND_WE_L or NAND_RE_L high hold time.
3:0	TRWP	NAND_WE_L or NAND_RE_L pulse width.

10.30.21 Timing Configuration 1 (TIMING_SYN)

Address Offset: 0x1B000294

The NAND flash controller is intended to be used with a wide range of host clock rates. To maximize flexibility, some timing parameters are configurable. This register contains one waveform configuration parameter.

Bit	Bit Name	Description
31:4	RES	Reserved
3:0	TCAD	Command address delay

10.30.22 FIFO Module Interface (FIFO_DATA)

Address Offset: 0x1B000298

This register is used as an entry point to the FIFO module for the SIU module. The external CPU can access the FIFO module by reading or writing to this register in the same way as it accesses any other registers.

Bit	Bit Name	Description
31:0	FIFO_DATA	FIFO data. The FIFO module works on 32-bit words so when the FIFO DATA register is accessed from the narrower bus then: ■ For the read operation: The access to lowest byte triggers the word read from the FIFO module. If the requested data is narrower than the FIFO word size, then the read word is stored for further accesses. If the read request does not strobe the lowest byte, the previously stored data is used instead, triggering new access to the FIFO. ■ For the write operation situation is almost the same. Only the request that strobe the lowest byte trigger the write access to the FIFO module. Any other requests cause only writes to the temporary register used in further access to the FIFO module.

10.30.23 DQS Signal Delay Effect (TIME_MODE)

Address Offset: 0x1B00029C

This register contains the DQS delay which determine the delay of the strobe signal introduced during data read in synchronous mode.

Bit	Bit Name	Description
31:28	DQS_DELAY_7	The DQS delay value for memory device 7
27:24	DQS_DELAY_6	The DQS delay value for memory device 6
23:20	DQS_DELAY_5	The DQS delay value for memory device 5
19:16	DQS_DELAY_4	The DQS delay value for memory device 4
15:12	DQS_DELAY_3	The DQS delay value for memory device 3
11:8	DQS_DELAY_2	The DQS delay value for memory device 2
7:4	DQS_DELAY_1	The DQS delay value for memory device 1
3:0	DQS_DELAY_0	The DQS delay value for memory device 0

10.30.24 DMA Module Address Offset (DMA_ADDR_OFFSET)

Address Offset: 0x1B0002A0

This register contains the offset vector for the master interface address bus. The value on the master interface address bus is composed from the offset part and address part. It is a concatenation of the this register and the DMA Module Base Address (DMA_ADDR) registers.

Bit	Bit Name	Description
31:0	DMA_ADDR_OFFSET	DMA address offset bytes

10.30.25 Control for the FIFO Module (FIFO_INIT)

Address Offset: 0x1B0002B0

Bit	Bit Name	Description
31:1	RES	Reserved
0	FIFO_INIT	FIFO init bit. Setting of this bit causes the flushing of FIFO.

10.30.26 Configuration for the Two Generic Sequences (GENERIC_SEQ_CTRL)

Address Offset: 0x1B0002B4

This register stores the set of the configuration for the two generic sequences available to mimic the almost any command available in the NAND flash devices.

Bit	Bit Name	Description	
31:18	RES	Reserved	
17	COL_ADDR	Enable or disable the column part of the address	
16	DATA_EN	Enable or disable the presence of the data phase in the universal command sequence	
15:8	CMD3_CODE	Command 3 code value. This field holds the value of the command that will be send to the NAND flash device in the command 3 phase of the generic command sequence.	
7:6	DEL_EN	Enable the busy 1 phase. This bit allows enabling or disabling the presence of the busy 1 phase in the universal command sequence.	
		00	Disable both delays
		01	Enable delay 0
		10	Enable delay 1
		11	Disable both delays
5	CMD3_EN	Enable command 3 phase. This bit allows enabling or disabling the presence of the command 3 phase in the universal command sequence.	
4	CMD2_EN	Enable command 2 phase. This bit allows enabling or disabling the presence of the command 2 phase in the universal command sequence.	
3	ADDR1_EN	Enable address 1 phase. This bit allows enabling or disabling the presence of the address 1 phase in the universal command sequence.	
2	CMD1_EN	Enable command 1 phase. This bit allows enabling or disabling the presence of the command 1 phase in the universal command sequence.	
1	ADDR0_EN	Enable address 0 phase. This bit allows enabling or disabling the presence of the address 0 phase in the universal command sequence.	
0	CMD0_EN	Enable command 0 phase. This bit allows enabling or disabling the presence of the command 0 phase in the universal command sequence.	

10.31 PCIE EP DMA Registers

Table 10-35 summarizes the PCIE EP DMA registers for the QCA9558.

Table 10-35 PCIE EP Host DMA Registers Summary

Client Register Address	Host Register Address	Name	Description	Page
0x18127000	—	RX_DESC_START_ADDRESS	Rx Descriptor Start Address	page 551
0x18127004	—	CLIENT_DMA_INTERRUPT_MASK	Client DMA Interrupt Mask	page 552
0x18127800 (Chain 0) 0x18127900 (Chain 1) 0x18127A00 (Chain 2) 0x18127B00 (Chain 3)	0x00000800 (Chain 0) 0x00000900 (Chain 1)	RX_DESC_START_ADDRESS	Rx Descriptor Start Address	page 552
0x18127804 (Chain 0) 0x18127904 (Chain 1) 0x18127A04 (Chain 2) 0x18127B04 (Chain 3)	0x00000804 (Chain 0) 0x00000904 (Chain 1)	RX_DMA_START	Rx DMA Start	page 553
0x18127808 (Chain 0) 0x18127908 (Chain 1) 0x18127A08 (Chain 2) 0x18127B08 (Chain 3)	0x00000808 (Chain 0) 0x00000908 (Chain 1)	RX_BURST_SIZE	Rx AHB Burst Size	page 553
0x1812780C (Chain 0) 0x1812790C (Chain 1) 0x18127A0C (Chain 2) 0x18127B0C (Chain 3)	0x0000080C (Chain 0) 0x0000090C (Chain 1)	PKT_OFFSET	Packet Offset	page 554
0x18127810 (Chain 0) 0x18127910 (Chain 1) 0x18127A10 (Chain 2) 0x18127B10 (Chain 3)	0x00000810 (Chain 0) 0x00000910 (Chain 1)	CHECKSUM	Checksum	page 554
0x1812781C (Chain 0) 0x1812791C (Chain 1) 0x18127A1C (Chain 2) 0x18127B1C (Chain 3)	—	RX_DATA_SWAP	Data Swap	page 555
0x18127C00 (Chain 0) 0x18127D00 (Chain 1)	0x00000C00 (Chain 0) 0x00000D00 (Chain 1) 0x00000E00 (Chain 2) 0x00000F00 (Chain 3)	TX_DESC_START_ADDRESS	Rx Descriptor Start Address	page 555
0x18127C04 (Chain 0) 0x18127D04 (Chain 1)	0x00000C04 (Chain 0) 0x00000D04 (Chain 1) 0x00000E04 (Chain 2) 0x00000F04 (Chain 3)	TX_DMA_START	Tx DMA Start	page 555
0x18127C08 (Chain 0) 0x18127D08 (Chain 1)	0x00000C08 (Chain 0) 0x00000D08 (Chain 1) 0x00000E08 (Chain 2) 0x00000F08 (Chain 3)	INTERRUPT_LIMIT	Interrupt Limit	page 556
0x18127C0C (Chain 0) 0x18127D0C (Chain 1)	0x00000C0C (Chain 0) 0x00000D0C (Chain 1) 0x00000E0C (Chain 2) 0x00000F0C (Chain 3)	TX_BURST_SIZE	Tx AHB Burst Size	page 556
0x18127C18 (Chain 0) 0x18127D18 (Chain 1)	0x00000C18 (Chain 0) 0x00000D18 (Chain 1) 0x00000E18 (Chain 2) 0x00000F18 (Chain 3)	TX_DATA_SWAP	Tx Data Swap	page 557
—	0x00000000	HOST_DMA_INTERRUPT	Interrupt Status	page 557
—	0x00000004	HOST_DMA_INTERRUPT_MASK	Interrupt Mask	page 558
—	0x00000008	PRIORITY	Arbitration Priority	page 558

10.31.1 Client DMA Interrupt (CLIENT_DMA_INTERRUPT)

Address: 0x18127000
Access: Read/Write
Reset: 0x0

This register is the interrupt status register for current statuses of the DMA engines.

Bit	Bit Name	Description
31:26	RES	Reserved
25	TX_1_END	The DMA engine has reached the end of the descriptor chain on Tx chain 1
24	TX_0_END	The DMA engine has reached the end of the descriptor chain on Tx chain 2
23:18	RES	Reserved
17	TX_1_COMPLETE	A packet has been received on Tx chain 2
16	TX_0_COMPLETE	A packet has been received on Tx chain 1
15:12	RES	Reserved
11	RX_3_END	The DMA engine has reached the end of the descriptor chain on RX chain 4
10	RX_2_END	The DMA engine has reached the end of the descriptor chain on RX chain 3
9	RX_1_END	The DMA engine has reached the end of the descriptor chain on RX chain 2
8	RX_0_END	The DMA engine has reached the end of the descriptor chain on RX chain 1
7:4	RES	Reserved
3	RX_3_COMPLETE	A packet has been received on Rx chain 4
2‘	RX_2_COMPLETE	A packet has been received on Rx chain 3
1	RX_1_COMPLETE	A packet has been received on Rx chain 2
0	RX_0_COMPLETE	A packet has been received on Tx chain 1

10.31.2 Client DMA Interrupt Mask (CLIENT_DMA_INTERRUPT_MASK)

Address: 0x18127004
Access: Read/Write
Reset: 0x0

This register is the interrupt status register for current statuses of the DMA engines.

Bit	Bit Name	Description
31:26	RES	Reserved
25	TX_1_END_MASK	If set to 1, enables TX_0_END interrupt
24	TX_0_END_MASK	If set to 1, enables TX_1_END interrupt
23:18	RES	Reserved
17	TX_1_COMPLETE_MASK	If set to 1, enables TX_0_COMPLETE interrupt
16	TX_0_COMPLETE_MASK	If set to 1, enables TX_1_COMPLETE interrupt
15:12	RES	Reserved
11	RX_3_END_MASK	If set to 1, enables RX_3_END interrupt
10	RX_2_END_MASK	If set to 1, enables RX_2_END interrupt
9	RX_1_END_MASK	If set to 1, enables RX_1_END interrupt
8	RX_0_END_MASK	If set to 1, enables RX_0_END interrupt
7:4	RES	Reserved
3	RX_3_COMPLETE_MASK	If set to 1, enables RX_3_COMPLETE interrupt
2	RX_2_COMPLETE_MASK	If set to 1, enables RX_2_COMPLETE interrupt
1	RX_1_COMPLETE_MASK	If set to 1, enables RX_1_COMPLETE interrupt
0	RX_0_COMPLETE_MASK	If set to 1, enables RX_0_COMPLETE interrupt

10.31.3 Rx Descriptor Start Address (RX_DESC_START_ADDRESS)

Client Address: 0x18127800 (Chain 0)
0x18127900 (Chain 1)
0x18127A00 (Chain 2)
0x18127B00 (Chain 3)
Host Address: 0x00000800 (Chain 0)
0x00000900 (Chain 1)
Access: Read/Write
Reset: 0s0

This register contains the address at the start of the descriptor chain. It needs to be set only once after reset.

Bit	Bit Name	Description
31:0	ADDRESS	The start address of the descriptor

10.31.4 Rx DMA Start (RX_DMA_START)

Client register address: 0x18127804 (Chain 0)
0x18127904 (Chain 1)
0x18127A04 (Chain 2)
0x18127B04 (Chain 3)
Host register address: 0x00000804 (Chain 0)
0x00000904 (Chain 1)
Access: Read/Write
Reset: 0x0

This register is used to start or resume reading the descriptor chain.

Bit	Bit Name	Description
31:5	RES	Reserved. Must be written with zero. Contains zeros when read.
4	RESTART	Write a 1 to this bit when a chain is stopped will force a reload of the Client DMA Interrupt (CLIENT_DMA_INTERRUPT) register.
3:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	START	Writing a 1 to this bit will start the DMA chain if it stopped. This bit will be cleared once the DMA engine has stopped and restarted.

10.31.5 Rx AHB Burst Size (RX_BURST_SIZE)

Client register address: 0x18127808 (Chain 0)
0x18127908 (Chain 1)
0x18127A08 (Chain 2)
0x18127B08 (Chain 3)
Host register address: 0x00000808 (Chain 0)
0x00000908 (Chain 1)
Access: Read/Write
Reset: 0x0

This register sets the standard DMA burst size used on the AHB bus.

Bit	Bit Name	Description	
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.	
1:0	BURST	Defines the burst size	
		00	4 words, 16 bytes
		01	8 words, 32 bytes
		10	16 words, 64 bytes

10.31.6 Packet Offset (PKT_OFFSET)

Client register address: 0x1812780C (Chain 0)
0x1812790C (Chain 1)
0x18127A0C (Chain 2)
0x18127B0C (Chain 3)
Host register address: 0x0000080C (Chain 0)
0x0000090C (Chain 1)
Access: Read/Write
Reset: 0x0

This register informs the DMA engine to place the packet a programmable number of bytes after the start of the buffer. This allows software to add an additional header in front of the packet without doing a copy.

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	OFFSET	The offset in bytes. The size of the buffer attached to the first descriptor of the packet must be larger than the offset value.

10.31.7 Checksum (CHECKSUM)

Client register address: 0x18127810 (Chain 0)
0x18127910 (Chain 1)
0x18127A10 (Chain 2)
0x18127B10 (Chain 3)
Host register address: 0x00000810 (Chain 0)
0x00000910 (Chain 1)
Access: See field description
Reset: 0x0

This register informs the DMA whether or not to insert a TCP or UDP checksum during a receive operation.

Bit	Bit Name	Type	Description
31:2	RES	RO	Reserved. Must be written with zero. Contains zeros when read.
1	UDP	RW	Insert a UDP checksum for packets received
0	TCP	WO	Insert a TCP checksum for packets received

10.31.8 Rx Data Swap (RX_DATA_SWAP)

Client register address: 0x1812781C (Chain 0)
0x1812791C (Chain 1)
0x18127A1C (Chain 2)
0x18127B1C (Chain 3)
Access: Read/Write
Reset: 0x0

This register controls whether the data is swapped before being sent on. Descriptors are never swapped.

Bit	Bit Name	Description
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	SWAPD	Swap descriptor data
0	SWAP	Swap data

10.31.9 Tx Descriptor Start Address (TX_DESC_START_ADDRESS)

Client register address: 0x18127C00 (Chain 0)
0x18127D00 (Chain 1)
Host register address: 0x00000C00 (Chain 0)
0x00000D00 (Chain 1)
0x00000E00 (Chain 2)
0x00000F00 (Chain 3)
Access: Read/Write
Reset: 0x0

This register contains the address at the start of the descriptor chain. It needs to be set only once after reset.

Bit	Bit Name	Description
31:0	ADDRESS	The start address of the descriptor

10.31.10 Tx DMA Start (TX_DMA_START)

Client register address: 0x18127C04 (Chain 0)
0x18127D04 (Chain 1)
Host register address: 0x00000C04 (Chain 0)
0x00000D04 (Chain 1)
0x00000E04 (Chain 2)
0x00000F04 (Chain 3)
Access: Read/Write
Reset: 0x0

This register is used to start or resume reading the descriptor chain.

Bit	Bit Name	Description
31:5	RES	Reserved. Must be written with zero. Contains zeros when read.
4	RESTART	Write a 1 to this bit when a chain is stopped will force a reload of the Tx Descriptor Start Address (TX_DESC_START_ADDRESS) register.
3:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	START	Writing a 1 to this bit will start the DMA chain if it stopped. This bit will be cleared once the DMA engine has stopped and restarted.

10.31.11 Interrupt Limit (INTERRUPT_LIMIT)

Client register address: 0x18127C08 (Chain 0)
0x18127D08 (Chain 1)
Host register address: 0x00000C08 (Chain 0)
0x00000D08 (Chain 1)
0x00000E08 (Chain 2)
0x00000F08 (Chain 3)
Access: Read/Write
Reset: See field description

This register contains limits that set how often the COMPLETE interrupt is asserted.

Bit	Bit Name	Reset	Description
31:16	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:4	TIMEOUT	0x0	This value sets the maximum time the DMA engine will wait before asserting an interrupt after a packet has been received. The value is set in units of 32 clock cycles.
3:0	COUNT	0x1	In the absence of a timeout, an interrupt will be asserted after the number of packets stated here have passed since the last time the interrupt register was read.

10.31.12 Tx AHB Burst Size (TX_BURST_SIZE)

Client register address: 0x18127C0C (Chain 0)
0x18127D0C (Chain 1)
Host register address: 0x00000C0C (Chain 0)
0x00000D0C (Chain 1)
0x00000E0C (Chain 2)
0x00000F0C (Chain 3)
Access: Read/Write
Reset: 0x0

This register sets the standard DMA burst size used on the AHB bus.

Bit	Bit Name	Description	
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.	
1:0	BURST	Defines the burst size	
		00	4 words, 16 bytes
		01	8 words, 32 bytes
		10	16 words, 64 bytes

10.31.13 Tx Data Swap (TX_DATA_SWAP)

Client register address: 0x18127C18 (Chain 0)
0x18127D18 (Chain 1)
Host register address: 0x00000C18 (Chain 0)
0x00000D18 (Chain 1)
0x00000E18 (Chain 2)
0x00000F18 (Chain 3)
Access: Read/Write
Reset: 0x0

This register controls whether the data is swapped before being sent on. Descriptors are never swapped.

Bit	Bit Name	Description
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	SWAPD	Swap descriptor data
0	SWAP	Swap data

10.31.14 Interrupt Status (HOST_DMA_INTERRUPT)

Address: 0x00000000
Access: Read-Only
Reset: 0x0

This register denotes the current status of the DMA engines.

Bit	Bit Name	Description
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.
27	TX_3_END	The DMA engine has reached the end of the descriptor chain on Tx chain 3
26	TX_2_END	The DMA engine has reached the end of the descriptor chain on Tx chain 2
25	TX_1_END	The DMA engine has reached the end of the descriptor chain on Tx chain 1
24	TX_0_END	The DMA engine has reached the end of the descriptor chain on Tx chain 0
23:20	RES	Reserved. Must be written with zero. Contains zeros when read.
19	TX_3_COMPLETE	A packet has been received on Tx chain 3
18	TX_2_COMPLETE	A packet has been received on Tx chain 2
17	TX_1_COMPLETE	A packet has been received on Tx chain 1
16	TX_0_COMPLETE	A packet has been received on Tx chain 0
15:10	RES	Reserved. Must be written with zero. Contains zeros when read.
9	RX_1_END	The DMA engine has reached the end of the descriptor chain on RX chain 1
8	RX_1_END	The DMA engine has reached the end of the descriptor chain on RX chain 0
7:2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	RX_1_COMPLETE	A packet has been received on Rx chain 1
0	RX_0_COMPLETE	A packet has been received on Rx chain 0

10.31.15 Interrupt Mask (HOST_DMA_INTERRUPT_MASK)

Address: 0x00000004
Access: Read/Write
Reset: 0x0

This register selectively enables or disables propagation of interrupts in the INTERRUPT register.

Bit	Bit Name	Description
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.
27	TX_3_END_MASK	Enables TX_3_END interrupt if 1
26	TX_2_END_MASK	Enables TX_2_END interrupt if 1
25	TX_1_END_MASK	Enables TX_1_END interrupt if 1
24	TX_0_END_MASK	Enables TX_0_END interrupt if 1
23:20	RES	Reserved. Must be written with zero. Contains zeros when read.
19	TX_3_COMPLETE_MASK	Enables TX_3_COMPLETE interrupt if 1
18	TX_2_COMPLETE_MASK	Enables TX_2_COMPLETE interrupt if 1
17	TX_1_COMPLETE_MASK	Enables TX_1_COMPLETE interrupt if 1
16	TX_0_COMPLETE_MASK	Enables TX_0_COMPLETE interrupt if 1
15:10	RES	Reserved. Must be written with zero. Contains zeros when read.
9	RX_1_END_MASK	Enables RX_1_END interrupt if 1
8	RX_0_END_MASK	Enables RX_0_END interrupt if 1
7:2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	RX_1_COMPLETE_MASK	Enables RX_1_COMPLETE interrupt if 1
0	RX_0_COMPLETE_MASK	Enables RX_0_COMPLETE interrupt if 1

10.31.16 Arbitration Priority (PRIORITY)

Address: 0x00000008
Access: Read/Write
Reset: 0x0

This register sets the priority level of each DMA chain.

Bit	Bit Name	Description
31:22	RES	Reserved. Must be written with zero. Contains zeros when read.
21:20	RX_1_PRIORITY	Priority level of Rx chain 1
19:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:16	RX_0_PRIORITY	Priority level of Rx chain 0
15:14	RES	Reserved. Must be written with zero. Contains zeros when read.
13:12	TX_3_PRIORITY	Priority level of Tx chain 3
11:10	RES	Reserved. Must be written with zero. Contains zeros when read.
9:8	TX_2_PRIORITY	Priority level of Tx chain 2
7:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5:4	TX_1_PRIORITY	Priority level of Tx chain 1
3:2	RES	Reserved. Must be written with zero. Contains zeros when read.
1:0	TX_0_PRIORITY	Priority level of Tx chain 0

10.32 Serial Flash SPI Controller Registers

Table 10-36 summarizes the serial flash SPI controller registers for the QCA9558.

Table 10-36 Serial Flash SPI Controller Registers Summary

Address	Name	Description	Page
0x1F000000	FUNCTION_SELECT_ADDR	SPI Controller GPIO Mode Select	page 559
0x1F000004	SPI_CONTROL_ADDR	SPI Address Control	page 559
0x1F000008	SPI_IO_CONTROL_ADDR	SPI I/O Address Control	page 560
0x1F00000C	SPI_READ_DATA_ADDR	SPI Read Data Address	page 560
0x1F000010	SPI_SHIFT_DATAOUT_ADDR	SPI Data to Shift Out	page 560
0x1F000014	SPI_SHIFT_CNT_ADDR	SPI Content to Shift Out or In	page 561
0x1F000018	SPI_SHIFT_DATAIN_ADDR	SPI Data to Shift In	page 561

10.32.1 SPI Controller GPIO Mode Select (FUNCTION_SELECT_ ADDR)

Address: 0x1F000000
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	FUNCTION_SELECT	Writing a non-zero value to this register selects the GPIO mode for the SPI controller.

10.32.2 SPI Address Control (SPI_CONTROL_ADDR)

Address: 0x1F000004
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:14	RES	Reserved
13:8	TSHSL_CNT	Minimum time for which CS has must be deasserted between two SPI transactions.
7	SPI_RELOCATE	When this bit is set, 16 MB of SPI space is mapped to 0x1E00_0000, else it is mapped to 0x1F00_0000.
6	REMAP_DISABLE	Disables the alias of the lower 4 MB of SPI space, enabling the ROM to boot from 0x1FC00000 to alias to 0x1F000000 until software disables the aliasing.
5:0	CLOCK_DIVIDER	The clock divider is based on the AHB clock. The generated clock is AHBclock/((CLOCK_DIVIDER+1) * 2).

10.32.3 SPI I/O Address Control (SPI_IO_CONTROL_ADDR)

Address: 0x1F000008
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:19	RES	Reserved	
18	IO_CS2	Chip select 2. Active low signal.	
		0	Enable chip select 2
		1	Disable chip select 2
17	IO_CS1	Chip select 1. Active low signal.	
16	IO_CS0	Chip select 0. Active low signal.	
15:9	RES	Reserved	
8	IO_CLK	SPI clock	
7:1	RES	Reserved	
0	IO_DO	Data out	

10.32.4 SPI Read Data Address (SPI_READ_DATA_ADDR)

Address: 0x1F00000C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	READ_DATA	The SPI read data is shifted in and sampled every cycle

10.32.5 SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR)

Address: 0x1F000010
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	SHIFT_DATAOUT	The data (either CMD, ADDR, or DATA) to be shifted out every clock cycle

10.32.6 SPI Content to Shift Out or In (SPI_SHIFT_CNT_ADDR)

Address: 0x1F000014
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31	SHIFT_EN	Enables shifting data out
30	SHIFT_CHNL	If set to 1, enables chip select 2
29		If set to 1, enables chip select 1
28		If set to 1, enables chip select 0
27	SHIFT_CLKOUT	Initial value of the clock signal
26	TERMINATE	When set to 1, deasserts the chip select
25:7	RES	Reserved
6:0	SHIFT_COUNT	The number of bits to be shifted out or shifted in on the data line

10.32.7 SPI Data to Shift In (SPI_SHIFT_DATAIN_ADDR)

Address: 0x1F000018
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	SHIFT_DATAIN	SPI read data

10.33 PLL SRIF Registers

Table 10-37 summarizes the PLL SRIF registers.

Table 10-37 PLL SRIF Registers

Offset					Name	Page
Baseband	CPU	AUD	DDR	PCIE		
0x18116180	0x181161C0	0x18116200	0x18116240	0x18116C00	DPLL	page 562
0x18116184	0x181161C4	0x18116204	0x18116244	0x18116C04	DPLL2	page 563
0x18116188	0x181161C8	0x18116208	0x18116248	0x18116C08	DPLL3	page 563

10.33.1 DPLL

Address Offset:
Baseband: 0x18116180
CPU: 0x181161C0
AUD: 0x18116200
DDR: 0x18116240
PCIE: 0x18116C00
Access: Read/Write

Bit	Bit Name	Description
31:27	REFDIV	Manual override PLL reference divider ratio
26:18	NINT	Manual override PLL feedback divide ratio
17:0	NFRAC	Manual override of PLL fractional value of PLL divide ratio

10.33.2 DPLL2

Address Offset:
Baseband: 0x18116184
CPU: 0x181161C4
AUD: 0x18116204
DDR: 0x18116244
PCIE: 0x18116C04
Access: Read/Write

Bit	Bit Name	Description	
31	RANGE	Manual override for bias current control bits inside the DPLL to cover the required frequency range.	
		0	Set it to range = 0 for VCO frequency above 650 MHz
		1	Set range = 1 for VCO frequency < 650 MHz
30	LOCAL_PLL	Selects if we want to manually set PLL control bits through the SRIF space	
29:26	KI	Integral path gain of loop filter in DPLL, please set to 0x4	
25:19	KD	Proportional gain of loop filter in DPLL, this sets the loop bandwidth of the PLL	
18:17	RES	Reserved; must be set to 0x0	
16	PLL_PWD	Manual override for PLL power down; set to 1 to power down the PLL; a falling edge on this signal is needed to latch in the PLL values and initialize the PLL	
15:13	OUTDIV	Manual override to divide output of VCO in DPLL by $2^{OUT\_DIV[2:0]}$	
12:7	RES	Reserved; must be set to 0x1E	
6	RES	Reserved; must be set to 0x0	
5:0	RES	Reserved	

10.33.3 DPLL3

Address Offset:
Baseband: 0x18116188
CPU: 0x181161C8
AUD: 0x18116208
DDR: 0x18116248
PCIE: 0x18116C08
Access: Read/Write

Bit	Bit Name	Description
31:30	RES	Reserved; must be set to 0x0
29:23	PHASE_SHIFT	Programmable phase shift for DPLL, set it to 0x6
22:0	RES	Reserved; must be set to 0x0

11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Table 11-1 summarizes the absolute maximum ratings and Table 11-2 lists the recommended operating conditions for the QCA9558. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document is not recommended.

Table 11-1 Absolute Maximum Ratings

Symbol	Parameter	Max Rating	Unit
V_{DD33}	Supply Voltage	-0.3 to 3.6	V
V_{DD33}	GPIO18, GPIO19, GPIO20 Voltages	-0.3 to 3.6	V
V_{DD25}	Maximum I/O Supply Voltage	-0.3 to 3.0	V
V_{DD25}	All Other GPIOs Voltages (Except GPIO18, GPIO19, GPIO20)	-0.3 to 3.0	V
V_{DD12}	Core Voltage	-0.3 to 1.8	V
T_{store}	Storage Temperature	-65 to 150	°C
T_j	Junction Temperature	125	°C
ESD	Electrostatic Discharge Tolerance	2000	V

11.2 Recommended Operating Conditions

Table 11-2 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	Supply Voltage	±5%	3.13	3.3	3.46	V
V_{DD25}	I/O Supply Voltage[1]	±5%	2.49	2.62	2.75	V
V_{DD12}	Core Voltage	±5%	1.17	1.23	1.29	V
AV_{DD12}	Analog Voltage	±5%	1.17	1.23	1.29	V
VDD_{SGMII}	Voltage for SGMII[1]	—	1.14	1.2	1.26	V
V_{DD_DDR}	DDR1 I/O Voltage[1]	±5%	2.47	2.6	2.73	V
	DDR2 I/O Voltage[1]	±5%	1.71	1.8	1.89	V
D_{DR_VREF}	DDR1 Reference Level for SSTL Signals[2]	—	1.24	1.3	1.37	V
	DDR2 Reference Level for SSTL Signals[2]	—	0.86	0.9	0.95	V
T_{case}	Case Temperature (Standard Temperature Range)	—	0	—	110	°C
Psi_{JT}	Junction-to-top-center of the Package Thermal Parameter[3]	—	—	—	2.5	°C/W

1. Voltage regulated internally by the QCA9558.
2. Divide VDD_DDR voltage by two externally, see reference design schematic.
3. The thermal parameter is for the 18x18 mm BGA package.

11.3 General DC Electrical Characteristics

Table 11-3 lists GPIO, NAND Flash, SYS_RST_OUT_L and PCIE_RST_OUT_L DC electrical characteristics. SYS_RST_OUT_L, GPIO18, GPIO19, GPIO20, and PCIE_RST_OUT_L are open drain.

These conditions apply to all DC characteristics unless otherwise specified:
T_{amb} = 25 °C, V_{DD25} = 2.62 V

Table 11-3 GPIO, NAND Flash, SYS_RST_OUT_L, and PCIE_RST_OUT_L DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	1.8	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	0.4	V
V_{OH}	High Level Output Voltage	—	2.2	—	—	V
V_{OL}	Low Level Output Voltage	—	—	—	0.3	V
I_{IL}	Low Level Input Current	—	—	—	15	µA
I_{OH}	High Level Output Current	—	—	—	8	mA
V_{IH}	High Level Input Voltage (GPIO18, GPIO19, GPIO20)	—	2.2	—	—	V
V_{IL}	Low Level Input Voltage (GPIO18, GPIO19, GPIO20)	—	—	—	0.4	V
V_{OH}	High Level Output Voltage (GPIO18, GPIO19, GPIO20)	—	2.4	—	—	V
V_{OL}	Low Level Output Voltage (GPIO18, GPIO19, GPIO20)	—	—	—	0.3	V
I_{IL}	Low Level Input Current (GPIO18, GPIO19, GPIO20)	—	—	—	7	µA
C_{IN}	Input Capacitance	—	—	3	—	pF

Table 11-4 lists the DDR1 DC electrical characteristics:
T_{amb} = 25 °C, V_{DD_DDR} = 2.6 V

Table 11-4 DDR1 Interface DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	1.8	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	0.4	V
V_{OH}	High Level Output Voltage	—	2.2	—	—	V
V_{OL}	Low Level Output Voltage	—	—	—	0.3	V
I_{IL}	Low Level Input Current	—	—	—	5	µA

Table 11-5 lists the DDR2 DC electrical characteristics:
T_{amb} = 25 °C, V_{DD_DDR} = 1.8 V

Table 11-5 DDR2 Interface DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	1.2	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	0.4	V
V_{OH}	High Level Output Voltage	—	1.6	—	—	V
V_{OL}	Low Level Output Voltage	—	—	—	0.3	V
I_{IL}	Low Level Input Current	—	—	—	3	µA

Table 11-6 lists the SERDES and SGMII DC electrical characteristics:

T_{amb} = 25 °C, V_{DD_SGMII} = 1.2 V

Table 11-6 Driver DC Characteristics LVDS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage[1]	—	—	1050	1195[3]	mV
V_{OL}	Low Level Output Voltage[1]	—	200[2]	750	—	mV
V_{RING}	Output Ringing	—	—	—	10	%
V_{OD}	Output Differential Voltage (Programmable note1)	—		300		mV
V_{OS}	Output Offset Voltage[1]	—	500[2]	900	1070[3]	mV
Ro	Output Impedance (single ended) 50 Termination	—	40	50	60	Ω
	Output Impedance (single ended) 75 Termination	—	60	75	90	Ω
Delta Ro	Mismatch in a Pair	—	—	—	10	%
Delta V_{OD}	Change in V_{OD} Between “0” and “1”	—	—	—	25	mV
Delta V_{OS}	Change in V_{OS} Between “0” and “1”	—	—	—	25	mV
Isa, Isb	Output Current on Short to GND	—	—	—	40	mA
Isab	Output Current when a, b, are Shorted	—	—	—	12	mA
I_{xa}, I_{xb}	Power off Leakage Current	—	—	—	10	mA

1. With 50 Ω termination
2. When output swing set to maximum
3. When output swing set to minimum

Table 11-7 lists the Receiver DC electrical characteristics:

T_{amb} = 25 °C, V_{DD_SGMII} = 1.2V

Table 11-7 Driver DC Characteristics LVDS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	Internal Offset Voltage	—	800	900	1000	mV
V_{IH}	Input Single Voltage High	—	—	—	1480	mV
V_{IL}	Input Single Voltage Low	—	520	—	—	mV
V_{IDTH}	Input Differential Threshold	—	-50	—	50	mV
V_{HYST}	Input Differential Hysteresis	—	25	—	—	mV
R_{IN}	Receiver Differential Input Impedance 50 Ω Termination	—	80	100	120	Ω
	Receiver Differenial Input Impedance 75 Ω Termination	—	120	150	180	Ω

Table 11-8 lists the RGMII DC electrical characteristics:

T_{amb} = 25 °C, V_{DD} = 2.62 V

Table 11-8 RGMII Interface DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	1.8	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	0.4	V
V_{OH}	High Level Output Voltage	—	2.2	—	—	V
V_{OL}	Low Level Output Voltage	—	—	—	0.3	V
I_{IH}	High Level Input Current	—	—	—	15	µA
I_{OH}	High Level Output Current	—	—	—	8	mA
V_{IH}	High Level Input Voltage (EMDC, EMDIO)[1]	—	2.2	—	—	V
V_{IL}	Low Level Input Voltage (EMDC, EMDIO)	—	—	—	0.4	V
V_{OH}	High Level Output Voltage (EMDC, EMDIO)	—	2.4	—	—	V
V_{OL}	Low Level Output Voltage (EMDC, EMDIO)	—	—	—	0.3	V
I_{IL}	Low Level Input Current (EMDC, EMDIO)	—	—	—	7	µA

1. EMDIO is open drain.

Table 11-9 lists the PCIE reset outputs DC electrical characteristics.

PCIE0_RST_OUT_L and PCIE1_RST_L are open drain.
T_{amb} = 25 °C, V_{DD} = 2.62 V

Table 11-9 PCIE0_RST_OUT_L and PCIE1_RST_L DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	1.8	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	0.4	V
V_{OH}	High Level Output Voltage	—	2.2	—	—	V
V_{OL}	Low Level Output Voltage	—	—	—	0.3	V
I_{IL}	Low Level Input Current	—	—	—	7	µA

11.4 40 MHz Clock Characteristics

When using an external clock (TCXO), the XTALI pin is grounded and the XTALO pin should be driven with a square wave clock.

AC coupling is recommended for the clock signal to the XTALO pin.

The internal circuit provides the DC bias of approximately 0.6 V. The peak to peak swing of the external clock can be between 0.3 V to 1.2 V. In general, larger swings and sharper edges will reduce jitter, but introduce the potential of high frequency spurious tones.

The phase noise of the oscillator should be lower than -145 dBc/Hz at 100 KHz carrier offset.

Table 11-10 Clock Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INMAX}	Input Voltage Maximum	—	—	—	1.4	V
V_{INMIN}	Input Voltage Minimum[1]	—	-0.2	—	—	V
T_{DCycle}	Duty Cycle	—	40	50	60	%
T_{Rise}	Clock Rise Time	—	—	—	2[2]	ns
T_{Fall}	Clock Fall Time	—	—	—	2[2]	ns

1. V_{INMAX} of -0.2 V is limited by the ESD protection diode. If V_{INMAX} is less than -0.2 V, the ESD diode turns on and protects the chip.
2. The 2 ns rise/fall time specification is for TCXO input only, does not apply when using a XTAL.

11.5 Internal Voltage Regulators

Figure 11-1 depicts the voltages regulated by the QCA9558. Refer to the reference design schematics for details.

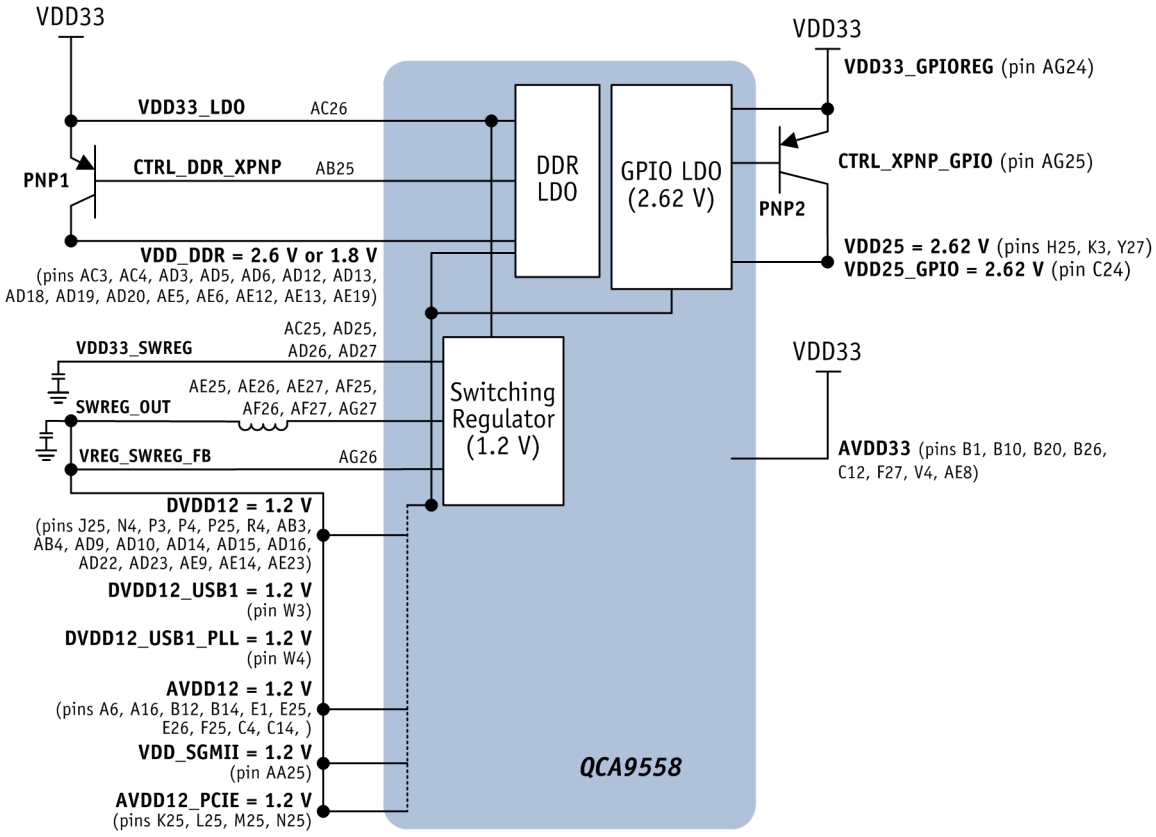


Figure 11-1 Output Voltages Regulated by the QCA9558

11.6 Radio Characteristics

The following conditions apply to the typical characteristics unless otherwise specified:

V_{DD12} = 1.2V
V_{DD33} = 3.3V, T_{amb} = 25 °C

11.6.1 Receiver Characteristics

See these tables for the QCA9558 receiver characteristics:

Table	Receive Characteristics for:
Table 11-11	2.4 GHz Operation
Table 11-12	5 GHz Operation

Table 11-11 Receiver Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range	5 MHz center frequency	2.412	—	2.472	GHz
NF	Receive chain noise figure (max gain)	See Note 1	—	6	—	dB
S_{rf}	Sensitivity					
	CCK, 1 Mbps	See Note 2	–80	–100	—	dBm
	CCK, 11 Mbps		–76	–93	—	
	OFDM, 6 Mbps		–82	–92	—	
	OFDM, 54 Mbps		–64	–82	—	
	HT20, MCS0, 1 stream, 3 Tx, 3 Rx	See Note 2	–82	–94	—	
	HT20, MCS7, 1 stream, 3 Tx, 3 Rx		–64	–79	—	
	HT20, MCS8, 2 stream, 3 Tx, 3 Rx		–82	–94	—	
	HT20, MCS15, 3 stream, 3 Tx, 3 Rx		–64	–76	—	
	HT20, MCS16, 3 stream, 3 Tx, 3 Rx		–82	–94	—	
	HT20, MCS23, 2 stream, 3 Tx, 3 Rx		–64	–73	—	
	HT40, MCS0, 1 stream, 3 Tx, 3 Rx	See Note 2	–79	–92	—	
	HT40, MCS7, 1 stream, 3 Tx, 3 Rx		–61	–76	—	
	HT40, MCS8, 2 stream, 3 Tx, 3 Rx		–79	–92	—	
	HT40, MCS15, 2 stream, 3 Tx, 3 Rx		–61	–74	—	
	HT40, MCS16, 3 stream, 3 Tx, 3 Rx		–79	–91	—	
	HT40, MCS23, 3 stream, 3 Tx, 3 Rx		–61	–71	—	
IIP1	Input 1 dB compression (min. gain)	—	—	-2	—	dBm
IIP3	Input third intercept point (min. gain)	—	—	7	—	dBm
Z_{RFin_input}	Recommended LNA differential drive impedance	Ch 0, Ch 1, Ch 2	—	50	—	Ω
ER_{phase}	I,Q phase error	See Note 3	—	0.11	—	°

Table 11-11 Receiver Characteristics for 2.4 GHz Operation (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ERamp	I,Q amplitude error	—	—	0.554	—	%
R_{adj}	Adjacent channel rejection					
	CCK	See Note 4	—	35	—	dB
	OFDM, 6 Mbps		16	31	—	
	OFDM, 54 Mbps		–1	10	—	
	HT20, MCS0		16	33	—	
	HT20, MCS15		–2	16	—	
	HT40, MCS0		16	16	—	
	HT40, MCS15		–2	6	—	
TRpowup	Time for power up (from synthesizer on)	—	—	1.5	—	µs

1. For improved sensitivity performance, an external LNA may be used.
2. Sensitivity performance based on Qualcomm Atheros reference design, which includes Tx/Rx antenna switch and xLNA. Minimum values based on the IEEE 802.11 specifications.
3. These are residual values after applying IQ calibration at chip level
4. Typical values measured with reference design; minimum values are based on IEEE 802.11 specifications.

Table 11-12 Receiver Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range	5 MHz center frequency	5.18	—	5.825	GHz
NF	Receive chain noise figure (max gain)	See Note 1	—	6	—	dB
S_{rf}	Sensitivity					
	6 Mbps	See Note 2	–82	–95	—	dBm
	54 Mbps		–65	–78	—	
	HT20, MCS0, 1 stream, 3 Tx, 3 Rx	See Note 2	–82	–95	—	dBm
	HT20, MCS7, 1 stream, 3 Tx, 3 Rx		–64	–75	—	
	HT20, MCS8, 2 stream, 3 Tx, 3 Rx		–82	–93	—	
	HT20, MCS15, 3 stream, 3 Tx, 3 Rx		–64	–73	—	
	HT20, MCS16, 3 stream, 3 Tx, 3 Rx		–82	-91		
	HT20, MCS23, 2 stream, 3 Tx, 3 Rx		–64	-70		
	HT40, MCS0, 1 stream, 3 Tx, 3 Rx	See Note 2	–79	–92	—	dBm
	HT40, MCS7, 1 stream, 3 Tx, 3 Rx		–61	–71	—	
	HT40, MCS8, 2 stream, 3 Tx, 3 Rx		–79	–89	—	
	HT40, MCS15, 2 stream, 3 Tx, 3 Rx		–61	–69	—	
	HT40, MCS16, 3 stream, 3 Tx, 3 Rx		-79	-87		
	HT40, MCS23, 3 stream, 3 Tx, 3 Rx		-61	-67		
IP1dB	Input 1 dB compression (min. gain)	—	—	3	—	dBm
IIP3	Input third intercept point (min. gain)	—	—	10	—	dBm
Z_{RFin_input}	Recommended LNA single-ended drive impedance	Ch 0, Ch 1, Ch 2	—	50	—	Ω
ER_{phase}	I,Q phase error	See Note 3	—	$\pm$ 0.11	—	°

Table 11-12 Receiver Characteristics for 5 GHz Operation (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ERamp	I,Q amplitude error	—	—	0.8	—	%
R_{adj}	Adjacent channel rejection					
	11a OFDM, 6 Mbps	See Note 4	16	22	—	dB
	11a OFDM, 54 Mbps		–1	8	—	
	HT20, MCS0	See Note 4	16	22	—	dB
	HT20, MCS15		–2	0	—	
	HT40, MCS0	See Note 4	16	22	—	dB
	HT40, MCS15		–2	0	—	
R_{alt}	Alternate channel rejection					
	11a OFDM 6 Mbps	See Note 4	32	36	—	dB
	11a OFDM 54 Mbps		15	21	—	
	HT20, MCS0	See Note 4	32	38	—	dB
	HT20, MCS15		14	18	—	
	HT40, MCS0	See Note 4	32	35	—	dB
	HT40, MCS15		14	17	—	
TRpowup	Time for power up (from synthesizer on)	—	—	1.5	—	µs

1. For improved sensitivity performance, an external LNA may be used.
2. Sensitivity performance based on Qualcomm Atheros reference design, which includes Tx/Rx antenna switch, and XLNA. Minimum values based on IEEE 802.11 specifications.
3. These are residual values after applying IQ calibration at chip level
4. Typical values measured with reference design. Minimum values based on IEEE 802.11 specifications.

11.6.2 Transmitter Characteristics

See these tables for the QCA9558 transmitter characteristics:

Table	Transmit Characteristics for:
Table 11-13	2.4 GHz Operation
Table 11-14	5 GHz Operation

Table 11-13 Transmitter Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	5 MHz center frequency	2.412	—	2.472	GHz
P_{out}	Mask compliant output power					
	1 Mbps	See Note 1	—	17	—	dBm
	6 Mbps		—	17	—	dBm
	HT20, MCS0		—	16	—	dBm
	HT40, MCS0		—	15	—	dBm
	EVM compliant output power:					
	54 Mbps	See Note 1	—	13.5	—	dBm
	HT20, MCS15		—	12	—	dBm
	HT40, MCS15		—	11	—	dBm
SP_{gain}	PA gain step	See Note 2	—	0.5	—	dB
A_{pl}	Accuracy of power leveling loop	See Note 3	—	±2	—	dB
Z_{RFout_load}	Recommended PA single-ended load impedance	See Note 4	—	50	—	Ω
OP1dB	Output P1dB (max. gain)	See Note 5	—	19	—	dBm
OIP3	Output third order intercept point (max. gain)	See Note 5	—	27	—	dBm
ER_{phase}	I,Q phase error		—	±0.11	—	°
ERamp	I,Q amplitude error		—	±0.4	—	%
RS	Synthesizer reference spur: 2/3 RF	—	—	-—	-60	dBc
TTpowup	Time for power up (from synthesizer on)	—	—	1.5	—	µs

1. Measured using the internal PA recommended by Qualcomm Atheros under open-loop power control.
2. Guaranteed by design.
3. Manufacturing calibration required.
4. See the impedance matching circuit in the Atheros reference design schematics. To achieve good RF performance, it is strongly recommended not to alter the RF portion of the Atheros reference design for different matching networks.
5. Measured at the antenna connector port of the reference design, which includes Tx/Rx antenna switch and XLNA.

Table 11-14 Transmitter Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	20 MHz center frequency	5.18	—	5.825	GHz
P_{out}	Mask compliant output power					
	6 Mbps	See Note 1	—	23.5	—	dBm
	HT20, MCS0		—	23.5	—	
	HT40, MCS0		—	22.5	—	
	EVM compliant output power					
	54 Mbps	See Note 1	—	20	—	dBm
	HT20, MCS23		—	19	—	
	HT40, MCS23		—	19	—	
SP_{gain}	Transmit output frequency range	See Note 2	—	0.25	—	dB
A_{pl}	PA gain step	See Note 3	—	±2	—	dB
Z_{RFout_load}	Accuracy of power leveling loop	See Note 4	—	50	—	Ω
OP1dB	Output P1dB (max gain)	See Note 5	—	29	—	dBm
OIP3	Output third order intercept point (max gain)	See Note 5	—	37	—	dBm
SS	Sideband suppression		—	-40	—	dBc
LO_{leak}	LO leakage: at 2/3 of the RF output					
	@ RF=5.15-5.35 GHz (FCC)		—	-49	—	dBm
	@ RF=5.35-5.725 GHz (ETSI)			-47	—	dBm
	@ RF=5.725-5.825 GHz (FCC)			-49	—	dBm
RS	Synthesizer reference spur		—	—	-60	dBc
TTpowup	Time for power up (from synthesizer on)		—	1.5	—	µs

1. Output power numbers are measured on Qualcomm Atheros reference design that includes Se5003L, Tx/ Rx Antenna switch
2. Guaranteed by design.
3. Manufacturing calibration required.
4. See the sample impedance matching circuit in the Atheros reference design schematics. To achieve good RF performance, it is strongly recommended not to alter the RF portion of the Qualcomm Atheros reference design for different matching networks.
5. Measured at the antenna connector port of the reference design, which includes Tx/Rx antenna switch and XLNA.

11.6.3 Synthesizer Characteristics

Table 11-15 and Table 11-16 summarize the synthesizer characteristics for the QCA9558.

Table 11-15 Synthesizer Composite Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out)					
	At 30 KHz offset	—	—	–95	—	dBc/Hz
	At 100 KHz offset		—	–97	—	
	At 500 KHz offset		—	–112	—	
	At 1 MHz offset		—	–119	—	
F_c	Center channel frequency	—	2.412	—	2.472	GHz
F_{ref}	Reference oscillator frequency	± 20 ppm[1]	—	40	—	MHz
TS_{powup}	Time for power up	—	—	200	—	µs

1. Over temperature variation and aging.

Table 11-16 Synthesizer Composite Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out)					
	At 30 KHz offset	—	—	–92	—	dBc/Hz
	At 100 KHz offset		—	–95	—	
	At 500 KHz offset		—	–105	—	
	At 1 MHz offset		—	–110	—	
F_c	Center channel frequency	Center frequency at 5 MHz spacing[1]	4.9425	—	5.825	GHz
F_{ref}	Reference oscillator frequency	± 20 ppm[2]	—	40	—	MHz
TS_{powup}	Time for power up	—	—	200	—	µs

1. Frequency is measured at the Tx output.
2. Over temperature variation and aging.

11.7 Power Consumption Parameters

The following conditions apply to the typical characteristics unless otherwise specified:

V_{DD33} = 3.3V, T_{amb} = 25 °C

Table 11-17 and Table 11-17 show the typical power drain of the on-chip power supply as a function of the QCA9558's operating mode.

Table 11-17 Power Consumption for 2.4 GHz Operation

Operating Mode[1]	3.3 V Supply[4] (mA)	VDD_DDR[5] (mA)	VDD12[5] (mA)	VDD25[5] (mA)
Tx (Three-chain at 23 dBm[2])	673	21	824	22
Tx (Three-chain at 17 dBm[3])	850	21	825	22
Rx (Three-chain)	615	19	907	22

1. PCIE RC interface, USB, RGMII, SGMII are all in maximum data transfer condition and CPU in maximum utilization.
2. Tx output power of 23 dBm with external PA
3. Tx output power of 17 dBm with internal PA
4. Current consumption from 3.3 V includes analog, RF, USB and the 1.2 V power using the internal switching regulator
5. Current consumption of the VDD_DDR, VDD12 and VDD25 power rails from the QCA9558

Table 11-18 Power Consumption for 5 GHz Operation

Operating Mode[1]	3.3 V Supply[3] (mA)	VDD_DDR[4] (mA)	VDD12[5] (mA)	VDD25[5] (mA)
Tx (Three-chain at 23 dBm[2])	595	9	819	21
Rx (Three-chain)	550	11	905	21

1. PCIE RC interface, USB, RGMII, SGMII are all in maximum data transfer condition and CPU in maximum utilization.
2. Tx output power of 23 dBm with external PA
3. Current consumption from 3.3 V includes analog, RF, USB and the 1.2 V power using the internal switching regulator
4. Current consumption of the VDD_DDR, VDD12 and VDD25 power rails from the QCA9558

12 AC Specifications

12.1 DDR Interface Timing

Figure 12-1 shows the DDR output timing. See Table 12-1 for timing values.

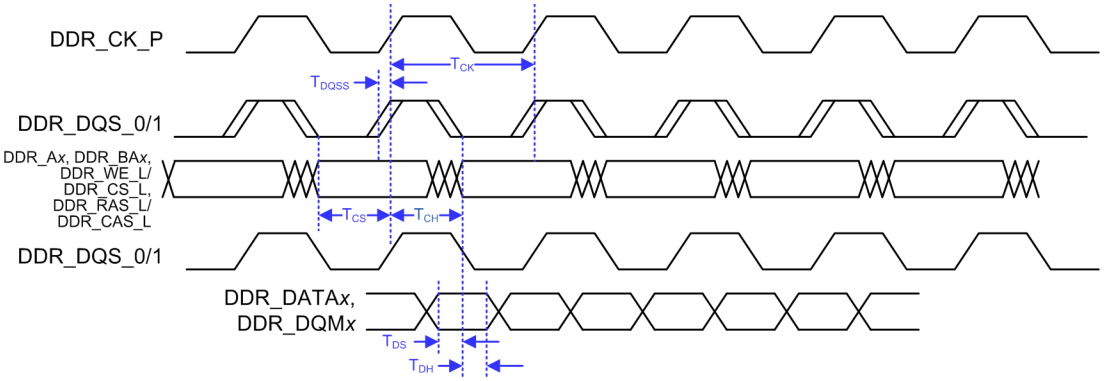


Figure 12-1 QCA9558-to-DDR Device Write Transaction Timing

Table 12-1 DDR Output Timing Values[1]

Parameter	Reference Signal	Min	Max	Comments
T_{CK}	—	3.3 ns	—	Normal period of CK_P clock output signal
T_{IS}	DDR_CK_P	1.7 ns	—	CLK-ADDR/CMD setup time
T_{IH}	DDR_CK_P	0.5 ns	—	CLK-ADDR/CMD hold time
T_{DQSS}	DDR_CK_P	—	0.3 ns	CLK-DQS skew
T_{DS}	DDR_DQS_0/1	0.4 ns	—	DQS-DQ setup time
T_{DH}	DDR_DQS_0/1	0.5 ns	—	DQS-DQ hold time

1. These numbers assume a 300 MHz DDR_CK_P frequency. Control signals include all address, bank address, RAS, CAS, CS_L, and CKE WE_L signals. Data signals include data and data mask signals.

12.2 DDR Input Timing

Figure 12-2 shows the DDR input timing. See Figure 12-2 for timing values.

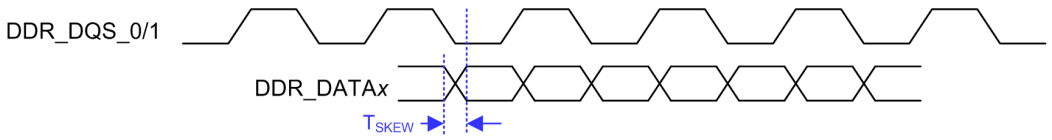


Figure 12-2 DDR Input Timing

Table 12-2 DDR Input Timing Values

Parameter	Reference Signal	Min	Max	Comments
T_{SKEW}	DDR_DQS_0/1	—	0.4 ns	Maximum skew from DQS to DQ being stable from memory

12.3 SGMII Driver AC Characteristics

Table 12-3 SGMII Driver AC Characteristics

Parameter	Reference Signal	Min	Max	Comments
T_{FALL}	SGMII_SIN/SGMII_SIP SGMII_SON/SGMII_SOP	100 pSec	200 pSec	V_{OD} Fall Time
T_{RISE}		100 pSec	200 pSec	V_{OD} Rise Time
T_{SKEW}[1]		—	20 pSec	Skew between two members of a differential pair

1. Skew measured at 50% of the transition

12.4 RGMII Output Timing

Figure 12-3 shows the RGMII output timing. See Table 12-4 for timing values

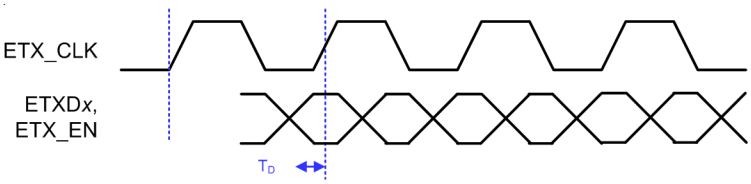


Figure 12-3 RGMII Output Timing

Table 12-4 RGMII Output Timing Values[1]

Parameter	Reference Signal	Comments			
T_D	ETX_CLK	Multiple options to delay the ETXD with respect to the ETX_CLK signal[2]			
		Setting	**Min**	**Max**	**Unit**
		0	-850	-1200	ps
		1	-200	-700	ps
		2	50	-100	ps
		3	550	350	ps
T_D	ETX_CLK	Multiple options to delay the ETX_EN with respect to the ETX_CLK signal[2]			
		Setting	**Min**	**Max**	**Unit**
		0	450	-950	ps
		1	0	-350	ps
		2	500	100	ps
		3	900	-100	ps

1. See Ethernet Configuration (ETH_CFG) for the register setting.
2. The negative sign on the delay indicates that the data edge is before the clock edge.

12.5 RGMII Input Timing

Figure 12-4 shows the RGMII input timing. See Table 12-5 for timing values.

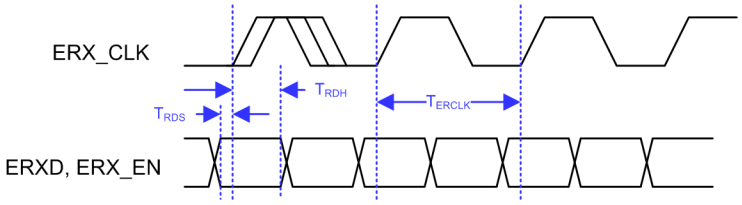


Figure 12-4 RGMII Input Timing

Table 12-5 RGMII Input Timing Values[1]

Parameter	Reference Signal	Min	Comments			
T_{ERCLK}	—	8 ns	Nominal RGMII clock			
T_{RDS}	ERX_CLK	Configurable	Multiple options to delay ERX_CLK signal ETH_XMII_RX_DELAY:			
			Setting	**Min**	**Max**	**Unit**
			0	600	1600	ps
			1	1120	2500	ps
			2	1570	3400	ps
			3	2020	4300	ps
T_{RDH}	ERX_CLK	Configurable	Multiple options to delay the ERX_CLK signal			

1. For a given DELAY setting, T_{RDS} indicates the setup margin available at the registering flop assuming the CLK and the DATA are aligned at the IO pins.

12.6 MII Mode Timing

Figure 12-5 shows the MII mode timing. See Table 12-6 for timing values.

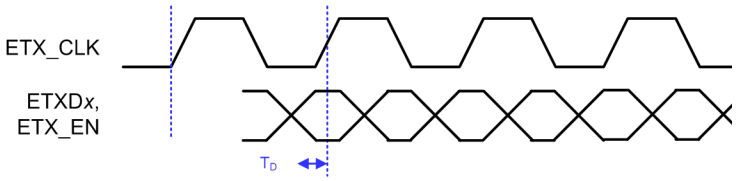


Figure 12-5 MII Mode Timing

Table 12-6 MII Mode Timing Values[1]

Parameter	Reference Signal	Min	Comments
T_{ETCLK}	—	40 ns	Nominal MII clock
T_{TDS}	—	Configurable	Configure using the Ethernet Configuration (ETH_CFG) register (ETH_TXD_DELAY and ETH_TXEN_DELAY bits); zero at reset.
T_{TDH}	—	Configurable	

1. The ETH_RXD_DELAY and ETH_RXDV_DELAY fields of the ETH_CFG registers configure the delays in the input path. Upon reset, because the delays are matched between the data and clock, for edge aligned input, setup/hold is not guaranteed. Four Steps of Delay are possible. [Min, Max] delay per step is [400 ps, 900 ps].

12.7 MDIO Timing

The management data clock (MDC) is generated by the 100 MHz clock from the internal Ethernet PLL or by the REF clock via a configurable divider.

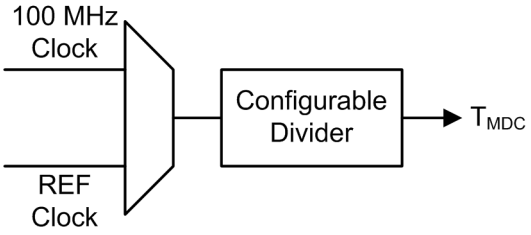


Figure 12-6 MDC Generation

MDIO / MDC is also available through the GPIO pads. See GPIO on page 71 for details.

It is strongly recommended to derive the MDC from the REF clock for external RGMII interface. For external GMII interface, it is recommended to derive the MDC source from the REF clock and use divider value of 0xB.

Figure 12-10 shows the QCA9558 management data input/output (MDC/MDIO) timing.

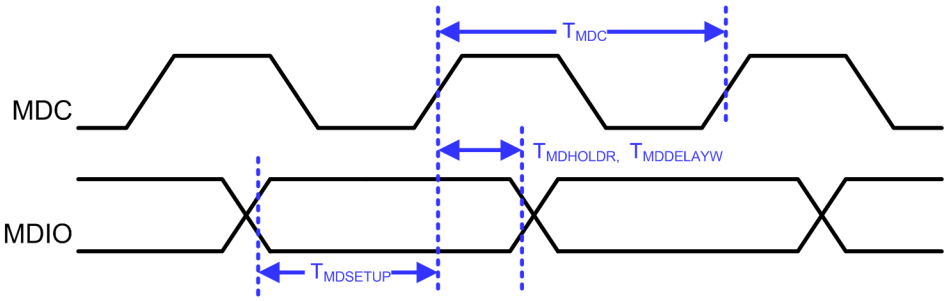


Figure 12-7 QCA9558 MDC/MDIO Timing

Table 12-7 MDC/MDIO Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
T_{MDC}	MDC Period[1]	100	1450	2450	ns
T_{MDCH}	MDC High Period	—	50	—	%
T_{MDCL}	MDC Low Period	—	50	—	%
$T_{MDSETUP}$	Input Setup Time Requirement MDC to MDIO[2]	5	—	—	ns
$T_{MDHOLDR}$	Input Hold Time Requirement MDC to MDIO[3]	0	—	—	ns
$T_{MDDELAYW}$	Delay Between MDC Rising Edge and Data Toggling Edge[4]	20	—	50	ns

1. Configurable with the source 100 MHz or by using REF clock.
2. During read, MDIO slave device data to be stable with respect to the rising edge of MDC clock.
3. During read, MDIO Slave device data hold time with respect to rising edge of MDC clock.
4. For MDIO write, data is output with respect to positive edge of MDC, with a delay of 20 ns or 50 ns depending on the clock selected for the SPI module by using the SWITCH_CLOCK_SPARE register.

12.8 SPI Timing

Figure 12-8 shows the SPI timing. See Table 12-8 for timing values.

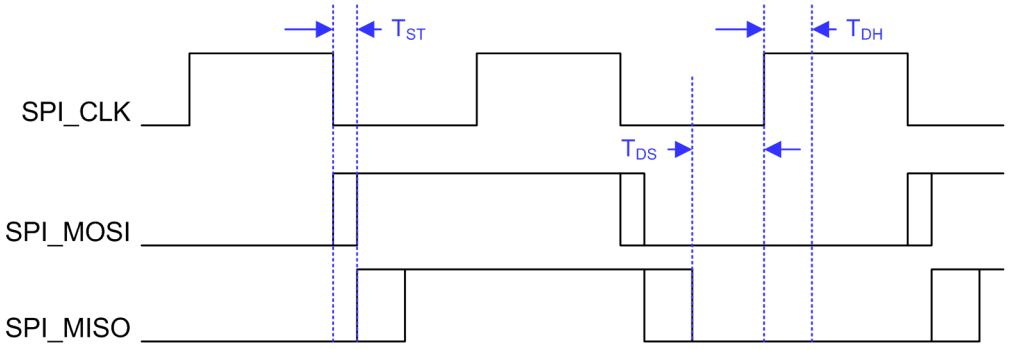


Figure 12-8 SPI Timing

Table 12-8 SPI Timing Values

Parameter	Min	Max	Comments
T_{DS}	11.0 ns	—	Minimum needed by the QCA9558
T_{ST}	—	3 ns	Maximum time by which data is available
T_{DH}	1 ns	—	Minimum hold duration

Actual SPI operating frequency is dependent on the CLK-to-SO flash delay and the CLK/MISO signals propagation delay in the board.

The minimum SPI_CLK period is 2 * (TDS + (CK-to-SO flash delay) + (board propagation delay of CLK + board propagation delay of MISO signals).

12.9 Reset Timing

The VDD33, VDD25 and VDD12 voltages can come up in any sequence. The last one to come up determines when the internal reset is deasserted. Typically, with an internal regulator generating VDD_DDR, VDD_DDR is available approximately 10 µs after VDD33, VDD25, and VDD12 are stable.

It is desirable for VDD12 to come up before VDD25.

Figure 12-9 shows an the QCA9558 power on and reset timing.

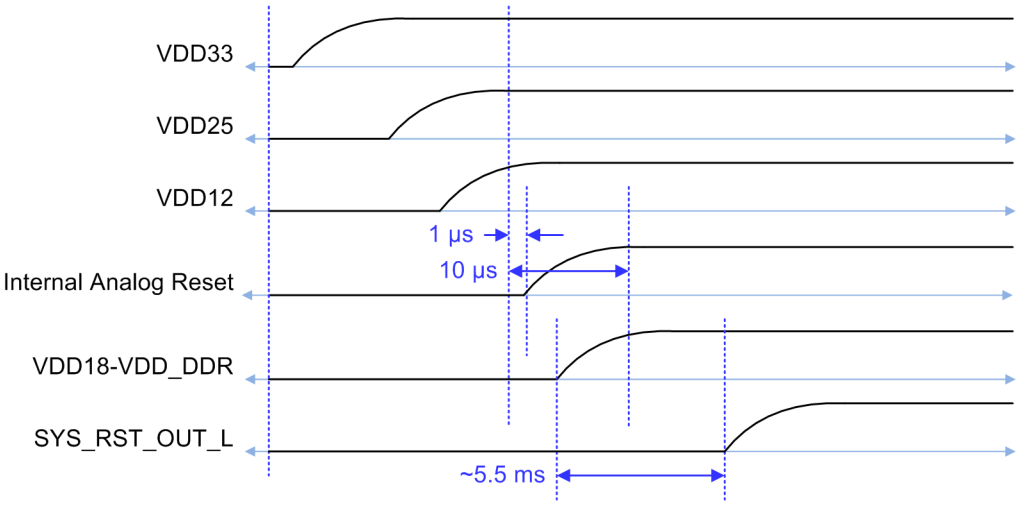


Figure 12-9 Power on and Reset Timing

Figure 12-10 shows the bootstrap timing.

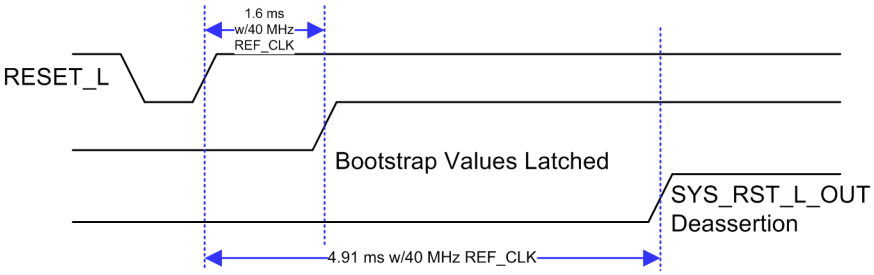


Figure 12-10 Bootstrap Timing

13 Package Dimensions

The QCA9558 is packaged in a BGA-415 package. The body size is 18 mm by 18 mm. Moisture Sensitivity Level (MSL) for this device is L3 per JSTD020D-01. The package drawings and dimensions are provided in Figure 13-1.

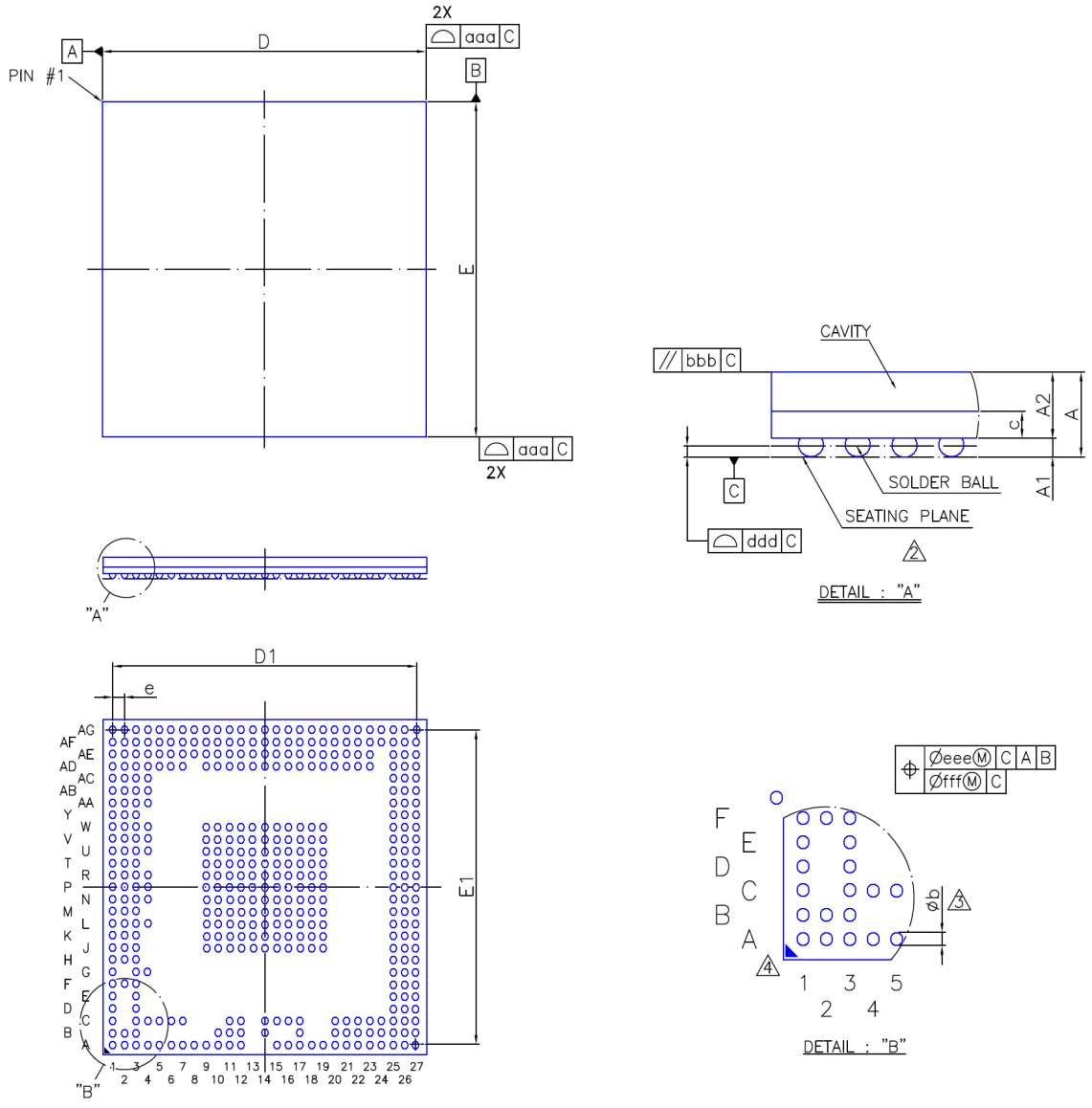


Figure 13-1 QCA9558 Package Drawing

Table 13-1 Package Dimensions

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	—	—	1.20	mm	—	—	0.047	inches
A1	0.25	0.25	0.30	mm	0.008	0.010	0.012	inches
A2	0.84	0.89	0.94	mm	0.033	0.035	0.037	inches
b	0.30	0.35	0.40	mm	0.012	0.014	0.016	inches
c	0.32	0.36	0.40	mm	0.013	0.014	0.016	inches
D/E	17.90	18.00	18.10	mm	0.705	0.709	0.713	inches
D1/E1	—	16.90	—	mm	—	0.665	—	inches
e	—	0.65	—	mm	—	0.026	—	inches
aaa		0.10		mm		0.004		inches
bbb		0.15		mm		0.006		inches
ddd		0.15		mm		0.006		inches
eee		0.15		mm		0.006		inches
fff		0.08		mm		0.003		inches
MD/ME		27/27				27/27		

[1] Controlling dimension: Millimeters
[2] Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
[3] Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
[4] There shall be a minimum clearance of 0.25 mm between the edge of the solder ball and the body edge.
[5] Special characteristics C class: bbb, ddd.
[6] The pattern of pin 1 fiducial is for reference only.

14 Ordering Information

The order number QCA9558-AT4A specifies a lead-free, halogen-free, standard-temperature version of the QCA9558.

The order number QCA9558-AT4A specifies-R a tape-and-reel version of the QCA9558.