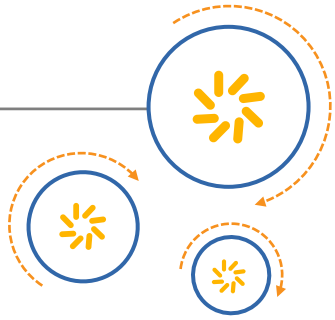
Qualcomm Atheros, Inc.



IPQ4019 Access Point SoC

Device Specification

80-Y9347-19 Rev. E

March 3, 2016

Qualcomm Atheros, Inc.
1700 Technology Drive
San Jose, CA 95110
U.S.A.

Revision history

Revision	Date	Description
A	August 2015	Initial release
B	September 2015	1. Table 2-2 “Pin assignments”: Change E24 and J25 to GND. Change B4, D21, F27, G27, L27, M27 to NC. 2. Table 2-5 “5 GHz Radio Signals”: Remove B4. 3. Table 2-7 “2.4 GHz Radio Signals”: Remove D21, E24, J25, F27, G27, L27, M27. 4. Table 2-13 “Font-end”: RBIAS is refined. 5. Section 3 “Electrical Specifications”: new 6. Section 4.5 “Thermal characteristics”: new.
C	November 2015	**Introduction** ■ IPQ4019 general description: revised functional block diagram ■ IPQ4019 features: revised CPU clock, Flash memory, Network subsystem, High-speed interfaces, and Miscellaneous interfaces **Pin Definitions** ■ Clock, power, and reset: revised AD12 and R24 functional description ■ DDR3L: revised P3, V3, R2, and P2 functional description ■ Front-end: revised AD27 functional description ■ PSGMII: revised PSGMII_RXN, SGMII_RXP, SGMII_TXN, and SGMII_TXP functional description ■ GPIO: removed smart_ant0, smart_ant1, smart_ant2 and smart_ant3, and revised GPIO44, GPIO45, GPIO46, GPIO47 functional description **Electrical Specifications** ■ Recommended operating conditions: updated operating temperature ■ Power sequencing: added power-on sequence ■ Digital characteristics: added digital I/O characteristics for 3.3 V IO and DDR3 PAD ■ Timing characteristics: added timing diagram conventions and rise and fall time specifications ■ Memory support: added DDR, EBI2 NAND interface, eMMC NAND flash on SDIO ■ Connectivity: added USB, UART, SDCC, I2C, I2S/TDM, SPI (master), PSGMII, RGMII **Mechanical Information** ■ Device ordering information: updated ordering information

Revision	Date	Description
D	January 2016	**Pin Definitions** ■ IPQ4019 pin assignments (top view), 2.4 GHz radio signals: updated E24, J25, F27, G27, L27, M27 **Electrical Specifications** ■ Crystal: updated crystal accuracy ■ DDR: updated differential input cross point voltage ■ RGMII interface: added a note for delay option ■ Radio characteristics: added Tx/Rx characteristics ■ Power consumption: added power consumption **Part Reliability** ■ Reliability qualification summary: added silicon reliability results and package reliability results ■ Qualification sample description: added IPQ4019 characteristics
E	March 2016	**Mechanical Information** ■ Device physical dimensions: added linear tolerances and notes

Contents

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1 Introduction

1.1 IPQ4019 general description

The IPQ4019 is a highly integrated system-on-chip (SoC) designed for high-performance, power-efficient, and cost-effective 2×2, 802.11ac, dual-band concurrent access-point applications. The SoC incorporates a quad-core ARM Cortex A7 processor, two dual-band, concurrent 802.11ac Wave-2 Wi-Fi subsystems, and a five-port Gigabit Ethernet Layer2/3/4 multilayer switch supporting line rate network address translation (NAT). It supports one USB3.0 and one USB2.0. It also supports other miscellaneous interfaces, which can be configured as general purpose I/O pins. The block diagram in Figure 1-1 shows the major components of the SoC.

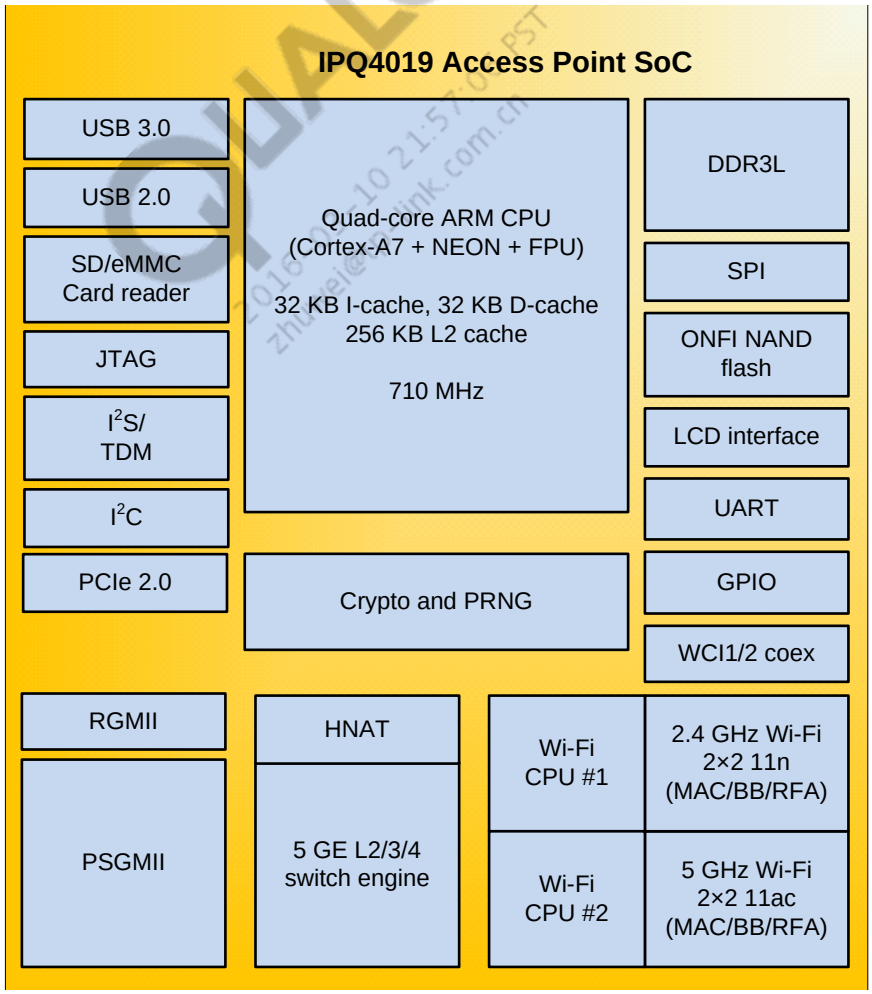


Figure 1-1 IPQ4019 functional block diagram

1.2 IPQ4019 features

- Quad-core ARM Cortex-A7 at 710 MHz
  - 32 KB instruction cache and 32 KB data cache per core
  - 256 KB L2 cache (shared)
  - Each core has NEON and FPU
  - Dynamic frequency scaling
  - Secure boot
- DRAM memory
  - JEDEC standard DDR3L SDRAM
  - Up to 1 GB
  - Supports 16-bit DDR interface
  - 667 MHz clock rate; 1333 MHz data rate
- Flash memory
  - SPI (x1b)
  - Supports SPI NOR
  - Supports SPI mode 0, 1, 2, 3
  - Cache and non-cache mode read channel
- Dual Wi-Fi subsystem with Qualcomm® VIVE™ technology
  - On-chip dual-band concurrent (DBDC) Wi-Fi, supporting MU-MIMO beamforming techniques, in either of these configurations:
    - 2×2 5-GHz 802.11ac plus 2×2 2.4-GHz 802.11ac (256QAM)
    - 2×2 5-GHz 802.11ac plus 2×2 5-GHz 802.11ac
  - Feature compatible with QCA99xx Wi-Fi chips
  - Two dedicated CPUs for Wi-Fi offloading and feature growth
  - Cooperates with QFE19x2 front-end chips or 3rd-party front-end chipsets
  - Smart antenna diversity
- Network Subsystem
  - Integrated L2/3 multilayer switch/router
  - ACL (access control list) mask rules
  - Hardware network address translation (NAT) engine
  - Supports flow cookie
  - Traffic steering
  - Seamless integration with Linux network stack
  - Supports external multiport gigabit Ethernet PHYs QCA8075 or QCA8072 via PSGMII.

- Supports external single port gigabit Ethernet PHYs AR8031/3/5 or AR8032 via RGMII and/or RMIIs.

- Security
  - Crypto engine
    - Encryption algorithms AES (128 and 256 bit key support) and DES/3DES
    - Authentication algorithms SHA1, SHA224 (the result of supporting SHA256), SHA256, and HMAC-SHA1 and HMAC-SHA2
    - XTS/CTR/CCM/CMAC mode for AES
    - CBC/ECB mode both for AES and DES/3DES.
  - Trust Zone
  - Pseudo-random number generator
- High-speed interfaces
  - 1× PCIe 2.0
  - 1× PSGMII
  - 1 × USB3.0
  - 1 × USB2.0
- Display
  - LCD controller
  - MIPI DBI v2.0 type B interface
- Miscellaneous interfaces
  - I^2S/TDM
  - I^2C
  - UART
  - PSGMII
  - RGMII
  - JTAG
  - GPIO
- Package
  - 18 mm × 18 mm 583-ball BGA micro scale package (583MSP) package

1.3 Terms and abbreviations

Table 1-1 defines terms, abbreviations, and acronyms commonly used throughout this document.

Table 1-1 Terms and abbreviations

Term	Definition
ACL	Access control list
BB	Baseband
BLSP	BAM-enabled low-speed peripheral
DDR	Double data rate
GE	Gigabit Ethernet
HNAT	Hardwired network address translation
LDO	Low drop-out (voltage regulator)
MDIO	Management data input/output
PCM	Pulse code modulation
PRNG	Pseudo-random number generator
PSGMII	Penta serial gigabit media independent interface
RGMII	Reduced gigabit media independent interface
SoC	System on a chip
SPDIF	Sony/Philips Digital Interface Format
SPI	Serial peripheral interface
TDM	Time-division multiplexed

1.4 Special marks

Table 1-2 defines special marks used in this document.

Table 1-2 Special marks

Mark	Definition
0x0000	Hexadecimal numbers are identified with an x in the number, for example, 0x0000. All numbers are decimal (base 10), unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number, for example, 0011 (binary).
|	A vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin Definitions

2.1 IPQ4019 pin map

Table 2-2 shows a high-level view of the pin assignments. Table 2-1 defines the color coding within Table 2-2.

The text within Table 2-2 is difficult to read when viewing an 8½" by 11" hard copy. Other viewing options are available:

- Print that one page on an 11" by 17" sheet.
- View the graphic soft copy and zoom in.

Table 2-1 Legend for pin assignments

Color	Net Group
	PCI*
	USB*
	GPIO
	VDD

Table 2-2 IPQ4019 pin assignments (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	GND	GND	VDD11_LO_R1	VDD33_VCO_R1	VDD11_BIAS_R1	XLNA_1_R1	FEM_1_R1		VDD11_TX_CH2	LNA5N_CH2	LNA5P_CH2		VDD11_TX_CH3	LNA5N_CH3	LNA5P_CH3	CHIP_PWD_L	GPIO1	GPIO3	VDD11_CLKBUF_R0	VDD11_BB_R0	VDD11_LO_R0	VDD33_VCO_R0	VDD11_BIAS_R0	XPA_0_R0	XLNA_0_R0	GND	GND	A
B	GND	VDD33_BB_R1	VDD33_SYN_R1	NC	VDDIO_R1	XPA_1_R1	FEM_0_R1		VDD11_RX_CH2	GND	GND		VDD11_RX_CH3	GND	GND	AVDD33	GPIO0	GPIO4	VDD11_ADDAC_R0	VDD33_BB_R0	VDD33_SYN_R0	VDDIO_R0	XLNA_1_R0	FEM_0_R0	GND	GND	GND	B
C	VDD11_ADDAC_R1	VDD11_BB_R1	GND	GND	GND	XPA_0_R1	GND	DA5_CH2	GND	GND	GND	DA5_CH3	GND	GND	GND	GND	GPIO2	GPIO5	VDD33_BBPLL_R0	GND	GND	XPA_1_R0	FEM_1_R0	GND	GND			C
D	GND	VDD33_BBPLL_R1	GND	GND	GND	GND	XLNA_0_R1	GND	GND	PDET_CH2	GND	GND	GND	PDET_CH3	GND	GND	VDDIO33	GND	GND	GND	NC	GND	GND	DA2_CH0		VDD11_TX_CH0	LNA2P_CH0	D
E	XTALI	GND	GND	GND																				DA5_CH0	GND	VDD11_RX_CH0	LNA2N_CH0	E
F	XTALO	AVDD33	GND	GND																				GND	GND	GND	LNA5N_CH0	F
G	AVDD11_LDO	GND	GND	GND			GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD	VDD	VDD	VDD	GND	GND			PDET_CH0	GND	VDD11_TX_CH1	LNA5P_CH0	G
H	GND	GPIO6	GPIO7	GPIO8			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	GND	GND			GND				H
J	GPIO9	GPIO10	GPIO11	VDDIO33			VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GND	DA5_CH1	DA2_CH1	LNA2P_CH1	J
K	GPIO12	GPIO13	GPIO14	VDDIO33			VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GND	GND	GND	LNA2N_CH1	K
L	GPIO15	GPIO16	GPIO17	GPIO18			VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			PDET_CH1	GND	VDD11_RX_CH1	LNA5N_CH1	L
M	GPIO19	GND	GND	GND			VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GND	GND	GND	LNA5P_CH1	M
N	DDR_RST_N	DDR_CKE	DDR_ADDR[15]	VDDQ			VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GPIO62	GPIO63	GND	GND	N
P	DDR_ODT	DDR_CS_N[0]	DDR_RAS_N	VDDQ			VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GPIO67	GPIO68	GPIO69	GPIO61	P
R	DDR_ADDR[10]	DDR_WE_N	DDR_ADDR[3]	VDDQ			VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD	GND			VDDIO_LDO_R	GPIO64	GPIO65	GPIO66	R
T	DDR_ADDR[2]	DDR_BA[2]	DDR_ADDR[11]	VDDQ			VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD	VDD			VDDIO33	GPIO58	GPIO59	GPIO60	T
U	DDR_ADDR[12]	DDR_ADDR[1]	DDR_ADDR[0]	VDDQ			VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD	VDD			GPIO54	GPIO55	GPIO56	GPIO57	U
V	DDR_CK_P	DDR_ADDR[13]	DDR_CAS_N	VDDQ			VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD	VDD			GPIO50	GPIO51	GPIO52	GPIO53	V
W	DDR_CK_N	DDR_ADDR[9]	DDR_ADDR[14]	AVDD11_LDO			VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD	VDD			GPIO46	GPIO47	GPIO48	GPIO49	W
Y	DDR_ADDR[5]	DDR_ADDR[7]	DDR_ADDR[8]	AVDD11_LDO			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD			VDDIO33	GPIO43	GPIO44	GPIO45	Y
AA	DDR_BA[0]	DDR_ADDR[4]	DDR_ADDR[6]	VDD11_LDO			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD			VDDIO33	GPIO40	GPIO41	GPIO42	AA
AB	DDR_DQ[7]	DDR_BA[1]	DDR_DQ[6]	VDD135																				GPIO36	GPIO37	GPIO38	GPIO39	AB
AC	DDR_DQS[0]	DDR_DQ[5]	DDR_DQ[4]	VTT_LDO																				GND	GND	GND	GND	AC
AD	DDR_DQS_N[0]	DDR_DQ[3]	DDR_DQ[2]	VDDQ	VDDQ	DDR_VREF_DQ[1]	GND	AVDD11	GPIO20	GND	VDDIO33	VDDIO_LDO_B	GND	AVDD11_LDO	AVDD11	PCIE_CLKOUT_P	PCIE_CLKOUT_N	AVDD11	GND	AVDD11_LDO	AVDD11_LDO	AVDD11	AVDD33	AVDD11_LDO	AVDD11_LDO	AVDD25_REG	RBIAS	AD
AE	DDR_DQ[1]	DDR_DQ[0]	DDR_DQM[0]	DDR_DQ[8]	DDR_DQ[9]	DDR_DQ[12]	GND	GPIO21	GPIO22	GPIO23	GPIO26	GPIO25	GND	GND	AVDD11	GND	GND	AVDD33	GND	GND	AVDD11	AVDD33	GND	AVDD11	AVDD11_LDO	GND	GND	AE
AF	VDDQ	DDR_VREF_DQ[0]	DDR_DQM[1]	DDR_DQ[10]	DDR_DQ[11]	DDR_DQ[13]	GND	GPIO24	GPIO27	GPIO31	GPIO29	GPIO30	GND	PCIE_TXP	PCIE_RXP	GND	USB2_DP	GND	USB1_TXP	GND	USB1_RXP	USB1_DP	GND	PSGMII_TXP	PSGMII_RXP	GND	CLK_25M_O	AF
AG	GND	VDDQ	DDR_DQS_N[1]	DDR_DQS[1]	DDR_DQ[14]	DDR_DQ[15]	GND	GPIO28	GPIO32	GPIO33	GPIO34	GPIO35	GND	PCIE_TXN	PCIE_RXN	GND	USB2_DM	GND	USB1_TXN	GND	USB1_RXN	USB1_DM	GND	PSGMII_TXN	PSGMII_RXN	AVDD11	GND	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

2.2 I/O parameter definitions

Table 2-3 I/O description (pad type) parameters

Symbol	Description
AI	Analog input
AO	Analog output
GND	Ground
NC	Not connected; leave disconnected
RF IN	RF input
RF Out	RF output
I	Digital input signal
O	Digital output signal
IO	Digital bidirectional signal

2.3 Pin descriptions

Descriptions of pins are presented in the tables of this section. The pins are grouped by function.

2.3.1 Clock, power, and reset

Table 2-4 Clock, power, and reset

Pin ID	Pin name	Voltage	Type	Functional description
AD8, AD15, AD18, AD22, AE15, AE21, AE24, AG26	AVDD11	1.1	AI	1.1 V analog power
G1, W4, Y4, AD14, AD20, AD21, AD24, AD25, AE25	AVDD11_LDO	1.1	AI	1.1 V analog power Connect with pin AA4 on board
B16, F2, AD23, AE18, AE22	AVDD33	3.3	AI	3.3 V analog power
G16, G17, G18, G19, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, J7, J8, K7, K8, L7, L8, M7, M8, N7, N8, P7, P8, R7, R8, R20, T7, T8, T20, T21, U7, U8, U20, U21, V7, V8, V20, V21, W7, W8, W20, W21, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, AA7, AA8, AA9, AA10, AA11, AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21	VDD	1.1	I	Digital power
AA4	VDD11_LDO	1.1	O	1.1 V LDO output
AB4	VDD135	1.35	I	Power input for VDD11_LDO and VTT_LDO. Route a dedicated wire from the 1.35 V switching regulator.
D17, J4, K4, T24, Y24, AA24, AD11	VDDIO33	3.3	I	Power for GPIO
AC4	VTT_LDO	0.5 * VDD135	O	DDR termination voltage
E1	XTALI		I	Crystal oscillator input
F1	XTALO		O	Crystal oscillator output
A16	CHIP_PWD_L		I	Chip power-on reset
AD12	VDDIO_LDO_B		O	LDO output for GPIO domain 2 (GPIO20 to GPIO35)
R24	VDDIO_LDO_R		O	LDO output for GPIO domain 4 (GPIO52 to GPIO69)

2.3.2 5 GHz radio

In pin names and descriptions, “radio 1” or “R1” refers to the 5 GHz radio. “Channel 2”, “CH2”, “Channel 3”, and “CH3” are on the 5 GHz radio.

Table 2-5 5 GHz radio signals

Pin ID	Pin Name	Voltage	Type	Functional description
A10 A11	LNA5N_CH2 LNA5P_CH2	1.1	IA	LNA differential input pair for chain 2
A14 A15	LNA5N_CH3 LNA5P_CH3	1.1	IA	LNA differential input pair for chain 3
C8	DA5_CH2	1.1	OA	DA single-ended output
C12	DA5_CH3			
D10	PDET_CH2	1.1	IA	PDET inputs
D14	PDET_CH3			
C6	XPA_0_R1		IO	External PA control
B6	XPA_1_R1			
D7	XLNA_0_R1		IO	External LNA control
A6	XLNA_1_R1			
B7	FEM_0_R1		IO	FEM control for CH0 of Radio 1
A7	FEM_1_R1			FEM control for CH1 of Radio 1

Table 2-6 5 GHz radio power and ground

Pin ID	Pin name	Voltage	Type	Functional description
C1	VDD11_ADDAC_R1	1.1	I	1.1 V power supply for Radio 1
C2	VDD11_BB_R1			
A5	VDD11_BIAS_R1			
A3	VDD11_LO_R1			
B9	VDD11_RX_CH2			
B13	VDD11_RX_CH3			
A9	VDD11_TX_CH2			
A13	VDD11_TX_CH3			
D2	VDD33_BBPLL_R1	3.3	I	3.3 V power supply for Radio 1
B2	VDD33_BB_R1			
B3	VDD33_SYN_R1			
A4	VDD33_VCO_R1			
B5	VDDIO_R1	3.3	I	

2.3.3 2.4 GHz radio

In pin names and descriptions, “radio 0” or “R0” refers to the 2.4 GHz radio. “Channel 0”, “CH0”, “Channel 1”, and “CH1” are on the 2.4 GHz radio.

Table 2-7 2.4 GHz radio signals

Pin ID	Pin name	Voltage	Type	Functional description
D27	LNA2P_CH0		IA	2.4 GHz LNA differential input pair for chain 0
E27	LNA2N_CH0			
J27	LNA2P_CH1		IA	2.4 GHz LNA differential input pair for chain 1
K27	LNA2N_CH1			
G27	LNA5P_CH0		IA	5 GHz LNA differential input pair for chain 0
F27	LNA5N_CH0			
M27	LNA5P_CH1		IA	5 GHz LNA differential input pair for chain 1
L27	LNA5N_CH1			
D24	DA2_CH0		OA	2.4 DA single-ended output
J26	DA2_CH1			
E24	DA5_CH0		OA	5 GHz DA single-ended output
J25	DA5_CH1			
G24	PDET_CH0		IA	PDET inputs
L24	PDET_CH1			
A24	XPA_0_R0		OA	External PA control
C22	XPA_1_R0			
A25	XLNA_0_R0		O	External LNA control
B23	XLNA_1_R0			
B24	FEM_0_R0			FEM control for CH0 of Radio 0
C23	FEM_1_R0			FEM control for CH1 of Radio 0

Table 2-8 2.4 GHz radio power and ground

Pin ID	Pin name	Voltage	Type	Functional description
B19	VDD11_ADDAC_R0	1.1	I	1.1 V power supply for Radio 0
A20	VDD11_BB_R0			
A23	VDD11_BIAS_R0			
A19	VDD11_CLKBUF_R0			
A21	VDD11_LO_R0			
E26	VDD11_RX_CH0			
L26	VDD11_RX_CH1			
D26	VDD11_TX_CH0			
G26	VDD11_TX_CH1			

Table 2-8 2.4 GHz radio power and ground (cont.)

Pin ID	Pin name	Voltage	Type	Functional description
C19	VDD33_BBPLL_R0	3.3	I	3.3 V power supply for Radio 0
B20	VDD33_BB_R0			
B21	VDD33_SYN_R0			
A22	VDD33_VCO_R0			
B22	VDDIO_R0	3.3	I	

2.3.4 DDR3L

Table 2-9 16/8-bit DDR3L

Pin ID	Pin name	Voltage	Type	Functional description
P1	DDR_ODT	1.35 V	O	
AE2	DDR_DQ[0]	1.35 V	I/O	DDR data[0:15]
AE1	DDR_DQ[1]			
AD3	DDR_DQ[2]			
AD2	DDR_DQ[3]			
AC3	DDR_DQ[4]			
AC2	DDR_DQ[5]			
AB3	DDR_DQ[6]			
AB1	DDR_DQ[7]			
AE4	DDR_DQ[8]			
AE5	DDR_DQ[9]			
AF4	DDR_DQ[10]			
AF5	DDR_DQ[11]			
AE6	DDR_DQ[12]			
AF6	DDR_DQ[13]			
AG5	DDR_DQ[14]			
AG6	DDR_DQ[15]			
V1	DDR_CK_P	1.35 V	O	Differential clock (+)
W1	DDR_CK_N			Differential clock (-)
N2	DDR_CKE	1.35 V	O	Clock enable
P3	DDR_RAS_N	1.35 V	O	Command outputs RAS_N, CAS_N, WE_N and CS_N[0]) define command outputs
V3	DDR_CAS_N			
R2	DDR_WE_N			
P2	DDR_CS_N[0]			
AE3	DDR_DQM[0]	1.35 V	O	Data mask
AF3	DDR_DQM[1]			

Table 2-9 16/8-bit DDR3L (cont.)

Pin ID	Pin name	Voltage	Type	Functional description
AA1	DDR_BA[0]	1.35 V	O	Byte access[0:2]
AB2	DDR_BA[1]			
T2	DDR_BA[2]			
U3	DDR_ADDR[0]	1.35 V	O	DDR command/address[0:15]
U2	DDR_ADDR[1]			
T1	DDR_ADDR[2]			
R3	DDR_ADDR[3]			
AA2	DDR_ADDR[4]			
Y1	DDR_ADDR[5]			
AA3	DDR_ADDR[6]			
Y2	DDR_ADDR[7]			
Y3	DDR_ADDR[8]			
W2	DDR_ADDR[9]			
R1	DDR_ADDR[10]			
T3	DDR_ADDR[11]			
U1	DDR_ADDR[12]			
V2	DDR_ADDR[13]			
W3	DDR_ADDR[14]			
N3	DDR_ADDR[15]			
AC1	DDR_DQS[0]	1.35 V	I/O	Differential data strobe for byte 0 and 1 (+)
AG4	DDR_DQS[1]			
AD1	DDR_DQS_N[0]			Differential data strobe for byte 0 and 1 (-)
AG3	DDR_DQS_N[1]			
N1	DDR_RST_N	1.35 V	O	Reset
AF2	DDR_VREF_DQ[0]	0.675 V	I	DDR RX reference voltage input
AD6	DDR_VREF_DQ[1]	0.675 V	I	DDR RX reference voltage input
N4, P4, R4, T4, U4, V4, AD4, AD5, AF1, AG2	VDDQ	1.35 V	I	DDR I/O power

2.3.5 PCIe 2.0

Table 2-10 PCIe 2.0 signals

Pin ID	Pin name	Voltage	Type	Functional description
AD17	PCIE_CLKOUT_N		AO	Clock to PCIe end point
AD16	PCIE_CLKOUT_P		AO	Clock to PCIe end point
AG15	PCIE_RXN		AI	PCIe receive lane – negative

Table 2-10 PCIe 2.0 signals (cont.)

Pin ID	Pin name	Voltage	Type	Functional description
AF15	PCIE_RXP		AI	PCIe receive lane – positive
AG14	PCIE_TXN		AO	PCIe transmit lane – negative
AF14	PCIE_TXP		AO	PCIe transmit lane – positive

2.3.6 USB 3.0 and 2.0

Table 2-11 USB 3.0 signals

Pin ID	Pin name	Voltage	Type	Functional description
AF22	USB1_DP		AI, AO	USB HS data positive
AG22	USB1_DM		AI, AO	USB HS data negative
AF21	USB1_RXP		AI	USB SS receive data positive
AG21	USB1_RXN		AI	USB SS receive data negative
AG19	USB1_TXN		AO	USB SS transmit data negative
AF19	USB1_TXP		AO	SS USB transmit data positive

Table 2-12 USB 2.0 signals

Pin ID	Pin name	Voltage	Type	Functional description
AF17	USB2_DP		AI, AO	USB HS data plus
AG17	USB2_DM		AI, AO	USB HS data negative

2.3.7 Front-end

Table 2-13 Front-end

Pin ID	Pin name	Voltage	Type	Functional description
AD26	AVDD25_REG	2.7	O	Power for pads and internal circuits.
AD27	RBIAS	1.175	O	Connect to an off-chip 5.9 Kohm (±1%) bias resistor

2.3.8 PSGMII

Table 2-14 PSGMII

Pin ID	Pin name	Voltage	Type	Functional description
AF27	CLK25M_O	1.2	O	Supply external PHY with 25 MHz clock
AG25	PSGMII_RXN	1.1	O	Differential negative output (6.25 Gbps in PSGMII mode)
AF25	PSGMII_RXP	1.1	O	Differential positive output (6.25 Gbps in PSGMII mode)
AG24	PSGMII_TXN	1.1	I	Differential negative input (6.25 Gbps in PSGMII mode)
AF24	PSGMII_TXP	1.1	I	Differential positive input (6.25 Gbps in PSGMII mode)

2.3.9 GPIO

Individual GPIOs are configured by software using GPIO_CFGn registers corresponding to the GPIO number.

Table 2-15 GPIO

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
B17	GPIO0	0	GPIO	3.3		
		1	JTAG TDI[1]	3.3	I	JTAG test data in
		–				
A17	GPIO1	0	GPIO	3.3		
		1	JTAG TCK[1]	3.3	I	JTAG test clock
		–				
C17	GPIO2	0	GPIO	3.3		
		1	JTAG TMS[1]	3.3	IO	JTAG test mode state
		–				
A18	GPIO3	0	GPIO	3.3		
		1	JTAG TDO[1]	3.3	Z	JTAG test data out
			boot_config(0)	3.3	I	
B18	GPIO4	0	GPIO	3.3		
		1	JTAG RST_N[1]	3.3	I	JTAG reset for debug
C18	GPIO5	0	GPIO	3.3		
		1	JTAG TRST_N[1]	3.3	I	JTAG test reset
		–				
H2	GPIO6	0	GPIO	3.3		
		1	mdio(0)	3.3 (output) 2.7 (input)	I/O	Management Data Input/Output
H3	GPIO7	0	GPIO	3.3		
		1	mdc	3.3	O	Management Data Clock
H4	GPIO8	0	GPIO	3.3		
		1	blsp_uart1_txd		O	Tx data
		2	wifi0_uart_txd		O	WIFI UART output
		3	wifi1_uart_txd		O	WIFI UART output
		–				
J1	GPIO9	0	GPIO	3.3		
		1	blsp_uart1_rxd		I	Rx data
		2	wifi0_uart_rxd(0)		I	WIFI UART input
		3	wifi1_uart_rxd(0)		I	WIFI UART input

Table 2-15 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
		–				
		5	wifi0_uart_txd		O	WIFI UART output
J2	GPIO10	0	GPIO	3.3		
		1	blsp_uart1_cts		I	Clear to send
		2	wifi0_uart_cts(0)		I	WIFI UART input
		3	wifi1_uart_cts(0)		I	WIFI UART input
		4	blsp_i2c0_sck(0)		I/O	I^2C0 sck
J3	GPIO11	0	GPIO	3.3		
		1	blsp_uart1_rts		O	Ready to send
		2	wifi0_uart_rts		O	WIFI UART output
		3	wifi1_uart_rts		O	WIFI UART output
		4	blsp_i2c0_sda(0)		I/O	I^2C0 sda
K1	GPIO12	0	GPIO	3.3		
		1	blsp_spi0_ss0_n(0)	1.8/3.0	O	SPI0 chip select 0
		2	blsp_i2c1_sck(0)		I/O	I^2C1 sck
K2	GPIO13	0	GPIO	3.3		
		1	blsp_spi0_miso(0)	1.8/3.0	I	SPI0 Master-in Slave-out data
		2	blsp_i2c1_sda(0)		I/O	I^2C1 sda
K3	GPIO14	0	GPIO	3.3		
		1	blsp_spi0_mosi(0)	1.8/3.0	O	SPI0 Master-out Slave-in data
L1	GPIO15	0	GPIO	3.3		
		1	blsp_spi0_sck(0)	1.8/3.0	O	SPI0 serial clock output
L2	GPIO16	0	GPIO	3.3		
		1	blsp_uart0_rxd(0)		I	Rx data
		2	led(0)			led_clk or led_dat or led_strobe
		–				
L3	GPIO17	0	GPIO	3.3		
		1	blsp_uart0_txd		O	Tx data
		2	led(1)			led_clk or led_dat or led_strobe
		–				
L4	GPIO18	0	GPIO	3.3		
		1	chi_irq_in		I	Chip interrupt input.

Table 2-15 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
		2	wifi0_uart_cts(1)		I	WIFI UART input
		3	wifi1_uart_cts(1)		I	WIFI UART input
M1	GPIO19	0	GPIO	3.3		
		1	chip_rst_out			Chip ouput reset signal
		2	wifi0_uart_rts		O	WIFI UART output
		3	wifi1_uart_rts		O	WIFI UART output
AD9	GPIO20	0	GPIO	3.3		
		1	blsp_i2c0_sck(1)		I/O	I^2C0 sck
		2	audio_rxmclk(0)	3.0	I/O	Master clock source of Audio I^2S/TDM Rx interface
AE8	GPIO21	0	GPIO	3.3		
		1	blsp_i2c0_sda(1)		I/O	I^2C0 sda
		2	audio_rxbclk(1)	3.0	I/O	Bit clock of Audio I^2S/TDM Rx interface
AE9	GPIO22	0	GPIO	3.3		
		1	sdio_cd	SDIO 1.8/3.0; eMMC: 1.8	I	SDIO card detect signal.
		2	rgmii_rxd(0)	1.5(2.0)/2.5(1.0)	I	RGMII Data input 0
		3	audio_rxfsync(1)	3.0	I/O	Left or Right indication of Audio I^2S Rx interface and frame start indication of Audio TDM Rx interface
AE10	GPIO23	0	GPIO	3.3		
		1	sdio_dat(0)	SDIO 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 0
		2	rgmii_rxd(1)	1.5(2.0)/2.5(1.0)	I	RGMII Data input 1
		3	audio_rxd(1)	3.0	I	Serial digital data of Audio Rx interface
AF8	GPIO24	0	GPIO	3.3		
		1	sdio_dat(1)	SDIO 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 1
		2	rgmii_rxd(2)	1.5(2.0)/2.5(1.0)	I	RGMII Data input 2
		3	audio_txmclk(0)	3.0	I/O	Master clock source of Audio I^2S/TDM Tx interface
AE12	GPIO25	0	GPIO	3.3		

Table 2-15 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
		1	sdio_dat(2)	SDIO 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 2
		2	rgmii_rxd(3)	1.5(2.0)/2.5(1.0)	I	RGMII Data input 3
		3	audio_txbclk(0)	3.0	I/O	Bit clock of Audio I^2S/TDM Tx interface
AE11	GPIO26	0	GPIO	3.3		
		1	sdio_dat(3)	SDIO 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 3
		2	rgmii_rx_ctl	1.5(2.0)/2.5(1.0)	I	RGMII Rx control
		3	audio_txfsync(0)	3.0	I/O	Left or Right indication of Audio I^2S Tx interface and frame start indication of Audio TDM Tx interface
AF9	GPIO27	0	GPIO	3.3		
		1	sdio_clk	SDIO 1.8/3.0; eMMC: 1.8	O	SDIO CLK
		2	rgmii_txc	1.5(2.0)/2.5(1.0)	O	RGMII Tx clock
		3	audio_td1	3.0	O	Serial digital data output 1 of Audio Multi-channel I^2S Tx interface and serial digital data of Audio TDM Tx interface
AG8	GPIO28	0	GPIO	3.3		
		1	sdio_cmd	SDIO 1.8/3.0; eMMC: 1.8	I/O	SDIO CMD
		2	rgmii_txd(0)	1.5(2.0)/2.5(1.0)	O	RGMII Tx Data 0
		3	audio_td2	3.0	O	Serial digital data output 2 of Audio Multi-channel I^2S Tx interface
AF11	GPIO29	0	GPIO	3.3		
		1	sdio_dat(4)	SDIO 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 4
		2	rgmii_txd(1)	1.5(2.0)/2.5(1.0)	O	RGMII Tx Data 1
		3	audio_td3	3.0	O	Serial digital data output 3 of Audio Multi-channel I^2S Tx interface
AF12	GPIO30	0	GPIO	3.3		
		1	sdio_dat(5)	SDIO 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 5
		2	rgmii_txd(2)	1.5(2.0)/2.5(1.0)	O	RGMII Tx Data 2

Table 2-15 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
		3	audio_pwm0	3.0	O	Audio Pulse Width Modulation interface 0
AF10	GPIO31	0	GPIO	3.3		
		1	sdio_dat(6)	SDIO 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 6
		2	rgmii_txd(3)	1.5(2.0)/2.5(1.0)	O	RGMII Tx Data 3
		3	audio_pwm1	3.0	O	Audio Pulse Width Modulation interface 1
AG9	GPIO32	0	GPIO	3.3		
		1	sdio_dat(7)	SDIO 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 7
		2	rgmii_rxc	1.5(2.0)/2.5(1.0)	I	RGMII Rx clock
		3	audio_pwm2	3.0	O	Audio Pulse Width Modulation interface 2
AG10	GPIO33	0	GPIO	3.3		
		1	rgmii_tx_ctl	1.5(2.0)/2.5(1.0)	O	RGMII Tx control
		2	audio_pwm3	3.0	O	Audio Pulse Width Modulation interface 3
AG11	GPIO34	0	GPIO	3.3		
		1	blsp_i2c1_sck(1)		I/O	I^2C1 sck
		2	audio_spdifin(0)	3.0	I	Audio SPDIF input
AG12	GPIO35	0	GPIO	3.3		
		1	blsp_i2c1_sda(1)		I/O	I^2C1 sda
		2	audio_spdifout	3.0 (confirm standard I/O voltage)	O	Audio SPDIF output
AB24	GPIO36	0	GPIO	3.3		
		1	rmii0_txd(0)	3.0	O	RMII0 Tx data 0
		2	led(2)			led_clk or led_dat or led_strobe
		3	led(0)			led_clk or led_dat or led_strobe
AB25	GPIO37	0	GPIO	3.3		
		1	rmii0_txd(1)	3.0	O	RMII0 Tx data 1
		2	wifi0_wci_out		O	WIFI0 LTE Coex output
		3	wifi1_wci_out		O	WIFI1 LTE Coex output

Table 2-15 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
		4	led(1)			led_clk or led_dat or led_strobe
AB26	GPIO38	0	GPIO	3.3		
		1	rmii0_tx_en	3.0	O	RMII0 Tx enable
		2	led(2)			led_clk or led_dat or led_strobe
AB27	GPIO39	0	GPIO	3.3		
		1	rmii0_rx_er	3.0	I/O	RMII Rx error when master mode; RMII Tx error when slave mode
		2	pcie_clk_req_n(0)			PCIe clock request (only use input mode)
		3	led(3)			led_clk or led_dat or led_strobe
AA25	GPIO40	0	GPIO	3.3		
		1	rmii0_refclk	3.0	I/O	Input reference clock when Slave mode. Output clock when master mode
		2	wifi0_rfsilient_bb(0)		I	WIFI0 RF silent signal (RF_kill)
		3	wifi1_rfsilient_bb(0)		I	WIFI1 RF silent signal (RF_Kill)
		–				
		5	led(4)			led_clk or led_dat or led_strobe
AA26	GPIO41	0	GPIO	3.3		
		1	rmii0_rxd(0)	3.0	I	RMII0 Rx data 0
		2	wifi0_cal_xpa_active		O	WIFI0 XPA control signal used for test purpose
		3	wifi1_cal_xpa_active		O	WIFI1 XPA control signal used for test purpose
		–				
AA27	GPIO42	0	GPIO	3.3		
		1	rmii0_rxd(1)	3.0	I	RMII0 Rx data 1
		2	wifi_wci_in(0)		I	WIFI LTE Coex input
Y25	GPIO43	0	GPIO	3.3		
		1	rmii0_dv	3.0	I	RMII0 Rx valid
		2	wifi_wci_in(1)		I	WIFI LTE Coex input

Table 2-15 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
Y26	GPIO44	0	GPIO	3.3		
		1	rmii1_refclk	3.0	I/O	Input reference clock when Slave mode. Output clock when master mode
		2	blsp_spi1_sck	1.8/3.0	O	SPI1 serial clock
		3	smart_ant4(0)		I/O	wifi_2g TXPCU_ ANTENNA_INFO[0] (from MAC) wifi_2g serial clock for smart antenna (serial mode)
Y27	GPIO45	0	GPIO	3.3		
		1	rmii1_rxd(0)	3.0	I	RMII1 Rx data 0
		2	blsp_spi1_ss0_n	1.8/3.0	O	SPI1 chip select 0
		3	blsp_spi0_ss1_n	1.8/3.0	O	SPI0 chip select 1
		4	smart_ant5(0)		I/O	wifi_2g TXPCU_ ANTENNA_INFO[1] (from MAC) wifi_2g serial Data for smart antenna (serial mode)
		5	led(6)			led_clk or led_dat or led_strobe
W24	GPIO46	0	GPIO	3.3		
		1	rmii1_rxd(1)	3.0	I	RMII1 Rx data 1
		2	blsp_spi1_mosi	1.8/3.0	O	SPI1 Master-out Slave-in data
		3	smart_ant6(0)		I/O	wifi_5g TXPCU_ ANTENNA_INFO[0] (from MAC) wifi_5g serial clock for smart antenna (serial mode)
		4	led(7)			led_clk or led_dat or led_strobe
W25	GPIO47	0	GPIO	3.3		
		1	rmii1_dv	3.0	I	RMII1 Rx valid
		2	blsp_spi1_miso	1.8V/3.0	I	SPI1 Master-in Slave-out data

Table 2-15 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
		3	smart_ant7(0)		I/O	wifi_5g TXPCU_ ANTENNA_INFO[1] (from MAC) wifi_5g serial Data for smart antenna (serial mode)
		4	led(8)			led_clk or led_dat or led_strobe
W26	GPIO48	0	GPIO	3.3		
		1	rmii1_tx_en	3.0	O	RMII1 Tx enable
		2	aud_pin_pcm_dtx	3.3	O	Transmitted data of Audio PCM interface
		–				
		4	led(9)			led_clk or led_dat or led_strobe
W27	GPIO49	0	GPIO	3.3		
		1	rmii1_rx_er	3.0	I/O	RMII Rx error when master mode; RMII Tx error when slave mode
		2	aud_pin_pcm_drx		I	Received data of Audio PCM interface
		–				
		4	led(10)			led_clk or led_dat or led_strobe
V24	GPIO50	0	GPIO	3.3		
		1	rmii1_txd(0)	3.0	O	RMII1 Tx data 0
		2	aud_pin_pcm_pclk		O	Clock of Audio PCM interface
		3	wifi0_rfsilient_bb(1)		I	WIFI0 RF siient signal (RF_Kill)
		4	wifi1_rfsilient_bb(1)		I	WIFI1 RF silent signal
		5	led(11)			led_clk or led_dat or led_strobe
V25	GPIO51	0	GPIO	3.3		
		1	rmii1_txd(1)	3.0	O	RMII1 Tx data 1
		2	aud_pin_pcm_fsync			Frame start indication of Audio PCM interface
		3	wifi0_cal_xpa_active			Wi-Fi 0 XPA control signal used for test purposes
		4	wifi1_cal_xpa_active			Wi-Fi 1 XPA control signal used for test purposes

Table 2-15 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
V26	GPIO52	0	GPIO	3.3		
		2	MDC	3.3	O	Management Data Clock
		3	pcie_clk_req_n(1)	3.3		PCIe clock request(only use input mode)
		4	audio_txmclk(1)	3.0	I/O	Master clock source of Audio I^{2}S/TDM Tx interface
			boot_config(13)			
V27	GPIO53	0	GPIO	3.3		
		1	qpic_pad_busy_n		I	nandc busy_not_ready input. Active low.
		2	MDIO	3.3	I/O	Management Data I/O
		3	audio_txbclk(1)	3.3	I/O	Bit clock of Audio I^{2}S/TDM Tx interface
U24	GPIO54	0	GPIO	3.3		
		1	qpic_pad_lcd_rs_n		O	lcdc RESX, reset signal. Active low.
		2	blsp_spi0_ss0_n(1)	3.3	O	SPI0 chipselect 0
		3	audio_td1	3.3	O	Serial digital data output 1 of Audio Multi-channel I^{2}S Tx interface and serial digital data of Audio TDM Tx interface
U25	GPIO55	0	GPIO	3.3		
		1	qpic_pad_we_n		O	nandc/lcdc write enable
		2	blsp_spi0_mosi(1)	3.3	O	SPI0 Master-out Slave-in data
		3	audio_td2	3.3	O	Serial digital data output 2 of Audio Multi-channel I^{2}S Tx interface and serial digital data of Audio TDM Tx interface
			boot_config(9)	3.3	I	
U26	GPIO56	0	GPIO	3.3		
		1	qpic_pad_oe_n		O	nandc/lcdc read enable
		2	blsp_spi0_sck(1)		O	SPI0 serial clock
		3	audio_td3	3.3	O	Serial digital data output 3 of Audio Multi-channel I^{2}S Tx interface
			boot_config(10)	3.3	I	

Table 2-15 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
U27	GPIO57	0	GPIO	3.3		
		1	qpic_pad_dat(4)		O	nandc/lcdc data
		2	blsp_spi0_miso(1)		I	SPI0 Master-in Slave-out data
		3	audio_txfsync(1)	3.3	I/O	Left or Right indication of Audio I^{2}S Tx interface and frame start indication of Audio TDM Tx interface
T25	GPIO58	0	GPIO	3.3		
		1	qpic_pad_dat(5)		O	nandc/lcdc data
		2	LED[2]	3.3	O	
		3	blsp_i2c0_sck(2)	3.3	IO	I^{2}C serial clock
		–				
		5	smart_ant6	3.3	IO	Smart antenna
		6	audio_rxmclk(1)	3.3	I/O	Master clock source of Audio I^{2}S/TDM Rx interface
T26	GPIO59	0	GPIO	3.3		
		1	qpic_pad_dat(6)		O	nandc/lcdc data
		2	blsp_i2c0_sda(2)	3.3	IO	I^{2}C serial data
		–				
		4	smart_ant7	3.3	IO	Smart antenna
		5	audio_spdifin(1)	3.3	O	Audio SPDIF input
T27	GPIO60	0	GPIO	3.3		
		1	qpic_pad_dat(7)		O	nandc/lcdc data
		2	blsp_uart0_rxd(1)	3.3	I	UART receive data
		–				
		4	smart_ant4	3.3	IO	Smart antenna
		5	LED[0]	3.3	O	
		6	audio_txbclk	3.3	IO	Audio transmit bit clock
		7	audio_rxbclk	3.3	IO	Audio receive bit clock

Table 2-15 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
P27	GPIO61	0	GPIO	3.3		
		1	qpic_pad_lcd_cs_n		O	lcdc chip select
		2	blsp_uart0_txd	3.3	O	UART transmit data
		–				
		4	smart_ant5	3.3	IO	Smart antenna
		5	audio_txfsync	3.3	IO	Audio transmit frame sync
		6	audio_rxfsync	3.3	IO	Audio receiver frame sync
		7	LED[1]	3.3	O	
			boot_config(14)	3.3	I	
N24	GPIO62	0	GPIO	3.3		
		1	qpic_pad_cle_lb_n		O	nandc CLE/lcdc DCX. CLE is commend latch enable. Active high. DCX is data/command. 1 is data, 0 is command.
		2	Chip_rst_out	3.3	O	Chip reset signal
		3	Wifi0_uart_txd	3.3	O	Wifi0 UART transmit data
		4	Wifi1_uart_txd	3.3	O	Wifi1 UART transmit data
		5	audio_spdifout	3.3	O	Audio SPDIF output
			boot_config(11)	3.3	I	
N25	GPIO63	0	GPIO	3.3		
		1	qpic_pad_nand_cs_n		O	nandc chip select
		2	Wifi0_uart_rxd	3.3	I	Wifi0 UART receive data
		3	Wifi1_uart_rxd	3.3	I	Wifi1 UART receive data
		4	Wifi1_uart_txd	3.3	I	Wifi1 UART transmit data
		5	Audio_txd[1]	3.3	O	Audio transmit data
		6	Audio_rxd	3.3	I	Audio receive data
		7	Audio_spdifout	3.3	O	Audio spdifout
		8	Audio_spdifin	3.3	I	Audio spdifin
R25	GPIO64	0	GPIO	3.3		
		1	qpic_pad_dat(1)		O	nandc/lcdc data
		2	audio_pwm0	3.3		Audio Pulse Width Modulation interface 0
R26	GPIO65	0	GPIO	3.3		

Table 2-15 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
		1	qpic_pad_dat(2)		O	nandc/lcdc data
		2	audio_pwm1	3.3		Audio Pulse Width Modulation interface 1
R27	GPIO66	0	GPIO	3.3		
		1	qpic_pad_dat(3)		O	nandc/lcdc data
		2	audio_pwm2	3.3		Audio Pulse Width Modulation interface 2
P24	GPIO67	0	GPIO	3.3		
		1	qpic_pad_dat(0)		O	nandc/lcdc data
		2	audio_pwm3	3.3		Audio Pulse Width Modulation interface 3
P25	GPIO68	0	GPIO	3.3		
		1	qpic_pad_dat(8)		O	nandc/lcdc data
		2	dbg_bus_out(12)			Dakota IP debug bus
P26	GPIO69	0	GPIO	3.3		
		1	qpic_pad_ale_lb_n		O	nandc ALE. Active high.

1. Can also be activated by boot configuration.

2.3.10 Boot configuration

Several GPIO signals can be used to configure the secure boot feature and boot device. They are sampled only during power-on reset. Table 2-16 shows the boot configuration signals.

Table 2-16 Boot configuration

Pin	Pin name Boot_CONFIG[n]	Alternate function	Type	Function description	
U26	10	GPIO56	I	Mode	
				0	Native mode
				1	Test mode
A18	0	GPIO3	I	Apps authentication Enable. Enables authentication for various AP code segments. Send to security control	
				0	No authentication
				1	Enable authentication
K3	1	GPIO14	I	GPIO51 (high order):GPIO14 (low order)	
V25	7	GPIO51		00	Boot interface is SPI
				01	Boot interface is EMMC
				10	Boot interface is QPIC

Table 2-16 Boot configuration (cont.)

Pin	Pin name Boot_CONFIG[n]	Alternate function	Type	Function description	
				11	Boot from USB
AB24	3	GPIO36	I	0	Boot from code RAM
				1	Boot from ROM
N24	11	GPIO62	I	JTAG enable	
				0	GPIO0~GPIO5 are normal GPIO. Can be configured by the FUN_SEL registers
				1	GPIO0~GPIO5 are used as JTAG interface. Cannot be changed by the FUN_SEL registers
AB25	4	GPIO37	I	APPS PBL boot speed (APSS PLL)	
AB26	5	GPIO38		GPIO38 (high order):GPIO37 (low order)	
				00	XO clock - 48MHz
				01	FE_PLL clock - 200MHz
				10	FE_PLL clock - 500MHz
				11	Reserved
P26	12	GPIO69	I	Select ROM PK hash index source	
				0	From QC EFUSE
				1	From OEM EFUSE
U25	9	GPIO55	I	0	Normal boot
				1	Force boot from USB
AG10	2	GPIO33	I	Use Serial Number for secure boot authentication	
				0	Use Serial Number
				1	Use OEM ID
L1	6	GPIO15	I	Watchdog enable	
				0	Watchdog disable
				1	Watchdog enable

3 Electrical Specifications

3.1 Absolute maximum ratings

Operating the IPQ4019 under conditions beyond its absolute maximum ratings (listed in Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, are not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
T_J	Junction temperature	–	125	°C
T_{store}	Storage temperature	-45	135	°C

3.2 Recommended operating conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage, ambient temperature, and case temperature. The IPQ4019 meets all performance specifications when used within the recommended operating conditions (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Recommended operating temperatures

Temperature	Description	Min	Typ	Max	Unit
Operating temperature (commercial)	Case temperature	0	–	110	°C

Table 3-3 Recommended operating voltages

Pin	Description	Min	Typ[1]	Max	Unit
General					
AVDD11		1.05	1.1	1.15	V
VDD11		1.05	1.1	1.15	V
AVDD11_LDO		1.08	1.1	1.12	V
VDD135		1.28	1.35	1.42	V
DDR_VDDQ		1.28	1.35	1.42	V
AVDD33		3.13	3.3	3.46	V
VDDIO		3.13	3.3	3.46	V
VTT_LDO		0.5 * VDD135 ± 40			mV
DDR_Vref		0.5 * VDD135 ± 20			mV
5 GHz Radio					
VDD11_ADDAC_R1	1.1 V power supply for Radio 1	1.05	1.1	1.15	V
VDD11_BB_R1		1.05	1.1	1.15	V
VDD11_BIAS_R1		1.05	1.1	1.15	V
VDD11_LO_R1		1.05	1.1	1.15	V
VDD11_RX_CH2		1.05	1.1	1.15	V
VDD11_RX_CH3		1.05	1.1	1.15	V
VDD11_TX_CH2		1.05	1.1	1.15	V
VDD11_TX_CH3		1.05	1.1	1.15	V
VDD33_BBPLL_R1	3.3 V power supply for Radio 1	3.13	3.3	3.46	V
VDD33_BB_R1		3.13	3.3	3.46	V
VDD33_SYN_R1		3.13	3.3	3.46	V
VDD33_VCO_R1		3.13	3.3	3.46	V
2.4 GHz Radio					
VDD11_ADDAC_R0	1.1 V power supply for Radio 0	1.05	1.1	1.15	V
VDD11_BB_R0		1.05	1.1	1.15	V
VDD11_BIAS_R0		1.05	1.1	1.15	V
VDD11_CLKBUF_R0		1.05	1.1	1.15	V
VDD11_LO_R0		1.05	1.1	1.15	V
VDD11_RX_CH0		1.05	1.1	1.15	V
VDD11_RX_CH1		1.05	1.1	1.15	V
VDD11_TX_CH0		1.05	1.1	1.15	V
VDD11_TX_CH1		1.05	1.1	1.15	V

Table 3-3 Recommended operating voltages (cont.)

Pin	Description	Min	Typ[1]	Max	Unit
VDD33_BBPLL_R0	3.3 V power supply for Radio 0	3.13	3.3	3.46	V
VDD33_BB_R0		3.13	3.3	3.46	V
VDD33_SYN_R0		3.13	3.3	3.46	V
VDD33_VCO_R0		3.13	3.3	3.46	V

1. Typical voltages are voltages at the pins of the package.

3.2.1 Crystal

A 48-MHz crystal with accuracy of ±20 ppm may be used; for 5 MHz operation, ±10 ppm is required.

Table 3-4 Reference requirements for 48 MHz crystal

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	—	—	48	—	MHz
Frequency trimming	—	-10	—	10	PPM
Duty cycle of output signal	—	48	—	52	%
Voltage swing	—	0.8	—	1.5	Vpp
Settling time	—	—	—	1	ms
Output phase noise (48 MHz)	*f* = 1 KHz	—	-123.5	-121.5	dBc/Hz
	f = 10 KHz	—	-145.5	-143.5	dBc/Hz
	f = 100 KHz	—	-156.5	-154.5	dBc/Hz
	f = 1000 KHz	—	-157.5	-155.5	dBc/Hz
Output harmonic spur	—	—	—	-40	dBc
Mode of vibration	—	Fundamental			

3.3 Power sequencing

Power is supplied by external voltage regulators, which should be configured for the power-up sequence shown in Table 3-5. Any other supplies that are not critical to this power-up sequence, can be powered on by software after this sequence is completed.

Table 3-5 Power-on sequence

Step	Rails grouped by regulator	Voltage	Comments
1	AVDD33	3.3	3.3 V analog power
	VDDIO33		Power for GPIO
	VDD33_BBPLL_R1, VDD33_BB_R1, VDD33_SYN_R1, VDD33_VCO_R1		3.3 V power supply for Radio 1
	VDD33_BBPLL_R0, VDD33_BB_R0, VDD33_SYN_R0, VDD33_VCO_R0		3.3 V power supply for Radio 0
2	VDD135	1.35	Power input for the VDD11 LDO and VTT LDO. Route a dedicated wire from the 1.35 V switching regulator.
	VDDQ		DDR I/O power
3	AVDD11	1.1	1.1 V analog power
	AVDD11_LDO		1.1 V analog power. Connect with pin A24 on board.
	VDD		Digital power
	VDD11_LDO		1.1 V LDO output
	VDD11_ADDAC_R1, VDD11_BB_R1, VDD11_BIAS_R1, VDD11_LO_R1, VDD11_RX_CH2, VDD11_RX_CH3, VDD11_TX_CH2, VDD11_TX_CH3		1.1 V power supply for Radio 1
	VDD11_ADDAC_R0, VDD11_BB_R0, VDD11_BIAS_R0, VDD11_CLKBUF_R0, VDD11_LO_R0, VDD11_RX_CH0, VDD11_RX_CH1, VDD11_TX_CH0, VDD11_TX_CH1		1.1 V power supply for Radio 0

NOTE Within each step, no requirement for rail sequence.

3.4 Digital characteristics

Table 3-6 Digital I/O characteristics for 3.3 V IO

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage	CMOS/Schmitt	2	3.6	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.4	V
V_{SHYS}	Schmitt hysteresis voltage		–	–	mV
I_{IH}	Input high leakage current [1, 2]	No pulldown	–	1	µA
I_{IL}	Input low leakage current [1, 2]	No pullup	-1	–	µA
I_{IHPD}	Input high leakage current [1, 3]	With pulldown	10	60	µA
I_{ILPU}	Input low leakage current [2, 3]	With pullup	-60	-10	µA
V_{OH}	High-level output voltage [4]	CMOS, at pin-rated drive strength	3.0	3.6	V
V_{OL}	Low-level output voltage [4]	CMOS, at pin-rated drive strength	-0.3	0.4	V
I_{OZH}	Tri-state leakage current [1]	Logic high output, no pulldown	–	1	µA
I_{OZL}	Tri-state leakage current [2]	Logic low output, no pullup	-1	–	µA
I_{OZHPD}	Tri-state leakage current [1, 3]	Logic high output with pulldown	10	60	µA
I_{OZLPU}	Tri-state leakage current [2, 3]	Logic low output with pullup	-60	-10	µA
C_{IN}	Input capacitance [5]		–	5	pF

1. Pin voltage = VDDIO max. For keeper pins, pin voltage = VDDIO max - 0.45 V.
2. Pin voltage = GND and supply = VDDIO max. For keeper pins, pin voltage = 0.45 V and supply = VIO max.
3. Refer to Table 2-1 for pullup, pulldown, and keeper details.
4. Refer to Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage.
5. Input capacitance is guaranteed by design, but is not 100% tested.

Table 3-7 Digital I/O characteristics for DDR3 PAD

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage [1]	CMOS	1.05	1.65	V
V_{IL}	Low-level input voltage [1]	CMOS	-0.2	0.2	V
I_{IH}	Input high leakage current [2]	No pulldown	–	1	µA
I_{IL}	Input low leakage current [3]	No pullup	-1	–	µA
I_{IHPD}	Input high leakage current [2, 4]	With pulldown	5	30	µA
I_{ILPU}	Input low leakage current [3, 4]	With pullup	-30	-5	µA
V_{OH}	High-level output voltage [5]	CMOS, at pin rated drive strength	1.2	1.5	V
V_{OL}	Low-level output voltage [5]	CMOS, at pin rated drive strength	-0.2	0.2	V
I_{OZH}	Tri-state leakage current	Logic high output	–	1	µA
I_{OZL}	Tri-state leakage current	Logic low output	-1	–	µA
C_{IN}	Input capacitance [6]		1	2	pF
$C_{I/O}$	I/O capacitance [6]	I/O, DQS, DQ, or clock pins	1.25	2.5	pF

1. V_{ref} = DDR_VDDQ.
2. Pin voltage = DDR_VDDQ max.
3. Pin voltage = GND and supply = DDR_VDDQ max.
4. Refer to Table 2-1 for pullup, pulldown, and keeper details.
5. Refer to Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage.
6. Input and I/O capacitances are guaranteed by design, but are not 100% tested.

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (see Figure 3-1) with respect to the drive current (see Table 2-1). They can be calculated using these relationships:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = Vdd\_px - \left(\frac{\%drive \times 450}{100}\right) mV$$

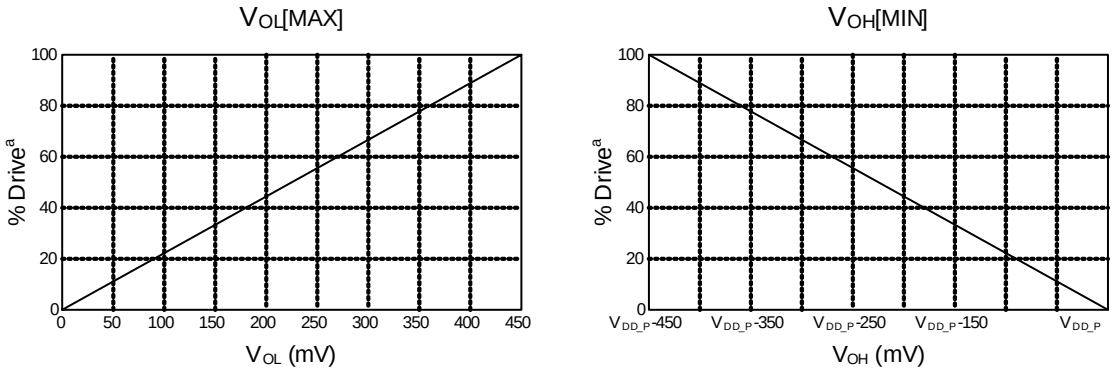


Figure 3-1 IV curve for V_{OL} and V_{OH} (valid for all V_{DD_PX})

3.5 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics are included here.

NOTE All IPQ4019 devices are characterized with actively terminated loads, so all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.5.2.

3.5.1 Timing diagram conventions

The conventions used throughout this document for timing diagrams are shown in Figure 3-2. For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown, the meaning depends on the signal.
- A single signal indicates *don't care*.
- In the case of bus activity, if both high and low levels are shown, this indicates that the processor or external interface is driving a value, but that this value may or may not be valid.

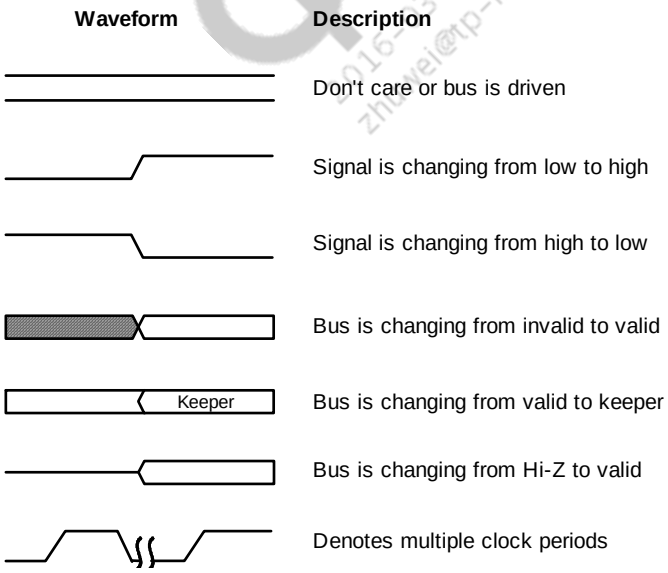


Figure 3-2 Timing diagram conventions

3.5.2 Rise and fall time specifications

The testers that characterize IPQ4019 have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-3.

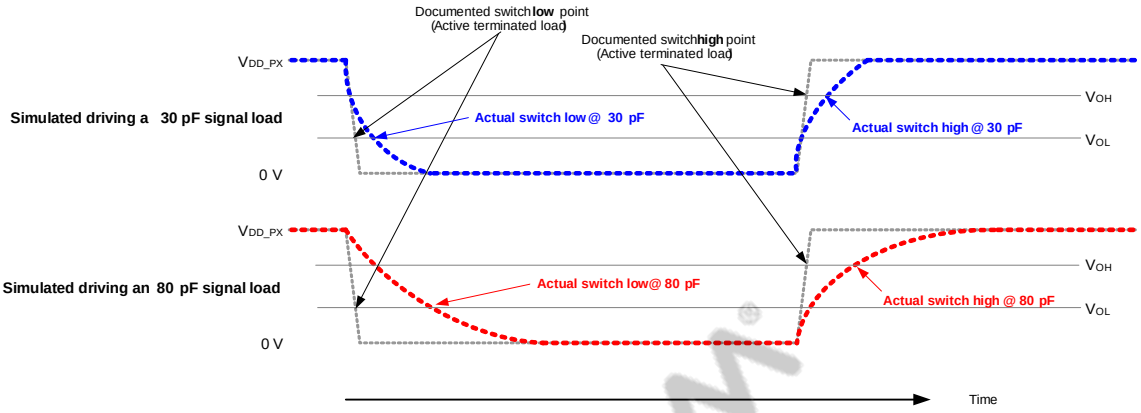


Figure 3-3 Rise and fall times under different load conditions

3.6 Memory support

3.6.1 DDR

All timing parameters in this document assume no bus loading. Rise/fall times must be factored into the numbers in this document. For example, setup times may get worse and hold times may get better.

Table 3-8 Summary of DDR support

Applicable standard	Feature exceptions	IPQ4019 variations
DDR3 SDRAM Specification JESD79-3A September 2007	None	None

3.6.1.1 Differential input cross point voltage

Make sure each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) meet the requirements in Table 3-9. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

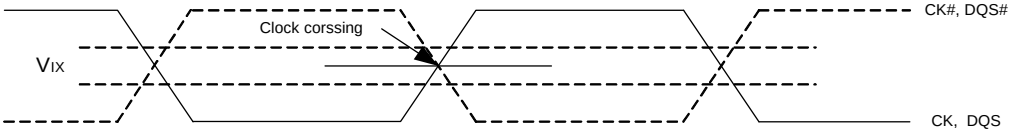


Figure 3-4 V_{IX} definition

Table 3-9 Cross point voltage for differential input signals (CK, DQS)

Parameter		Min	Typ	Max	Unit
1/t(ck)	PCDDR3L clock frequency	–	667	–	MHz
V_{IX}	Differential input cross-point voltage relative to VDD/2 for CK, CK#	-0.15		0.15	V

3.6.2 EBI2 NAND interface

Each access to the NAND flash device involving the controller executes a sequence of signal assertion and de-assertion. The state-machine registers are designed to allow up to seven distinct configurations, including wait states.

The register settings dictate the signal status once the state-machine is started. For example, CMD_CLE_EN (FLASH_XFR_STEPx[22]) values in the step controls the CLE pin state (1: high, 0: low). If the controller must send a multiple command sequence, it may not need to do all the steps. It can start from the beginning of the sequence and, after sending the command, it can loop back and send the next command without finishing the sequence.

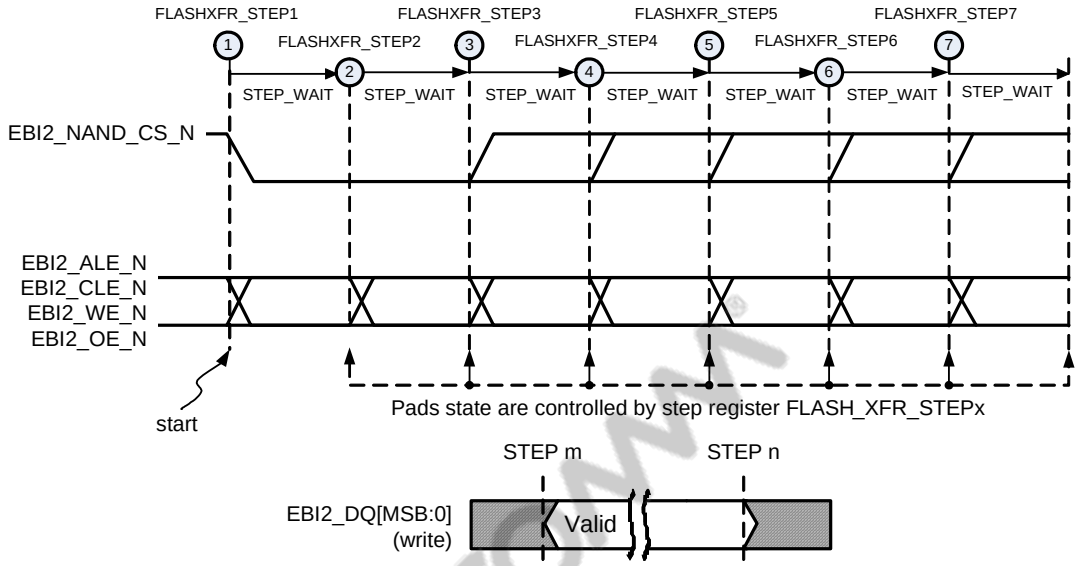
FLASH_XFR_STEPx[31:30] – CMD_SEQ_STEP_NUMBER and
FLASH_XFR_STEPx[15:14] – DATA_SEQ_STEP_NUMBER defines the step number in the command/data sequence:

00 => Simple step
01 => Loop start
10 => Loop end
11 => Last step

If a value of “11” is programmed to the SEQ_STEP_NUMBER register, it indicates the step is the last step in the sequence and the controller will end the sequence after finishing the step. The timing parameters in Table 3-10 use a four-step configuration as an example. If the step configuration is changed, the timing parameters that mapped to the registers should be adjusted accordingly. In step configuration registers (FLASH_XFR_STEPx), the upper 16 bits [31:16] configure the NAND *command* and *address* cycles, whereas the lower 16 bits [15:0] configure the *data* read and write cycles.

Table 3-10 NAND timing parameters

Parameter	Description
T	EBI2 CLK cycle, usually 10 ns, depending on GCC configuration of QPIC CORE CLOCK; timing parameters are based upon a 4-step configuration FLASH_XFR_STEP1 to FLASH_XFR_STEP4.
a	FLASH_XFR_STEP1[29:26] + 1
b	FLASH_XFR_STEP2[29:26] + 1
c	FLASH_XFR_STE[29:26] + 1
d	FLASH_XFR_STEP4[29:26] + 1
e	FLASH_XFR_STEP1[13:10] + 1
f	FLASH_XFR_STEP2[13:10] + 1
g	FLASH_XFR_STE[13:10] + 1
h	FLASH_XFR_STEP4[13:10] + 1
i	NAND_DEVn_CFG1[4:2]+1
k	FLASH_XFR_STEP2[13:10] + FLASH_XFR_STEP2[1:0] + 1
m	FLASH_XFR_STE[13:10] + FLASH_XFR_STE[1:0] + 1
n	(NAND_DEVn_CFG[22:17] + 1) × 2



FLASH_XFR_STEPx (x = 1 to 7)			* Not used
Command/Address		**Data**	
31:30	CMD_SEQ_SETP_NUM	15:14	DATA_SEQ_STEP_NUMBER
29:26	CMD_STEP1_WAIT	13:10	DATA_STEP1_WAIT
25	CMD_AOUT_EN*	9	DATA_AOUT_EN*
24	CMD_DATA_EN	8	DATA_DATA_EN
23	CMD_CE_EN	7	DATA_CE_EN
22	CMD_CLE_EN	6	DATA_CLE_EN
21	CMD_ALE_PIN	5	DATA_ALE_PIN
20	CMD_WE_EN	4	DATA_WE_EN
19	CMD_RE_EN	3	DATA_RE_EN
18	CMD_WIDE	2	DATA_WIDE
17:16	RESERVED*	1:0	EXTA_READ_WAIT

Figure 3-5 NAND state machine registers

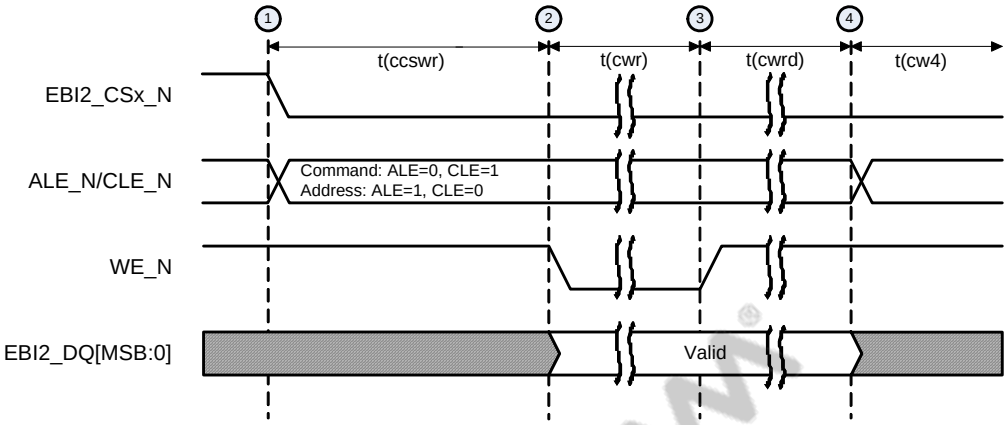
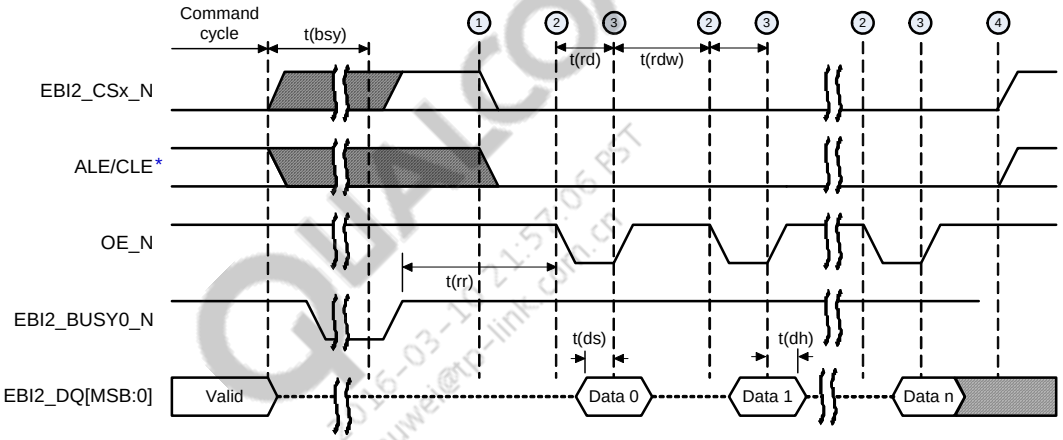


Figure 3-6 NAND command and address cycles



* During data read wait period, ALE and CLE stay low only if EBI2_CSx_N is driven low as required by the FLASH device.

Figure 3-7 NAND data write

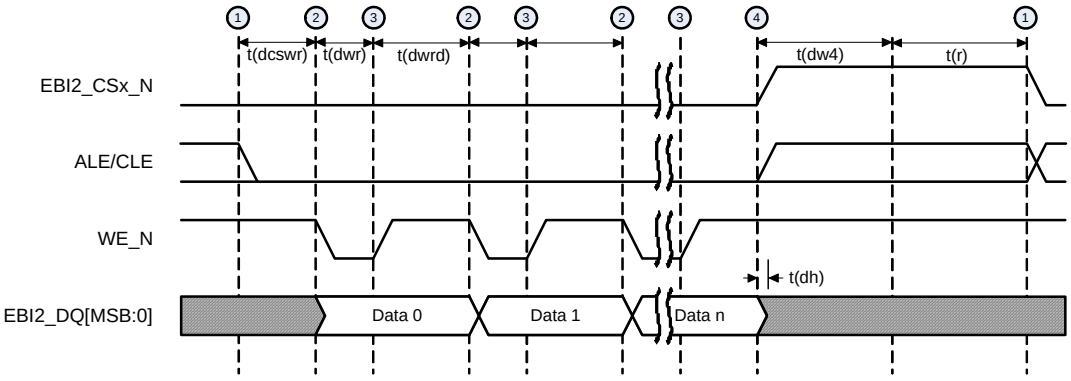


Figure 3-8 NAND data read

Table 3-11 NAND timing – AC characteristics [1]

Parameter		Comments	Min	Max	Unit
Command/address cycles					
t(ccswr)	Chip-select active to write active		aT-5	–	ns
t(cwr)	WE_N active time		bT-5	–	ns
t(cwrd)	Data hold time		cT-5	–	ns
t(cw4)	Wait cycle		dT-5	–	ns
Data cycles					
t(dcswr)	Chip-select active to write active		eT-5	–	ns
t(dwr)	WE_N active time		fT-5	–	ns
t(dwrd)	Write-data hold time		gT-5	–	ns
t(dw4)	Wait cycle		hT-5	–	ns
t(r)	Recovery cycles		iT-5	–	ns
t(rr)	Busy to read delay		3T	–	ns
t(rd)	OE_N active time		kT-5	–	ns
t(rdw)	Read wait cycle		mT-5	–	ns
t(bsy)	Busy detect delay		nT-5	–	ns
t(ds)	Read-data setup time		15	–	ns
t(dh)	Read-data hold time		0	–	ns

1. Variables ‘a’ through ‘n’ are defined in Table 3-10.

3.6.3 eMMC NAND flash on SDIO

Both eMMC NAND flash and SD card can be supported via the SDIO ports.

3.7 Connectivity

The connectivity functions supported by the IPQ4019 include:

- USB 3.0 and USB 2.0 ports
- Universal asynchronous receiver transmitter (UART) serial ports
- Secure digital card controller (SDCC) ports
- Inter-integrated circuit (I^2C) interfaces for peripheral devices
- Multichannel I^2S and TDM interfaces for digital audio support
- Serial peripheral interface (SPI) ports
- Media-independent interface PSGMII

Pertinent specifications for these functions — where appropriate — are stated in the following subsections.

In addition to the following hardware specifications, consult the latest software release notes for software-based performance features or limitations.

3.7.1 USB interfaces

Table 3-12 Summary of USB support

Applicable standard	Feature exceptions	IPQ4019 variations
Universal Serial Bus Specification, Revision 3.0	None	None
Universal Serial Bus Specification, Revision 2.0	None	For operating voltages, system clock, and VBUS – see Table 3-3

3.7.2 High-speed UART interface

Table 3-13 Summary of UART support

Applicable standard	Feature exceptions	IPQ4019 variations
EIA RS232-C	None	None

3.7.3 Secure digital card controller interface

Table 3-14 Summary of SDCC support

Applicable standard	Feature exceptions	IPQ4019 variations
MultiMediaCard Host Specification version 4.4.1 and 4.5	None	Timing specifications – see Figure 3-9 and Figure 3-10
Secure Digital: Physical Layer Specification version 3.0	None	

Double Data Rate - DDR

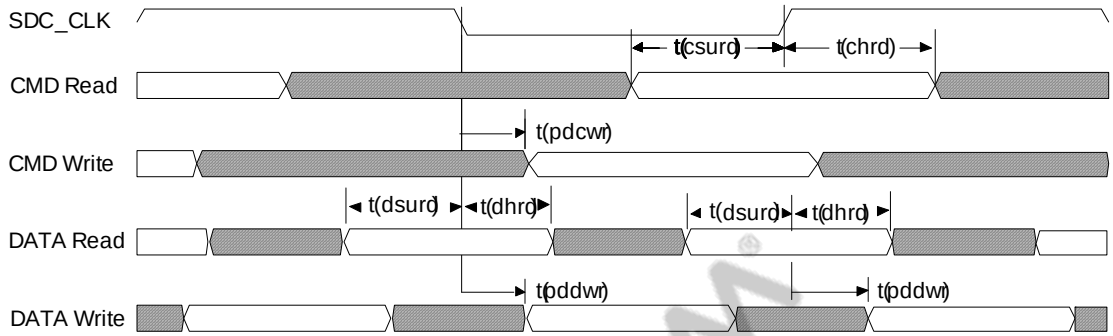


Figure 3-9 SDCC SDR timing waveforms

Single Data Rate - SDR

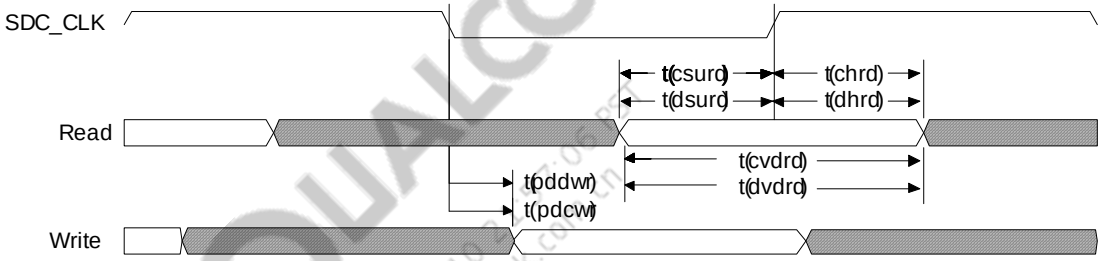


Figure 3-10 SDCC DDR timing waveforms

Table 3-15 SDC1 DDR mode timing parameters [1]

Parameter		Min	Max	Unit
t(chrd)	Command hold	1.5	–	ns
t(csurd)	Command setup	5.8	–	ns
t(dhrd)	Data hold	1.5	–	ns
t(dsurd)	Data setup	2.5	–	ns
t(pddwr)	Propagation delay on data write	-2.75	3.25	ns
t(pdcwr)	Propagation delay on command write	-2.75	3.25	ns

1. SDC1 DDR mode timing parameters are for clock frequencies up to 48 MHz.

Table 3-16 SDC1 SDR mode timing parameters [1]

Parameter		Min	Max	Unit
t(chrd)	Command hold	1.5	–	ns
t(csurd)	Command setup	2.0	–	ns
t(dhrd)	Data hold	1.5	–	ns
t(dsurd)	Data setup	2.0	–	ns
t(pddwr)	Propagation delay on data write	-1.05	1.65	ns
t(pdcwr)	Propagation delay on command write	-1.05	1.65	ns

1. SDC1 SDR timing parameters are for clock frequencies up to 96 MHz.

Table 3-17 SDC1 SDR104 mode timing parameters [1]

Parameter		Min	Max	Unit
t(cvdrd)	Command valid	3.12	–	ns
t(dvdrd)	Data valid	3.12	–	ns
t(pddwr)	Propagation delay on data write	-1.05	1.65	ns
t(pdcwr)	Propagation delay on command write	-1.05	1.65	ns

1. SDC1 SDR104 mode timing parameters are for clock frequencies up to 192 MHz.

3.7.4 I²C interface

Table 3-18 Summary of I²C support

Feature exceptions	IPQ4019 variations
■ High-speed mode (3.4 Mbps) is not supported. ■ 10-bit addressing is not supported. ■ Fast mode plus (1 Mbps) is not supported.	None

3.7.5 I²S interface

The IPQ4019 supports multichannel I²S. The I²S interface meet the timing given in this section.

Table 3-19 Supported I²S standards and exceptions

Applicable standard	Feature exceptions	IPQ4019 variations
Philips Semiconductor, *I²S Bus Specification*, revised June 5, 1996		The IPQ4019 meets or exceeds this standard. The only exception is the IPQ4019 requires a 45/55 duty cycle when the SCK clock source is from an external source.

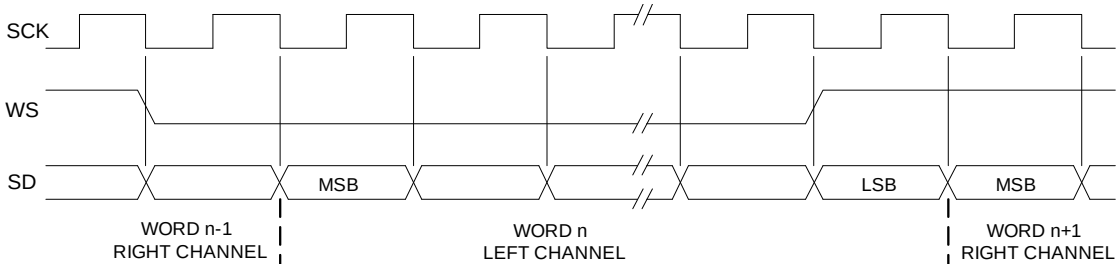


Figure 3-11 I²S interface basic timing

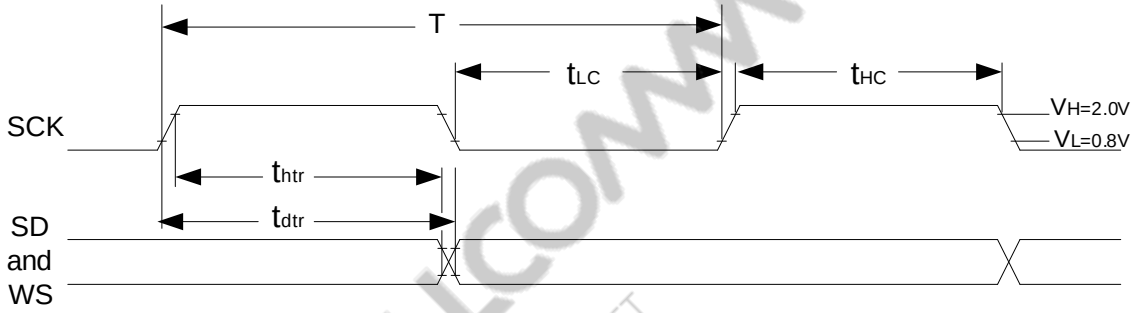


Figure 3-12 I²S interface transmitter timing

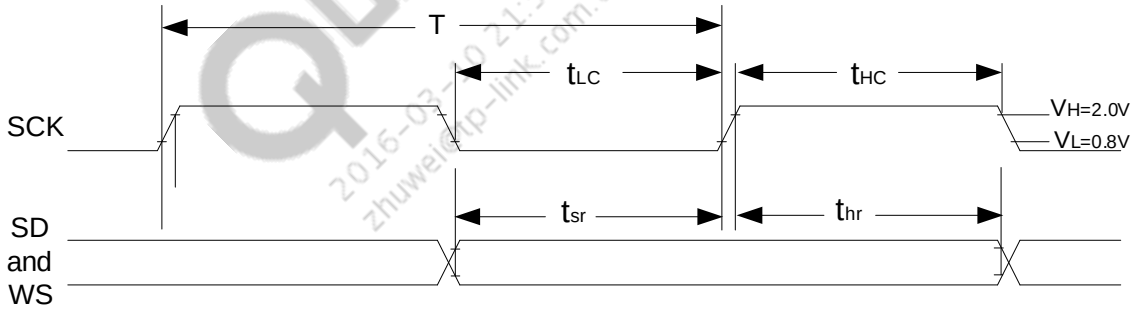


Figure 3-13 I²S interface receiver timing

Table 3-20 I²S interface timing using internal SCK clock

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Clock SCK						
Frequency	f	0		6.144	MHz	C_L = 10 pF
Clock period	T	0		162.76	ns	C_L = 10 pF
Clock high	t_{HC}	0.45T		0.55T	ns	C_L = 10 pF
Clock low	t_{LC}	0.45T		0.55T	ns	C_L = 10 pF
Inputs SD*, WS						
Setup time	t_{sr}	0.2T	–	–	ns	
Hold time	t_{hr}	0	–	–	ns	
Outputs SD*, WS						
Delay	t_{dtr}	–	–	0.8T	ns	C_L = 10 pF
Hold time	t_{htr}	0	–	–	ns	C_L = 10 pF

Table 3-21 I²S interface timing using external SCK clock

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Clock SCK						
Frequency	f	0		6.144	MHz	C_L = 10 pF
Clock period	T	0		162.76	ns	C_L = 10 pF
Clock high	t_{HC}	0.45T		0.55T	ns	C_L = 10 pF
Clock low	t_{LC}	0.45T		0.55T	ns	C_L = 10 pF
Inputs SD*, WS						
Setup time	t_{sr}	0.2T	–	–	ns	
Hold time	t_{hr}	0	–	–	ns	
Outputs SD*, WS						
Delay	t_{dtr}	–	–	0.8T	ns	C_L = 10 pF
Hold time	t_{htr}	0	–	–	ns	C_L = 10 pF

3.7.6 TDM

The IPQ4019 supports TDM. The TDM interface meet the timing given in this section.

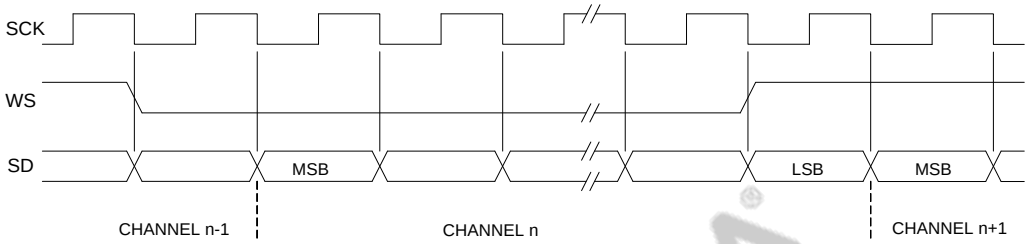


Figure 3-14 TDM interface basic timing

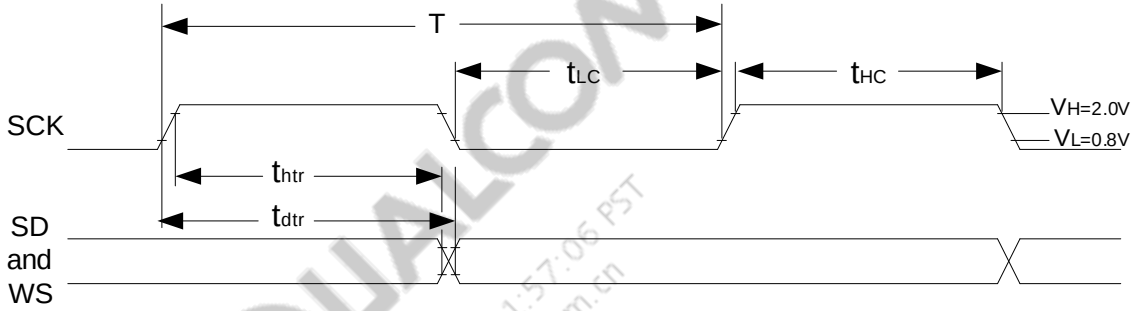


Figure 3-15 TDM interface transmitter timing

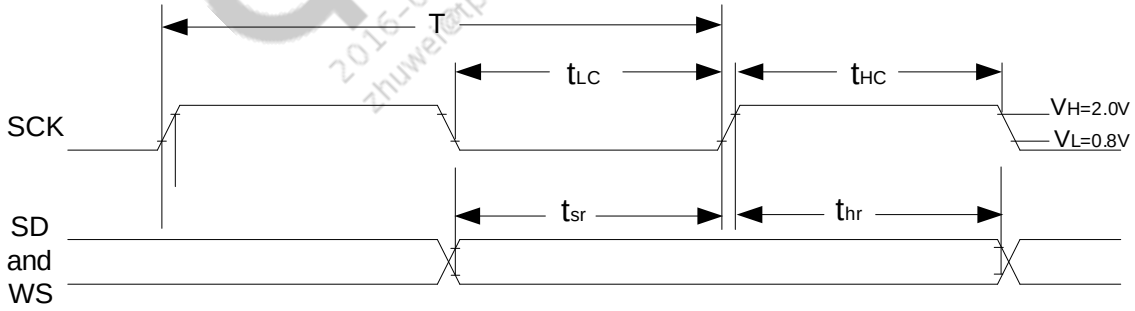


Figure 3-16 TDM interface receiver timing

Table 3-22 TDM interface timing using internal SCK clock

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Clock SCK						
Frequency	f	0		30.7	MHz	C_L = 10 pF
Clock period	T	0		32.552	ns	C_L = 10 pF
Clock high	t_{HC}	0.45T		0.55T	ns	C_L = 10 pF
Clock low	t_{LC}	0.45T		0.55T	ns	C_L = 10 pF
Inputs SD*, WS						
Setup time	t_{sr}	13	–	–	ns	
Hold time	t_{hr}	0	–	–	ns	
Outputs SD*, WS						
Delay	t_{dtr}	–	–	5	ns	C_L = 10 pF
Hold time	t_{htr}	0	–	–	ns	C_L = 10 pF

Table 3-23 TDM interface timing using external SCK clock

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Clock SCK						
Frequency	f	0		30.72 (receiver) / 24.576 (transmitter)	MHz	C_L = 10 pF
Clock period	T	0		32.552 (receiver) / 40.69 (transmitter)	ns	C_L = 10 pF
Clock high	t_{HC}	0.45T		0.55T	ns	C_L = 10 pF
Clock low	t_{LC}	0.45T		0.55T	ns	C_L = 10 pF
Inputs SD*, WS						
Setup time	t_{sr}	11.5	–	–	ns	
Hold time	t_{hr}	0	–	–	ns	
Outputs SD*, WS						
Delay	t_{dtr}	–	–	5	ns	C_L = 10 pF
Hold time	t_{htr}	0	–	–	ns	C_L = 10 pF

3.7.7 Serial peripheral interface (master only)

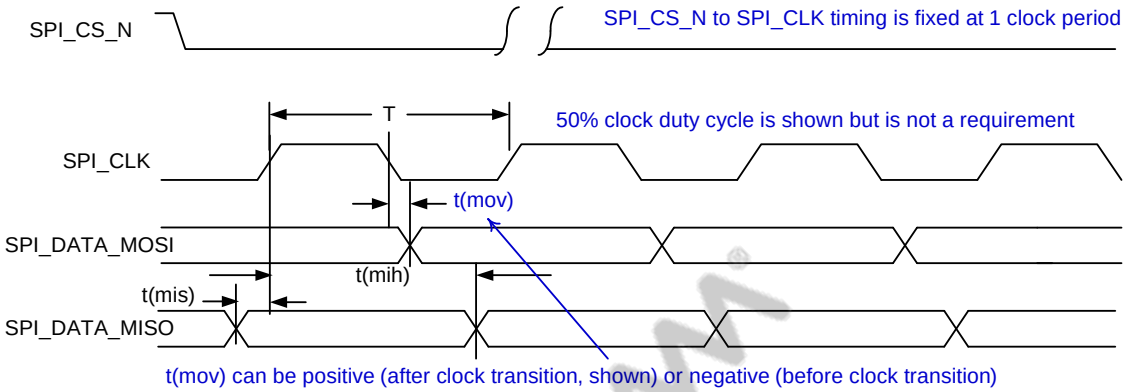


Figure 3-17 SPI master timing diagram (output_first mode and clock_idle_low mode)

Table 3-24 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
SPI clock frequency		–	–	25	MHz
T (SPI clock period)		40	–	–	ns
t(ch)	Clock high	18	–	–	ns
t(cl)	Clock low	18	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	15	–	–	ns
t(mih)	Master input hold	1	–	–	ns

3.7.8 PSGMII interface

Table 3-25 PSGMII transmit DC electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_BAUD	Transmit baud rate	–	6.250	–	Gbps
T_VDIFF[1]	Output differential voltage (into the load Rload=100Ω)	300	600	900	mVppd
T_Rs	Single-ended termination resistance	40	50	60	Ω
T_Vcm[2]	Output common mode voltage	0.6	0.8	1.05	V

1. The default value is 600 mVppd, and can be adjusted from 300 to 900 mVppd by register configuration.
2. The output common mode voltage changes accordingly if T_VDIFF is adjusted. It is also affected by supply voltage which is assumed 1.1 V+100mV/-50mV.

Table 3-26 PSGMII receive DC electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_BAUD	Receive baud rate	–	6.250	–	Gbps
R_VDIFF	Input differential voltage	100	–	1600[2]	mVppd
R_Rs	Single-ended termination resistance	40	50	60	Ω
R_Vcm[1]	Input common mode voltage	1.05	1.1	1.2	V

1. The input common mode voltage is affected by supply voltage which is assumed 1.1 V+100mV/-50mV.
2. The maximum differential voltage the receiver can tolerate.

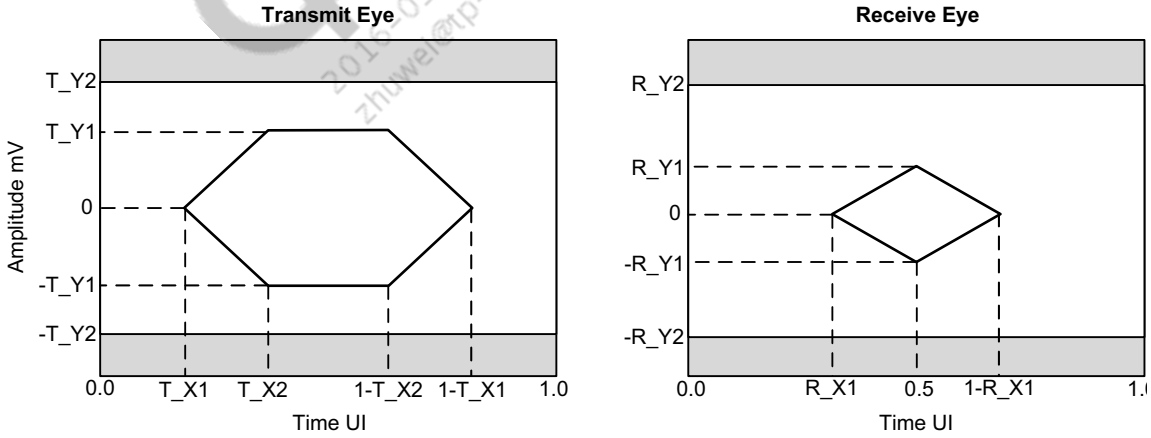


Figure 3-18 PSGMII jitter eye diagrams

Table 3-27 PSGMII transmit jitter specifications

Symbol	Parameter	Min	Typ	Max	Unit
T_UHPJ[1]	Uncorrelated high-probability jitter	–	–	0.15	UIpp
T_DCD	Duty cycle distortion	–	–	0.05	UIpp
T_Tj	Total jitter	–	–	0.30	UIpp
T_X1	Eye mask	–	–	0.15	UI
T_X2	Eye mask	–	–	0.40	UI
T_Y1	Eye mask	200	–	–	mV
T_Y2	Eye mask	–	–	450	mV

1. DJ component; no correlation to any signal level being transmitted.

Table 3-28 PSGMII receive jitter specifications

Symbol	Parameter	Min	Typ	Max	Unit
R_BHPJ[1]	Bounded high-probability jitter	–	–	0.45	UIpp
R_SJ_max	Sinusoidal jitter, maximum	–	–	5	UIpp
R_SJ_hf	Sinusoidal jitter, high frequency	–	–	0.05	UIpp
R_TJ	Total jitter (sinusoidal jitter not included)	–	–	0.60	UIpp
R_X1	Eye mask	–	–	0.30	UI
R_Y1	Eye mask	50	–	-	mV
R_Y2	Eye mask	–	–	450	mV

1. The sum of uncorrelated, bounded, high-probability jitter (UBHPJ, 0.15UI) and correlated, bounded, high-probability jitter (CBHPJ, 0.3UI). UBHPJ shows no correlation to any signal level being transmitted. CBHPJ shows a strong correlation to the signal level being transmitted, so can be considered equalizable.

3.7.9 RGMII interface

Multiplexing of data and control information takes advantage of both edges of the reference clocks, sending the lower 4 bits on the rising edge and the upper 4 bits on the falling edge. Control signals can be multiplexed into a single clock cycle using the same technique. (See Figure 3-19.)

NOTE IPQ4019 does not have delay option in either Rx or Tx direction. Need to add delay outside the chip. Setup/hold time for Rx direction is 0.9 ns.

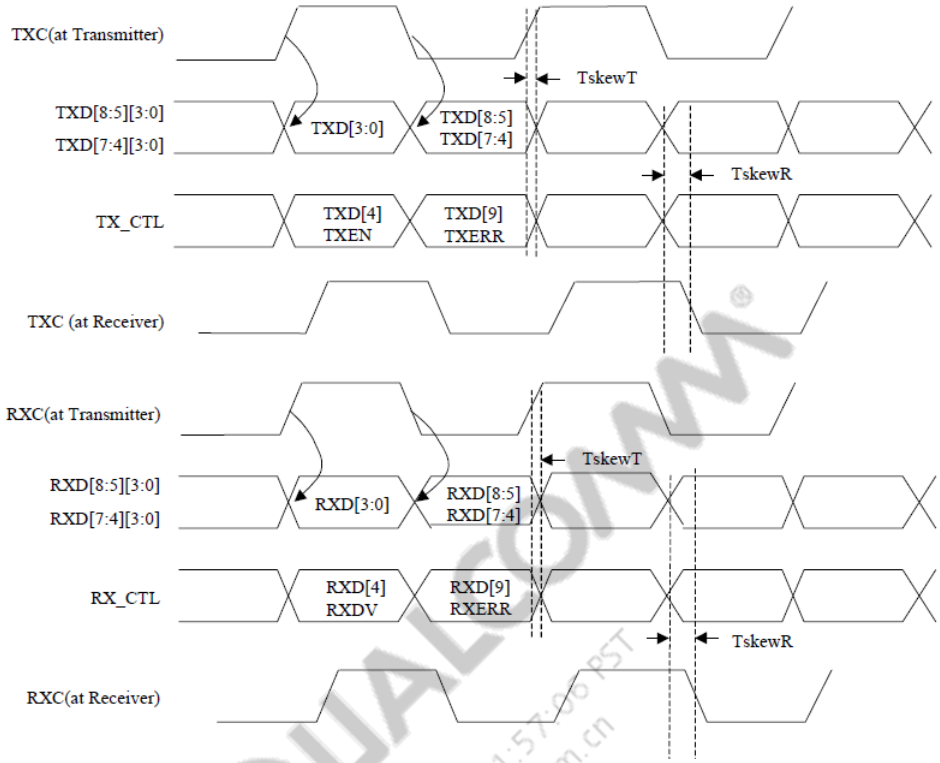


Figure 3-19 RGMII multiplexing and timing diagram

Timing for this interface is such that the clock and data are generated simultaneously by the source of the signals; therefore, the skew between clock and data is critical to proper operation. This approach provides tighter control of skew. Timing values in Table 3-29 are defined in percentages of the nominal clock period so that the table is speed independent.

Table 3-29 RGMII speed-independent timing parameters

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Data to Clock output Skew (at Transmitter)	-750	0	750	ps
TskewR	Data to Clock input Skew (at Receiver)[1]	0.9		2.7	ns
Tcyc	Clock Cycle Duration[2]	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit[3]	45	50	55	%
Duty_T	Duty Cycle for 10/100T[3]	40	50	60	%
Tr / Tf	Rise / Fall Time (20-80%)	–	–	.75	ns

1. This implies clocks on the PC board are routed such that an additional trace delay of greater than 1.6 ns and less than 2.0 ns is be added to the associated clock signal. For 10/100 the Max value is unspecified.
2. For 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.
3. Duty cycle may be stretched or shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three **Tcyc** of the lower of the transition speeds.

3.8 Radio characteristics

These conditions apply to the typical per chain characteristics unless otherwise specified:

V_{DD11} = 1.1 V
V_{DD33} = 3.3 V, T_a = 25 °C

3.8.1 Rx characteristics

Table 3-30 Rx characteristics for 2.4 GHz operation

Symbol	Parameter			Min	Typ	Max	Unit	Conditions
Frx	Receive input frequency range			2.412	—	2.484	GHz	5 MHz center frequency
Sensitivity								
Srf (CCK)	CCK	1 Rx Chain	1 Mbps	—	-97	—	dBm	See Note
			11 Mbps	—	-95	—		
	CCK	2 Rx Chains	1 Mbps	—	-100	—	dBm	
			11 Mbps	—	-98	—		
Srf (OFDM)	OFDM	1 Rx Chain	6 Mbps	—	-92.5	—	dBm	See Note
			54 Mbps	—	-75	—		
	OFDM	2 Rx Chains	6 Mbps	—	-94.5	—	dBm	
			54 Mbps	—	-78	—		
Srf (802.11ac)	802.11ac VHT20	1 Stream (1x1)	MCS0	—	-92	—	dBm	—
			MCS8	—	-67	—		
	802.11ac VHT20	2 Streams (2x2)	MCS0	—	-91	—	dBm	
			MCS8	—	-66	—		
	802.11ac VHT40	1 Stream (1x1)	MCS0	—	-89.5	—	dBm	—
			MCS9	—	-65	—		
	802.11ac VHT40	2 Streams (2x2)	MCS0	—	-88.5	—	dBm	
			MCS9	—	-64	—		
Z_{RFin_input}	Recommended LNA differential drive impedance			—	2450 MHz Impedance 167-163j	—	Ω	Ch 0, Ch 1
Adjacent channel rejection								
R_{adj}	CCK			35	41.5	—	dB	See Note 1
	OFDM		6 Mbps	16	31	—		
			54 Mbps	-1	15	—		
	VHT20		1 Stream MCS0	16	28	—		
			2 Streams MCS8	-7	6	—		
	VHT40		1 Stream MCS0	16	24	—		
			2 Streams MCS9	-9	1	—		

1. Measured with reference design AP.DK04 at RF input with NF = 5.0 dB. Minimum values based on IEEE 802.11 requirements. Tested with chain mask 3. Additional ±1.5 dB board-to-board variation must be accounted.

Table 3-31 Rx characteristics for 5 GHz operation

Symbol	Parameter			Min	Typ	Max	Unit	Conditions
Frx	Receive input frequency range			5.18	—	5.905	GHz	5 MHz center frequency
Sensitivity								
Srf (802.11a)	1 Stream (1x1)	1 Rx Chain	6 Mbps	—	-90	—	dBm	See Note 1
			54 Mbps	—	-75	—		
	2 Streams (2x2)	2 Rx Chains	6 Mbps	—	-93	—	dBm	
			54 Mbps	—	-78	—		
Srf (802.11ac)	802.11ac VHT20	1 Stream (1x1)	MCS0	—	-87	—	dBm	See Note 1
			MCS7	—	-70.5	—		
			MCS8	—	-67	—		
	802.11ac VHT40		MCS0	—	-85	—	dBm	
			MCS7	—	-68.5	—		
			MCS9	—	-61.5	—		
	802.11ac VHT80		MCS0	—	-82	—	dBm	
			MCS7	—	-65	—		
			MCS9	—	-58.5	—		
	802.11ac VHT20	2 Streams (2x2)	MCS0	—	-86	—	dBm	See Note 1
			MCS7	—	-69.5	—		
			MCS8	—	-66	—		
	802.11ac VHT40		MCS0	—	-84	—	dBm	
			MCS7	—	-67.5	—		
			MCS9	—	-60.5	—		
	802.11ac VHT80		MCS0	—	-81	—	dBm	
			MCS7	—	-64	—		
			MCS9	—	-57.5	—		
Z_{RFin_input}	Recommended LNA differential drive impedance			—	5500 MHz impedance 27 + 100j	—	Ω	Ch 2, Ch 3
Adjacent channel rejection								
R_{adj}	802.11a OFDM (4x4)		6 Mbps	16	25	—	dB	See Note 1
			54 Mbps	-1	10	—		
	VHT20	1 Stream	MCS0	16	23	—	dB	See Note 1
		2 Streams	MCS8	-7	1	—		
	VHT40	1 Stream	MCS0	16	25	—	dB	See Note 1
		2 Streams	MCS9	-9	1	—		
	VHT80	1 Stream	MCS0	16	24	—	dB	See Note 1
		2 Streams	MCS9	-9	1	—		

Table 3-31 Rx characteristics for 5 GHz operation (cont.)

Symbol	Parameter			Min	Typ	Max	Unit	Conditions
Alternate channel rejection								
R_{alt}	802.11a OFDM		6 Mbps	32	36	—	dB	See Note 1
			54 Mbps	15	19	—		
	VHT20	1 Stream	MCS0	32	36	—	dB	See Note 1
		2 Streams	MCS8	9	13	—		
	VHT40	1 Stream	MCS0	32	32	—	dB	See Note 1
		2 Streams	MCS9	7	7	—		
	VHT80	1 Stream	MCS0	32	32	—	dB	See Note 1
		2 Streams	MCS9	7	10	—		

1. Simulated at chip input with an NF = 5.8 dB.Tested with chain mask 3. Additional ±1.5 dB board-to-board variation must be accounted.

3.8.2 Tx Characteristics

Table 3-32 Tx chain characteristics for 2.4 GHz operation at chip output without external PA

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
F_{tx}	Transmit output frequency range		2.421	—	2.484	GHz	5 MHz center freq
P_{out}	Mask compliant output power						
	1 Mbps		—	-3	—	dBm	See Note[1]
	6 Mbps		—	-3	—		
	HT20, MCS0		—	-3	—		
	HT40, MCS0		—	-3	—		
EVM (Header Only)			**Tx Power (dBm)[2]:**				
	802.11ac, VHT20 (Per Tx chain)	MCS8	—	-40	—	dB	Tx power < -6.5 dBm See Note[1]
	802.11ac, VHT40 (Per Tx chain)	MCS9	—	-39.5	—	dB	Tx power < -6.5 dBm See Note[1]
SP_{gain}	Tx gain step		—	0.5	—	dB	See Note[2]
A_{pl}	Accuracy of power control loop		—	±1.5	—	dB	See Note[3]
Z_{RFout_load}	Recommended PA single-ended load impedance		—	50	—	Ω	—

1. Simulated at the chip output
2. Guaranteed by design.
3. Manufacturing calibration required.

Table 3-33 Tx chain characteristics for 5 GHz operation at chip output without external PA

Symbol	Parameter			Min	Typ	Max	Unit	Conditions
F_{tx}	Transmit output frequency range			5.18	—	5.905	GHz	20 MHz center frequency
P_{out}	Mask compliant output power							
	6 Mbps			—	-1.6	—	dBm	See Note[1]
	VHT20, MCS0			—	-1.6	—		
	VHT40, MCS0			—	-1.6	—		
	VHT80, MCS0			—	-1.6	—		
EVM (Header Only) (Per Tx Chain)				**Tx Power (dBm)[2]:**				
	802.11ac	VHT20	MCS8	—	-39.5	—	dB	Tx power < -6.5 dBm See Note[1]
	802.11ac	VHT40	MCS9	—	-39.5	—	dB	Tx power < -9.5 dBm See Note[1]
	802.11ac	VHT80	MCS9	—	-39.5	—	dB	Tx power < -10.5 dBm See Note[1]
SP_{gain}	Tx gain step			—	0.5	—	dB	See Note[2]
A_{pl}	Accuracy of power control loop			—	±1.5	—	dB	See Note[3]
Z_{RFout_load}	Recommended PA single-ended load impedance			—	50	—	Ω	—
SS	Sideband suppression			—	-48	—	dBc	—

1. Simulated at the chip output
2. Guaranteed by design.
3. Manufacturing calibration required.

3.9 Power consumption

This section shows the typical power consumption with external PMU as a function of the IPQ4019's operating mode. See Note [1].

Table 3-34 802.11ac power consumption for 2.4 GHz (VHT20)

Mode	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	VDDR1.35 (mA)	Power consumption (W)
Rx (two chains) MCS0	276	371	968	136.5	2.57
Rx (two chains) MCS8	277	341	985	139	2.56
Tx (two chains) MCS0	263	216	806	123.5	2.16
Tx (two chains) MCS8	263	222	847	130.5	2.22

Table 3-35 802.11ac power consumption for 2.4 GHz (VHT40)

Mode	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	VDDR1.35 (mA)	Power consumption (W)
Rx (two chains) MCS0	276	228	984	133.5	2.20
Rx (two chains) MCS9	277	352	1005	139.5	2.32
Tx (two chains) MCS0	263	229	833	125	2.42
Tx (two chains) MCS9	264	224	925	139.5	2.60

Table 3-36 802.11ac power consumption for 5 GHz (VHT20)

Mode	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	VDDR1.35 (mA)	Power consumption (W)
Rx (two chains) MCS0	263	163	735	123.5	2.51
Rx (two chains) MCS8	263	164	807	131	2.54
Tx (two chains) MCS0	276	313	964	143	2.02
Tx (two chains) MCS8	276	314	990	145	2.11

Table 3-37 802.11ac power consumption for 5 GHz (VHT40)

Mode	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	VDDR1.35 (mA)	Power consumption (W)
Rx (two chains) MCS0	262	178	795	125	2.10
Rx (two chains) MCS9	263	173	885	138	2.22
Tx (two chains) MCS0	276	313	1001	143.5	2.55
Tx (two chains) MCS9	276	314	1011	148.5	2.57

1. Measured with AP.DK04 reference design using CS meta IPQ4019.ILQ.1.1.r1/00011.1.

Table 3-38 802.11ac power consumption for 5 GHz (VHT80)

Mode	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	VDDR1.35 (mA)	Power consumption (W)
Rx (two chains) MCS0	263	215	919	126.5	2.29
Rx (two chains) MCS9	263	217	1086	154.5	2.51
Tx (two chains) MCS0	277	339	1090	144	2.68
Tx (two chains) MCS9	276	342	1123	155.5	2.73

Table 3-39 802.11ac power consumption for 2.4 GHz (VHT40) + 5 GHz (VHT80)

Mode	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	VDDR1.35 (mA)	Power consumption (W)
Rx (two chains) MCS0	290	478	1309	160	3.14
Rx (two chains) MCS9	263	209	1223	169.5	2.67
Tx (two chains) MCS0	264	212	1149	127.5	2.54
Tx (two chains) MCS9	291	491	1337	171.5	3.20

4 Mechanical Information

The IPQ4019 uses 583-ball BGA micro scale package (583MSP) technology.

4.1 Device physical dimensions

Figure 4-1 shows the package drawing and dimensions. All linear dimensions are in millimeters.

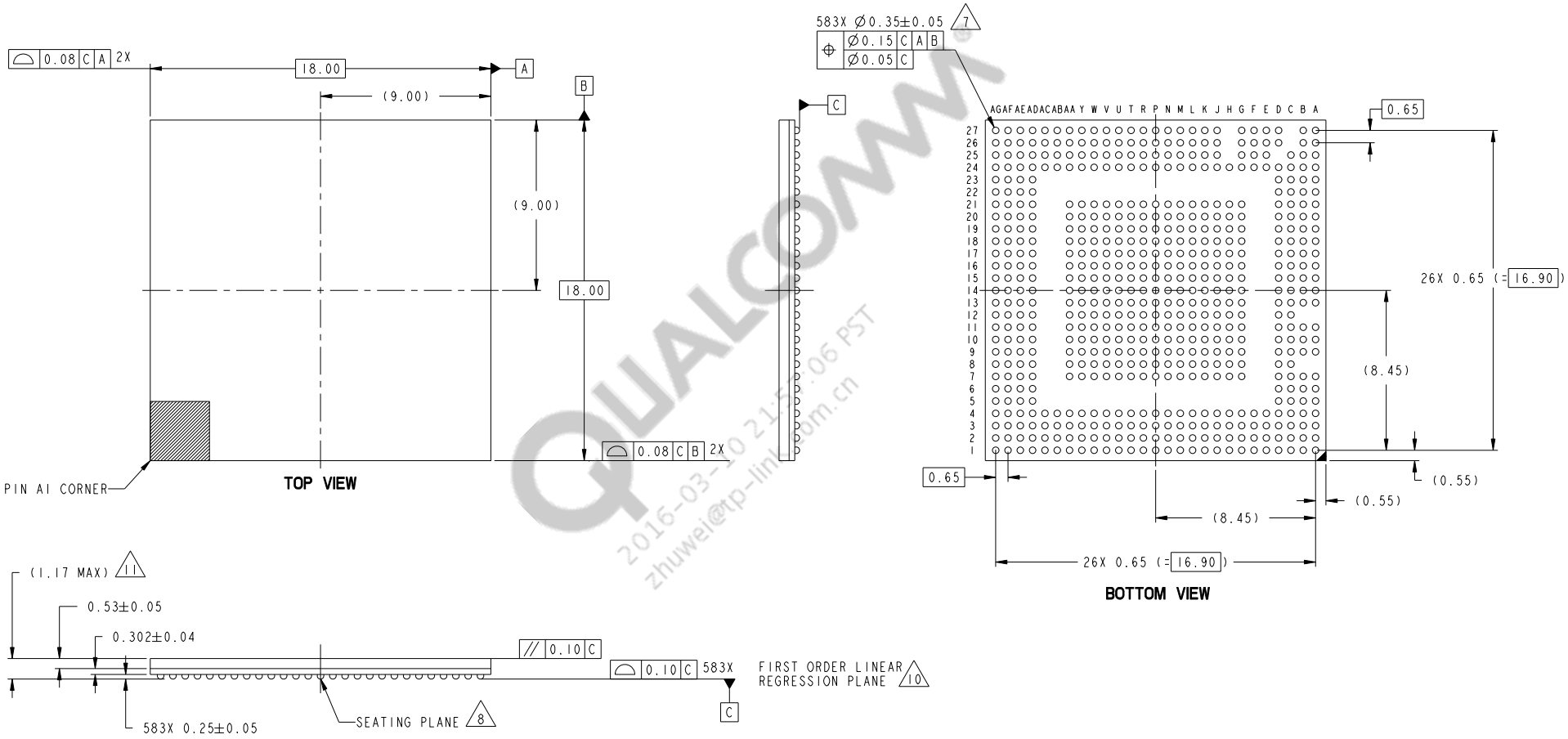


Figure 4-1 IPQ4019 package details

Table 4-1 Linear tolerances

x	± 1
x.x	± 0.3
x.xx	± 0.10
x.xxx	± 0.080

Notes: Unless otherwise specified.

1. Interpret drawing per ASME Y14.100.
2. All dimensions shown on this drawing are in millimeters (MM).
3. Interpret dimensions and tolerances per ASME Y14.5-2009.
4. Workmanship shall be in accordance with *Qualcomm Package Assembly Workmanship Standard* 80-V0691-2.
5. Qualcomm supplied electronic database(s) are for reference only. Dimensional information on current revision of released drawing takes precedence over electronic database(s).
6. Change approval. All changes shall be in accordance with 80-V3652-1 *General Supplier Quality Requirements*.
7. Dimension measured at the maximum solder ball diameter, parallel to the primary datum.
8. The seating plane is defined by three non-collinear balls that support the free standing package when it is placed on a flat surface. The vectors formed by the three balls establishing the seating plane shall include the center of gravity.
9. The surface finish of the package shall be EDM CHARMILLE #24-#27.
10. Primary datum is determined by the first order LMS regression plane through the spherical crowns of all solder balls on this side of the package.
11. Maximum package hight determined by RSS tolerance methods.

4.2 Part marking

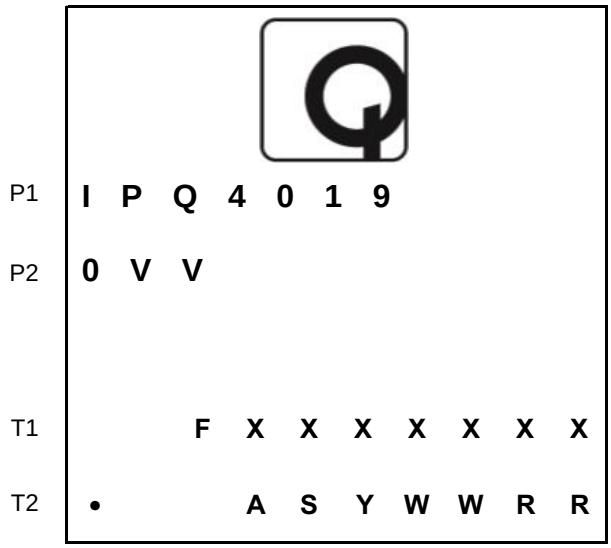


Figure 4-2 IPQ4019 marking (top view, not to scale)

Table 4-2 IPQ4019 marking line definitions

Line	Marking	Description
P1	IPQ4019	Product name
P2	PBB	P: configuration code = 0 BB: feature code = VV
T1	FXXXXXXX	F: fab code XXXXXXX = lot number
T2	ASYWWRR	A: assembly site code S: assembly sequence number Y: single, last digit of year WW: work week (based on calendar year) RR: revision code

4.3 Device ordering information

Order numbers have the form shown in Figure 4-3.

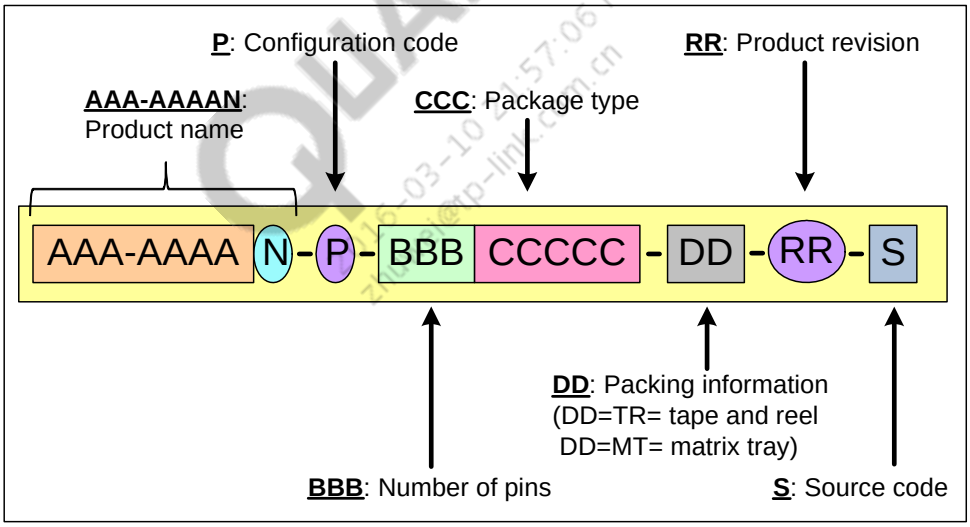


Figure 4-3 Device identification code

Table 4-3 shows the available order numbers.

Table 4-3 IPQ4019 order numbers

PRR	Order number	Description
000	IPQ-4019-0-583MSP-MT-00-0	RoHS & BrCl-free, C-Temp
000	IPQ-4019-0-583MSP-TR-00-0	RoHS & BrCl-free, C-Temp

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. Qualcomm follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. The IPQ4019 is classified as MSL3; the qualification temperature was 250ºC.

4.5 Thermal characteristics

Table 4-4 Thermal resistance[1]

Parameter		Comment	Typical	Unit
θ_{JC}	Junction-to-Case	■ JESD51-7, JESD51-8 ■ Cu block at top of package maintained at 25°C	3.59	°C/W
θ_{JB}	Junction-to-Board	■ JESD51-7, JESD51-8 ■ Cold pate ring maintained at 25C at top and bottom of PCB	4.89	°C/W
Ψ_{JT}	Junction-to-Top-Center	■ JESD51-2A, JESD51-7	0.03	°C/W
θ_{JA}	Junction-to-Ambient	■ JESD51-2A, JESD51-7	21	°C/W

1. Contact your Qualcomm representative for power dissipation for each use case.

5 Carrier, Storage, and Handling

5.1 Carrier

5.1.1 Tape and reel information

The carrier tape system conforms to EIA-481 standards.

Simplified sketches of the IPQ4019 tape carrier are shown in Figure 5-1 and Figure 5-2, including the part orientation. Tape and reel details for the IPQ4019 are as follows:

- Reel diameter: 330 mm
- Hub size: 102 mm
- Tape width: 32 mm
- Tape pocket pitch: 24 mm
- Feed: Single
- Units per reel: 1000

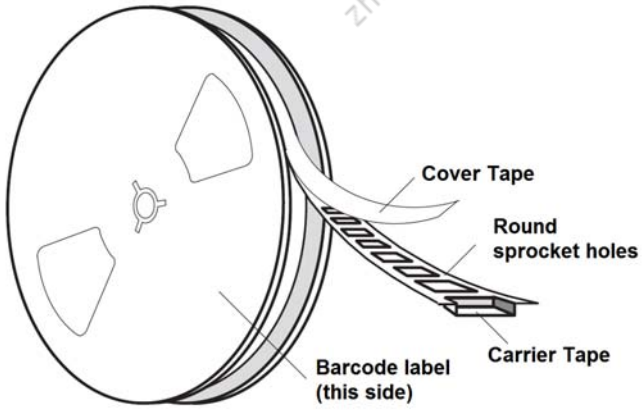


Figure 5-1 Tape orientation on reel

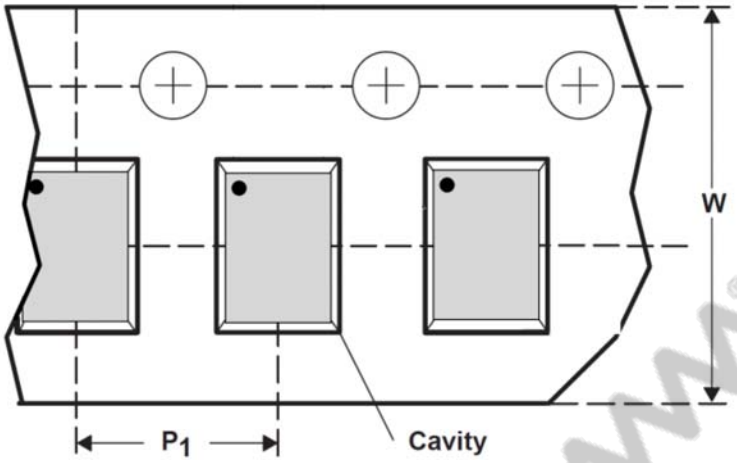
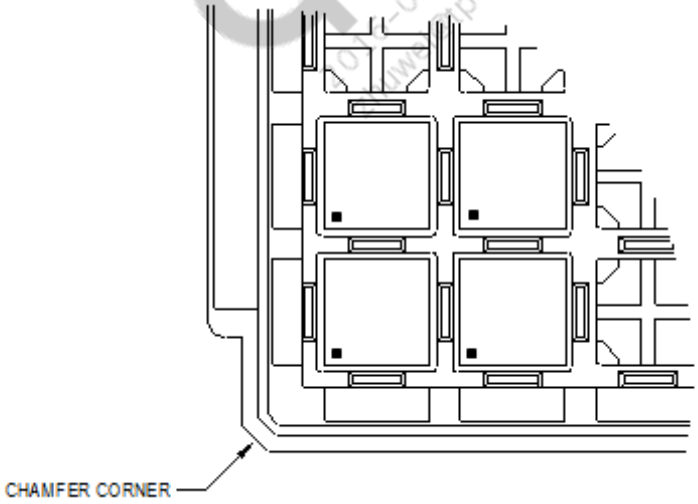


Figure 5-2 Part orientation in tape

5.1.2 Matrix tray information

Matrix tray carriers confirm to JEDEC standards. The device pin 1 is oriented to the chamfered corner of the matrix tray. Each tray of IPQ4019 contains up to 84 devices. See Figure 5-3 for matrix-tray key attributes and dimensions.



Key dimensions	
Array	6 × 14 = 84
M	14.60 mm
M1	18.79 mm
M2	21.34 mm
M3	21.34 mm

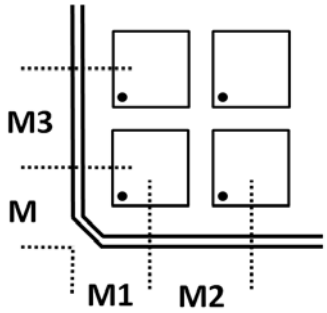


Figure 5-3 Matrix tray part orientation

5.2 Storage

5.2.1 Bagged storage conditions

IPQ4019 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling is described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is **not necessary** to bake the IPQ4019 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the IPQ4019 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see *ASIC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Barcode label and packing for shipment

Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

6 PCB Mounting Guidelines

Guidelines for mounting the IPQ4019 device onto a PCB are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification.

6.1 RoHS compliance

The IPQ4019 device is externally lead-free and RoHS-compliant. Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products.

6.2 SMT parameters

This section describes board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil-pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability. Review the land pattern and stencil pattern design recommendations as a guide for characterization:

PCB Land and Stencil Design Guide (LS90-NG134-1).

6.2.2 Reflow profile

Reflow profile conditions typically used by Qualcomm for lead-free systems are listed in Table 6-1 and are shown in Figure 6-1.

Table 6-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Dry-out and flux activation	150 to 190°C	60 to 120sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C. This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

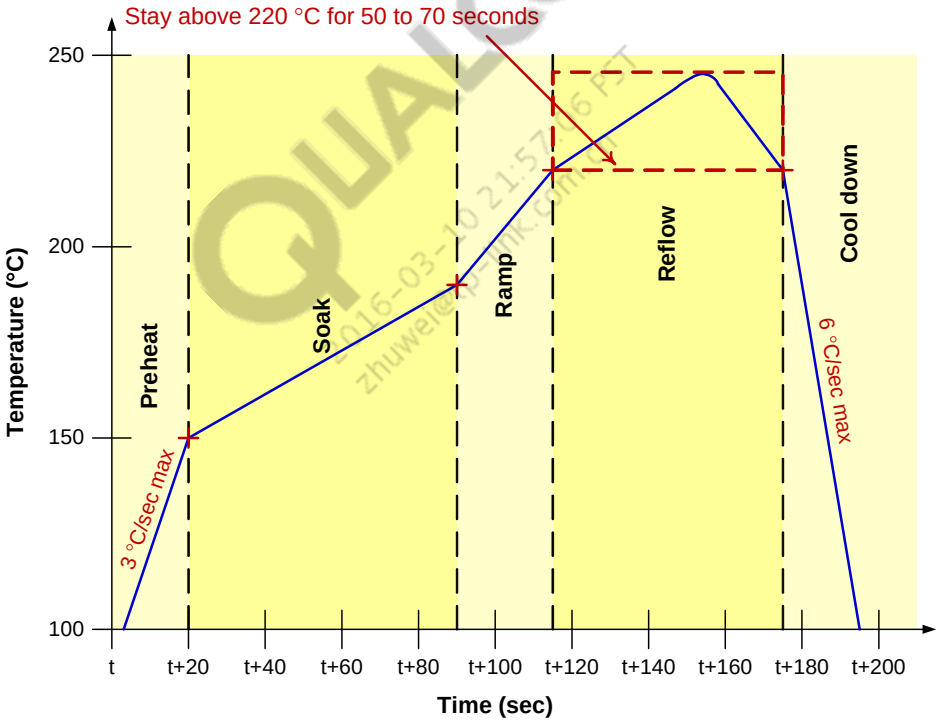


Figure 6-1 Typical SMT reflow profile

6.2.3 SMT peak package-body temperature

During a production board's reflow process, the temperature seen by the package must be controlled. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more). Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the Qualcomm recommended limits must not be exceeded.

6.2.4 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume board assembly, including:

- Electrical continuity
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume

6.3 Board-level reliability

Qualcomm conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

For board-level reliability data, refer to *Board-Level Reliability DRQFN/MQFN* (BR80-NT096-1).

7 Part Reliability

7.1 Reliability qualification summary

IPQ4019 reliability evaluation report.

Table 7-1 Silicon reliability results

Tests, Standards and Conditions	Lot/Sample	Result
Average failure rate (AFR) in FIT (λ) failure in billion device-hours HTOL: JESD22-A108-A Use condition: Temperature: 65°C, core voltage: 1.2 V (Total samples from three different wafer lots)	3x77	0F/231 AFR=10.2
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from three different wafer lots)	3x77	97.7
ESD - Human-body model (HBM) rating JESD22-A114-F Target: 2000 V (Total samples from one wafer lot)	1x3	Pass
ESD - Charge-device model (CDM) rating JESD22-C101-D Target: 500 V (Total samples from one wafer lot)	1x3	Pass
Latch-up (I-test) EIA/JESD78A Trigger current: ±100 mA; temperature: 85°C (Total samples from one wafer lot)	1x6	Pass
Latch-up (Vsupply overvoltage) EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × Vdd max per device specification; temperature: 85°C (Total samples from one wafer lot)	1x6	Pass

Table 7-2 Package reliability results

Tests, Standards and Conditions	Package a Lot/Sample	Package b Lot/Sample	Result
Moisture resistance test (MRT) MSL3; J-STD-020/JESD22-A113-F Reflow at 260°C +0/-5 °C, Total samples from three different assembly lots	6x231	6x231	Pass
Temperature cycle JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8-10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning** JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C, Total samples from three different assembly lots	6x77	6x77	Pass
Unbiased highly accelerated stress test JESD22-A118 130°C / 85% RH and 96 hrs duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5 °C, Total samples from three different assembly lots	6x77	6x77	Pass
Biased Highly Accelerated Stress test JESD22-A110 110°C / 85% RH and 264 hrs duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5 °C, Total samples from three different assembly lots	3x77	3x77	Pass
High-Temperature Storage Life JESD22-A103-C Temperature 150°C, 500, 1000 hours Total samples from three different assembly lots	6x77	6x77	Pass
Physical dimensions JESD22-B100-A	3x15	3x15	Pass
Die shear MIL-STD-883E, Method 2019 Total samples from three different assembly lots at each SAT	3x5	3x5	Pass

7.2 Qualification sample description

Table 7-3 IPQ4019 characteristics

Device name	IPQ4019
Package type	583MSP BGA
Package body size	18.0 mm × 18.0 mm × 1.17 mm
BGA pin count	583
Process	40 nm