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AMPLITUDE SHIFT KEYING:

ECE dept.

- 1) ASK is the simplest digital modulation technique where a binary information signal directly modulates the amplitude of an analog carrier.
- 2) ASK is sometimes called Digital Amplitude Modulation (DAM).

Mathematically, ASK is :-

$$V_{(ASK)}(t) = [1 + V_m(t)] \left[\frac{A}{2} \cos(\omega_c t) \right]$$

Where,

$V_{ASK}(t)$ = amplitude-shift keying wave.

$V_m(t)$ = digital information (modulating) signal.

$A/2$ = unmodulated carrier amplitude.

ω_c = analog carrier radian frequency ($\omega_c = 2\pi f_c$)

When $V_m(t) = 1V$,

$$\begin{aligned} V_{(ASK)}(t) &= [1+1] \left[\frac{A}{2} \cos(\omega_c t) \right] \\ &= 2 \left[\frac{A}{2} \cos(\omega_c t) \right] \end{aligned}$$

logic 1 = 1V.

logic 0 = -1V.

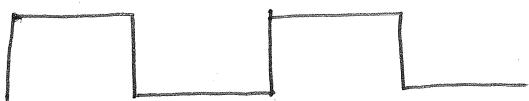
$$V_{(ASK)}(t) = A \cos(\omega_c t) \quad \text{--- ①}$$

When $V_m(t) = -1V$

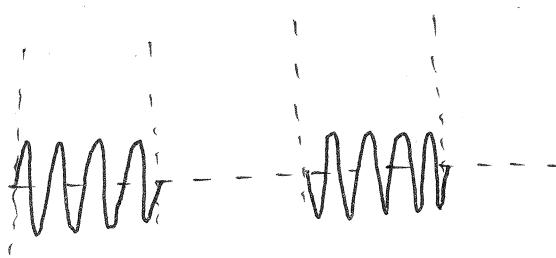
$$V_{(ASK)}(t) = [1-1] \left[\frac{A}{2} \cos(\omega_c t) \right]$$

$$V_{(ASK)}(t) = 0 \quad \text{--- ②}$$

- 3) Thus the modulated wave $V_{ASK}(t)$, is either $A \cos(\omega_c t)$ or 0. Hence the carrier is either 'on' or 'off' which is why amplitude shift keying is sometimes referred to as on-off keying (OOK).



Binary Input.



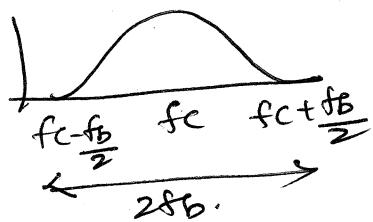
Output of ASK waveform.

- 4) For every change in the input binary data stream, there is one change in the ASK waveform and the time of one bit (t_b) equals the time of one analog signaling element (t_s).
- 5) Rate of change of the ASK waveform is the same as the rate of change of the binary input (bps); thus the bit rate equals the baud.
- 6) Baud rate is also equal to the minimum Nyquist bandwidth.

$$B = \frac{f_b}{N}; \text{ setting } N \text{ to 1} \therefore B = \frac{f_b}{1} = f_b.$$

$$\begin{aligned} B.W &= f_b \\ (B.W &= f_c + \frac{f_b}{2}) - (f_c - \frac{f_b}{2}) \\ \text{band} &= \frac{f_b}{1} = \frac{f_b}{1} = f_b. \\ \therefore &= \Delta f \\ B.W &= (f_c + \frac{\Delta f}{2}) - (f_c - \frac{\Delta f}{2}) = \Delta f. \end{aligned}$$

FREQUENCY SHIFT KEYING:-



- 1) Simple, low performance type of digital modulation.
- 2) Constant-amplitude angle modulation similar to standard frequency modulation (FM) except the modulating signal is a binary signal that varies b/w two discrete voltage levels rather than a continuously changing analog waveform.

$$V_{fsk}(t) = V_c \cos [2\pi (f_c + v_m(t) \Delta f) t]$$

(2)

✓ (6)

$V_{FSK}(t)$ = binary FSK waveform

V_c = Peak analog carrier amplitude (volts)

f_c = analog carrier center frequency (Hz)

Δf = peak change (shift) in the analog carrier frequency (Hz).

$V_m(t)$ = Binary input signal.

3) Peak shift in the carrier freq (Δf) is proportional to the amplitude of the binary input signal ($V_m(t)$), and the direction of the shift is determined by the polarity.

4) logic 1 = +V & a logic 0 = -V.

For logic 1 input, $V_m(t) = +1$,

$$\text{So, } V_{FSK}(t) = V_c \cos [2\pi(f_c + \Delta f)t]$$

For logic 0 input, $V_m(t) = -1$,

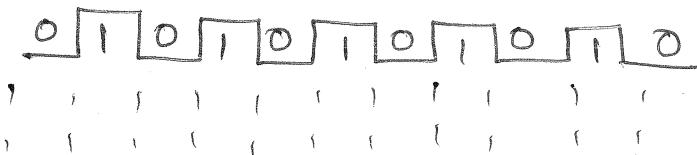
$$V_{FSK}(t) = V_c \cos [2\pi(f_c - \Delta f)t]$$

5) With PSK, freq-deviation is the difference b/w either the mark or space frequency and the carrier center freq, or half the difference b/w the mark & space frequencies.

$$\Delta f = \frac{|f_m - f_s|}{2}$$

Δf = freq. deviation (Hz)

$|f_m - f_s|$ = Difference b/w mark & space frequencies (Hz).



Binary input.



FSK O/p.

0 1 0 1 0 1 0 1 0
fs fm

6) Mark frequency is the higher freq ($f_c + \Delta f$), and the Space frequency is the lower frequency ($f_c - \Delta f$).

Binary I/P	freq. O/P
0	Space (f_s)
1	mark (f_m)

FSK Bit Rate, Baud and Bandwidth:

- i) Time of one bit (t_b) is the same as the time for FSK O/p is a mark of space frequency (t_s). Thus the bit time equals the time of an FSK signaling element, and the bit rate equals the baud.

The baud for binary FSK can also be determined by substituting $N=1$,

$$\text{band} = \frac{f_b}{N} = \frac{f_b}{1} = f_b.$$

The minimum bandwidth for FSK is given as

$$\begin{aligned} B &= |(f_s - f_b) - (f_m - f_b)| \\ &= |f_s - f_m| + 2f_b. \end{aligned}$$

B = minimum Nyquist bandwidth (Hz)

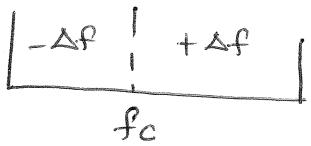
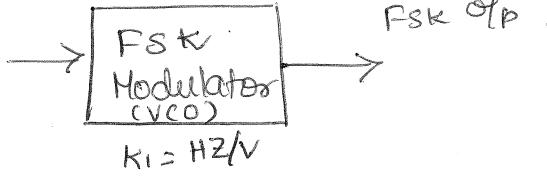
Δf = freq. deviation ($|f_m - f_s|$) (Hz)

f_b = input bit rate (bps)

FSK TRANSMITTER:

NRZ

binary I/P



logic 0

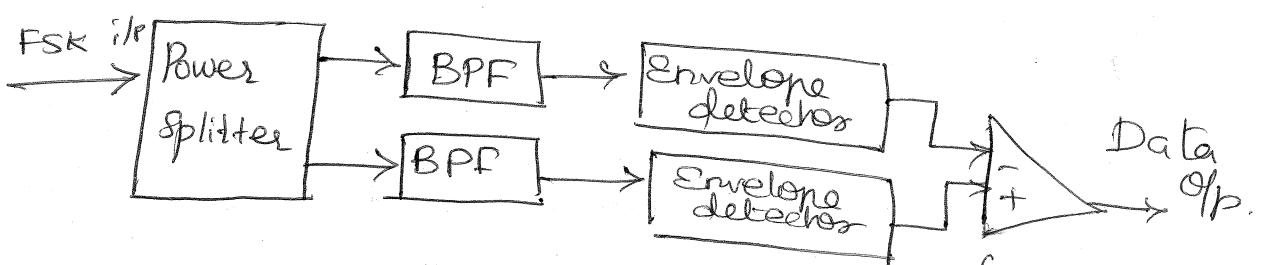
logic 1

- 1) FSK modulator is often a Voltage Controlled Oscillator. Centre freq. falls halfway between the mark and space frequencies.
 - 2) Logic 1 input shifts the VCO O/P to the mark frequency, and a logic 0 input shifts the VCO O/P to the space frequency.
 - 3) Thus, when binary input signal changes back and forth b/w logic 0 and 1 conditions, VCO O/P shifts or deviates back and forth b/w mark and space frequencies.
 - 4) A VCO-FSK modulator can be operated in the sweep mode where the peak frequency deviation is simply the product of the binary input voltage and the deviation sensitivity of the VCO. In sweep mode of modulation, the freq. deviation is,
- $$\Delta f = V_m(t) K_e$$
- K_e = deviation sensitivity
- $V_m(t)$ = peak binary modulating signal voltage.
- Δf = peak freq. deviation.
- 5) Freq. deviation is simply plus or minus the peak voltage of the binary signal times the deviation sensitivity of the VCO.

FSK Receiver :-

- 1) FSK i/p signal is simultaneously applied to the inputs of both bandpass filters through a power splitter. The respective filter passes only the mark or only the space frequency on to its respective envelope detectors.
- 2) Envelope detector in turn indicates the total power in each passband, and comparator responds to the largest of the two powers. This is called non-coherent detection.

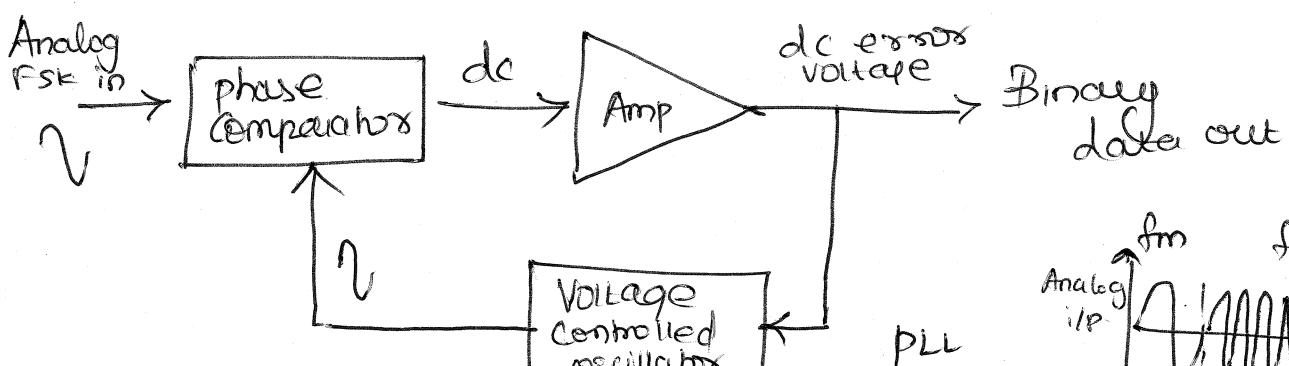
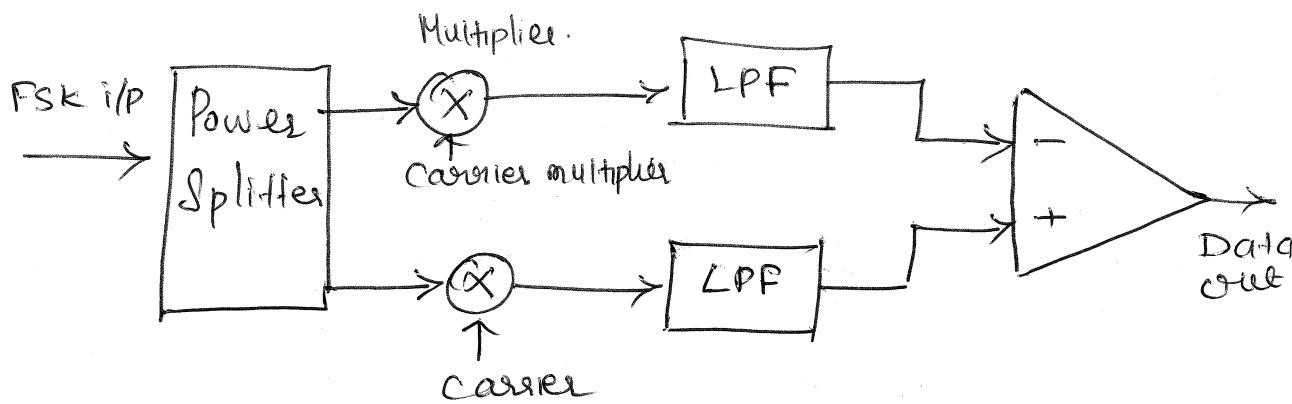
Non-Coherent PSK demodulation.



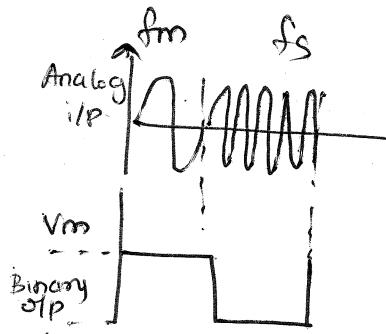
- 2) In Coherent FSK receiver, the incoming FSK signal is multiplied by a recovered carrier signal that has the exact same freq & phase as the reference. The two transmitted frequencies are not generally continuous.
- 3) The most common circuit for demodulation of binary FSK is the phase locked loop (PLL). Input to the PLL shifts b/w the mark and space frequencies, the dc error voltage at the output of the phase comparator follows the frequency shift.
- 4) One represents logic 1 and the other a logic 0. So, o/p is a two level representation of the FSK i/p.
- 5) Natural frequency of the PLL is made equal to the center frequency of the FSK modulator.

6) Changes in the dc error voltage follow the changes in the analog i/p frequency and are symmetrical around OV.

Coherent FSK demodulator



PLL FSK demodulator



Phase-Shift Keying :-

- 1) Another form of angle-modulated, constant-amplitude digital modulation.
- 2) The input binary information is encoded into groups of bits before modulating the carrier. The number of bits in a group ranges from 1 to 12 or more.

→ Binary Phase Shift Keying :-

- 1) The simplest form of PSK is binary phase shift keying (BPSK), where $N=1$ and $M=2$.

- 2) Two phases ($2^1=2$) are possible for the carrier.

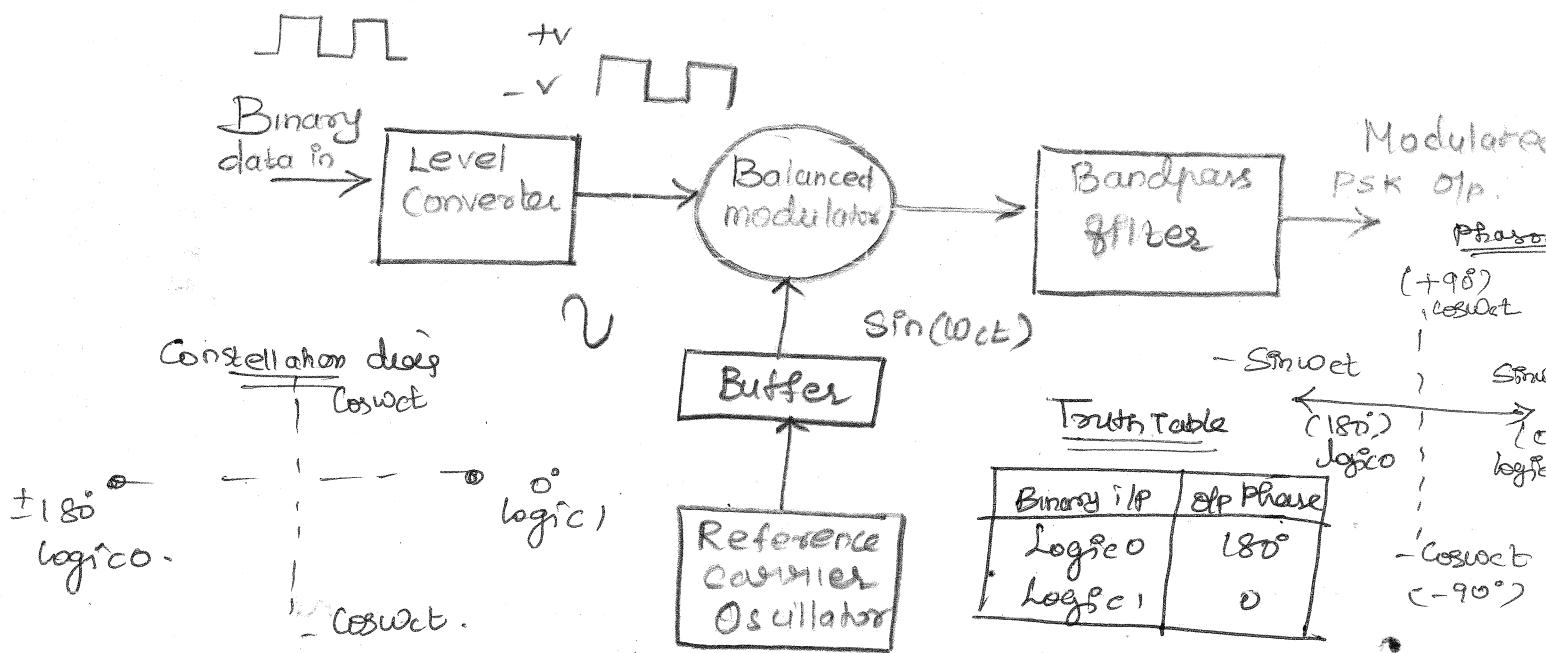
One phase represents a logic 1, and the other phase represents a logic 0.

3) As the input digital signal changes state, the phase components of the o/p carrier signals b/w two angles there are represented separated by 180° . Hence, BPSK can also be called Phase Reversal Keying (PRK) & biphase modulation.

\Rightarrow BPSK Transmitter:-

- 1) The balanced modulator acts as a phase reversing switch.
- 2) Depending on the logic condition of the digital I/P's the carrier is transferred to the o/p either in phase or 180° out of phase with the reference carrier oscillator.

3)



4) Bandwidth Considerations of BPSK:-

A balanced modulator is a product modulator. The o/p signal is the product of the two I/P signals. In a BPSK modulator, the carrier I/P signal is multiplied by the binary data. If $+V$ is assigned to a logic 1 & $-V$ is assigned to a logic 0, the I/P carrier is multiplied by either +1 or -1. Consequently o/p signal is either $+1 \sin \omega ct$ or $-1 \sin \omega ct$;

✓ (9)

+1 Sin ω t = representation of a signal that is in phase with reference oscillator.

-1 Sin ω t = 180° out of phase with reference oscillator.

- 5) Output rate of change (band) is equal to the input rate of change and the widest off b-w occurs when the input binary data are an alternating I/O Sequence.

O/p of BPSK modulator is proportional to

$$\text{BPSK O/p} = [\sin(2\pi f_a t)] \times [\sin(2\pi f_c t)]$$

f_a = maximum fundamental freq. of binary input (Hz).

f_c = Reference carrier frequency (Hz).

Solving product of two 'sin' functions,

$$\frac{1}{2} \cos[2\pi(f_c - f_a)t] - \frac{1}{2} \cos[2\pi(f_c + f_a)t]$$

Thus minimum double sided Nyquist bandwidth (B) is

$$\frac{f_c + f_a}{2}$$

$$-\frac{(f_c + f_a)}{2}$$

$$\underline{\underline{0}}$$

because $f_a = f_b/2$ where f_b = Input bit rate.

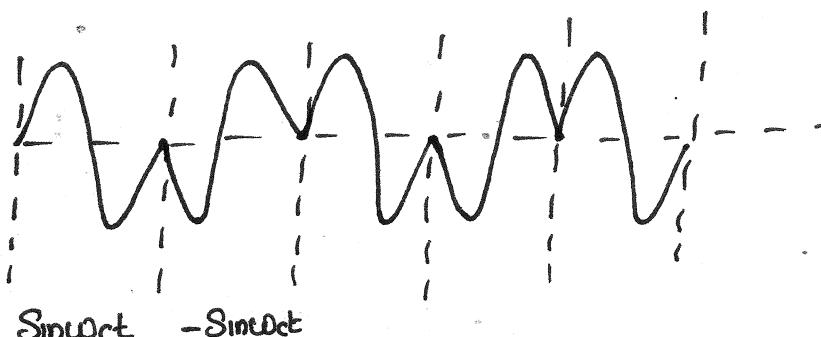
$$B = \frac{2f_b}{2} = f_b$$

Where, B = minimum double sided Nyquist b-w.

BPSK Waveform.



→ Binary I/P.



BPSK O/P.

→ A logic 1 input produces an analog O/P signal with a 0° phase angle, and a logic 0 input produces an analog O/P signal with a 180° phase angle.

→ As the binary input shifts b/w a logic 1 and logic 0, vice-versa, phase shift b/w 0° and 180° respectively.

BPSK RECEIVER :-

- 1) Input of the signal may be $+\sin\omega ct$ or $-\sin\omega ct$.
- 2) The Coherent Carrier Recovery circuit detects and regenerates a carrier signal that is both frequency and phase coherent with the original transmit carrier.
- 3) Balanced modulator O/P will be product of two inputs.
- 4) LPF Separates the recovered binary data from the Complex demodulated Signal.

for a BPSK input signal of $+\sin\omega ct$ (logic 1),

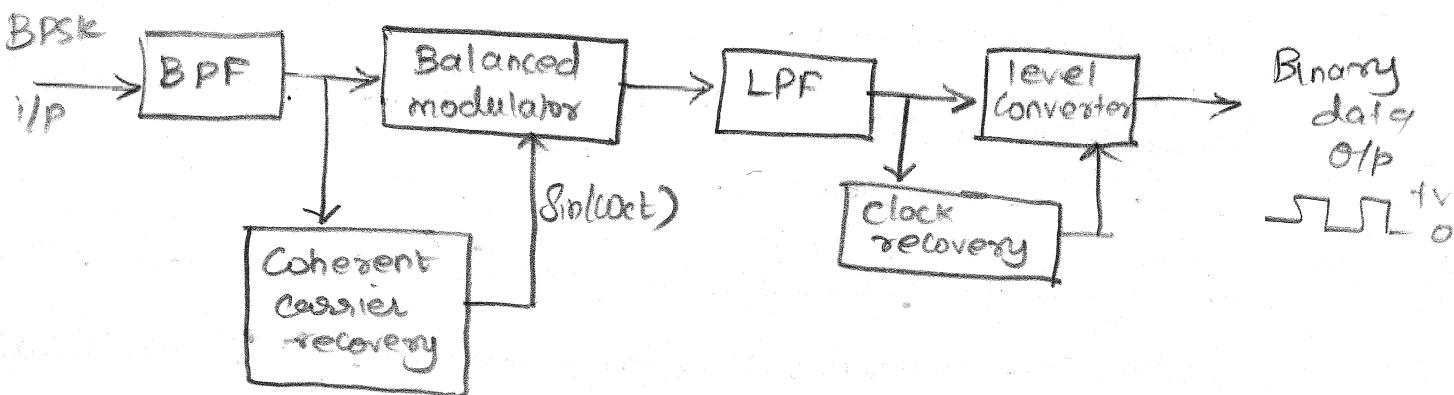
$$O/P_{(BPSK)} = (\sin\omega ct)(\sin\omega ct) = \sin^2\omega ct.$$

$$\text{Cos}, \quad \sin^2\omega ct = \frac{1}{2}(1 - \cos 2\omega ct) = \frac{1}{2} - \frac{1}{2}\cos 2\omega ct$$

filter off ↑

$$\text{So, } O/P = +\frac{1}{2}V = \text{logic 1.}$$

- ✓
- 5) Output of the balanced modulator contains a ⁶ ~~tre~~ voltage ($\pm \frac{1}{2}V$) and a cosine wave at twice the carrier freq ($2\omega_c$).
- 6) LPF has a cutoff freq much lower than $2\omega_c$ and thus blocks the second harmonic of the carrier and passes only the positive constant component. A tre voltage represents a demodulated logic 1.
- 7) For BPSK input signal of $-\sin \omega_c t$ (logic 0), the O/P of the balanced modulator is,
- $$O/P = (-\sin \omega_c t)(\cos \omega_c t) = -\sin^2 \omega_c t.$$
- (or), $-\sin^2 \omega_c t = -\frac{1}{2}(1 - \cos 2\omega_c t)$
 $= -\frac{1}{2} + \frac{1}{2} \cos 2\omega_c t$
- $$O/P = -\frac{1}{2}V = \text{logic 0.}$$
- 8) O/P of the balanced modulator contains negative voltage ($-\frac{1}{2}V$) and a cosine wave at twice the carrier freq ($2\omega_c$). Again the LPF blocks the second harmonic of the carrier and passes on the negative constant component. A negative voltage represents a demodulated logic 0.



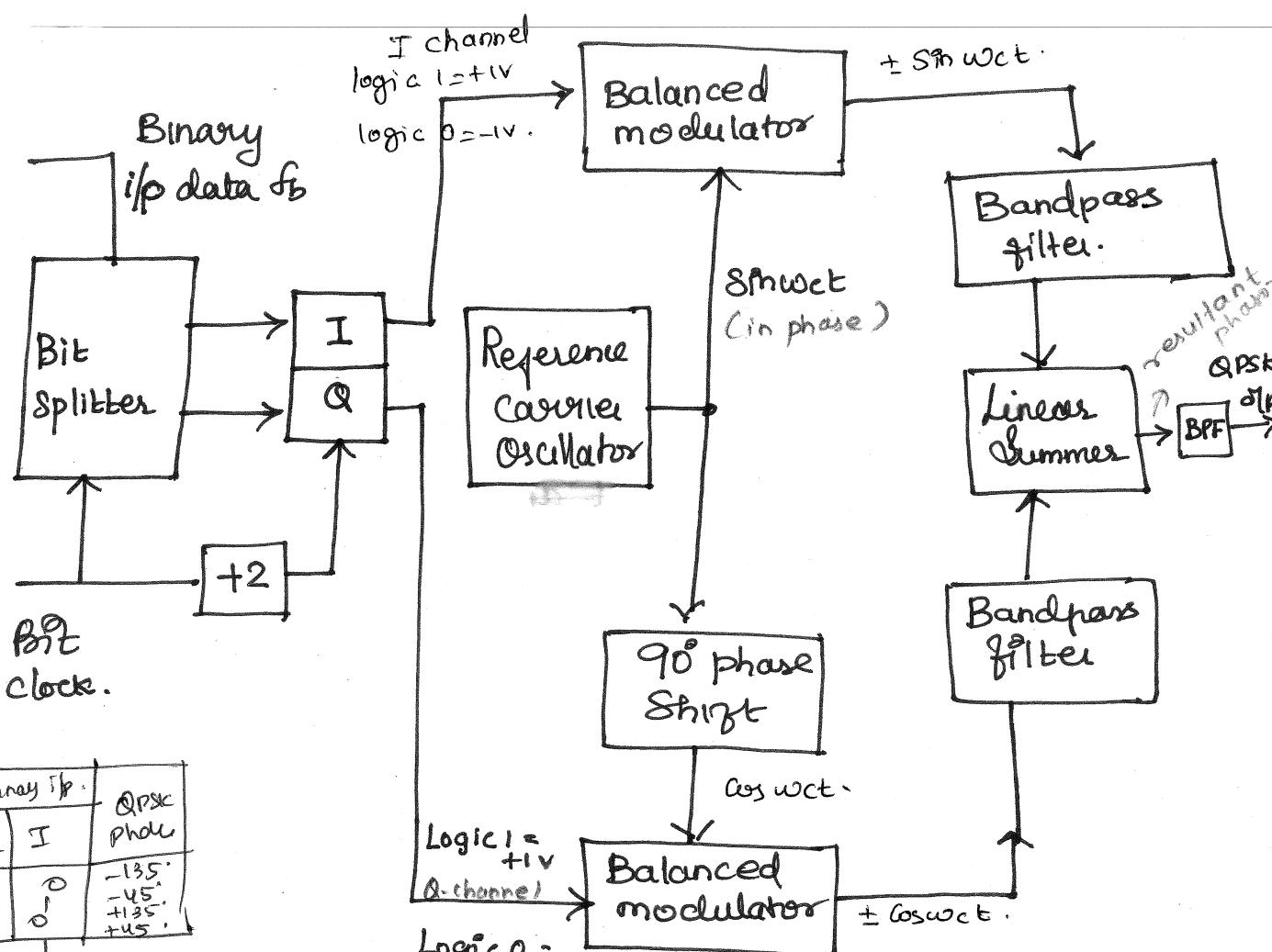
Quaternary Phase Shift Keying :-

- 1) QPSK is an N-ary encoding scheme where $N=2$ and $M=4$.
- 2) With QPSK, four output phases are possible for a single carrier frequency.
- 3) Because there are four output phases, there must be four different input conditions.
- 4) Because the digital input to a QPSK modulator is a binary signal, to produce four different input combinations the modulator requires more than a single input bit to determine the QPSK conditions.
- 5) Four possible conditions for 2 bits are, 00, 01, 10 & 11.
- 6) Binary & Input data are combined into groups of two bits, called dibits.
- 7) In modulator, each dibit code generates one of the four possible QPSK phases ($+45^\circ, +135^\circ, -45^\circ, -135^\circ$).
- 8) For each two-bit dibit clocked into the modulator, a single output change occurs, and the rate of change at the output (baud) is equal to one-half the input bit rate.

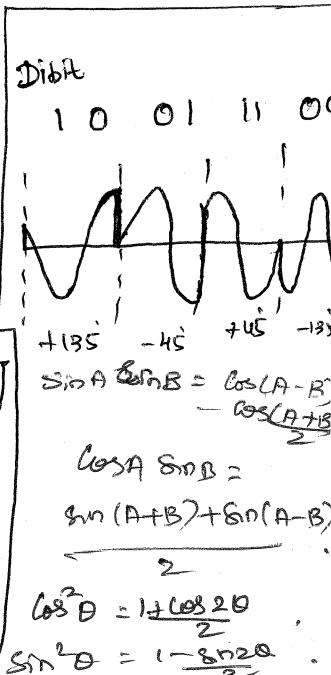
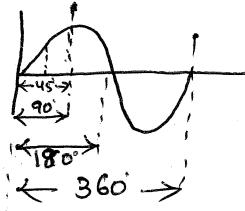
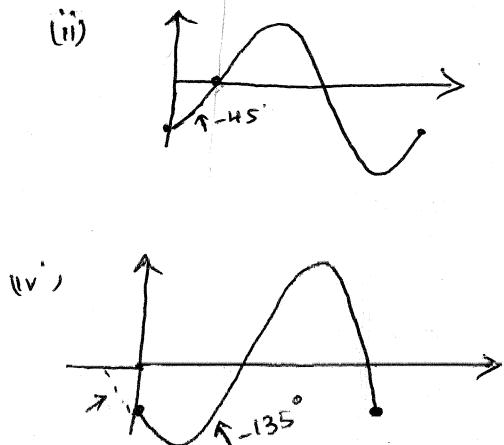
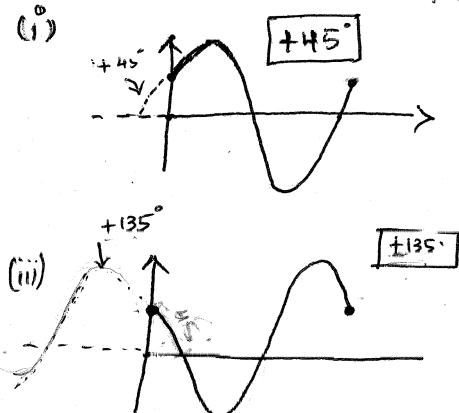
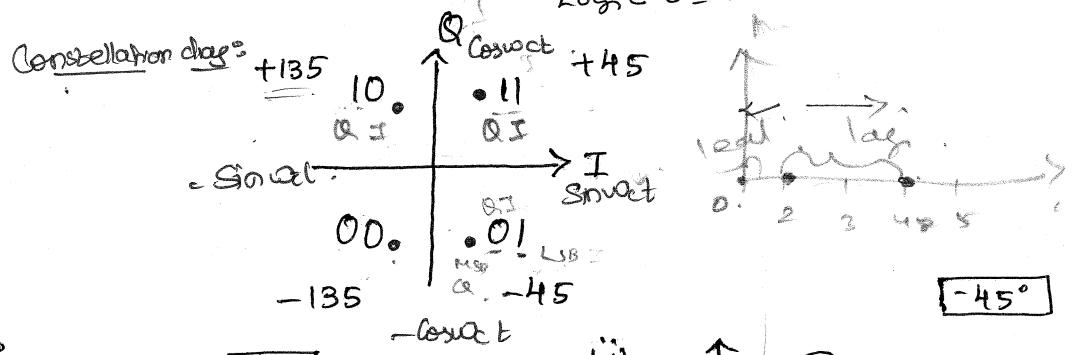
⇒ QPSK Transmitter :-

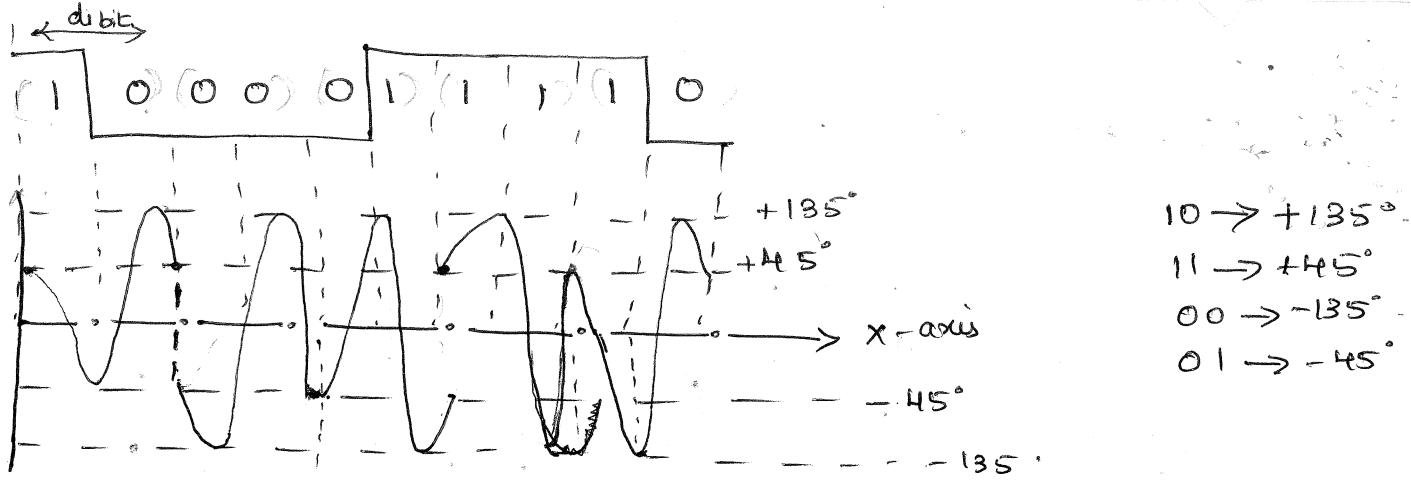
- 1) Two bits are clocked into a bit splitter. After both bits have been serially inputted, they are simultaneously parallel outputted.
- 2) One bit is directed to the I channel and the other to the Q-channel.
- 3) The I bit modulates a carrier that is in phase with the reference oscillator and the Q bit modulates

a carrier that is 90° out of phase or in quadrature with the reference carrier.



QPSK Waveform :-



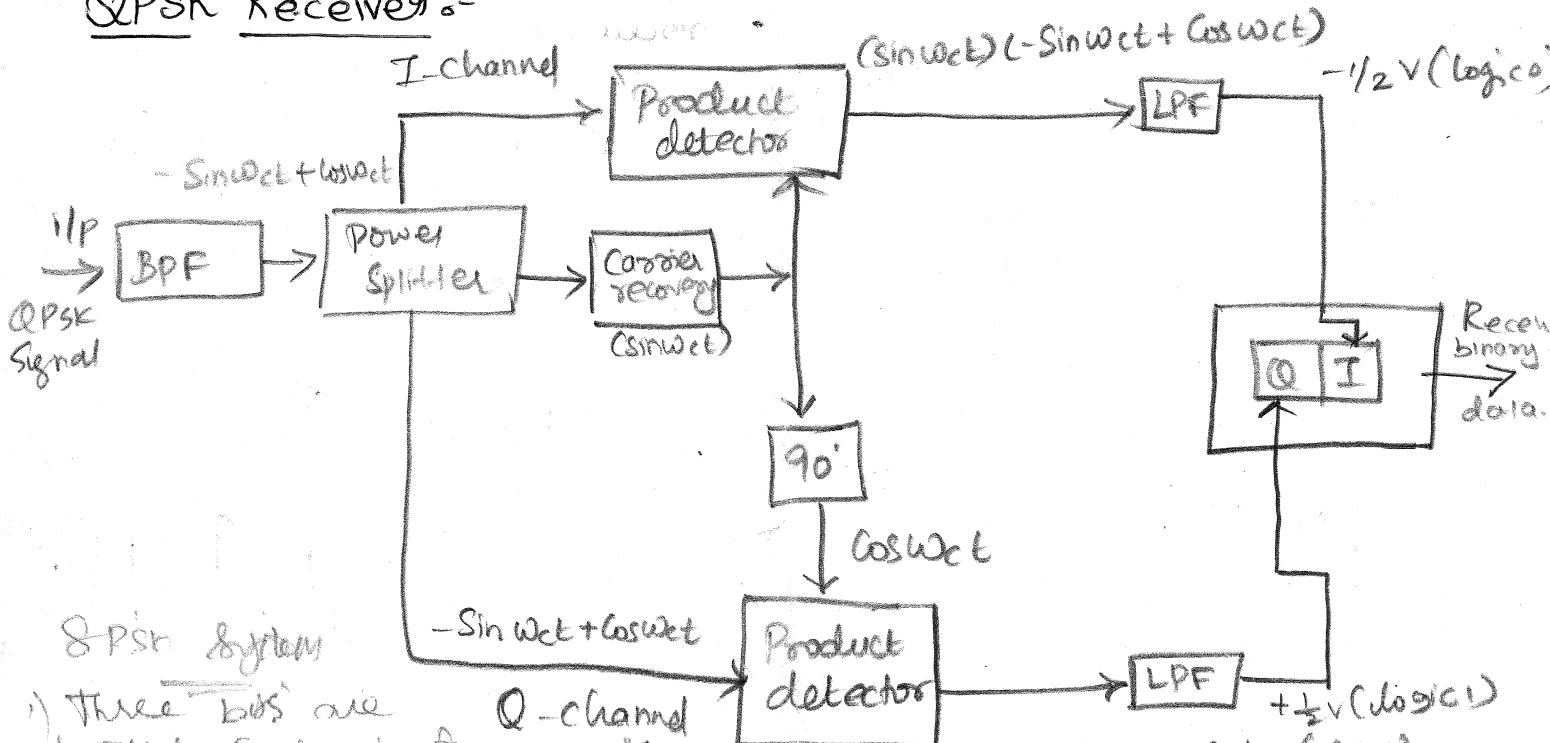


Once a bit has been split into the I and Q channels, the operation is the same as BPSK modulator for logic $1 = +IV$ and a logic $0 = -IV$, two phases are possible at the output of the Q balanced modulator ($+\cos\omega_ct$ and $-\cos\omega_ct$) and two phases for I balanced modulator ($+\cos\omega_ct$ and $-\cos\omega_ct$ ($+\sin\omega_ct$ and $-\sin\omega_ct$)). When the linear summer combines the two quadratures (90° out of phase) signals, there are four possible resultant phases by these expression signals, there are four possible resultant phases by these expression signals, there are four possible resultant phases by these expression signals.

Advantages of QPSK: Higher data rate than in PSK (2 bits/intervall).

4-PSK can easily be extended to 8-PSK i.e., n-PSK.

QPSK Receiver :-



1) Three bits are Q-channel bits brought together to form a ring.

2) There will be $2^3 = 8$ memory.

3) A PSK system that uses eight diff. phase shift to transmit 8 symbols.

It is known as 8PSK system.

QPSK Receiver:-

Let us take input QPSK signal be $(-\sin \omega_c t + \cos \omega_c t)$

The output of product detector of I is :-

$$I = (-\sin \omega_c t + \cos \omega_c t) \underbrace{\sin \omega_c t}_{\text{QPSK i/p}} + \underbrace{\cos \omega_c t}_{\text{carrier}}$$

$$= -\sin^2 \omega_c t + \cos \omega_c t \cdot \sin \omega_c t$$

$$= -\frac{1}{2} [1 - \cos 2\omega_c t] + \frac{1}{2} \sin(\omega_c t + \omega_c t) = \frac{1}{2} \sin(2\omega_c t)$$

$$= -\frac{1}{2} + \frac{\cos 2\omega_c t}{2} + \frac{1}{2} \sin(2\omega_c t) = \frac{1}{2} \sin(\omega_c t)$$

$\xrightarrow{\text{filtered out}}$ $\xrightarrow{\text{filtered out}}$ $\xrightarrow{\text{equal}}$

$$= -\frac{1}{2} V (\text{logic 0})$$

The output of product detector of Q is :-

$$Q = (-\sin \omega_c t + \cos \omega_c t) \cdot \underbrace{\cos \omega_c t}_{\text{QPSK i/p}} + \underbrace{\sin \omega_c t}_{\text{carrier}}$$

$$= -\sin \omega_c t \cdot \cos \omega_c t + \cos^2 \omega_c t$$

$$= \cos^2 \omega_c t - \sin \omega_c t \cdot \cos \omega_c t$$

$$= \left[\frac{1 + \cos 2\omega_c t}{2} \right] - \frac{1}{2} \sin(2\omega_c t) - \frac{1}{2} \frac{\sin(\omega_c t + \omega_c t)}{\sin(\omega_c t - \omega_c t)} = \frac{\sin(A+B) + \sin(A-B)}{2}$$

$$= \frac{1}{2} + \frac{\cos 2\omega_c t}{2} - \frac{\sin(2\omega_c t)}{2} - \frac{1}{2} \sin(\omega_c t)$$

$\xrightarrow{\text{filtered out}}$ $\xrightarrow{\text{filtered out}}$ $\xrightarrow{\text{equal}}$

$$= \frac{1}{2} V (\text{logic 1})$$

Note :-

$$1) \sin^2 \theta = \frac{1 - \cos 2\theta}{2}$$

$$2) \cos A \sin B =$$

$$\frac{\sin(A+B) - \sin(A-B)}{2}$$

Note ! -

$$1) \cos^2 \theta = \frac{1 + \cos 2\theta}{2}$$

or

$$\cos^2 \theta = \left(\frac{1 + \cos 2\theta}{2} \right)$$

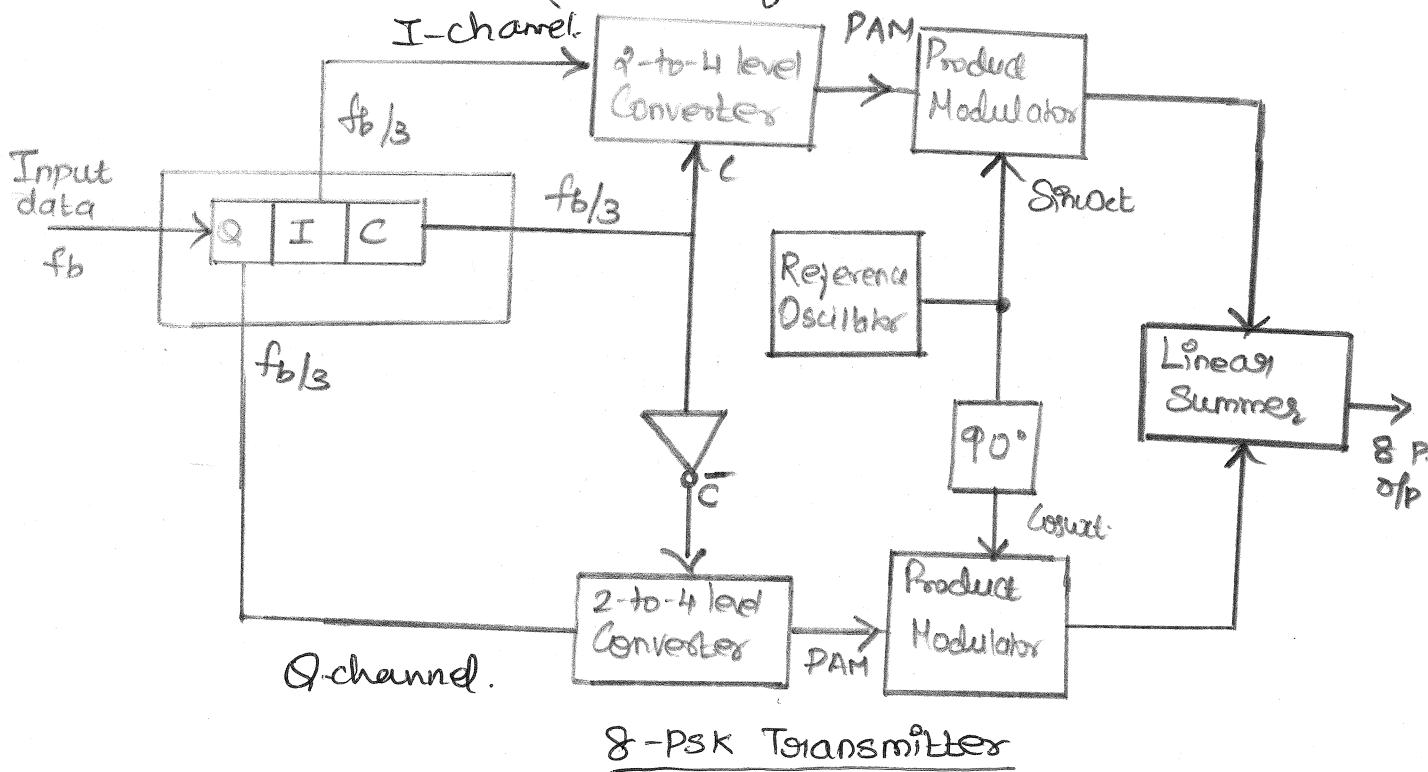
$$2) \sin A \cos B =$$

$$\frac{\sin(A+B) + \sin(A-B)}{2}$$

$\xrightarrow{\text{filtered out}}$ $\xrightarrow{\text{filtered out}}$ $\xrightarrow{\text{equal}}$

EIGHT - PHASE PSK :-

With an 8-PSK modulator, there are eight possible output phases. To encode eight different phases, the incoming bits are considered in groups of 3 bits, called tribits.



The incoming, serial bit stream enters the bit splitter, where it is converted to a parallel, three channel output (the I or in-phase channel, the Q or in-quadrature channel and C or control channel). Consequently the bit rate in each of the three channels is $f_b/3$. The bits in the I and C channel enter the I channel 2-to-4 level converter, and the bits in the Q and C channels enter the Q channel 2-to-4 level converter. 2-to-4 level converters are parallel-input digital to analog converters (DACs).

(9)

The algorithm for the DACs is quite simple.

The I or Q bit determines the polarity of the RF analog signal (logic 1 = +V and logic 0 = -V), whereas the C or \bar{C} bit determines the magnitude (logic 1 = 1.307V and logic 0 = 0.541V). Thus with two magnitudes and two polarities, four different RF conditions are possible.

Bandwidth considerations of 8-PSK with 8-PSK, because the data are divided into three channels, the bit rate in the I, Q or C channel is equal to one-third of the binary data rate ($f_b/3$).

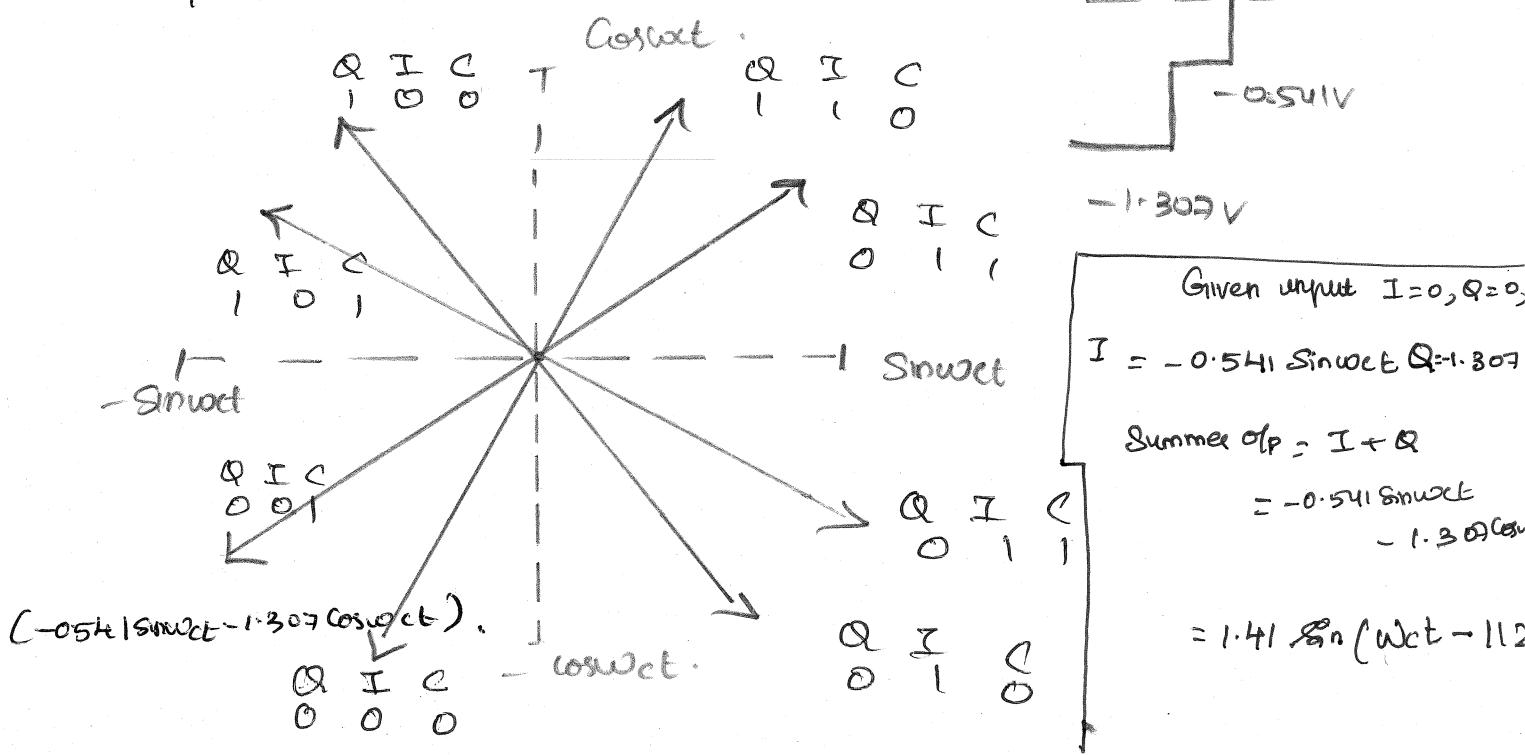
I-channel truth table

I	C	Output
0	0	-0.541V
0	1	-1.307V
1	0	+0.541V
1	1	+1.307V

Q-channel truth table.

Q	\bar{C}	Output
0	1	-1.307 V
0	0	-0.541V
1	1	+1.307
1	0	+0.541V

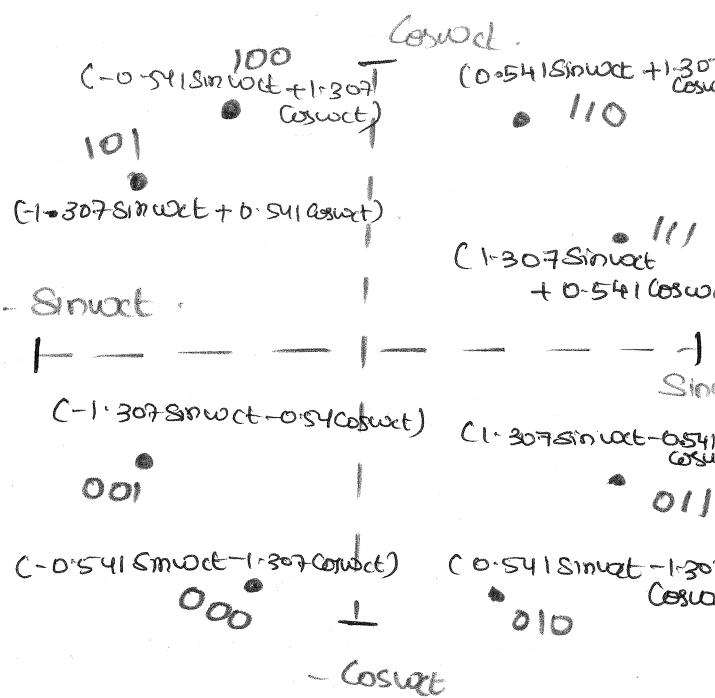
phasor diagram.



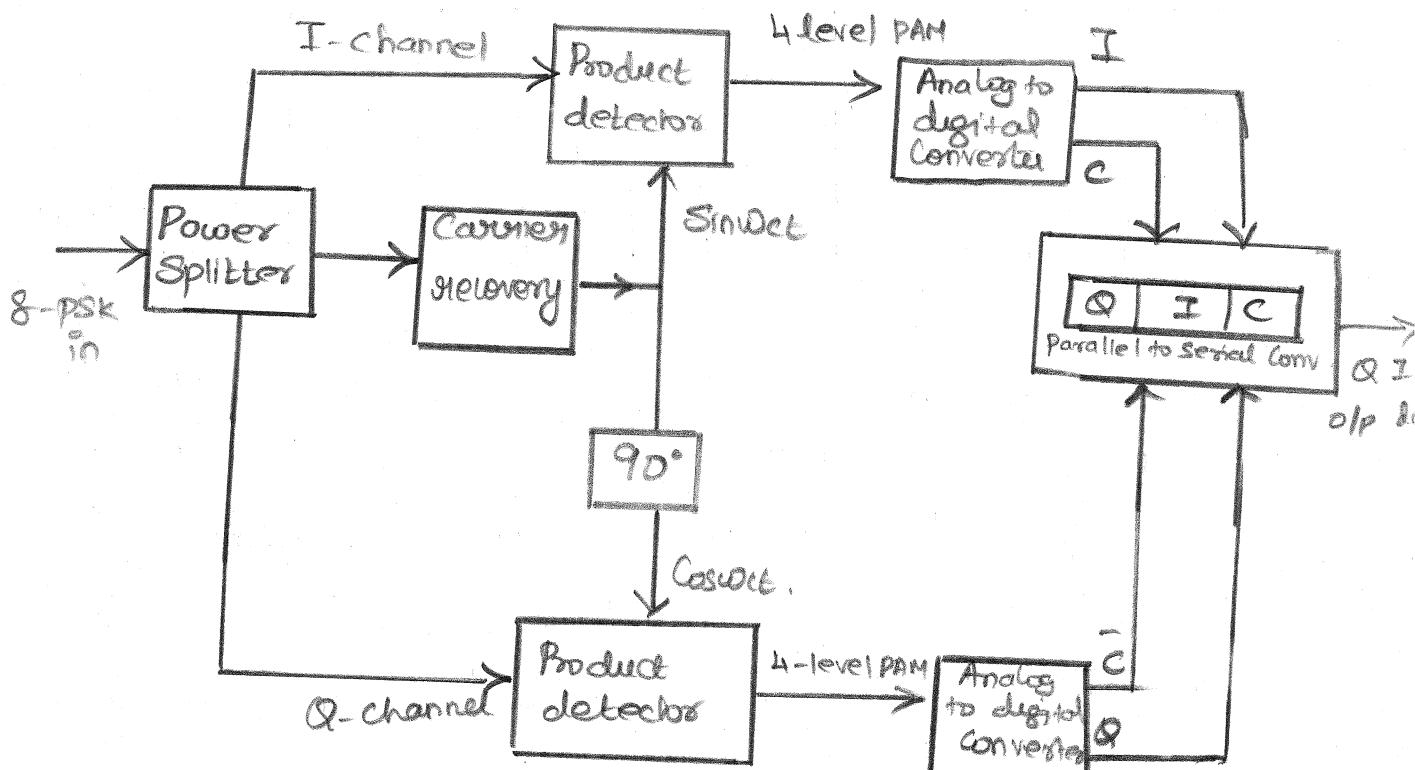
Truth table of 8-PSK modulator:-

Constellation diag :-

Binary Input			8-PSK O/p phase
Q	I	C	
0	0	0	-112.5°
0	0	1	-157.5°
0	1	0	-67.5°
0	1	1	-22.5°
1	0	0	+112.5°
1	0	1	+157.5°
1	1	0	+67.5°
1	1	1	+22.5°



8-PSK Receiver :-



- The power splitter directs the input 8-PSK signal to the I and Q product detectors and the carrier recovery circuit. The ops of the product detector and with a quadrature channel are discussed below.

- (b)
- The output of the product detectors are 4-level PAM signal that are fed to 4-to-2-level analog to digital converters (ADCs).
 - The outputs from the I-channel 4-to-2 level converter are the I and C bits, whereas the outputs from the Q-channel 4-to-2 level converter are the Q and C bits.
 - The parallel to serial logic circuit converts the I/C and Q/C bit pairs to serial Q, I and C output data streams.

For example:

Consider the received 8-PSK signal $(-0.541 \sin \omega ct - 1.307 \cos \omega ct)$

I-channel:

The output of product detector is,

$$= (-0.541 \sin \omega ct - 1.307 \cos \omega ct) \sin \omega ct.$$

$$= -0.541 \sin^2 \omega ct - 1.307 \cos \omega ct \cdot \sin \omega ct.$$

$$= -0.541 \left[\frac{1 - \cos 2\omega ct}{2} \right] - 1.307 \left[\frac{\sin(\omega ct + \omega ct) - \sin(\omega ct - \omega ct)}{2} \right]$$

$$= -\frac{0.541}{2} + \underbrace{\frac{0.541 \cos 2\omega ct}{2}}_{\text{filtered out}}$$

$$- \underbrace{\frac{1.307 \sin 2\omega ct}{2}}_{\text{filtered out}}$$

$$+ \frac{1.307 \sin(0)t}{2}$$

$$= -0.2705$$

→ equals 0

I = logic 0, C = logic 1.

Q-channel: The output of product detector is,

$$= (-0.541 \sin \omega ct - 1.307 \cos \omega ct) \cos \omega ct.$$

$$= -0.541 \sin \omega ct \cdot \cos \omega ct - 1.307 \cos^2 \omega ct.$$

$$= -0.541 \left[\frac{\sin(2\omega ct) + \sin(0)}{2} \right] - 1.307 \left[\frac{1 + \cos 2\omega ct}{2} \right]$$

$$\begin{aligned}
 &= -\frac{0.541 \sin(2\omega_0 t)}{2} - \underbrace{\frac{0.541 \sin(\omega_0 t)}{2}}_{\text{zero}} - \frac{1.307}{2} - \underbrace{\frac{1.307 \cos 2\omega_0 t}{2}}_{\text{filtered out}} \\
 &= -\frac{1.307}{2} = -0.6535.
 \end{aligned}$$

$Q = \text{logic 0}$; $\bar{C} = \text{logic 1}$.

Therefore, the received output data stream is 000. The remaining ten bits, the procedure is same.

Bandwidth Consideration for 8-PSK System :-

$$B \cdot N = \frac{f_b}{3}$$

16-PSK :

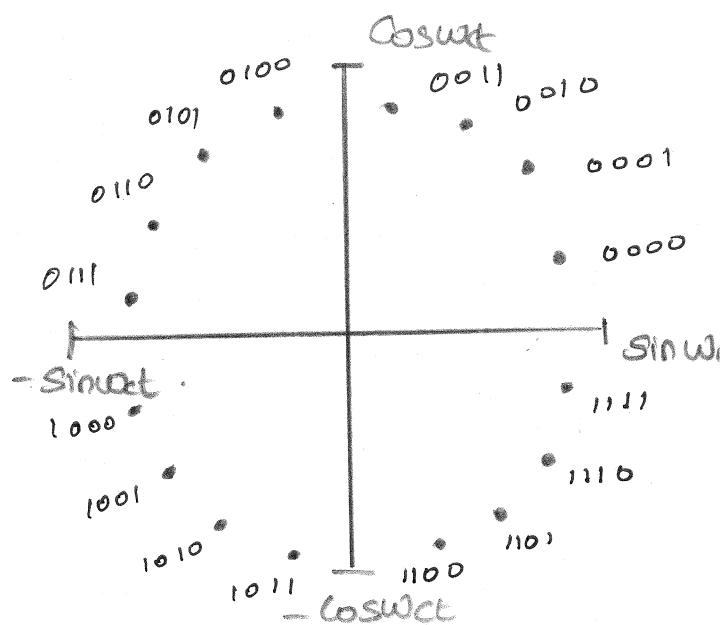
- 1) 16-PSK is an M-ary encoding technique where $M = 16$. There are 16 different output phases possible.
- 2) With 16-PSK, four bits (called quadbit) are combined, producing 16 different phases (where $n = 4$, $M = 2^n$ & $M = 16$).
- 3) The minimum bandwidth and baud equal to one-fourth the bit rate ($f_b/4$).
- 4) For 16-PSK, the angular separation between adjacent output phases is only 22.5° . Therefore 16-PSK can undergo only a 11.25° phase shift during transmission and still retain its integrity.

(11)

Truth table for 16-PSK

Bit Code	Phase
0 0 0 0	11.25°
0 0 0 1	33.75°
0 0 1 0	56.25°
0 0 1 1	78.75°
0 1 0 0	101.25°
0 1 0 1	123.75°
0 1 1 0	146.25°
0 1 1 1	168.75°
1 0 0 0	191.25°
1 0 0 1	213.75°
1 0 1 1	258.75°
1 1 0 0	284.25°
1 1 0 1	303.75°
1 1 1 0	326.25°
1 1 1 1	348.75°

Constellation diagram for 16-



QUADRATURE- AMPLITUDE MODULATION:-

- 1) In all the PSK modulation methods, one symbol is distinguished from the others in phase, but all the symbols transmitted using BPSK or QPSK (or) M-way PSK of same amplitude.
- 2) The ability of a receiver to distinguish b/w one signal vector from another in presence of noise, depends on the distance b/w the vector end points.
- 3) This suggests that the noise immunity will improve if the signal vectors differ not only in phase but also in amplitude.

Such a system is called as amplitude and phase shift keying system.

4) In this system the direct modulation of carriers in quadrature is involved, therefore this system is called (cosine & sin wave) as the quadrature amplitude phase shift keying. Also known as Quadrature Amplitude Modulation (QAM).

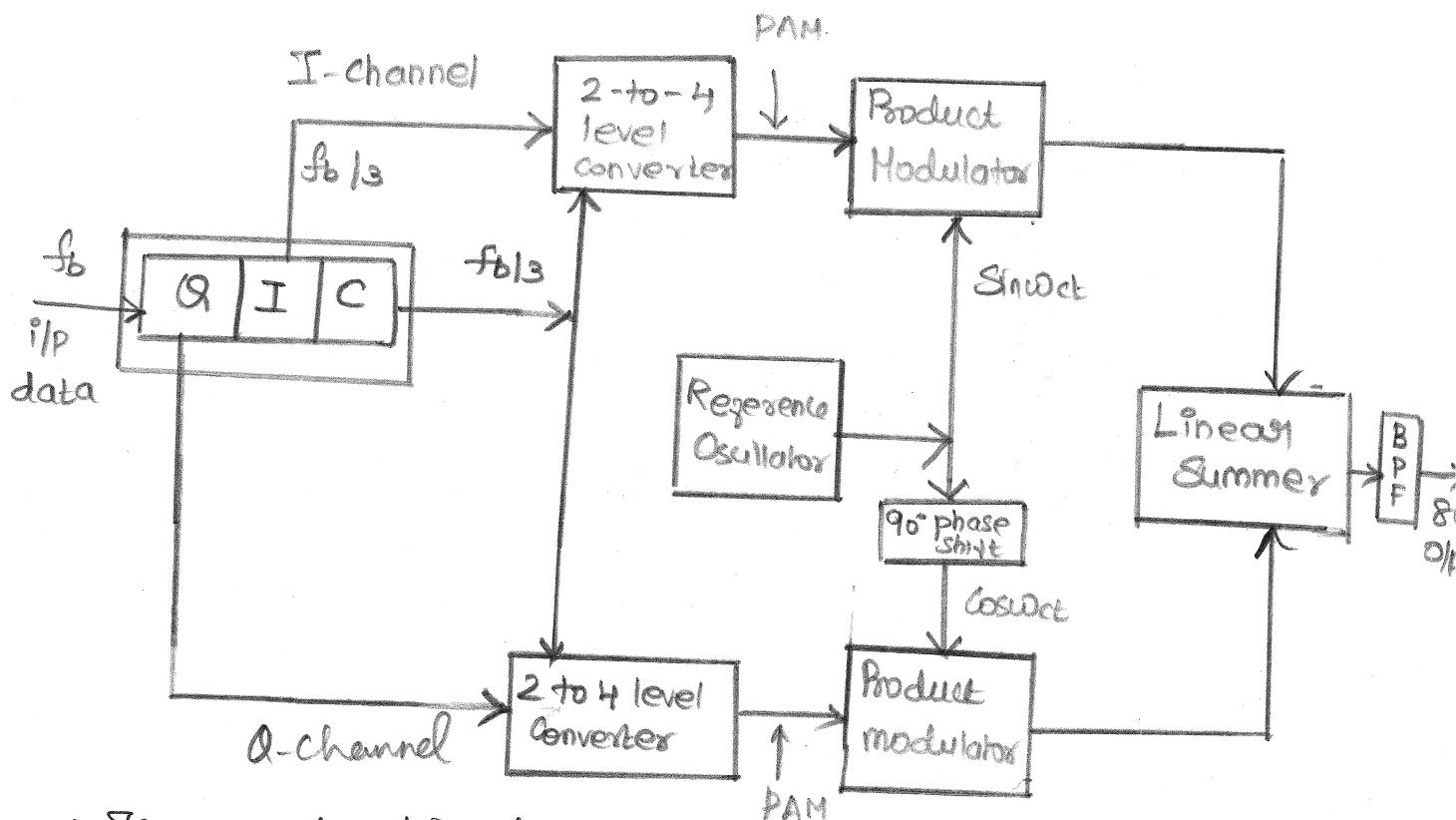
Types of QAM:

Type	Bits/symbol	Number of Symbols
4-QAM	2	$2^2 = 4$
8-QAM	3	$2^3 = 8$
16-QAM	4	$2^4 = 16$
32-QAM	5	$2^5 = 32$
64-QAM	6	$2^6 = 64$

8-QAM TRANSMITTER:

- 1) 8-QAM is an M-ary encoding technique where $M = 8$, unlike 8-PSK, the output signal from an 8-QAM modulator is not a constant amplitude signal.
- 2) The only difference b/w 8-QAM transmitter and 8-PSK transmitter is the omission of the inverter b/w C-channel and the Q-product modulator.
- 3) The incoming data are divided into groups of three bits (tritits). The I, Q and c bit streams, each with a bit rate equal to one-third of the incoming data rate ($f_b/3$)

(12) 8-QAM Transmitter Block diagram.



- 4) The I and Q bits determine the polarity of the PAM signal at the o/p of the 2-to-4 level converters and the C-bit determines the magnitude. Because the C-bit is fed uninvolved to both the I and the Q-channel, 2-to-4 level converters the magnitudes of the I and Q PAM signals are always equal.
- 5) Their polarities depends on the logic condition of the I and Q bit and therefore be different.

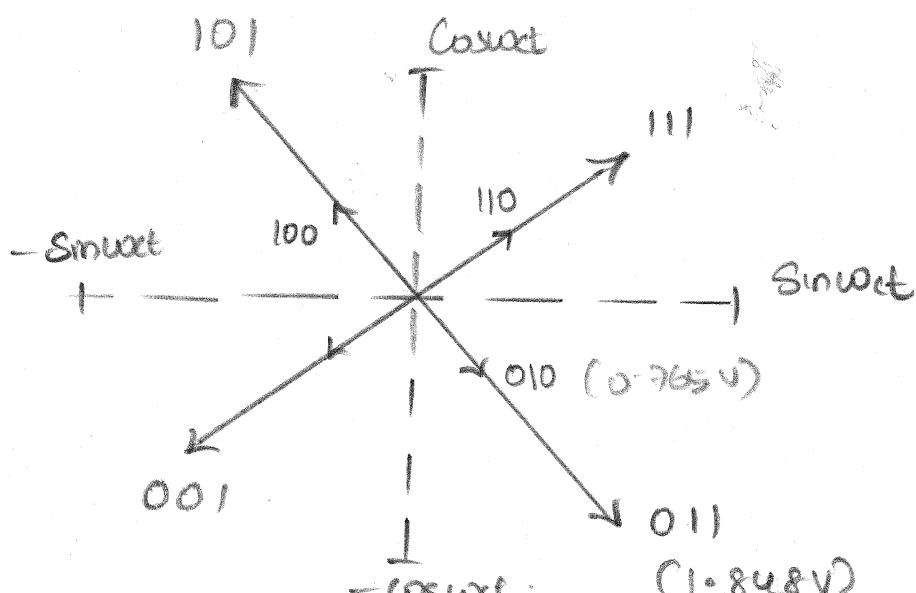
Truth table for 2-to-4 level converter

I/Q	C	Output.
0	0	-0.54V
0	1	-1.307 V
1	0	+0.541V
1	1	+1.307 V.

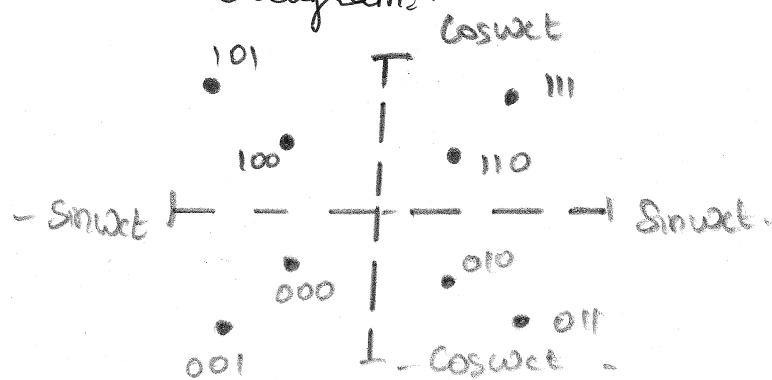
Truth table for 8-QAM transmitter :-

Binary ip			8-QAM output	
Q	I	C	Amp	Phase
0	0	0	0 - 765V	-135°
0	0	1	1 + 848V	-135°
0	1	0	0 + 765V	-45°
0	1	1	1 + 848V	-45°
1	0	0	0 + 765V	+135°
1	0	1	1 + 848V	+135°
1	1	0	0 + 765V	+45°
1	1	1	1 + 848V	+45°

Phasor diagram:-



Constellation diagram:-



for ex:- If bit stream to the bit splitter is 000

(13)

I-channel :-

The output of I channel product modulator is,

$$I = (-0.541)(\sin \omega t) = -0.541 \sin \omega t.$$

Q-channel :-

The output of Q-channel product modulator is

$$Q = (-0.541)(\cos \omega t) = -0.541 \cos \omega t.$$

$$\text{Summer output} = -0.541 \sin \omega t - 0.541 \cos \omega t$$

$$= 0.765 \sin(\omega t - 135^\circ).$$

8-QAM Receiver :

Almost identical to the 8-PSK receiver.

- 1) The differences are the PAM levels at the output of the product detectors and the binary signals at the output of the analog-to-digital converters.
- 2) With 8-QAM the binary output signals from the I-channel analog-to-digital converter are two I and Q bits, and the binary output signals from the Q-channel analog-to-digital converter are Q and C-bits.

Bandwidth required for 8-QAM is same as 8-PSK.

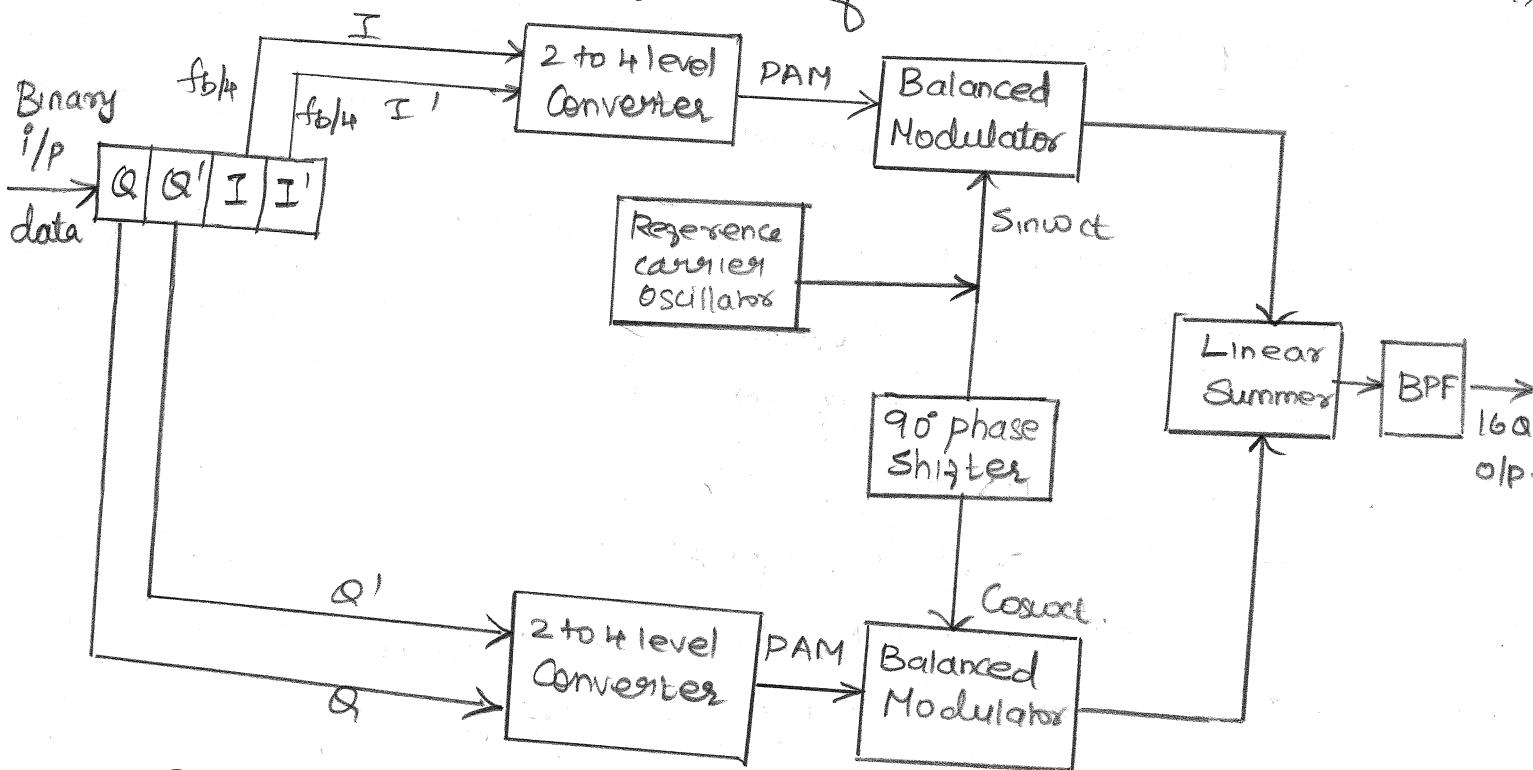
$$\text{Minimum BW} = \frac{f_B}{2},$$

16 QAM :-

As with 16-PSK, 16-QAM is an M-ary system where $M=16$. The input data are acted on in groups of four ($2^4=16$). As with 16QAM both the phase and magnitude of the transmit carrier are varied.

16-QAM Transmitter:

1) The input binary data are divided into four channels: I, I', Q, Q' . The bit rate in each channel is equal to one-fourth of the input bit rate ($f_b/4$).



Bit splitter:

Four bits are serially clocked into the bit splitter, then they are outputted simultaneously and in parallel with I, I', Q, Q' -channels.

2 to 4 level Converter: The I and Q bits determine the polarity at the o/p of the 2-to 4 level converters (a logic 1 = +ve and a logic 0 = negative). The I' and Q' bits determine

The magnitude (at logic 1 = 0.821V) and (logic 0 = 0.22V).

Consequently, the 2-to-4 level Converter generates 4-level PAM Signal for each 2-to-4 level Converters.

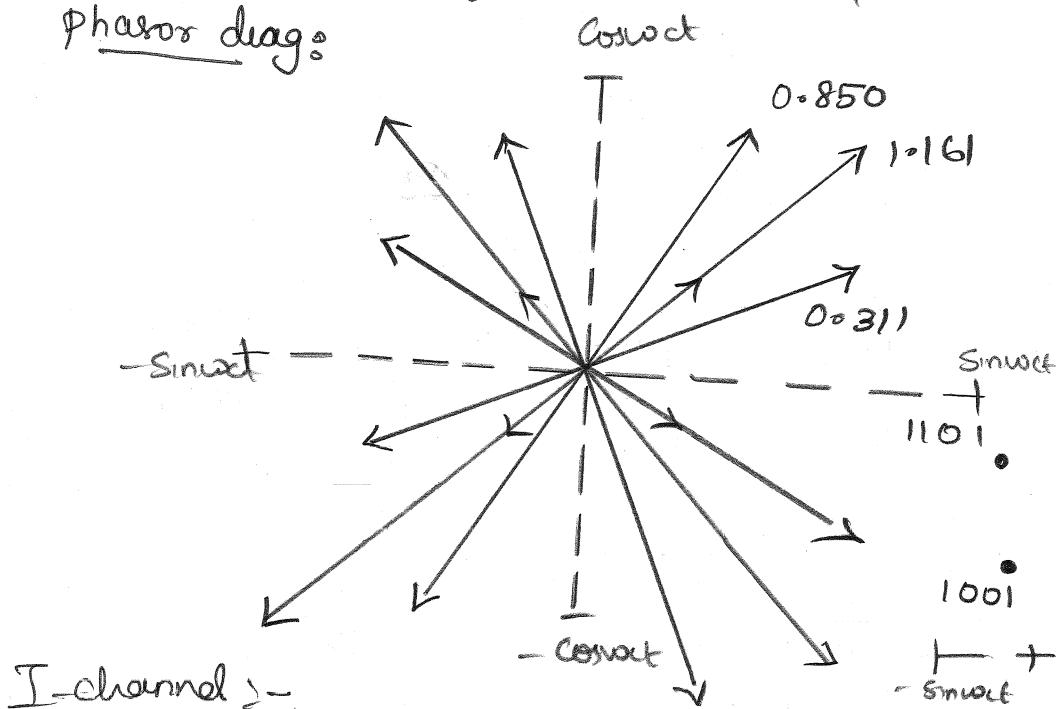
Two polarities and two magnitudes are possible at the o/p of each 2-to-4 level converter. They are $\pm 0.22\text{V}$ and $\pm 0.821\text{V}$.

For I-product modulator :-

They are $+0.821\text{Sm}^{\text{const}}$, $-0.821\text{Sm}^{\text{const}}$,
 $+0.22\text{Cos}^{\text{const}}$ and $-0.22\text{Cos}^{\text{const}}$.

Summer : Summer Combines the o/p from I and Q channel product modulators and produce the 16 o/p conditions necessary for 16-QAM.

Phasor diag:



The o/p of I. channel product modulator is :-

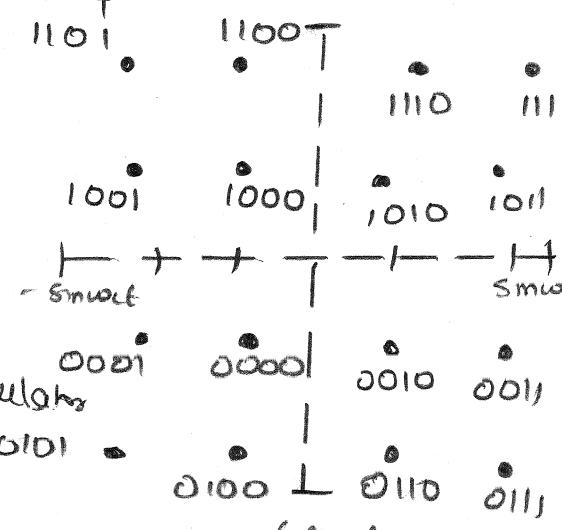
$$I = -0.22\text{Sm}^{\text{const}}$$

Q-channel :-

The o/p of Q-channel product modulator is :-

$$Q = -0.22\text{Cos}^{\text{const}}$$

Constellation diag:



Summer Opt w

$$= -0.22 \sin \omega t - 0.22 \cos \omega t$$

Bandwidth consideration of 16 QAM is $f_b/4$.

$$\text{Minimum B.W} = \frac{f_b}{4}$$

Truth table:-

Binary I/P				16-QAM O/P	
Q	Q'	I	I'		
0	0	0	0	0.311V	-135°
0	0	0	1	0.850V	-165°
0	0	1	0	0.311V	-45°
0	0	1	1	0.850V	-15°
0	1	0	0	0.850V	-105°
0	1	0	1	1.161V	-135°
0	1	1	0	0.311V	-75°
0	1	1	1	0.850V	-45°
1	0	0	0	0.311V	135°
1	0	0	1	0.850V	165°
1	0	1	0	0.850V	45°
1	0	1	1	0.311V	15°
1	1	0	0	0.850V	105°
1	1	0	1	1.161V	135°
1	1	1	0	0.850V	75°
1	1	1	1	1.161V	45°

DIFFERENTIAL BPSK (DPSK) :-

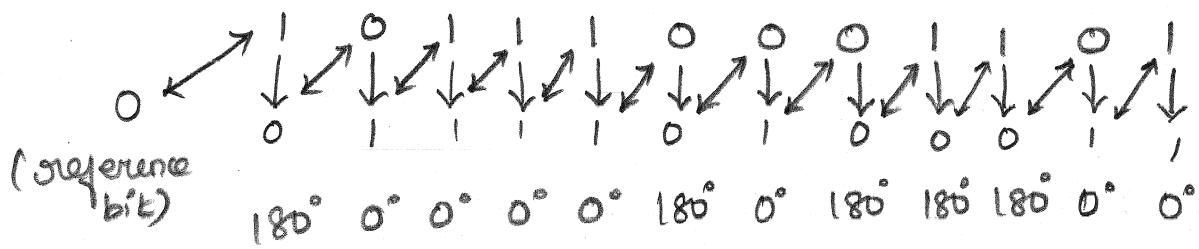
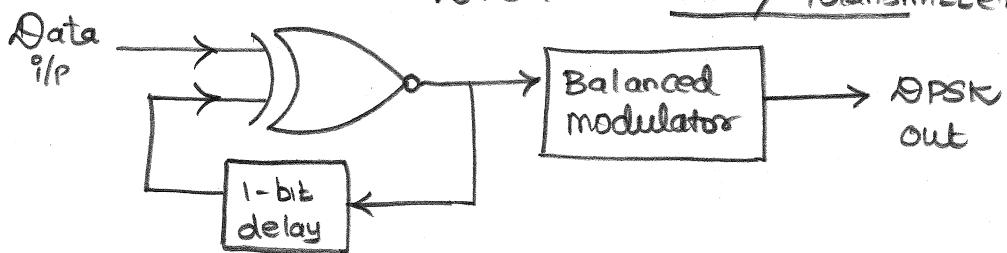
DPSK Transmitter :-

i) An incoming information bit is XNORed with the preceding bit prior to entering the BPSK modulator. For the first data bit, there is no preceding bit with which to compare it. Therefore, an initial reference bit is assumed. If the initial reference bit is assumed a logic 1, the output from the XNOR circuit is simply the complement.

ii) The first data bit is XNORed with the reference bit.

If they are the same, the XNOR o/p is a logic 1; if they are different, the XNOR o/p is a logic 0. The balanced modulator operates the same as a conventional BPSK modulator; a logic 1 produces $+ \sin \omega t$ at the output and a logic 0 produces $- \sin \omega t$ at the o/p.

DPSK Modulator / Transmitter



DBPSK Receiver :-

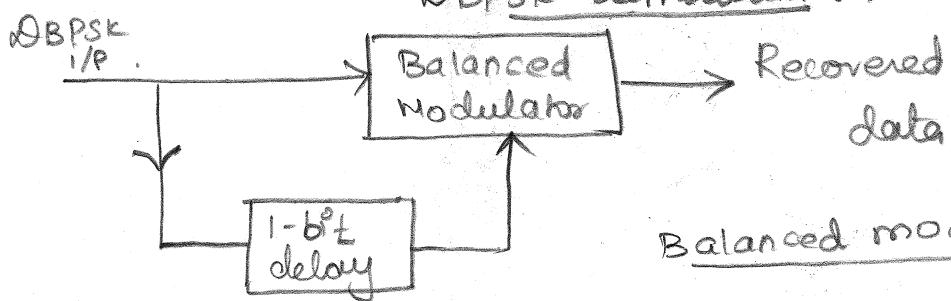
i) The received signal is delayed by one bit time, then compare with the next signaling element in the balanced modulator. If they are the same, a logic 1 (+ voltage) is generated. If they are different, a logic 0 (- voltage) is generated.

2) If the reference phase is incorrectly assumed, only the first demodulated bit is in error. Differential encoder can be implemented with higher than binary digital modulation schemes.

3) Primary advantage of QPSK is the simplicity with which it can be implemented. With QPSK, no carrier recovery circuit is needed.

4) A disadvantage of QBPSK is that it requires 6dB and 3dB more signal-to-noise ratio to achieve the same bit error rate as that of absolute PSK.

DBPSK demodulator :-



$$(+8n\omega t)(+8n\omega t) = +\frac{1}{2} - \frac{1}{2} \cos 2\omega t$$

$$(-\sin \omega t) (-\sin \omega t) = +\frac{1}{2} - \frac{1}{2} \cos 2\omega t$$

$$(-8\cos(\omega t))(-8\sin(\omega t)) = -\frac{1}{2} + \frac{1}{2}\cos(2\omega t)$$

DBPSK
Input phase

