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Anna University Exams Nov. /Dec. 2014 – Regulation 2013
 Rejinpaul.com Unique Important Questions – 3rd Semester BE/BTECH

CS6303 COMPUTER ARCHITECTURE

UNIT I

1. Define Addressing mode and explain the basic addressing modes with an example for each
2. Discuss in detail the various measures of performance of a computer
3. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.
 - a. Which processor has the highest performance expressed in instructions per second?
 - b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
 - c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?
4. Discuss the Logical operations and control operations of computer and Write short notes on Power wall
5. List and explain the developments made during different generations of computer

UNIT II

1. Explain the Multiplication algorithm in detail with diagram and examples
2. Discuss in detail about division algorithm in detail with diagram and examples
3. Design the full adder circuit and explain in detail
4. Explain floating point addition in detail with example
5. Give the algorithm for multiplication of signed 2's complement numbers and illustrate with an example

UNIT III

1. What is data hazard and control hazard? How do you overcome it? What are its side effects?
2. Discuss the influence of pipelining in detail
3. Explain dynamic branch prediction in detail
4. Explain the basic MIPS implementation of instruction set
5. With the help of a neat diagram explain the operation of data path for load instruction and R type instruction

UNIT IV

1. Explain Multi-core processors and Instruction level parallelism in detail
2. Explain the different types of multithreading
3. Explain SISD, MIMD, SIMD and SPMD
4. Explain cluster and other Message passing Multiprocessor

Unit V

1. Explain in detail about memory Hierarchy with neat diagram
2. Explain the virtual memory address translation and TLB with necessary diagram
3. Discuss the various mapping schemes used in cache design
4. Explain in detail about interrupts and I/O processor with diagram
5. Discuss the methods used to measure and improve the performance of the cache.

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