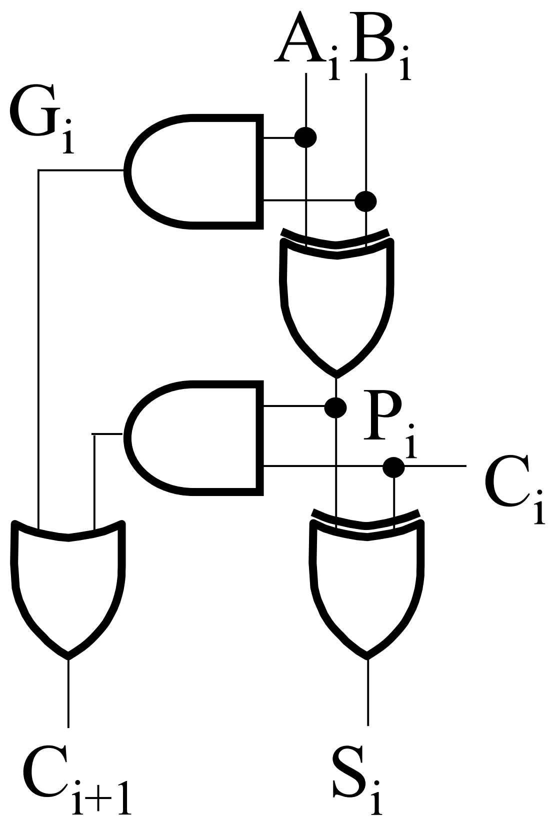
Carry Lookahead

- Given Stage i from a Full Adder, we know that there will be a carry generated when $A_i = B_i = "1"$, whether or not there is a carry-in.
- Alternately, there will be a carry propagated if the "half-sum" is "1" and a carry-in, C_i occurs.
- These two signal conditions are called *generate,* denoted as G_i, and *propagate*, denoted as P_i respectively and are identified in the circuit:



Carry Lookahead **(continued)**

- In the ripple carry adder:
  - G_i, P_i, and S_i are <u>local</u> to each cell of the adder
  - C_i is also local each cell
- In the carry lookahead adder, in order to reduce the length of the carry chain, C_i is changed to a more global function spanning multiple cells
- Defining the equations for the Full Adder in term of the P_i and G_i:

$$\mathbf{P_i = A_i \oplus B_i} \qquad \mathbf{G_i = A_i\, B_i}$$

$$\mathbf{S_i = P_i \oplus C_i} \qquad \mathbf{C_{i+1} = G_i + P_i\, C_i}$$

Carry Lookahead Development

- C_{i+1} can be removed from the cells and used to derive a set of carry equations spanning multiple cells.
- Beginning at the cell 0 with carry in C_0:

$$\mathbf{C_1 = G_0 + P_0\, C_0}$$

$$\mathbf{C_2 = G_1 + P_1\, C_1 = G_1 + P_1(G_0 + P_0\, C_0)}$$
$$\mathbf{= G_1 + P_1G_0 + P_1P_0\, C_0}$$

$$\mathbf{C_3 = G_2 + P_2\, C_2 = G_2 + P_2(G_1 + P_1G_0 + P_1P_0\, C_0)}$$
$$\mathbf{= G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0\, C_0}$$

$$\mathbf{C_4 = G_3 + P_3\, C_3 = G_3 + P_3G_2 + P_3P_2G_1}$$
$$\mathbf{+ P_3P_2P_1G_0 + P_3P_2P_1P_0\, C_0}$$

Carry Lookahead Adder

- Ripple carry adder
  - Simple but has a long circuit delay
- Define a partial full adder
- Try to lower gate delays for ripple carry adder

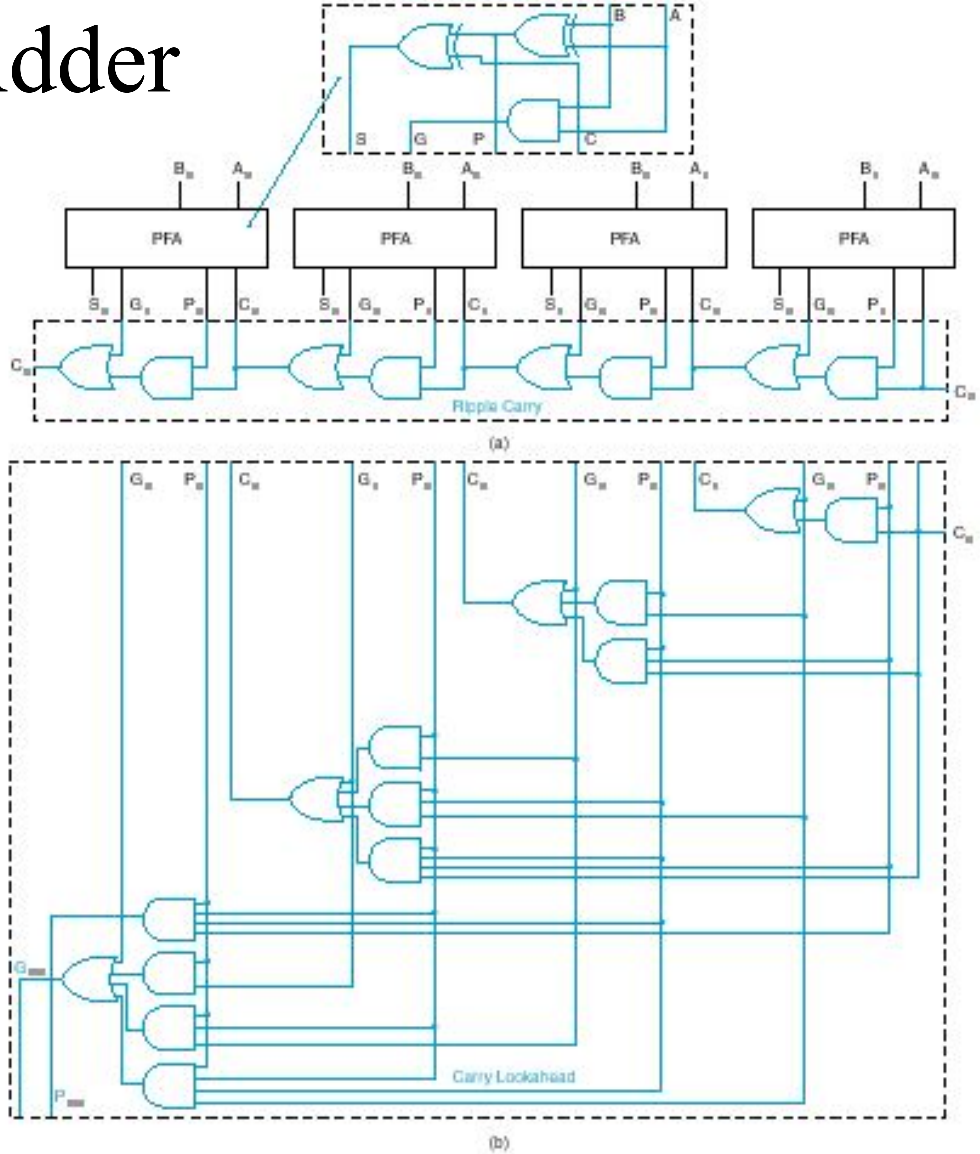


Fig. 3-29 Development of a Carry Lookahead Adder