UNIT IV - MEMORY SYSTEM

Basic concepts – Semiconductor RAM – ROM – Speed – Size and cost – Cache memories – Improving cache performance – Virtual memory – Memory management requirements – Associative memories – Secondary storage devices.

INTRODUCTION

- Programs and data that they operate in a system are stored in the memory of computer.
- The execution speed of the program is highly dependent on the speed with which instructions and data can be transferred between the processor and the memory.
- The large memory helps to execute programs that are large and deal with huge amount of data.
- Ideally, the memory would be fast, large and inexpensive. But, it's impossible to meet all the three requirements simultaneously.
- **Because increased speed and size are achieved at increased cost.**
- By improving the apparent speed and size of the memory, will help to keep the cost reasonable.
- The apparent speed can be increased by using **cache memory** and
- The apparent size can be achieved by **Virtual memory**.

I BASIC CONCEPTS OF MEMORY SYSTEMS

- The maximum size of the memory in any computer is determined by the **addressing scheme**.
- For example:
    - A 16-bit computer that generates 16-bit addresses is capable of addressing up to 2^{16}=64KB memory locations.
    - Likewise 32 –bit computer can utilize up to 2^{32} =4GB (giga) memory locations,
    - Whereas 40-bit computer can access up to 240=1T (tera) locations.

Note:

So the **number of the location represents the size of the address space** of the computer.

- Most modern computers are **byte addressable**.

There are 2 formats in byte addressable scheme:

1. The big- endian arrangement is used in 68000 processor and

2. The Little endian arrangement is used in Intel processors.

Note:

The ARM architecture can be configured to use either arrangement.

The address assignment for a byte – addressable 32-bit computer

Big-endian Arrangement

Word address	Byte address			
0	3	2	1	0
4	7	6	5	4
	.	.	.	
2^k-4	2^k-1	2^k-2	2^k-3	2^k-4

Little-endian Arrangement

Word address	Byte address			
0	0	1	2	3
4	4	5	6	7
	.	.	.	
2^k-4	2^k-4	2^k-3	2^k-2	2^k-1

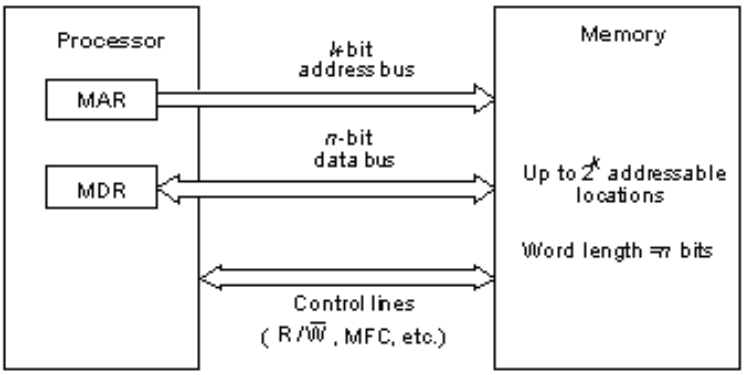
The memory is usually designed to store and retrieve data in word – length quantities. **Word length is the number of bits actually stored or retrieved in one memory access.**

Example:

- When a 32-bit address is sent from the processor to the memory unit, the *high-order 30 bits* determine which word will be accessed.
- If a byte address is specified, *the low- order 2 bits* of the address specify which byte location is involved.
- In Read operation, other bytes may be fetched from the memory, but they are ignored by the processor.
- If write operation, the control circuitry of the memory must ensure that the contents of other bytes of the same word are not hanged.

Note: Modern computer memory is complex and difficult to understand.

The connection between the processor and the memory



Data transfer between the memory and the processor takes place through the use of two processor registers:-

1. **The registers are MAR (memory address register)**
2. **MDR (memory data register).**
   - ✓ If MAR is k bits long and MDR is n bits long, then the memory unit may contain 2^k addressable locations.
   - ✓ During a memory cycle, n bits of data are transferred between the memory and the processor.
   - ✓ This transfer takes place over the processor bus, which has k address lines and n data lines. The bus has the control lines Read/ Write ($R/\overline{W}$) and MFC (memory function completed) for coordinating data transfers.
   - ✓ Other control lines may be added to indicate the number of bytes to be transferred.

The steps for data transfer between memory and the processor:

For read operation

1. The processor reads the data from the memory by loading the address of the required memory location into the MAR register and setting the(R/W) line to 1(high).
2. The memory responds by placing the data from the addressed locations onto the data lines, and conform this action by asserting the MFC signal.
3. After receipting the MFC signal, the processor loads the data on the data lines into the MDR register.

For write operation

1. The processor writes data into a memory location by loading the address of this location into MAR and loading the data into MDR. It indicates that a write operation is involved by setting the R/W lines to 0(low).
2. If read or write operations involve consecutive address locations in the main memory, then a BLOCK TRANSFER operation can be performed in which the only address sent to the memory is the one that identifies the first location.
3. Memory accesses may be synchronized using a **clock** or by using a special signal that control transfers on the bus, using the bus signaling schemes.

The speed of the memory unit is measured in terms of :-

- ✓ **Memory access time**
- ✓ **Memory cycle time**

Memory access time:

It is the time that elapses between the initiation of an operation and the completion of that operation. Example the time between read and MFC signals.

Memory cycle time:

It is the minimum time delay required between two successive memory operations. Example the time between two successive read operation.

Note:

The cycle time is usually slightly longer than the access time, depending on the implementation of memory unit.

RAM – (Random Access Memory)

- ✓ A memory unit is called RAM, if any location can be accessed for a read or write operation in some fixed amount of time that is independent of the location's address. Access time is same for all memory location.
- ✓ But in serial, partly serial, access storage devices such as magnetic disks and tapes, the access time depends on the address or position of the data.
- ✓ The basic technology for implementing the memory uses **semiconductor integrated circuits**
- ✓ The processor of a computer processes instructions and data faster than they can be fetched from a memory unit.
- ✓ The memory cycle time is the bottleneck in the system. One way to reduce the memory access time is to use a **cache memory**.

Cache memory:

It is a small, fast memory that is inserted between the larger, slower main memory and the processor. It holds the currently active segments of a program and their data.

Virtual memory:

It is another important concept related to memory organization. So far, we have assumed that the addresses generated by the processor directly specify physical locations in the memory. This may not always be the case.

- ✓ Actually data may be stored in physical memory locations that have addresses different from those specified by the program.
- ✓ The memory control circuitry translates the address specified by the program into an address that can be used to access the physical memory.
- ✓ In such a case, an address generated by the processor is referred to as a **virtual or logical address**.
- ✓ The virtual address space is mapped onto the physical memory where data are

actually stored.

- ✓ The mapping function is implemented by a special memory control circuit, often called the **memory management unit.**
- ✓ This mapping function can be changed during program execution according to system requirements.

Virtual memory: is used to increase the apparent size of the physical memory. Data are addressed in a virtual address space that can be as large as the addressing capability of the processor. But at any given time, only the active portion of this space is mapped onto locations in the physical memory.

- The remaining virtual addresses are mapped onto the bulk storage devices used, which are usually magnetic disks. As the active portion of the virtual address space changes during program execution, the memory management unit changes the mapping function and transfers data between the disk and the memory.
- Thus, during every memory cycle, an address-processing mechanism determines whether the addressed information is in the physical memory unit. If it is, then the proper word is accessed and execution proceeds.
- If it is not, a page of words containing the desired word is transferred from the disk to the memory. This page displaces some page in the memory that is currently inactive.
- Because of the time required to move pages between the disk and the memory, there is speed degradation if pages are moved frequently.
- By carefully choosing which page to replace in the memory, there may be reasonably long periods when me probability is high that the words accessed by the processor are in the physical memory unit.

II SEMICONDUCTOR RAM MEMORIES

Semiconductor memories are available in a wide range of speeds. Their cycle times range from **100 ns to less than 10ns**.

1. INTERNAL ORGANIZATION OF MEMORY CHIPS

How memory cells are organized?

Memory cells are usually organized in the form of an array, in which each cell is capable of storing one bit of information.

Example:-**I (small memory organization)**

A very small memory chip consisting of **16 words of 8 bits** each.

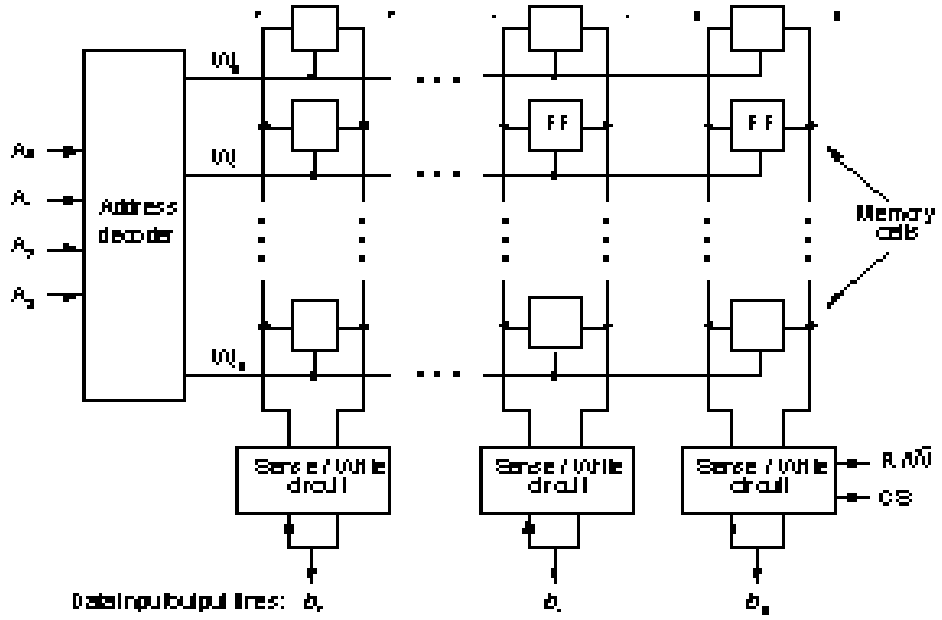
This is referred to as a **16 x 8 organization**.

- Each row of cells constitutes a memory word, and all cells of a row are connected to a common line referred to as the **word line**, which is driven by the **address decoder** on the chip.
- The cells in each column are connected to a **Sense/Write circuit** by two **bit lines**. The Sense/Write circuits are connected to the **data input/output lines** of the chip.
- The data input and the data output of each Sense/Write circuit are connected to a **single bidirectional data line** that can be connected to the data bus of a computer.
- It has
    - Two control lines:
        - R/W
        - CS
    - address lines
    - data lines.
- The **R/W (Read/Write**) input specifies the required operation
- The **CS (Chip Select)** input selects a given chip in a multichip memory system.
- The 16 x 8 organization stores 128 bits and requires **14 external connections:**
    - 4 address lines,
    - 8 data lines
    - 2 control lines(R/ W and CS) and also needs
    - Two lines for power supply and ground connections.

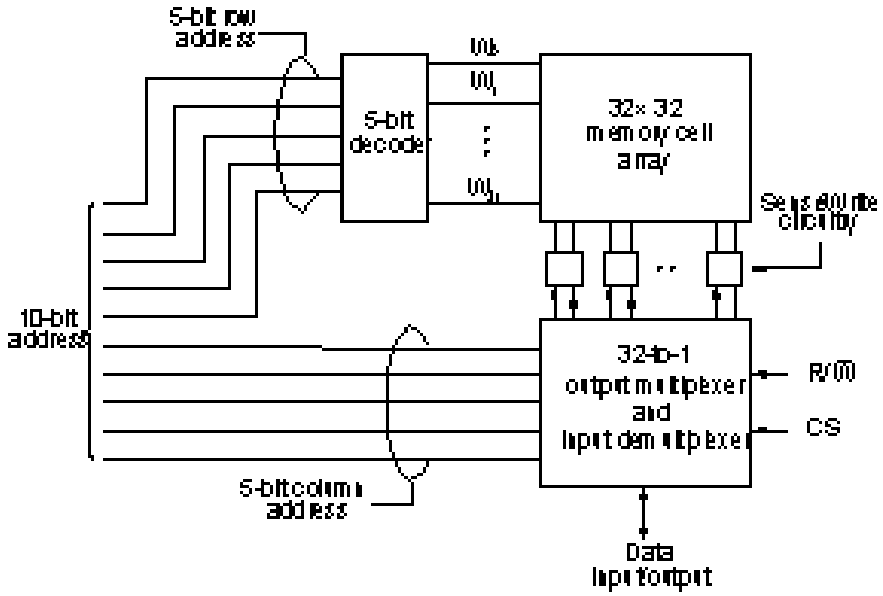
Example: II (A slightly larger memory system)

- Consider a slightly larger memory circuit, one that has **lK (1024) memory cells**.
- (i). This circuit can be organized as a **128 x 8 memory**, requiring a total of **19 external connections.**
- (ii). Suppose if the same number of cells can be organized into an **lK x 1 format**. In this case, a 10-bit address is needed, but there is only one data line, resulting in **15 external connections**.

The organization of bit cells in the memory chip



The below figure shows organization of 1K x 1 memory Chip



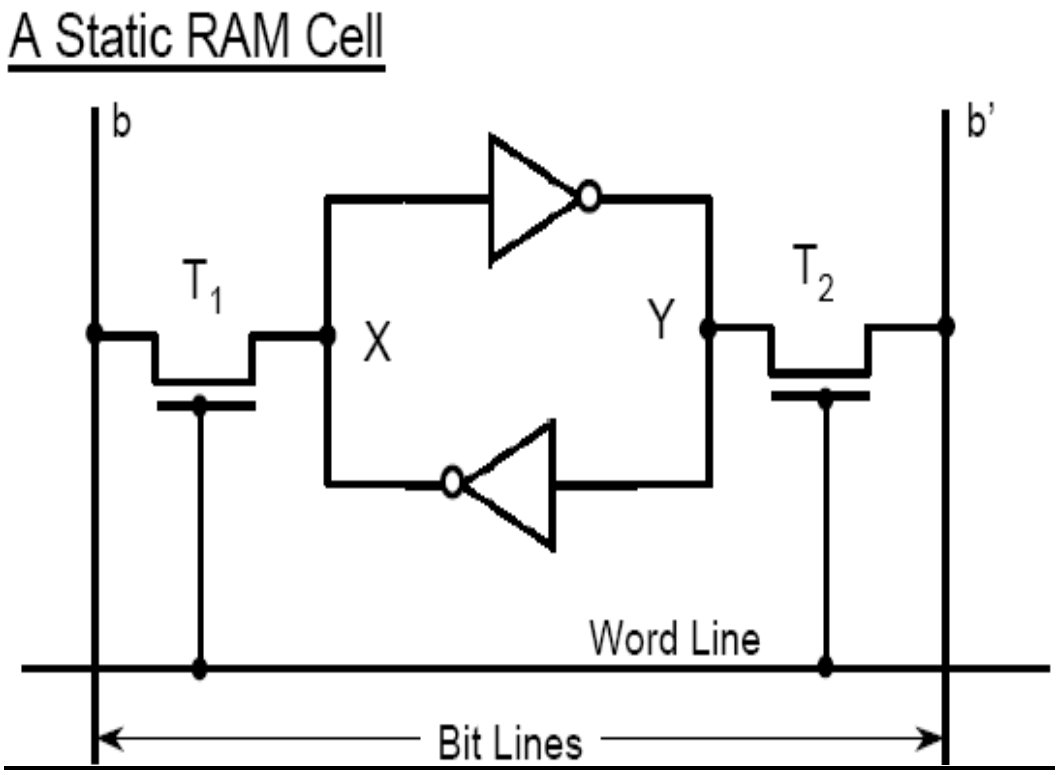
- The required 10-bit address is divided into **two groups of 5 bits each** to form the **row and column addresses** for the cell array.
  - A row address selects a row 32 cells, all of which are accessed in parallel.
  - The column address, only one of these cells is connected to the external data line by the output multiplexer and input demultiplexer.
- Commercially available memory chips contain a much larger number of memory cells. Large chips have the same organization as above 1K x 1 memory chip organization but use a larger memory cell array and have more external connections.

- For example, a 4M-bit chip may have a 5l2K x 8 organization, in which case 19 address and 8 data input/output pins are needed.

2 STATIC MEMORIES

Memories that consist of circuits capable of retaining their state as long as power is applied are known as static memories.

STATIC RAM (SRAM) CELL



- ✓ In Static memory two inverters are cross-connected to form a **latch**.
- ✓ The latch is connected to two bit lines by transistors T1 and T2.
- ✓ These transistors act as **switches** that can be opened or closed under control of the **word line**.
- ✓ When the word line is at ground level, the transistors are turned off and the latch retains its state.

For example:-, let us assume that the cell is in state 1 if the logic value at point X is 1 and at point *Y* is 0. This state is maintained as long as the signal on the word line is at ground level.

→ READ OPERATION

- ❖ In order to read the state of the SRAM cell, the word line is activated to close switches T1 and T2.
- ✓ If the cell is in state 1,

The signal on bit line *b* is high and

The signal on bit line b’ is low.

- ✓ If the cell is in state 0,(b and *b'* are complements of each other)

  The signal on bit line *b* is low and

  The signal on bit line b’ is high.

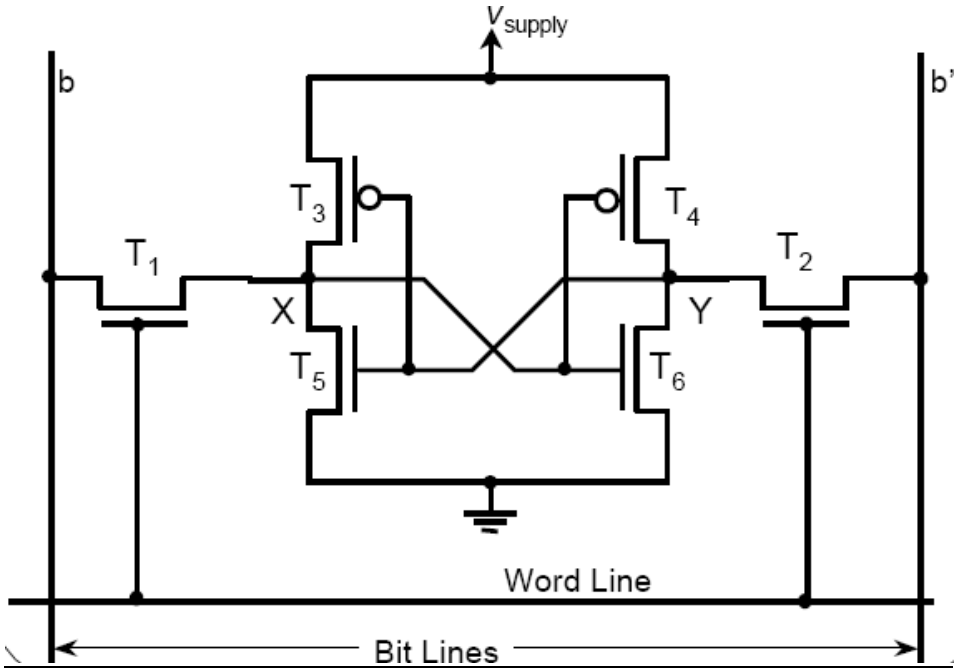
- ❖ Sense/Write circuits at the end of the bit lines monitor the state of b and b’ and set the output accordingly.

→WRITE OPERATION

- ❖ The state of the cell is set by placing the appropriate value on bit line *b* and its complement on b’, and then activating the word line.
- ❖ This forces the cell into the corresponding state. The required signals on the bit lines are generated by the Sense/Write circuit.

CMOS CELL

A CMOS realization of the above Static memory



Configuration:

- Transistor pairs (T3, T5) and (T4, T6) form the inverters in the latch.
- The state of the cell is read or written same as static memory cell. For example, in state 1, the voltage at point X is maintained high by having transistors T3 and T6 on, while T4 and Ts are off. Thus, if TI and T2 are turned on (closed), bit lines b and b' will have high and low signals, respectively.
- The power supply voltage, Vsupply,
  - is 5 V in older CMOS SRAMs or
  - 3.3 V in new low-voltage versions.

Note:

The continuous power is needed for the cell to retain its slate. If power is interrupted, the cell's contents will be lost. When power is restored, the latch will settle into a stable state, but it will not necessarily be the same state the cell was in before the interruption. Hence, SRAMs are said to be volatile memories because their contents are lost when power is interrupted.

Advantage of CMOS SRAMs:

- It consumes **very low power** because current flows in the cell only when the cell is being accessed.
- Static RAMs can be accessed very quickly. It requires very less access times in terms of few nanoseconds.

Disadvantage of CMOS SRAMs:

- Static RAMs are fast,
- High cost because their cells require several transistors.

3 . DYNAMIC RAMS

Static RAMs are fast, but they come at a high cost because their cells require several transistors. Less expensive RAMs can be implemented if simpler cells are used. However, **such cells do not retain their state indefinitely; hence, they are called dynamic RAMs (DRAMs).**

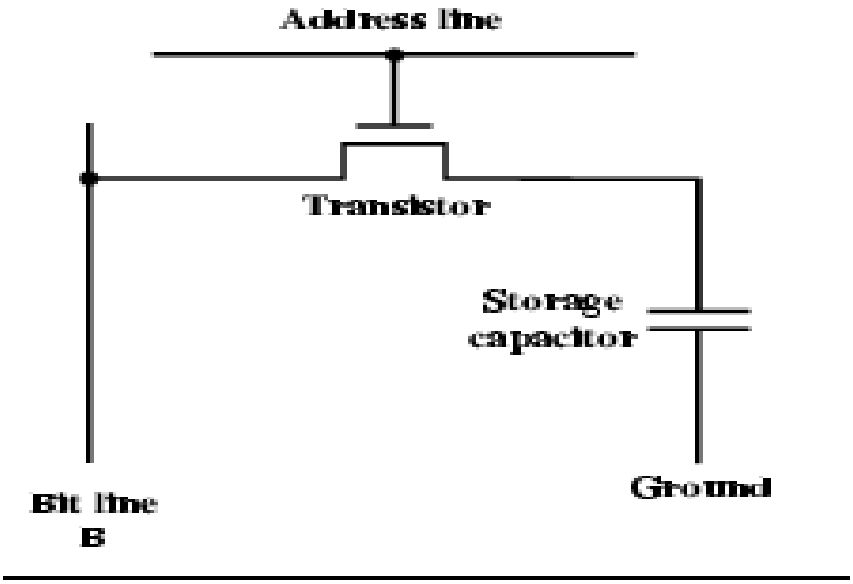
Dynamic RAMs are classified into 2,

- ✓ **ASYNCHRONOUS Dynamic RAM**
- ✓ **SYNCHRONOUS Dynamic RAM**

3.1 ASYNCHRONOUS DRAM

1. Information is stored in a dynamic memory cell in the form of a **charge on a capacitor**, and this charge can be maintained for **only tens of milliseconds**.
2. Since the cell is required to store information for a much longer time, its **contents must be periodically refreshed by restoring the capacitor charge to its full value**.

A single – transistor dynamic memory cell



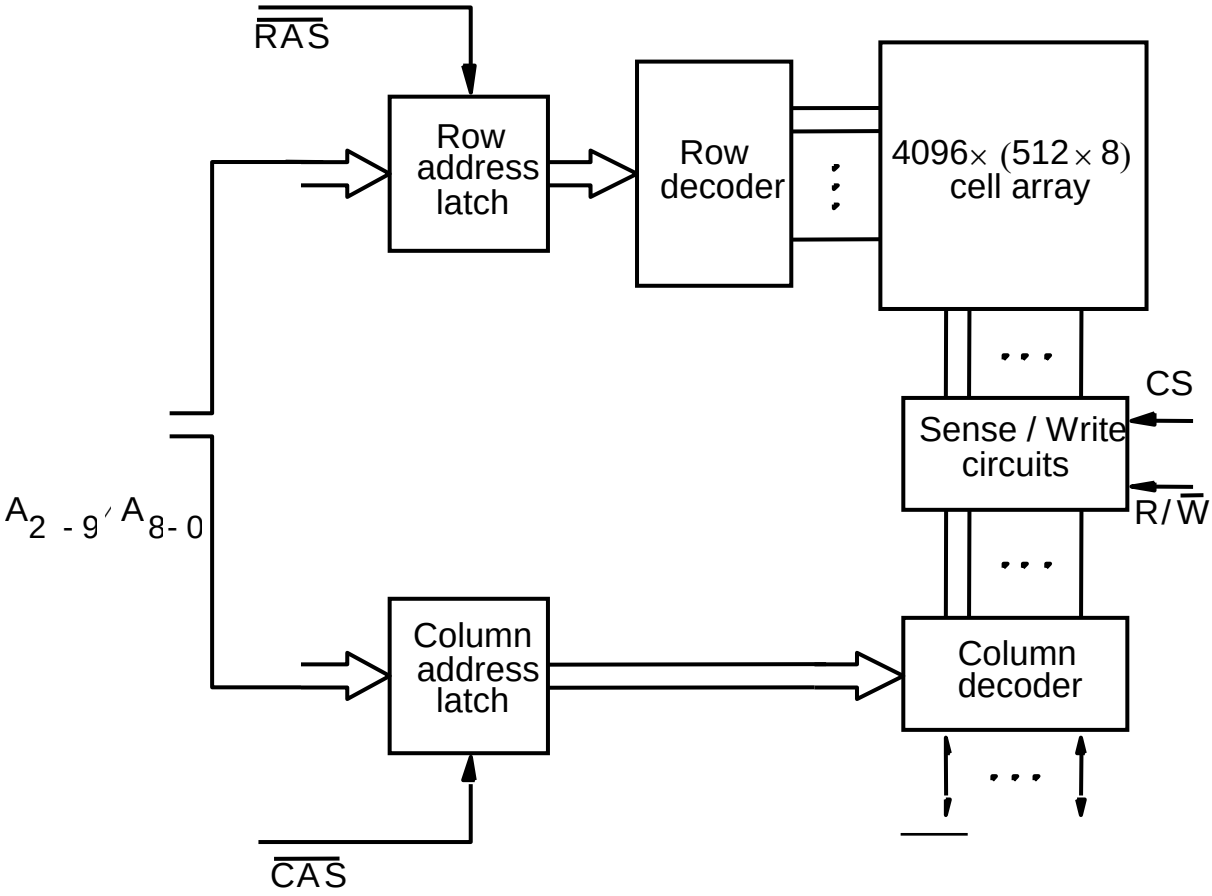
- A dynamic memory cell that consists of a capacitor, C, and a transistor, T.
- In order to **store information** in this cell, transistor T is turned on and an appropriate voltage is applied to the bit line. This causes a known amount of charge to be stored in the capacitor.
- After the transistor is **turned off, the capacitor begins to discharge**. This is caused by the capacitor's own leakage resistance and by the fact that the transistor continues to conduct a tiny amount of current, measured in **Pico amperes**, after it is turned off.
- **Hence the information stored in the cell can be retrieved correctly only if it is read before the charge on the capacitor drops below some threshold value**.

→ **During a Read operation the transistor in a selected cell is turned on**.

- A sense amplifier connected to the bit line detects whether the charge stored on the capacitor is above the threshold value.
- If so it drives the bit line to a full voltage that represents logic value 1. This voltage recharges the capacitor to the full charge that corresponds to logic value 1.
- If the sense amplifier detects that the charge on the capacitor is below the threshold value, it pulls the bit line to ground level, which ensures that the capacitor will have no charge, representing logic value 0.
- Thus, reading the contents of the cell automatically refreshes its contents.
- All cells in a selected row are read at the same time, which refreshes the contents of the entire row.

A 16-megabit DRAM chip, configured as 2M x 8 is shown below.

Internal organization of a 2M x 8 dynamic memory cell



- The cells are organized in the form of a **4K x 4K array**.
    - The 4096 cells in each row are divided into 512 groups of 8, so that a row can store 512 bytes of data.
    - Therefore, 12 address bits are needed to select a row.
    - Another 9 bits are needed to specify a group of 8 bits in the selected row.
- Thus, a 21-bit address is needed to access a byte in this memory.
    - The high-order 12 bits and
    - the low-order 9 bits of the address constitute the row and column addresses of a byte, respectively.
- **To reduce the number of pins** needed for external connections, the row and column addresses are multiplexed on 12 pins.

a Read or a Write operation:-

- The row address is applied first.
    - It is loaded into the row address latch in response to a signal pulse on the Row Address Strobe (RAS) input of the chip.
    - Then a Read operation is initiated, in which all cells on the selected

row are read and refreshed.

- Shortly after the row address is loaded, the column address is applied to the address pins and
    - It is loaded into the column address latch under control of the Column Address Strobe (CAS) signal.
    - The information in this latch is decoded and the appropriate group of 8 Sense/Write circuits is selected.

→***Read operation***

If the R/W control signal indicates a Read operation, the output values of the selected circuits are transferred to the data lines, D7-D0.

→***Write operation:-***

The information on the D7-D0 lines is transferred to the selected circuits. This information is then used to overwrite the contents of the selected cells in the corresponding 8 columns.

- Applying a row address causes all cells on the corresponding row to be read and refreshed during both Read and Write operations. To ensure that the contents of a DRAM are maintained, each row of cells must be accessed periodically.
- A **refresh circuit** usually performs this function automatically. Many dynamic memory chips incorporate a refresh facility within the chips themselves. Here, the dynamic nature of these memory chips is almost invisible to the user.

DRAM: the timing of the memory device is controlled asynchronously. A specialized memory controller circuit provides the necessary control signals, RAS and CAS that govern the timing. The processor must take into account the delay in the response of the memory. Such memories are referred to as asynchronous DRAMs.

Advantage of DRAMs :

High density and low cost, DRAMs are widely used in the memory units of computers.

Note:

Available chips range in size from 1M to 256M bits, and even larger chips are being developed. To reduce the number of memory chips needed in a given computer, a DRAM chip is organized to read or write a number of bits in parallel. To provide flexibility in designing memory systems, these chips are manufactured in different organizations. For example, a 64-Mbit chip may be organized as 16M x 4, 8M x 8, or 4M x 16.

FAST PAGE MODE:

When the DRAM in above Figure is accessed, the contents of all 4096 cells in the selected row are sensed, but only 8 bits are placed on the data lines D7-D0. This byte is selected by the column address bits A8-A0.

A simple modification can make it possible to access the other bytes in the same row without having to reselect the row. A latch can be added at the output of the sense amplifier in each column. The application of a row address will load the latches corresponding to all bits in the selected row. Then, it is only necessary to apply different column addresses to place the different bytes on the data lines.

The most useful arrangement is to transfer the bytes in sequential order, which is achieved by applying a consecutive sequence of column addresses under the control of successive CAS signals. This scheme allows transferring a block of data at a much faster rate than can be achieved for transfers involving random addresses. The block transfer capability is referred to as the fast page mode feature.

Advantage of Fast page mode:

The faster rate attainable in block transfers can be exploited in applications in which memory accesses follow regular patterns, such as in graphics terminals.

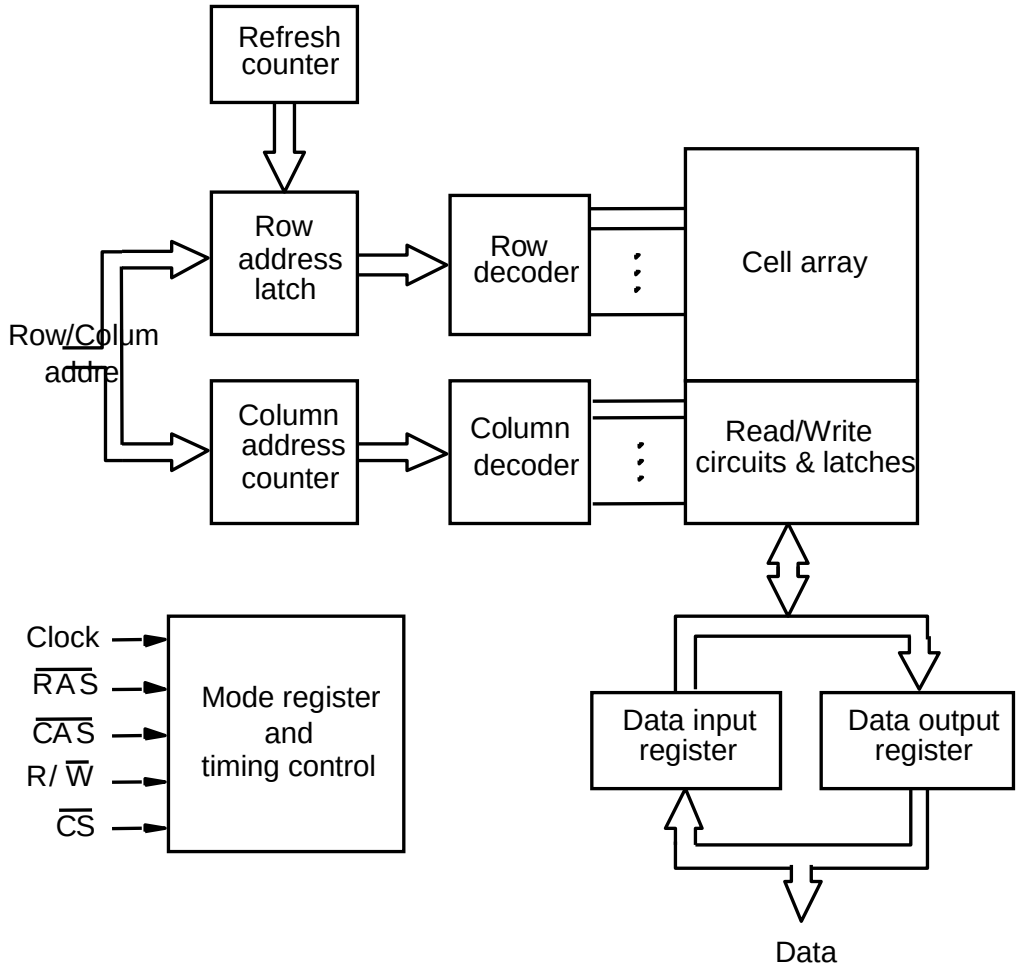
This feature is also beneficial in general-purpose computers for transferring data blocks between the main memory and a cache.

3.2 SYNCHRONOUS DRAMS

DRAMs operation is directly synchronized with a clock signal. Such memories are known as synchronous DRAMs (SDRAMs).

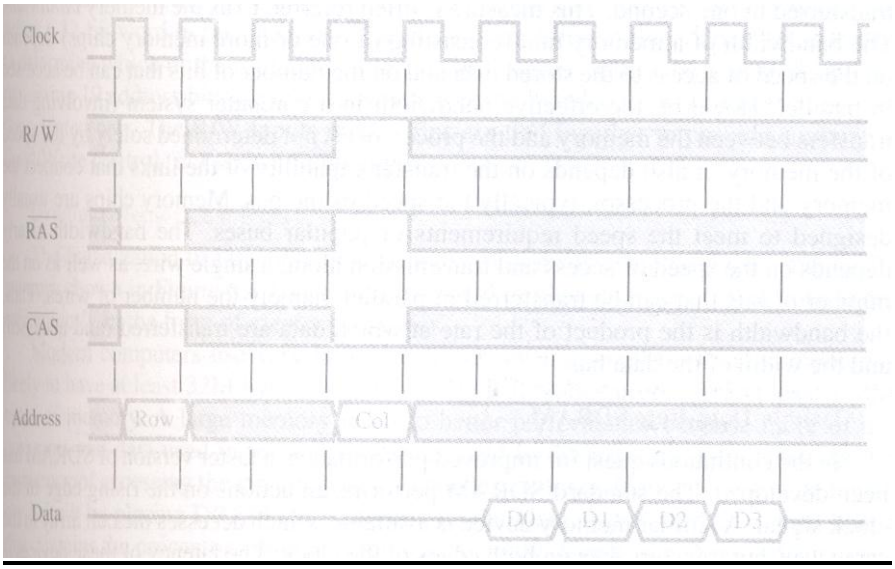
- The cell array is the same as in asynchronous DRAMs. The address and data connections are buffered by means of registers.
- The output of each sense amplifier is connected to a latch.
- A Read operation causes the contents of all cells in the selected row to be loaded into these latches. But, if an access is made for refreshing purposes only, it will not change the contents of these latches; it will merely refresh the contents of the cells.
- Data held in the latches that correspond to the selected column(s) are transferred into the data output register, thus becoming available on the data output pins.
- SDRAMs have several different modes of operation, which can be selected by writing control information into a mode register.

Structure of a Synchronous DRAM



- In SDRAMs, it is not necessary to provide externally generated pulses on the CAS line to select successive columns. The necessary control signals are provided internally using a column counter and the clock signal. New data can be placed on the data lines in each clock cycle. All actions are triggered by the rising edge of the clock.
- The burst operation is used for the block transfer of data as fast page mode feature. It is specified by setting the mode register.
- First, the row address is latched under control of the RAS signal. The memory typically takes 2 or3 clock cycles to activate the selected row. Then, the column address is latched under control of the CAS signal.
- After a delay of one clock cycle, the first set of data bits is placed on the data lines. The SDRAM automatically increments the column address to access the next three sets of bits in the selected row, which are placed on the data lines in the next 3 clock cycles.

A timing diagram for a typical burst read of length 4 in an SDRAM



- SDRAMs have built-in refresh circuitry. A part of this circuitry is a refresh counter, which provides the addresses of the rows that are selected for refreshing. **In a typical SDRAM, each row must be refreshed at least every 64 ms.**
- Commercial SDRAMs can be used with clock speeds above 100 MHz. These chips are designed to meet the requirements of commercially available processors.

For example, Intel has defined PC 100 and PC 133 bus specifications in which the system bus (to which the main memory is connected) is controlled by a 100 or 133, MHz clock, respectively. Therefore, major manufacturers of memory chips produce 100 and 133 MHz SDRAM chips.

Latency and Bandwidth:

Transfers between the memory and the processor involve single words of data or small blocks of words to or from the processor caches.

Large blocks, constituting a page of data, are transferred between the memory and the disks. The speed and efficiency of these transfers have a large impact on the performance of a computer system.

A good indication of the performance is given by two parameters:

- ✓ Latency
- ✓ Bandwidth.

The term **memory latency** is used to refer to the amount of time it takes to transfer a word of data to or from the memory.

In the case of reading or writing a single word of data, the latency provides a complete indication of memory performance. But, in the case of burst operations that transfer a block of data, the time needed to complete the operation depends also on the rate at which

successive words can be transferred and on the size of the block.

In block transfers, the term latency is used to denote the time it takes to transfer the first word of data. This time is usually substantially longer than the time needed to transfer each subsequent word of a block.

Consider in the above timing diagram, the access cycle begins with the assertion of the RAS_signal. The first word of data is transferred five clock cycles later. Thus, the latency is five clock cycles. If the clock rate is 100 MHz, then the latency is 50 ns. The remaining three words are transferred in consecutive clock cycles.

When transferring blocks of data, it is of interest to know how much time is needed to transfer an entire block. Since blocks can be variable in size, it is useful to define a performance measure in terms memory bandwidth.

Memory bandwidth:

It is defined as the number of bits or bytes that can be transferred in one second.

The bandwidth of a memory unit depends on the speed of access to the stored data and on the number of bits that can be accessed in parallel.

The effective bandwidth in a computer system is not only determined by the speed of the memory. It also depends on the transfer capability of the links that connect the memory and the processor, typically the speed of the bus.

The bandwidth is mainly depends on the

- ✓ Speed of access and transmission along a single wire
- ✓ The number of bits that can be transferred in parallel (number of wires)

So the bandwidth is the product of the rate at which data are transferred (and accessed) and the width of the data bus.

Double – data rate SDRAM (DDR SDRAM)

The standard SDRAM performs all actions on the rising edge of the clock signal.

The SDRAM, which accesses the cell array for transfers of data on both edges of the clock signal is called double – data rate SDRAMs. The latency of these devices is same as for standard SDRAMs. But, they transfer data on both edges of the clock. Such devices is called double – data- rate SDRAMs. Their bandwidth is doubled for long burst transfers.

Application of DDR SDRAM and Standard SDRAMs:

Mainly used in the application where block transfers are established. Some examples are,

- ✓ Used in general purpose computers in which transfer is mainly between main memory and processor caches.
- ✓ Used in high - quality video displays.

III. STRUCTURE OF LARGER MEMORIES

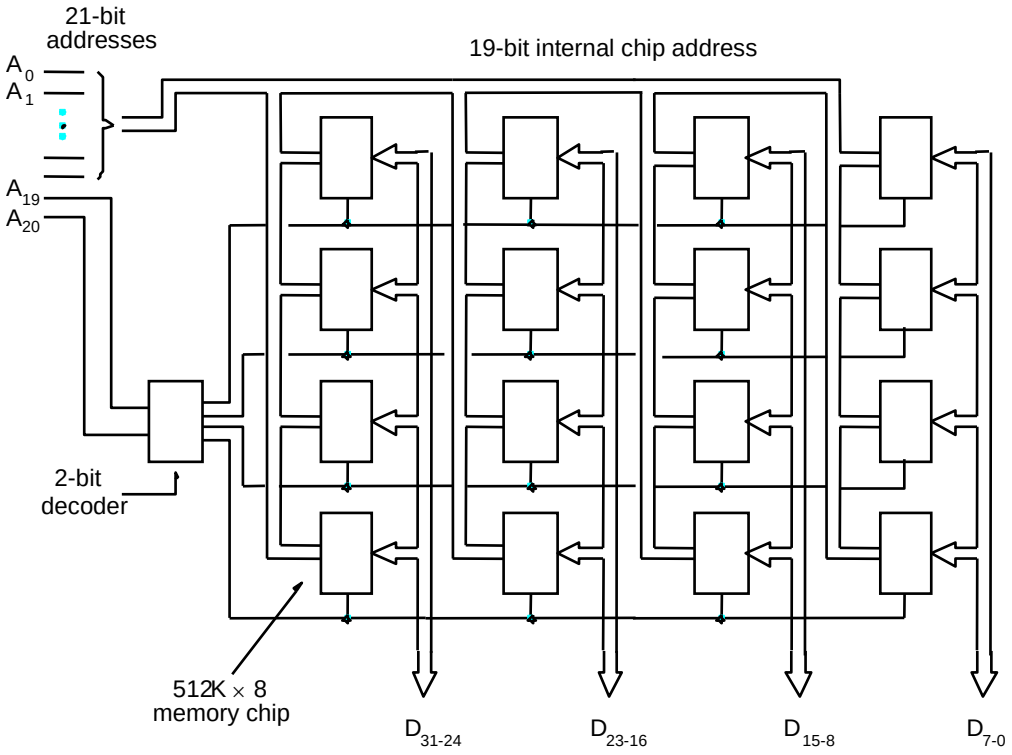
How memory chips may be connected to form a much larger memory.

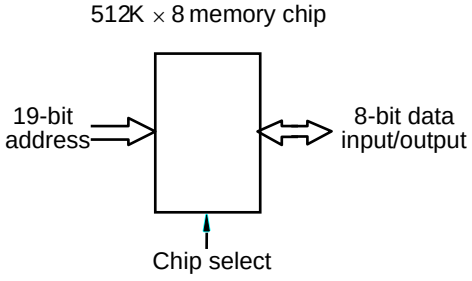
Static Memory System

Consider a memory consisting of 2M (2,097,152) words of 32 bits each. This can be implemented using 512K x 8 static memory chips as shown below in the diagram.

- Each column in the diagram consists of four chips, which implement one byte position.
- Four of these sets provide the required 2M x 32 memory.
- Each chip has a control input called Chip Select. When this input is set to 1, it enables the chip to accept data from or to place data on its data lines.

Organization of a 2M x 32 memory module using 512K x 8 static memory chips





- The data output for each chip is of the three-state type. Only the selected chip places data on the data output line, while all other outputs are in the high-impedance state. Twenty one address bits are needed to select a 32-bit word in this

memory.

- The high-order 2 bits of the address are decoded to determine which of the four Chip Select control signals should be activated and the remaining 19 address bits are used to access specific byte locations inside each chip of the selected row.
- The R/W inputs of all chips are tied together to provide a common Read /Write control as shown in the diagram.

Dynamic memory systems:

The physical implementation of memory systems is done more conveniently in the form of **memory modules.**

Advantages of large memory:

Modern computers use very large memories. A large memory leads to better performance because more of the programs and data used in processing can be held in the memory, thus reducing the frequency of accessing the information in secondary storage.

Demerits of large memory:

If a large memory is built by placing DRAM chips directly on the main system printed-circuit board that contains the processor, often referred to as a **motherboard**, it will occupy an unacceptably large amount of space on the board.

It is also uncomfortable to provide for future expansion of the memory, because space must be allocated and wiring provided for the maximum expected size.

These can be overcome by packaging in the form of memory modules. The different memory modules are

- ✓ SIMM*s* (Single In-line Memory Modules)
- ✓ DIMMs (Dual In-line Memory Modules)

Such a module is an assembly of several memory chips on a separate small board that plugs vertically into a single socket on the motherboard.

SIMMs and DIMMs of different sizes are designed to use the same Size socket.

For example, 4M x 32, 16M x 32, and 32M x 32 bit DIMMs all use the same 100-pin socket. Similarly, 8M x 64, 16M x 64, 32M x 64, and 64M x 72 DIMMs use l68-pin socket.

Such modules (both SIMM and DIMM) occupy a smaller amount of space on a motherboard, and they allow easy expansion by replacement if a larger module uses the same socket

IV. MEMORY SYSTEMS CONSIDERATIONS

The factors to be considered for choosing of a RAM chip for a given application depends on

- ✓ Cost
- ✓ Speed
- ✓ Power dissipation
- ✓ Size of the chip.

Static RAMs are generally used in the application where very fast operation is required. But the cost and size will be increased as the complexity of the circuit increases. They are used mostly in cache memories.

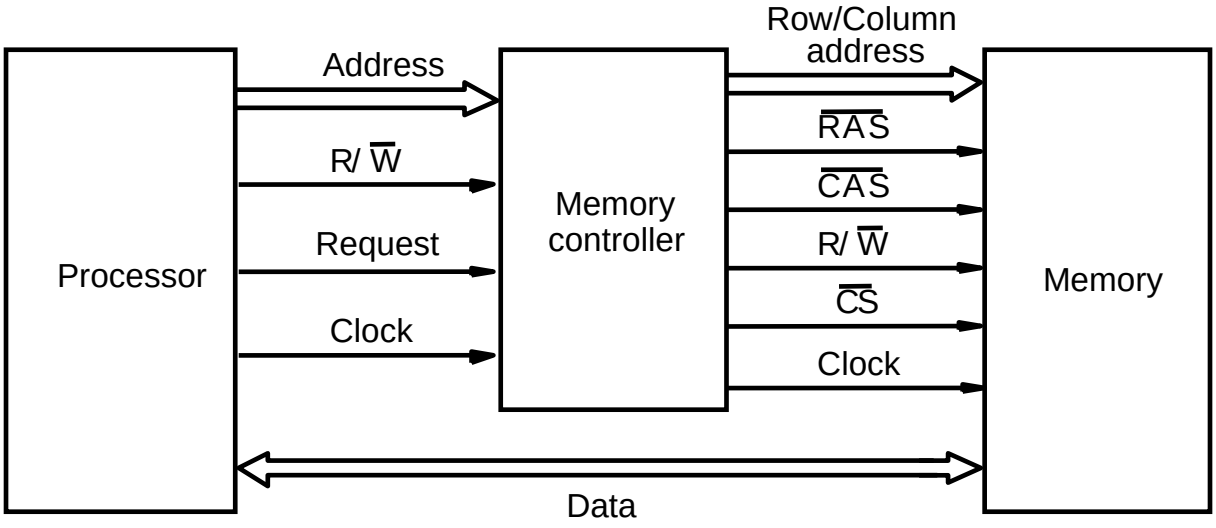
Dynamic RAMs are the mainly used for implementing computer main memories. The high densities achievable in these chips make large memories economically feasible.

To reduce the number of pins, the dynamic memory chips use multiplexed address inputs. The address is divided into two parts.

- ✓ The high-order address bits, which select a row in the cell array, are provided first and latched into the memory chip under control of the RAS signal.
- ✓ Then, the low-order address bits, which select a column, are provided on the same address pins and latched using the CAS signal.

A typical processor issues all bits of an address at the same time. The required multiplexing of address bits is usually performed by a **memory controller circuit,** which is inserted between the processor and the dynamic memory as shown in the diagram below.

Interposing of memory controller between memory and the processor



- ➢ The controller accepts a complete address and the R/W signal from the processor, under the control of a Request signal which indicates that a memory access

operation is needed.

- The controller then forwards the row and column portions of the address to the memory and generates the RAS and CAS signals. Thus, the controller provides the RAS-CAS timing, in addition to its address multiplexing function.
- It also sends the R/W and CS signals to the memory. The CS signal is usually active low; hence it is shown as CS in the diagram.
- Data lines are connected directly between the processor and the memory.
- The clock signal is needed for SDRAM chips.

When used with DRAM chips, which do not have self-refreshing capability, the memory controller has to provide all the information needed to control the refreshing process. It contains a refresh counter that provides successive row addresses. Its function is to cause the refreshing of all rows to be done within the period specified for a particular device.

Refresh overhead

All dynamic memories have to be refreshed. In older DRAMs, a refreshing period for all rows was 16 ms. In SDRAMs, it is 64 ms.

Consider an SDRAM whose cells are arranged in 8K (=8192) rows. Suppose that it takes four clock cycles to access (read) each row. Then, it takes 8192 x 4 = 32,768 cycles to refresh all rows.

At a clock rate of 133 MHz, the time needed to refresh all rows is

32,768 / (133 x 10^6) = 246 x 10^{-6} seconds. Thus, the refreshing process occupies 0.246 ms in each 64-ms time interval. Therefore, the refresh overhead is 0.246/64 = 0.0038, which is less than 0.4 percent of the total time available for accessing the memory.

RAMBUS MEMORY

A very wide bus is expensive and requires a lot of space on a motherboard; an alternative approach is to implement a narrow bus that is much faster. This approach was used by Rambus Inc. to develop a proprietary design known as **Rambus.**

Rambus provides a complete specification for the design of such communication links, called the Rambus channel.

V. READ ONLY MEMORIES

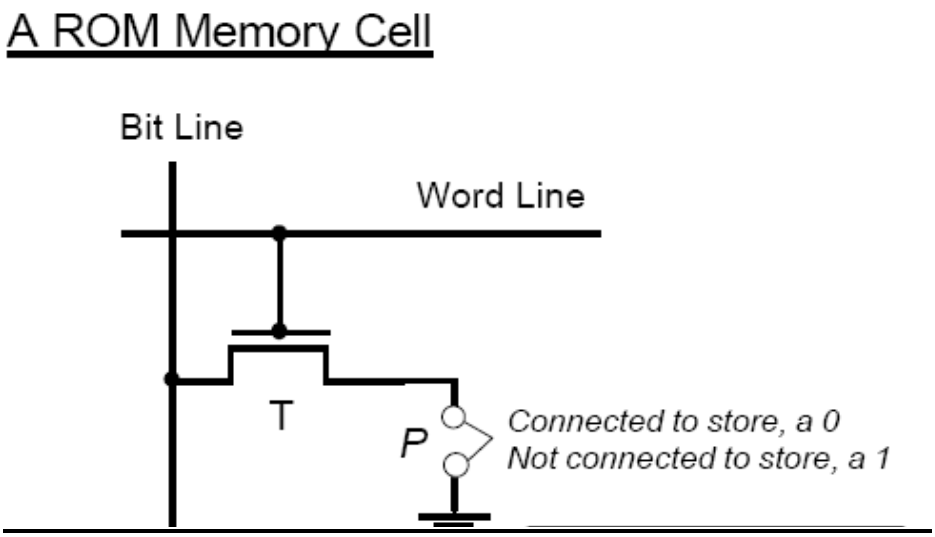
Introduction:

- Both SRAM and DRAM chips are volatile, which means that they lose the stored information if power is turned off.
- There are many applications that need memory devices which retain the stored information if power is turned off. For example, in a typical computer a hard disk drive is used to store a large amount of information, including the operating system software.
- When a computer is turned on, the operating system software has to be loaded from the disk into the memory. This requires execution of a program that "boots" the operating system. Since the boot program is quite large, most of it is stored on the disk.
- The processor must execute some instructions that load the boot program into the memory. If the entire memory consisted of only volatile memory chips, the processor would have no means of accessing these instructions.
- A practical solution is to provide a small amount of nonvolatile memory that holds the instructions whose execution results in loading the boot program from the disk.
- Nonvolatile memory is used extensively in embedded systems. Such systems typically do not use disk storage devices. Their programs are stored in nonvolatile semiconductor memory devices.
- Different types of nonvolatile memory have been developed. Generally, the contents of such memory can be read as if they were SRAM or DRAM memories. But, a special writing process is needed to place the information into this memory. Since its normal operation involves only reading of stored data, a memory of this type is called read-only memory (ROM).

1. ROM – Read Only Memory

- A logic value 0 is stored in the cell if the transistor is connected to ground at point P; otherwise, a 1 is stored
- The bit line is connected through a resistor to the power supply.
- To read the state of the cell, the word line is activated.
- Thus, the transistor switch is closed and the voltage on the bit line drops to near zero, if there is a connection between the transistor and ground.
- If there is no connection to ground, the bit line remains at the high voltage, indicating a 1.
- A sense circuit at the end of the bit line generates the proper output value.

Data are written into a ROM when it is manufactured.



Advantages of ROM:

1. Non-volatile memory (data will not be erased after the power is turned off)

Disadvantages of ROM:

1. Data are written into a ROM when it is manufactured.
2. Not allow the data to be loaded by the programmer (user).

2. PROM – Programmable ROM

- PROM designs allow the data to be loaded by the user.
- Programmability is achieved by inserting a fuse at point P.
- Before it is programmed, the memory contains all 0s.
- The user can insert 1s at the required locations by **burning out the fuses** at these locations using high-current pulses.

Advantage of PROM over ROM

- ✓ PROMs provide more **flexibility and convenience** in storing the data.
- ✓ They are economically attractive for storing fixed programs and data when high volumes of ROMs are produced.
- ✓ PROMs provide a **faster and considerably less expensive** approach because they can be programmed directly by the user.

Disadvantages of PROM

1. The cost of preparing the masks needed for storing a particular information pattern in ROMs makes them **very expensive** when only a small number are required.

3. EPROM – Erasable Programmable ROM

- ➢ The ROM chip, which allows the stored data to be erased and new data to be loaded,

such an erasable, **reprogrammable ROM** is usually called an EPROM.

- It provides considerable flexibility during the development phase of digital systems.
- Since EPROMs are capable of **retaining stored information for a long time**, they can be used in place of ROMs while software is being developed. In this way, memory changes and updates can be easily made.

Advantage of EPROM:

- The contents of EPROM chips can be erased and reprogrammed. This can be done by exposing the chip to ultraviolet light.

Disadvantage of EPROM:

- To erase the contents from EPROMs chip, it must be physically removed from the circuit for reprogramming and that its entire contents are erased by the ultraviolet light.

Note:-

The disadvantage of EPROM is that, a chip must be physically removed from the circuit for reprogramming and that its entire contents are erased by the ultraviolet light. To overcome this problem, another version of erasable PROMs that can be both programmed and erased electrically. Such chips, called EEPROMs.

4.EEPROM – Electrically Erasable Programmable ROM

It is possible to erase the cell contents selectively.

Advantage of EEPROM over EPROM

- ✓ Chip need not have to be removed for erasure.
- ✓ It is possible to erase the cell contents selectively.

Disadvantage of EEPROMs

- ✓ The different voltages are needed for erasing, writing, and reading the stored data.

5. FLASH MEMORY

- It is possible to read the contents of a single cell, but it is only possible to write an entire block of cells. Prior to writing, the previous contents of the block are erased.
- Flash devices have greater density, which leads to higher capacity and a lower cost per bit.
- They require a single power supply voltage, and consume less power in their operation.

Application of Flash memory

The low power consumption of flash memory makes it attractive for use in portable equipment that is battery driven.

Typical applications include

- ✓ **hand-held computers**
- ✓ **cell phones**
- ✓ **digital cameras**
- ✓ **MP3 music players**

- In hand-held computers and cell phones, flash memory holds the software needed to operate the equipment, thus preventing the need for a disk drive.
- In digital cameras, flash memory is used to store picture image data.
- In MP3 players, flash memory stores the data that represent sound.
- **Cell phones, digital cameras, and MP3 players are good examples of embedded systems.**
- Single flash chips do not provide sufficient storage capacity for hand-held computers, cell phones, digital cameras, and MP3 music player applications.
- Larger memory modules consisting of a number of chips are needed.

Two such modules are,

- ✓ **Flash cards**
- ✓ **Flash drives.**

Note: Similarities in Flash memory and EEPROM

Technology used

Both are based on a single transistor controlled by trapped charge.

Flash Cards

- One way of constructing a larger module is to mount flash chips on a small card. Such flash cards have a standard interface that is used for variety of products. A card is plugged into a conveniently accessible slot. Flash cards have a variety of memory sizes.
- Typical sizes are 8, 32, and 64 Mbytes.
- A minute of music can be stored in about 1 Mbyte of memory, using the MP3 encoding format. Hence, a 64-MB flash card can store an hour of music.

Flash Drives:

- Larger flash memory modules have been developed to replace hard disk drives. These flash drives are designed to fully emulate the hard disks, to the point that they can be fitted into standard disk drive bays.
- But, the storage capacity of flash drives is significantly lower. Currently, the capacity of

flash drives is less than one gigabyte. In contrast, hard disks can store many gigabytes.

Advantages of Flash drives

- The flash drives are solid state electronic devices that have no movable parts.
- They have shorter seek and access times, which results in faster response.
- They have lower power consumption, which is used in battery driven applications
- They are insensitive to vibration.

Disadvantages of flash drives

- Smaller capacity and higher cost per bit, but disks provide an extremely low cost per bit.
- The flash memory will deteriorate after it has been written a number of times. This number is high, typically at least one million times.

Differences between flash memory and EEPROM

Flash memory	EEPROM
It is possible to read the contents of a single cell, but it is only possible to write an entire block of cells. Prior to writing, the previous contents of the block are erased.	it is possible to read and write the contents of a single cell
Flash devices have greater density, which leads to higher capacity and a lower cost per bit.	Less capacity than Flash device
They require a single power supply voltage, and consume less power in their operation.	The different voltages are needed for erasing, writing, and reading the stored data

VI. SPEED, SIZE, AND COST of Memory

SRAM

- A very fast memory can be implemented if SRAM chips are used.
- But these chips are expensive because their basic cells have 6 transistors, with very large number of cells onto a single chip.
- Thus, for cost reasons, it is impractical to build a large memory using SRAM chips.

DRAM

- It has simpler basic cells and thus is much less expensive. But such memories are significantly slower.
- But it is expensive for higher capacity (hundred of megabytes)

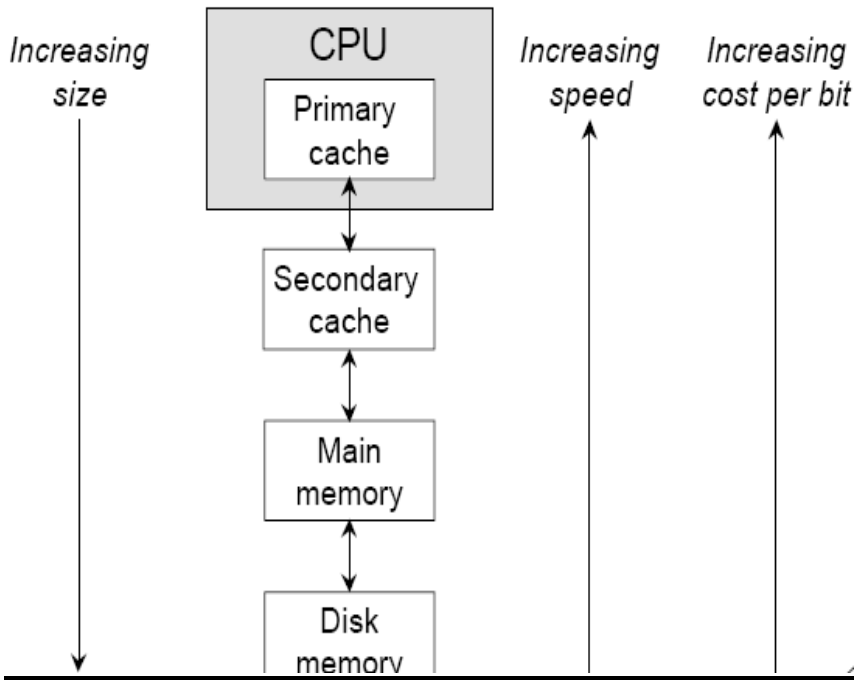
Magnetic Disks

- Large memory spaces.
- Very large disks are available at a reasonable price
- Slower than the semiconductor memory units.

So we conclude the following:

- A huge amount of cost-effective storage can be provided by magnetic disks.
- Main memory can be built with dynamic RAM technology.
- This leaves SRAMs to be used in smaller units where speed is of the essence, such as in cache memories.

Memory hierarchy



- *All of these different types of memory units are employed effectively in a computer.*
- The fastest access is to data held in **processor registers**. Therefore, if we consider the registers to be part of the memory hierarchy, then the processor registers are at the top in terms of the speed of access.
- At the next level of the hierarchy is a relatively small amount of memory that can be implemented directly on the processor chip. This memory, called **a processor cache**, holds copies of instructions and data stored in a much larger memory that is provided externally.
- **There are often two levels of caches.**
    - **Primary cache**

- **Secondary cache**

- A primary cache (L1) is always located on the processor chip. This cache is small because it competes for space on the processor chip.
- A larger, secondary cache (L2) is placed between the primary cache and the rest of the memory. It is usually implemented using SRAM chips.
- The next level in the hierarchy is called the main memory. This rather large memory is implemented using dynamic memory components.
- The main memory is much larger but significantly slower than the cache memory. In a typical computer, the access time for the main memory is about ten times longer than the access time for the L I cache.
- Disk devices provide a huge amount of inexpensive storage. They are very slow compared to the semiconductor devices used to implement the main memory.

Note:

During program execution, the speed of memory access is of very important.

VII. CACHE MEMORIES

- ✓ A cache memory is faster than the main memory.
- ✓ The effectiveness of the cache mechanism is based on a property of computer programs called **locality of reference.**
- ✓ Most of the execution time is spent on routines in which many instructions are executed repeatedly. These instructions may constitute a simple loop, nested loops, or a few procedures that repeatedly call each other.
- ✓ Many instructions in localized areas of the program are executed repeatedly during some time period, and the remainder of the program is accessed relatively infrequently. This is referred to as **locality of reference.**
- ✓ **Locality of reference is manifested itself in two ways**:
  - Temporal locality
  - Spatial locality

Temporal locality:-

- **The temporal means that a recently executed instruction is likely to be executed again very soon**.
- The temporal aspect of the locality of reference suggests that whenever an instruction or data is first needed, then they should be brought into the cache where it will hopefully **remain until it is needed again**.

Spatial locality:-

- **The spatial aspect means that instructions in close nearness to a recently executed instruction are also likely to be executed soon.**
- The spatial aspect suggests that instead of fetching one item from the main memory to the cache, it is useful to **fetch several items that reside at adjacent addresses**.

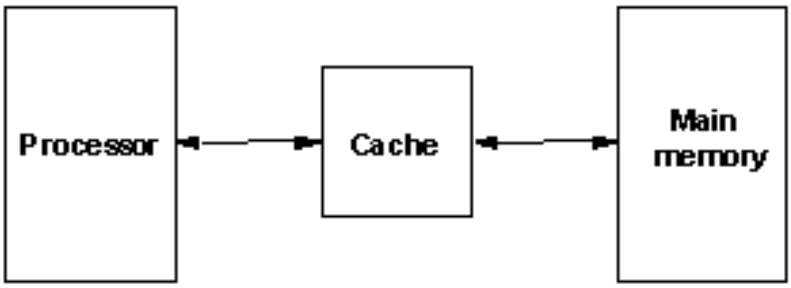
Note: We can use the term block to refer to a set of contiguous address locations of some size.

- ✓ If the active segments of a program can be placed in a fast cache memory, then the total execution time can be reduced significantly.

Use of a Cache Memory

- When a Read request is received from the processor, the contents of a block of memory words containing the location specified are transferred into the cache one word at a time.
- Subsequently, when the program references any of the locations in this block, the desired contents are read directly from the cache.

USE OF CACHE MEMORY



- Usually, the cache memory can store a reasonable number of blocks at any given time, but this number is small compared to the total number of blocks in the main memory.
- The correspondence between the main memory blocks and those in the cache is specified by a **mapping function**.
- When the cache is full and a memory word that is not in the cache is referenced, the cache control hardware must decide which block should be removed to create space for the new block that contains the referenced word. The collection of rules for making this decision constitutes the **replacement algorithm.**
- The processor does not need to know explicitly about the existence of the cache.

Read or Write Hit

- It simply issues Read and Write requests using addresses that refer to locations in the memory.

- The cache control circuitry determines whether the requested word currently exists in the cache.
- If it does, the Read or Write operation is performed on the appropriate cache location. In this case, **a read or write hit** is said to have occurred.
- In a Read operation, the main memory is not involved.
- For a **Write operation**, the system can proceed in two ways.
  - ✓ **Write through protocol**
  - ✓ **Write back / copy back protocol**

Write-Through Protocol:-

The cache location and the main memory location are updated simultaneously.

Write Back / Copy Back Protocol:-

It is used to update only the cache location and to mark it as updated with an associated flag bit, often called the **dirty or modified bit**.

The main memory location of the word is updated later, when the block containing this marked word is to be removed from the cache to make room for a new block. This technique is known as the **write back, or copy-back, protocol.**

- The write-through protocol is simpler, but it results in unnecessary Write operations in the main memory when a given cache word is updated several times during its cache residency.
- In the write-back protocol may also result in unnecessary Write operations because when a cache block is written back to the memory all words of the block are written back, even if only a single word has been changed while the block was in the cache.

Read / write Miss

- When the addressed word in a Read operation is not in the cache, a **read miss** occurs. The block of words that contains the requested word is copied from the main memory into the cache.
- After the entire block is loaded into the cache, the particular word requested is forwarded to the processor.
- Alternatively, this word may be sent to the processor as soon as it is read from the main memory. This technique is called **load-through, or early restart**, reduces the processor's waiting period. Because of more complex circuitry, it increases the cost.
- During a Write operation, if the addressed word is not in the cache, a write miss occurs.
- Then, **if the write-through protocol is used**, the information is written directly into the main memory.
- **If the write-back protocol**, the block containing the addressed word is first brought into the cache, and then the desired word in the cache is overwritten with the new

information.

MAPPING FUNCTIONS

The correspondence between the main memory blocks into their cache position is specified by mapping function.

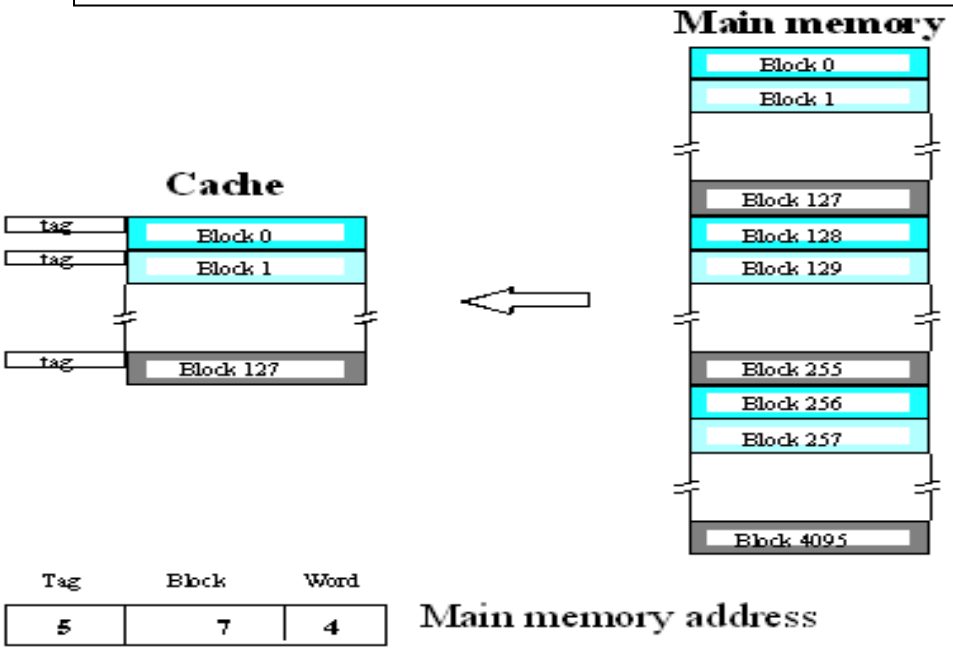
EXAMPLE:-

- ✓ Consider a **cache memory** consisting of 128 blocks of 16 words each. So it can have a total of 2048 (2K) words.
- ✓ Assume that the **main memory** is addressable by a 16-bit address. The main memory has 64K words, which we will view as 4K blocks of 16 words each.
- ✓ For ease of understanding, assume that **consecutive addresses refer to consecutive words**.
- ✓ Three types of mapping techniques used. They are
  - **Direct Mapping**
  - **Associative Mapping**
  - **Set Associative Mapping**

Direct Mapping

- ➢ The simplest way to determine cache locations in which to store memory blocks is the direct-mapping technique.
- ➢ In this technique, block j of the main memory maps onto **block j modulo 128** of the cache.

Block address of main memory % number of blocks in cache memory



- Thus, whenever one of the main memory blocks 0, 128, 256, . . . is loaded in the cache, it is stored in cache block 0. Blocks 1, 129, 257, . . . are stored in cache block 1, and so on.

Disadvantage:

- Since more than one memory block is mapped onto a given cache block position, **contention** may arise for that position even when the cache is not full.
  - ✓ For example, instructions of a program may start in block 1 and continue in block 129, possibly after a branch. As this program is executed, both of these blocks must be transferred to the block-1 position in the cache. Contention is resolved by allowing the new block to overwrite the currently resident block.
  - ✓ In this case, the **replacement algorithm is trivial**.

Placement of a block in the cache is determined from the memory address. The memory address can be divided into three fields.

Tag	Block	word
5	7	4

The low-order 4 bits, select one of 16 words in a block.

- When a new block enters the cache, the 7-bit cache block field determines the cache position in which this block must be stored.
- The high-order 5 bits of the memory address of the block are stored in 5 tag bits associated with its location in the cache. They identify which of the 32 blocks that are mapped into this cache position are currently resident in the cache.
- As execution proceeds, the 7-bit cache block field of each address generated by the processor points to a particular block location in the cache.
- The high-order 5 bits of the address are compared with the tag bits associated with that cache location., If they match, then the desired word is in that block of the cache.
- If there is no match, then the block containing the required word must first be read from the main memory and loaded into the cache. This approach is called direct-mapping technique.

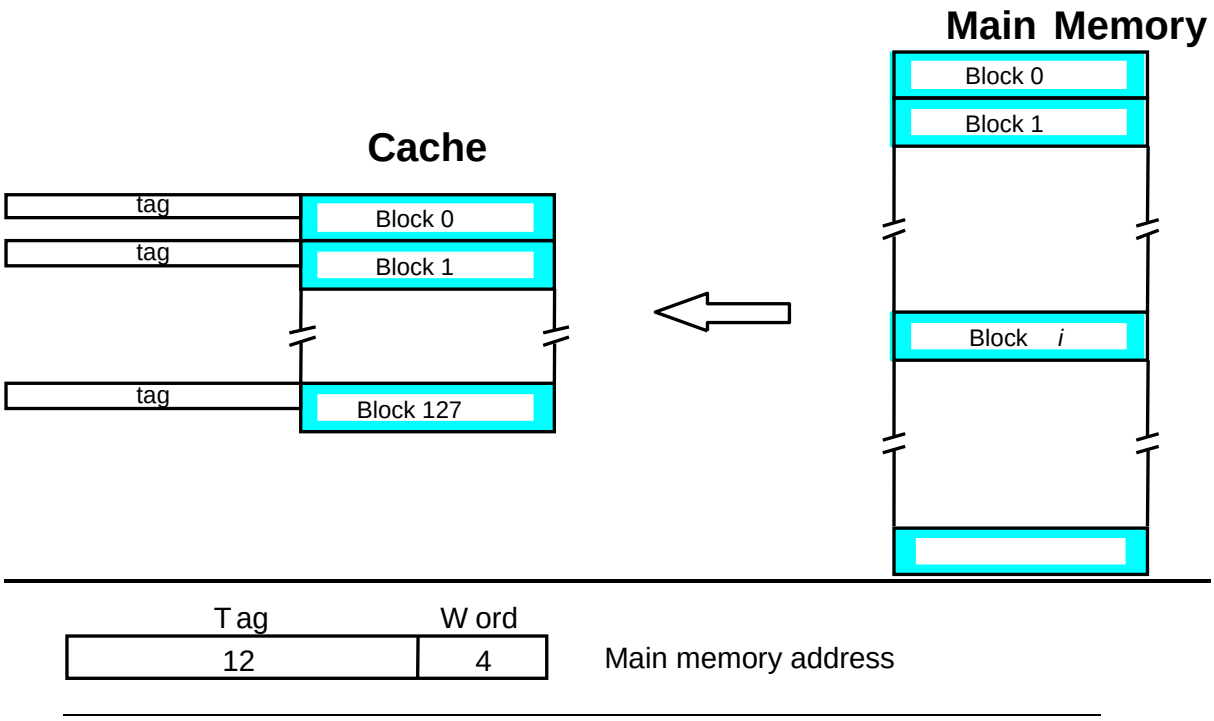
Advantages:

- It is easy to implement, but it is not very flexible.

ASSOCIATIVE MAPPING

Associative mapping is much more flexible mapping method, in which a main memory block can be placed into any cache block position.

Associative mapped cache



- Here 12 tag bits are required to identify a memory block when it is resident in the cache. The tag bits of an address received from the processor are compared to the tag bits of each block of the cache to see if the desired block is present. This is called the **associative-mapping technique.**
- It gives complete freedom in choosing the cache location in which to place the memory block. Thus, the space in the cache can be used more efficiently.
- A new block that has to be brought into **the cache has to replace an existing block only if the cache is full.** In this case, we need an algorithm to select the block to be replaced.

Disadvantage:-

- The **cost of an associative cache is higher** than the cost of a direct-mapped cache because of the need to search all 128 tag patterns to determine whether a, given block is in the cache. A search of this kind is called an associative search. For better performance**, the tags must be searched in parallel.**

SET – ASSOCIATIVE MAPPING

- A combination of the direct- and associative-mapping techniques can be used.
- Blocks of the cache are grouped into sets, and the mapping allows a block of the main memory to reside in any block of a specific set.

Hence, the contention problem of the direct method is eased by having a few choices for block placement. At the same time, the hardware cost is reduced by decreasing the size of the associative search.

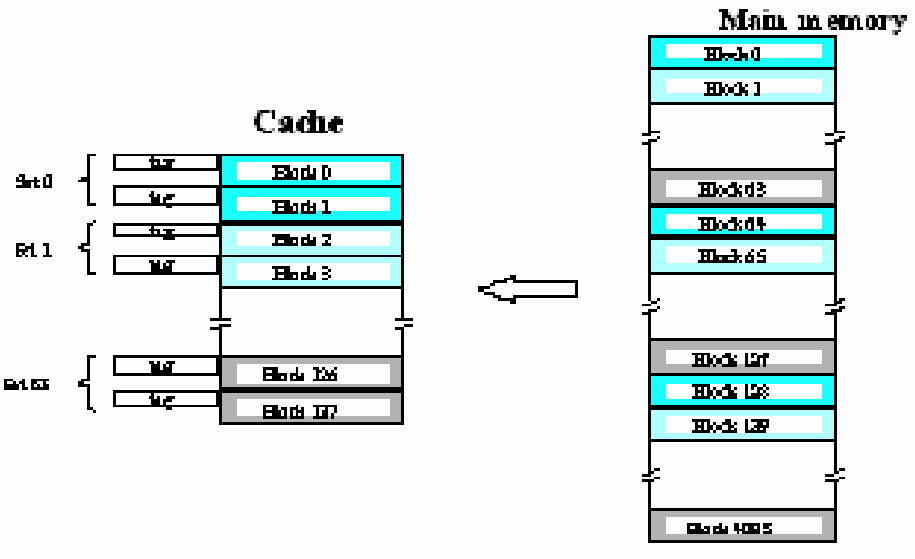
Example:

Set-associative-mapping technique is shown below for **a cache with two blocks per set.**

- Here memory blocks 0, 64, 128,…, 4032 map into cache set 0, and they can occupy either of the two block positions within this set. Having 64 sets means that the 6-bit set field of the address determines which set of the cache might contain the desired block.

Block address of main memory % number of sets in cache memory

Set-associative-mapped cache with two blocks per set



The main memory address is represented as,

Tag	Set	word
6	6	4

Block Search: (two-way associative search)

- ✓ 6-bit set filed of the address determines which set of the cache might contain then desired block.
- ✓ The 6-bit tag field of the address must then be associatively compared to the tags of the 2 blocks of the set to check if the desired block is present.

(Note:

The other extreme of one block per set is the direct-mapping method. A cache that has k blocks per set is referred to as **a k-way set-associative cache.)**

- One more control bit, called the **valid bit**, must be provided for each block. This bit indicates whether the block contains valid data. It should not be confused with the modified, or dirty, bit mentioned earlier.
- The dirty bit, which indicates whether the block has been modified during its cache residency, is needed only in systems that do not use the write-through method.
- The valid bits are all set to 0 when power is initially applied to the system or when the main memory is loaded with new programs and data from the disk.
- Transfers from the disk to the main memory are carried out by a DMA mechanism.
- The valid bit of a particular cache block is set to 1 the first time this block is loaded from the main memory.
- Whenever a main memory block is updated by a source that bypasses the cache, a check is made to determine whether the block being loaded is currently in the cache. If it is, its valid bit is cleared to 0. This ensures that old data will not exist in the cache.

REPLACEMENT ALGORITHMS

- In a direct-mapped cache, the position of each block is predetermined; hence, no replacement strategy exists.
- But in associative and set-associative caches there exists some flexibility.
- When a new block is to be brought into the cache and the positions that it may occupy are full, the cache controller must decide which of the old blocks to overwrite.
- Therefore, when a block is to be overwritten, it is sensible to overwrite the one that has gone the longest time without being referenced. This block is called the least recently used (LRU) block, and the technique is called the **LRU replacement** algorithm.
- To use the LRU algorithm, the cache controller must track references to all blocks as computation proceeds. A 2-bit counter can be used for each block.

Counter is updated under 3 conditions

- ✓ When hit occurs in a cache
- ✓ When miss occurs but cache is not full
- ✓ When miss occurs but cache is full

- **When a hit occurs**, the counter of the block that is referenced is set to 0. Counters with values originally lower than the referenced one are incremented by one, and all

others remain unchanged.

- **When a miss occurs and the set is not full**, the counter associated with the new block loaded from the main memory is set to 0, and the values of all other counters are increased by one.
- When a miss occurs and the set is full, the block with the counter value 3 is removed, the new block is put in its place, and its counter is set to 0. The other three block counters are incremented by one. It can be easily verified that the counter values of occupied blocks are always distinct.
- The LRU algorithm has been used extensively. Although it performs well for many access patterns, it can lead to poor performance in some cases.
- Performance of the LRU algorithm can be improved by introducing a small amount of randomness in deciding which block to replace.
- A naturally reasonable rule would be to remove the "oldest" block from a full set when a new block must be brought in. But this algorithm does not take into account the recent pattern of access to blocks in the cache.

VIII. CACHE MEMORY-PERFORMANCE CONSIDERATIONS

- Two key factors in the commercial success of a computer are
  - Performance
  - Cost
- To improve the performance without increasing the cost, a common measure of success is the **price/performance ratio**.
- Performance depends on how fast machine instructions can be brought into the processor for execution and how fast they can be executed.
- The speed and efficiency of data transfer between various types of memory are having greater significance. Both is not possible if, both the slow and the fast units are accessed in the same manner, but can be achieved by the **parallelism** in the organization of the slower unit.
- An effective way to introduce **parallelism is to use an interleaved organization**.

1 INTERLEAVING

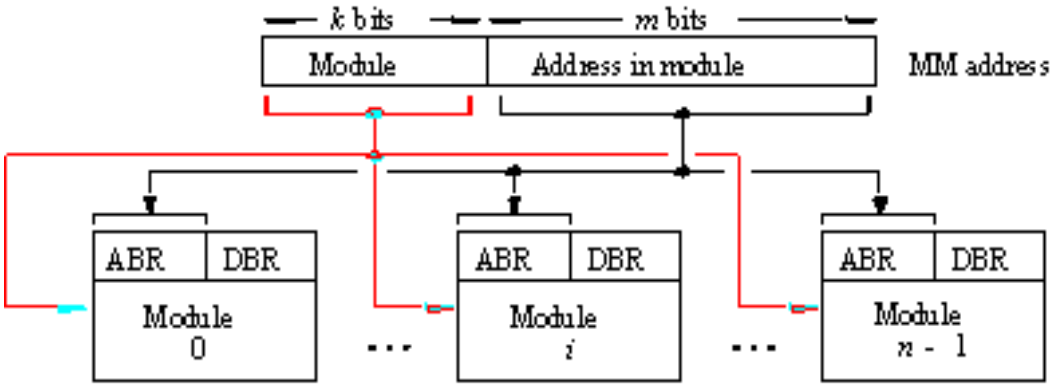
- If the main memory of a computer is structured as a ***collection of physically separate modules.***
- Each module has its own
  - Address buffer register (**ABR**) and

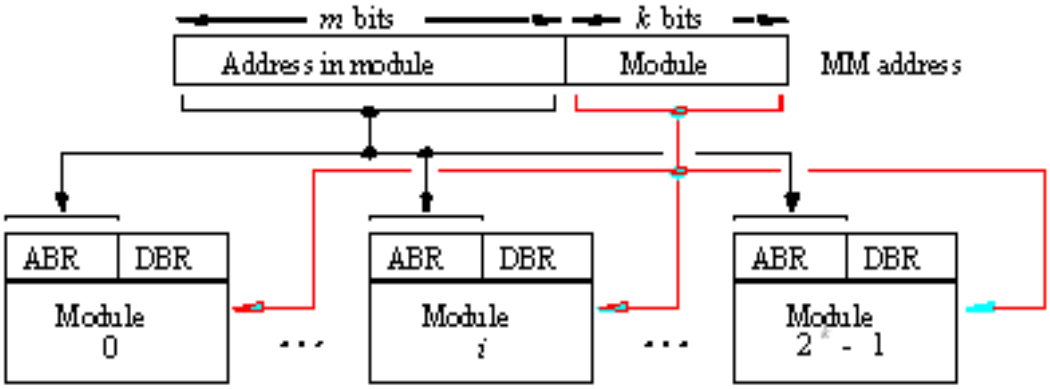
- Data buffer register (**DBR**)

- Thus, the aggregate rate of transmission of words to and from the main memory system can be increased.
- Memory access operations may proceed in ***more than one module at the same time***.
- The individual addresses are distributed over the modules is critical in determining the average number of modules that can be kept busy as computations proceed.

Two methods of address layouts are:-

- ✓ **Consecutive words in a module**
- ✓ **Consecutive words in consecutive modules**





1.Consecutive words in a module:-

- The **high order k bits** name one of n modules, and the **low-order m bits** name a particular word in that module.
- When consecutive locations are accessed, as happens when a block of data is transferred to a cache, only one module is involved.

2) **Consecutive words in consecutive modules:-**

- The more effective way to address the modules is Consecutive words in consecutive modules .It is called **memory interleaving**.

- The low-order k bits of the memory address select a module, and the high-order m bits name a location within that module.
- In this way, consecutive addresses are located in successive modules.
- Thus, any component of the system that generates requests for access to consecutive memory locations can keep several modules busy at anyone time.

Note:

To implement the interleaved structure, there must be 2k modules.

2 HIT RATE AND MISS PENALTY

HIT: A successful access to data in a cache is called a hit.

HIT RATE

The number of hits stated as a fraction of all attempted accesses is called the hit rate.

MISS RATE

The miss rate is the number of misses stated as a fraction of attempted accesses.

High hit rates, well over 0.9, are essential for high-performance computers.

Performance is adversely affected by the actions that must be taken after a miss.

MISS PENALTY

The extra time needed to bring the desired information into the cache is called the miss penalty.

- In general **the miss penalty is the time needed to bring a block of data from a slower unit in the memory hierarchy to a faster unit.**
- The miss penalty is reduced if efficient mechanisms for transferring data between the various units of the hierarchy are implemented.
- The hit rates depend on the design of the cache and on the instruction and data access patterns of the programs being executed.

How can the hit rate be improved?

Possibilities are

- ✓ To make the cache larger, but this entails increased cost.
- ✓ To increase the block size while keeping the total cache size constant, to take advantage of spatial locality.

If all items in a larger block are needed in a computation, then it is better to load these items into the cache as a consequence of a single miss, rather than loading several smaller blocks as a result of several misses.

Example:

- Consider the impact of the cache on the overall performance of the computer.
- Let h be the hit rate, M the miss penalty.
- The time to access information in the main memory, and C is the time to access information in the cache.
- The average access time by the processor is
  - $t_{ave} = hC + (1 - h)\,M$
- If the computer has no cache memory, then using a fast processor and a typical DRAM main memory, it takes 10 clock cycles for each memory read access.
- Suppose the computer has a cache that holds 8-word blocks and an interleaved main memory.
- 17 cycles are needed to load a block into the cache.

3 CACHES ON THE PROCESSOR CHIP

- All high-performance processor chips include some form of a cache.
- A combined cache for instructions and data is likely to have a somewhat better hit rate because it offers greater flexibility in mapping new information into the cache.
- If separate caches are used, it is possible to access both caches at the same time, which leads to **increased parallelism** and, hence, **better performance**.
- **Disadvantage**:- If separate caches (i.e., increased parallelism) are used that makes the circuit more complex and expensive.
- In high-performance processors two levels of caches are normally used:-
  - ✓ The Ll cache(s) is on the processor chip.
  - ✓ The L2 cache, which is much larger, may be implemented externally using SRAM chips.
  - ✓ If both Ll and L2 caches are used, the L1 cache should be designed to allow very fast access by the processor
  - ✓ The L2 cache can be slower, but it should be much larger to ensure a high hit rate. Its speed is less critical because it only affects the miss penalty of the Ll cache.

The average access time experienced by the processor in a system with two levels of caches is

$$t_{ave} = h_1C_1 + (1 - h_l)h_2C_2 + (1 - h_1)(l - h_2)M$$

- ✓ h1 is the hit rate in the Ll cache.
- ✓ h2 is the hit rate in the L2 cache.
- ✓ C1 is the time to access information in the Ll cache.

- ✓ C2 is the time to access inforn1ation in the L2 cache.
- ✓ M is the time to access information in the main memory.

The number of misses in the L2 cache, given by the term (1 - h1)(1 - h2), should be low. If both h1 and h2 are in the 90 percent range, then the number of misses will be less than 1 percent of the processor's memory accesses.

4. OTHER ENHANCEMENTS

Apart from the main design issues just discussed, several other possibilities exist for enhancing performance. They are

- ✓ Write Buffer
- ✓ Prefetching
- ✓ Lockup – free cache

4.1WRITE BUFFER

- When the write-through protocol is used, each write operation results in writing a new value into the main memory. If the processor must wait for the memory function to be completed, as we have assumed until now, then the processor is slowed down by all write requests.
- Yet the processor typically does not immediately depend on the result of a write operation, so it is not necessary for the processor to wait for the write request to be completed.
- To improve performance, a **write buffer can be included for temporary storage of write requests**. The processor places each write request into this buffer and continues execution of the next instruction.
- The write requests stored in the write buffer are sent to the main memory whenever the memory is not responding to read requests. The read requests are serviced immediately because the processor usually cannot proceed without the data that are to be read from the memory. Hence, these requests are given priority over write requests.
- The write buffer may hold a number of write requests. Thus, it is possible that a subsequent read request may refer to data that are still in the write buffer. To ensure correct operation, the addresses of data to be read from the memory are compared with the addresses of the data in the write buffer. In case of a match, the data in the write buffer are used.

4.2 PREFETCHING

- To avoid delay in the processor, it is possible to prefetch the data into the cache before they are needed.

- Prefetching can be done through software or hardware.

Through software

- A special prefetch instruction may be provided in the instruction set of the processor. Executing this instruction causes the addressed data to be loaded into the cache, as in the case of a read miss.
- A prefetch instruction is inserted in a program to cause the data to be loaded in the cache by the time they are needed in the program. The hope is that prefetching will take place while the processor is busy executing instructions that do not result in a read miss, thus allowing accesses to the main memory to be overlapped with computation in the processor.
- Prefetch instructions can be inserted into a program either by the programmer by the compiler.

Through Hardware

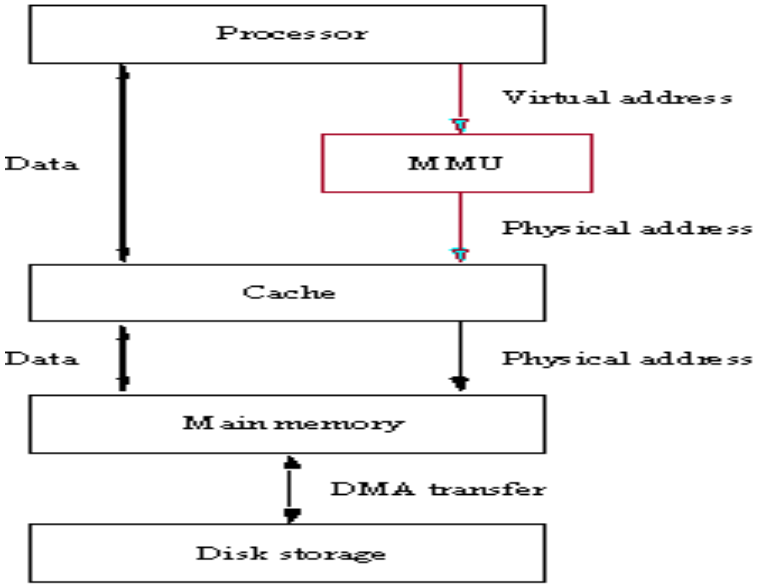
This involves adding circuitry that attempts to discover a pattern in memory references and then prefetches data according to this pattern.

4.3 LOCKUP – FREE CACHE

- The software prefetching scheme does not work well if it interferes significantly with the normal execution of instructions.
- This is the case if the action of prefetching stops other accesses to the cache until the prefetch is completed. A cache of this type is said to be locked while it services a miss.
- We can solve this problem by modifying the basic cache structure to allow the processor to access the cache while a miss is being serviced. In fact, it is desirable that more than one outstanding miss can be supported.
- We have used software prefetching as an obvious motivation for a cache that is not locked by a read miss.
- A much more important reason is that, in a processor that uses a pipelined organization, which overlaps the execution of several instructions, a read miss caused by one instruction could stall the execution of other instructions.

VIII. VIRTUAL MEMORIES

- In most modern computer systems, the physical main memory is not as large as the address space spanned by an address issued by the processor.
- For example, a processor that issues 32-bit addresses has an addressable space of 4G bytes. The size of the main memory in a typical computer ranges from a few hundred megabytes to 1G bytes.
- When a program does not completely fit into the main memory, the parts of it not currently being executed are stored on secondary storage devices, such as magnetic disks, while executing brought into the main memory.
- The operating system moves programs and data automatically between the main memory and secondary storage.
- Techniques that automatically move program and data blocks into the physical main memory when they are required for execution are called **virtual-memory techniques.**
- The binary addresses that the processor issues for either instructions or data are called **virtual or logical addresses.**



Virtual memory organization.

- A special hardware unit, called the **Memory Management Unit (MMU),** translates virtual addresses into physical addresses.
- When the desired data (or instructions) are in the main memory, these data are fetched. If the data are not in the main memory, the MMU causes the operating system to bring the data into the memory from the disk. Transfer of data between the disk and the main memory is performed using the DMA scheme.

ADDRESS TRANSLATION

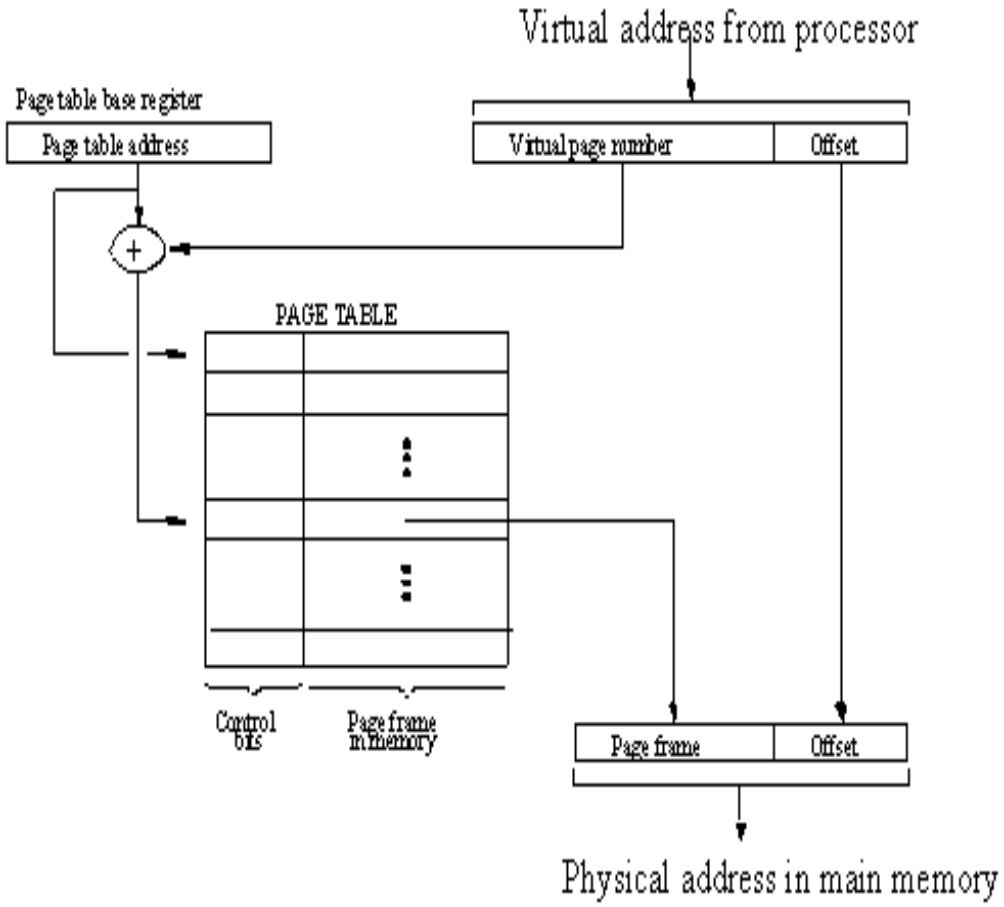
Pages:

- Assume that all programs and data are composed of fixed-length units called pages, each of which consists of a block of words that occupy contiguous locations in the main memory. Pages commonly range from 2K to 16K bytes in length.
- They constitute the basic unit of information that is moved between the main memory and the disk Pages should not be too small, because the access time of a magnetic disk is much longer than the access time of the main memory.
- On the other hand, if pages are too large it is possible that a substantial portion of a page may not be used. Cache techniques and virtual memory techniques are very similar.
- Each virtual address generated by the processor, has a virtual page number (high-order bits) followed by an offset (low-order bits) that specifies the location of a particular byte (or word) within a page.

Page table:

- Information about the main memory location of each page is kept in a **page table**. This information includes the main memory address where the page is stored and the current status of the page.
- An area in the main memory that can hold one page is called a page frame. The starting address of the page table is kept in a **page table base register**. By adding the virtual page number to the contents of this register, the address of the corresponding entry in the page table is obtained. The contents of this location give the starting address of the page if that page currently resides in the main memory.
- Each entry in the page table also has some **control bits** that describe the status of the page while it is in the main memory.
- One bit indicates the validity of the page, that is, whether the page is actually loaded in the main memory. This bit allows the operating system to invalidate the page without actually removing it.
- Another bit indicates whether the page has been modified during its residency in the memory. Other control bits indicate various restrictions that may be imposed on accessing the page. For example, a program may be given full read and write permission. or it may be restricted to read accesses only.

Virtual-memory address translation



Translation Lookaside Buffer (TLB):

- Page table information is used by MMU for every read and write operation but due large size of page table it is impossible to include in MMU of processor. Hence, page table is kept in main memory.
- However, a copy of small portion of page can be accommodated within MMU. This portion consists of the page table entries that correspond to the most recently accessed pages. A small cache, usually called the **Translation Lookaside Buffer** (TLB) is incorporated into the MMU for this purpose.
- In addition to the information that constitutes a page table entry, the TLB must also include the virtual address of the entry.

When the operating system changes the contents of page tables, it must simultaneously invalidate the corresponding entries in the TLB.

Address translation of TLB:

Given a virtual address, the MMU looks in the TLB for the referenced page. If the page table entry for this page is found in the TLB, the physical address is obtained immediately.

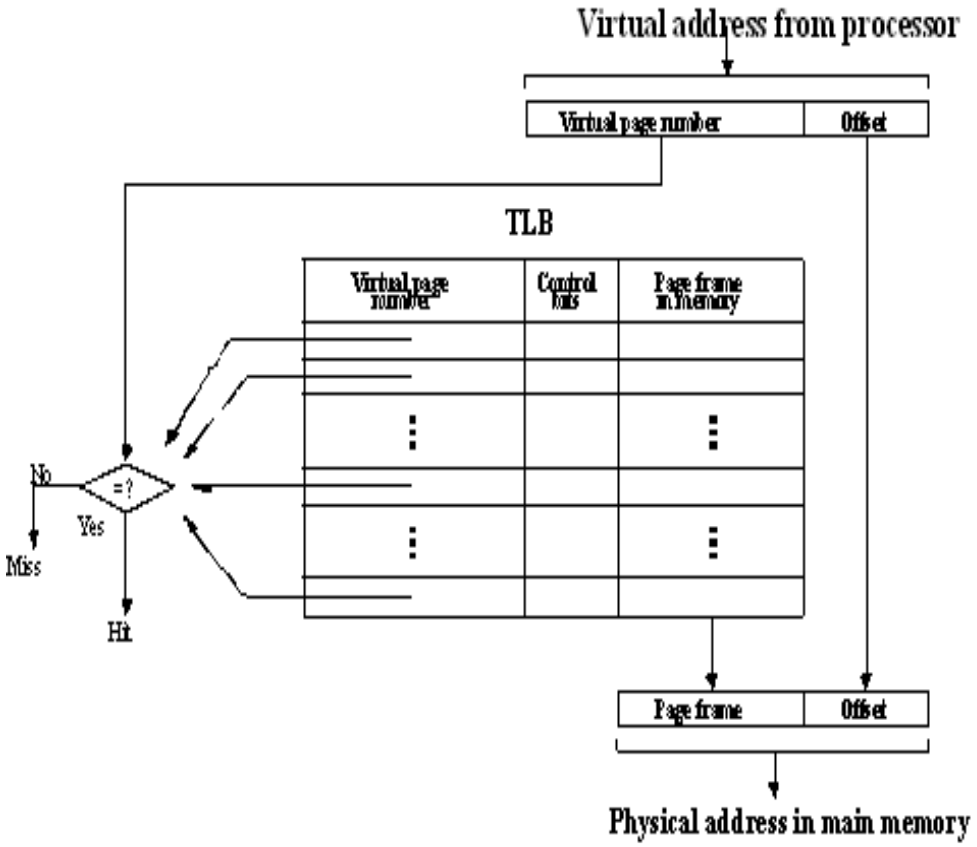


Fig: Organization of a TLB using associative mapping technique

If there is a **miss in the TLB**, is called **page fault**. Then the required entry is obtained from the page table in the main memory and the TLB is updated.

Page Fault:

- When a program generates an access request to a page that is not in the main memory, a **page fault** is said to have occurred. The whole page must be brought from the disk into the memory before access can proceed.
- When it detects a page fault, the MMU asks the operating system to intervene by raising an **exception (interrupt)**. Processing of the active task is interrupted, and control is transferred to the operating system.
- The operating system then copies the requested page from the disk into the main memory and returns control to the interrupted task, a long delay may occur hence, once their is page fault it begin execution of another task whose pages are in the main memory.
- Hence, when the task resumes, either the execution of the interrupted instruction must continue from the point of interruption or the instruction must be restarted.
- If a new page is brought from the disk when the main memory is full, it must replace one of the resident pages. The problem of choosing which page to remove is just as critical.

- The Least Recently Used is removed normally. A control bit that is set to 1 whenever the corresponding page is referenced (accessed). The operating system occasionally dears this bit in all page table entries, thus providing a simple way of determining which pages have not been used recently.
- The average translation time can be reduced by including one or more special registers that retain the virtual page number and the physical page frame of the most recently performed translations. The information in these registers can be accessed more quickly than the TLB.

IX. MEMORY MANAGEMENT REQUIREMENTS

- Management routines are part of the operating system of the computer. It is convenient to assemble the operating system routines into a virtual address space, called the **system space** that is separate from the virtual space in which user application programs reside called the **user space**.
- In fact, there may be a number of user spaces, one for each user. This is arranged by providing a separate page table for each user program.
- The MMU uses a page table base register to determine the address of the table to be used in the translation process. Hence, by changing the contents of this register, the operating system can switch from one space to another.
- The physical main memory is thus shared by the active pages of the system space and several user spaces. However, only the pages that belong to one of these spaces are accessible at any given time.
- The independent user programs coexist in the main memory, the notion of protection must be addressed. No program should be allowed to destroy either the data or instructions of other programs in the memory. Such protection can be provided in several ways.

The processor has two states:-

1. **The supervisor state**
2. **The user state**.

→ Supervisor state

- The processor is usually placed in the supervisor state when operating system routines are being executed and in the user state to execute user programs.

→ User State

- In the user state, some machine instructions cannot be executed.
- These privileged instructions, which include such operations as modifying the page table base register, can only be executed while the processor is in the supervisor state. Hence, a user program is prevented from accessing the page tables of other user spaces or of the system space.
- Sometimes some application programs have access to certain pages belonging to another program.
- The operating system can arrange this by causing these pages to appear in both spaces. The **shared pages** will therefore have entries in two different page tables.
- The control bits in each table entry can be sent to control the access privileges granted to each program.

X. SECONDARY STORAGE DEVICES

Large storage requirements of most computer systems are economically realized in the form of **magnetic disks, optical disks, and magnetic tapes**, which are usually referred to as secondary storage devices.

3 types of secondary storage devices:

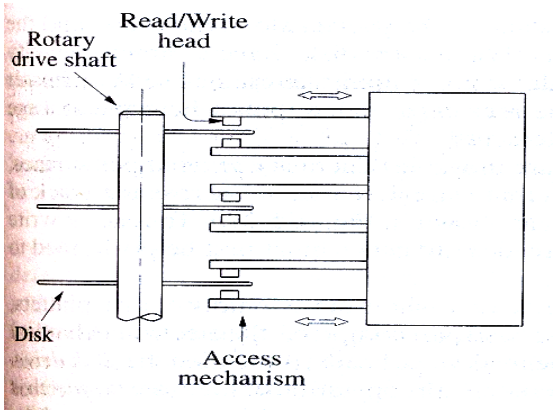
1. **Magnetic disks**
    i. **Hard disk**
    ii. **Floppy disk**
2. **Optical disks**
    i. **CD**
    ii. **DVD**
3. **Magnetic tapes**

I. MAGNETIC DISKS

1. HARD DISKS

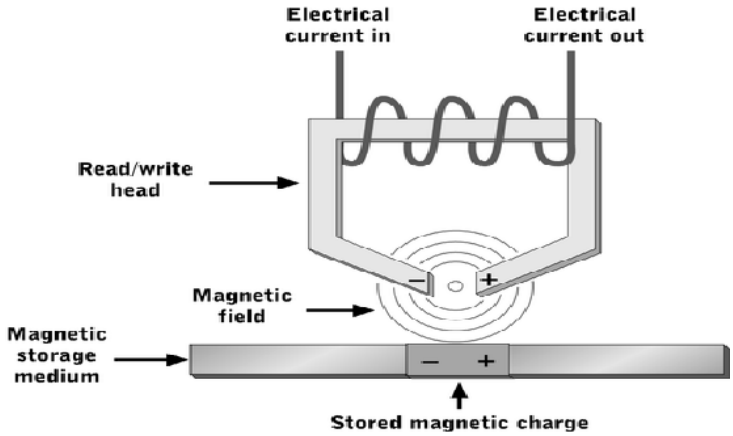
- The storage medium in a magnetic-disk system consists of one or more disks mounted on a common spindle. A **thin magnetic film** is deposited on each disk, usually on both sides.
- The disks are placed in a **rotary drive** so that the magnetized surfaces move in close proximity to read/write heads, as shown below.

Mechanical structure of magnetic hard disks



- The disks rotate at a **uniform speed**. Each head consists of a magnetic yoke and a magnetizing coil, as indicated below.

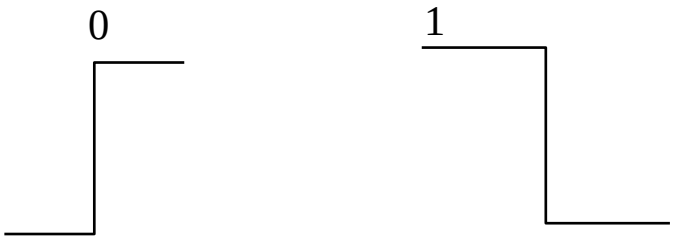
Read / write head



- **Digital information** can be stored on the magnetic film by applying current pulses of suitable polarity to the magnetizing coil.
- This causes the magnetization of the film; changes in the magnetic field induce a voltage in the coil.
- The polarity of this voltage is monitored by the control circuitry to determine the state of magnetization of the film.
- Only changes in the magnetic field under the head can be sensed during the Read operation. Therefore, if the binary states 0 and 1 are represented by two opposite states of magnetization, a voltage is induced in the head only at 0-to-l and at 1-to-0 transitions in the bit stream. A long string of 0s or 1s causes an induced voltage only at the beginning and end of the string.
- To determine the number of consecutive 0s or 1s stored, a clock must provide information for synchronization.

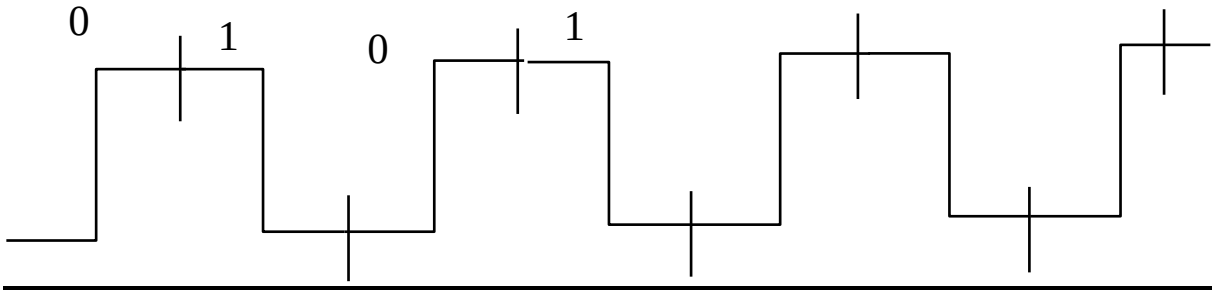
- The modem approach is to combine the clocking information with the data. Several different techniques have been developed for such encoding. One such simple scheme is called **Manchestor or Phase encoding.**

BIT REPRESENTATION OF MANCHESTOR OR PHASE ENCODING



Phase encoding

Winchestor technology



- The read/write heads of a disk system are movable.
- To read or write data on a given track, the arm holding the read/write heads must first be positioned to that track.

The disk system consists of three key parts. They are,

- ✓ Disk platters
- ✓ Disk drive
- ✓ Disk controller

- **Disk platters**:-are usually referred to as the disk.
- **Disk Drive:-**the electromechanical mechanism that spins the disk and moves the read/write heads; it is called the disk drive.
- **Disk Controller:-**is the electronic circuitry that controls the operation of the system, which is called the disk controller.

ORGANIZATION AND ACCESSING OF DATA ON A DISK

- Each surface is divided into concentric **tracks**, and each track is divided into **sectors**.
- The set of corresponding tracks on all surfaces of a stack of disks forms a **logical cylinder.**
- The data on all tracks of a cylinder can be accessed without moving the read/write heads. The data are accessed by specifying the surface number, the track number, and the sector number.
- The Read and Write operations start at sector boundaries. Data bits are stored serially on each track. Each sector usually contains **512 bytes of data**, but other sizes may be used.
- Following the data, there are additional bits that constitute an **error correcting code (**ECC). These bits are used to detect and correct errors that may have occurred in writing or reading of the 512 data bytes.
- **An unformatted disk has no information on its tracks**.
- The **formatting process** divides the disk physically into tracks and sectors. This process may discover some defective sectors or even whole tracks.
- The disk controller keeps a record of such defects and excludes them from use. In a typical computer, the disk is subsequently divided into logical partitions. There must be at least one such partition, called the **primary partition**. There may be a number of additional partitions.
- Each track has the same number of sectors. So, all tracks have the same storage capacity. Thus, the stored information is packed more densely on inner tracks than on outer tracks.
- This arrangement is used in many disks because it simplifies the electronic circuits needed to access the data. But, it is possible to increase the storage density by placing more sectors on outer tracks, which have longer circumference, at the expense of more complicated access circuitry. This scheme is used in large disks.

ACCESS TIME

There are two components involved in the time delay between receiving an address and the beginning of the actual data transfer.

- Seek Time
- Latency Time / rotational delay

→ SEEK TIME:

It is the time required to move the read/write head to the proper track. This depends on the initial position of the head relative to the track specified in the address. Average values are in the **5- to 8-ms range**.

→ROTATIONAL DELAY/ LATENCY LIME

It is the amount of time that elapses after the head is positioned over the correct track until the starting position of the addressed sector passes under the read/write head.

On average, this is the time for half a rotation of the disk.

→DISK ACCESS TIME:

The sum of these two delays is called the disk access time.

Disk access Time = Seek time + Latency Time

TYPICAL DISKS

The parameters representation of 3.5-inch (diameter) disk

- There **are 20 data-recording surfaces with 15,000 tracks per surface**.
- There is an average of **400 sectors per track**, and each **sector contains 512 bytes of data**.

The total capacity of the formatted disk is

=20 x 15,000 x 400 x 512

= 60 x 10^9 = 60 gigabytes (high-capacity).

- The average seek time is 6 ms.
- The platters **rotate at 10,000 revolutions per minute**, so that the average latency is 3 ms, this is the time for a half-rotation.
- The average internal transfer rate, from a track to the data buffer in the disk controller, is 34 Mbytes/s (high-data-rate).
- When connected to a SCSI bus, a drive of this type may have an external transfer rate of 160 Mbytes/s.

DATA BUFFER / CACHE

SCSI disk

- ✓ A disk drive is connected to the rest of a computer system using SCSI (Small

Computer System Interface) bus.

- ✓ A disk drive that incorporates the required SCSI interface circuitry is usually referred to as a SCSI drive.

Data buffer

- ✓ The SCSI bus is capable of transferring data at much higher rates than the rate at which data can be read from disk tracks. To deal with the possible differences in transfer rates between the disk and the SCSI bus a data buffer is included in the disk unit. This buffer is a semiconductor memory, capable of storing a few megabytes of data.
- ✓ The requested data are transferred between the disk tracks and the buffer at a rate dependent on the rotational speed of the disk. Transfers between the data buffer and other devices connected to the bus, normally the main memory, can then take place at the maximum rate allowed by the bus.

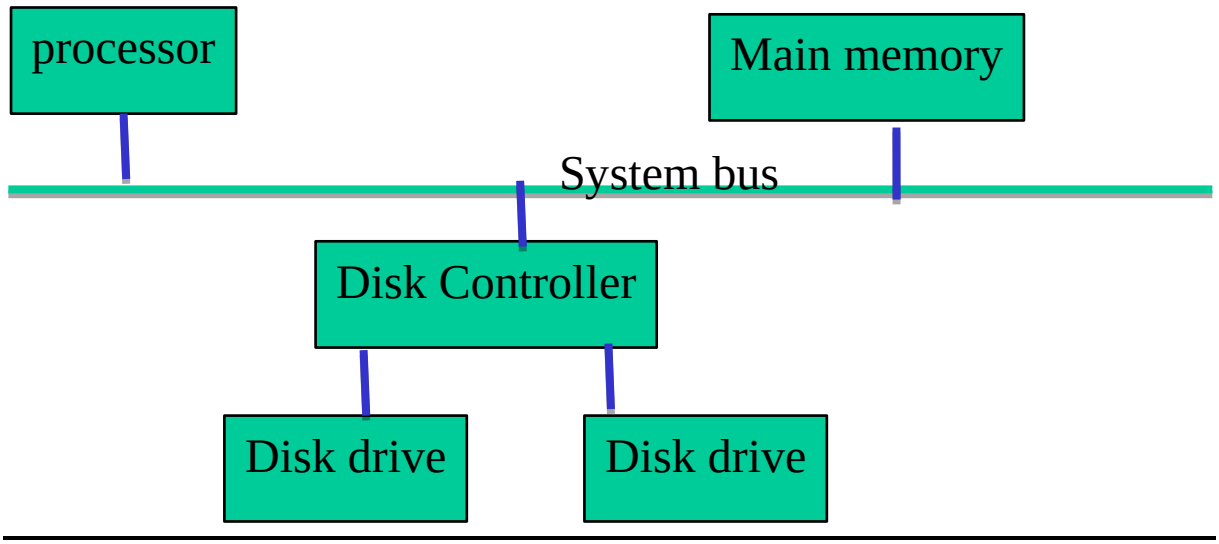
Caching mechanism for the disk

- ✓ The data buffer can also be used to provide a caching mechanism for the disk.
- ✓ When a read request arrives at the disk, the controller can first check to see if the desired data are already available in the cache (**buffer**).If so, the data can be accessed and placed on the SCSI bus in microseconds rather than milliseconds. Otherwise, the data are read from a disk track in the usual way and stored in the cache.

DISK CONTROLLER

- ➢ It controls the Operation of a disk drive
- ➢ It also provides an interface between the disk drive and the bus that connects it to the rest of the computer system.
- ➢ The disk controller may be used to control more than one drive.

DISK CONNECTED TO THE SYSTEM BUS



- The disk controller uses the DMA scheme to transfer data between the disk and the main memory. Actually, these transfers are from/to the data buffer of the disk, which is implemented as a part of the disk controller module.
- The OS initiates the transfers by issuing Read and Write requests, and it loads the controller's registers of disk controller with the addressing information such as main memory and disk address and control information such as Word count.

Main memory address:

The address of the first main memory location of the block of words involved in the transfer.

Disk address:

The location of the sector containing the beginning of the desired block of words.

Word count:

The number of words in the block to be transferred.

Major functions of disk Controller are,

→**Seek** Causes the disk drive to move the read/write head from its current position to the desired track.

→ **Read**

Initiates a Read operation, starting at the address specified in the disk address register. Data read serially from the disk are assembled into words and placed into the data buffer for transfer to the main memory. The number of words is determined by the word count register.

→ **Write**

Transfers data to the disk, using a control method similar to that for the Read operations.

→**Error checking**

Computes the error correcting code (ECC) value for the data read from a given sector and compares it with the corresponding ECC value read from the disk. In case of a mismatch, it corrects the error if possible; otherwise, it raises an interrupt to inform the as that an error has occurred. During a write operation, the controller computes the ECC value for the data to be written and stores this value on the disk.

SOFTWARE AND OPERATING SYSTEM IMPLICATIONS

- When the system is turned on, the OS which is available in secondary memory has to be loaded into the main memory, this process is known as **booting.**
- Booting is initiated by a small monitor program stored on nonvolatile ROM. This small program loads one block of data on disk at address 0 into main memory. This

block, referred to as the boot block, contains a loader program.

- After the boot block is loaded into main memory by the ROM monitor program, it loads the main parts of the OS into the main memory.
- Disk accesses are very slow compared. After the OS initiates a disk transfer operation, it switches execution to some other task without waiting for I/O completion. The disk controller informs the OS when the transfer is completed by raising an interrupt.
- In a computer system that has multiple disks, the OS may require transfers from several disks. OS allow transfer from/to one disk occurs while another disk is doing a seek. The OS can schedule such overlapped I/O activities.

2. FLOPPY DISK

- Floppy disks are
    - smaller,
    - simpler, and
    - cheaper disk units that consist of a
        - flexible,
        - removable,
        - Plastic diskette coated with magnetic material.
    - ✓ The magnetic disk is also called as diskette, disk or floppy disk.
- The diskette is enclosed in a plastic jacket, which has an **opening where the read/write head** makes contact with the diskette.
- A hole in the center of the diskette allows a **spindle mechanism** in the disk drive to position and rotate the diskette.
- One of the simplest schemes used in the first floppy disks for recording data is phase or Manchester encoding. Disks encoded in this way are said to have **single density**.
- A more complicated variant of this scheme, called **double density**: is most often used in current standard floppy disks. It increases the storage density by a factor of 2 but also requires more complex circuits in the disk controller.

- <u>Advantage</u>:
    - They are low cost
    - Easily portable
- Disadvantage

- Small storage capacities
- longer access times
- higher failure rates

➢ Current standard floppy disks are 3.25 inches in diameter and store 1.44 Mbytes of data.

❑ Size =3.25 inch diameter

❑ Storage capacity =144 or 2 Mbytes of data

Larger floppy disk is also available(ZIP disk)

❑ Storage capacity =more than 100 Mbytes

RAID Disk Arrays

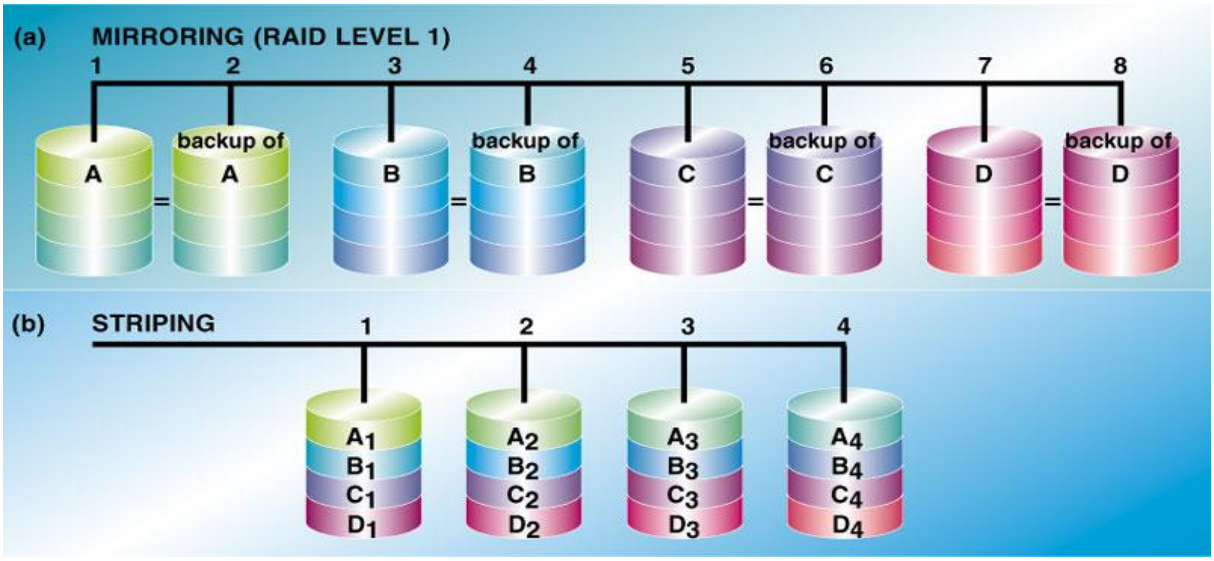
- They called it RAID, for **Redundant Array of Inexpensive Disks (or) Redundant Array of Independent Disk.**
- Using ***multiple disks also makes it possible to improve the reliability of the overall system***.
- Six different configurations were proposed. They are known as RAID levels.

RAID 0

- RAID 0 is the basic configuration intended to enhance performance. ***A single large file is stored in several separate disk units by breaking the file up into a number of smaller pieces and storing these pieces on different disks***. This is called **data striping**.
- When the file is accessed for a read, all disks can deliver their **data in parallel**. The total transfer time of the file is equal to the transfer time that would be required in a single-disk system divided by the number of disks used in the array.

RAID 1

- RAID 1 is intended to provide better reliability by ***storing identical copies of data on two disks rather than just one.***
- The two disks are said to be mirrors of each other. This is called as **disk mirroring**.
- Then, if one disk drive fails, all read and write operations are directed to its mirror drive. ***Disadvantage:***
- This is a costly way to improve the reliability because all disks are duplicated.



RAID 2, RAID 3, and RAID 4

RAID 2, RAID 3, and RAID 4 levels achieve increased reliability through **various parity checking schemes without requiring a full duplication of disks**. All of the parity information is kept on one disk.

RAID 5

RAID 5 also makes use of a **parity-based error-recovery scheme**. However, the parity information is distributed among all disks, rather than being stored on one disk.

RAID DISKS

- They have excellent performance and provide a large and reliable storage.
- They are used either in high-performance computers, or in systems where a higher than normal degree of reliability is required.

II. OPTICAL DISKS

Large storage devices can also be implemented using optical means. The familiar compact disk (CD), used in audio systems, was the first practical application of this technology. The optical technology was also adapted to the computer environment to provide high-capacity read-only storage and referred to as **CD-ROM.**

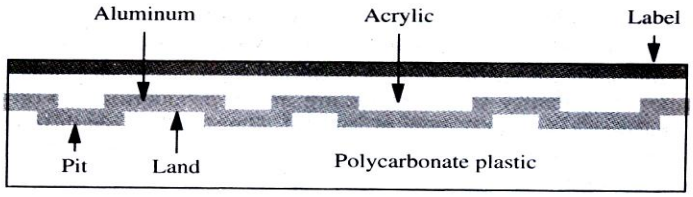
History of CD –ROM

- The first generation of CDs was developed in the mid-1980s by the **Sony and Philips companies.** This technology exploited the possibility of using digital representation of analog sound signals.
- The CDs were required to hold **at least an hour of music**. The first version was designed to hold up to 75 minutes, which requires a total of about **3 x 109 bits (3 gigabits) of storage.**
- A video CD is capable of storing a **full-length movie**. This requires approximately an order of magnitude more bit-storage capacity than that of audio CDs. Multimedia CDs are also suitable for storing large amounts of computer data.

CD Technology

- The optical technology that is used for CD systems is based on a **laser light** source.
- A **laser beam** is directed onto the surface of the spinning disk. Physical indentations in the surface are arranged along the tracks of the disk. They reflect the focused beam toward a photo detector, which detects the stored binary patterns.
- The laser emits a coherent light beam that is sharply focused on the surface of the disk. Coherent light consists of synchronized waves that have the same wavelength.
- If a coherent light beam is combined with another beam of the same kind, and the two beams are in phase, then the result will be a brighter beam.
- If the waves of the two beams are 180 degrees out of phase, they will cancel each other. Thus, if a photo detector is used to detect the beams, it will detect a bright spot in the first case and a dark spot in the second case.

A cross-section of a small portion of a CD is shown below.

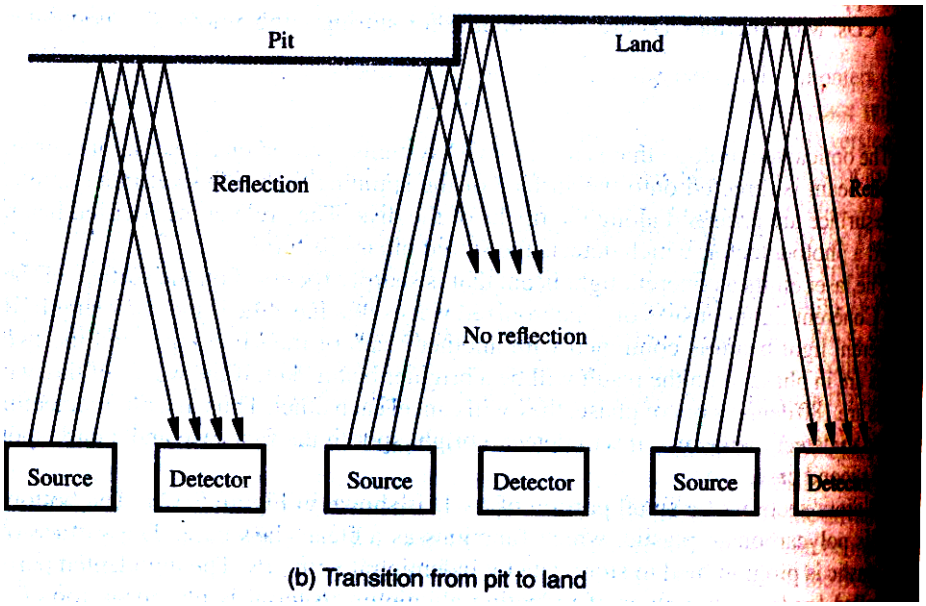


(a) Cross-section

- The bottom layer is polycarbonate plastic, which functions as a clear glass base.
- The surface of this plastic is programmed to store data by indenting it with pits. The unintended parts are called lands.

- A thin layer of reflecting aluminum material is placed on top of a programmed disk. The aluminum is then covered by a protective acrylic.
- Finally, the topmost layer is deposited and stamped with a label. The total thickness of the disk is 1.2 mm. almost all of it is contributed by the polycarbonate plastic. The other layers are very thin.
- The laser source and the photo detector are positioned below the polycarbonate plastic. The emitted beam travels through this plastic, reflects off the aluminum layer, and travels back toward the photo detector. Note that from the laser side, the pits actually appear as bumps with respect to the lands.

Let us see what happens as the laser beam scans across the disk and encounters a transition from a pit to a land.

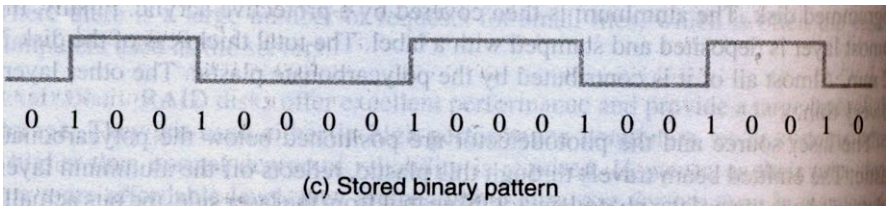


(b) Transition from pit to land

Three different positions of the laser source and the detector are shown, as would occur when the disk is rotating.

- When the light reflects solely from the pit, or solely from the land, the detector will see the reflected beam as a bright spot. But, a different situation arises when the beam moves through the edge where the pit changes to the land, and vice versa.
- The pit is recessed one quarter of the wavelength of the light. Thus, the reflected wave from the pit will be 180 degrees out of phase with the wave reflected from the land, canceling each other. Hence, at the pit – land transitions the detector will not see a reflected beam and will detect a dark spot.

It represents several transitions between lands and pits.



- If each transition detected a dark spot, it is taken to denote the binary values 1, and the flat portions represent 0s, then detected binary pattern will be as shown in the figure.
- This representation is not a direct pattern of stored data. CDs scheme to represent data.
- Each byte of data is represented by a 14-bit code, which provides considerable error detection capability.

CD – ROM

- Since information is stored in binary form in CDs, they are suitable for use as a storage medium in computer systems. The biggest problem is to ensure the integrity of stored data. Because the pits are very small, it is difficult to implement all of the pits perfectly.
- In audio and video applications, some errors in data can be tolerated because they are unlikely to affect the reproduced sound or image in a perceptible way. However, such errors are not acceptable in computer applications.
- Since physical imperfections cannot be avoided, it is necessary to use additional bits to provide error checking and correcting capability.
- CDs used in computer applications have such capability. They are called CD-ROMs, because after manufacture their contents can only be read, as with semiconductor ROM chips.
- Stored data are organized on CD-ROM tracks in the form of blocks that are called sectors. There are several different formats for a sector. One such format is known as Mode 1.

Mode 1

- Mode 1, uses 2352-byte sectors.
- There is a 16-byte header that contains a synchronization field used to detect the beginning of the sector and addressing information used to identify the sector. This is followed by 2048 bytes of stored data.
- At the end of the sector, there are 288 bytes used to implement the error-correcting scheme. The number of sectors per track is variable; there are more sectors on the longer outer tracks.
- Error detection and correction is done at more than one level. Each byte of stored information is encoded using a l4-bit code that has some error-correcting capability.

This code can correct single-bit errors. Errors that occur in short bursts, affecting several bits, are detected and corrected using the error-checking bits at the end of the sector.

- CD-ROM drives operate at a number of different rotational speeds. The basic speed, known as IX, is 75 sectors per second. This provides a data rate of 153,600 bytes/s (150 Kbytes/s), using the Mode 1 format.
- CD-ROMs are widely used for the distribution of software, databases, large texts (books), application programs, and video games.

CD - Recordable

- A new type of CD was developed in the late 1990s on which data can be easily recorded by a computer user. It is known as CD-Recordable (CD-R).
- A spiral track is implemented on a disk during the manufacturing process.
- A laser in a CD-R drive is used to burn pits into an organic dye on the track. When a burned spot is heated beyond a critical temperature, it becomes opaque. Such burned spots reflect less light when subsequently read. The written data are stored permanently.
- Unused portions of a disk can be used to store additional data at a later time.

CD - Rewritable

- The most flexible CDs are those that can be written multiple times by the user. They are known as CD-RWs (CD-ReWritables).The basic structure of CD- RW s is similar to the structure of CD- Rs.
- Basic structure of CD-RWs is similar to CD-RWs uses an alloy of silver, indium, antimony and tellurium in the recording surface instead of organic dye as in case of CD-Rs. This alloy has interesting and useful behavior when it is heated and cooled. If it is heated above its melting point (500 degrees C) and then cooled down, it goes into an amorphous state in which it absorbs light.
- But, if it is heated only to about 200 degrees C and this temperature is maintained for an extended period a process known as annealing takes place, which leaves the alloy in a crystal1ine state that allows light to pass through.
- If the crystalline state represents land area, pits can be created by heating selected spots past the melting point. The stored data can be erased using the annealing process, which returns the alloy to a uniform crystalline state.
- A reflective material is placed above the recording layer to reflect the light when the

disk is read.

The CD-RW drive uses three different laser powers.

- ✓ The highest power is used to record the pits.
- ✓ The middle power is used to put the alloy into its crystalline state; it is referred to as the "erase power."
- ✓ The lowest power is used to read the stored information. There is a limit on how many times a CD-RW disk can be rewritten. Presently, this can be done up to 1000 times.

CD-RW drives can usually also deal with other compact disk media. They can read CD-ROMs, and both read and write CD-Rs. They are designed to meet the requirements of standard interconnection interfaces, such as EIDE, SCSI, and USB.

Advantage of CD- RW

- ➢ CD-RWs provide a low-cost storage medium.
- ➢ They are suitable for archival storage of information that may range from databases to photographic images.
- ➢ They can be used for low-volume distribution of information, just like CD-Rs.
- ➢ The CD-RW drives are now fast enough to be used for daily hard disk backup purposes. The CD-RW technology has made CD-Rs less relevant because it offers superior capability at only slightly higher cost.

DVD Technology

- ➢ The success of CD technology and the need for greater storage capability has led to the development of DVD (Digital Versatile Disk) technology.
- ➢ The first DVD standard was defined in 1996 by a consortium of companies. The objective is to be able to store a full-length movie on one side of a DVD disk.
- ➢ The physical size of a DVD disk is the same as for CDs. The disk is 1.2 mm thick, and it is 120 mm in diameter.
- ➢ Its storage capacity is made much larger than that of CDs by several design changes:
  - ✓ A red light laser with a wavelength of 635 nm is used instead of the infrared light laser used in CDs, which has a wavelength of 780 nm. The shorter wavelength makes it possible to focus the light to a smaller spot.
  - ✓ Pits are smaller, having a minimum length of 0.4 micron.
  - ✓ Tracks are placed closer together; the distance between tracks is 0.74 micron.

Using these improvements leads to a DVD capacity of 4.7 Gbytes.

Access time

Access times for DVD drives are similar to CD drives. However, when the DVD disks rotate at the same speed, the data transfer rates are much higher because of the higher density of pits.

DVD-5

- Further increases in capacity have been achieved by going to two-layered and two sided disks. Such a disk with double-layer is called DVD-9 in the standard. The total storage capacity of both layers is 8.5 Gbytes.
- A double-layered disk makes use of two layers on which tracks are implemented on top of each other. The first layer is the clear base, as in CD disks. But, instead of using reflecting aluminum, the lands and pits of this layer are covered by a translucent material that acts as a semireflector.
- The surface of this material is then also programmed with indented pits to store data. A reflective material is placed on top of the second layer of pits and lands. The disk is read by focusing the laser beam on the desired layer.
- When the beam is focused on the first layer, sufficient light is reflected by the translucent material to detect the stored binary patterns.
- When the beam is focused on the second layer, the light reflected by the reflective material corresponds to the information stored on this 1ayer. In both cases, the layer on which the beam is not focused reflects a much smaller amount of light, which is eliminated by the detector circuit as noise.

DVD-10

In DVD-10 two single-sided disks can be put together to form a sandwich-like structure where the top disk is turned upside down. This can be done with single-layered disks giving a composite disk with a capacity of 9.4 Gbytes.

DVD18

It is similar to DVD-10 but instead of Single layered it uses double-layered disks yielding a capacity of 17 Gbytes.

DVD RAM

- A rewritable version of DVD devices, known as DVD-RAM, has also been developed. It provides a large storage capacity.
- To ensure that the data have been recorded correctly on the disk, a process known as write verification is performed. This is done by the DVD-RAM drive, which reads

the stored contents and checks them against the original data.

- Disadvantages

  Higher in price

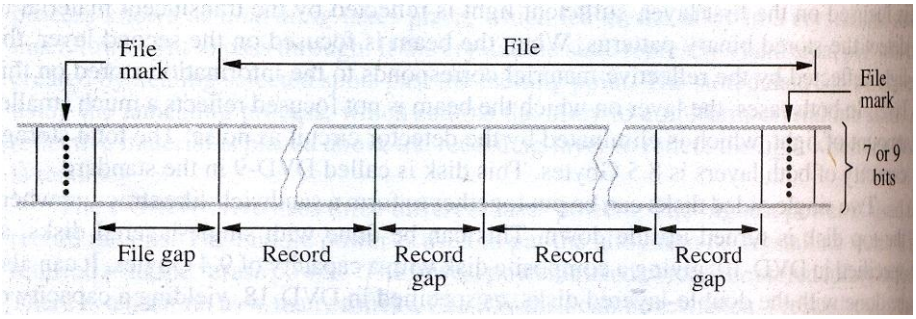
  Relatively slow writing speed.

III. MAGNETIC TAPE SYSTEMS

- Magnetic tapes are suited for off-line storage of large amounts of data. They are typically used for hard disk backup purposes and for archival storage.
- Magnetic-tape recording uses the same principle as used in magnetic-disk recording.
- The main difference is that the magnetic film is deposited on a very thin 0.5- or 0.25-inch wide plastic tape. Seven or 9 bits (corresponding to one character) are recorded in parallel across the width of the tape, perpendicular to the direction of motion.
- A separate read/write head is provided for each, bit position on the tape, so that all bits of a character can be read or written in parallel.

Data on the tape are organized in the form of records separated by gaps, as shown below.

ORGANISATION OF DATA ON A MAGETIC TAPE



- Tape motion is stopped only when a record gap is underneath the read/write heads. The record gaps are long enough to allow the tape to attain its normal speed before the beginning of the next record is reached.
- To help users organize large amounts of data a group of related records is called a file. The beginning of a file is identified by a file mark, as shown in Figure.
- The file mark is a special single- or multiple-character record, usually preceded by a gap longer than the interrecord gap. The first record following a file mark can be used as a header or identifier for this file. This allows the user to search a tape containing a large number of files for a particular file.
- The controller of a magnetic tape drive enables the execution of a number of control commands in addition to read and write commands. Control commands include the

following operations:

- ✓ Rewind tape
- ✓ Rewind and unload tape
- ✓ Erase tape
- ✓ Write tape mark
- ✓ Forward space one record
- ✓ Backspace one record
- ✓ Forward space one file
- ✓ Backspace one file

The tape mark referred to in the operation "Write tape mark" is similar to a file mark except that it is used for identifying the beginning of the tape.

- The end of the tape is sometimes identified by the EOT (end of tape) character.

Two methods of formatting and using tapes:

- ✓ In the first method, the records are variable in length. This allows efficient use of the tape, but it does not permit updating or overwriting of records in place.
- ✓ The second method is to use fixed-length records. In this case, it is possible to update records in place.

Cartridge Tape system

- Tape systems have been developed for backup of on-line disk storage. One such system uses an 8-mm video format tape housed in a cassette. These units are called cartridge tapes.
- They have capacities in the range of 2 to 5 gigabytes and handle data transfers at the rate of a few hundred kilobytes per second.
- Reading and writing is done by a helical scan system operating across the tape, similar to that used in video cassette tape drives. Bit densities of tens of millions of bits per square inch are achievable.
- Multiple-cartridge systems are available that automate the loading and unloading of cassettes so that tens of gigabytes of on-line storage can be backed up unattended