UNIT - I
BOOLEAN ALGEBRA AND LOGIC GATES
PART - A

1. How many bits are required to represent the decimal numbers in the range 0 to 999 using straight binary code? Using BCD codes?

$(999)_{10} = (1111100111)_2 \rightarrow$ 10 bits are required using straight binary code

$(999)_{10} = (1001\ 1001\ 1001)_{BCD} \rightarrow$ 12 bits are required using BCD code

2. Show that the excess-3 code is self-complementing.

Self-complementing property: 1's complemfent of XS-3 code of a decimal digit is equal to XS-3 code of 9's complement of the corresponding decimal digit.

Example:

XS-3 code of the decimal digit 2 = 0101
1's complement of 0101 = 1010 ----------(1)
9's complement of 2 = 9-2 = 7
XS-3 code of 7 = 1010 ----------(2)

The self- complementing property of XS-3 code is proved from equations (1)&(2)

3. How is the letter A coded as in the ASCII code?

7-bit ASCII code for the Letter A is 1000001

4. What is meant by weighted and non-weighted code?

- **Weighted codes** are those, which obey the positional weighting principles. In weighed code, each position of the number represents a specific weight.
  Example: 8421, 2421 & 84-2-1.
- **Non-Weighted Codes** are codes that are not positionally weighted. Each position of the number is not assigned a fixed value.
  Example: Excess-3 & Gray code

5. Add the decimals 67 and 78 using excess-3 code.

$67 = (0110\ 0111)_{BCD} = (1001\ 1010)_{XS-3}$
$78 = (0111\ 1000)_{BCD} = (1010\ 1011)_{XS-3}$

```
------------------------------
   1  0100  0101 ( + )
0011  0011  0011
------------------------------
(0100  0111  1000 )XS-3
------------------------------
```

6. Add the decimals 57 and 68 using 8421 BCD code.

$57 = (0101\ 0111)_{BCD}$
$68 = (0110\ 1000)_{BCD}$

```
-------------------------
     1011  1111 ( + )
     0110  0110
-------------------------------
(0001  0010  0101 )BCD
-------------------------------
```

7. Write the two properties of Gray code & mention the application of Gray code

Properties:

- The gray code is non-weighted code, which means that there are no specific weights assigned to the bit positions.
- In gray code, only one bit changes from one number to the next.

Application: Shaft position encoder in which analog data are represented by continuous change of a shaft position. The shaft is partitioned into segments, and each segment is assigned a number.

8. Use De Morgan's theorem to convert the following expressions to one that has only single variable inversions?

a) $Y = (RS'T+Q')' = (R'+S+T')Q$

b) $Z = [(A+BC)(D+EF)]' = (A+BC)'+(D+EF)$
$Z = A'(BC)' + D'(EF)' = A'(B'+C') + D'(E'+F') = A'B'+A'C'+D'E'+D'F'$

c) $X = [(A'+C)(B+D')]' = (A'+C)' + (B+D')' = AC'+B'D$

9. State & prove De-Morgan's theorem.

De-Morgan's theorem 1: The complement of product of any number of variables is equivalent to sum of the individual complements.

De-Morgan's theorem 2: The complement of sum of any number of variables is equivalent to product of the individual complements.

Proof:

a) (AB)' = A' + B'

A	B	AB	**(AB)'**		A'	B'	**A'+B'**
0	0	0	**1**		1	1	**1**
0	1	0	**1**		1	0	**1**
1	0	0	**1**		0	1	**1**
1	1	1	**0**		0	0	**0**

b) (A+B)' = A'B'

A	B	A+B	**(A+B)'**		A'	B'	**A'B'**
0	0	0	**1**		1	1	**1**
0	1	1	**0**		1	0	**0**
1	0	1	**0**		0	1	**0**
1	1	1	**0**		0	0	**0**

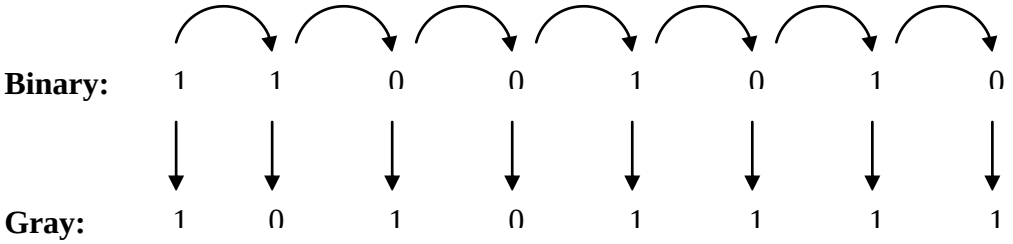
10. Write the maxterm for M_{45} using minimum number of variables.

$(45)_{10}$ = 101101 = A' + B + C' + D' + E + F'

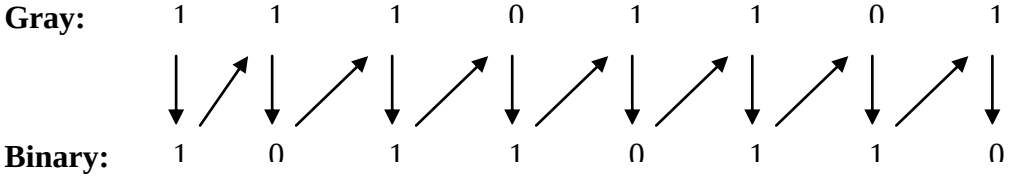
11. a) Convert $(11001010)_2$ into gray code.

b) Convert a Gray code 11101101 into binary code.

Binary to Gray code conversion:



Gray to Binary code conversion:



12. Define distributive law.

a) X (Y + Z) = XY + XZ

b) X + YZ = (X + Y) (X + Z)

13. Simplify the expression: X = (A'+B)(A+B+D)D'

X = (A'+B)(A+B+D)D' = (AA' + A'B + A'D + AB + BB + BD)D'

X = (0 + A'B + A'D + AB + B + BD)D'

X = (A'D + B(A' + A + 1 + D))D' = (A'D + B)D'

X = A'DD' + BD' = 0 + BD'

X = BD'

14. Simplify the expression using Demorgan's theorems Y = [A(B+C')D]'

Y = [A(B+C')D]' = A' + B'C +D'

15. Describe the canonical forms of the Boolean function.

a) Sum of minterms: Combination of minterms using OR operation

Minterm (standard product) is a combination of n variables using AND operation for the function of n variables.

Example for function of two variables A & B

F = A'B + AB = $m_1 + m_3$

F = $\sum m(1,3)$

b) Product of maxterms: Combination of maxterms using AND operation.

Maxterm (standard sum) is a combination of n variables using OR operation for the function of n variables.

Example for function of two variables A & B
$F = (A+B)(A'+B) = M_0 M_2$
$F = \prod M(0,2)$

16. Describe the importance of don't care conditions.

- Functions that have unspecified outputs for some input combinations are called incompletely specified functions. We simply don't care what value is assumed by the function for the unspecified minterms.
- The unspecified minterms are called don't care conditions.

These don't care conditions can be used on a map to provide further simplification of the Boolean expression.

17. Give the canonical product form of $F=x_1'x_2'x_3+x_1'x_2x_3'+x_1x_2'x_3'+x_1'x_2x_3$

$F=x_1'x_2'x_3+x_1'x_2x_3'+x_1x_2'x_3'+x_1'x_2x_3$
$F=001+010+100+011 = m_1+m_2+m_4+m_3$
$F=\sum m\ (1, 2, 3, 4)$ ----------This is Sum form of F. Collecting the missing terms in the Sum form of F derives the product form of F.
Product form:
$F=\prod M\ (0, 5, 6, 7) = M_0 M_5 M_6 M_7$
F=(000) (101) (110) (111)
$F=(x_1+x_2+x_3)(x_1'+x_2+x_3')(x_1'+x_2'+x_3)(x_1'+x_2'+x_3')$

18. Simplify Y = (A+B)(A'+C)

Y = (A+B)(A'+C) = AA' + AC + A'B + BC = 0 + AC + A'B + BC
Y = AC + A'B + BC
Y = AC + A'B ---------using consensus theorem XY+X'Z+YZ=XY+X'Z

19. What is a prime implicant?

A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map.
Example: The possible prime implicants in the following K-Map are A'B' & AB

A \ BC	00	01	11	10
0	1 (0)	1 (1)	0 (3)	0 (2)
1	0 (4)	0 (5)	1 (7)	1 (6)

20. Give the canonical SUM form of F

$F=(x_1+x_2+x_3)(x_1'+x_2+x_3')(x_1'+x_2'+x_3)(x_1'+x_2'+x_3')$
F=(000) (101) (110) (111) = $M_0 M_5 M_6 M_7$
$F=\prod M\ (0, 5, 6, 7)$ ----------This is product form of F. Collecting the missing terms in the Product form of F derives the SUM form of F.
SUM form:
$F=\sum m\ (1, 2, 3, 4) = m_1+m_2+m_4+m_3$
F=001+010+100+011
$F=x_1'x_2'x_3+x_1'x_2x_3'+x_1x_2'x_3'+x_1'x_2x_3$

21. Write the dual form of F=AB+A'C+BC

$F^D = (A+B)(A'+C)(B+C)$

22. Define the following: minterm and maxterm?

- **Minterm** (standard product) is a combination of n variables using AND operation for the function of n variables.
- Possible minterms for a function of two variables A & B:
  A'B', A'B, AB', AB
- **Maxterm** (standard sum) is a combination of n variables using OR operation for the function of n variables.
- Possible maxterms for a function of two variables A & B:
  A+B, A+B', A'+B, A'+B'

23. Write the minterm of m_{32} using minimum number of variables.
(32)10 = 100000 =AB'C'D'E'F'

24. Minimize the function using K-map: F=∑m(1,2,3,5,6,7)

A \ BC	00	01	11	10
0	0 (0)	1 (1)	1 (3)	1 (2)
1	0 (4)	1 (5)	1 (7)	1 (6)

Quad (2,3,6,7) = B
Quad (1,3,5,7) = C

F = B + C

25. Find the complement of x+yz.
F = x + yz
F' = (x + yz)' = x' (y' + z')

26. For a switching function of n variables, how many distinct minterms and maxterms are possible?
2^n distinct minterms and maxterms are possible

27. If A and B are Boolean variables and if A=1 and (A+B)' = 0, find B.
If B = 0 ; (A + 0)' = (1+0)' = 1' =0
If B = 1 ; (A + 1)' = (1+1)' = 1' =0
So, B takes the value of both '0' & '1'

28. Express the switching function f(BA) = A in terms of minterms.
f(BA) = A(1) = A (B+B') = AB + AB'

29. Apply DeMorgans theorems to simplify (A+BC')'.
(A+BC')' = A' (BC')' = A' (B' + C)

30. Plot the expression on K-map: F(w,x,y) =∑m (0, 1, 3, 5, 6) + d (2, 4)

w \ xy	00	01	11	10
0	1 (0)	1 (1)	1 (3)	X (2)
1	X (4)	1 (5)	0 (7)	1 (6)

31. Simplify A+AB+A'+B
A+AB+A'+B = A+A' + AB + B
= 1+ AB + B ----------(X+X'=1)
= 1 ----------(X+1 = 1)

32. Express x + yz as the sum of minterms.
x + yz = x(1) + (1)yz = x(y + y') + (x + x')yz = xy + xy' + xyz + x'yz
= xy(1) + xy'(1) + xyz + x'yz = xy(z + z') + xy'(z + z') + xyz + x'yz
= xyz + xyz' + xy'z + xy'z' + xyz + x'yz
= xyz + xyz' + xy'z + xy'z' + x'yz ----------(x + x = x)
=111 + 110 + 101 + 100 + 011
=m7 + m6 + m5 + m4 + m3
x + yz =∑m(3, 4, 5, 6, 7)

33. Simplify: a) Y = AB'D + AB'D' b) Z = (A'+B)(A+B)
a) Y = AB'D + AB'D' = AB'(D+D') = (AB') (1) = AB'
b) Z = (A'+B)(A+B) = AA'+A'B+AB+BB
Z = 0+B(A'+A)+B = B+B =B

34. What are Universal Gates? Why are they called so?

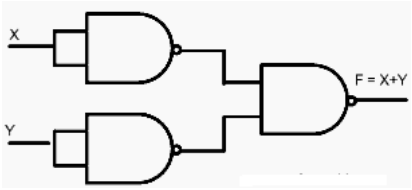
A Universal gates are NAND and NOR ,they are called so because using these codes any logical gate or logical expression can be derived .

35. Define Karnaugh map.

To simplify the Boolean expression that in canonical form, Karnaugh map is used.

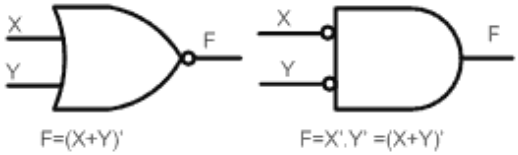
36. Implement OR using NAND only.

Input	Output	Rule
((XX)'(YY)')'	= (X'Y')'	Idempotent
	= X"+Y"	DeMorgan
	= X+Y	Involution



37. Implement NOR using NAND only

Input	Output	Rule
((XX)'(YY)')'	=(X'Y')'	Idempotent
	=X"+Y"	DeMorgan
	=X+Y	Involution
	=(X+Y)'	Idempotent



38. What are the two forms of Boolean expressions?

Two forms of a function, one is a sum of products form (either standard or normal), the other a product of sums form (either standard or normal)

39. What are the limitations of karnaugh map? (May/June 2013)

i) Generally it is limited to six variable map (i.e.) more then six variable involving expressions are not reduced.

ii) The map method is restricted in its capability since they are useful for simplifying only Boolean expression represented in standard form

40. What is tabulation method?

A method involving an exhaustive tabular search method for the minimum expression to solve a Boolean equation is called as a tabulation method

41. What are prime-implicants?

The terms remained unchecked are called prime-implicants. They cannot be reduced further.

42. Write the application of gray code.

- Position encoders
- Towers of Hanoi
- Genetic algorithms
- Karnaugh maps
- Error correction
- Communication between clock domains
- Gray code counters and arithmetic

43. The solution of quadratic equation x^2-11x+22=0 is x=3; x=6. What is the base of numbers?

$x^2 - 11x + 22 = (x - 3) . (x - 6)$

$x^2 - 11x + 22 = x^2 - (6 + 3)x + (6.3)$

$\Rightarrow$ (11)a = (6)a + (3)a

$\Rightarrow$ 1 + a = 6 + 3

$\Rightarrow$ a = 8

44. Find complement and dual of F=x (y'z'+yz).

- Use DeMorgan's law to keep "pushing" the complements inwards

f(x,y,z) = x(y'z' + yz)

f'(x,y,z)= (x(y'z' + yz))' [complement both sides]

= x' + (y'z' + yz)' [because (xy)' = x' + y']
= x' + (y'z')' (yz)' [because (x + y)' = x' y']
= x' + (y + z)(y' + z') [because (xy)' = x' + y', twice]

- Take the dual of the function, and then complement each literal
  If f(x,y,z) = x(y'z' + yz)
  the dual of f is x + (y' + z')(y + z)
  then complementing each literal gives x' + (y + z)(y' + z')
  so f'(x,y,z) = x' + (y + z)(y' + z')

45. What is the significance of BCD code? (Nov/Dec 2012)

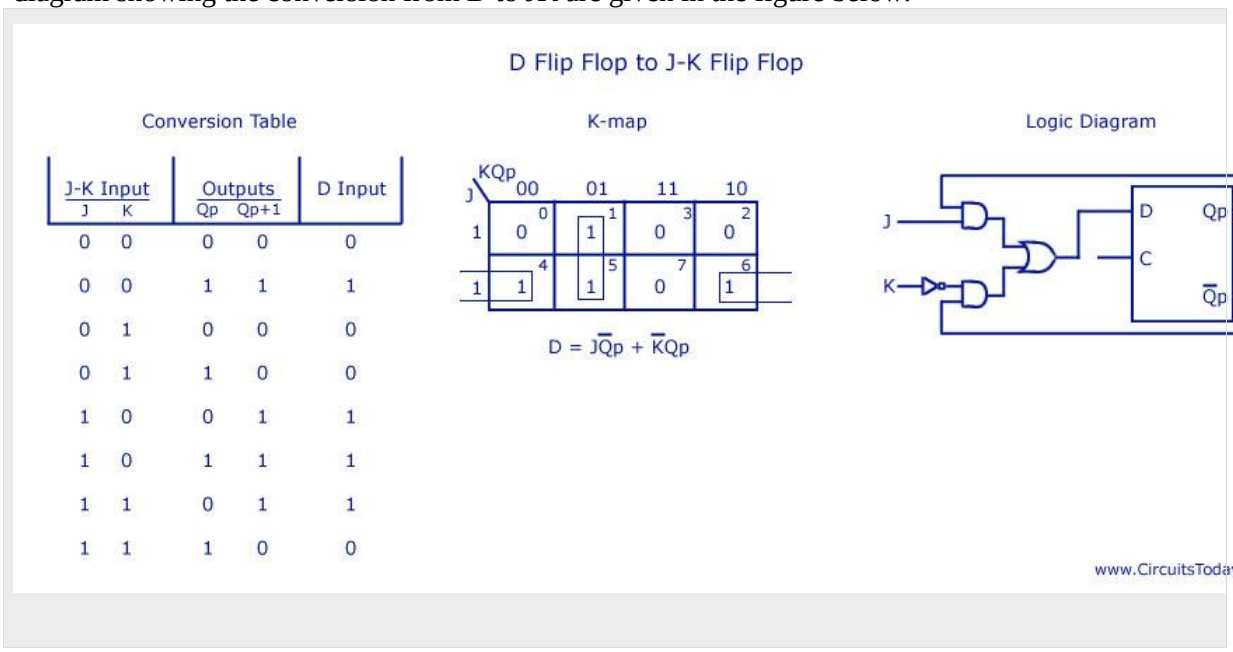
a. Any large decimal number can be easily converted into corresponding binary number
b. A person needs to remember only the binary equivalents of decimal number from 0 to 9.
c. Conversion from BCD into decimal is also very easy.

46. Convert the following hexadecimal numbers into decimal numbers: (May/June 2012)
(a) 263 (b)1C3

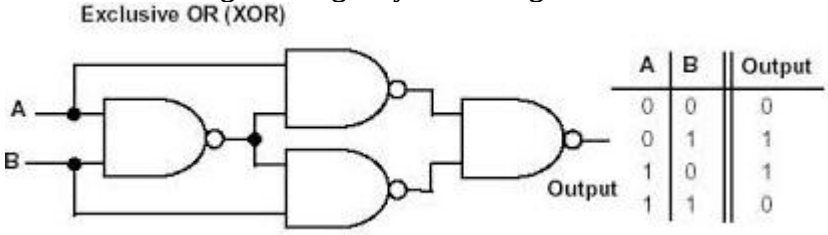
263H= 2x16x16+6x16+3x1=611
1C3H=1x16x16+12x16+3x1=451

47. Realize JK flip flop using D flip flop. (Nov/Dec 2013)

In this conversion, D is the actual input to the flip flop and J and K are the external inputs. J, K and Qp make eight possible combinations, as shown in the conversion table below. D is expressed in terms of J, K and Qp. The conversion table, the K-map for D in terms of J, K and Qp and the logic diagram showing the conversion from D to JK are given in the figure below.



36. Realize XOR gate using only 4 NAND gates. (Nov/Dec 2013)



PART-B

1. Discuss about various codes in digital system.

2. Find the complement of $A\overline{B} + \overline{B}C + C\overline{D}$.

3. What is K-map? Why we need K-maps? Give the various types of K-map.

4. Solve following using K-map and Boolean algebra:

(i) F (A, B) = Σm (1, 3)
(ii) F (A, B) = Σm (0, 2)
(iii) F (A, B) = Σm (1, 2)

5. Solve following using K-map and boolean algebra:

(i) F (A, B, C) = Σm (2, 3)

(ii) F (A, B, C) = Σm (1, 3, 5, 7)

(iii) F (A, B, C) = Σm (0, 4, 1, 3, 6)

6. Solve the following using K-map and verify by using boolean algebra:

F (A, B, C, D) = Σm (3, 4, 5,7, 9, 13, 14, 15)

7. Solve the following using k-map:

f (A, B, C, D) = Σm (0,2, 3, 8, 11, 12) + d (1,9, 14)

8. Find the maxterms for the expression $F = A\bar{C} + AB\bar{C} + \bar{A}BC$

9. Construct the truth table for F = $x\bar{y} + \bar{x}y$

10. Convert the given expression in canonical SOP form Y = AC + AB + BC

11. Two minterms can be adjacent only if they differ by ……

12. Realize and OR and NOT using NOR gates.

13. Realize X-OR function using NOR gates only.

14. A four-variable function is given as f (A, B, C, D) = Σm (0, 2, 3, 4, 5, 7, 8, 13, 15). Use a K-map to minimize the function.

15. Simplify the expression 2. =AB + AC + ABC (AB + C). Implement using minimum number of NAND gates.

16. A four-variable function is given as f (A, B, C, D) = ∑M (0, 3, 4, 5, 6, 7, 11, 13, 14, 15) Use a K-map to minimize the function.

17. Realize OR, AND, NOT, NOR gates using NAND gates only.

18. Minimize the function using K-map. f (A, B, C, D) = Σm (0, 1, 2, 3, 5, 7, 8, 9, 11,14)

19. Obtain the minimal SOP expression for (0, 1, 2, 4, 6, 9. 11, 12, 13) and implement it in NAND logic.

20. Obtain the minimal POS expression for πM (0, 1, 2, 4, 5, 6, 9, 11, 12, 13, 14, 15) and implement it in NOR logic.

21. Simplify the function using Karnaugh map and implement using minimum Lumber of logic gates. F = (2, 9, 10, 12, 13) + D(1, 5, 14) What are the limitations of Karnaugh map?

22. Minimize the following function by Quine Mccluskey method and list all prime implicants of essential prime implicants. Is the minimum SOP unique, if not all the minimal solutions for the functions?

F (a,b,c,d,e,f) = (0,2,4,7,8,16,24,32,36,40,48) + d (5,18,22,23,54,56)

23. i) Define prime implicant and essential prime implicant.

ii) Procedure logic diagram with NAND gate from Boolean function.

iii) Implement $F(x,y,z)=\Sigma_m(1,2,3,4,5,7)$ with NAND gates.

24. Minimize the following function by Quine Mccluskey method. Y'=A'BC'D'+A'BC'D+ABC'D'+ABC'D+AB'C'D+A'B'CD'.

25. i) Simplify $F(A,B,C,D)=\Sigma_m(0,1,2,5,8,9,10)$ in SOP, POS using K map.

ii) Write notes on negative/positive logic.

26. Simplify $F(A,B,C,D)=\Sigma_m(1,4,6,7,8,9,10,11,15)$ using Quine Mccluskey method. Check if NOR operator is associative.

27. i) State the differences between 1's complement and 2's complement subtraction with suitable examples. (May/June 2012)

ii) Determine the hamming format for the data 1010.

28. i) State and prove DeMorgan's theorem. (May/June 2012)

ii) Simplify the following using K-map.

F (A, B, C, D) = Σm (3, 4, 5,7, 9, 13, 14, 15)

29. Simlify the following Boolean function F using K-map method. (Nov/Dec 2012)

i) F (A, B, C, D) = ∑m (0,2,4,5,8,14,15) ,d (A, B, C, D)= ∑m (7,10,13)

ii) F (A, B, C, D) = ∑m (4,6,7,8,12,15) ,d (A, B, C, D)= ∑m (2,3,5,10,11,14)

30. Simlify the following Boolean function F using Tabulation method. (Nov/Dec 2012)

i) F (A, B, C, D) = ∑m (0,6,8,13,14) ,d (A, B, C, D)= ∑m (2,4,10)

ii) F (A, B, C, D) = ∑m (1,3,5,7,9,15) ,d (A, B, C, D)= ∑m (4,6,12,13)

31. Reduce the following function using K-map technique. (May/June 2013)

i) f (A, B, C) = ∑m (0,1,3,7) + ∑d (2,5)

ii) F (w,x,y,z) = ∑m (0,7,8,9,10,12) + ∑d (2,5,13)

32. Simplify the Boolean function using Quine McCluskey method: (May/June 2013)

F (A, B, C, D,E,F) = ∑m (0,5,7,8,9,12,13,23,24,25,28,29,37,40,42,44,46,55,56,57,60,61)

33. Simplify the Boolean function using Quine McCluskey method: (Nov/Dec 2013)

F (A, B, C, D,E) = ∑m (0,1,3,7,13,14,21,26,28) + ∑d(2,5,9,11,17,24)

34. i) Simplify the given boolean function in POS form using K-map and draw the logic diagram using only NOR gates. (Nov/Dec 2013)

F(A,B,C,D)=πM(0,1,4,7,8,10,12,15)+d(2,6,11,14)

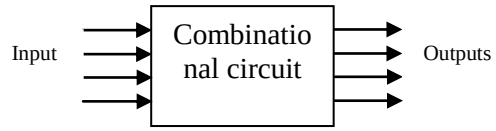
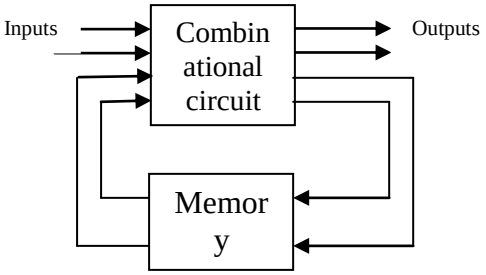
ii) Convert 78.5_{10} into binary.

iii) Find the dual and complement of the following Boolean expression.

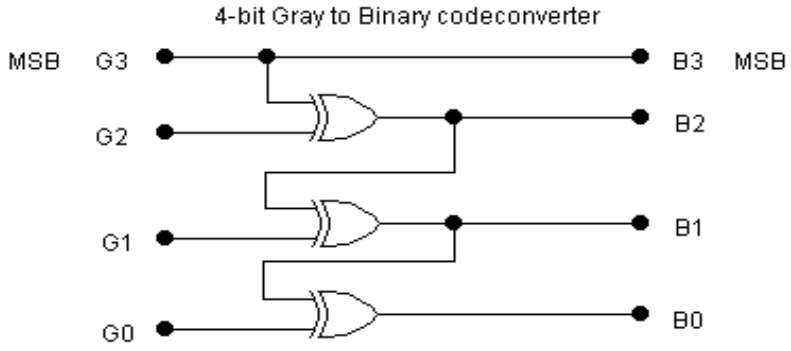
Xyz'+x'yz+z(xy+w).

UNIT 2
COMBINATIONAL LOGIC
PART - A

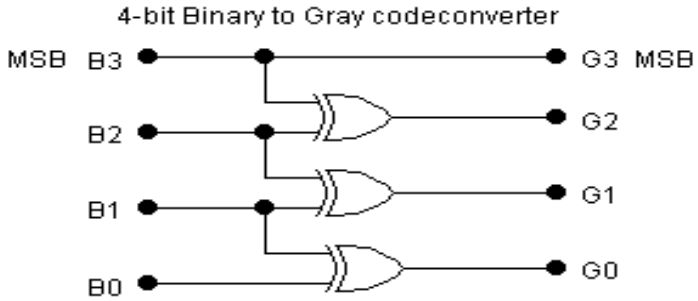
1. Distinguish between combinational logic and sequential logic.

S.No	Combinational logic circuit	Sequential logic circuit
1	Block diagram: 	
2	It consists of input signal, gates and output signals	It consists of a combinational circuit to which memory elements are connected to form a feedback path.
3	The outputs at any instant of time are entirely dependent upon the inputs present at that time.	The outputs dependent not only on the present input variable but they also depend upon the past value of the input variable.
4	Combinational circuits are faster in speed	Sequential circuits are slower than the combinational circuits.
5	Combinational circuits are easy to design	Sequential circuits are comparatively harder to design
6	Example: Parallel adder, Code converter, Decoder	Example: Serial Adder, Counter, shift register

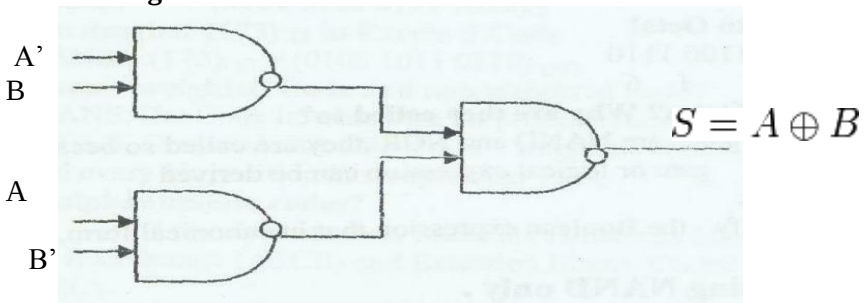
2. Draw the 4 bit Gray to Binary code converter:

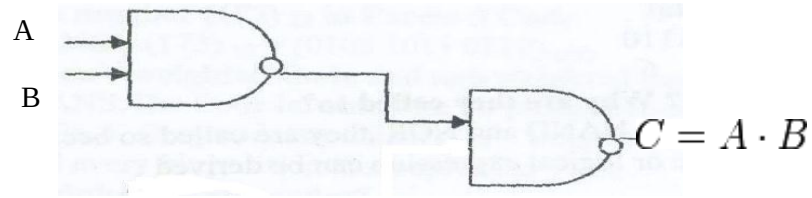


3. Draw the 4 bit Binary to Gray code converter:

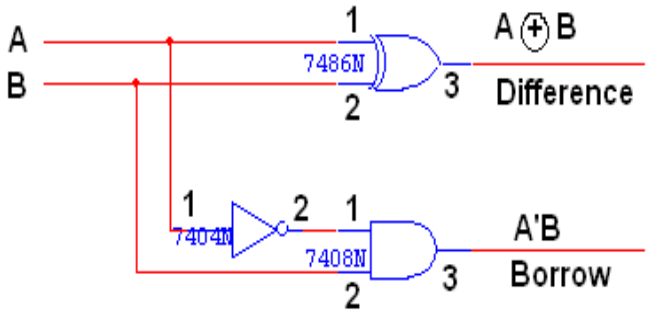


4. Implement half Adder using NAND Gates.





5. Design a half subtractor. **(May/June 2012)**



Truth Table

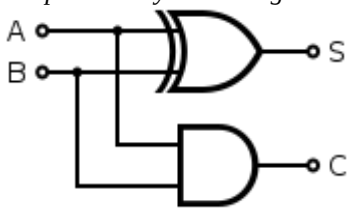
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

6. How many binary outputs would a 3 digit BCD-to-Binary converter have?
12 outputs

7. Define Combinational circuit?
A combinational circuit consists of logical gates whose outputs at any time are determined from the present combination of inputs. A combinational circuit performs an operation that can be specified logically by a set of Boolean functions. It consists of input variables, gates and output variables.

8. What is an ALU?
An ALU is an arithmetic logical Unit. It performs all arithmetical like(Addition, Multiplication, subtraction, division) operations.

9. Give the truth table for half adder and write the expression for sum and carry?



A half adder is a logical circuit that performs an addition operation on two binary digits. The half adder produces a sum and a carry value which are both binary digits.The drawback of this circuit is that in case of a multibit addition, it cannot include a carry.

$$S = A \oplus B \qquad C = A \cdot B$$

Logic table for a half adder:

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

10. Obtain the expression for sum and carry output of a full adder and implement the same.

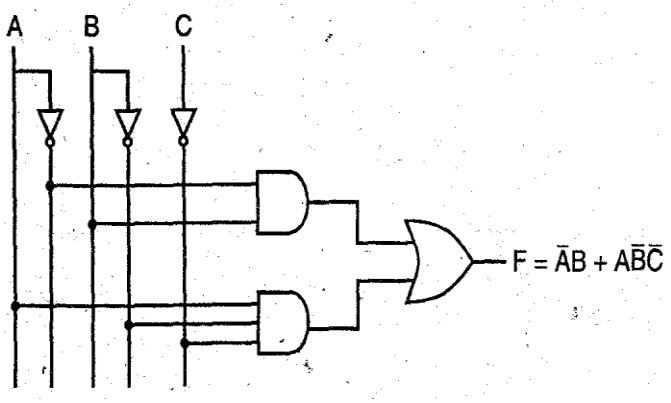
S=z $\oplus$ (X $\oplus$ Y)
= Z'(XY'+X'Y) + Z(XY'+X'Y)'.
= Z'(XYM-X'Y) + Z(XY+X'Y').
= XY'Z'+X'YZ'+XYZ+X'Y'Z.
C = XY'Z+X'YZ+XY.

11. Obtain an expression for difference and borrow outputs of a full subtractor.

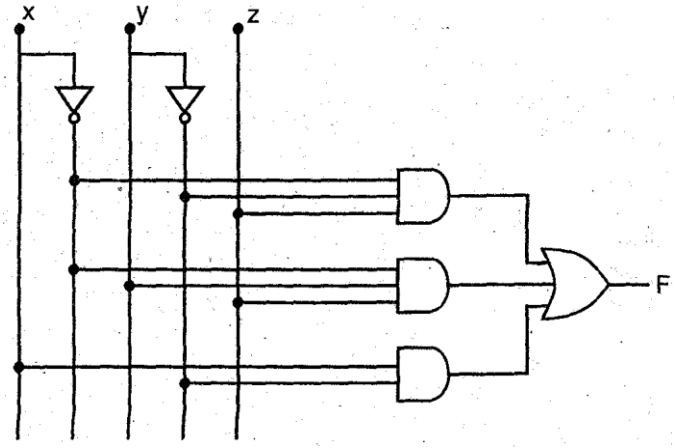
$$\begin{aligned} d &= x'y'b_{in} + xyb_{in} + x'yb'_{in} + xy'b'_{in} \\ &= b_{in}(x'y' + xy) + b'_{in}(x'y + xy') \\ &= b_{in}(x \oplus y)' + b'_{in}(x \oplus y) \\ &= b_{in} \oplus x \oplus y \end{aligned}$$

$$b_{out} = x'b_{in} + x'y + yb_{in}$$

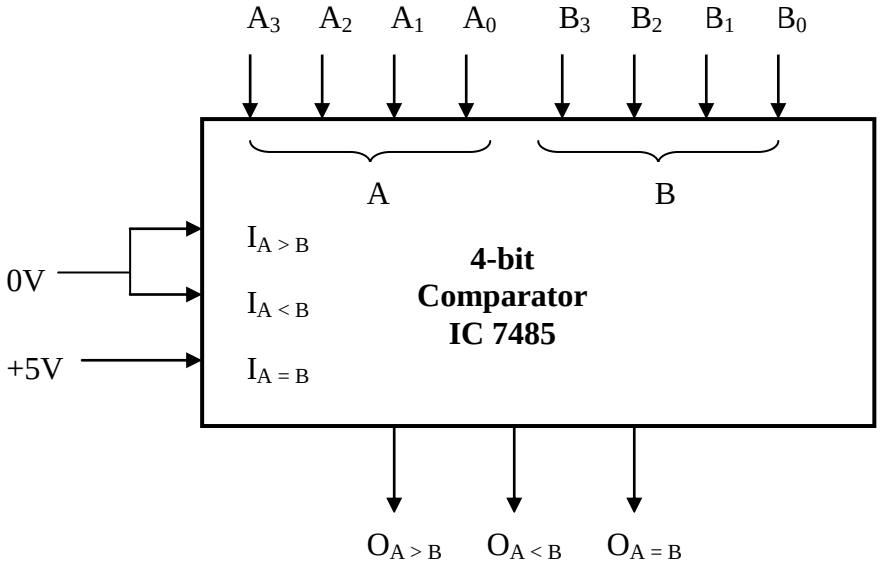
12. Draw the logic circuit for the expression $F = \bar{A}B + A\bar{B}\bar{C}$.



13. Draw the logic circuit for the expression $F = \bar{x}\bar{y}z + \bar{x}y\acute{z} + x\bar{y}$



14. Using a single IC 7485, draw the logic diagram of a 4-bit comparator.



15. What is a half-adder?
The combinational circuit that performs the addition of two bits are called a halfadder

16. What is a full-adder?
The combinational circuit that performs the addition of three bits are called a halfadder.

17. What is half-subtractor?
The combinational circuit that performs the subtraction of two bits are called a half-sub tractor.

18. What is a full-subtractor?
The combinational circuit that performs the subtraction of three bits are called a half- sub tractor.

19. What is Binary parallel adder?
A binary parallel adder is a digital function that produces the arithemetic sum of two binary numbers in parallel.

20. What is meant by self-complementing code?
A self-complementing code is the one in which the members of the number system complement on themselves. This requires the following two conditions to be satisfied.
a. The complement of the number should be obtained from that number by replacing 1s with 0s and 0s with 1s.
b. The sum of the number and its complement should be equal to decimal 9.
Example of a self-complementing code is i. 2-4-2-1 code. ii. Excess-3 code.

21. Mention the advantages of ASCII code?
The following are the advantages of ASCII code

a. There are 27 =128 possible combinations. Hence, a large number of symbols, alphabets etc.., can be easily represented.
b. There is a definite order in which the alphabets, etc.., are assigned to each code word.
c. The parity bits can be added for error-detection and correction.

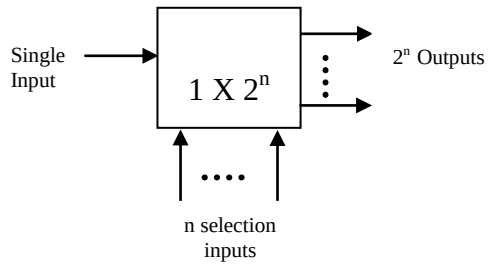
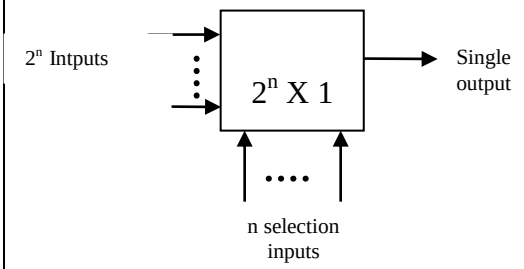
22. What are the disadvantages of ASCII code?
The disadvantages of ASCII code are
a. The length of the code is larger and hence more bandwidth is required for transmission.
b. With more characters and symbols to represent, this is not completely sufficient.

23. What are the needs for binary codes?
a. Code is used to represent letters, numbers and punctuation marks.
b. Coding is required for maximum efficiency in single transmission.
c. Binary codes are the major components in the synthesis (artificial generation) of speech and video signals.
d. By using error detecting codes, errors generated in signal transmission can be detected.
e. Codes are used for data compression by which large amounts of data are transmitted in very short time.

24. Mention the different type of binary codes?
The various types of binary codes are,
1. BCD code (Binary Coded decimal). 2. Self-complementing code. 3. The excess-3 (X's-3) code. 4. Gray code. 5. Binary weighted code. 6. Alphanumeric code. 7. The ASCII code. 8. Extended binary-coded decimal interchange code (EBCDIC). 9. Error-detecting and error-correcting code. 10. Hamming code.

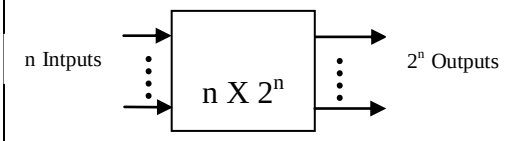
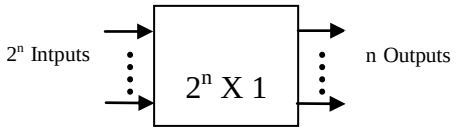
25. List the advantages and disadvantages of BCD code?
The advantages of BCD code are
a. Any large decimal number can be easily converted into corresponding binary number
b. A person needs to remember only the binary equivalents of decimal number from 0 to 9.
c. Conversion from BCD into decimal is also very easy.
The disadvantages of BCD code are
a. The code is least efficient. It requires several symbols to represent even small numbers.
b. Binary addition and subtraction can lead to wrong answer.
c. Special codes are required for arithmetic operations.
d. This is not a self-complementing code.
e. Conversion into other coding schemes requires special methods.

26. Mention the difference between a DEMUX and a MUX

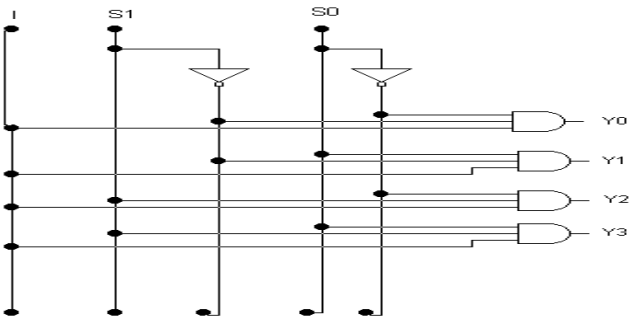
S.No	DEMUX	MUX
1	Block diagram: 	
2	A demultiplexer is a circuit that receives information on a single line and transmits this information on one of many output lines	A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line.
3	Data Distributor	Data selector

27. Give some of the major applications of multiplexers.
a. Data selection b. Data routing c. Operation sequencing d. Parallel to serial conversion e. Waveform generation f. Logic-function generation

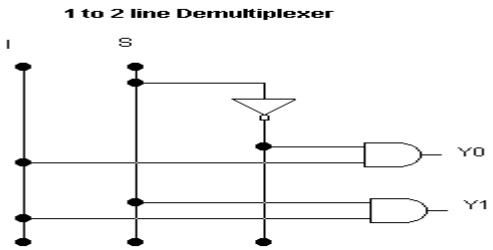
28. How does an encoder differ from a decoder?

S.No	Decoder	Encoder
1	Block diagram: 	
2	A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.	An encoder is a digital circuit that performs the reverse operation of a decoder. An encoder has 2^n input lines and n output lines.
3	A decoder accepts a set of binary inputs and activates only the output that corresponds to that input number.	An encoder generates the binary code corresponding to the input activated.
4	Example: Binary to Octal decoder	Example: Octal to Binary encoder.

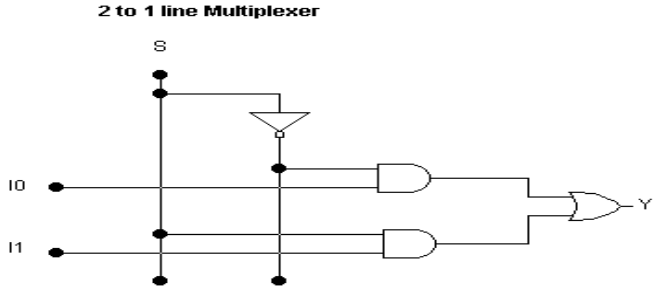
29. Draw the logic diagram of a one to four line demultiplexer.



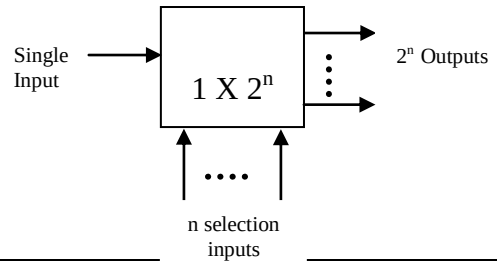
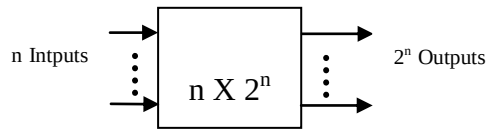
30.Draw a 1 to 2 demultiplexer circuit.



31. Draw a 2 to 1 multiplexer circuit.



32. Distinguish between a decoder and a demultiplexer. (May/June 2013) (May/June 2012)

S.No	DEMUX	DECODER
1	Block diagram: 	

2	A demultiplexer is a circuit that receives information on a single line and transmits this information on one of many output lines	A decoder accepts a set of binary inputs and activates only the output that corresponds to that input number.
3	Data Distributor	Decoder with enable input is used as demultiplexer.

33. What is priority encoder?

A priority encoder is an encoder circuit that includes the priority function. The operation of the priority encoder is such that if two or more inputs are activated at the same time, the output binary code will be generated to the highest-numbered input.

34.Define SSI and MSI.

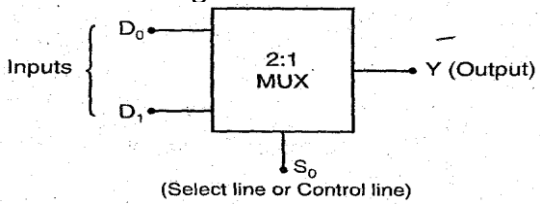
SSI: Small scale integration- less than 10 logic Gates are fabricated in a single chip.

MSI: Medium scale Integration-Logic components fabricated in single packages has an volumes less than 100. These Ics are used for digital operation for decoders, demux, adders etc.

35. List the applications of decoders.

1. Decoders are used in counter systems
2. Decoders are used for A/D conversion.
3. Decoders are used for D/A conversion
4. Decoders are used in seven segment digital displays.

36. Give functional block diagram of 2 1 MUX



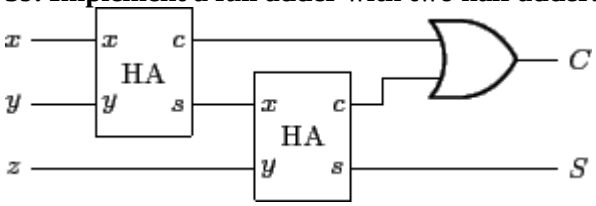
37. Define Tristate gates.

In digital electronics **three-state**, **tri-state**, or **3-state** logic allows an output port to assume a high impedance state in addition to the 0 and 1 logic levels, effectively removing the output from the circuit. This allows multiple circuits to share the same output line or lines (such as a bus which cannot listen to more than one device at a time).

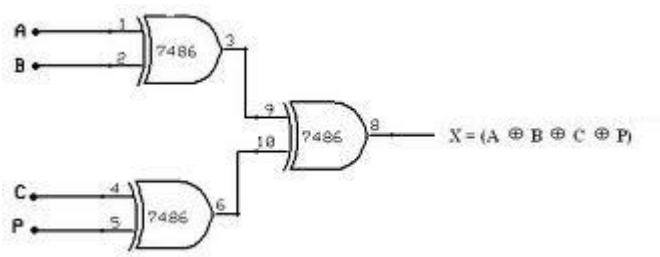
38. Define logic synthesis and simulation.

Logic synthesis is an automatic process of transforming a high level language description such HDL into an optimized net list of gates that perform the operations specified by the source code. Simulation is the representation of the structure and behavior of a digital logic system through the use of a computer. A simulator interprets the HDL description and produces output, such as timing diagram, that predicts how the hardware will behave before it is actually fabricated.

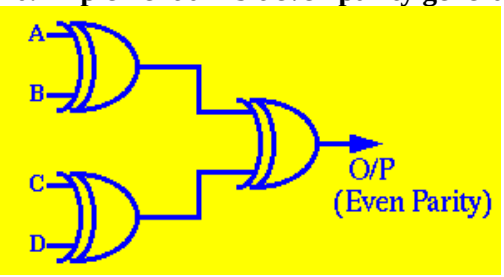
39. Implement a full adder with two half adder.



40. Implement a 4 bit even parity checker.



40. Implement a 4 bit even parity generator.



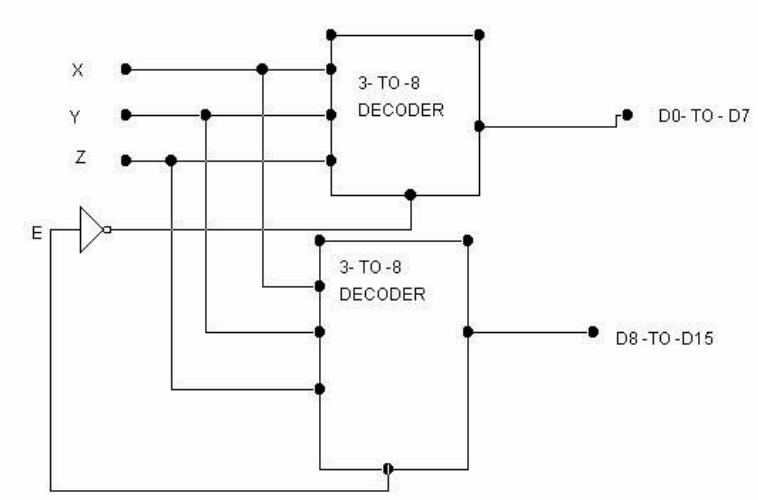
41. Write HDL behavioural description of 4 bit comparator with 6 bit output y[5:0]. Bit 5 of y->equal, bit 4 -> unequal, bit 3 -> >, bit 2 -> <, bit 1 -> >=, bit 0 -> <=.

```
Module comparatot(eq,greater,lesser,greatereq,lesseq,a,b);
Input [3:0] a,b;
Output eq,greater,lesser,greatereq,lesseq;
begin
If(a==b)
y[5]=1'b1 else
If (a!=b)
y[4]=1'b1 else
if(a>b)
y[3]=1'b1 else
if(a<b)
y[2] =1'b1 else
if(a>=b)
y[1]=1'b1 else
if(a<=b)
y[0]=1'b1;
endmodule
```

42. Write the stimulus for 2 to 1 line Mux. (May/June 2012)

```
module exm4_6(A,B,S,O);
input A,B,S;
output O;
assign O=S ? A:B;
endmodule
```

43. Construct 4X16 decoder using 3X8 decoder.



44. Write down the truth table of a full subtractor. (May/June 2013)

Inputs			Difference	Borrow
X	Y	Z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

45. Obtain the truth table for BCD to Excess-3 code converter. (Nov/Dec 2013)

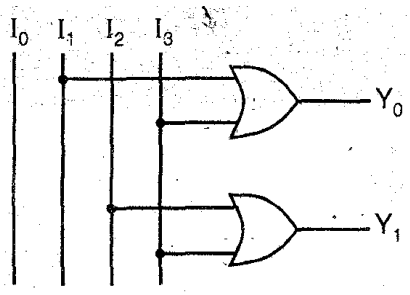
Decimal	BCD				Excess – 3 code			
	A	B	C	D	E_3	E_2	E_1	E_0
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	1	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	0	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

46. Draw the truth table and circuit diagram of 4 to 2 encoder. (Nov/Dec 2013)

The Truth-table is as:

Input		Output	
		Y_0	Y_1
I_0	0	0	0
I_1	1	0	1
I_2	2	1	0
I_3	3	1	1

Circuit diagram

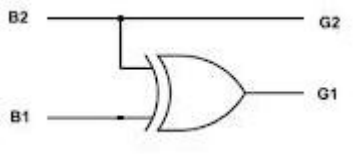


47. Design a 2-bit binary to gray code converter. (May/June 2012) (Nov/Dec 2012)

Truth Table

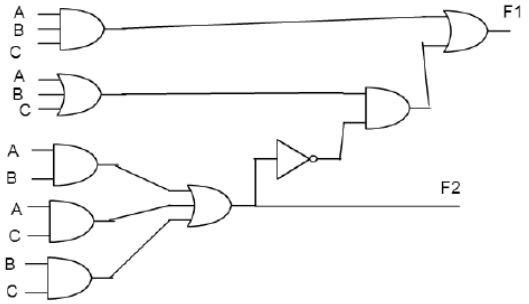
Binary B2B1	Gray G2G1
00	00
01	01
10	11
11	10

Circuit Diagram



PART - B

1. Design 3 bit Gray Code to binary converters
2. Design BCD to Excess-3 code converter.
3. Design full subtractor using NAND gates.
4. Design a Gray-to Excess-3 Code converter using NAND gates
5. Discuss the need and working principle of Carry Look ahead adder. (Nov/Dec 2012)
6. Draw the circuit of a 3 bit binary subtractor and explain its operation with the help of an example
7. Design a Gray to Excess-3 code converter using NOR gates.
8. Design the circuit for one bit comparator.
9. Design a full adder circuit using NAND gates only
10. Design a combinational circuit to perform BCD addition. (Nov/Dec 2013)
11. Write note on 3 bit binary magnitude comparator.
12. Realize the circuit of a full adder in terms of two half adders from its truth table.
13. What are Magnitude comparators" Explain the design of magnitude comparators with the help of a suitable example
14. Construct 16-bit comparator using 4-bit comparator as a building block.
15. Design Half/Full Subtractor circuits.
16. Design 8421 BCD code to Excess 3 code.
17. i) Analyze the circuit give truth table and Boolean expression.



ii) Explain BCD adder.
18. i) Design BCD to excess 3 code.
ii) Draw 4 bit adder/subtractor using full adder.
19. Implement half adder circuit using 4 : 1 MUX or multiplexers only.
20. Implement using 4: 1 MUX $F = \Sigma m\ (0, 3, 4, 7)$
21. Draw the logic circuit for the expression $F = \bar{A}B + A\bar{B}\bar{C}$.
22. Draw the logic circuit for 3 line to 8 line decoder
23. Draw the logic circuit for the expression $F = \bar{x}\bar{y}z + \bar{x}y\acute{z} + x\bar{y}$
24. How many select lines are there for a 30 to 1 MUX?
25. Implement using 4 x 1 MUX $F = \Sigma m\ (0, 3, 4, 7)$
26. Describe the operations performed by an encoder and a decoder.
27. Implement the following function using 3 to 8 decoder
$f(A, B, C) = \Sigma m\ (0, 1, 4, 5, 7)$ $f(A, B, C) = \Sigma m\ (0, 1, 4, 5, 7)$
28. Define a demultiplexer Show how to convert a decoder into a demultiplexer indicate how to add a strobe to this system
29. Give the logic diagram of 4-to-2 encoder and explain its importance in design of digital system.
30. Use a 8 x 1 MUX to implement the logic function $F = \Sigma\ m\ (0, 1, 2, 3, 4, 10, 11, 14, 15)$
31. Implement $F(A,B,C,D)=\Sigma_m(1,3,4,11,12,13,14,15)$ **using 8X1 mux.**
32. Design 4 bit priority encoder.
33. Briefly explain about HDL.
34. Write HDL programme for the given circuit.
35. Write HDL for the expression. x = A.B + C1 y = C1
36. Write HDL for MUX in behaviour mode.
37. i) Design full adder using NAND gates. (May/June 2012)
ii) Design a 4-bit 2's complement circuit.
38. i) Design a 4-bit Binary to Excess-3 code converter. (May/June 2012)
ii) Design a BCD Adder using two 4-bit parallel binary adder blocks and additional logic.
39. i) Design a priority encoder and explain its operation. (May/June 2012)

ii) Implement full adder using suitable decoder and additional logic.

40. Design a BCD to 7 segment decoder and implement it by using basic gates. (Nov/Dec 2012)

41. Construct a 4 to 16 line decoder with an enable input using five 2 to 4 line decoders with enable inputs. (Nov/Dec 2012)

42. Design a full adder using 2 half adders. (May/June 2013)

43. Design a combinational circuit to convert binary to gray code. (May/June 2013)

44. Implement the switching function $F=\Sigma_m(0,1,3,4,12,14,15)$ using an 8 input mux. (May/June 2013)

45. i) Design a 4-bit magnitude comparator with three outputs: A>B, A=B & A<B.

ii) Construct a 4-bit odd parity generator circuit using gates. (Nov/Dec 2013)

46. i) Realize 4 x 16 decoder using two 3 x 8 decoders with enable input. (Nov/Dec 2013)

ii) Implement the following function using a multiplexer.

$F(W,X,Y,Z)=\Sigma_m(0,1,3,4,8,9,15)$

UNIT – 3
SYNCHRONOUS SEQUENTIAL LOGIC
PART - A

1. Give the truth table for J-K flip-flop

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

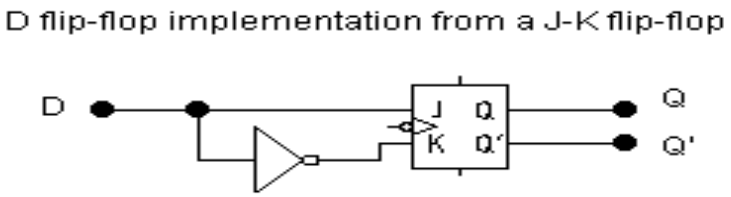
2. What type of FF is best suited for synchronous transfer?

D Flip-Flop is best suited for synchronous transfer.

3. What is meant by the term edge triggered?

Output transitions occur at a leading edge or a trailing edge of the clock pulse.

4. Show D flip-flop implementation from a J-K flip-flop



5. Give the excitation table of J-K flip flop.

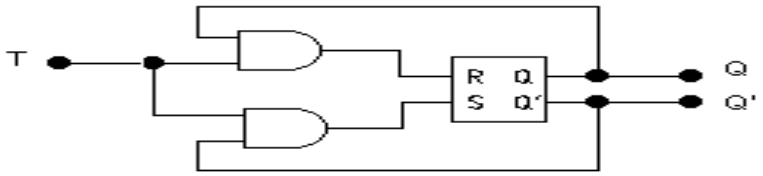
Q	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

6. Write the characteristics table of a D flip flop.

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

7. Show the T flip-flop implementation from S-R flip-flop.

T flip-flop implementation from S-R flip-flop



8. With reference to a JK flip-flop, what is racing?

- Because of the feedback connection in the JK flip-flop, when both J & K are equal to 1 at the same time, the output will be complemented while activating the clock pulse.
- The output is complemented again and again if the pulse duration of the clock signal is greater than the signal propagation delay of the JK flip-flop for this particular input combination (J=K=1)
- There is a race between 0 and 1 within a single clock pulse. This condition of the JK FF is called race-around condition or racing.

9. How do you define Excitation table?

Excitation table consists of two columns, Q(t) and Q(t+1), and a column for each input to show how the required transition is achieved.

10. Define the hold time requirement of a clocked FF?

The input must not change after application of the positive going transition of the pulse. The hold time is equal to the propagation delay of gate.

11. What is meant by triggering of Flip flop?

The state of a flip-flop is switched by a momentary change in the input signal. This momentary change is called a trigger and the transition it causes is said to trigger the flip-flop

12. Differentiate between Flip flop & Latch.

Flip-flop has clocked memory element. Latch has unclocked memory element.

13. Give the truth table of T flip flop.

Q	**T**	**Q(t+1)**
0	0	0
0	1	1
1	0	1
1	1	0

14. Why D FF is known as Delay FF?

The binary information present at the data i/p of the D FF is transferred to the Q o/p when the cp input is enabled. The o/p follows the data i/p as long as the pulse remains in its 1 state. When the pulse goes to 0, the binary information that was present at the data i/p at the time the pulse transition occurred is retained at the Q o/p until the pulse i/p is enabled again. So D FF is known as Delay FF.

15. Distinguish between synchronous and asynchronous counters.

S.No	Synchronous counter	Ripple or Asynchronous counter
1	All the flip-flops are clocked simultaneously	All the flip-flops are not clocked simultaneously.
2	There is no connection between the output of the first flip-flop and the clock input of the next flip-flop	The clock input of each flop-flop is driven by the output of previous flip-flop. External clock is given to the flip-flop that holds LSB of the binary count.
3	As clock is simultaneously given to all flip-flops there is no problem of propagation delay. Hence they are preferred when number of flip-flops increases in the given design	Main draw back of these counters is their low speed as the clock is propagated through number of flip-flops before it reaches last flip-flop.
4	Parallel counter	Serial counter

5	Design involves complex circuit as number of states increases	Logic circuit is very simple even for more number of states

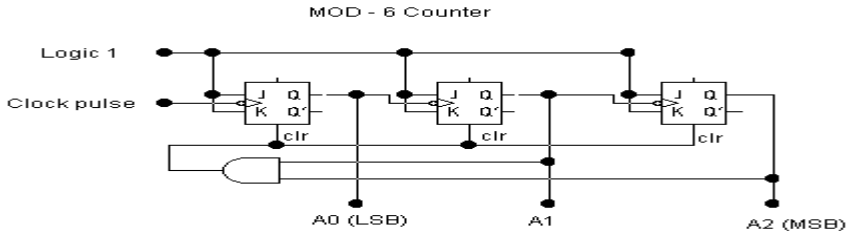
16. Name the two problems that may arise in ripple counters or asynchronous counters.

1. Cumulative flip-flop Delay
2. There is a possibility of glitches occurring at the output of decoding gates used with a ripple counter.

17. Why is parallel counter referred to as synchronous?

In parallel counter all flip-flops are triggered by the same clock at the same time. All flip-flops are synchronized by the common clock signal.

18. Draw a Mod 6 counter using feedback technique.



19. When is a counter said to suffer from lockout?

In a counter if the next state of some unused state is again an unused state and if by chance the counter happens to find itself in the unused states and never arrived at a used state then the counter is said to be in the lockout conditions.

20. What is a self-correcting counter?

A self-correcting counter is one that if it happens to be in one of the unused states, it eventually reaches the normal count (valid state) sequence after one or more clock pulses.

21. Mention why the decoding gates for an asynchronous counter may have glitches on their outputs?

- Since each flip-flop in the asynchronous counter is triggered by the output of the previous flip-flop, the output of each flip-flop is delayed by one flip-flop delay time.
- The accumulated propagation delays serve to essentially limit the frequency response of ripple counter.
- The decoding gates can be connected to the ripple counter to reset the count. The glitches at the output of decoding gates are caused by the delay between the flip-flop outputs.

22. State how an asynchronous down counter differs from an up counter circuit

- In asynchronous up counter each flip-flop is triggered by the normal output of the previous flip-flop.
- Whereas in asynchronous down counter each flip-flop is triggered by the complemented output of the previous flip-flop.

23. What is a ripple counter?

An asynchronous counter in which each flip-flop is triggered by the output of the previous flip-flop.

24. What is the minimum number of flip-flops needed to build a counter of modulus 60?

Modulus $N \leq 2^k$, where k is the number of flip-flops

Modulus $60 < 2^6 = 64$, k = 6

The minimum number of flip-flops needed to build a counter of modulus 60 is 6.

25. What is Shift Register?

A register capable of shifting its binary information either to the right or to the left is called a shift register.

26.What is the major advantage of serial transfer over parallel transfer?

Serial operations require less equipment.

27. What is a universal shift register?

- A register may operate in any of the following five modes

1. SISO 2. SIPO 3. PIPO 4. PISO 5. Bidirectional

- If a register can be operated in all the five possible ways, it is known as Universal Shift Register.

28.A shift register comprises of JK flip-flops. How will you complement the contents of the register?

By setting J and K inputs of all flip-flops to 1 at the same time, we can complement the contents of the shift register (PIPO) that comprises of JK flip-flops.

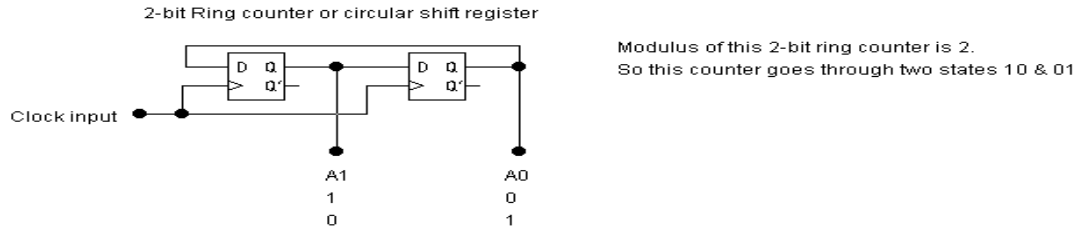
29. Mention the uses of shift registers.

- **Storage Device:** The primary use of shift register is temporary data storage.
- **Time delay generation:** A SISO shift register can be used to introduce time delay T_D between the input and the output digital signals. The time delay can be given as $T_D = N \times (1/f_c)$ Where N is the number of stages and f_c is the clock frequency.
- **Serial-to-Parallel Converter** (SIPO)
- **Parallel-to-serial Converter** (PISO)
- **Shift register counter:** A shift register with the serial output connected back to the serial input is called shift register counter. Because of such a connection, special specified sequences are produced as the output. The most common shift register counters are the ring counter and the Johnson counter.

30. If a serial-in-serial-out shift register has N stages and if the clock frequency is f, what will be the time delay between input and output?

Time delay between input and output = N / f

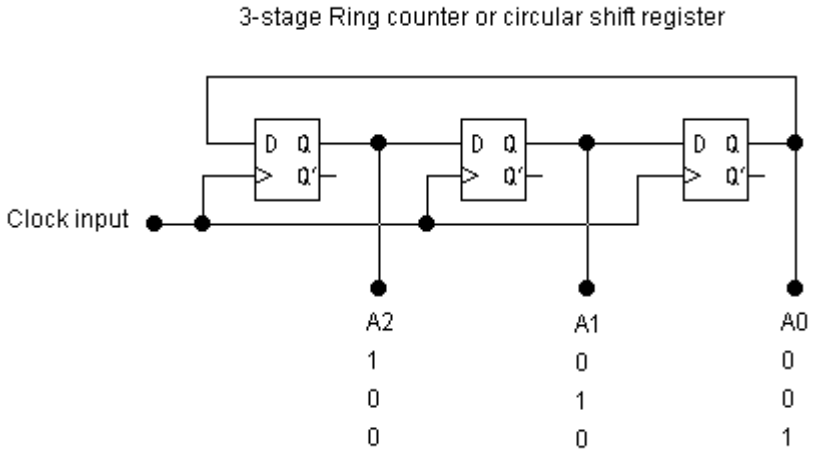
31. Draw the circuit diagram of a basic ring counter.



32. What are Mealy and Moor machines?

- Mealy and Moor machines are two models of clocked or synchronous sequential circuit.
- **Mealy machine:** The output depends on both the present state of the flip-flops and on the inputs.
- **Moore machine:** The output depends only on the present state of the flip-flops.

33. Draw the timing diagram for a 3-stage ring counter.



34. What is a state diagram?

- State diagram is the graphical representation of state table of sequential logic circuits.
- In the state diagram, a state is represented by a circle and the transition between states is indicated by directed lines connecting the circles.

- The directed lines are labeled with two binary numbers separated by a slash. The input value during the present state is labeled first and the number after the slash gives the output during the present state.

35. What is finite state machine?

A finite state machine (or finite automation) is an abstract model describing the synchronous sequential machine and its spatial counter, part, the iterative network

36. What do you meant by the term state reduction problem?

The reduction of the number of flip-flops in a sequential circuit is referred to as the state – reduction problem. State – reduction algorithms are concerned with procedures for reducing the number of states in a state table while keeping the external input – output requirements unchanged.

37. Define Bit time & Word time.

The time interval between clock pulses is called the bit time, and the time required to shift the entire contents of a shift register

38. Give applications of J-K flip-flops.

1. J-K flip-flops are used in shift registers. 2. J-K flip-flops are used in counters.

39. Give difference between latch and flip-flop.

Latch	Flip-flops
1. Latch has an enable input.	1. Flip-flops has a clock signal.
2. As long as enable input is active, the latch output will keep changing according to input.	2. Flip-flop samples its inputs and changes its outputs only at a particular instant of time i.e. when clock is provided.

.

40. How race around condition can be eliminated?

Race around condition can be eliminated in JK latch by two ways

1. Using the edge triggered J-K flip-flop.
2. Using the master slave J-K flip-flop.

41. How many flip-flops are required to count 16 clock pulses? Why?

To count 'n' clock pulses 'm' flip-flops are required, where,

$$n \leq 2^m$$

Thus, for 16 clock pulses to count, 4 flip-flops are required as $2^4 = 16$.

42. Give application of D and T flip-flops.

D flip-flops are delay flip flops and are extensively used for temporary storage of data in registers. Hence, registers make use of D flip-flops.

T flip-flops are toggle flip-flops and are used in counters. Hence, counter designing make use of T flip- flop

43. Differentiate between sequential and combinational circuits.

Combinational Circuits	Sequential Circuits
1. Output depends only on the past values of input.	1. Output depends on the present and past values of input.
2. Feedback path is not used in combinational circuits.	2. Feedback path is used for sequential circuits.
3. Memory element is not present.	3. Memory element is present.
4. Clock is not used in combinational circuits.	4. Clock is used in sequential circuits.
5. Circuit is simple.	5. Circuit is complex.
6. Examples of combinational circuits are: Adders, subtractors, code converters, comparators, multiplexer, de-multiplexer, decoder, encoder, etc.	6. Examples of sequential circuits are : Flip-flops, counters, registers etc.

44. A presettable counter has eight flip-flops. If the preset number is 125, what is the modulus?

$2^8 = 256$ 256 – 125 = 131 Thus, MOD — 131.

45. What is flip-flop?

Flip-flop : Flip-flop is a sequential circuit which is used to store single bit of information at a time i.e. either '1' or '0' at a time. It has two stable output states. It can stay in one of the two stable states unless state is changed by applying external inputs. Thus, it as a basic memory element for storage of data in binary form.There are various types of flip-flops

1. S-R flip flop 2. J-K flip-flop 3. D-type flip flop 4. T-type flip-flop

46. Write the characteristics table and equation of JK flip flop.

("X" is "don't care")

Previous state	**Present state**	**J**	**K**
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Characteristic equation Q(next) = JQ' + K'Q

47. Write any two applications of shift registers.

- Parallel to serial conversion for signal transmission
- Pattern recognition

48. How many flip flops are required to realize MOD 50 counter? (Nov/Dec 2012)

6 flip flops

49. What is ring counter?

A ring counter is a type of counter composed of a type circular shift register. The output of the last shift register is fed to the input of the first register.

50. What is a Mealy circuit? (May/June 2013)

- Mealy circuit is a clocked or synchronous sequential circuit.
- The output depends on both the present state of the flip-flops and on the inputs.

51. Write the HDL code for up-down counter using behavioral model. (Nov/Dec 2013)

```
module behav_counter( d, clk, clear, load, up_down, qd);
input   [7:0] d;
input   clk;
input   clear;
input   load;
input   up_down;
output  [7:0] qd;
reg     [7:0] cnt;
assign qd = cnt;
always @ (posedge clk)
begin
   if (!clear)
      cnt = 8'h00;
   else if (load)
      cnt = d;
   else if (up_down)
      cnt = cnt + 1;
   else
      cnt = cnt - 1;
end
endmodule
```

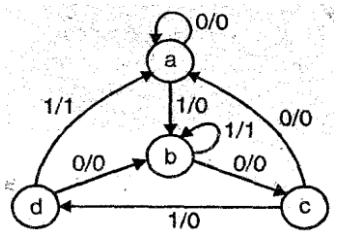
PART-B

1. Explain T-flip-flop with suitable internal structure.

2. Convert SR flip-flop to T flip-flop.

3. For the given state diagram, draw the state reduction diagram.

Stats Diagram:



4. Why is gated D latch called transparent latch?

5. Give the truth-table for each flip-flop type: (a) J-K ; (b) D ; and (c) T

6. Draw logic circuit diagram for 3-bit synchronous up-down counter with clear input, start input and 'done' output. The counter should produce 'done' output after completion of counter in either direction.

7. Draw the logic circuits and the excitation tables for the T, JK flip-flops.

8. Classify the sequential circuits.

9. Describe the difference between a gated S-R latch and an edge-triggered S-R flip flop.

10. What is the difference between level and edge triggering? Explain the working of master slave J-K flip flop.

11. Draw a master-slave J-K flip-flop system. Explain its operation and show that the race-around condition is eliminated.

12. Explain what is universal shift register? Explain its working.

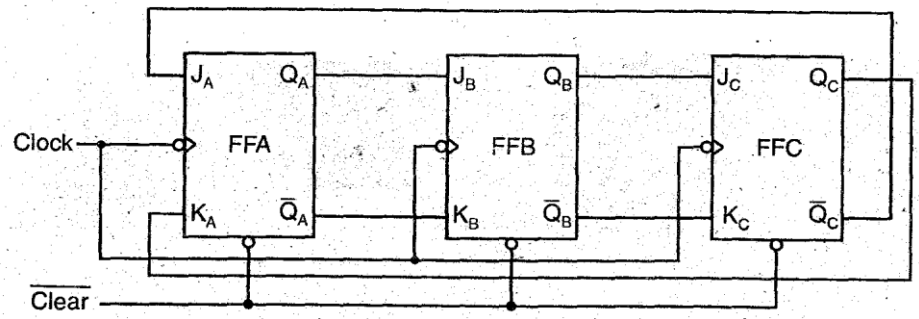
13. Draw the logic symbols for T and RS flip-flops. Explain the function of each type of flip-flop.

14. Draw the circuit of an S-R flip-flop using NAND gates. Modify it to include clock Derive J-K circuit from S-R flip-flop circuit and explain its truth table

15. Design a J-K counter that goes through states 2, 4, 5, 7, 2, 4…… is the counter-self starting.

16. Perform the following conversions T flip-flop to D flip-flop.

17. Twisted ring counter is also known as Johnson counter. It is an application of shift register. Following figure shows the circuit diagram for its operation.



18. Design a synchronous decade counter to count in the following sequence

1, 0, 2, 3, 4, 8, 7, 6, 5

19.Write short note on the following: Counter design with state equation and state diagrams.

20. What is race around condition in J-K flip flop? How it is eliminated?

21. Write note on: 4 bit binary shift register.

22. Design a BCD counter using JK flip-flops.

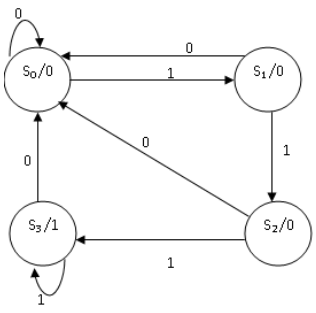
23. Design an up-down counter using JK Flip-flop to count 0, 2, 3, 6, 4, 0….

24. Design an up-down counter using D-flip-flops to count 0, 3, 2, 6, 4, 0,.....

25. i) Draw a 4 bit ripple counter with D flip flop.

ii) Write the HDL for the above circuit.

26. Design sequential circuit by the state diagram using JK flip flop.



27. i) Design 3 bit binary counter.
ii) Write HDL of T flip flop and JK flip flop from D flip flop.

28. Design a sequential circuit using RS flip flop for the state table with minimum flip flop.

Present State	Next State		Output	
	x=0	x=1	x=0	x=1
A	a	b	0	0
B	c	d	0	0
C	a	d	0	0
D	e	f	0	1
E	a	f	0	1
F	g	f	0	1
G	a	f	0	1

28. i) Explain the operation of a JK Master Slave flip flop with logic diagram. (May/June 2012)
ii) Design a counter that goes through the following sequence of states: 0,3,2,4,1,5,7,0,3,2,..

29. Design a 4-bit parallel in serial out shift register. (May/June 2012)

30. Design synchronous mod 16 counter using JK flip flop. (Nov/Dec 2012)

31. i) Write behavioural VHDL Description of 8 bit shift register with direct reset.
ii) What is the difference serial and parallel transfer? Explain how to convert parallel data to serial and serial data to parallel. What type of register is needed? (Nov/Dec 2012)

32. Design a shift register using JK flip flops. (May/June 2013)

33. Using D flip flops, design a synchronous counter which counts in the sequence, 000,001,010,011,100,101,110,111,000,... (May/June 2013)

34. Design a synchronous counter with the following sequence: 0,1,3,7,6,4 and repeats. Use JK flip flops. (Nov/Dec 2013)

UNIT- 4
ASYNCHRONOUS SEQUENTIAL LOGIC
PART - A

1. What is asynchronous sequential circuit?

Asynchronous sequential circuit is a system which depends upon the order in which its input signals change and can be affected at any instant of time. The memory elements used are time delay devices.

2.What is the difference between synchronous and asynchronous sequential circuits? (Nov/Dec 2012)

S.No	Synchronous sequential circuits	Asynchronous sequential circuits
1	The change of internal state occurs in response to a clock pulse.	The change in internal state occurs whenever there is a change in input variable.
2	Memory elements are clocked flip-flops	Memory elements are unclocked flip-flops or Time delay units.
3	The present state is totally specified by FF values and does not change if input changes while clock pulse is inactive	There is no clock pulse. Because of absence of clock, asynchronous circuits are faster than synchronous circuits.
4	Design is easy.	Design is more difficult because of the timing problems involved in the feedback path.

3. Mention the applications of Asynchronous circuits.

- Asynchronous circuits are used when speed of operation is important, especially in those cases where the digital system must respond quickly without having to wait for a clock pulse.
- They are more economical to use in small independent systems that require only a few components
- Asynchronous circuits are useful in applications where the i/p signal may change at any time, independently of an internal clock.
- Asynchronous circuits are helpful in verifying that the total digital system is operating in the proper manner.

4. Explain the fundamental mode of operation.

Asynchronous sequential circuits must be allowed to attain a stable state before the i/p is changed to a new value. Because of delays in the wires & the gate circuits, it is impossible to have two or more i/p

variables change at exactly the same instant of time without an uncertainty as to which one changes first. Therefore, simultaneous changes of two or more variables are usually prohibited. This restriction means that only one i/p variable can change at any one time & the time between two i/p changes must be longer than the time it takes the circuit to reach a stable state. This type of operation is defined as fundamental mode.

5. Distinguish between fundamental mode circuits and pulse-mode circuits. (Nov/Dec 2013)
Fundamental Mode Circuit
- The input variables change only when the circuit is stable
- Only one input variable can change at a given time
- Inputs are levels and not pulses.

Pulse Mode Circuits
- The input variables are pulses instead of levels.
- The width of the pulses is long enough for the circuit to respond to the input.
- The pulse width must not be so long that it is still present after the new state is reached and cause a faulty change of state.
- No two pulses should arrive at the input lines simultaneously.

6. Why is the pulse mode operation of asynchronous sequential circuits not very popular?
Because of the input variable pulse width restrictions, pulse mode circuits are difficult to design. For this reason the pulse mode operation of asynchronous sequential circuits is not very popular.

7. What are Latches.
Un clocked memory elements are called latches.

8. Define Flow table.
During the design of asynchronous sequential circuits, it is more convenient to name the states by letter symbols without making specific reference to their binary values, such a table is called a Flow table.

9.What do you mean by Race condition? (Nov/Dec 2012)
A race condition is said to exist in an asynchronous sequential circuit when two or more binary state variables change value in response to a change in an i/p variable. When unequal delays are encountered, a race condition may cause the state variables to change in an un predictable manner.

10. Explain non- critical race.
The order by which the state variables change may not be known in advance. If the final stable state that the circuit reaches does not depend on the order in which the state variable change, the race is called a non-critical race.

11. Explain critical race.
If it is possible to end up in two or more different stable states, depending on the order in which the State variable change, then it is called a critical race.

12. Define the term Maximal compatible.
The maximal compatible is a group of compatibles that contains all the possible combinations of compatible states. The maximal compatible can be obtained from a merger diagram.

13. Define closed covering.
The condition that must be satisfied for row merging is that the set of chosen compatibles must cover all the states that must be closed. The set will cover all the states if it includes all the states of the original state table. The closure condition is satisfied if there are no implied states or if the implied states are included within the set. A closed set of compatibles that covers all the states is called a closed covering.

14. Explain Shared Row method.
The method of making race free assignment by adding extra rows in the flow table is sometimes referred to as Shared Row method.

15. Define Merger diagram.
The merger diagram is a graph in which each state is represented by a dot placed along the circumference of a circle. Lines are drawn between any two corresponding dots that form a

compatible pair. All possible compatibles can be obtained from the merger diagram by observing the geometrical patterns in which states are connected to each other.

16. Explain Multiple row method.
In the multiple row assignment each state in the original flow table is replaced by two or more combinations of state variables. The state assignment map shows the multiple row assignment that can be used with any four-row flow table.

y_3 \ y_2y_1	00	01	11	10
0	a_1	b_1	c_1	d_1
1	c_2	d_2	a_2	b_2

17. What is a hazard? (May/June 2012)
Hazards are unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays. Hazards occur in combinational circuits, where they may cause a temporary false output value. When this condition occurs in asynchronous sequential circuits, it may result in a transition to a wrong stable state. Steps must be taken to eliminate this effect.

18. Differentiae Static & Dynamic Hazard.
- Static 1-hazard: The output may momentarily go to 0 when it should remain 1.
- Static 0-hazard: The output may momentarily go to 1 when it should remain 0.
- Dynamic hazard causes the output to change three or more times when it should change from 1 to 0 or from 0 to 1.

19. Explain Hazards in sequential circuits.
In normal combinational circuit design associated with synchronous sequential circuits, hazards are not of concern. Since momentary erroneous signals are not of generally troublesome. If a momentary incorrect signal is fed back in asynchronous sequential circuits, it may cause the circuit to go to the wrong stable state. The malfunction can be eliminated by adding an extra gate. To avoid static hazards, the asynchronous sequential circuits can be implemented with S R latches.

20. Define Essential Hazard.
- An essential Hazard is caused by unequal delays along two or more paths that originate from the same input.
- An excessive delay through an inverter circuit in comparison to the delay associated with the feed back path may cause such a hazard.
- Essential hazards cannot be corrected by adding redundant gates as in static hazards.
- To avoid essential hazard, each feed back loop must be handled with individual care to ensure that the delay in the feedback path is long enough compared to delays of other signals that originate from the input terminals.

21. Explain the use of SR latches in asynchronous sequential circuits.
- The use of SR latches in asynchronous circuits produce a more orderly pattern, which may result in a reduction of the circuit complexity.
- An added advantage is that the circuit resembles the synchronous circuit in having distinct memory elements that store & specify the internal states.
- One of the ways to avoid static hazards in asynchronous sequential circuits is to implement the circuit with SR latches.

22. What is Primitive Flow table? (May/June 2013), (Nov/Dec 2013)
A primitive flow table is a flow table with only one stable total state in each row.

23. What do you understand by the term merging?
The primitive flow table has only one stable state in each row. The table can be reduced to a smaller rows number of if two or more stable states are placed in the same row of the flow table. The grouping of stable states from separate rows in to one common row is called merging.

24. What is finite state Machine?
A finite state machine (or finite automation) is an abstract model describing the synchronous sequential machine and its spatial counter, part, the iterative network.

25. Define critical race in asynchronous sequential circuits.
Critical race in asynchronous circuits occur between two signals that are required to change at the same time when the next stable state is dependent on the delay paths in the circuit

26. What is meant by debouncing switch?
Data is often entered into a digital system by means of switches. A common characteristic of all these switches are they have a tendency to bounce when actuated, causing a short series of repetitive make and break connections lasting for several milli seconds. A latch circuit can be used as a debounce and the technique adopted is called debouncing.

27. What is State Assignment?
- Assigning binary values to each state that is represented by letter symbol in the flow table of sequential circuit is called state assignment.
- The primary objective in choosing a proper binary state assignment in asynchronous circuit is the prevention of critical races

28. List any two drawbacks of asynchronous circuits.
Race condition Hazards

29. What is the need of state reduction in sequential circuit design?
a. To reduce the number of flip-flops
b. To reduce the number of gates in the combinational circuit that drives the flip-flop inputs.

30.What is the use of flip-flop excitation table?
If the transition from present state to next state is known in the design of sequential circuit, the flip-flop excitation table is used to find the flip-flop input conditions that will cause the required transition.

31. What is dynamic hazard?
Dynamic hazard is unwanted switching transition that causes the output to change three or more times when it should change from 1 to 0 or from 0 to 1.

32. What is state machine?
A state machine is another term for a sequential circuit, which is the basic structure of a digital system.

33. What is the reason for essential hazard to occur?
Unequal delays along two or more paths that originate from the same input in the asynchronous sequential circuit is the reason for essential hazard to occur.

34. Define compatible states.
Two states are compatible (equivalent) if in every column of the corresponding rows in the flow table, there are identical or equivalent next states and if there is no conflict in the output values.

35. When is a sequential machine said to be strongly connected?
A sequential machine is said to be strongly connected when it goes through all possible synchronization states. Example: Natural counter.

36. What is One-Hot assignment?
One hot state assignment is made so that only one variable is active or “hot” for each row in the original flow table. This technique requires as many state variables, as there are rows in a flow table. Additional rows are introduced to provide single variable changes between internal state transitions.

37. What is the difference between an internal state and a total state?
Internal state: The combination of secondary variables gives the internal state of the asynchronous circuit.
Total state: The combination of secondary variables (present state) and the external input variables gives the total state by which the operation of the asynchronous circuit is described.

38. Explain the difference between the stable state and the unstable state.

Stable state: If the next state is equal to the present state for the given input combination, the state is called stable state.

Unstable state: If the next state is not equal to the present state for the given input combination, the state is called unstable state.

39. Define cycle.

- A cycle occurs when an asynchronous machine makes a transition through a series of unstable states.
- Care must be taken to make sure whether the cycle terminated with a stable state or not.
- If a cycle does not terminate with a stable state, the circuit will keep going from one unstable state to another, making the entire circuit unstable.

40.What is ASM chart?

- Algorithmic State Machine (ASM) chart is a special type of flow chart suitable for describing the sequential operations in a digital system.
- A state machine is another term for a sequential circuit, which is the basic structure of a digital system.
- The ASM chart is composed of three basic elements: the state box, the decision box and the conditional box.

41. What are static '1' and static '0' hazards? (May/June 2013)

- Static 1-hazard: The output may momentarily go to 0 when it should remain 1.
- Static 0-hazard: The output may momentarily go to 1 when it should remain 0.

42. Give the block diagram of asynchronous sequential circuit.

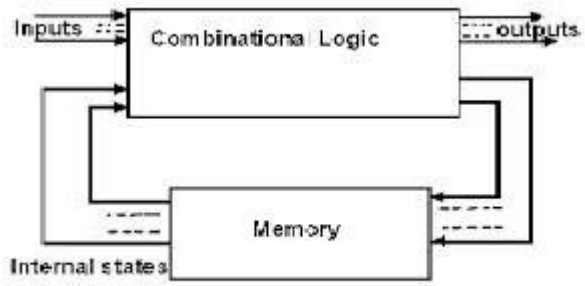


Figure 1: Asynchroncus Sequential Circuit

43. What are cycles and races? (May/June 2012)

A cycle occurs when an asynchronous circuit makes a transition through a series of unstable states. If a cycle does not contain a stable state, the circuit will go from one unstable to stable to another, until the inputs are changed.

When 2 or more binary state variables change their value in response to a change in an input variable, race condition occurs in an asynchronous sequential circuit. In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.

44. What are the different types of shift type? (Nov/Dec 2012)

There are five types. They are,

- Serial In Serial Out Shift Register
- Serial In Parallel Out Shift Register
- Parallel In Serial Out Shift Register
- Parallel In Parallel Out Shift Register
- Bidirectional Shift Register

PART-B

1.Give the design procedure for Mealy and Moore machine.

2. Explain about hazards in digital systems.

3. Give the design Procedure for asynchronous sequential circuit.

(May/June 2013) (Nov/Dec 2012)

4. Design a gated latch circuit with two inputs, *G* (gate) and *D* (data), and one output *Q*. The gated latch is a memory element that accepts the value of *D* when *G* = 1 and retains this value after *G* goes to 0. Once *G* = 0, a change in *D* does not change the value of the output *Q*.

5. Design procedure for Hazard free network.

6. Explain in detail about Hazards. (Nov/Dec 2012) (May/June 2013)

7. Design asynchronous circuit that has 2 input X_2 and X_1 and output Z. When X_1 =0, Z=0. The first change is X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0.

8. Find a circuit that has no static hazards and implements the Boolean function $F(A,B,C,D)=\Sigma_m(1,3,5,7,8,9,14,17)$.

9. Explain race free state assignment.

10. Write notes on hazards on combinational and sequential circuits.

11. i) Design a asynchronous serial parity generator with proper state assignment procedure. (May/June 2012)

ii) Write a note on pulsed mode and fundamental asynchronous sequential circuit.

12. Implement the switching function $F=\Sigma_m(1,3,5,7,8,9,14,15)$ by a static hazard free 2 level AND-OR gate network. (May/June 2013)

13. Design an asynchronous sequential circuit with inputs x1 and x2 and one output z. Initially and at any time if both the inputs are 0, output is equal to 0. When x1 or x2 becomes 1, z becomes 1. When second input also becomes 1, z=0; the output stays at 0 until circuit goes back to initial state. (Nov/Dec 2013)

14. i) What is the objective of state assignment in asynchronous circuit? Explain race-free state assignment with an example. (Nov/Dec 2013)

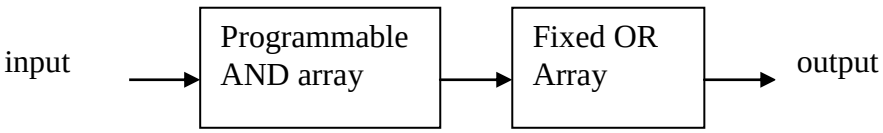
ii) Discuss about static, dynamic and essential hazards in asynchronous sequential circuits.

UNIT -5
MEMORY AND PROGRAMMABLE LOGIC
PART - A

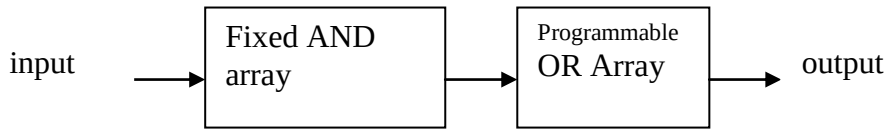
1. What is the difference between PROM and PLA? (Nov/Dec 2012)

- The programmable array logic (PAL) is a programmable logic device with a fixed OR array and a programmable AND array.
- The Programmable Read Only Memory (PROM) is a programmable logic device with a fixed AND array and a programmable OR array.

Architecture: PAL



- Architecture: PROM



2. What is a PLA? Describe its uses.

a. PLA (Programmable Logic Array) is a programmable logic device with a Programmable AND array and a programmable OR array.

b. PLA can be used to implement complex logic circuits.

c. It is more economical to use PLA rather than PROM to implement logic circuits that have more number of don't care conditions in order to reduce number of gates.

d. PLA is flexible compared to PROM & PAL.

3. Define Bit time & Word time.

The time interval between clock pulses is called the bit time, and the time required to shift the entire contents of a shift register is called the word time.

4. What is non- volatile memory?

Memory units that retain its stored information after removal of power. Eg magnetic disk. This is because the data stored on magnetic components is manifested by the direction of magnetization, which is retained after power is turned off.

5. Distinguish between EPROM and EEPROM

S.No	EPROM	EEPROM
1	Erasable Programmable Read Only Memory	Electrically Erasable Programmable Read Only Memory
2	Placing the EPROM chip under a special ultraviolet erases the stored information.	Applying electrical signal erases the stored information.
3	It can also be called as UV EPROM	It can also be called as Electrically Alterable ROM (EAROM).

6. What does burning a ROM mean?

The process of entering data into the ROM by burning internal fuses is called programming or burning a ROM.

7. What are the major drawbacks of the EEPROM?

a. COST: In EEPROM, the erasing and programming of an EEPROM can be done *in circuit.* (Without using separate UV light source and special PROM programmer unit). Because of this on-chip support circuitry the EEPROM is available with more cost.

b. DENSITY: The high level integration of the EEPROM occupies more space. For example, 1-Mbit EEPROM requires about twice as much silicon as a 1-Mbit EPROM.

8. How many data inputs, data outputs and address inputs are needed for a 1024 ×4 ROM?

No. of data inputs and outputs = 4

$1024 = 2^{10}$

No of address inputs = 10

9. Describe the basic functions of ROM and RAM

ROM: Read only memory is used to store information permanently. The information can not be altered.

RAM: Random Access Memory is used to store information. The information can be read form it and the new information can be written into the memory.

10. How long will it take to erase UV erasable EPROM completely?

15 to 20 min.

11. Distinguish between PAL and PLA. (May/June 2012)

a. Programmable Array Logic (PAL) is a programmable logic device with a fixed OR array and a programmable AND array. Because only the AND gates are programmable, the PAL is easier to program, is not flexible as the PLA. It uses array logic symbol.

b. Programmable Logic Array (PLA) is a programmable logic device with a Programmable AND array and a programmable OR array. PLA can be used to implement complex logic circuits. It uses conventional symbol. It is more flexible than PAL.

12. What is Configurable Logic Block?

The programmable logic blocks in the Xilinx family of FPGAs are called configurable logic blocks (CLBs). The CLB of Xilinx 3000 series can be configured to perform any logic function of up to a maximum of seven variables. .

13. Give the different types of RAM.

RAM can be classified into two types:

1. Static RAM: The storage elements used in this type RAM are latches (unclocked FFs).

2. Dynamic RAM: A dynamic RAM is one in which data are stored on capacitors which require periodic recharging (refreshing) to retain the data.

RAMs are manufactured with either bipolar or MOS technologies. Bipolar RAMs are all static RAM. MOS RAM are available in both static and dynamic types

14. What is dynamic RAM cell? Draw its basic structure.

A dynamic RAM is one in which data are stored on capacitors which require periodic recharging (refreshing) to retain the data.

15. What is Memory refresh?

Dynamic RAMs are fabricated using MOS technology. They store 1s and 0s as charges on a small MOS capacitor (typically a few picofarads). Because if the tendency for these charges to leak of after a period of time, dynamics require periodic recharging of the memory cells This is called refreshing the dynamic RAM or memory refresh.

16. What is the difference between PAL and PLA?

Ans.

PLA	PAL
In case of PLA i.e. programable logic array both AND and OR arrays are programmable.	1. In case of PAL i.e. programmable array logic OR arrays are fixed and and AND arrays are programmable.
It is costlier as compared to PAL.	2. It is cheaper.
It is complex than PAL.	3. It is simple.
It can't easily be programmed.	4. It is easy to program a PAL.

17. What do you mean by PLD's?

Ans. PLDs: Programmable logic devices are the special type of IC's used by the USE and are programmed before use Different type of logic functions can be implemented using a single programmed IC chip of PLD's. PLD s can be reprogrammed because these are based on re-.writable memory technologies Fuse links are used to programmed the PLD b the user according to the type of PLD to be manufactured

18. Where do we use PLA's?

1. Combinational circuits can be implemented using PLA's
2. Sequential circuits can be implemented using PLA's.
3. In sequential circuits implementation flip-flops and buffers are used at output stage with PLA devices while in combinational circuits only buffers are used.
4. Compact circuits can be built using PLA's, which covers less space.

19. Compare SRAM and DRAM. (May/June 2013)

SRAM: Static RAM uses the flip-flop for its basic storage element. It is possible to store data as long as power is applied to the chip. It make use of cross coupled TTL multiemitter bipolar transistors or cross coupled MOSFETs for its construction.

DRAM : Dynamic RAM make use of capacitive element for storing the data bit. Binary information is stored as charge. If charge is present at a capacitive element it represents a logic 1 and in the absence of the charge a logic 0 is stored. DRAM's consumes less power as compared to SRAM's.

33. Distinguish EEPROM and flash memory. (Nov/Dec 2013)

EEPROM is an older, more reliable technology. It is somewhat slower than Flash. Flash and EEPROM are very similar, but there is a subtle difference. Flash and EEPROM both use quantum cells to trap electons. Each cell represents one bit of data. The presence - or absence - of electons in a cell indicates whether the bit is a 1 or 0. The cells have a finite life - every time a cell is erased, it wears out a little bit. In EEPROM, cells are erased one-by-one. The only cells erased are those which are 1 but need to be zero. (Writing a 1 to a cell that's 0 causes very little wear, IIRC) . In Flash, a large block is erased all at once. In some devices, this "block" is the entire device. So in Flash, cells are erased whether they need it or not. This cuts down on the lifespan of the device, but is much, much faster than the EEPROM method of going cell-by-cell. Erasure method: Both Flash and EEPROM erase cells by means of an electric field. I think it is high-frequency and "pops" the electrons out of the cells, but I am not certain.

PART-B

1. Implement the boolean function using PAL.

$Y_1 = \Sigma m (1, 3, 5, 7)$

$Y_2 = \Sigma m (2, 4)$.

2. Design half adder circuit using PLA.

3. What is PAL?

4. Describe with diagram internal architecture of PLA

5. The difference between static and dynamic memories.

6. Give the classification of memories.

7. A certain memory stores 8 k x 16 bit words. How many data input lines, data output lines and address lines does it have ? What is its capacity in bytes?

8. What are the various types of ROMs? Discuss their relative advantages and disadvantages.

9. State and explain the difference among ROM, PROM, RAM, SRAM and DRAM.

10. Write short note on Classification and characteristics of memories.

11. Explain the architecture and function of programmable logic arrays

12. Implement using PLA $A(x,y,z)= \Sigma_m(1,2,4,6)$ $B(x,y,z)= \Sigma_m(0,1,6,7)$ $C(x,y,z)= \Sigma_m(2,6)$.

13. Implement a full adder with two 4X1 Mux.

14. i) Write short notes on PLA/PAL.

ii) Write notes on RAM its operation and types.

15. i) Explain the operation of a Static RAM. (May/June 2012)

ii) Implement the following function using PAL:

$f(A,B,C,D)= \Sigma_m(0,2,4,6,8,10,12,14)$

16. With suitable example explain how combinational circuits are implemented using Programmable logic arrays. (Nov/Dec 2012)

17. Implement the switching functions. (May/June 2013)

Z1=ab'd'e+a'b'c'd'e'+bc+de

Z2=a'c'e

Z3=bc+de+c'd'e'+bd

Z4=a'c'e+ce using 5 x 8 x 4 PLA

17. i) Implement the following Boolean functions using 8 x 2 PROM. (Nov/Dec 2013)

$F1= \Sigma_m(3,5,6,7)$ and $F2= \Sigma_m(1,2,3,4)$

ii) Implement the following function Boolean functions using PLA with 3 inputs, 4 product terms and 2 outputs.

$F1= \Sigma_m(3,5,6,7)$ and $F2= \Sigma_m(1,2,3,4)$