UNIT –II DIGITAL COMMUNICATION

AMPLITUDE SHIFT KEYING (ON –OFF KEYING)

IT is a simple digital amplitude modulation (DAM) where the input message signal is a digital signal .the carrier signal is the very old analog high frequency itself. For a logic 1= +1 V and logic 0 = -1V is generated and it is $v_m(t)$.

When the input signal $v_m(t) = +1$

$$v_{(ask)}(t) = [1 + v_m(t)]\left[\frac{A}{2}\cos(\omega_c t)\right]$$

where $v_{ask}(t)$ = amplitude-shift keying wave
$v_m(t)$ = digital information (modulating) signal (volts)
$A/2$ = unmodulated carrier amplitude (volts)
ω_c = analog carrier radian frequency (radians per second, $2\pi f_c t$)

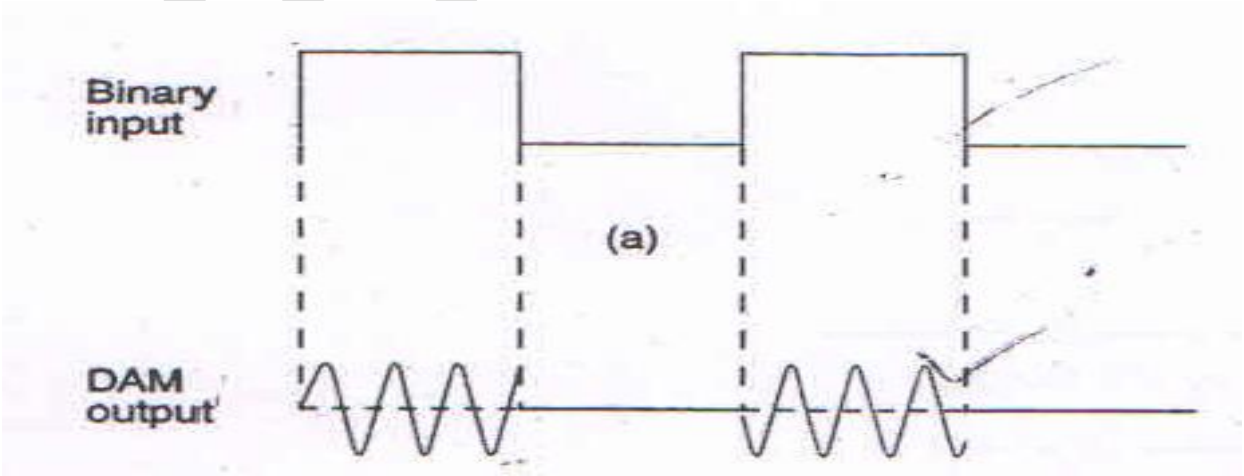
$$v_{(ask)}(t) = [1 + 1]\left[\frac{A}{2}\cos(\omega_c t)\right]$$

$$= A\cos(\omega_c t)$$

for a logic 0 input, $v_m(t) = -1$ V, Equation 9-12 reduces to

$$v_{(ask)}(t) = [1 - 1]\left[\frac{A}{2}\cos(\omega_c t)\right]$$

$$= 0$$



FREQUENCY SHIFT KEYING

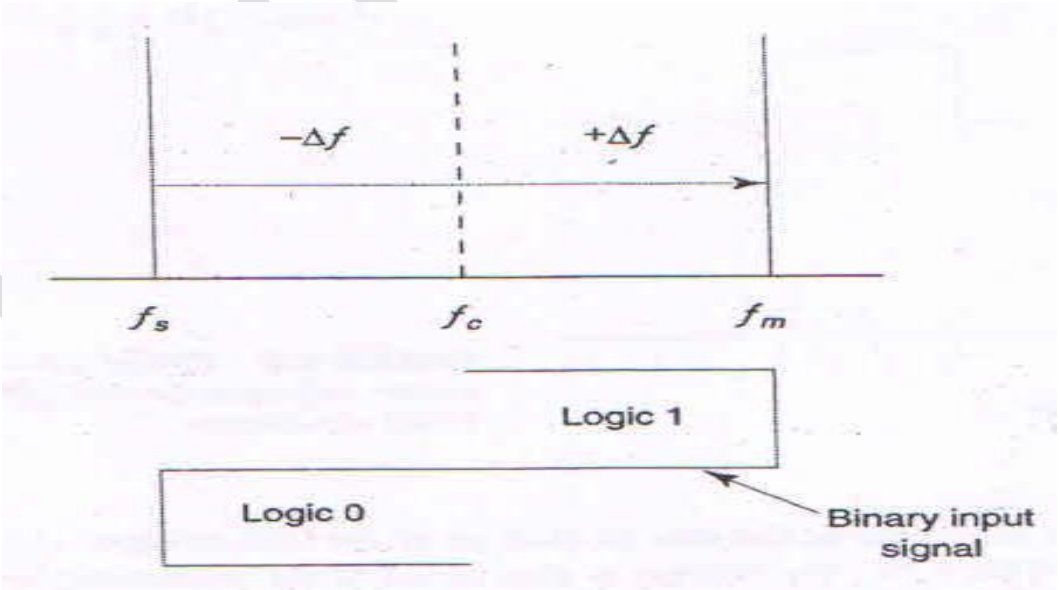
Binary FSK is a form of constant amplitude angle modulation except that the modulation signal is a binary signal that varies between two discrete voltage levels and the frequency of a sinusoidal carrier is shifted between two discrete value frequencies.

The general expression for BFSK is

$$v_{fsk}(t) = V_c \cos\{2\pi[f_c + v_m(t)\,\Delta f]t\}$$

$v_{fsk}(t)$ = binary FSK waveform
V_c = peak analog carrier amplitude (volts)
f_c = analog carrier center frequency (hertz)
Δf = peak change (shift) in the analog carrier frequency (hertz)
$v_m(t)$ = binary input (modulating) signal (volts)

From the above eqa it is understood that the peak shift in the carrier frequency Δf is proportional to the amplitude of the binary signal Vm(t) and the direction is determined by the polarity.



$$v_{fsk}(t) = V_c \cos[2\pi(f_c + \Delta f)t]$$

For a logic 0 input, $v_m(t) = -1$, Equation 9-13 becomes

$$v_{fsk}(t) = V_c \cos[2\pi(f_c - \Delta f)t]$$

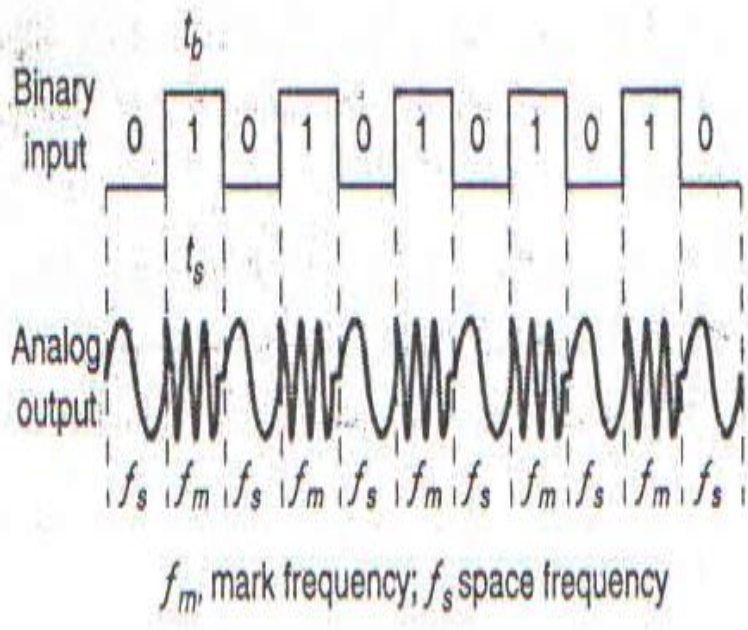
The center frequency fc is shifted u and down in the frequency domain by the binary input signal.when the binary input signal changes from logic 0 to a logic 1 and vice versa the output frequency shifts between two frequency .

(i) mark or logic 1.fm

(ii) space frequency or logic 0 .fs

as the input changes from logic 1 to logic 0 .the FSK output frequency changes from mark frequency fm to space frequency fs.

Mark frequency =(fc+Δf) space frequency is the lowest frequency =(fc-Δf).



binary input	frequency output
0	space (f_s)
1	mark (f_m)

FSK TRANSMITTER

The carrier center frequency is chosen such that it falls between the mark and space frequencies.a logic 1 input shift the voltage controlled oscillator output to the mark frequency .logic 0 input shifts the VCO output to the space frequency .when the binary input signal changes back and fourth between logic 1 and logic 0 the VCO output shifts or deviates back and fourth between mark and space frequencies .a VCO FSK modulator canbe operated in sweep mode where the peak frequency deviation is simply the product of the binary input voltage and deviation sensitivity of VCO.

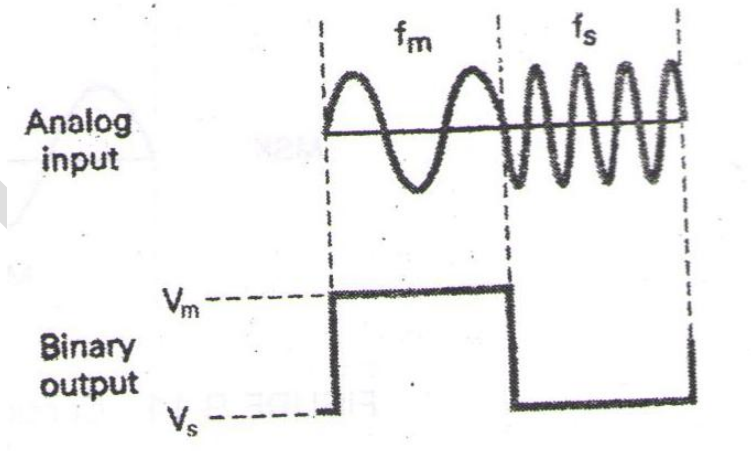
FREQUENCY SHIFT KEYING RECEIVER

The FSK input signal is simultaneously applied to the input of both band pass filter through a power splitter .the Respective filter passes only the mark frequency or only the space frequency on to its respective envelop detector. The envelope detector in turn indicate the total power in each pass band and the comparator responds to the largest of the two powers .in a non coherent detection there is no frequency involved in the demodulation process

COHERENT FSK DETECTION:

In a coherent FSK receiver where the frequency come in action. The incoming FSK signal is multiplied by a recovered carrier signal that has the exacts carrier frequency and phase as the transmitter reference .it is down converted by multiply with local carrier and the corresponding space and mark frequency is produced .where the low pass filter gives an corresponding output to fs and fm .which in compared in a data comparator like which frequency is high and corresponding output is produced .generally it is not used because of its practical difficulty in reproducing a local reference that is in coherent with receiver .so it is seldom used.

FREQUENCY SHIFT KEYING(FSK)

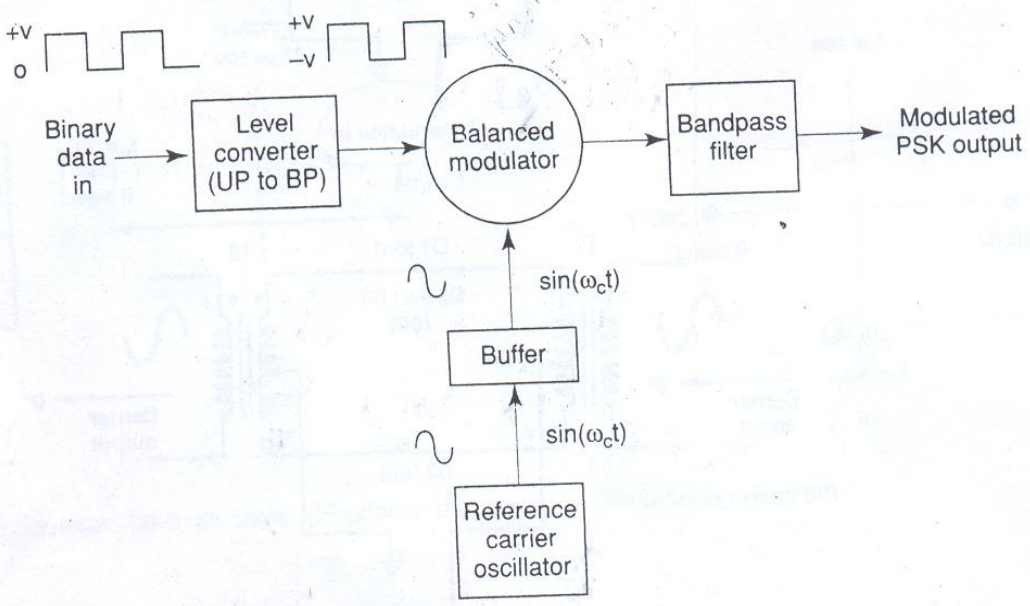


BINARY PHASE SHIFT KEYING

With BPSK input signal is binary and a limiter number of output phses is possible.with BPSK two output phases are possible for a single frequency.

- Logic 1 represents a 0 degree phase shift.
- Logic 0 represents a 180 degree phase shift.

As the input digital signal changes state the phase of the output carrier shifts between two angles that are 180 degree out of phase.



The balanced modulator acts as a phase reversing switch .depending on the logic condition of the input the carrier is transferred to the output either in phase or 180 degree out of phase with thr reference carrier oscillator.

The balanced ring modulator has two input : a carrier that is in phase with the reference oscillator and the binary digital data as other.for a balanced modulator to operate properly the binary input signal voltage must be much greater than the peak carrier voltage .this ensure that the digital input controls the ON/OFF states of

the diode.if the binary input is a logic 1 (+ve volt)diodes D1 and D2 are forward bised and ON while diodes D3 and D4 are reverse biased and put OFF.

The carrier voltage is developed across transformer T2 in phase with the carrier voltage across T1 consequently the output signal is in phase with the reference oscillator.

If the binary input is logic 0 diodes D1 and D2 are reverse biased ,diodes D3 and D4 are forward biased . As a result the carrier voltage is developed accross transformer T2 with 180 ' out of phase shift with the carrier voltage across T1.

BPSK RECEIVER

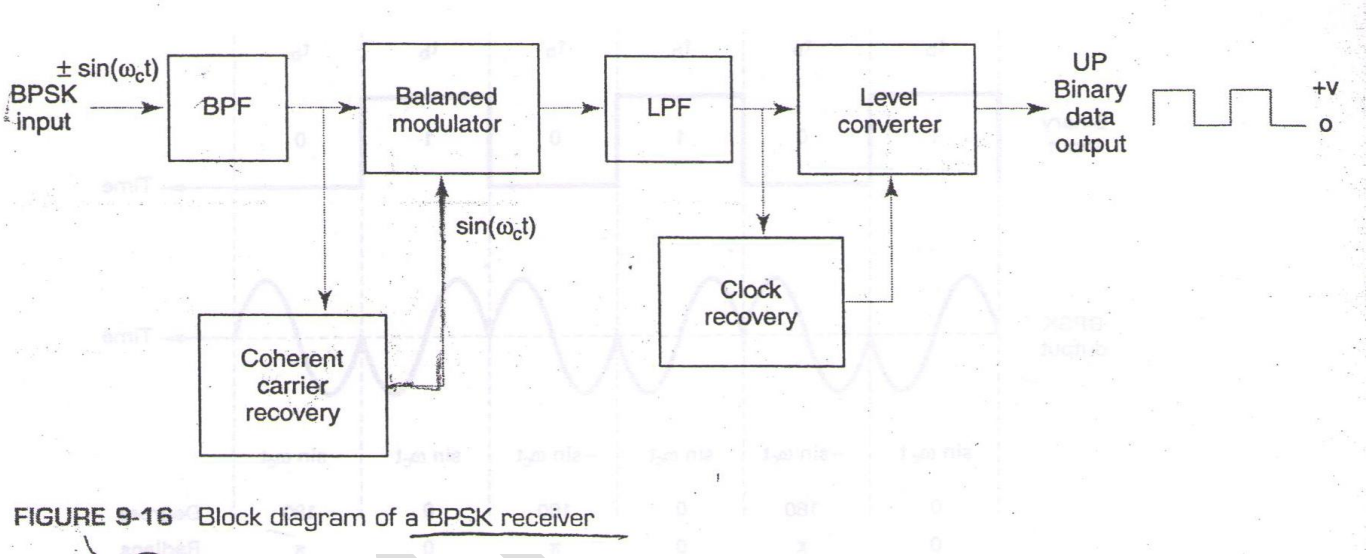


FIGURE 9-16 Block diagram of a BPSK receiver

when a sine wave with a 0' phase shift is received at the input of the receiver it is made product with the local carrier which generates a positive constant (+1/2v) and a cosine which is twice the carrier frequency . This is filtered out in a low pass filter . The resulting positive voltage is demodulated as a logic 1.

when a sine wave with a 180' phase shift is received at the input of the receiver it is made product with the local carrier which generates a negative constant (-1/2v) and a cosine which is twice the carrier frequency . This is filtered out in a low pass filter . The resulting negative voltage is demodulated as a logic 0.

BANDWIDTH CONSIDERATION OF BPSK.

IF LOGIC 1 +1 , 0' phase shift

if logic 0 -1 ,180 ' phase shift.

BPSK the output rate of change is equal (baud) is equal to the input rate of change .the fundamental frequency (Fa) af an alternating 1/0 bit sequence is equal to one half of the bit rate (fb/2).

Bandwidth = fb

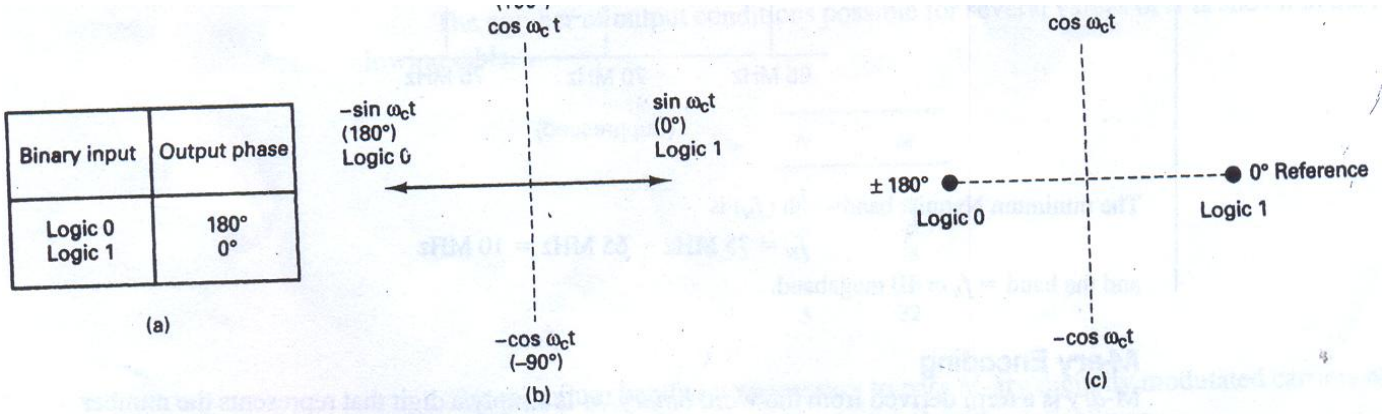


FIGURE 12-16 BPSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

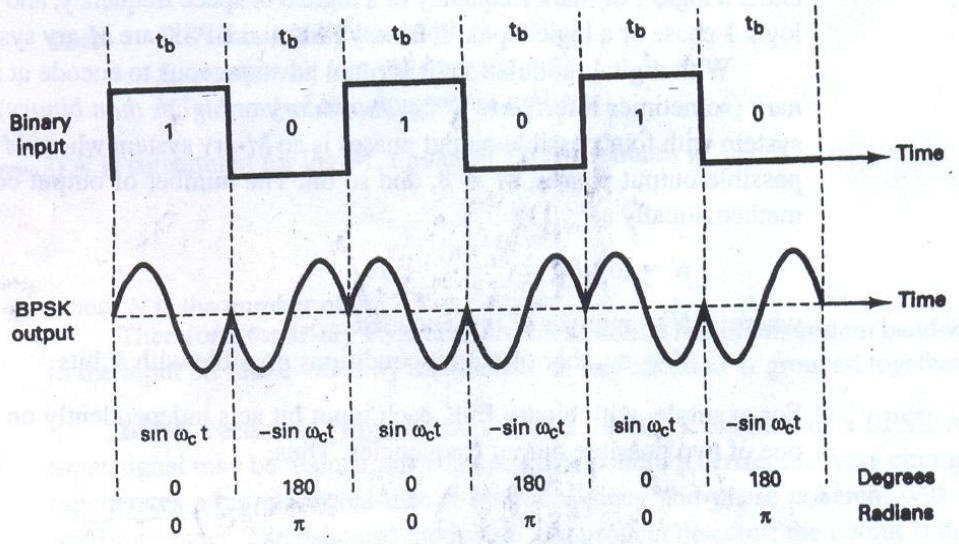


FIGURE 12-17 Output phase-versus-time relationship for a BPSK modulator

QUATERNARY PHASE SHIFT KEYING (QPSK).

Quadrature PSK it is another form of angle modulation.

QPSK is an m-ary encoding technique where M= 4 ,N = 2.

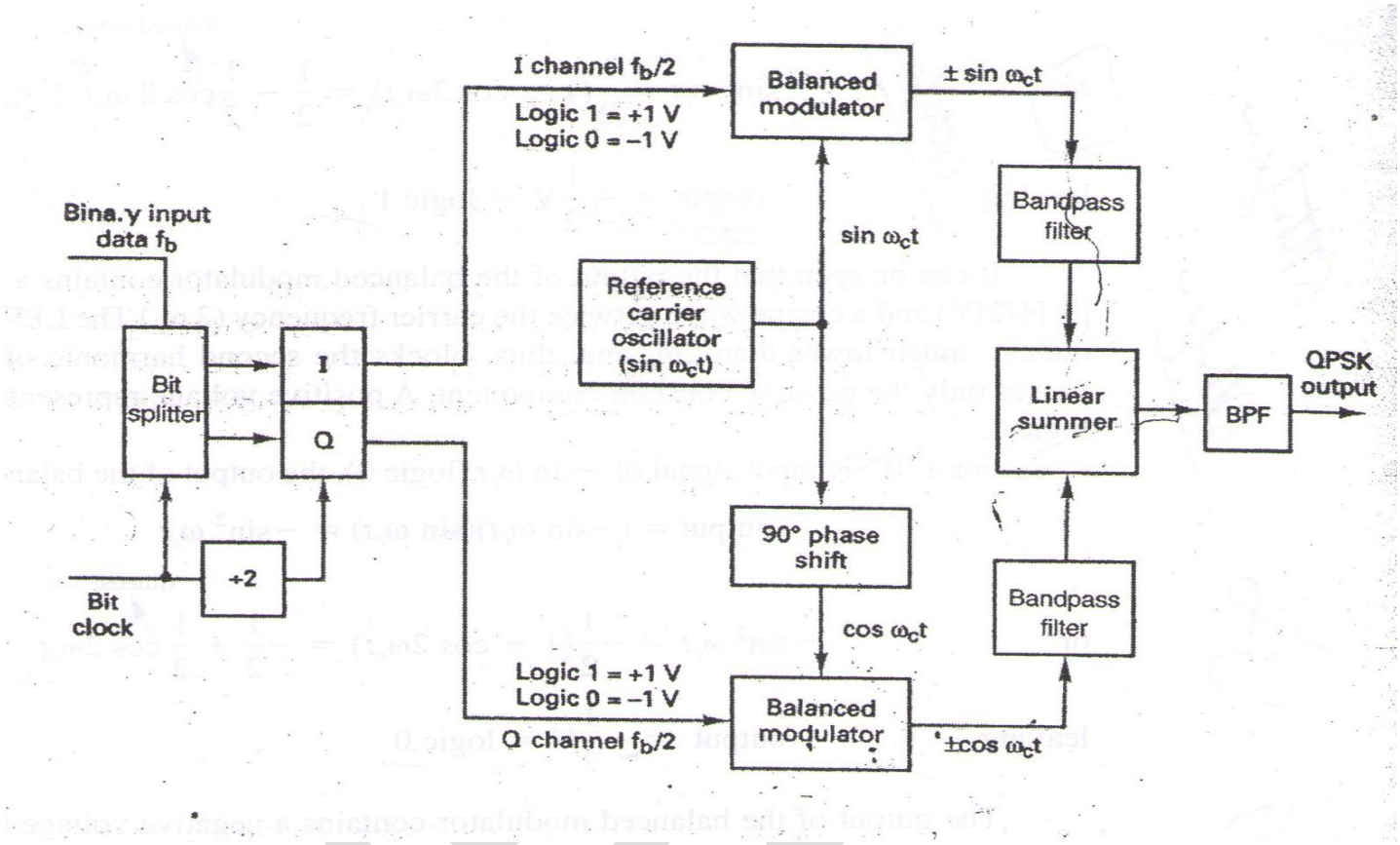
with QPSK four output phases are possible for a single carrier frequency . Because there are four different output phase ,there must be four different input condition.but the digital input to a QPSK modulator is a binary (base 2) signal ,to produce four different input condition .it takes more than a single input bit.

With two bits ,four possible condition are possible :00,01,10,11.

therefore with QPSK the binary input data are combined into group of two bits called DIBITS.

Therefore for a each two bit clocked into the modulator a single output change occurs.

QPSK TRANSMITTER



a dibit is clocked into the bit splitter after both bits have been serially inputted, they are simultaneously paralled outputted .one bit is directed to the I channel and the other to the Q channel.

One bit is directed to the I channel and the bit to the Q channel. the I bit modulates a carrier that is in phase with the reference oscillator .the Q bit modulates a carrier that is 90' out of phase or in quadrature with the reference carrier (Q is quadrature channel) .one the dibit has been split into I and Q channel,the operation is same as BPSK. Again for a logic 1= +1 v and a logic 0 = -1 V . the two phase are possible at the output of the I balance modulator. For a logic 1 and logic 0 two possible output phase are possible from the Q balance modulator .

Where a 90' phase shift circuit gives the Q channel a phase shifted input .with the linear summer the two quadrature signals are combined. which gives four possible expressions.

+Sin ωct – cos ωct

-Sin ωct + cos ωct

-Sin ωct – cos ωct

+Sin ωct + cos ωct

DIAGRAM

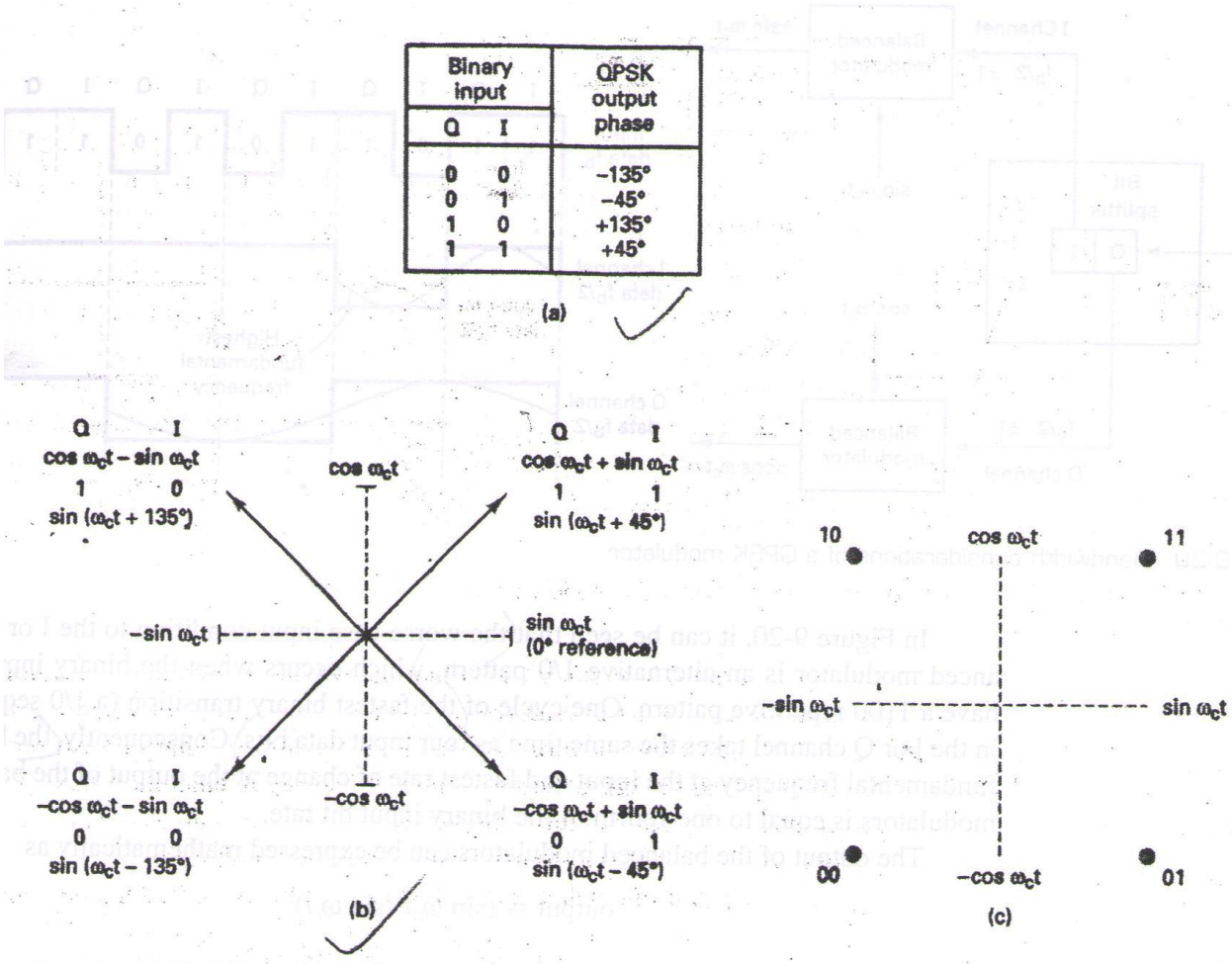


FIGURE 9-18 QPSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

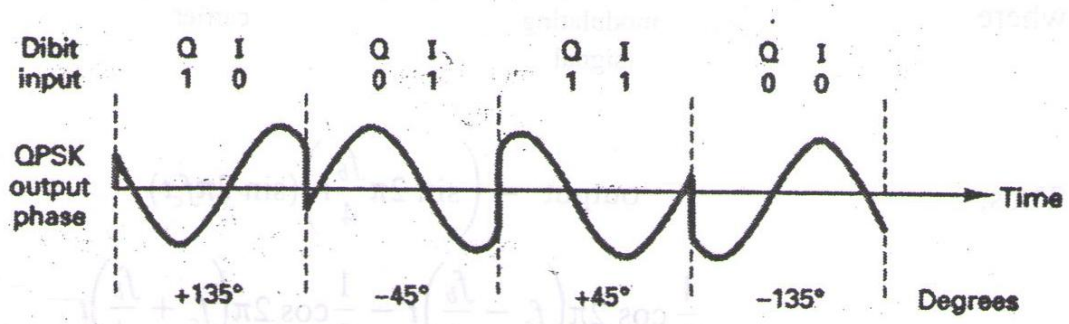
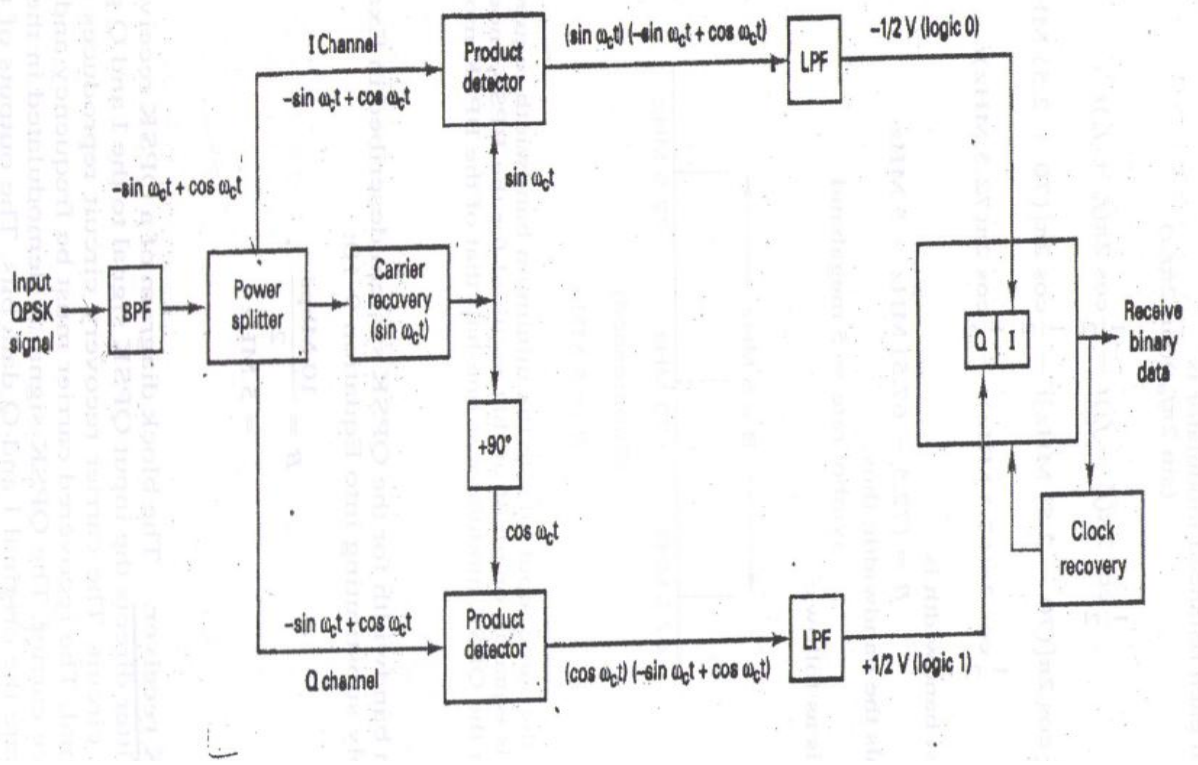


FIGURE 9-19 Output phase-versus-time relationship for a QPSK modulator

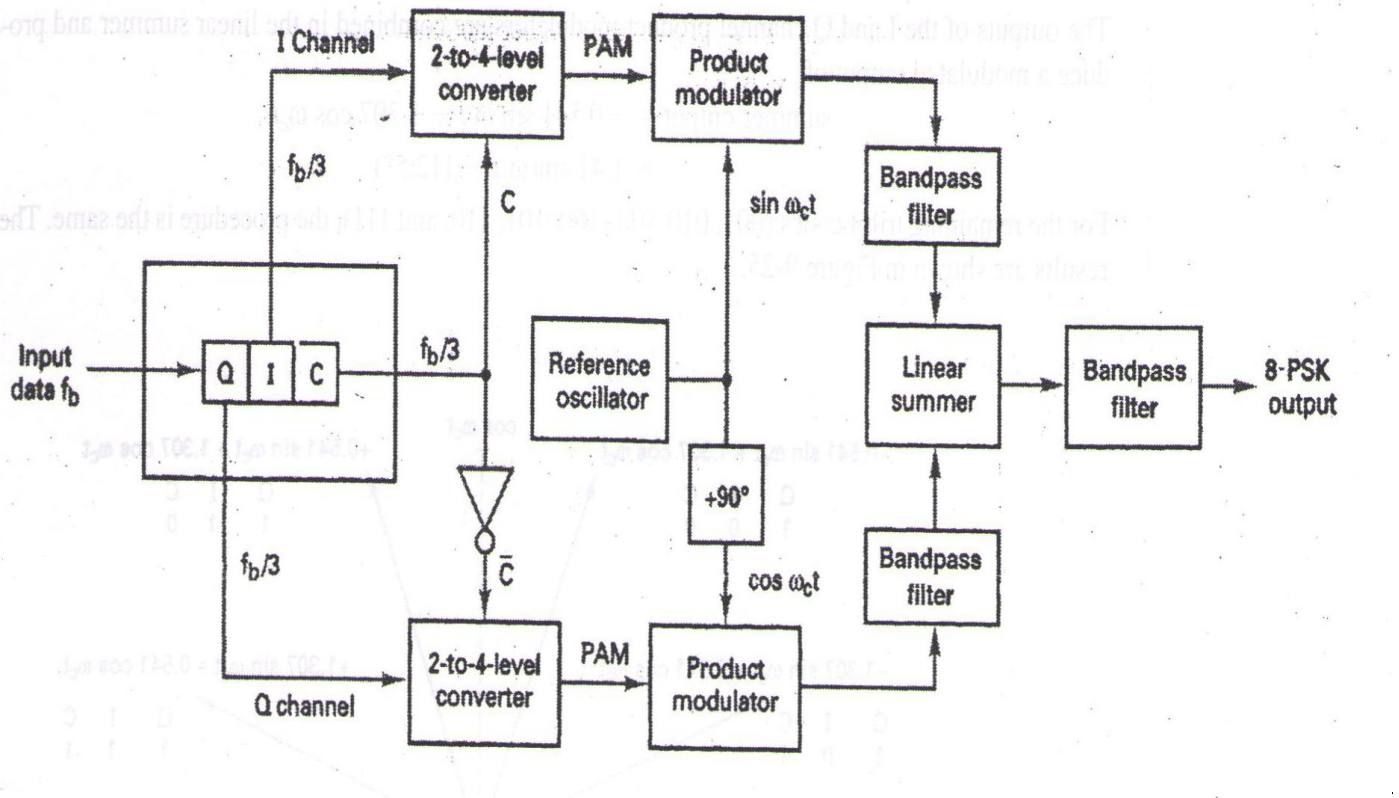
QPSK RECEIVER



The power splitter directs the input QPSK signal to the I and Q channel then to the product detector.the carrier recovery circuit reproduces the original transmitter carrier oscillator signal.the I and Q channel ,which generates the original I and Q data bits.the output of the product detector is a constant ,sine and cosine component . in the I channel a (-1/2V) with Sin 2ωct and cos 2ωct .pass through LPF where the cut off frequency is Fc and eliminates the high frequency component only the constant pass through LPF where in

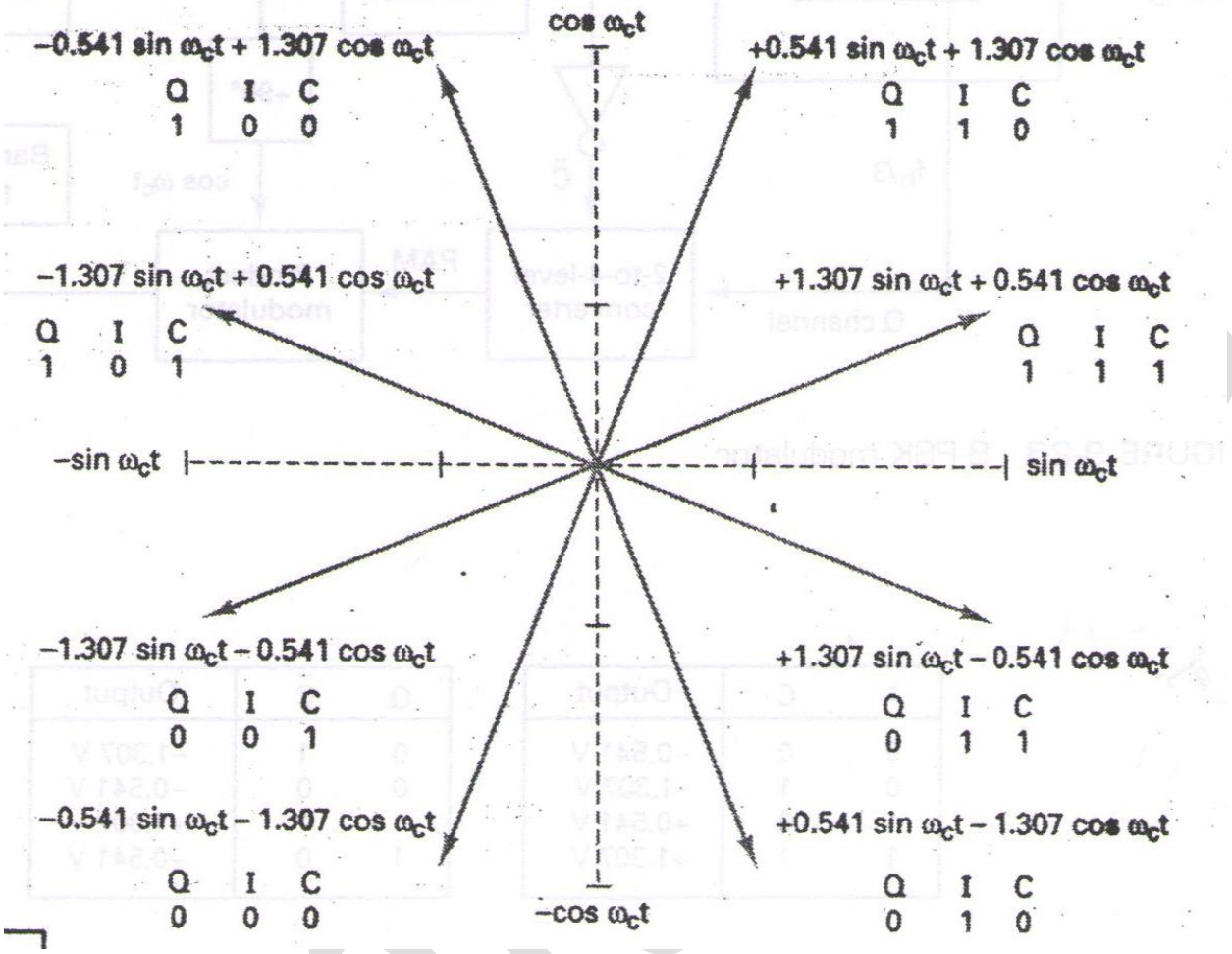
demodulation a constant (-1/2V) os coded as logic 0. in the Q channel a (+1/2V) with Sin 2ωct and cos 2ωct .pass through LPF where the cut off frequency is Fc and eliminates the high frequency component only the constant pass through LPF where in demodulation a constant (+1/2V) as coded as logic 1

8 – QPSK TRANSMITTER MODULATOR

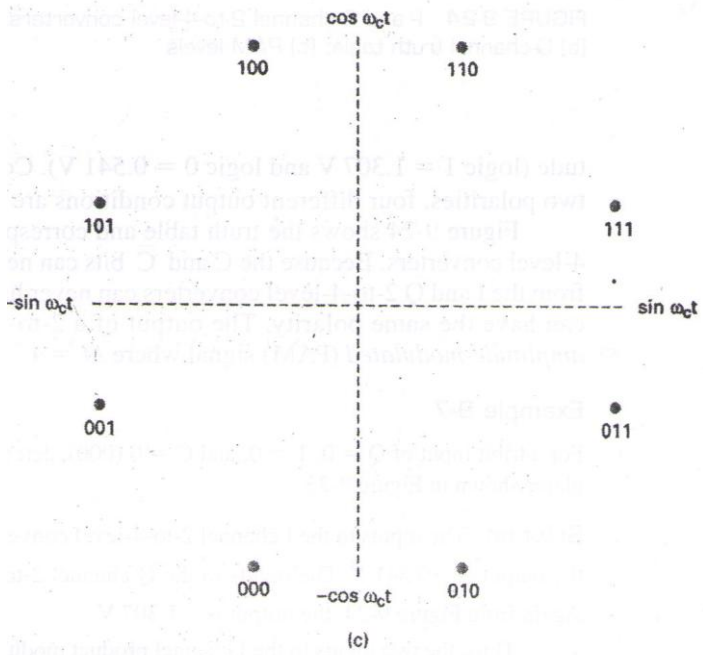


Here n=3 and M=8 The incoming serial bit stream enters the bit splitter ,where converted in to parallel as I cannel ,Qchannel and C or control channel. where the bit rate in each channel Fb/3.the bit enter I and C channel enter the I channel 2 to 4 level converter .and the bits in the Q and ~~C~~ enter the 2 to 4 level converter.eith to input bits four output voltages are possible.where the 2 to 4 level converter are digital to analog converters which is a quite simple algorithm.the I or Q bit determine the polarity of the output analog signal (logic 1 =+V and logic 0 = - v)where C or ~~C~~ bit determines the magnitude (logic 1 =1.307V and logic 0 = 0.541).consequently with two magnitude and two polarity ,four different output conditions are possible.

PHASOR DIAGRAM



Binary input			8-PSK output phase
Q	I	C	
0	0	0	−112.5°
0	0	1	−157.5°
0	1	0	−67.5°
0	1	1	−22.5°
1	0	0	+112.5°
1	0	1	+157.5°
1	1	0	+67.5°
1	1	1	+22.5°



Constellation diagram

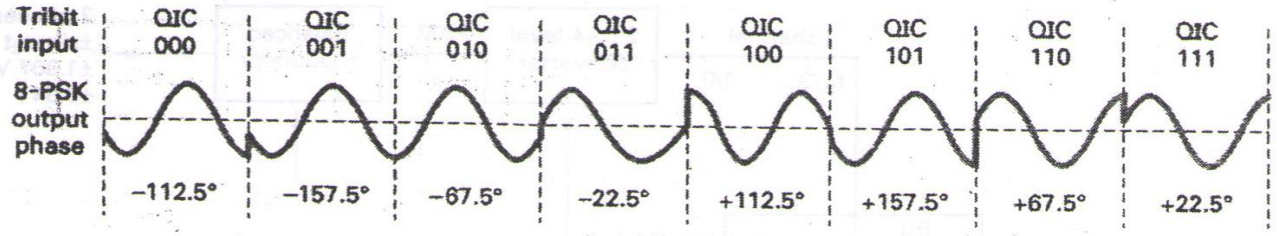
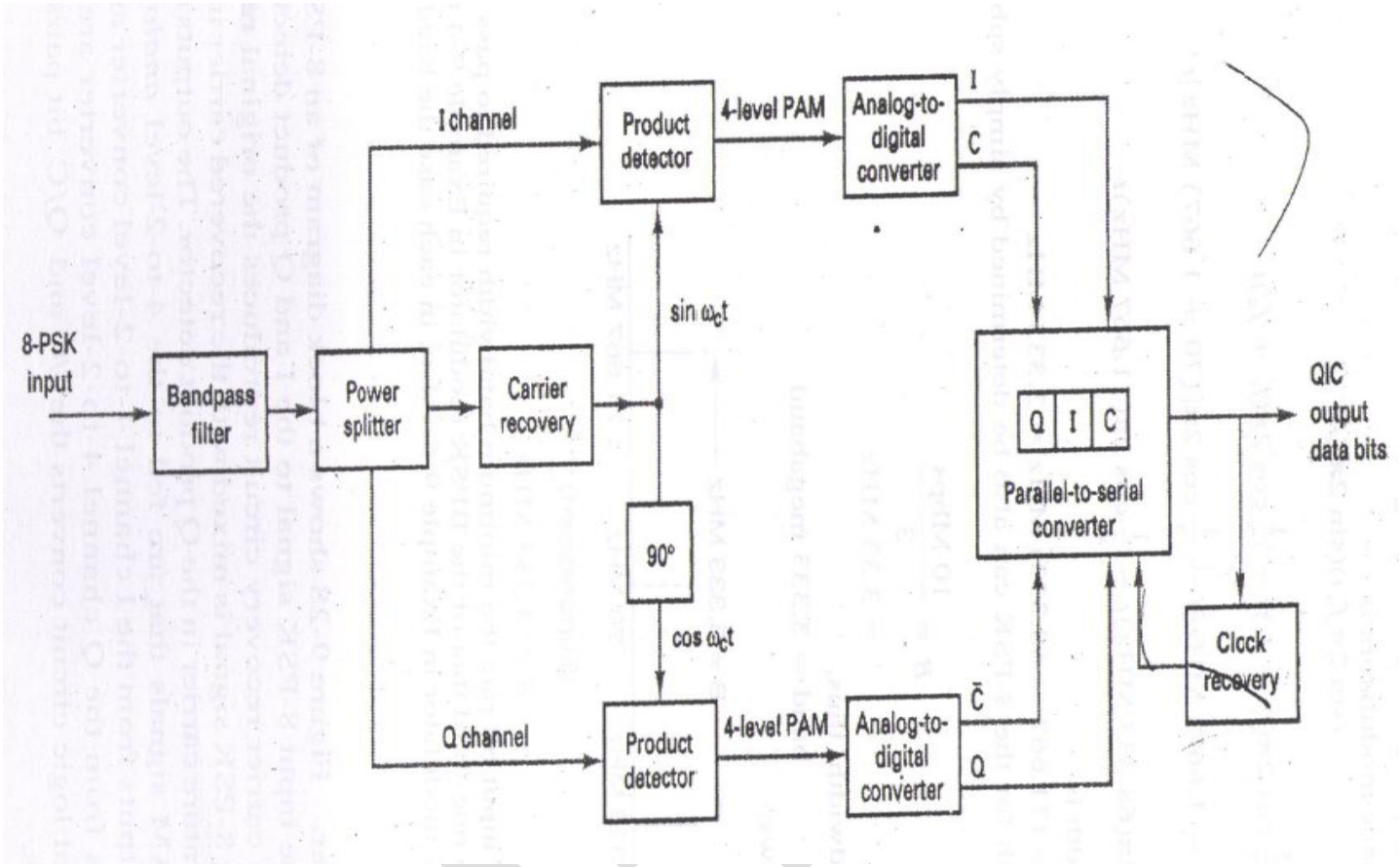


FIGURE 9-26 Output phase-versus-time relationship for an 8-PSK modulator

BANDWIDTH = Fb/3

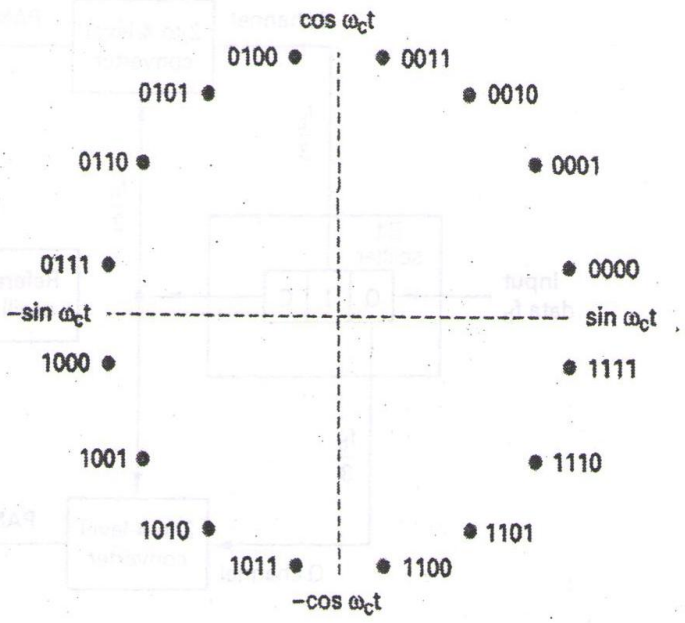
8-QPSK RECEIVER



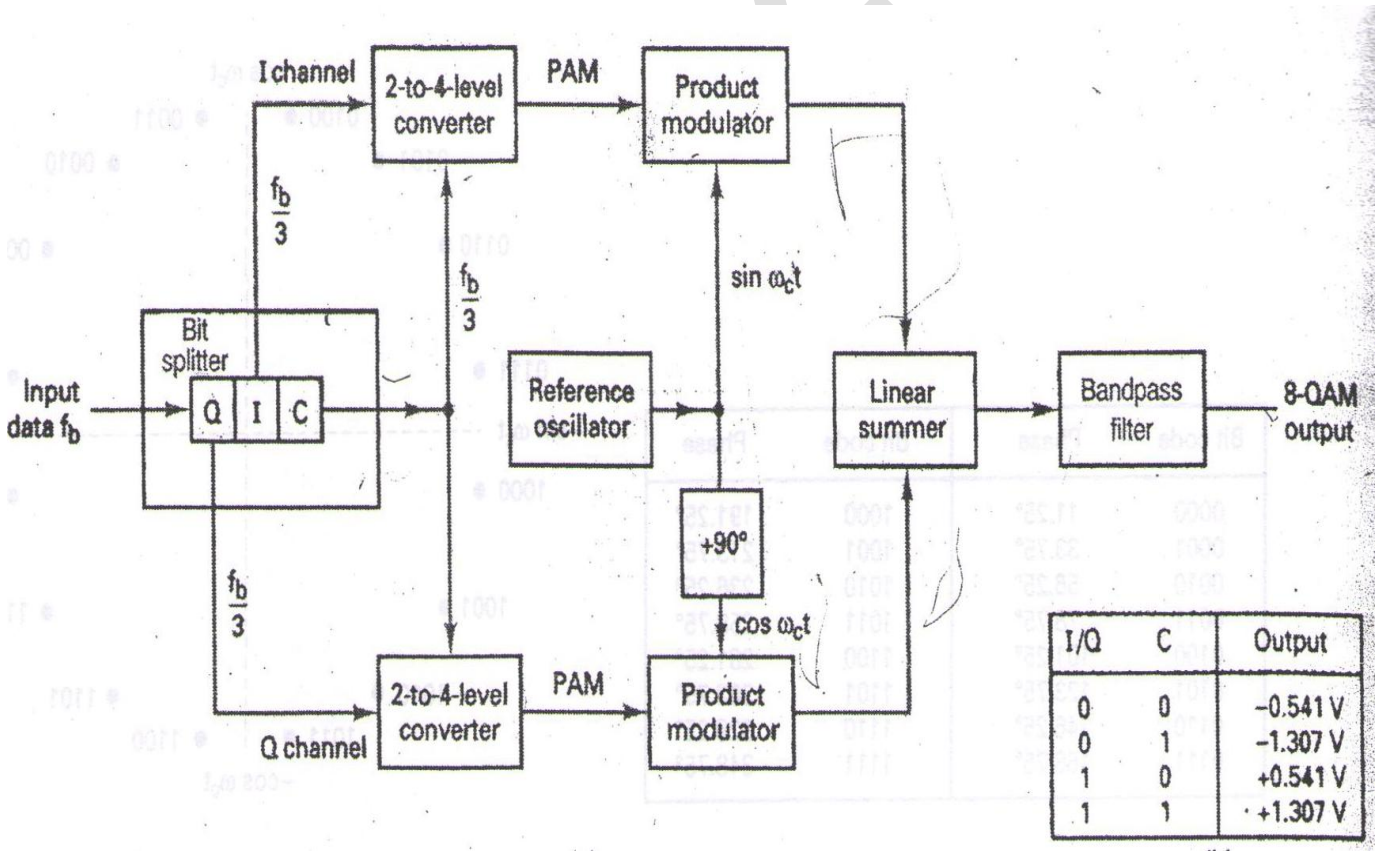
The power splitter directs the input 8-PSK directs the input to the I and Q product detector and the carrier recovery unit.the carrier unit generates the original reference signal .the incoming signal is made product in the product detector .the output of the is a 4 level PAM signal and fed to the 4 – to -2 level analog to digital converters .the output from the I channel 4 to 2 level converter are he I and C bits .where the Q channel gives the Q and C̄ bits output.this parellel bits are converted to serial I,Q and C bit streams.

8 QPSK TRUTH TABLE AND CONSTILLATION DIAGRAM

Bit code	Phase	Bit code	Phase
0000	11.25°	1000	191.25°
0001	33.75°	1001	213.75°
0010	56.25°	1010	236.25°
0011	78.75°	1011	258.75°
0100	101.25°	1100	281.25°
0101	123.75°	1101	303.75°
0110	146.25°	1110	326.25°
0111	168.75°	1111	348.75°



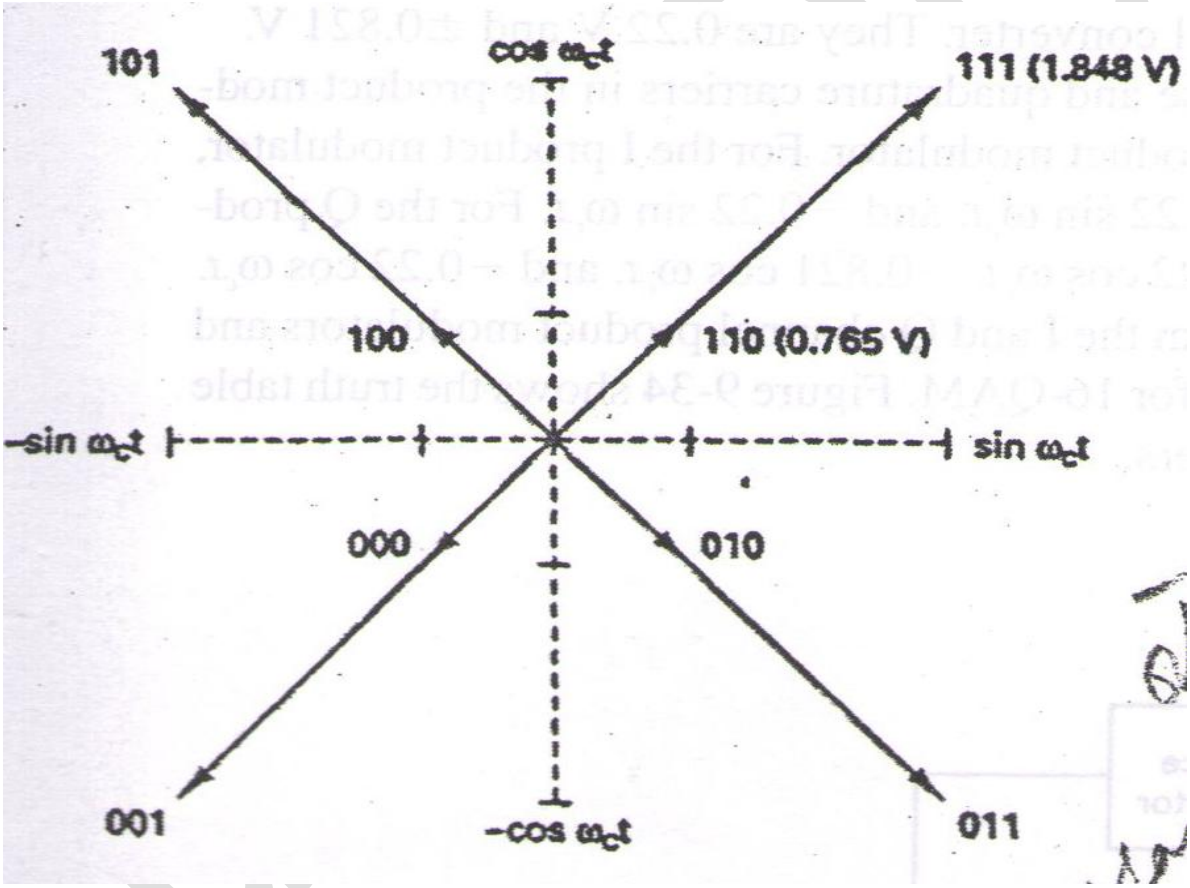
QUADRATURE AMPLITUDE MODULATION 8 – QAM TRANSMITTER



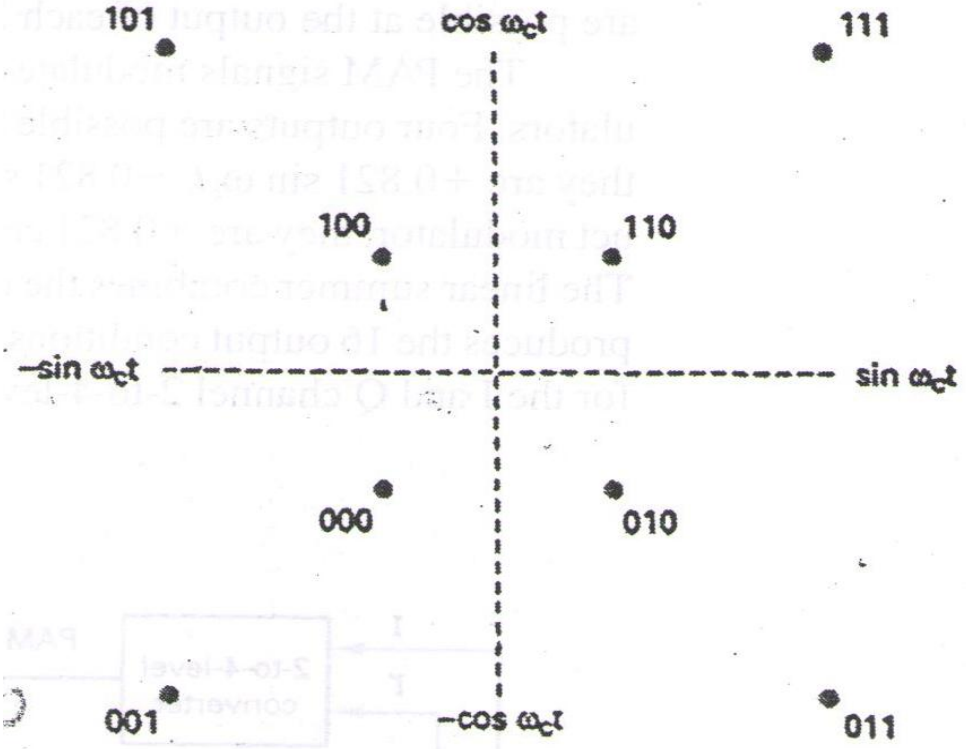
I/Q	C	Output
0	0	−0.541 V
0	1	−1.307 V
1	0	+0.541 V
1	1	+1.307 V

It is similar to that of 8 psk where the inverted control C bit is removed from the block and given to the 2 to 4 level converter .the I and Q bits determine the polarity of the PAM signal at the output of the 2 to 4 level converter.c channel determines the magnitude of the and fed to the 2 to 4 level converter where the magnitude are equal where the I and Q PAM signal are always same.

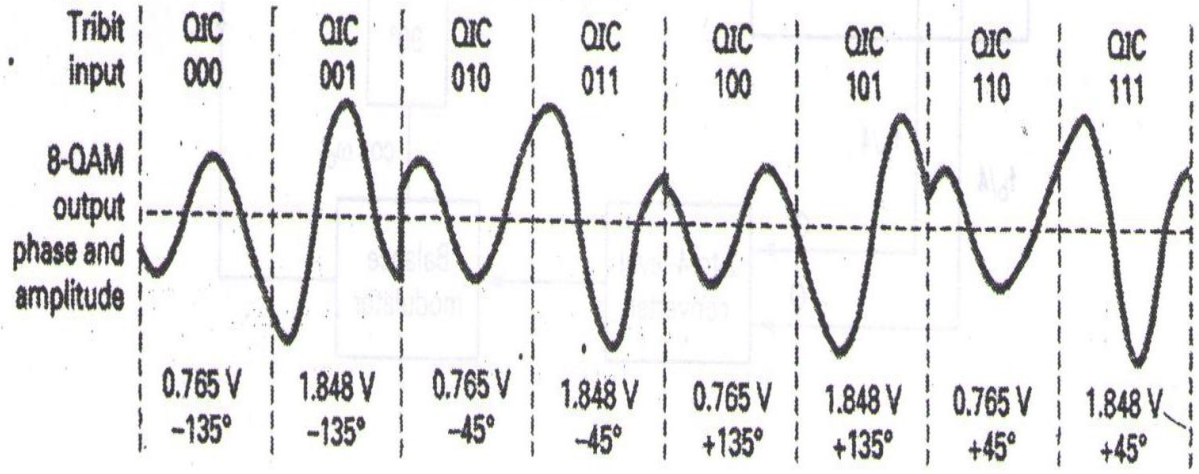
PHASOR DIG



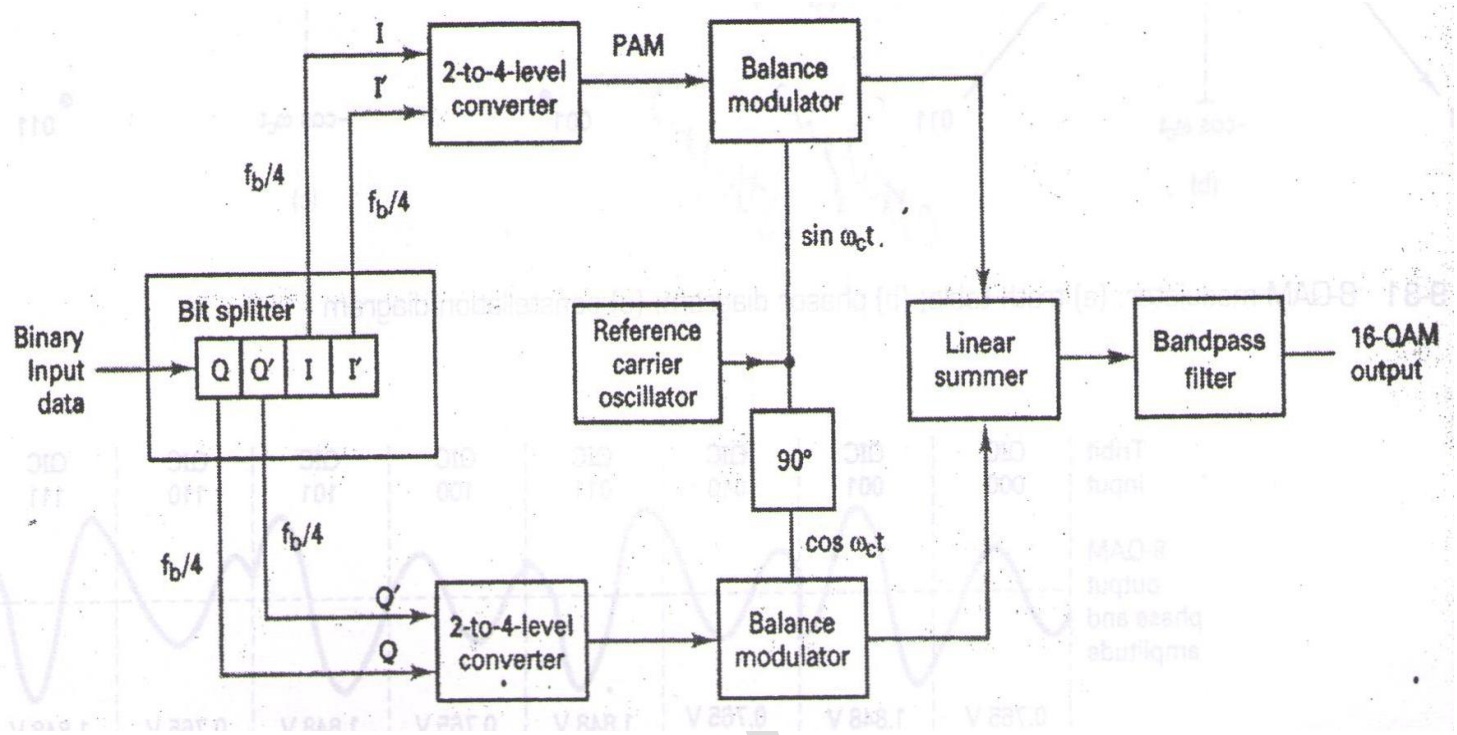
CONSTELLATION DIAGRAM

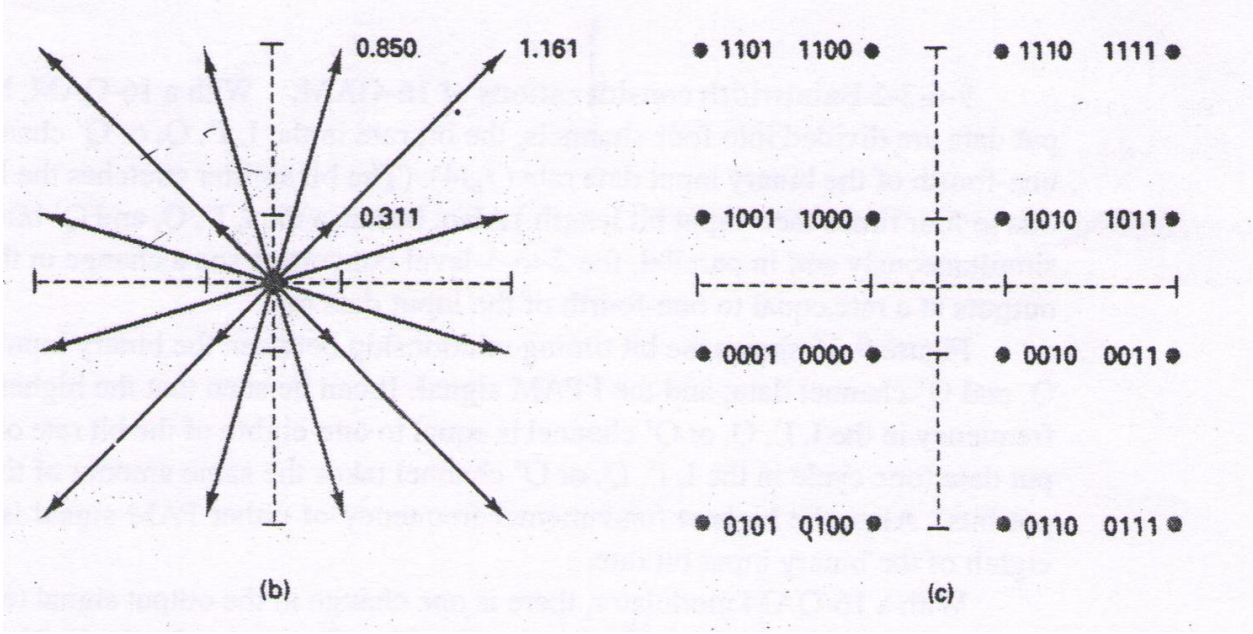


OUTPUT PHASE AND AMPLITUDE RELATION SHIP



16 – QAM TRANSMITTER





PHASOR DIAGRAM **CONSTELLATION DIAGRAM**

COMPRASION OF DIGITAL MODULATION

Table 9-1 ASK, FSK, PSK, and QAM Summary

Modulation	Encoding Scheme	Outputs Possible	Minimum Bandwidth	Baud
ASK	Single bit	2	f_b	f_b
FSK	Single bit	2	f_b	f_b
BPSK	Single bit	2	f_b	f_b
QPSK	Dibits	4	$f_b/2$	$f_b/2$
8-PSK	Tribits	8	$f_b/3$	$f_b/3$
8-QAM	Tribits	8	$f_b/3$	$f_b/3$
16-QAM	Quadbits	16	$f_b/4$	$f_b/4$
16-PSK	Quadbits	16	$f_b/4$	$f_b/4$
32-PSK	Five bits	32	$f_b/5$	$f_b/5$
32-QAM	Five bits	32	$f_b/5$	$f_b/5$
64-PSK	Six bits	64	$f_b/6$	$f_b/6$
64-QAM	Six bits	64	$f_b/6$	$f_b/6$
128-PSK	Seven bits	128	$f_b/7$	$f_b/7$
128-QAM	Seven bits	128	$f_b/7$	$f_b/7$

Note: f_b indicates a magnitude equal to the input bit rate.

BANDWIDTH EFFICIENCY

It is the ratio of the transmission bit rate to the minimum bandwidth required for a particular modulation scheme.

$$B\eta = \frac{\text{transmission bit rate (bps)}}{\text{minimum bandwidth (Hz)}}$$

$$= \frac{\text{bits/s}}{\text{hertz}} = \frac{\text{bits/s}}{\text{cycles/s}} = \frac{\text{bits}}{\text{cycle}}$$

where $B\eta$ = bandwidth efficiency