UNIT-I: THE 8086 MICROPROCESSOR
PART-A

1. What are the types of instruction sets of 8086 microprocessor?

There are eight types of instructions. They are

a) Data copy/Transfer instructions
b) Arithmetic & Logical instructions
c) Branch instructions
d) Loop instructions
e) Machine control instructions
f) Flag manipulation instructions
g) Shift & rotate instructions
h) String instructions

2. What are flag manipulation instructions?

The instructions that directly modify the flags of 8086 are called as the flag manipulation instructions.

E.g.: CLC --- clear carry flag, CMC --- complement carry flag, STC --- set carry flag
CLD --- clear direction flag

3. Explain the instructions LODS & STOS.

a) LODS: Load String Byte or String Word
- The LODS instruction loads the AL/AX register by the content of a string pointed to by DS: SI registers pair.
- The SI is modified automatically depending on direction flag. If it is a byte transfer (LODSB), the SI is modified by one & if it is a word transfer (LODSW), the SI is modified by two.
- No other flags are affected by this instruction.

b) STOS: Store String Byte or String Word
- The STOS instruction stores the AL/AX register contents to a location in the string pointed by ES: DI register pair.
- The DI is modified accordingly.
- No flags are modified by this instruction.

4. Define control transfer instruction & explain their types.

- The instructions that transfer the flow of execution of the program to a new address specified in the instruction directly or indirectly are called the control transfer or Branching instructions.
- They are of two types.

a) Unconditional control transfer instructions: In these types of instructions, the execution control is transferred to the specified location independent of any status or condition.
b) Unconditional control transfer instructions: In these instructions, The control is transferred to the specified location provided the result of the previous operation satisfies a particular condition, otherwise, the execution continues in normal flow sequence.

5. Write a program to generate a delay of 100 ms using 8086.

- The required delay Td=100 ms

	Instructions selected	states for execution
	MOV CX, COUNT	4
L1	DEC CX	2
	NOP	3
	JNZ L1	16

- No. of clock cycles for execution of the loop once =2+3+16 = 21
- Time required to execute the loop once is 21*.1=2.1 micro sec.
  COUNT=required delay (td),N* T
- Required count = 100*10^-3
  2.1*10^-6
  = 47.619*10^3

= 47619
= BA03 H

6. What are assembler directives? Give example.

The assembler is a program used to convert an assembly language program into the equivalent machine code modules that may be further converted to executable codes. Therefore the hints given to the assembler to complete all these tasks in some predefined alphabetical strings is called an assembler directive.

Eg: DB------define byte,END----end of program,EQU-----equate

7. Which interrupt has got the highest priority among all the external interrupts?

The Non-Maskable Interrupt pin of 8086 has got the highest priority among the external interrupts.

8. When is a processor said to have multiple interrupt processing capability?

When a number of devices interrupt a CPU at a time, & if the processor is able to handle them properly, then the processor is said to have a multiple interrupt processing capability.

9. Define a MACRO.

- A number of instructions appearing again & again in the main program can be assigned as a macro definition (i.e.) a label is assigned to the repeatedly appearing string of instructions.
- The process of assigning a label or macro name to the string is called defining a macro. A macro within a macro is called a nested macro.

10. Given

ADD AL, CL
DAA
AL=53 CL=29

Give the output.

ADD AL, CL ; AL← AL+CL
; AL← 53+29
; AL←7C
C>09
DAA ; AL←7C+06
; AL←82

11. What are the segment registers present in 8086?

There are four segment registers in 8086.They are

i. Code Segment register (CS)
ii. Data Segment register (DS)
iii. Extra Segment register (ES)
iv. Stack Segment register (SS).

12. What are the units of the 8086 microprocessor?

The 8086 microprocessor is divided into two units

i. Bus Interface Unit
ii. Execution Unit.

13. What do you mean by instruction pipelining?

While the execution unit executes the previously decoded instruction, the Bus Interface Unit fetches the next instruction and places it in the prefetched instruction byte queue. This forms a pipeline.

14. What are the advantages of the segmented memory scheme in 8086?

The following are the advantages of the segmented memory scheme

- Allows the memory capacity to be 1 Mbytes although the actual addresses to be handled are of 16-bit size.
- Allows the placing of code, data and stack portions of the same program in different parts of memory, for data and code protection.
- Permits a program and/or its data to be put into different areas of memory each time program is executed.

15. What is the use of the Trap flag in the flag register of 8086?

When the Trap flag is set, the processor enters the single step execution mode. A trap interrupt is generated after execution of each instruction. The processor executes the current instruction and the control is transferred to the Trap interrupt service routine.

16. List the instruction formats in 8086 instruction set.

There are six general formats of instruction in 8086.They are

i) One byte instruction.
ii) Register to Register.
iii) Register to/from Memory with no Displacement.
iv) Register to/from memory with Displacement.
v) Immediate operand to Register.
vi) Immediate operand to Memory with 16-bit Displacement.

17. What are the addressing modes of sequence control transfer instructions in 8086? Give example.

The addressing modes are

i. Immediate eg: Mov AX,0005H.
ii. Direct eg:Mov AX,[5000H].
iii. Register eg:Mov BX,AX.
iv. Register Indirect eg:Mov AX,[Bx].
v. Indexed eg:Mov AX,[SI].
vi. Register Relative eg:Mov AX,50H[BX].
vii. Based Indexed eg:Mov AX,[Bx] [SI].
viii. Relative Based Indexed eg:Mov AX,50H [BX] [SI].

18. How is the physical address generated in 8086? (or) How 16 bit address is converted into 20 bit address in 8086? (Nov/Dec 2013)

The content of the segment register called as segment address is shifted Left bit-wise four times and to this result, content of an offset register also called as offset address is added, to produce a 20-bit physical address.

eg: segment address →1005H
Offset address →5555H
Segment address → 0001 0000 0000 0101
Shifted by 4 bit positions → 0001 0000 0000 0101 0000
+
Offset address → 0101 0101 0101 0101
Physical address → 0001 0101 0101 1010 0101
1 5 5 A 5

19. What are control transfer instructions?

These instructions transfer control to some predefined address specified in the instruction after their execution. Eg: CALL, INT, RET & JUMP instructions.

20. What are intersegment and intrasegment modes of addressing?

- For control transfer instructions, if the location to which the control is transferred lies in a different segment other than the current one, the mode is called intersegment mode.
- If the destination location lies in the same segment, the mode is called intrasegment mode.

21. What are the differences between 8085 and 8086? (Nov/Dec 2013)

S.No	8085	8086
1	8-bit microprocessor	16-bit microprocessor
2	It is capable of addressing 2^{16} memory locations	It is capable of addressing 2^{20} memory locations
3	Low speed	High speed
4	It can be configured only in single processor mode	It can be configured in single processor mode(Minimum) and Multiprocessor mode(Maximum)

22. Explain XLAT instruction.

- The XLAT (Translate) instruction replaces a byte in the AL register with a byte from a 256-byte, user coded translation table.
- XLAT is useful for translating characters from one code to another like ASCII to EBCDIC and ASCII to HEX etc.

23. Draw the PSW format for 8086.

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
U	U	U	U	OF	DF	IF	TF	SF	ZF	U	AF	U	PF	U	CF

U : Undefined
CF : Carry flag - Set by carry out of MSB
PF : Parity flag - set if result has even parity
AF : Auxiliary carry flag - used for BCD operation
ZF : Zero flag - set if result = 0
SF : Sign flag - set if result is –ve.
TF : Trap flag - set to enable single step execution mode.
IF : Interrupt flag - set to enable interrupt
DF : Direction flag - set to enable auto decrement mode for string operation
OF : Overflow flag - used for signed arithmetic operation

24. Explain the function of TEST pin in 8086

This input is examined by a "WAIT" instruction. When the processor executes WAIT instruction it enters into wait state (Idle state). If the TEST pin goes low, the processor will come out from the idle state and continues the execution; otherwise it remains in an idle state.

25. What is the function of parity flag? (Nov/Dec 2013)

The parity flag is set, if the result of the byte operation or lower byte of the word operation contains an even number of ones.

26. Give the operation of CBW and TEST instructions of 8086? (Nov/Dec 2013)

CBW instruction converts the byte in AL to word value in AX by extending the sign of AL throughout the register AH.

TEST instruction performs logical AND operation of the two operands updating the flag register without saving the result.

27. What do you mean by addressing modes? (May/Jun 2014)

The addressing modes clearly specify the location of the operand and also how its location may be determined.

28. What is meant by a vectored interrupt? (May/Jun 2014)

There is an interrupt vector table which stores the information regarding the location of interrupt service routine (ISR) of various interrupt. Whenever an interrupt occurs the memory location of ISR is determined using the vector table and the program control branches to ISR after saving the flags and the program location (Instruction Pointer and Code Segment Register) in the stack

PART-B

1. Discuss in detail the three types of interrupt system of Intel 8086.
2. Explain the memory concepts of Intel 8086 and explain how data transfer takes place.
3. Describe the addressing modes 8086 with examples from instruction set of 8086.
4 .Explain the internal architecture of 8086 and explain the functions of each block in detail. **(Nov/Dec 2013)**
5. Draw the pin details of 8086 and explain the function of each pin.
6. List out and explain the 8086 instruction used for address object transfers.
7. Design a microcomputer based on 8086 with 16k EPROM and 16K RAM.
8. Write an 8086 ALP to logically shift a 16 bit number stored in location starting at 8000H twice to the right. Store the result in A000 H.
9. Draw the interface diagram to connect a 32 KB RAM to 8086 processor.
10. Explain the different instruction used for input and output operation in I/O mapped I/O mode of 8086.
11. Describe the 8086 min and max mode signals. Also explain with timing diagram how 8086 executes a bus cycle.

12. Discuss the memory segmentation in the 8086. Explain how a variety of program and data memory sizes can be obtained.
13. Discuss in detail the hardware and software feature of 8086 interrupt structure.
14. Draw the functional block diagram of 8086 processor and explain about the registers and their functions.
15. What are the data related addressing modes used in 8086? Explain each with neat diagrams.(10)
16. Compare memory mapped I/O with I/O mapped I/O. (6)
17. Show the ODD, EVEN memory bank arrangement with reference to 8086.
18. Explain byte data and word data are need from ODD addressed locations and EVEN addressed locations. (10)
19. Explain the register organization of the 8086. Discuss how the physical address generation is carried out.
20. What is meant by memory segmentation? What are the advantages of memory segmentation?
21. Draw and discuss the interrupt structure of 8086. **(May/Jun 2014)**
22. Write an 8086 ALP to sort out any given ten numbers in ascending and descending order. **(Nov/Dec 2013)**
23. Give the functions of NMI, BHE and TEST pins of 8086. (4) **(Nov/Dec 2013)**

UNIT-II: 8086 SYSTEM BUS STRUCTURE

PART – A

1. What is meant by multiprocessor system?

In a microprocessor system contains two or more components that can excute insections independtely then the system is called as multi processor system

2. What are the architectures of multiprocessor system?

Loosely coupled architecture
Closely coupled architecture

3. What is closely coupled configuration

If the processor supporting processor, clock generator, bus control logic, memory and I/O System, communicate shared memory then it is called closely coupled system.

4. What the advantages are of loosely coupled?

1.Better system throughput by having more than one processor
2.A greater degree of parallel processing can be achieved
3.system structure is more flexible
4.A failure in one module does not cause any breakdown of the system.

5.What is meant by cross bar switch

If the number of buses in a common bus system is increased, a point is reached at which there is a separate path available for each memory module. This interconnection is called as crossbar switch

6.Mention some network topologies?

There are three basic network topologies

1.The bus
2.The star
3.The star wires ring (Token Ring)

7.What is meant by memory contention

A memeory module can handle only one access request at a time. Hence when several processors request the same memory module.

8.What is hot spot contention

When several processors repeatedly across the same memory location, it gives rise to hot spot contention.

9. Name some techniques for reducing contentions

1.Local memories
2.Better interconnection network
3.Cache memory
4.Memory Allocation

10.What is meant by bus arbitration

The mechanism which decides the selection of current master to access bus is known as bus arbitration.

11.What are the advantages of Daisy Chaining

1.It is simple and cheaper method

2.It requires the least number of lines and this number is independent of the number of masters in the system

12.What is menat by bus arbitration

The mechanism which decides the selection of current master to access bus ia called bus arbitration.

13.What is meant by Numeric processor

The numeric processor 8087 is a coprocessor which has been specially designed to work under the control of the processor 8086 and to support additional numeric processing capabilities

14.What is meant by instruction Queue

It maintains a 6 Byte instruction queue and tracks a execution of the host

15.On which data types can memery operands operate?

1.Word integer
2.Short integer
3.Long integer
4.Packed BCD
5.Short real
6.Long Real
7.Temporary real

16. List some of the instructions format

1. Data Transfer Instructions
2. Arithmetic Instructions
3. Compare Instructions
4. Transcendental Instructions
5. Load Constant Instructions
6. Processor control Instructions

17. What is the use of TC STOP Mode

If the TC Stop bit is set the channel is disabled after the TC output goes high, thus automatically preventing further DMA Operation on that channel.

18. Name some of the DMA Cycles

DMA Read, DMA Write, DMA Verify

19. Name some of the DMA Cycles.

Idle Cycle and Active Cycle

20. What are the modes in DMA?

Single Transfer Mode
Block Transfer Mode
Demand Transfer Mode
Cascade Mode

21. What is co-processor? (Nov/Dec 2013)

The 8086/8088 must be supplemented with co-processors that extends the instruction set to allow the necessary special computations to be accomplished more efficiently. Eg: 8087 Numeric Data Processor.

22. What is a Floating point Coprocessor? (Nov/Dec 2013)

The floating point coprocessor uses real data types or floating point types of the following format:
Real data $X=\pm 2^{exp} \times$mantissa, which may vary from extremely small to extremely large values.

23. What are advantages of coprocessor? (May/Jun 2014)

The co-processors are supplementary processors which can fetch operands and execute it**.**
It can read CPU status and queue status, make bus and interrupt request, receive reset and ready signals, receive bus grants, maintain an instruction queue and decode the external opcode.

24. What is meant by loosely coupled configuration? (May/Jun 2014)

In a loosely coupled multiprocessor system each CPU has its own bus control logic and bus arbitration is resolved by extending this logic and adding external logic that is common to all the modules.

PART-B

1. How do you group the instructions of 8087 NDP according to their function? Also name and explain the types of operations that can be performed using instructions in each group.
2. Explain with the suitable diagram the co-processor configuration of multiprocessing system.
3. Explain the internal structure of 8087 NDP.
4. Explain how the coprocessor interfaced to a CPU. Explain the different multiprocessor configuration in which the coprocessor can be used.
5. Explain the salient features of 8087 NDP and explain how it's use enhance the performance of the host processor.
6. Explain the different numerical data processors supported by 8086. Compare the performance of 8087 with 8086 and without coprocessor.
7. In what ways are a standard microprocessor & coprocessor different from each other? Discuss the different data formats of 8087 NDP.
8. Draw the block diagram of 8089 IOP and explain. **(May/Jun 2014)**
9. How do you classify the instruction set of 8089 IOP.
10. Explain the instruction set of IOP Explain the bus interfacing controller used with Coprocessor.
11. Discuss the instruction set of I/O Coprocessor. Explain the bus arbiter.
12. Draw the functional block diagram of the I/O Processor (8089) and explain its working in the remote mode. **(Nov/Dec 2013).**
13. What is a bus arbiter? Explain the functions of bus arbiter and briefly explain the addressing modes supported by 8089 I/O processor.
14. Assume that a loosely coupled multiprocessor system consists of the following three module:
    Module A: An 8086 with a local memory.
    Module B: Two 8089s with a local I/O bus.
    Module C: An 8086 with an 8087 and an 8089. (8)
    Determine and discuss the major bus interface devices required for each module.
15. Discuss the architectural features of 8086 that support multiprocessor design. (10)
16. .Define a macro that produces code for adding two binary N-byte operands and storing the N-byte result beginning at an arbitrary location. N is to be the name of a constant and is to appear as the fourth dummy parameter. (6)
17. How does an 8086/8088 cooperate and communicate with
    i) A coprocessor and ii) and an IOP.(16)

18. (i) Write an 8086 assembly language program to get an input from the keyboard for 2 digits and convert that input into a hexa decimal number using BIOS int. (8) **(May/Jun 2014)**
(ii) Write an 8086 assembly language program to multiply 2 digit numbers by getting an input from the keyboard using BIOS interrupt call. (8)
19.(i) Explain the execution steps of 8087 coprocessor. (8) **(May/Jun 2014)**
20. Explain the closely coupled configuration of multi-processor configuration with suitable diagram. **(May/Jun 2014)**
21. Explain the maximum mode and minimum mode of operation of 8086. **(Nov/Dec 2013)**
22. Differentiate closely coupled configuration and loosely coupled configuration. (6) **(Nov/Dec 2013)**

UNIT-III I/O INTERFACING

PART –A

1. **Name the Command word to set bit PC, using BSR mode.**

0	D6	D5	D4	D3	D2	D1	D0

D6,D5,D4 – Don't Care
D3,D2,D1- Bit Select
Do- Bit set.Reset

2. **Why the 8255A is designed so that only the bits in PORT C can be set/reset?**
Since the pins are designed to activate for selecting PortA and Port B.
3. **What is the use of BSR mode in 8255**
It is used for setting and Reset the Bits

4. **How many I/O devices with a word length of 1 bit can be connected to 8255 PPI**
   8 I/O devices can be connected to 8255 PPI
5. **How does 8255 PPI discriminate between the memory section data and I/O section data**
   The 8255 PPI discriminate between memory section data and I/O Section by use of the Address lines and by use of the decoder.
6. **What is the function of STB and OBF signal in the 8255 when programmed for mode –1 operation?**
   The input device activates this signal to indicate CPU that the data to be read is already sent on the port lines of 8255 port.
7. **Name the major block of 8259 Programmable Interrupt Controller.**
   There are three major blocks
   1.Inrerrupt service reg
   2.Priority resolver
   3.Interrrupt Request Register
   4.Interrupt Mask Reg
8. **What are the modes of operation of 8259 Interrupt Controller?**
   1.Fully Nested Mode
   2.Special Fully Mode
   3.Rotating Priority Mode
   4.Special masked Mode
   5.Polled Mode
9. **What is the maximum number of devices that can be connected to interrupt mode**
   We can connect 8 Devices in the interrupt mode
10. **Mention the function of SP/EN signal in the 8259 PIC.**
    With the help of SP/EN signal it can either be operated in Master mode and Salve Mode
11. **Why CAS2-CAS0 lines on 8259 PIC are bi-directional?**
    CAS2-CAs0 is used for selecting one of the possible slaves that can be connected.
12. **What is the use of address enable (AEN) pin of 8257 DMA Controller?**
    ALE is used to differentiate between the Address and Data Signals.
13. **What is the use of the READY input of the DMA controller?**
    When the READY PIN is high the data connected to the external devices can be activated.
14. **What is the purpose of the IC 8257?**
    IC 8257 is used for transferring the data from memory to the CPU
15. **What are TC and MARK signal in a DMA controller?**
    TC is used for denoting that Terminal count of the data has been reached.
    MARK is used to indicate the frames that can be sent
16. **List the four possible modes of operation in 8237 DMA controller.**
    1.Rotating Priority Mode
    2.Fixed Priority Mode
    3.Extended Write Mode
    4.TC Stop Mode
    5.Auto Load Mode
17. **What is an USART.**
    Universal Synchronous and asynchronous Receiver and Transmitter is used for transmitting and Receiving data.
18. **Explain TxD and TxE signals.**
    Transmit Data- TXd, TxE- Transmitter Enable
19. **What are the operating modes of 8255? (Nov/Dec 2013)**
    Mode-0, Mode-1 and Mode-2.
20. **What is bus stealing? (Nov/Dec 2013)**
    During DMA data transfer, the I/O component connected to the system bus is given control of the system bus for a bus cycle. This is called bus stealing or cycle stealing.
21. **What are the advantages of Programmable Interval Timer/Counter IC? (May/Jun 2014)**
    - Interrupt a time sharing operating system at evenly spaced intervals.

- Output precisely timed signals with programmed period to an I/O device.
- Count the number of times an event occurs in an external experiment.
- Cause the processor to be interrupted after a programmable number of external events have occurred.

22. List the features of Memory Mapped I/O. (May/Jun 2014)

- The device registers can be accessed and manipulated with any instruction or addressing mode.
- The maximum number of available memory locations are reduced.

PART – B

1. With a block diagram of internal structure of 8255 PPI and explain the functions of each block
2. Illustrate the 8255 mode 1 output and input port timings.
3. With a neat block diagram explain the function of each block of a programmable interrupt controller.
4. Draw the block diagram of DMA controller IC and explain the function of each block.
5. Show the schematic for 8086 system with 8237 DMA controller and explain the operation of the DMA mode of data transfer.
6. With a block schematic explain how a (4x4) matrix hex keyboard can be interfaced to a CPU using 8279 keyboard display controller?
7. With suitable timing diagram and block schematic explain how the double handshake data transfer from peripheral to CPU is achieved? (Use 8255 PPI chip)
8. Draw the interface circuit to interface a 8 bit ADC to a CPU through port lines and explain how the circuit can be used to generate sinusoidal and RAMP waveforms.
9. Interface a keyboard with a microprocessor Explain the software to find the key closure by giving the relevant program.
10. Interface a D/A converter with a microprocessor. Explain with a program, how to generate a sine wave using this.
11. Explain with neat diagram, flow charts, necessary software a keyboard interfacing circuit with software keys debouncing facility.
12. (i) Describe with MODE 0 and MODE 3 configurations of 8254 timer in detail.(8)
    (ii) Draw and explain the operation of a sample and hold circuit. (4)
    (iii) Show the control word format of 8255 and explain how each bit is programmed.(4)
13. Explain the advantages of using the following chips in microprocessor based systems.
    i. USART.(5)
    ii. PIC.(5)
    iii. Keyboard and Display Controller.(6)
14. (i) Explain the mode 0 operation of 8255 Programmable Peripheral interface. (8) **(May/Jun 2014)**
    (ii) Explain the different modes of operation of timer. (8)
15. Explain the internal architecture of 8237 Direct Memory Access Controller. **(May/Jun 2014)**
16. (i) Bring about the features of 8251. (6) **(Nov/Dec 2013)**
    (ii) Discuss how 8251 is used for serial data communication. (6)
    (iii) Explain the advantages of using the USART chips in microprocessor based systems. (4)
17. List the major components of 8279 keyboard display interface and explain their functions. **(Nov/Dec 2013)**
18. Explain design of Traffic Light Controller using 8086 microprocessor in detail.
19. Discuss the operation of LCD display and LED display, by interfacing with 8086 microprocessor.

UNIT-IV: MICROCONTROLLER

PART –A

1. Discuss the salient features of 8051 family of controllers?

- ✓ Eight-bit CPU with registers A (the accumulator) and B.
- ✓ Sixteen-bit program counter (PC) and data pointer (DPTR).

- ✓ Eight-bit program status word (PSW).
- ✓ Eight-bit stack pointer (SP).
- ✓ Internal ROM or EPROM (4 KB).
- ✓ Internal RAM (128 bytes)
  1. Four register banks (each 8 registers)
  2. 16 bytes, which may be addressed at bit level
  3. Eighty bits of general purpose data memory
- ✓ Two 16-bit timer / counters: T0 & T1
- ✓ Full duplex serial data receivers / transmitter (SBUF)
- ✓ Control registers: TCON, TMOD, SCON, PCON, IP and IE.
- ✓ Two external and three internal interrupt sources
- ✓ Oscillator and clock circuits

2.What is the size of RAM in 8051?

The size of the RAM is **128 bytes**

1. Four register banks (each 8 registers)
2. 16 bytes, which may be addressed at bit level
3. Eighty bits of general purpose data memory

3. How many ports are available in 8051 micro controller?

There are mainly four ports available in this 8051 micro controller. They are

Port0: serve as inputs, outputs, or, when used together, as a bi-directional low order address and as data bus for external memory.

Port1: has got no dual functions.

Port2: may be used as an input / output port similar in operation to port 1. The alternate use of port2 is to supply a high-order address byte in conjunction with the Port0 low-order byte to address external memory.

Port3: is an input / output pin similar to the Port 1. In this case each and every pin has an additional function.

PIN	ALTERNATE USE	SFR
P3.0 – RXD	Serial data input	SBUF
P3.1 – TXD	Serial data output	SBUF
P3.2 - INT0	External interrupt 0	TCON.1
P3.3 - INT1	External interrupt 1	TCON.3
P3.4 – T0	External timer 0 input	TMOD
P3.5 – T1	External timer 1 input	TMOD
P3.6 – WR	External memory write pulse	_
P3.7 - RD	External memory read pulse	_

4. State the function of RS1 and RS0 bits in the flag register of Intel 8051.

RS0 and RS1 are the D3 and D4 bits present in the 8-bit register of the PSW (Program Status Word).

RS1	RS0	DESC.
0	0	BANK 0 is selected from Internal ROM
0	1	BANK 1 is selected from Internal ROM
1	0	BANK 2 is selected from Internal ROM
1	1	BANK 3 is selected from Internal ROM

5. What is meant by microcontroller?

A device which contains the microprocessor with integrated peripherals like memory, serial ports, parallel ports, timer/counter, interrupt controller, data acquisition interfaces like ADC, DAC on single chip is called microcontroller.

6. List the flags of 8051 and give their usage.

Status flags: These flags are modified according to the result of arithmetic and logical operations.

1. Carry flag
2. Auxiliary carry flag
3. Overflow flag
4. Parity flag

General purpose user flags: These flags can be set or cleared by the programmer as desired

1. Flag 0
2. GF0
3. GF1

7. What is the difference between microprocessor and microcontroller? (May/Jun 2014)

S.No	Microprocessor	Microcontroller
1.	It has only CPU	It has CPU, memory, timers, parallel and serial I/O port on single chip
2.	It has few bit manipulating instructions	It has large number of bit manipulating instructions
3.	It has more number of instructions for transferring data from external memory.	It has only few instructions for transferring data form external memory.
4.	No special function registers are available	Special functions registers are available

8. What happens in power down mode of 8051 microcontroller?

The memory locations of power down RAM can be maintained through a separate small battery backup supply so that the content of these RAM can be preserved during power failure conditions.

9. Compare the 8051, 8031 and 8751 microcontrollers.

8051	8031	8751
On-chip program memory(ROM) available - 4KB	No on-chip ROM	On-chip program memory(EPROM) available

10. List any applications of Microcontroller.

1. Building control(Fire detection)
2. Industrial control (Process control)
3. Motor speed control(Stepper motor control)
4. Stand alone devices(Color Xerox machine)
5. Automobile applications (Power steering)

11. What is the function of DPTR register?

The data pointer (DPTR) is the 16-bit address register that can be used to fetch any 8 bit data from the data memory space. When it is not being used for this purpose, it can be used as two eight bit registers, DPH and DPL

12. What is the significance of EA line of 8051 microcontroller? (May/Jun 2014)

When there is no on-chip ROM in microcontroller and EA pin is connected to GND, it indicates that the code is stored in external ROM.

13. What is the difference between MOVX and MOV ? (Nov/Dec 2013)

The MOV instruction is used to access code space of on-cip ROM and MOVX instruction is used to access data space or external memory.

14.How is memory organized in 8051?

8051 can access upto 64kb of program memory and 64kb of external data memory and internal data RAM locations.

15. Mention some of the 8051 special function register.

ACC: Accumulator, B: B-Register, PSW: Program Status Word, SP: Stack Pointer, DPTR: Data Pointer, IE: Interrupt Enable, SCON: Serial Control, PCON: Power Control.

16. What is the function of XTAL 1 and XTAL 2 pins?

8051 has internal clock circuit. In this crystal of proper frequency can be connected to these two pins. XTAL 1 is connected to GND and oscillator signal is connected to XTAL 2.

17. **Write an ALP to add the values ABH and 47H. Store the result in R1.**

```
    MOV A, #AB H
    ADD A, #47 H
    MOV R1, A
L1: SJMP L1
```

18. Write the instruction to use registers of bank 3.

SETB PSW.4
SETB PSW.3

19. How is RAM memory space allocated in 8051?

- 32 bytes from 00 to 1F H is for register bank and stack.
- 16 bytes from 20H to 2FH is for bit addressable read/write memory
- 80 byte 30H to 7FH is for scratch pad

20. Differentiate overflow flag and carry flag.

Carry flag is used to detect error in unsigned arithmetic.
Carry flag is used to detect error in unsigned arithmetic.

PART-B

1.Determine the value of the accumulator after the execution of instructions A:,B:, C: and D:

```
MOV 40H , #88H
MOV R0 , #40H
A:  MOV A , R0
B:  MOV A, @R0
C:  MOV A, 40H
D:  MOV A, #40H
```

With neat diagram explain the timer / counter functions in 8051 Micro Controller.

2. Draw the pin configuration of 8051 and explain the function of each pin in detail.(6) **(May/Jun 2014)**
3. Explain in detail the different addressing modes supported by 8051.(6)
4. Draw the architecture of 8051 and explain.(16)
5. Write an ALP to arrange a set of numbers in descending order.(6)
6. Write a program using 8051 assembly language to add three BCD numbers stored in internal RAM locations 25H, 26H and 27H and put the result in RAM locations 31H (MSB) and 30 H (LSB).Use register R0 to store the intermediate result.
7. List the features of 8051 microcontroller. (8)
8. How do you classify the instruction set of 8051? (8)
9. Explain the I/O structure of 8051 μC.(8) **(Nov/Dec 2013) (May/Jun 2014)**
10. Draw the bit pattern of PSW of 8051 μC and explain the significance of each bit with examples.(8)
11. List the special function registers of 8051 μC and explain their functions.(8)
12. Explain the significance of SFR's in 8051 μC.(8)
13. Write an 8051 ALP to sort the numbers stored in an array.(8)
14. Compare the features of 8 bit and 16 bit μC. (8)
15. Explain the internal and external data memory organization of 8051. (10) **(Nov/Dec 2013)**

UNIT-V INTERFACING MICROCONTROLLER

PART-A

1. What is the purpose of counters in 8051 micro controller?

The counters have been included on the chip to relieve the processor of timing and control chores. When the program wishes to count a certain number of internal pulses or external events, a number is placed in one of the counters. The number represents the following: **(Maximum count)-(Desired count) + 1.** The counter increments from the initial number to the maximum and then rolls over to zero on the final pulse.

2. Write short notes on interrupts in 8051?

Interrupts may be generated by internal chip operations or provided by external interrupts sources.

Five interrupts are provided in 8051. Three of these interrupts are generated automatically by internal operations: **Timer flag 0, Timer flag 1, and the serial port interrupts (RI or TI)**. Two interrupts are triggered by external signals provided by the circuitry that is connected to the pins INT0 and INT1 (port pins P3.2 and P3.3).

3. What is the purpose of Interrupt priority (IP) Control register in 8051?

Register IP bits determine if any interrupt is to have a high or low priority. Bits set to 1 give the accompanying interrupt a high priority; a 0 assigns a low priority.If two interrupts with the same priority occur at the same time, then they have the following ranking:

1. IE0, 2.TF0, 3.IE1, 4.TF1,5.Serial = RI or TI

For example, the serial interrupt could be given the highest priority by setting the PS bit in the IP to 1, and all others to 0.

4.What is SBUF?

SBUF stands for SERIAL BUFFER. SBUF is physically two registers. One is write only and is used to hold the data to be transmitted out of the 8051 via TXD. The other one is read only and holds the received data from external sources via RXD. Both mutually exclusive registers use address 99H.

5. What is the basic difference between a timer and a counter?

The only difference between a timer and a counter is the source of clock pulses to the counters.When used as a timer, the clock pulses are sourced from the oscillator through the divide-by-12d circuit. When used as a counter, pin T0 (P3.4) supplies pulses to counter 0, and pin T1(P3.5) to counter 1.

6. Explain the operating mode 0 of 8051 serial port?

- Mode 0 of 8051 serial port is shift register mode.
- Serial data enters and exits through RXD pin.
- Pin TXD is connected to the internal shift frequency pulse source to supply shift pulses to external circuits.
- 8-bits are transmitted and received.
- The baud rate is fixed at 1/12 of the crystal frequency.

7. Define watch dog timer.

- Watch dog timer is a dedicated timer to take care of system malfunction. It can be used to reset the controller during software malfunction, which is referred to as “Hanging”.
- A watchdog timer contains a timer that expires after a certain interval unless it is restarted.
- It resets the microcontroller and starts the software over from the beginning if the software does not restart it periodically.

8. What is the function of the TMOD register?

TMOD (Timer mode) register is used to set the various timer operation modes. TMOD is dedicated solely to the two timers (T0 & T1) and can be considered to be two duplicate 4-bit registers, each of which controls the action of the timers.

9. What is the difference between watch dog timer and ordinary timer? (Nov/Dec 2013)

The watch dog timer is provided for the system to check itself and reset if it is not functioning properly. The watch dog register is a 16 bit-counter which is incremented every state time.

10. List out the advantages of LCD over LED.

- Declining prices of LED,
- Ability to display numbers, characters and graphics
- Incorporating a refreshing controller.
- Ease of programming for characters and graphics.

11.What is the significance of BUSY flag in LCD interfacing?

When D7 pin=1 and RS pin=0 the BUSY flag is set which means that LCD is busy taking care of internal operations and will not accept any new information. Therefore we have to check BUSY flag before writing data to LCD.

12. How a pressed key is detected in keyboard interfacing?

The keyboards are organized in a matrix of rows and columns. The microcontroller grounds all rows by providing zero to the output latch then reads the columns.

13. What is the significance of WR and INTR pin in ADC chip?

WR is an active low input and when it undergoes low to high transition the Start of conversion signal is given. INTR is an active low output pin. It is normally high when the A to D conversion is finished. It goes low to signal EOC.

14.Write an ALP to generate a saw tooth waveform.

```
MOV A.#00H
MOV P1,A
BACK: INC A
SJMP BACK
```

21. What is the significance of PSEN in memory interfacing?

PSEN (Program Store Enable) is an output signal for the 8051 microcontroller, which is connected to the OE pin of external ROM containing the program code. This is used when external ROM has to be accessed.

22. What is the relation between RPM and steps per second in stepper motor interfacing?

Steps per second= (rpm × steps per revolution)/60

23. What are the serial communication modes available in 8051?

Mode 0, Mode 1, Mode 2, Mode 3 are the serial communication modes available in 8051.

24. What are the contents of SCON register?

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

SM0 - Serial port mode bit 0 , **SM1** - Serial port mode bit 1, **SM2** - Serial port mode 2 bit (or) multiprocessor communication enable bit, **REN** - Reception Enable bit, **TB8** - Transmitter bit 8.

RB8 - Receiver bit 8 or the 9th bit received in modes 2 and 3, **TI** - Transmit Interrupt flag,

RI - Receive Interrupt flag.

25. What are the various baud rates possible in 8051 and how are they set?

Baud rate	TH1 (Dec)	TH1 (Hex)
9600	-3	FD
4800	-6	FA
2400	-12	F4
1200	-24	E8

26. What is the frame format for mode 2 serial communication?

The 11 bit frame is classified as: 1 bit for start, 8 bits for data, 1 bit can be programmed, 1 bit for stop.

PART-B

1. Draw the block diagram of Intel 8051 timer/counter and explain its different modes of operations.
2. What are the different timer mode operations of 8051? Explain them in detail.
3. Draw an interfacing circuit using 8051 to read the status of 4 thumb wheel switches and display the status in 7 segment LED after I min delay. Write an ALP for the same.
4. Discuss the interrupt system of the 8051 μC.(8)
5. Explain how to interface i) ADC and ii) DAC with 8051 μC.(16)
6. Explain how to interface external memory devices with 8051 μC.(8)
7. With necessary h/w & s/w details explain how to interface LCD'S with 8051 μC.(16)
8. Explain the different modes of operation of serial port in 8051, indicating various registers associated with it.(16)
9. Describe the structure of 4 parallel ports in 8051 with necessary diagrams.(16)
10. (i)How do you interface 8051 microcontroller with keyboard? Explain in detail. (8)
    (ii) How do you interface 8051 microcontroller with ADC? Explain in detail. (8) **(Nov/Dec 2013)**
11. (i)Vin=2.25V, Vref=5V, NO. of data lines are 5. Convert the given analog quantity to its equivalent digital output quantity. (8) **(May/Jun 2014)**
    (ii) Explain the different techniques to convert digital quantity to its equivalent analog quantity.
12. Explain in detail the procedure to interface stepper motor with 8051.
13. Describe the means to access program code available in external ROM interfaced to 8051.