시스템반도체설계
Final_Project_<7조>

12181762 김현진
12191401 이찬희
12191787 엄찬하

목차

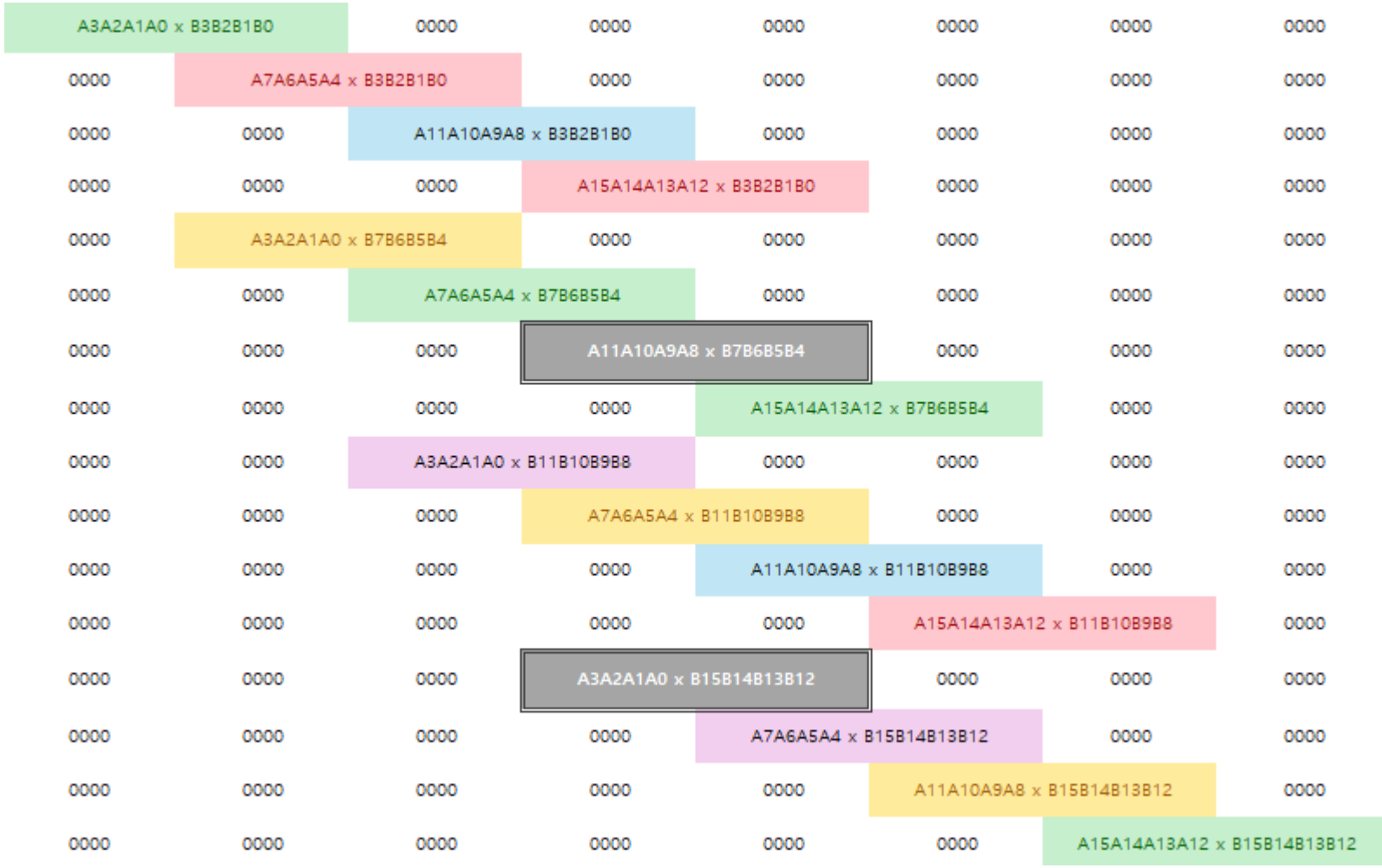
곱셈 방식에 대한 고찰

A.16개, 16개의 인풋을 각각 비트 단위로 곱셈

VS

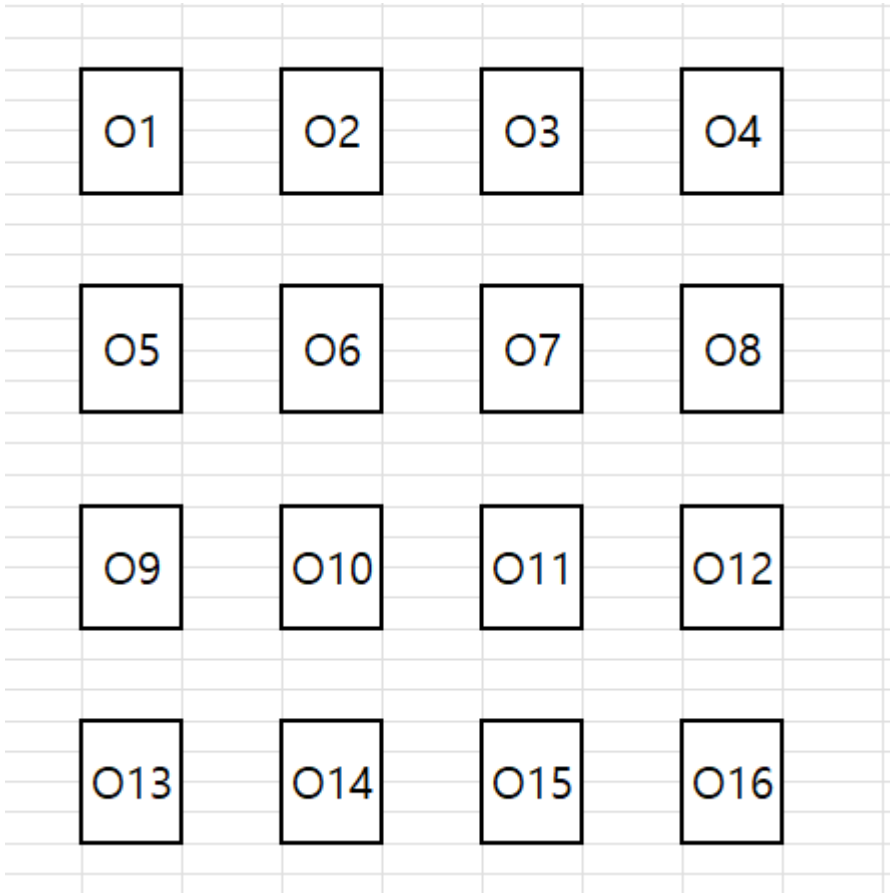
B.16비트를 4비트씩으로 나누어 부분 곱들 간의 곱셈

Partial Product Adding Algorithm(1)



Wallace tree Output

Partial Product Adding Algorithm(2)



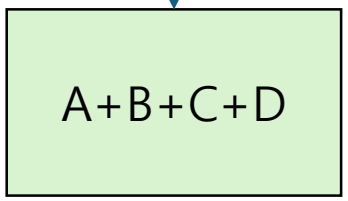
4bit Multiplier의 자리가 다른 출력 16개
->이론적으로 15개의 32bit adder가 필요

Partial Product Adding Algorithm(3)

A3A2A1A0 x B3B2B1B0		A7A6A5A4 x B7B6B5B4		A15A14A13A12 x B7B6B5B4		A15A14A13A12 x B15B14B13B12		A
0000	0000	0000	0000	0000	0000	0000	0000	
0000	A7A6A5A4 x B3B2B1B0		A15A14A13A12 x B3B2B1B0		A15A14A13A12 x B11B10B9B8		0000	B
0000	0000	0000	A11A10A9A8 x B7B6B5B4		0000	0000	0000	
0000	A3A2A1A0 x B7B6B5B4		A7A6A5A4 x B11B10B9B8		A11A10A9A8 x B15B14B13B12		0000	C
0000	0000	0000	A3A2A1A0 x B15B14B13B12		0000	0000	0000	
0000	0000	A11A10A9A8 x B3B2B1B0		A11A10A9A8 x B11B10B9B8		0000	0000	D
0000	0000	A3A2A1A0 x B11B10B9B8		A7A6A5A4 x B15B14B13B12		0000	0000	

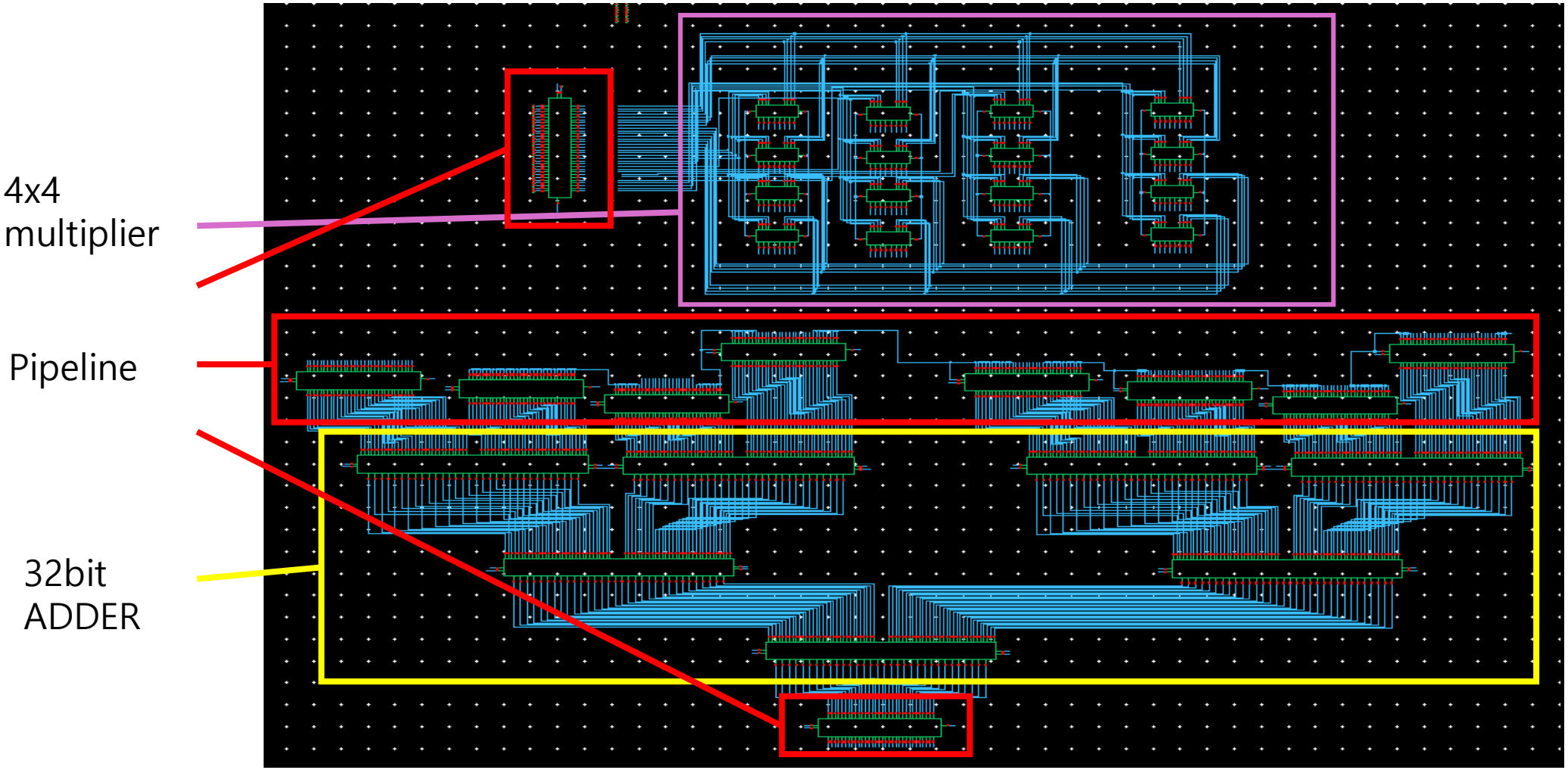
1st stage

2nd stage

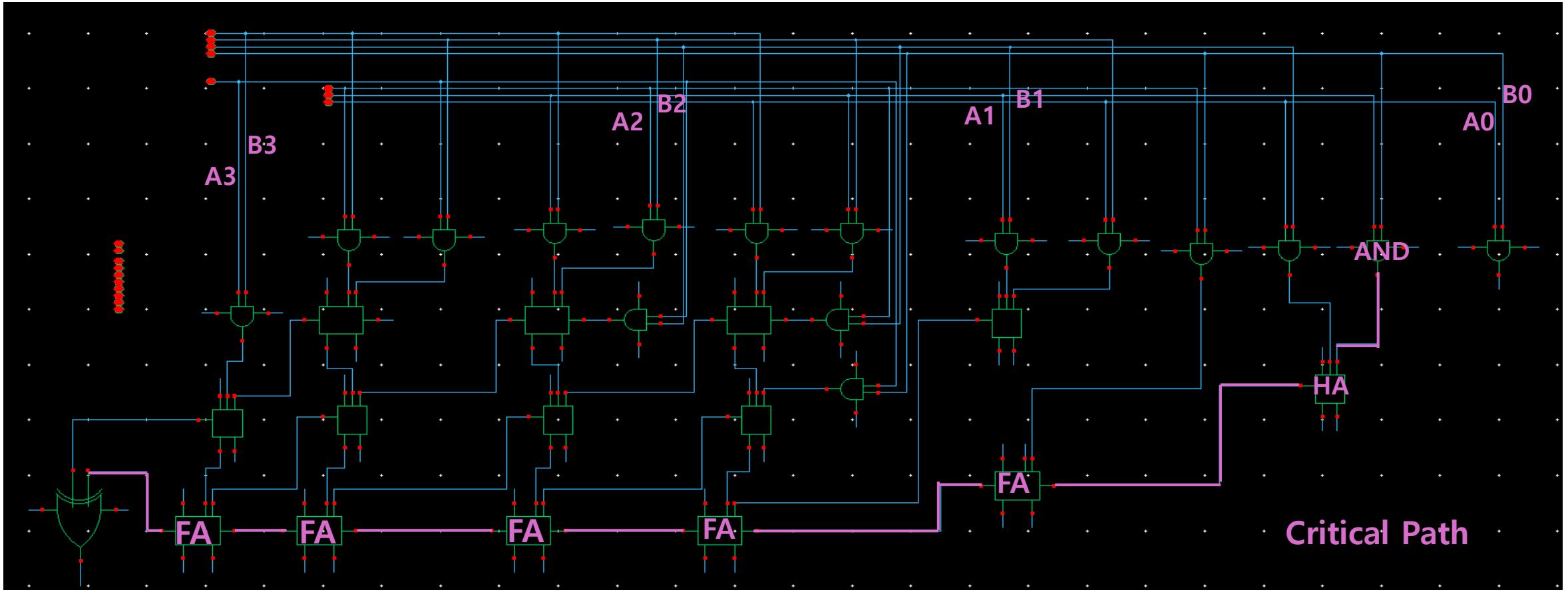


final stage

16bit unsigned multiplier (wallace)



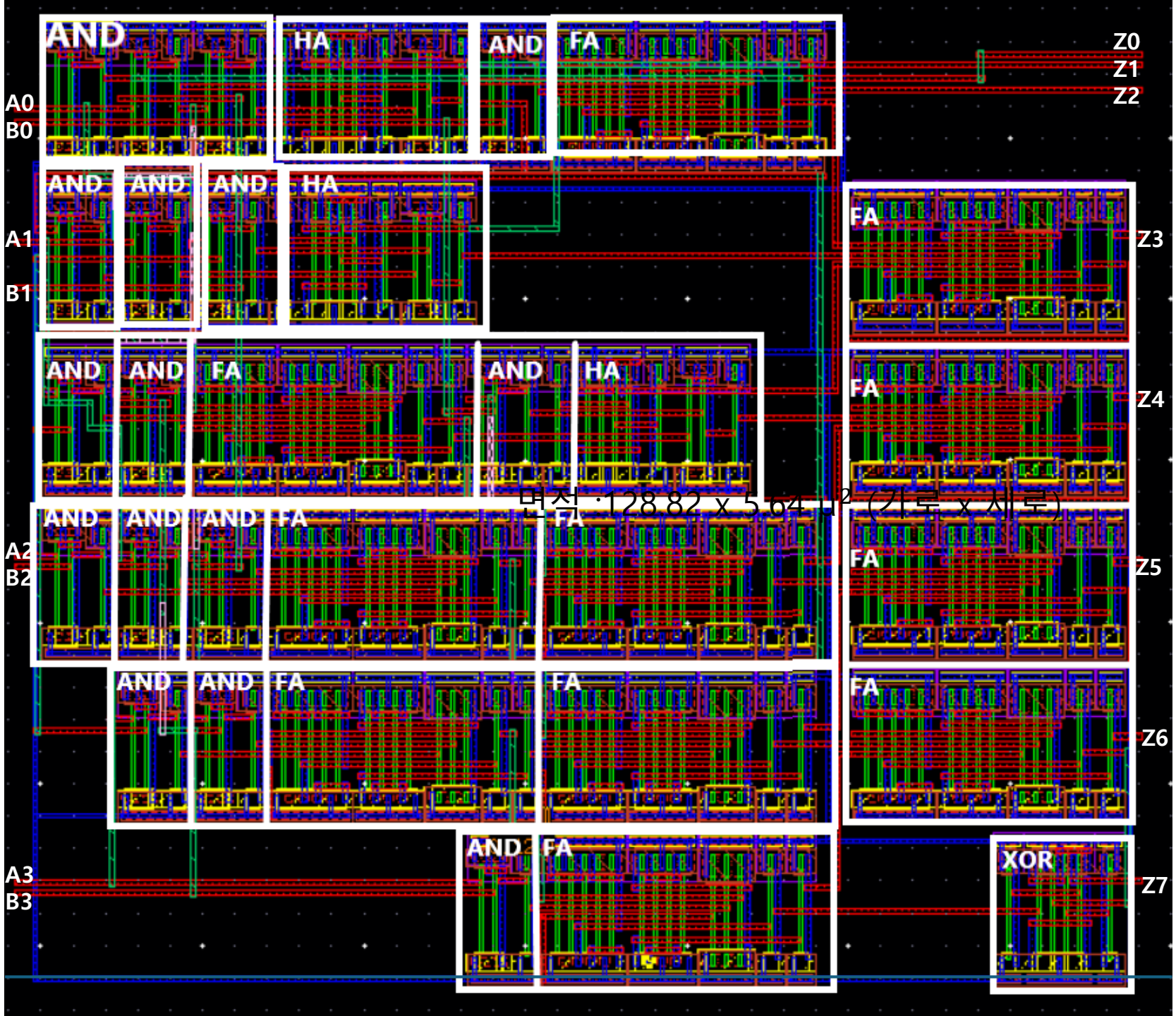
4bit unsigned multiplier (wallace) - Schematic



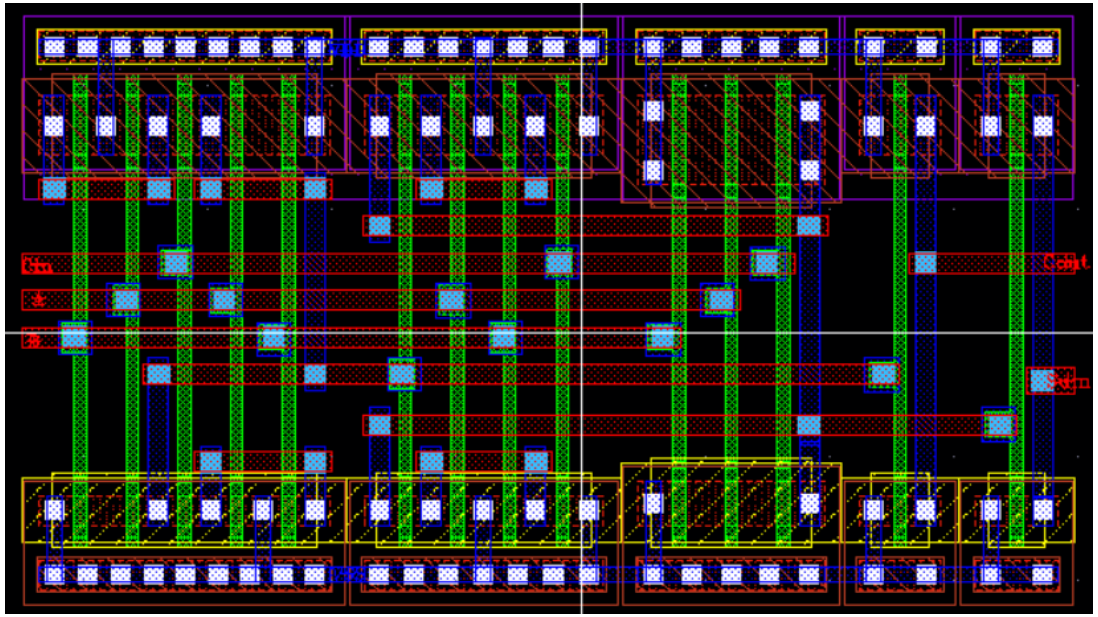
4X4multiplier

<Layout>

면적 ->34.04X29.82 (단위 u^2)



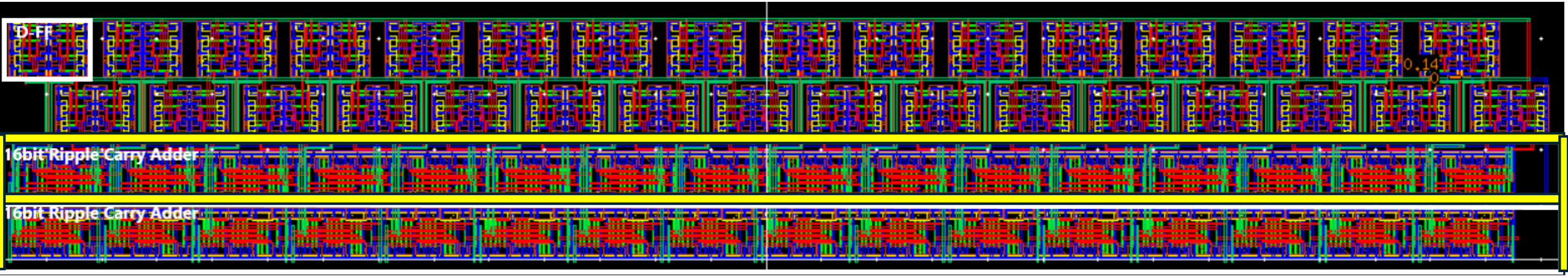
32bit Adder



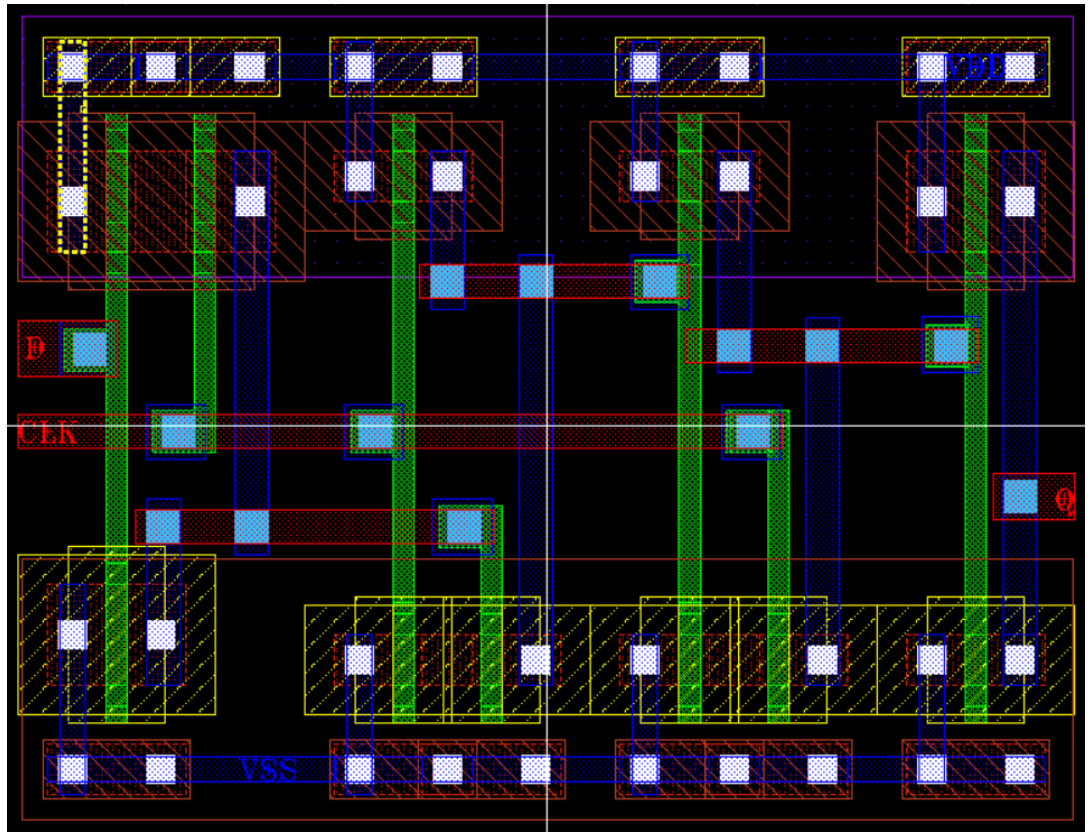
Full_Adder

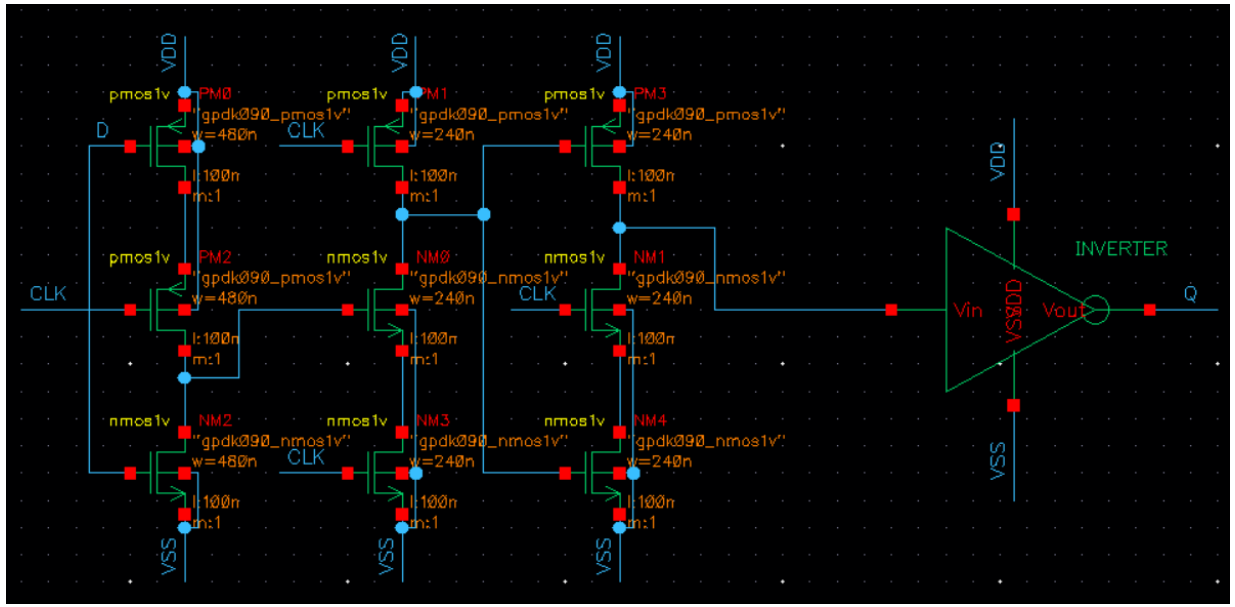
TR 28개 사용

다음 연결을 통해 아래 32bit 구조 설계



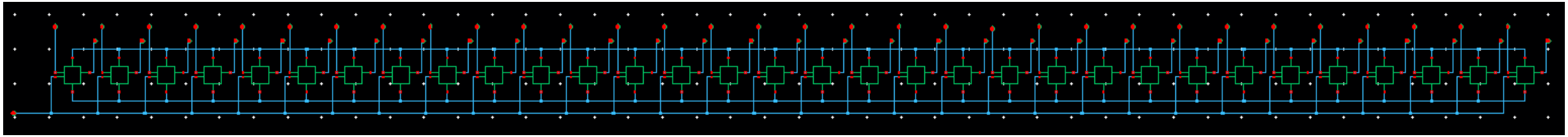
D-FF 설계 설명

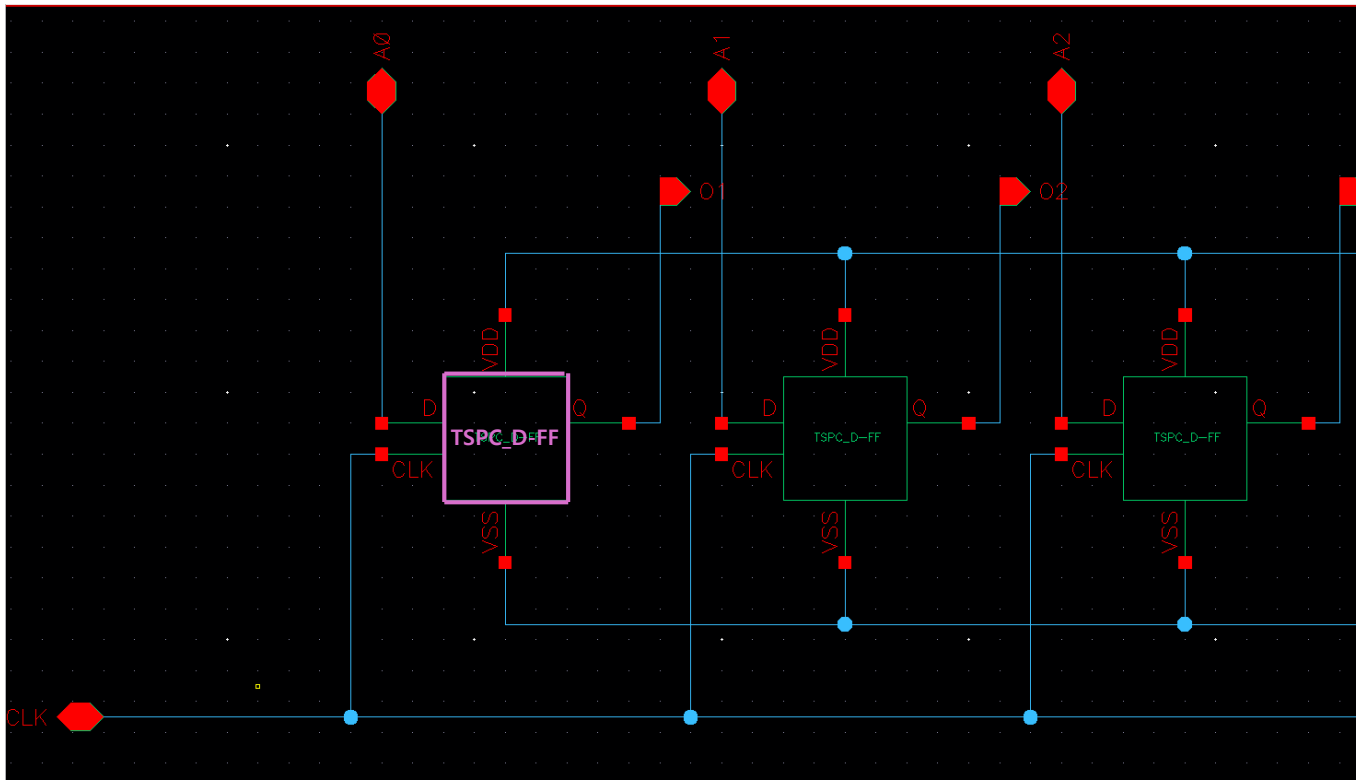

VDD
D
CLK
Q
VSS


VDD
pmos1v
PM0
"gpdk090_pmos1v"
w=480n
l:100n
m:1
D
pmos1v
PM1
"gpdk090_pmos1v"
w=240n
CLK
pmos1v
PM3
"gpdk090_pmos1v"
w=240n
pmos1v
PM2
"gpdk090_pmos1v"
w=480n
CLK
nmos1v
NM0
"gpdk090_nmos1v"
w=240n
nmos1v
NM1
"gpdk090_nmos1v"
w=240n
CLK
nmos1v
NM2
"gpdk090_nmos1v"
w=480n
nmos1v
NM3
"gpdk090_nmos1v"
w=240n
CLK
nmos1v
NM4
"gpdk090_nmos1v"
w=240n
VSS
INVERTER
Vin
Vout
Q

pipelining및 전체 구조설계 및 예측

(Power-Performance-Area, clock speed, 동작속도 등)



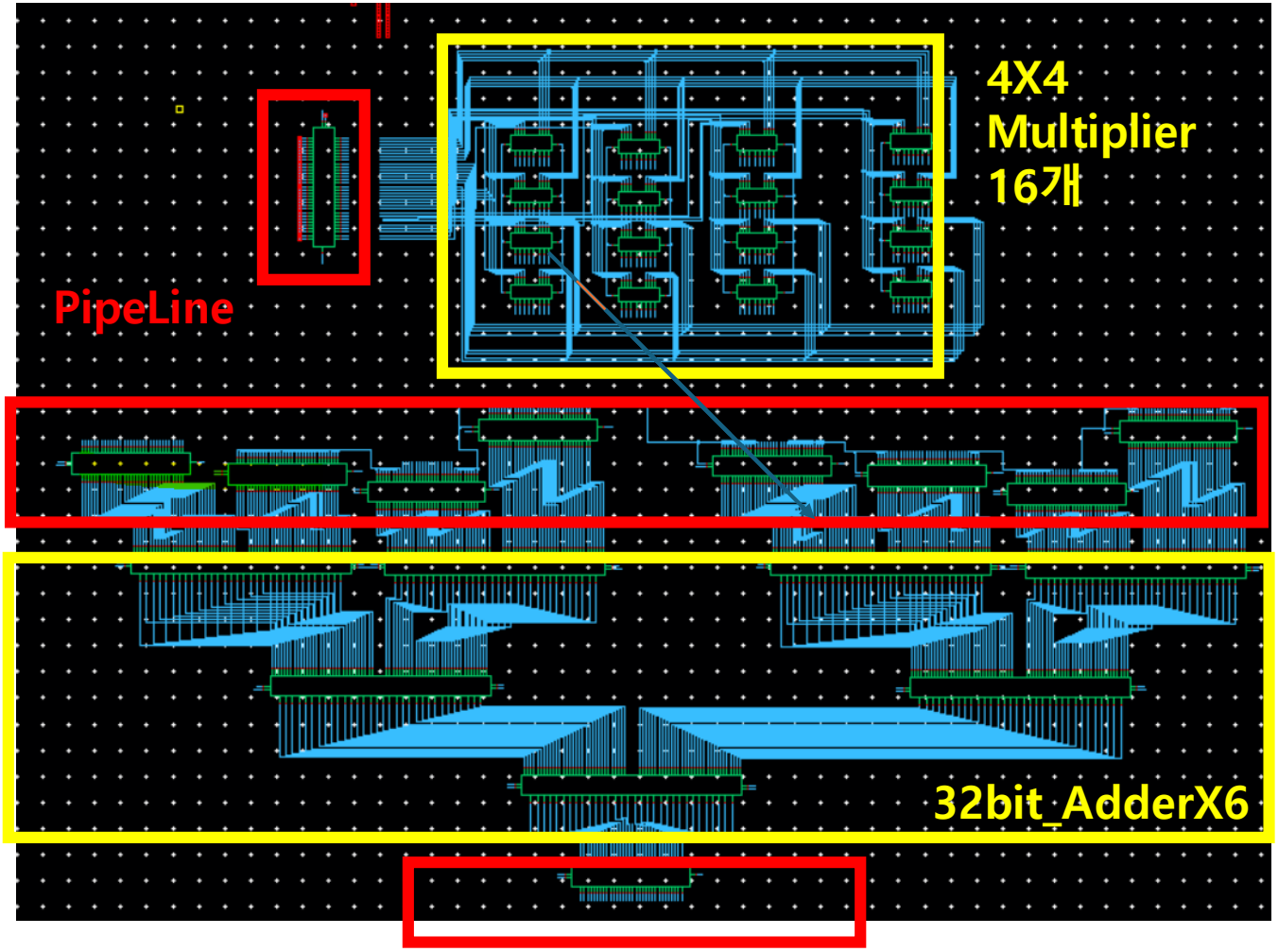


면적 :128.82 x 5.64 μ^2 (가로 x 세로)

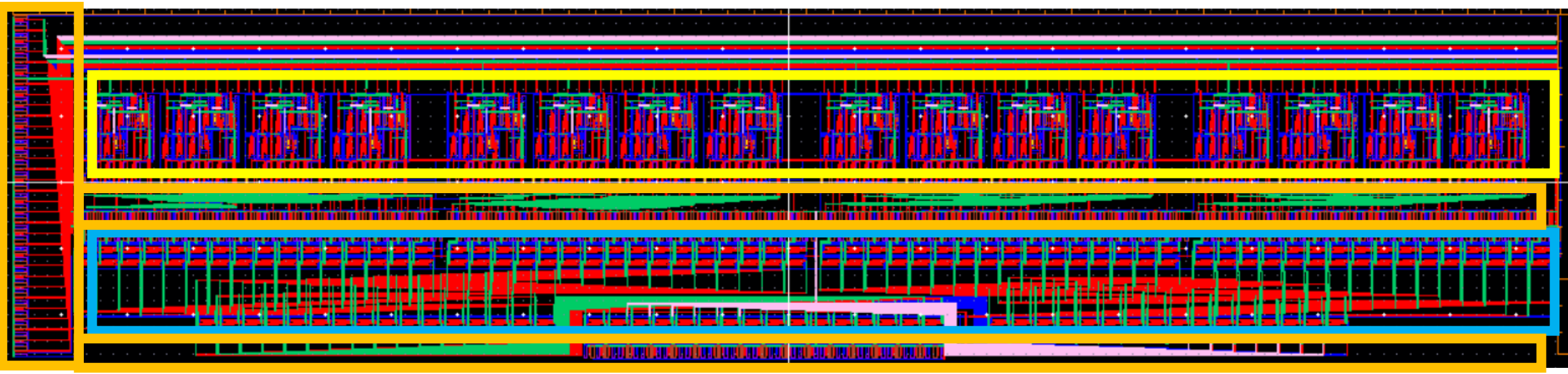
TSPC D-FF

- 고속 동작
- 낮은 전력 소모
- 작은 면적

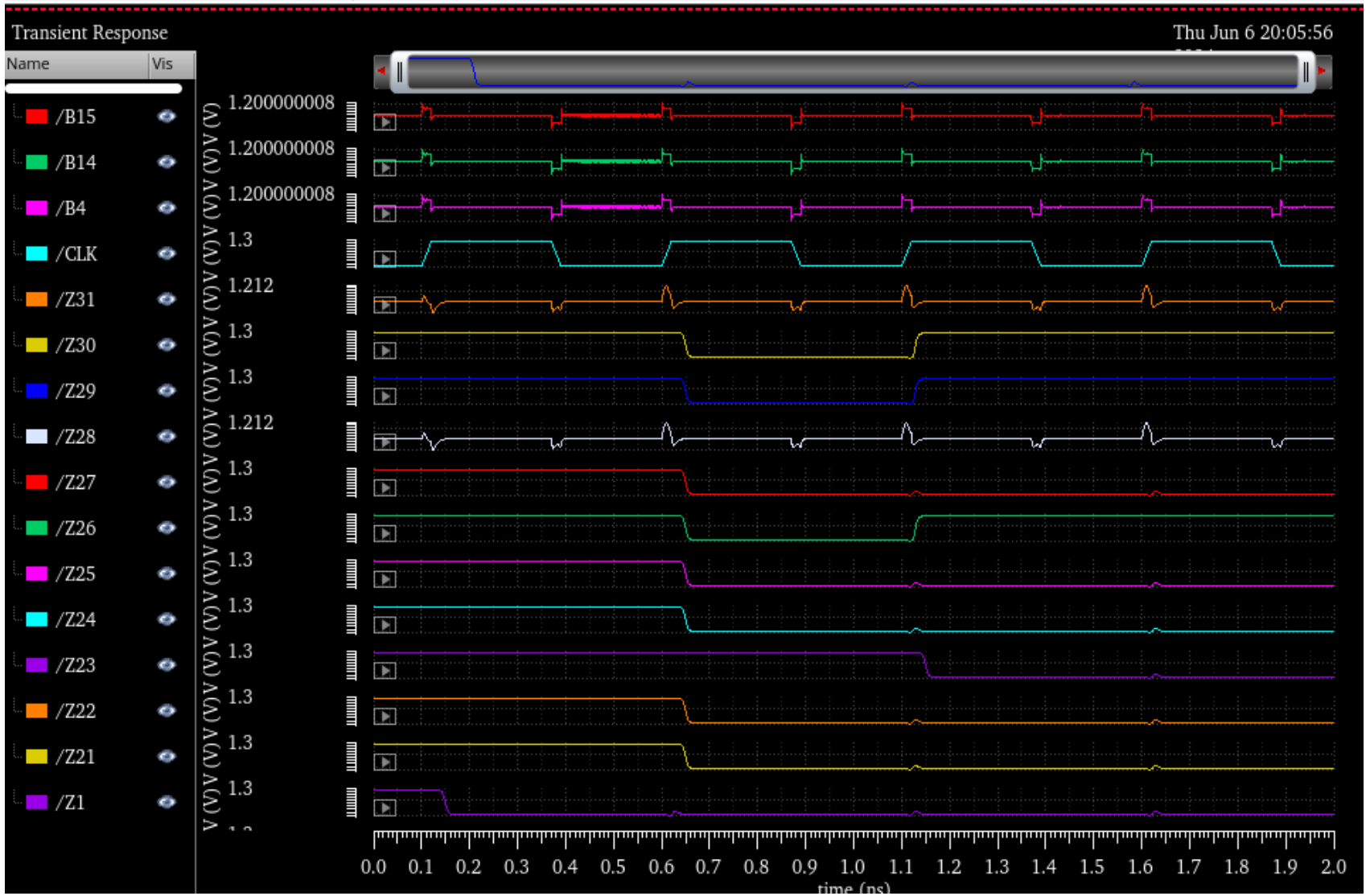
pipelining및 전체 구조설계 및 예측



LayOut



실제 시뮬레이션 값 성능


Transient Response
Thu Jun 6 20:05:56
Name
Vis
/B15
/B14
/B4
/CLK
/Z31
/Z30
/Z29
/Z28
/Z27
/Z26
/Z25
/Z24
/Z23
/Z22
/Z21
/Z1
1.200000008
1.200000008
1.200000008
1.3
1.212
1.3
1.3
1.212
1.3
1.3
1.3
1.3
1.3
1.3
1.3
1.3
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8 1.9 2.0
time (ns)

DRC,LVS 검증

감사합니다