Sitronix

ST7669

262K 132x162 Color Dot Matrix LCD Controller/Driver

1 INTRODUCTION

The ST7669 is a driver & controller LSI for 262K color graphic dot-matrix liquid crystal display systems. It generates 396 Segment and 162 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit/16-bit/18-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2 FEATURES

Driver Output Circuits

- 396 segment outputs / 162 common outputs

Applicable Duty Ratios

- Various partial display
- Partial window moving & data scrolling

Gray-Scale Display

- 4FRC & 31 PWM function circuit to display 64 gray-scale display
- Support 8 color mode (Idle mode)

On-chip Display Data RAM

- Capacity: 132 x 162 x 18 =384,912 bits

Color support by Inteface

- 256 color mode(RGB)=(332) mode (via LUT)
- 4K colors (RGB)=(444) mode (via LUT)
- 65K colors (RGB)=(565) mode
- 262K colors (RGB)=(666) mode
- Truncated 16M colors (RGB)=(888) mode

Microprocessor Interface

- 8/16/18-bit parallel bi-directional interface with 6800-series or 8080-series
- 3-line (9-bits) or 4-line(8-bit) serial interface

On-chip Low Power Analog Circuit

- On-chip oscillator circuit
- Voltage converter (x1, x2, x3, x4, x5, x6, x7, x8) with internal booster capacitors.
- Extremely Few Outsider Compoment. (Required outsider components: Three Capacitors)
- On-chip Voltage Regulator
- On-chip electronic contrast control function
- Voltage follower(LCD bias: 1/5,1/7,1/9,1/10,/11,1/12, 1/13, 1/14)

Operating Voltage Range

- Supply Digital Voltage (VDD): 1.65 to 3.0V
- Supply Analog Voltage (VDD2, VDD3, VDD4, VDD5): 2.4 to 3.3V
- LCD driving voltage (VOP = V0 - VSS): Max: 18V

LCD Driving Voltage (OTP)

- Contrast Adjustment Value is stored in the Built-In OTP-ROM for better display quility.

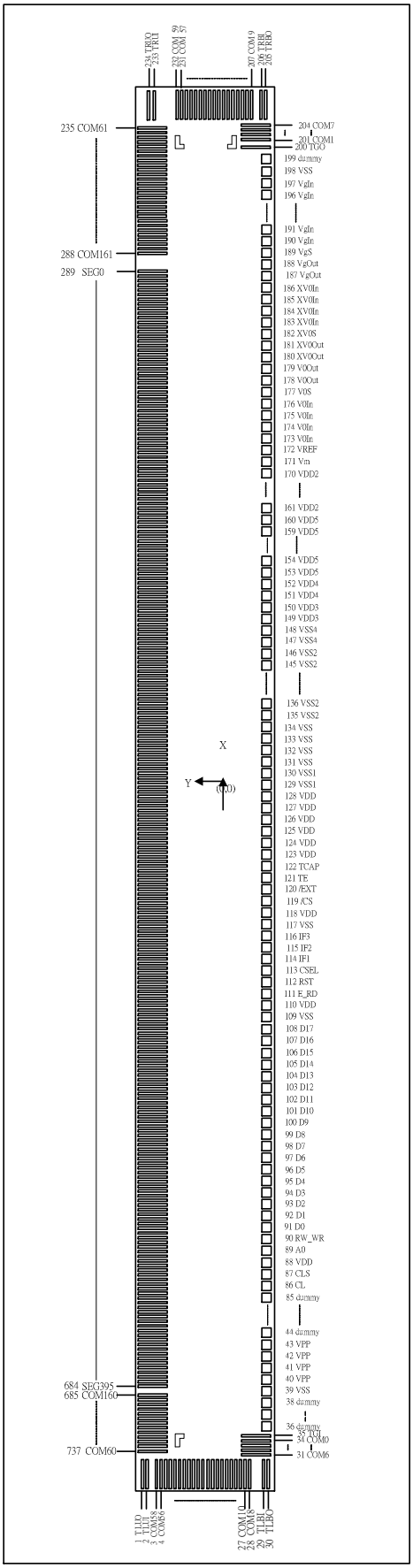
LCD Driving setting suggestion

- Vop=16.52, Bias=1/10

Package Type

- Application for COG

3 Pad Arrangement (COG)



Chip Size :

14030 um x 970 um

Bump Pitch :

PAD 1 ~ 30, 31 ~ 35 pitch=27um(min, com/seg)

PAD 200 ~ 204, 205 ~ 737 pitch=27um(min, com/seg)

PAD 36 ~ 199 pitch=80um (I/O)

PAD 87,88 pitch= 79.72um(I/O)

Bump Size :

PAD 1 ~ 35 , PAD 200 ~ 737

Bump width=14um(min, com/seg)

Bump space=13um(min, com/seg)

Bump length=128um(min, com/seg)

Bump area=1800um^2(com/seg)

PAD 36 ~86,89~199(except 87,88)

Bump width=65um(I/O)

Bump space=15um(I/O)

Bump length=63um(I/O)

Bump area=4095um^2

PAD 87,88

Bump width=65um(I/O)

Bump space=14.72um(I/O)

Bump length=63um(I/O)

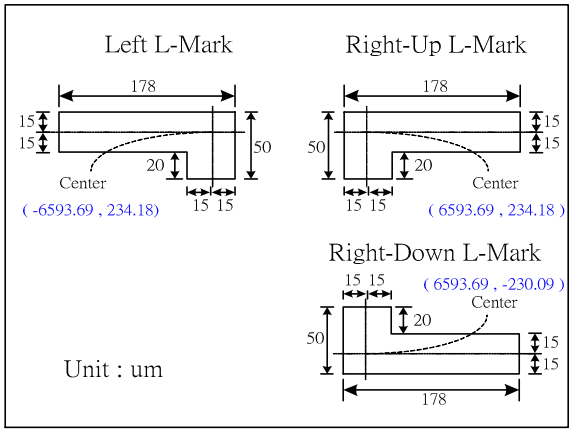
Bump area=4095um^2

Bump Height : 15 um

Chip Thickness : 400 um

Aligment mark

The center of alignment mark: see bellow Table



4 Pad Center Coordinates

PAD	NAME	X	Y
1	TLUO	-6897.71	421.50
2	TLUI	-6897.71	394.50
3	COM58	-6897.71	337.50
4	COM56	-6897.71	310.50
5	COM54	-6897.71	283.50
6	COM52	-6897.71	256.50
7	COM50	-6897.71	229.50
8	COM48	-6897.71	202.50
9	COM46	-6897.71	175.50
10	COM44	-6897.71	148.50
11	COM42	-6897.71	121.50
12	COM40	-6897.71	94.50
13	COM38	-6897.71	67.50
14	COM36	-6897.71	40.50
15	COM34	-6897.71	13.50
16	COM32	-6897.71	-13.50
17	COM30	-6897.71	-40.50
18	COM28	-6897.71	-67.50
19	COM26	-6897.71	-94.50
20	COM24	-6897.71	-121.50
21	COM22	-6897.71	-148.50
22	COM20	-6897.71	-175.50
23	COM18	-6897.71	-202.50
24	COM16	-6897.71	-229.50
25	COM14	-6897.71	-256.50
26	COM12	-6897.71	-283.50
27	COM10	-6897.71	-310.50
28	COM8	-6897.71	-337.50
29	TLBI	-6897.71	-394.50
30	TLBO	-6897.71	-421.50
31	COM6	-6749.45	-367.71
32	COM4	-6722.45	-367.71
33	COM2	-6695.45	-367.71
34	COM0	-6668.45	-367.71
35	TGI	-6608.30	-367.71
36	DUMMY	-6491.97	-394.50
37	DUMMY	-6411.97	-394.50
38	DUMMY	-6331.97	-394.50
39	VSS	-6251.97	-394.50
40	VPP	-6171.97	-394.50
41	VPP	-6091.97	-394.50
42	VPP	-6011.97	-394.50
43	VPP	-5931.97	-394.50
44	DUMMY	-5851.97	-394.50
45	DUMMY	-5771.97	-394.50
46	DUMMY	-5691.97	-394.50
47	DUMMY	-5611.97	-394.50
48	DUMMY	-5531.97	-394.50
49	DUMMY	-5451.97	-394.50
50	DUMMY	-5371.97	-394.50
51	DUMMY	-5291.97	-394.50
52	DUMMY	-5211.97	-394.50
53	DUMMY	-5131.97	-394.50
54	DUMMY	-5051.97	-394.50
55	DUMMY	-4971.97	-394.50
56	DUMMY	-4891.97	-394.50
57	DUMMY	-4811.97	-394.50
58	DUMMY	-4731.97	-394.50
59	DUMMY	-4651.97	-394.50
60	DUMMY	-4571.97	-394.50
61	DUMMY	-4491.97	-394.50
62	DUMMY	-4411.97	-394.50
63	DUMMY	-4331.97	-394.50
64	DUMMY	-4251.97	-394.50
65	DUMMY	-4171.97	-394.50
66	DUMMY	-4091.97	-394.50
67	DUMMY	-4011.97	-394.50
68	DUMMY	-3931.97	-394.50
69	DUMMY	-3851.97	-394.50

70	DUMMY	-3771.97	-394.50
71	DUMMY	-3691.97	-394.50
72	DUMMY	-3611.97	-394.50
73	DUMMY	-3531.97	-394.50
74	DUMMY	-3451.97	-394.50
75	DUMMY	-3371.97	-394.50
76	DUMMY	-3291.97	-394.50
77	DUMMY	-3211.97	-394.50
78	DUMMY	-3131.97	-394.50
79	DUMMY	-3051.97	-394.50
80	DUMMY	-2971.97	-394.50
81	DUMMY	-2891.97	-394.50
82	DUMMY	-2811.97	-394.50
83	DUMMY	-2731.97	-394.50
84	DUMMY	-2651.97	-394.50
85	DUMMY	-2571.97	-394.50
86	CL	-2491.97	-394.50
87	CLS	-2411.97	-394.50
88	VDD	-2332.25	-394.50
89	A0	-2252.25	-394.50
90	RW_WR	-2172.25	-394.50
91	D0	-2092.25	-394.50
92	D1	-2012.25	-394.50
93	D2	-1932.25	-394.50
94	D3	-1852.25	-394.50
95	D4	-1772.25	-394.50
96	D5	-1692.25	-394.50
97	D6	-1612.25	-394.50
98	D7	-1532.25	-394.50
99	D8	-1452.25	-394.50
100	D9	-1372.25	-394.50
101	D10	-1292.25	-394.50
102	D11	-1212.25	-394.50
103	D12	-1132.25	-394.50
104	D13	-1052.25	-394.50

105	D14	-972.25	-394.50
106	D15	-892.25	-394.50
107	D16	-812.25	-394.50
108	D17	-732.25	-394.50
109	VSS	-652.25	-394.50
110	VDD	-572.25	-394.50
111	E_RD	-492.25	-394.50
112	/RST	-412.25	-394.50
113	CSEL	-332.25	-394.50
114	IF1	-252.25	-394.50
115	IF2	-172.25	-394.50
116	IF3	-92.25	-394.50
117	VSS	-12.25	-394.50
118	VDD	67.75	-394.50
119	/CS	147.75	-394.50
120	/EXT	227.75	-394.50
121	TE	307.75	-394.50
122	TCAP	387.75	-394.50
123	VDD	467.75	-394.50
124	VDD	547.75	-394.50
125	VDD	627.75	-394.50
126	VDD	707.75	-394.50
127	VDD	787.75	-394.50
128	VDD	867.75	-394.50
129	VSS1	947.75	-394.50
130	VSS1	1027.75	-394.50
131	VSS	1107.75	-394.50
132	VSS	1187.75	-394.50
133	VSS	1267.75	-394.50
134	VSS	1347.75	-394.50
135	VSS2	1427.75	-394.50
136	VSS2	1507.75	-394.50
137	VSS2	1587.75	-394.50
138	VSS2	1667.75	-394.50
139	VSS2	1747.75	-394.50

140	VSS2	1827.75	-394.50
141	VSS2	1907.75	-394.50
142	VSS2	1987.75	-394.50
143	VSS2	2067.75	-394.50
144	VSS2	2147.75	-394.50
145	VSS2	2227.75	-394.50
146	VSS2	2307.75	-394.50
147	VSS4	2387.75	-394.50
148	VSS4	2467.75	-394.50
149	VDD3	2547.75	-394.50
150	VDD3	2627.75	-394.50
151	VDD4	2707.75	-394.50
152	VDD4	2787.75	-394.50
153	VDD5	2867.75	-394.50
154	VDD5	2947.75	-394.50
155	VDD5	3027.75	-394.50
156	VDD5	3107.75	-394.50
157	VDD5	3187.75	-394.50
158	VDD5	3267.75	-394.50
159	VDD5	3347.75	-394.50
160	VDD5	3427.75	-394.50
161	VDD2	3507.75	-394.50
162	VDD2	3587.75	-394.50
163	VDD2	3667.75	-394.50
164	VDD2	3747.75	-394.50
165	VDD2	3827.75	-394.50
166	VDD2	3907.75	-394.50
167	VDD2	3987.75	-394.50
168	VDD2	4067.75	-394.50
169	VDD2	4147.75	-394.50
170	VDD2	4227.75	-394.50
171	Vm	4307.75	-394.50
172	VREF	4387.75	-394.50
173	V0in	4467.75	-394.50
174	V0in	4547.75	-394.50
175	V0in	4627.75	-394.50
176	V0in	4707.75	-394.50
177	V0s	4787.75	-394.50
178	V0out	4867.75	-394.50
179	V0out	4947.75	-394.50
180	XV0out	5027.75	-394.50
181	XV0out	5107.75	-394.50
182	XV0s	5187.75	-394.50
183	XV0in	5267.75	-394.50
184	XV0in	5347.75	-394.50
185	XV0in	5427.75	-394.50
186	XV0in	5507.75	-394.50
187	Vgout	5587.75	-394.50
188	Vgout	5667.75	-394.50
189	Vgs	5747.75	-394.50
190	Vgin	5827.75	-394.50
191	Vgin	5907.75	-394.50
192	Vgin	5987.75	-394.50
193	Vgin	6067.75	-394.50
194	Vgin	6147.75	-394.50
195	Vgin	6227.75	-394.50
196	Vgin	6307.75	-394.50
197	Vgin	6387.75	-394.50
198	VSS	6467.75	-394.50
199	DUMMY	6547.75	-394.50
200	TGO	6608.30	-367.71
201	COM1	6668.45	-367.71
202	COM3	6695.45	-367.71
203	COM5	6722.45	-367.71
204	COM7	6749.45	-367.71
205	TRBO	6897.71	-421.50
206	TRBI	6897.71	-394.50
207	COM9	6897.71	-337.50
208	COM11	6897.71	-310.50
209	COM13	6897.71	-283.50

210	COM15	6897.71	-256.50
211	COM17	6897.71	-229.50
212	COM19	6897.71	-202.50
213	COM21	6897.71	-175.50
214	COM23	6897.71	-148.50
215	COM25	6897.71	-121.50
216	COM27	6897.71	-94.50
217	COM29	6897.71	-67.50
218	COM31	6897.71	-40.50
219	COM33	6897.71	-13.50
220	COM35	6897.71	13.50
221	COM37	6897.71	40.50
222	COM39	6897.71	67.50
223	COM41	6897.71	94.50
224	COM43	6897.71	121.50
225	COM45	6897.71	148.50
226	COM47	6897.71	175.50
227	COM49	6897.71	202.50
228	COM51	6897.71	229.50
229	COM53	6897.71	256.50
230	COM55	6897.71	283.50
231	COM57	6897.71	310.50
232	COM59	6897.71	337.50
233	TRUI	6897.71	394.50
234	TRUO	6897.71	421.50
235	COM61	6743.18	367.71
236	COM63	6716.18	367.71
237	COM65	6689.18	367.71
238	COM67	6662.18	367.71
239	COM69	6635.18	367.71
240	L-Mark	6593.69	234.18
241	COM71	6608.18	367.71
242	L-Mark	6593.69	234.18
243	L-Mark	6593.69	234.18
244	COM73	6581.18	367.71
245	COM75	6554.18	367.71
246	COM77	6527.18	367.71
247	COM79	6500.18	367.71
248	COM81	6473.18	367.71
249	COM83	6446.18	367.71
250	COM85	6419.18	367.71
251	COM87	6392.18	367.71
252	COM89	6365.18	367.71
253	COM91	6338.18	367.71
254	COM93	6311.18	367.71
255	COM95	6284.18	367.71
256	COM97	6257.18	367.71
257	COM99	6230.18	367.71
258	COM101	6203.18	367.71
259	COM103	6176.18	367.71
260	COM105	6149.18	367.71
261	COM107	6122.18	367.71
262	COM109	6095.18	367.71
263	COM111	6068.18	367.71
264	COM113	6041.18	367.71
265	COM115	6014.18	367.71
266	COM117	5987.18	367.71
267	COM119	5960.18	367.71
268	COM121	5933.18	367.71
269	COM123	5906.18	367.71
270	COM125	5879.18	367.71
271	COM127	5852.18	367.71
272	COM129	5825.18	367.71
273	COM131	5798.18	367.71
274	COM133	5771.18	367.71
275	COM135	5744.18	367.71
276	COM137	5717.18	367.71
277	COM139	5690.18	367.71
278	COM141	5663.18	367.71
279	COM143	5636.18	367.71

280	COM145	5609.18	367.71
281	COM147	5582.18	367.71
282	COM149	5555.18	367.71
283	COM151	5528.18	367.71
284	COM153	5501.18	367.71
285	COM155	5474.18	367.71
286	COM157	5447.18	367.71
287	COM159	5420.18	367.71
288	COM161	5393.18	367.71
289	SEG0	5332.50	367.71
290	SEG1	5305.50	367.71
291	SEG2	5278.50	367.71
292	SEG3	5251.50	367.71
293	SEG4	5224.50	367.71
294	SEG5	5197.50	367.71
295	SEG6	5170.50	367.71
296	SEG7	5143.50	367.71
297	SEG8	5116.50	367.71
298	SEG9	5089.50	367.71
299	SEG10	5062.50	367.71
300	SEG11	5035.50	367.71
301	SEG12	5008.50	367.71
302	SEG13	4981.50	367.71
303	SEG14	4954.50	367.71
304	SEG15	4927.50	367.71
305	SEG16	4900.50	367.71
306	SEG17	4873.50	367.71
307	SEG18	4846.50	367.71
308	SEG19	4819.50	367.71
309	SEG20	4792.50	367.71
310	SEG21	4765.50	367.71
311	SEG22	4738.50	367.71
312	SEG23	4711.50	367.71
313	SEG24	4684.50	367.71
314	SEG25	4657.50	367.71

315	SEG26	4630.50	367.71
316	SEG27	4603.50	367.71
317	SEG28	4576.50	367.71
318	SEG29	4549.50	367.71
319	SEG30	4522.50	367.71
320	SEG31	4495.50	367.71
321	SEG32	4468.50	367.71
322	SEG33	4441.50	367.71
323	SEG34	4414.50	367.71
324	SEG35	4387.50	367.71
325	SEG36	4360.50	367.71
326	SEG37	4333.50	367.71
327	SEG38	4306.50	367.71
328	SEG39	4279.50	367.71
329	SEG40	4252.50	367.71
330	SEG41	4225.50	367.71
331	SEG42	4198.50	367.71
332	SEG43	4171.50	367.71
333	SEG44	4144.50	367.71
334	SEG45	4117.50	367.71
335	SEG46	4090.50	367.71
336	SEG47	4063.50	367.71
337	SEG48	4036.50	367.71
338	SEG49	4009.50	367.71
339	SEG50	3982.50	367.71
340	SEG51	3955.50	367.71
341	SEG52	3928.50	367.71
342	SEG53	3901.50	367.71
343	SEG54	3874.50	367.71
344	SEG55	3847.50	367.71
345	SEG56	3820.50	367.71
346	SEG57	3793.50	367.71
347	SEG58	3766.50	367.71
348	SEG59	3739.50	367.71
349	SEG60	3712.50	367.71

350	SEG61	3685.50	367.71
351	SEG62	3658.50	367.71
352	SEG63	3631.50	367.71
353	SEG64	3604.50	367.71
354	SEG65	3577.50	367.71
355	SEG66	3550.50	367.71
356	SEG67	3523.50	367.71
357	SEG68	3496.50	367.71
358	SEG69	3469.50	367.71
359	SEG70	3442.50	367.71
360	SEG71	3415.50	367.71
361	SEG72	3388.50	367.71
362	SEG73	3361.50	367.71
363	SEG74	3334.50	367.71
364	SEG75	3307.50	367.71
365	SEG76	3280.50	367.71
366	SEG77	3253.50	367.71
367	SEG78	3226.50	367.71
368	SEG79	3199.50	367.71
369	SEG80	3172.50	367.71
370	SEG81	3145.50	367.71
371	SEG82	3118.50	367.71
372	SEG83	3091.50	367.71
373	SEG84	3064.50	367.71
374	SEG85	3037.50	367.71
375	SEG86	3010.50	367.71
376	SEG87	2983.50	367.71
377	SEG88	2956.50	367.71
378	SEG89	2929.50	367.71
379	SEG90	2902.50	367.71
380	SEG91	2875.50	367.71
381	SEG92	2848.50	367.71
382	SEG93	2821.50	367.71
383	SEG94	2794.50	367.71
384	SEG95	2767.50	367.71

385	SEG96	2740.50	367.71
386	SEG97	2713.50	367.71
387	SEG98	2686.50	367.71
388	SEG99	2659.50	367.71
389	SEG100	2632.50	367.71
390	SEG101	2605.50	367.71
391	SEG102	2578.50	367.71
392	SEG103	2551.50	367.71
393	SEG104	2524.50	367.71
394	SEG105	2497.50	367.71
395	SEG106	2470.50	367.71
396	SEG107	2443.50	367.71
397	SEG108	2416.50	367.71
398	SEG109	2389.50	367.71
399	SEG110	2362.50	367.71
400	SEG111	2335.50	367.71
401	SEG112	2308.50	367.71
402	SEG113	2281.50	367.71
403	SEG114	2254.50	367.71
404	SEG115	2227.50	367.71
405	SEG116	2200.50	367.71
406	SEG117	2173.50	367.71
407	SEG118	2146.50	367.71
408	SEG119	2119.50	367.71
409	SEG120	2092.50	367.71
410	SEG121	2065.50	367.71
411	SEG122	2038.50	367.71
412	SEG123	2011.50	367.71
413	SEG124	1984.50	367.71
414	SEG125	1957.50	367.71
415	SEG126	1930.50	367.71
416	SEG127	1903.50	367.71
417	SEG128	1876.50	367.71
418	SEG129	1849.50	367.71
419	SEG130	1822.50	367.71

420	SEG131	1795.50	367.71
421	SEG132	1768.50	367.71
422	SEG133	1741.50	367.71
423	SEG134	1714.50	367.71
424	SEG135	1687.50	367.71
425	SEG136	1660.50	367.71
426	SEG137	1633.50	367.71
427	SEG138	1606.50	367.71
428	SEG139	1579.50	367.71
429	SEG140	1552.50	367.71
430	SEG141	1525.50	367.71
431	SEG142	1498.50	367.71
432	SEG143	1471.50	367.71
433	SEG144	1444.50	367.71
434	SEG145	1417.50	367.71
435	SEG146	1390.50	367.71
436	SEG147	1363.50	367.71
437	SEG148	1336.50	367.71
438	SEG149	1309.50	367.71
439	SEG150	1282.50	367.71
440	SEG151	1255.50	367.71
441	SEG152	1228.50	367.71
442	SEG153	1201.50	367.71
443	SEG154	1174.50	367.71
444	SEG155	1147.50	367.71
445	SEG156	1120.50	367.71
446	SEG157	1093.50	367.71
447	SEG158	1066.50	367.71
448	SEG159	1039.50	367.71
449	SEG160	1012.50	367.71
450	SEG161	985.50	367.71
451	SEG162	958.50	367.71
452	SEG163	931.50	367.71
453	SEG164	904.50	367.71
454	SEG165	877.50	367.71
455	SEG166	850.50	367.71
456	SEG167	823.50	367.71
457	SEG168	796.50	367.71
458	SEG169	769.50	367.71
459	SEG170	742.50	367.71
460	SEG171	715.50	367.71
461	SEG172	688.50	367.71
462	SEG173	661.50	367.71
463	SEG174	634.50	367.71
464	SEG175	607.50	367.71
465	SEG176	580.50	367.71
466	SEG177	553.50	367.71
467	SEG178	526.50	367.71
468	SEG179	499.50	367.71
469	SEG180	472.50	367.71
470	SEG181	445.50	367.71
471	SEG182	418.50	367.71
472	SEG183	391.50	367.71
473	SEG184	364.50	367.71
474	SEG185	337.50	367.71
475	SEG186	310.50	367.71
476	SEG187	283.50	367.71
477	SEG188	256.50	367.71
478	SEG189	229.50	367.71
479	SEG190	202.50	367.71
480	SEG191	175.50	367.71
481	SEG192	148.50	367.71
482	SEG193	121.50	367.71
483	SEG194	94.50	367.71
484	SEG195	67.50	367.71
485	SEG196	40.50	367.71
486	SEG197	13.50	367.71
487	SEG198	-13.50	367.71
488	SEG199	-40.50	367.71
489	SEG200	-67.50	367.71

490	SEG201	-94.50	367.71
491	SEG202	-121.50	367.71
492	SEG203	-148.50	367.71
493	SEG204	-175.50	367.71
494	SEG205	-202.50	367.71
495	SEG206	-229.50	367.71
496	SEG207	-256.50	367.71
497	SEG208	-283.50	367.71
498	SEG209	-310.50	367.71
499	SEG210	-337.50	367.71
500	SEG211	-364.50	367.71
501	SEG212	-391.50	367.71
502	SEG213	-418.50	367.71
503	SEG214	-445.50	367.71
504	SEG215	-472.50	367.71
505	SEG216	-499.50	367.71
506	SEG217	-526.50	367.71
507	SEG218	-553.50	367.71
508	SEG219	-580.50	367.71
509	SEG220	-607.50	367.71
510	SEG221	-634.50	367.71
511	SEG222	-661.50	367.71
512	SEG223	-688.50	367.71
513	SEG224	-715.50	367.71
514	SEG225	-742.50	367.71
515	SEG226	-769.50	367.71
516	SEG227	-796.50	367.71
517	SEG228	-823.50	367.71
518	SEG229	-850.50	367.71
519	SEG230	-877.50	367.71
520	SEG231	-904.50	367.71
521	SEG232	-931.50	367.71
522	SEG233	-958.50	367.71
523	SEG234	-985.50	367.71
524	SEG235	-1012.50	367.71
525	SEG236	-1039.50	367.71
526	SEG237	-1066.50	367.71
527	SEG238	-1093.50	367.71
528	SEG239	-1120.50	367.71
529	SEG240	-1147.50	367.71
530	SEG241	-1174.50	367.71
531	SEG242	-1201.50	367.71
532	SEG243	-1228.50	367.71
533	SEG244	-1255.50	367.71
534	SEG245	-1282.50	367.71
535	SEG246	-1309.50	367.71
536	SEG247	-1336.50	367.71
537	SEG248	-1363.50	367.71
538	SEG249	-1390.50	367.71
539	SEG250	-1417.50	367.71
540	SEG251	-1444.50	367.71
541	SEG252	-1471.50	367.71
542	SEG253	-1498.50	367.71
543	SEG254	-1525.50	367.71
544	SEG255	-1552.50	367.71
545	SEG256	-1579.50	367.71
546	SEG257	-1606.50	367.71
547	SEG258	-1633.50	367.71
548	SEG259	-1660.50	367.71
549	SEG260	-1687.50	367.71
550	SEG261	-1714.50	367.71
551	SEG262	-1741.50	367.71
552	SEG263	-1768.50	367.71
553	SEG264	-1795.50	367.71
554	SEG265	-1822.50	367.71
555	SEG266	-1849.50	367.71
556	SEG267	-1876.50	367.71
557	SEG268	-1903.50	367.71
558	SEG269	-1930.50	367.71
559	SEG270	-1957.50	367.71

560	SEG271	-1984.50	367.71
561	SEG272	-2011.50	367.71
562	SEG273	-2038.50	367.71
563	SEG274	-2065.50	367.71
564	SEG275	-2092.50	367.71
565	SEG276	-2119.50	367.71
566	SEG277	-2146.50	367.71
567	SEG278	-2173.50	367.71
568	SEG279	-2200.50	367.71
569	SEG280	-2227.50	367.71
570	SEG281	-2254.50	367.71
571	SEG282	-2281.50	367.71
572	SEG283	-2308.50	367.71
573	SEG284	-2335.50	367.71
574	SEG285	-2362.50	367.71
575	SEG286	-2389.50	367.71
576	SEG287	-2416.50	367.71
577	SEG288	-2443.50	367.71
578	SEG289	-2470.50	367.71
579	SEG290	-2497.50	367.71
580	SEG291	-2524.50	367.71
581	SEG292	-2551.50	367.71
582	SEG293	-2578.50	367.71
583	SEG294	-2605.50	367.71
584	SEG295	-2632.50	367.71
585	SEG296	-2659.50	367.71
586	SEG297	-2686.50	367.71
587	SEG298	-2713.50	367.71
588	SEG299	-2740.50	367.71
589	SEG300	-2767.50	367.71
590	SEG301	-2794.50	367.71
591	SEG302	-2821.50	367.71
592	SEG303	-2848.50	367.71
593	SEG304	-2875.50	367.71
594	SEG305	-2902.50	367.71

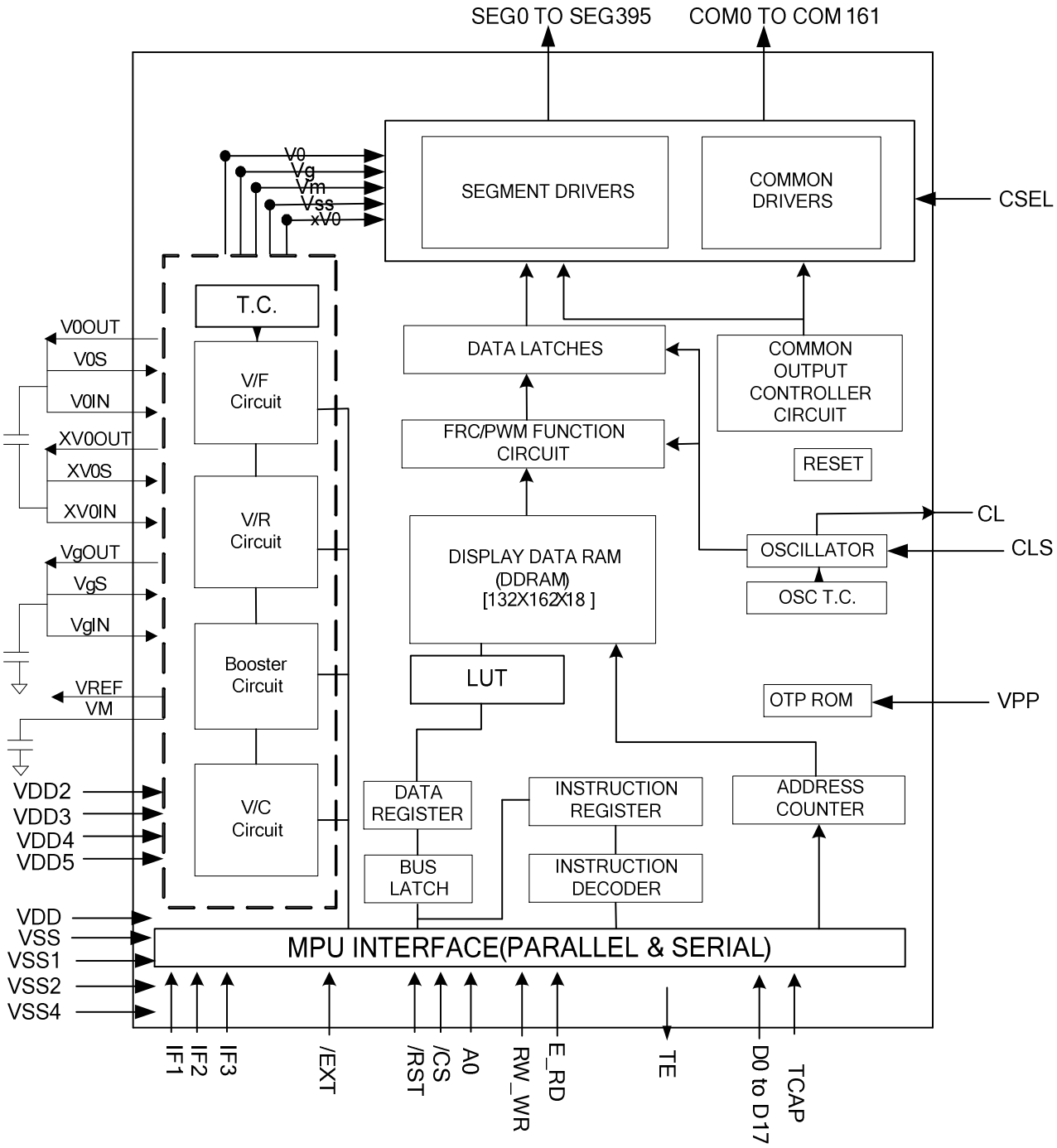
595	SEG306	-2929.50	367.71
596	SEG307	-2956.50	367.71
597	SEG308	-2983.50	367.71
598	SEG309	-3010.50	367.71
599	SEG310	-3037.50	367.71
600	SEG311	-3064.50	367.71
601	SEG312	-3091.50	367.71
602	SEG313	-3118.50	367.71
603	SEG314	-3145.50	367.71
604	SEG315	-3172.50	367.71
605	SEG316	-3199.50	367.71
606	SEG317	-3226.50	367.71
607	SEG318	-3253.50	367.71
608	SEG319	-3280.50	367.71
609	SEG320	-3307.50	367.71
610	SEG321	-3334.50	367.71
611	SEG322	-3361.50	367.71
612	SEG323	-3388.50	367.71
613	SEG324	-3415.50	367.71
614	SEG325	-3442.50	367.71
615	SEG326	-3469.50	367.71
616	SEG327	-3496.50	367.71
617	SEG328	-3523.50	367.71
618	SEG329	-3550.50	367.71
619	SEG330	-3577.50	367.71
620	SEG331	-3604.50	367.71
621	SEG332	-3631.50	367.71
622	SEG333	-3658.50	367.71
623	SEG334	-3685.50	367.71
624	SEG335	-3712.50	367.71
625	SEG336	-3739.50	367.71
626	SEG337	-3766.50	367.71
627	SEG338	-3793.50	367.71
628	SEG339	-3820.50	367.71
629	SEG340	-3847.50	367.71

630	SEG341	-3874.50	367.71
631	SEG342	-3901.50	367.71
632	SEG343	-3928.50	367.71
633	SEG344	-3955.50	367.71
634	SEG345	-3982.50	367.71
635	SEG346	-4009.50	367.71
636	SEG347	-4036.50	367.71
637	SEG348	-4063.50	367.71
638	SEG349	-4090.50	367.71
639	SEG350	-4117.50	367.71
640	SEG351	-4144.50	367.71
641	SEG352	-4171.50	367.71
642	SEG353	-4198.50	367.71
643	SEG354	-4225.50	367.71
644	SEG355	-4252.50	367.71
645	SEG356	-4279.50	367.71
646	SEG357	-4306.50	367.71
647	SEG358	-4333.50	367.71
648	SEG359	-4360.50	367.71
649	SEG360	-4387.50	367.71
650	SEG361	-4414.50	367.71
651	SEG362	-4441.50	367.71
652	SEG363	-4468.50	367.71
653	SEG364	-4495.50	367.71
654	SEG365	-4522.50	367.71
655	SEG366	-4549.50	367.71
656	SEG367	-4576.50	367.71
657	SEG368	-4603.50	367.71
658	SEG369	-4630.50	367.71
659	SEG370	-4657.50	367.71
660	SEG371	-4684.50	367.71
661	SEG372	-4711.50	367.71
662	SEG373	-4738.50	367.71
663	SEG374	-4765.50	367.71
664	SEG375	-4792.50	367.71

665	SEG376	-4819.50	367.71
666	SEG377	-4846.50	367.71
667	SEG378	-4873.50	367.71
668	SEG379	-4900.50	367.71
669	SEG380	-4927.50	367.71
670	SEG381	-4954.50	367.71
671	SEG382	-4981.50	367.71
672	SEG383	-5008.50	367.71
673	SEG384	-5035.50	367.71
674	SEG385	-5062.50	367.71
675	SEG386	-5089.50	367.71
676	SEG387	-5116.50	367.71
677	SEG388	-5143.50	367.71
678	SEG389	-5170.50	367.71
679	SEG390	-5197.50	367.71
680	SEG391	-5224.50	367.71
681	SEG392	-5251.50	367.71
682	SEG393	-5278.50	367.71
683	SEG394	-5305.50	367.71
684	SEG395	-5332.50	367.71
685	COM160	-5393.18	367.71
686	COM158	-5420.18	367.71
687	COM156	-5447.18	367.71
688	COM154	-5474.18	367.71
689	COM152	-5501.18	367.71
690	COM150	-5528.18	367.71
691	COM148	-5555.18	367.71
692	COM146	-5582.18	367.71
693	COM144	-5609.18	367.71
694	COM142	-5636.18	367.71
695	COM140	-5663.18	367.71
696	COM138	-5690.18	367.71
697	COM136	-5717.18	367.71
698	COM134	-5744.18	367.71
699	COM132	-5771.18	367.71

700	COM130	-5798.18	367.71
701	COM128	-5825.18	367.71
702	COM126	-5852.18	367.71
703	COM124	-5879.18	367.71
704	COM122	-5906.18	367.71
705	COM120	-5933.18	367.71
706	COM118	-5960.18	367.71
707	COM116	-5987.18	367.71
708	COM114	-6014.18	367.71
709	COM112	-6041.18	367.71
710	COM110	-6068.18	367.71
711	COM108	-6095.18	367.71
712	COM106	-6122.18	367.71
713	COM104	-6149.18	367.71
714	COM102	-6176.18	367.71
715	COM100	-6203.18	367.71
716	COM98	-6230.18	367.71
717	COM96	-6257.18	367.71
718	COM94	-6284.18	367.71
719	COM92	-6311.18	367.71
720	COM90	-6338.18	367.71
721	COM88	-6365.18	367.71
722	COM86	-6392.18	367.71
723	COM84	-6419.18	367.71
724	COM82	-6446.18	367.71
725	COM80	-6473.18	367.71
726	COM78	-6500.18	367.71
727	COM76	-6527.18	367.71
728	COM74	-6554.18	367.71
729	COM72	-6581.18	367.71
730	L-Mark	-6593.69	234.18
731	L-Mark	-6593.69	234.18
732	COM70	-6608.18	367.71
733	COM68	-6635.18	367.71
734	COM66	-6662.18	367.71
735	COM64	-6689.18	367.71
736	COM62	-6716.18	367.71
737	COM60	-6743.18	367.71
738	L-Mark	6593.69	-230.09

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1 Power Supply

Name	I/O	Description
VDD	Supply	Power supply for logic circuit (Digital VDD 1.65V~3.0V)
VDD2	Supply	Power supply for Booster Circuit (Analog VDD 2.4V~3.3V)
VDD3	Supply	Power supply for LCD. (Analog VDD 2.4V~3.3V)
VDD4	Supply	Power supply for LCD. (Analog VDD 2.4V~3.3V)
VDD5	Supply	Power supply for LCD. (Analog VDD 2.4V~3.3V)
VSS	Supply	Ground for logic circuit. Ground system should be connected together.
VSS1	Supply	Ground for OSC circuit. Ground system should be connected together.
VSS2	Supply	Ground for Booster Circuit. Ground system should be connected together.
VSS4	Supply	Ground for LCD. Ground system should be connected together.

6.2 LCD Power Supply Pins

Name	I/O	Description
$V0_{OUT}$ $V0_{IN}$ $V0_S$	I/O	Positive LCD driver supply voltages. $V0_{OUT}$ is the output voltage of V0 generated by ST7669. $V0_{IN}$ is the input pin of power supply to generate V0 voltage for LCD. $V0_S$ is the input pin of power supply to sense the V0 voltage. $V0_{OUT}$ 、$V0_{IN}$ & $V0_S$ should be connected together in FPC.
$XV0_{OUT}$ $XV0_{IN}$ $XV0_S$	I/O	Negative LCD driver supply voltages. $XV0_{OUT}$ is the output voltage of XV0 generated by ST7669. $XV0_{IN}$ is the input pin of power supply to generate XV0 voltage for LCD. $XV0_S$ is the input pin of power supply to sense the XV0 voltage. $XV0_{OUT}$ 、$XV0_{IN}$ & $XV0_S$ should be connected together in FPC.
Vg_{OUT} Vg_{IN} Vg_S Vm	I/O	Bias LCD driver supply voltages. VgOUT is the output voltage of Vg generated by ST7669. VgIN is the input pin of power supply to generate Vg voltage for LCD. VgS is the input pin of power supply to sense the Vg voltage. VgOUT 、VgIN & VgS should be connected together in FPC. Vm is the I/O pin of LCD bias supply voltage Voltages should have the following relationship: $V0 \geqq Vg \geqq Vm \geqq VSS \geqq XV0$ and VDDA-0.7V>Vm>0.7V, 2xVDDA$\geqq$Vg>1.8V When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.

LCD bias	Vg	Vm
1/N bias	(2/N) x V0	(1/N) x V0

NOTE: N = 5,7,9,10,11,12,13 and 14

6.3 System Control

Name	I/O	Description
CLS	I	When using internal clock oscillator, connect CLS to VDD. When using external clock oscillator, connect CLS to VSS.
CL	I/O	When using external clock oscillator, it's clock input.
CSEL	I	This pin should connect to VDD.
TCAP	I/O	Test pin. Left it opens.
VREF	O	Reference voltage output for monitor only. Left it opened.
VPP	I	When writing OTP, it needs outer power supply voltage 7.50~7.75V(>4mA) input to write successfully.

6.4 Microprocessor Interface

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>/RST</td><td>I</td><td>Reset input pin
When /RST is “L”, initialization is executed.</td></tr>
<tr><td>IF[3:1]</td><td>I</td><td>Parallel / Serial data input select input
<table>
<tr><th>IF3</th><th>IF2</th><th>IF1</th><th>MPU interface type</th><th>MPU interface type</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>80 series 16-bit parallel</td><td>80 series 16-bit parallel</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>80 series 8-bit parallel</td><td>80 series 8-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>68 series 16-bit parallel</td><td>68 series 16-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>68 series 8-bit parallel</td><td>68 series 8-bit parallel</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>8-bit serial (4 line)</td><td>8-bit serial (4 line)</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>9-bit serial (3 line)</td><td>9-bit serial (3 line)</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>80 series 18-bit parallel</td><td>80 series 18-bit parallel</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>68 series 18-bit parallel</td><td>68 series 18-bit parallel</td></tr>
</table>
Note:
1. When fixing IF2=H & IF1=L, IF3 can be defined as P/SX pin (parallel/Serial selection pin).IF3=H: Parallel interface (80 8-bit); IF3=L: Serial interface (3-line)
2. Refer to Table 7.1-1. for detail interface connecton.</td></tr>
<tr><td>/CS</td><td>I</td><td>Chip select input pins
Data / Instruction I/O is enabled only when /CS is "L". When chip select is non-active, D0 to D17 become high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin
A0 = "H": D0 to D17 or SI are display data
A0 = "L": D0 to D17 or SI are control data
** In 3-line/4-line interface this pad will be used for SCL function</td></tr>
</table>

<table>
<tr><td>RW_WR</td><td>I</td><td>Read / Write execution control pin. (This pin is only used in parallel interface)
<table><tr><th>MPU type</th><th>RW_WR</th><th>Description</th></tr><tr><td>6800-series</td><td>RW</td><td>Read / Write control input pin
RW = “H” : read
RW = “L” : write</td></tr><tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on D0 to D17 are latched at the rising edge of the /WR signal.</td></tr></table>When in the serial interface, connect it to VDD.</td></tr>
<tr><td>E_RD</td><td>I</td><td>Read / Write execution control pin. (This pin is only used in parallel interface)
<table><tr><th>MPU Type</th><th>E_RD</th><th>Description</th></tr><tr><td>6800-series</td><td>E</td><td>Read / Write control input pin
RW = “H”: When E is “H”, D0 to D17 are in an output.
RW = “L”: The data on D0 to D17 are latched at the falling edge of the E signal.</td></tr><tr><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, D0 to D17 are in an output status.</td></tr></table>When in the serial interface, connect it to VDD.</td></tr>
<tr><td>D17 to D0</td><td>I/O</td><td>They connect to the standard 8-bit or 16 bit MPU bus via the 8/16/18 –bit bi-directional bus.
When the following interface is selected and /CS pin is high, following pins become high impedance.
1. In 8-bit parallel: D17-D8 pins are in the state of high impedance should connect to VDD.
2. In 3-line/4-line interface D0 pad will be used for SI function
3. In 4-line interface D1 pad will be used for A0 function
4. In Serial interface: The unused pins are in the state of high impedance should connect to VDD.</td></tr>
<tr><td>SI</td><td>I</td><td>SI is used to input serial data when the serial interface is selected.(3 line and 4 line)
In ST7669, D0 is the SI when select serial interface. See Table 7.1.1</td></tr>
<tr><td>SCL</td><td>I</td><td>SCL is used to input serial clock when the serial interface is selected.
The data is converted in the rising edge. (3 line and 4 line)
In ST7669, RS is the SCL when select serial interface.See Table 7.1.1</td></tr>
<tr><td>TE</td><td>O</td><td>Tearing effect output.</td></tr>
<tr><td>/EXT</td><td>I</td><td>OTP burn-in control Pin
There is a pull-high resistor between /EXT & VDD in ST7669.
When burning OTP, please add an external VSS on /EXT. (needs external power supply voltage VPP=7.5V~7.75V)</td></tr>
</table>

NOTE： 1. In any status the control bus and data bus can not floating.

2. The no used pin should connect to VDD (Supply Digital Voltage).

6.5 LCD DRIVER OUTPUTS

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG395</td><td>O</td><td>LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">M (Internal)</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>Vg</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>Vg</td></tr>
<tr><td>L</td><td>H</td><td>VSS</td><td>Vg</td></tr>
<tr><td>L</td><td>L</td><td>Vg</td><td>VSS</td></tr>
<tr><td colspan="2">Sleep-In mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM161</td><td>O</td><td>LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>M (Internal)</th><th>Common driver output voltage</th></tr>
<tr><td>H</td><td>H</td><td>XV0</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>Vm</td></tr>
<tr><td>L</td><td>L</td><td>Vm</td></tr>
<tr><td colspan="2">Sleep-In mode</td><td>VSS</td></tr>
</table></td></tr>
</table>

Name	I/O	Description
TGI TGO	I O	TGI must connect to TGO by ITO which run a ring on LCM glass
TRUI TRUO	I O	TRUI must connect to TRUO by ITO
TLUI TLUO	I O	TLUI must connect to TLUO by ITO
TRBI TRBO	I O	TRBI must connect to TRBO by ITO
TLBI TLBO	I O	TLBI must connect to TLBO by ITO

Driving Waveform

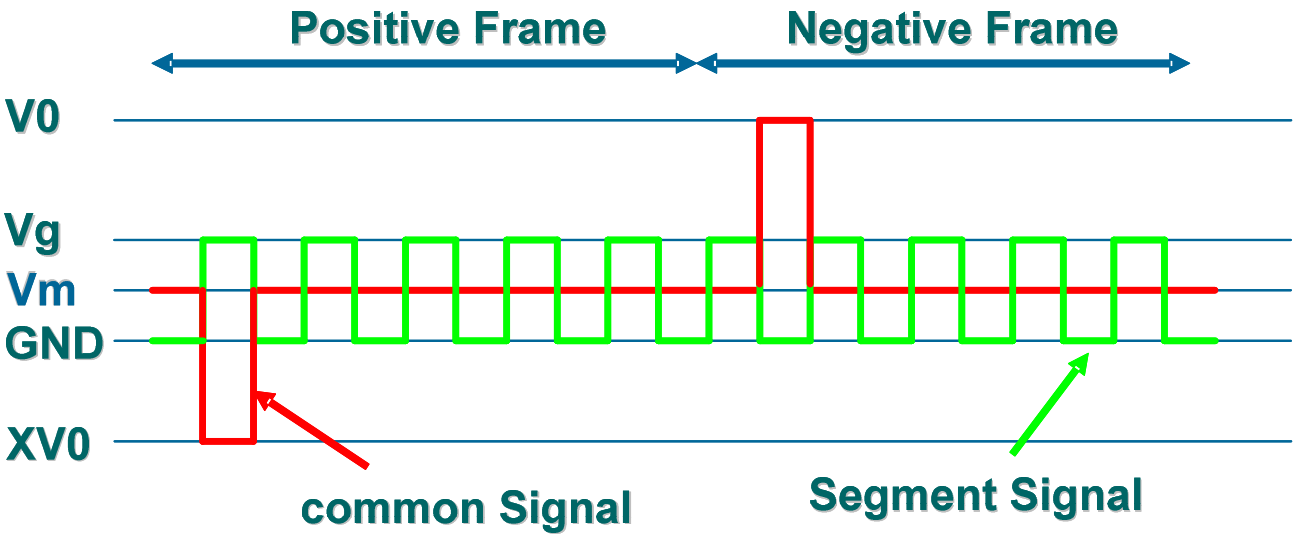


Figure 6.5-1 ST7669 COM/SEG Driving Waveform

ST7669 I/O PIN ITO Resister Limitation

Pin Name	ITO Resister
VDD, VDD2~VDD5, VSS,VSS1,VSS2,VSS4	<100Ω
$V0_{IN}$, $V0_{OUT}$, $V0_S$,$XV0_{IN}$, $XV0_{OUT}$,$XV0_S$, Vg_{IN}, Vg_{OUT} ,Vg_S ,Vm	<300Ω
VPP	<50Ω
A0, E_RD, RW_WR, /CS, D0 …D17, (SI), (SCL), TE	<1KΩ
/RST	<10KΩ
IF[3:1], CLS, CSEL, /EXT	<1KΩ
TCAP, CL, VREF	Floating

NOTE: 1. Make sure that the ITO resistance of COM0 ~ COM161 is equal, and so is it of SEG0 ~ SEG395.

These Limitations include the bottleneck of ITO layout.

2. The ITO layout suggestion is shown as below:

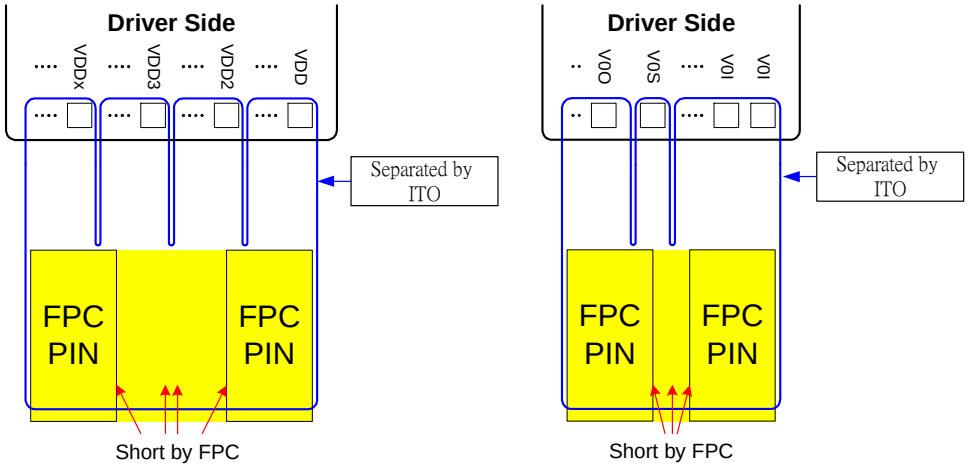


Figure 6.5-2 Power ITO layout sugestion

7 FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

/CS pin is for chip selection. The ST7669 is active when /CS=L. In serial interface mode,the internal shift register and the counter are reset when /CS=H.

7.1.1 Selecting Parallel / Serial Interface

ST7669 has eight types of interface with an MPU, which are two serial and six parallel interfaces. This parallel or serial interface is determined by IF pin as shown in Table 7.1-1.

Table 7.1-1Parallel / Serial Interface Mode

I/F Mode			I/F Description	Pin Assignment						
IF3	IF2	IF1		/CS	A0	E_RD	RW_WR	Used Data Bus	D1	D0
H	H	L	80 serial 8-bit parallel	/CS	A0	/RD	/WR	D7~D2	D1	D0
H	H	H	80 serial 16-bit parallel	/CS	A0	/RD	/WR	D15~D2	D1	D0
L	L	H	80 serial 18-bit parallel	/CS	A0	/RD	/WR	D17~D2	D1	D0
H	L	L	68 serial 8-bit parallel	/CS	A0	E	R/W	D7~D2	D1	D0
H	L	H	68 serial 16-bit parallel	/CS	A0	E	R/W	D15~D2	D1	D0
L	L	L	68 serial 18-bit parallel	/CS	A0	E	R/W	D17~D2	D1	D0
L	H	H	8-bit SPI mode (4 line)	/CS	SCL	--	--	--	A0	SI
L	H	L	9-bit SPI mode (3 line)	/CS	SCL	--	--	--	---	SI

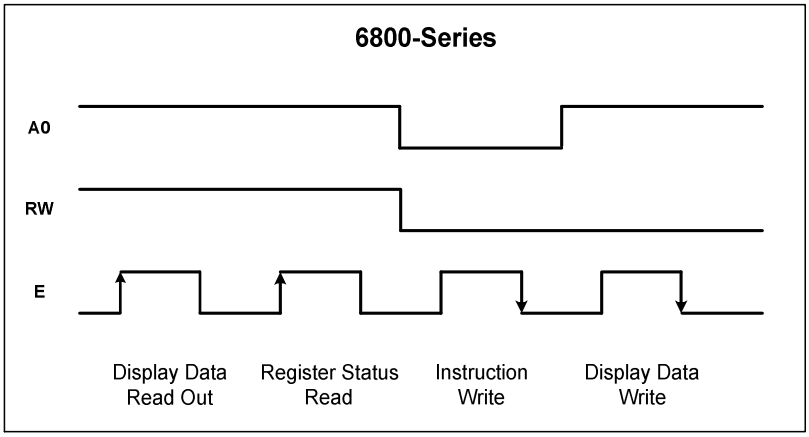
NOTE: When these pins are set to any other combination, A0, E_RD and RW_WR inputs are disabled and D0 to D17 are to be high impedance.

7.1.2 8-bit or 16-bit Parallel Interface

The ST7669 identifies the type of the data bus signals according to the combination of A0, /RD (E) and /WR (W/R) signals, as shown in**Table 7.1-2.**

Table 7.1-2Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	R/W	E	/RD	/WR	
H	H	↑	↓	H	Register status read
H	H	↑	↓	H	Display data read out
L	L	↓	H	↑	Instruction write
H	L	↓	H	↑	Display data write



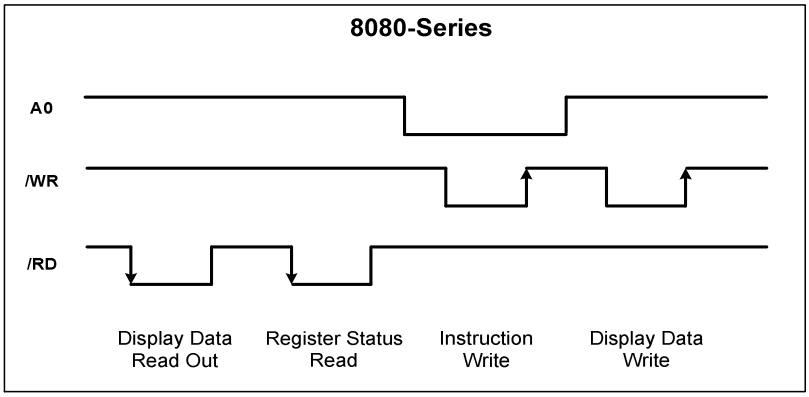


Figure 7.1-1 Parallel Data Transfer Example Chart

Relation between Data Bus and Gradation Data

ST7669 offers 256 color, 4096 color display, 65K color display, 262K color display, and truncated 16M color display. When using 256 color, 4096, 65K, 262K, and 16M color display; you can specify color for each of R, G, and B using the palette function. Use the command for switching between these modes.

(1) 256 color input mode

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: RRRGGGBB 1st -write

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st -write operation finishes.

2. 16-bit interface

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: XXXXXXXXRRRGGGBB 1st -write

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes. “X” are ignored dummy bits.

(2) 4096-color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRR 1st-write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB 2nd-write

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes. “X” are ignored dummy bits.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRRGGGGBBBB 1st-write

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes. “X” are ignored dummy bits.

(3) 65K color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGG 1st-write

D7, D6, D5, D4, D3, D2, D1, D0: GGGBBBBB 2nd-write

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGGGGGBBBBB

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes.

(4) 262K color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXX 1st-write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGXX 2nd-write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBXX 3rd-write

There are 3 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 3rd–write operation finishes. “X” are ignored dummy bits.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXXGGGGGGXX 1st-write

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBXXXXXXXXXXXX 2nd-write

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes. “X” are ignored dummy bits.

3. 18 bit mode

D17, D16, D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRGGGGGGBBBBBB

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes. “X” are ignored dummy bits.

(5) Truncated 16M color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRR 1st-write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGGG 2nd-write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBB 3rd-write

There are 3 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 3rd–write operation finishes. “X” are ignored dummy bits.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRRGGGGGGGG 1st-write

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBBXXXXXXXX 2nd-write

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes. “X” are ignored dummy bits.

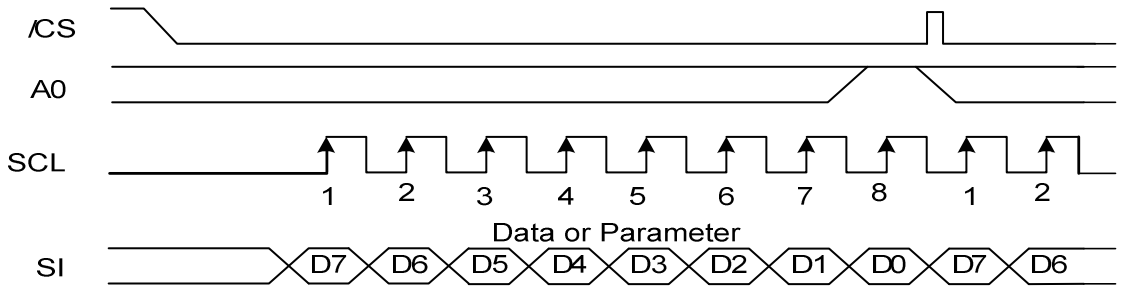
7.1.3 8- and 9-bit Serial Interface

The 8-bit serial interface uses four pins /CS, SI, SCL, and A0 to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins /CS, SI and SCL for the same purpose.

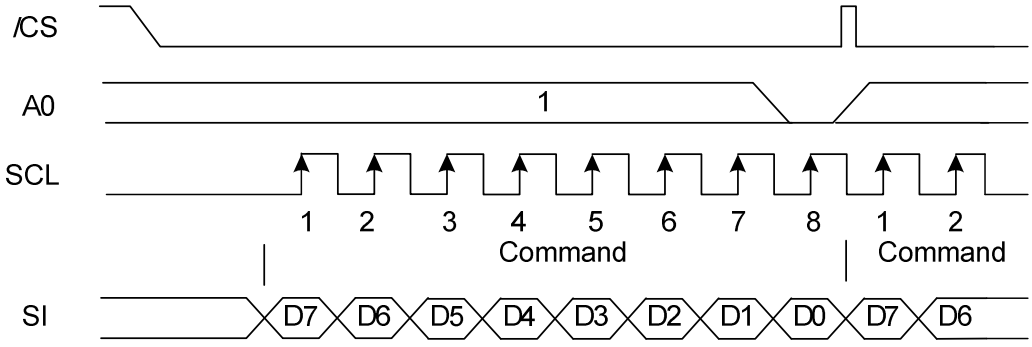
Data read is not available in the serial interface. Data entered must be 8 bits. The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4-line)

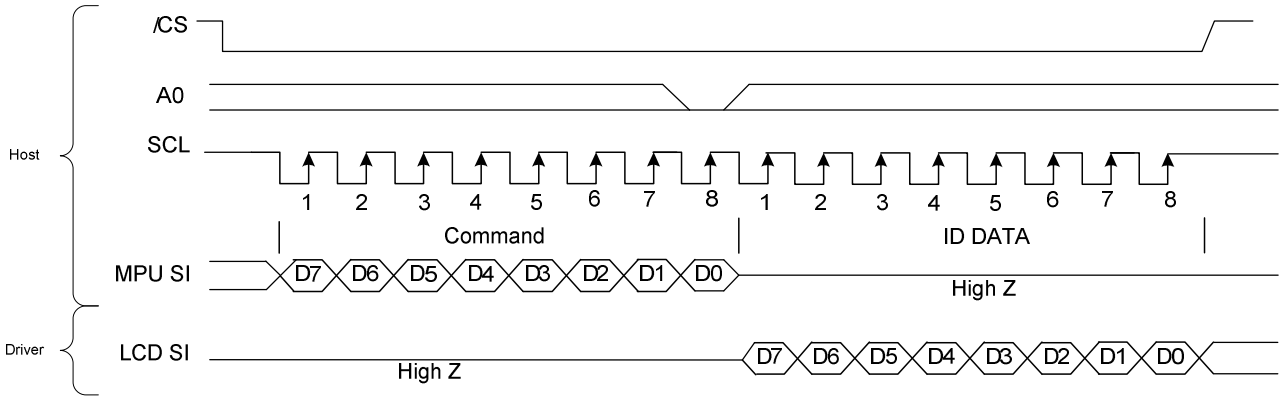
When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.



When entering command: A0= LOW at the rising edge of the 8th SCL

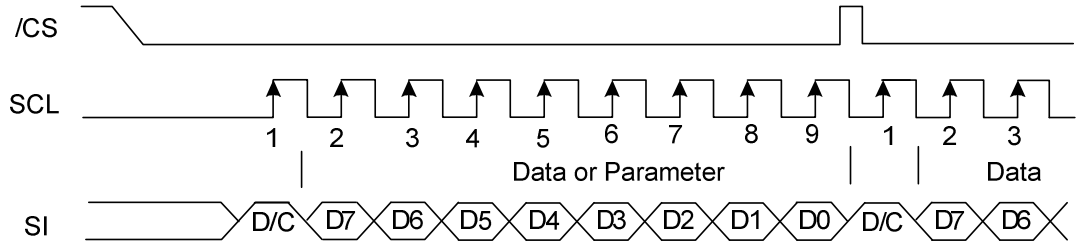


When entering reading command:

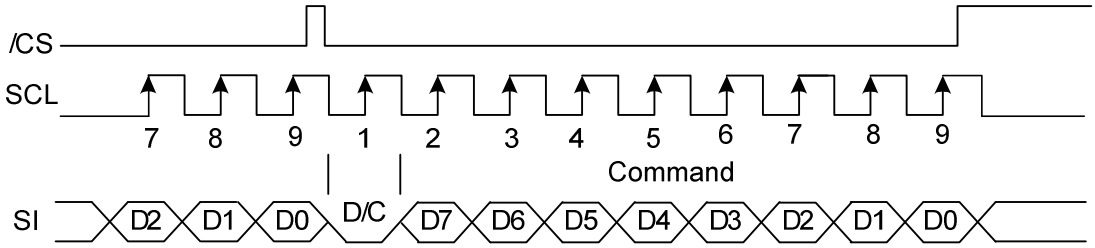


(2) 9-bit serial interface (3-line)

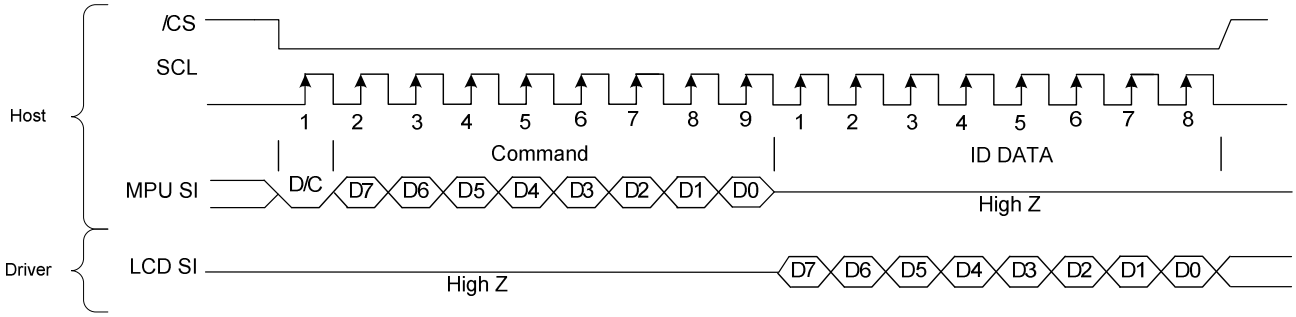
When entering data (parameters): SI= HIGH at the rising edge of the 1st SCL.



When entering command: SI= LOW at the rising edge of the 1st SCL.



When entering reading command :



- If /CS is set to HIGH while the 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set /CS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.

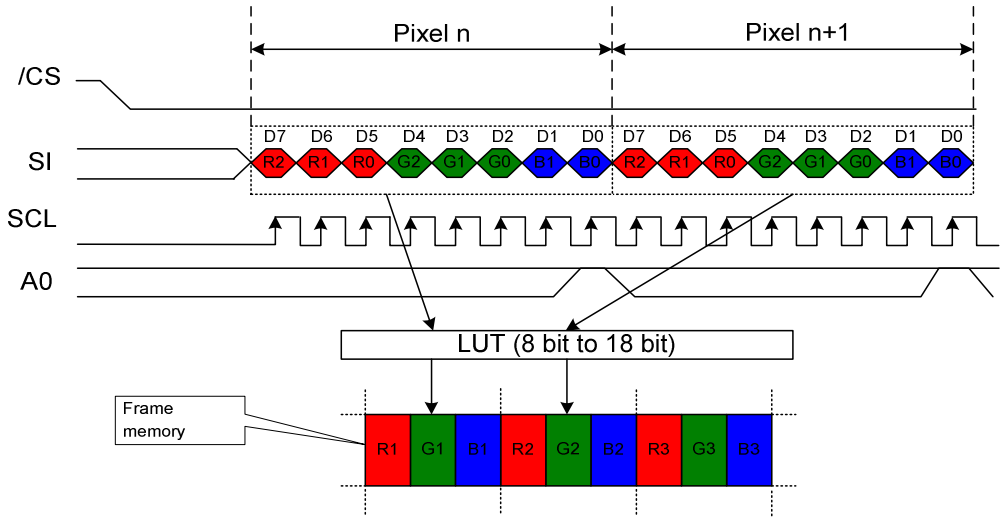
7.1.4 8-bit and 9-bit Serial Interface Data Color Coding

8-bit serial interface (4-line)

(1) R 3-bit, G 3-bit, B 2-bit, 256 colors

There is 1 pixel (= 3 sub-pixels) per byte.

There is 1 pixel (= 3 sub-pixels) per byte.

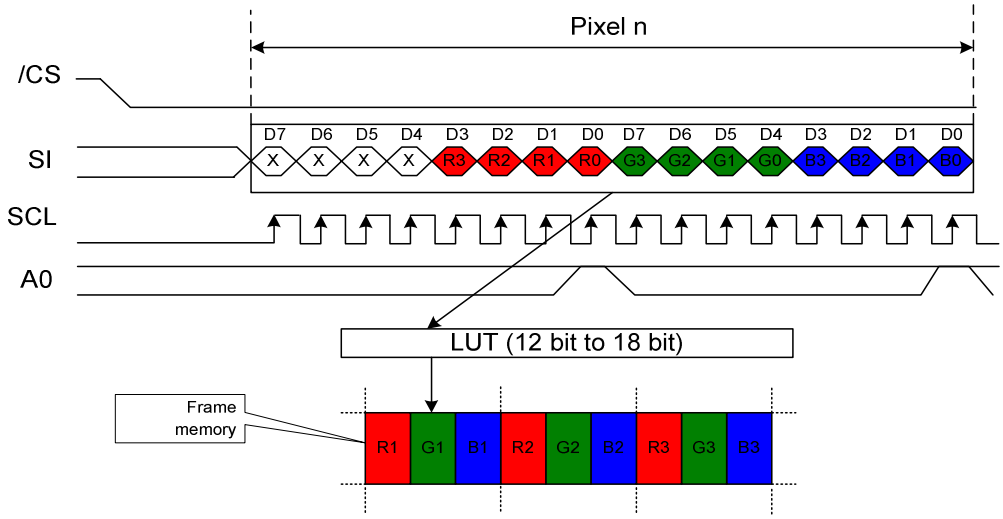


Note: R2, G2, B1 are the most significant bits and R0, G0, B0 are the least significant bits.

(2) R 4-bit, G 4-bit, B 4-bit, 4,096 colors

There is 1 pixel (= 3 sub-pixels) per 2 bytes.

There is 1 pixel (= 3 sub-pixels) per 2 bytes.

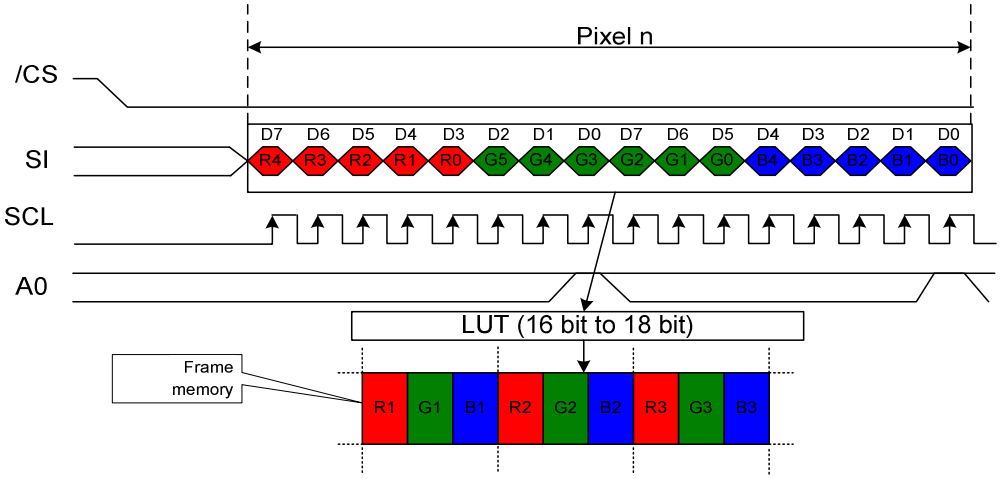


Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(3) R 5-bit, G 6-bit, B 5-bit, 65,536 colors

There is 1 pixel (= 3 sub-pixels) per 2 byte.

There is 1 pixel (= 3 sub-pixels) per 2 byte.

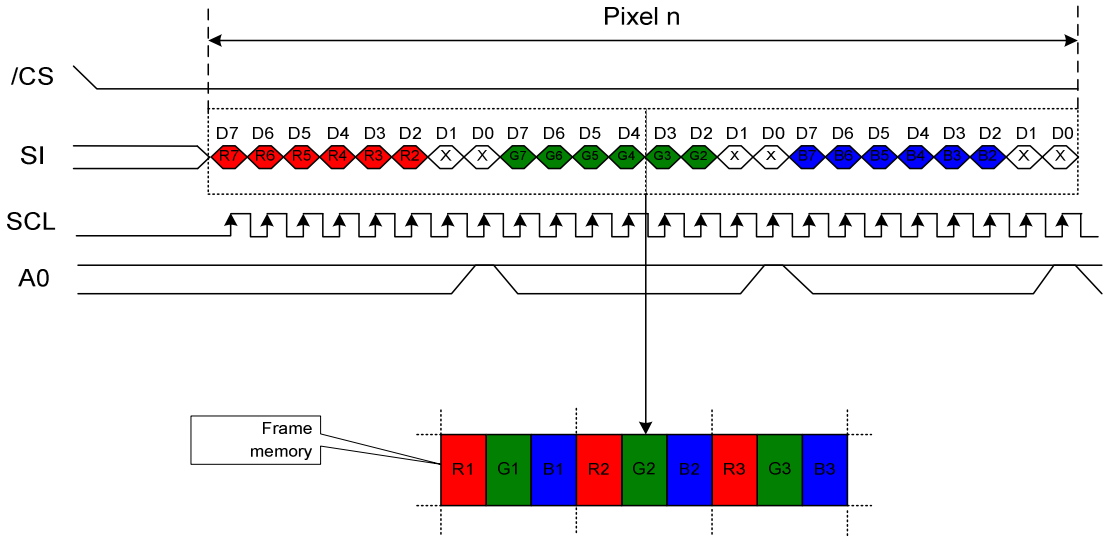


Note: R4, G5, B4 are the most significant bits and R0, G0, B0 are the least significant bits.

(4) R 6-bit, G 6-bit, B 6-bit, 262,144 colors

There is 1 pixel (= 3 sub-pixels) per 3 byte.

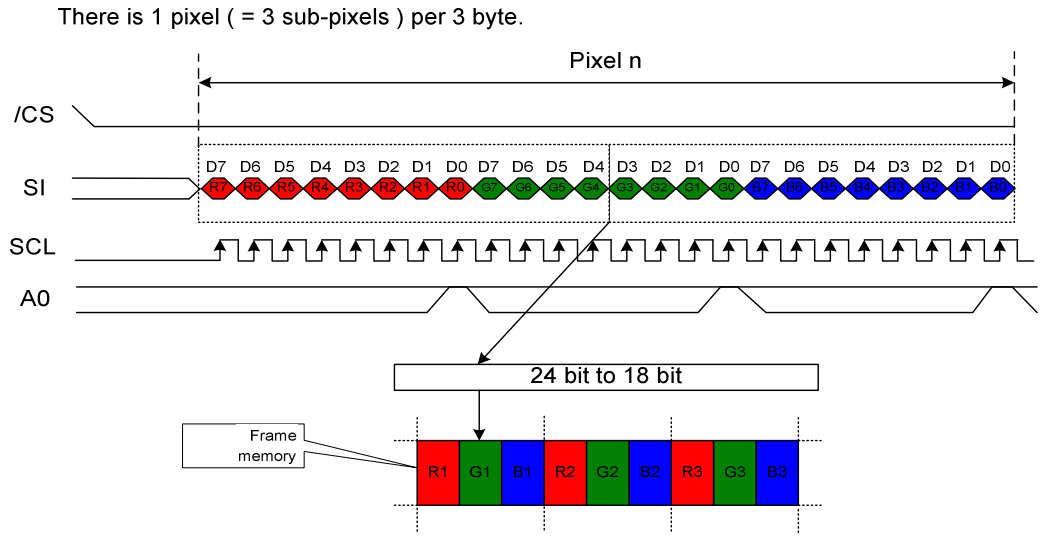
There is 1 pixel (= 3 sub-pixels) per 3 byte.



Note: R7, G7, B7 are the most significant bits and R2, G2, B2 are the least significant bits.

(5) R 8-bit, G 8-bit, B 8-bit, 16M colors

There is 1 pixel (= 3 sub-pixels) per 3 byte.

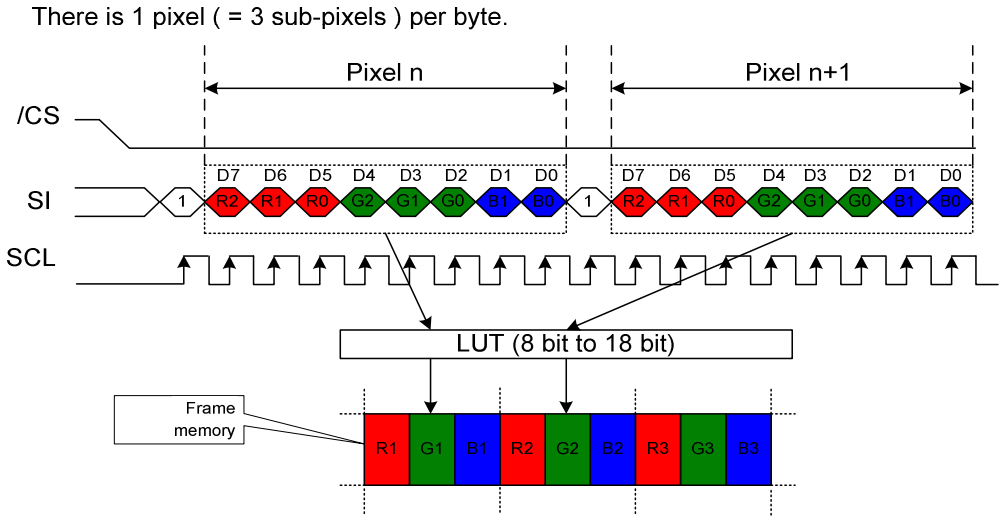


Note: R7, G7, B7 are the most significant bits and R0, G0, B0 are the least significant bits.

9-bit serial interface (3-line)

(1) R 3-bit, G 3-bit, B 2-bit, 256 colors

There is 1 pixel (= 3 sub-pixels) per byte.

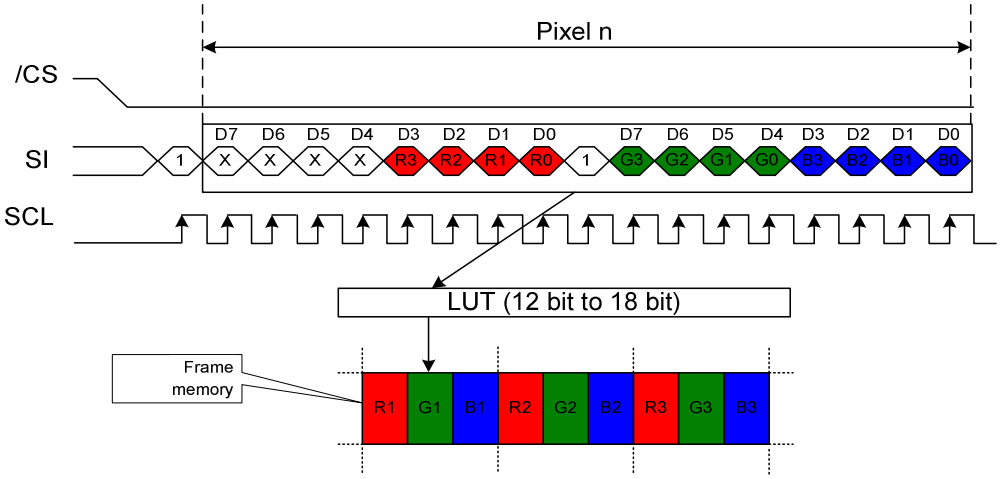


Note: R2, G2, B1 are the most significant bits and R0, G0, B0 are the least significant bits.

(2) R 4-bit, G 4-bit, B 4-bit, 4,096 colors

There is 1 pixel (= 3 sub-pixels) per 2 bytes.

There is 1 pixel (= 3 sub-pixels) per 2 bytes.

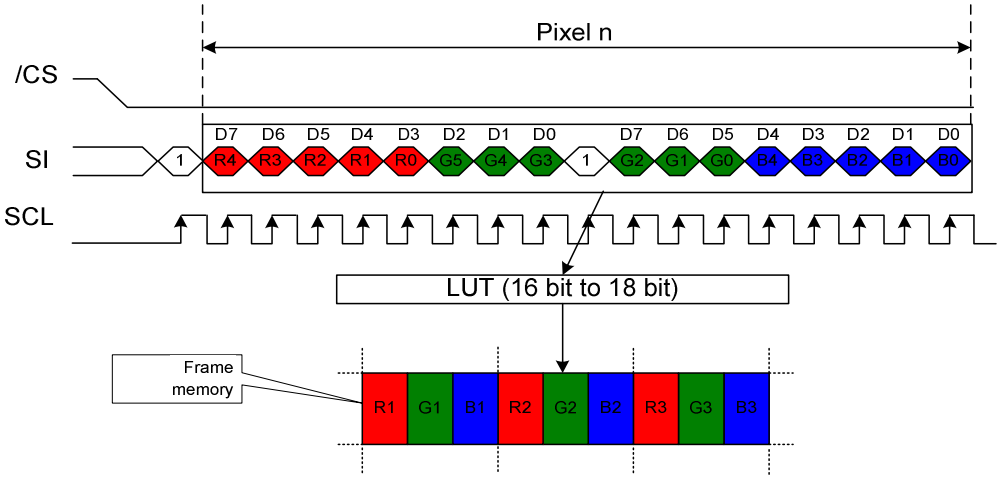


Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(3) R 5-bit, G 6-bit, B 5-bit, 65,536 colors

There is 1 pixel (= 3 sub-pixels) per 2 byte.

There is 1 pixel (= 3 sub-pixels) per 2 byte.

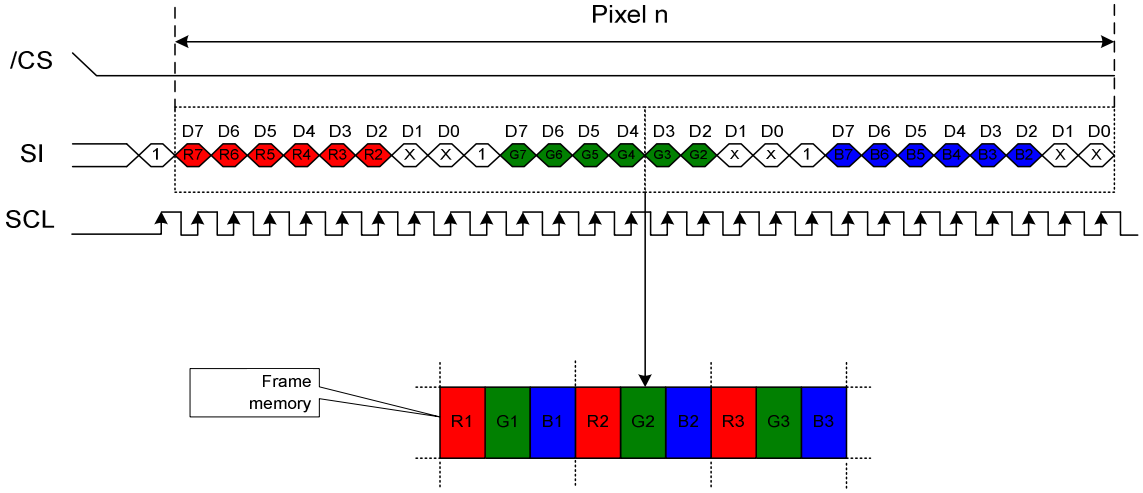


Note: R4, G5, B4 are the most significant bits and R0, G0, B0 are the least significant bits.

(4) R 6-bit, G 6-bit, B 6-bit, 262,144 colors

There is 1 pixel (= 3 sub-pixels) per 3 byte.

There is 1 pixel (= 3 sub-pixels) per 3 byte.

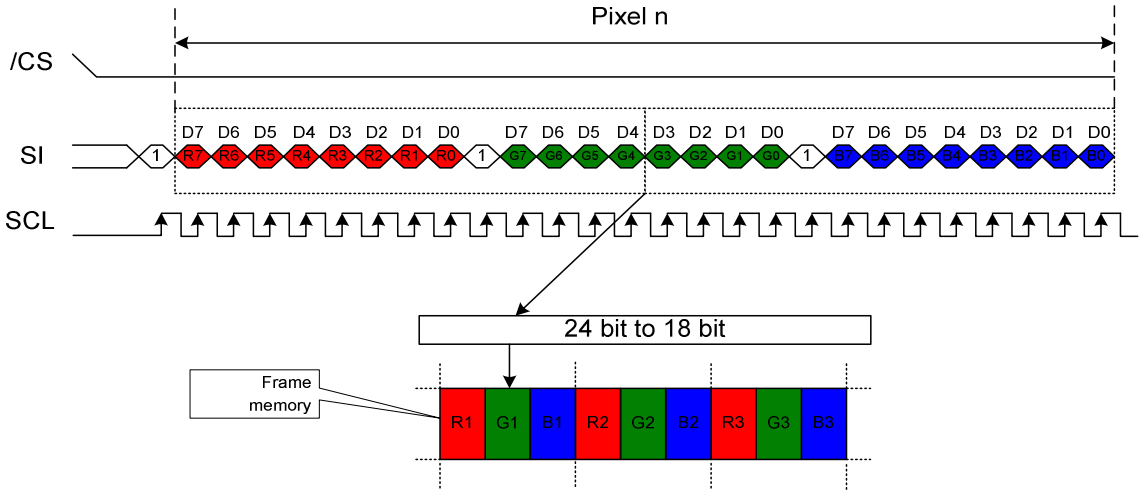


Note: R7, G7, B7 are the most significant bits and R2, G2, B2 are the least significant bits.

(5) R 8-bit, G 8-bit, B 8-bit, 16M colors

There is 1 pixel (= 3 sub-pixels) per 3 byte.

There is 1 pixel (= 3 sub-pixels) per 3 byte.



Note: R7, G7, B7 are the most significant bits and R0, G0, B0 are the least significant bits.

7.2 ACCESS TO DDRAM AND INTERNAL REGISTERS

ST7669 realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle. Figure 7.2-1 illustrates these relations.

In 80-series interface mode:

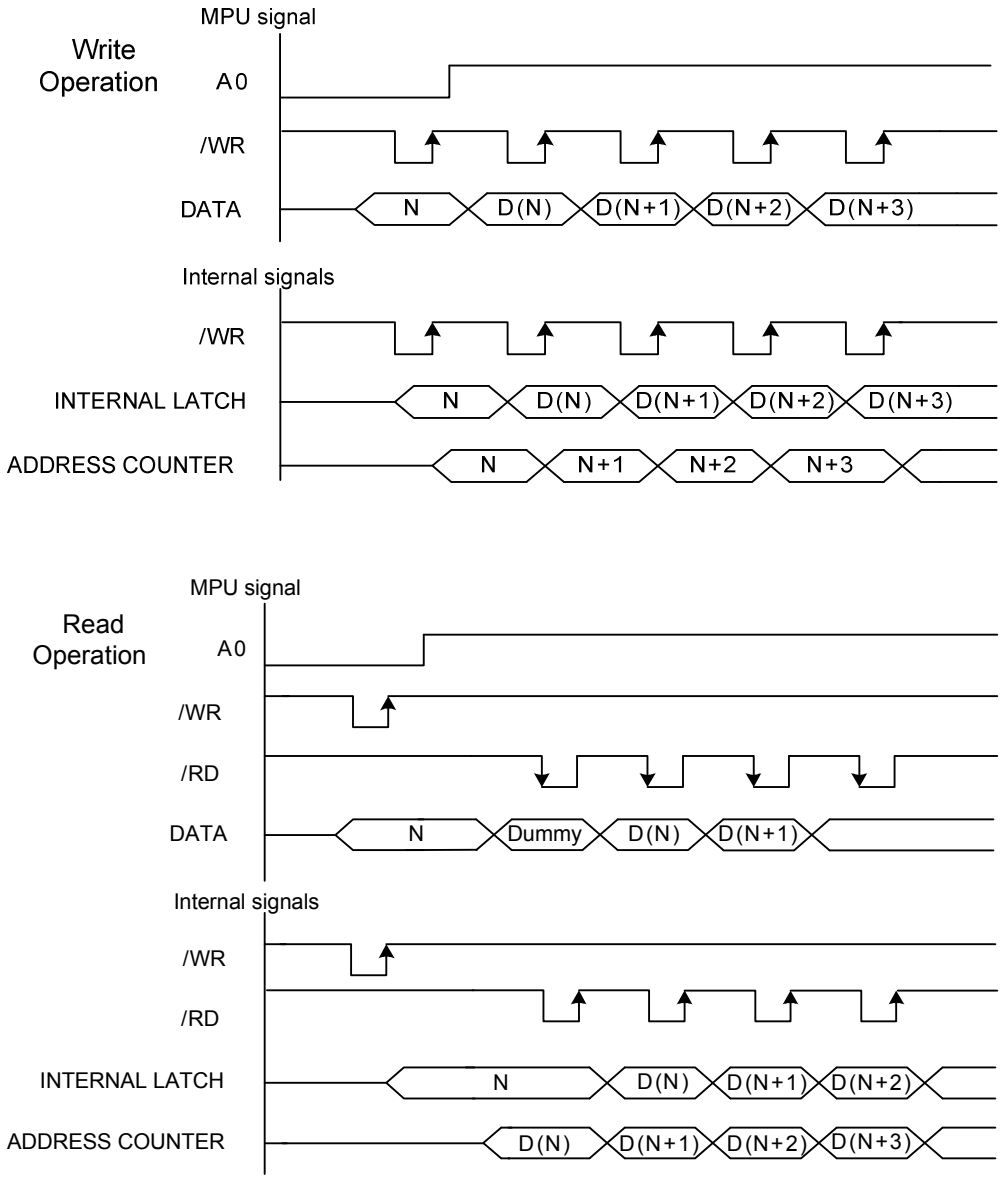


Figure 7.2-1

7.3 DISPLAY DATA RAM (DDRAM)

7.3.1 DDRAM

It is 132 X 162 X 18 bits capacity RAM prepared for storing dot data. Refer to the following memory map for the RAM configuration.

Memory Map

RGB alignment													
Data control command			**Column**										
	(MADCTR) MX=0		**0**			**1**					**131**		
	(MADCTR) MX=1		**131**			**130**					**0**		
	Color		**R**	**G**	**B**	**R**	**G**	**B**			**R**	**G**	**B**
	Data / Page												
	(MADCTR) MY=0	**(MADCTR) MY=1**											
	0	**161**											
	1	**160**											
	2	**159**											
	3	**158**											
	4	**157**											
	5	**156**											
	6	**155**											
	7	**154**											
	:	**:**											
	154	**7**											
	155	**6**											
	156	**5**											
	157	**4**											
	158	**3**											
	159	**2**											
	160	**1**											
	161	**0**											
SEGout			**0**	**1**	**2**	**3**	**4**	**5**			**393**	**394**	**395**

You can change position of R and B with MADCTR command.

7.3.2 Address Control

The address counter sets the addresses of the display data RAM for writing.

Data is written pixel into the RAM matrix of ST7669. The data for one pixel or two pixels is collected (RGB 6-6-6 bit), according to the data formats. As soon as this pixel-data information is complete, the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed.

Before writing to the RAM, a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=131 (83h), YE=161 (A1h).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (MV=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to SC and Y increments to address the next row. After the every last address (X=XE and Y=XE) the address pointers wrap around to address (X=XS and Y=YS). For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET” and “MADCTR” , define flags MX, MY and MV, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Figure 7.3-1 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

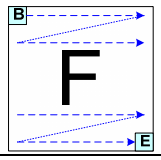
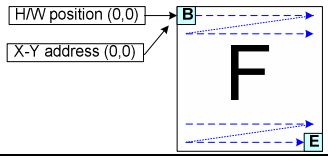
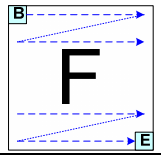
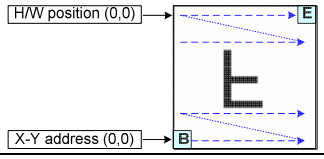
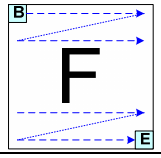
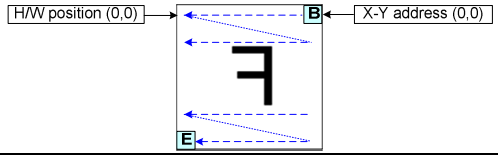
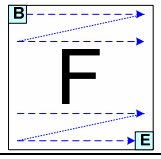
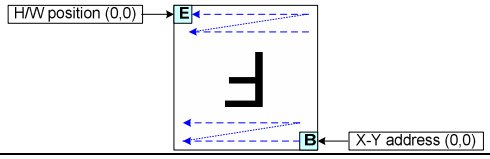
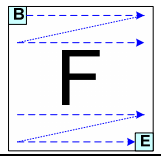
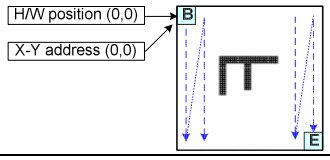
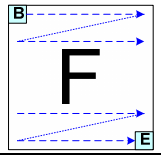
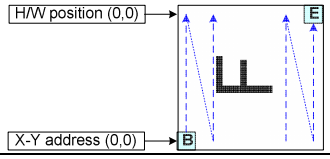
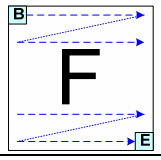
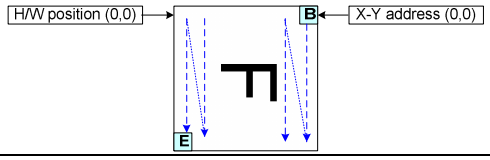
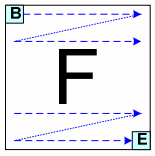
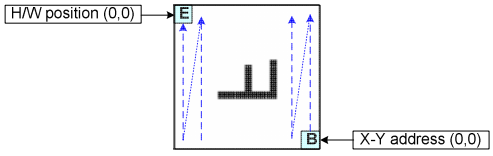
Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 7.3-1 Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

7.3.3 I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM when the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.4 Scroll Address Circuit

The circuit associates pages on DDRAM with COM output. ST7669 processes signals for the liquid crystal display on 1-page basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in block

7.3.5 Display data Latch Circuit

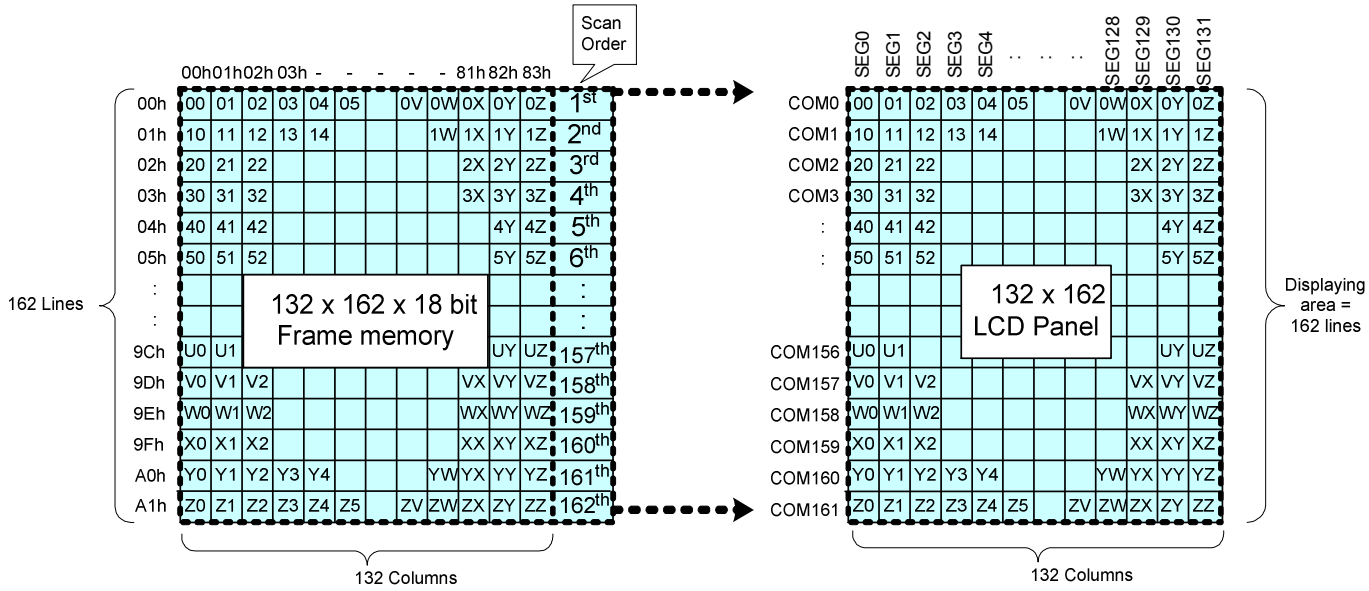
This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

7.3.6 Normal Display On or Partial Mode On, Vertical Scroll Off

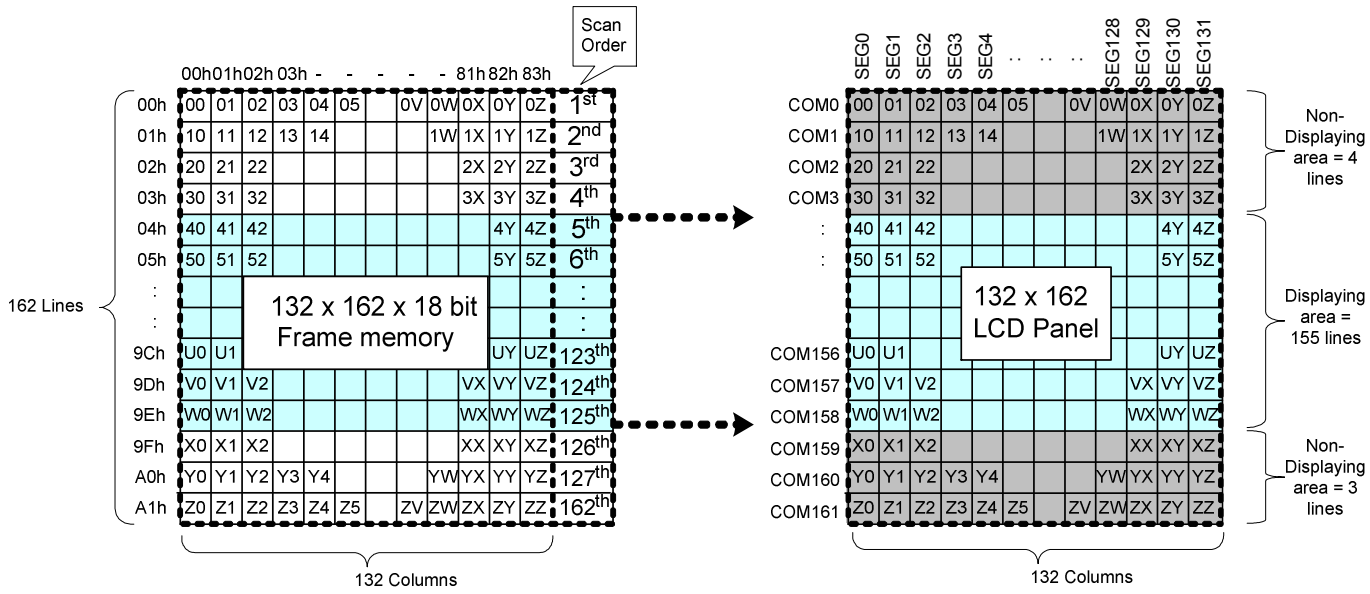
In this mode, contents of the frame memory within an area where column address is 00h to 83h and row address is 00h to A1h is displayed.

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).

Example1) Normal Display On



Example2) Partial Display On: SR[15:0] = 0004h, ER[15:0] = 009Eh, MADCTL (ML)=0



7.3.7 Vertical Scroll/Rolling Scroll

Rolling Scroll

There is just one types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

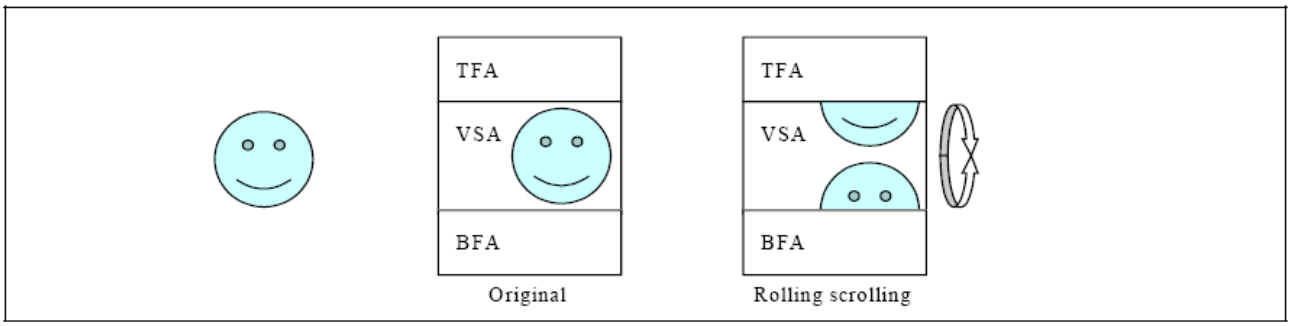
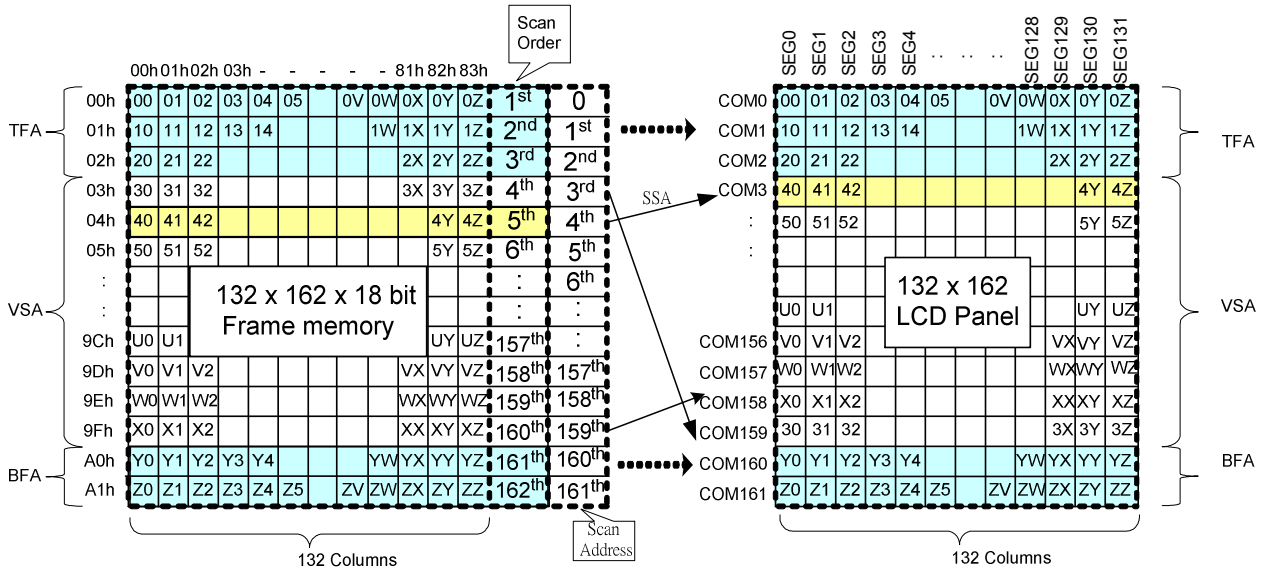


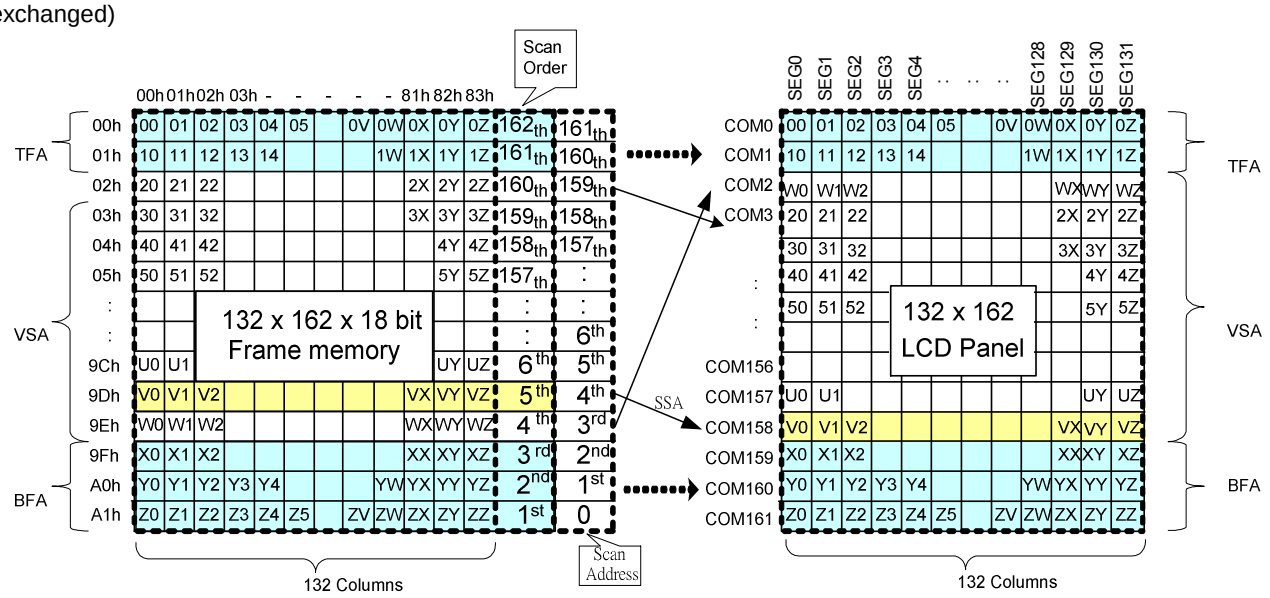
Figure 7.3-2 Rolling Scroll Definition

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =162. In this case, ‘rolling’ scrolling is applied as shown below. All the memory contents will be used.

Example1) Panel size=162 x 132, TFA =3, VSA=157, BFA=2, SSA=4, MADCTL (ML)=0: Rolling Scroll



Example2) Panel size=162 x 132, TFA =2, VSA=157, BFA=3, SSA=4, MADCTL (ML)=1: Rolling Scroll (TFA and BFA are exchanged)



Vertical Scroll Example

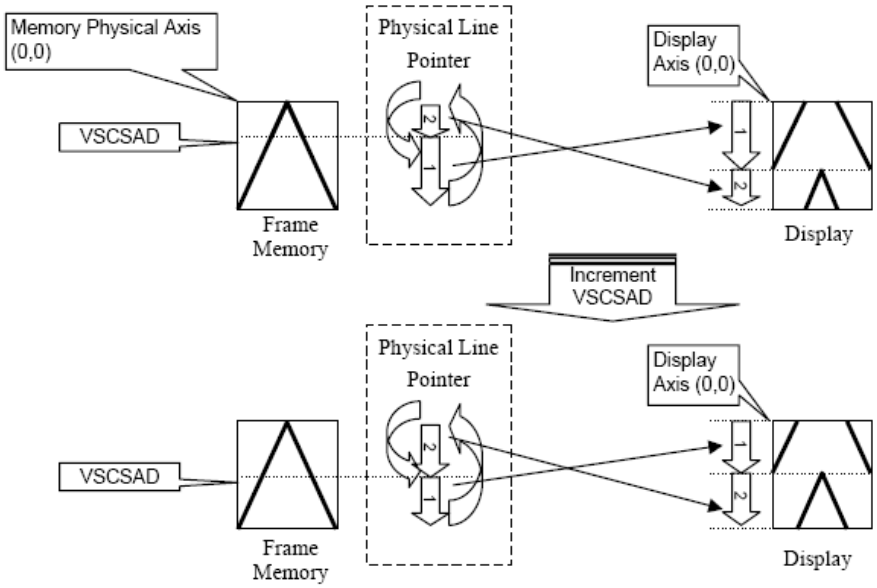
There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA<162

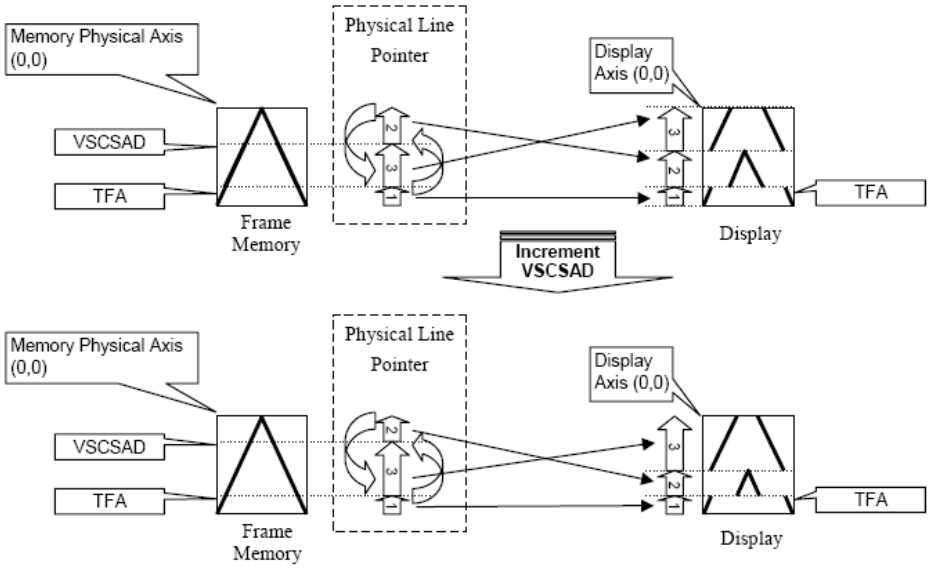
N/A. Do not set TFA + VSA + BFA<162. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=162 (Rolling Scrolling)

Example1) When MADCTL parameter ML="0", TFA=0, VSA=162, BFA=0 and VSCSAD=40.



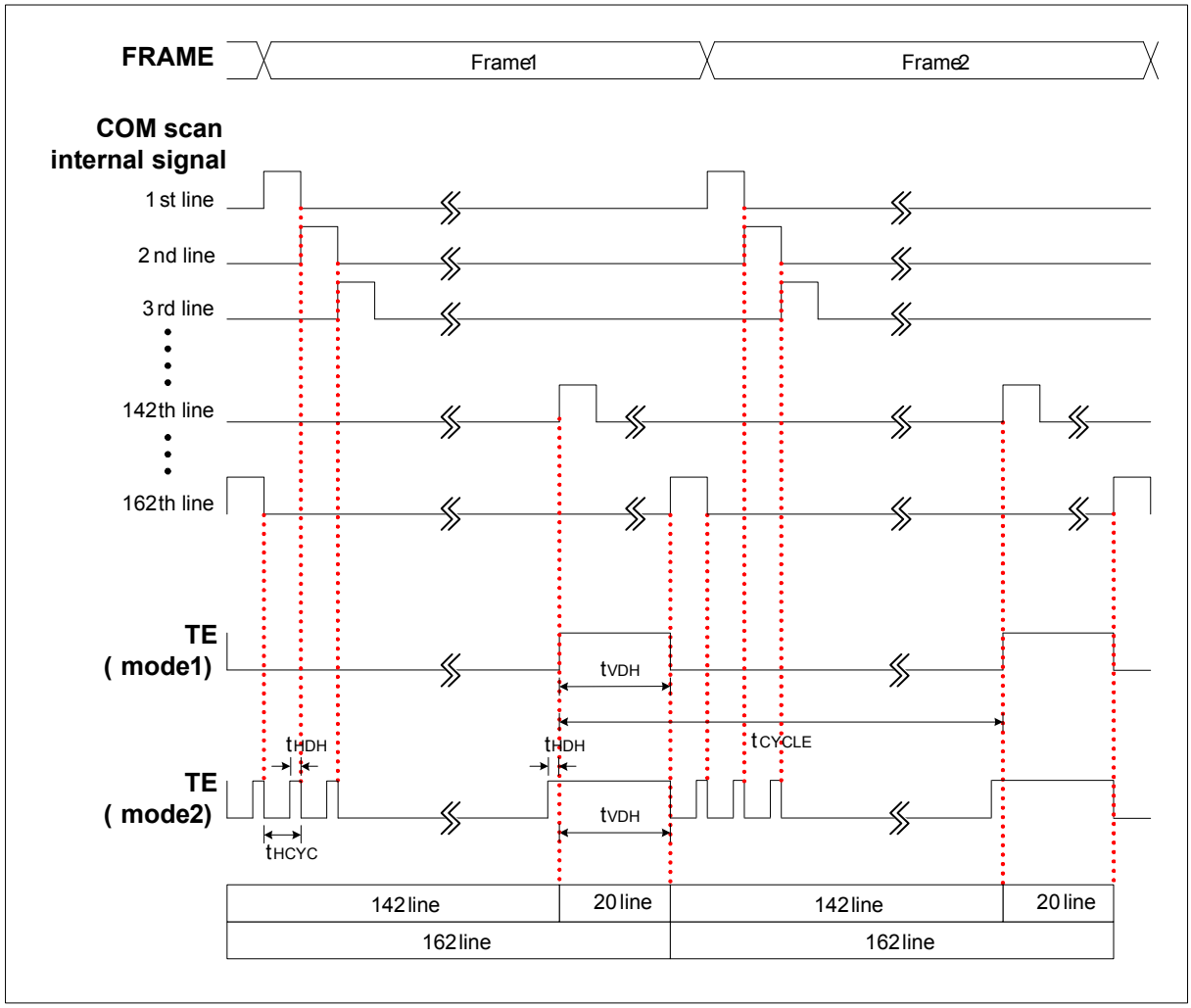
Example2) When MADCTL parameter ML="1", TFA=10, VSA=152, BFA=0 and VSCSAD=30.



7.3.8 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

Tearing Effect Line Modes



Mode 1, the Tearing Effect Output signal consists of V-Sync(tVDH) information. It starts at 142th line signal and ends at the 162th line signal. There is one high pulse during each frame.

Mode 2, the Tearing Effect Output signal consists of both H-Sync(tHDH) and V-Sync(tVDH) information. TE pin output tHDH pulse on each COM scan signal. During 142th ~ 162th line signal, it output a high pulse which equals 1 tHDH + 1 tVDH.

Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

Tearing Effect Line Timing

The Tearing Effect signal is described below:

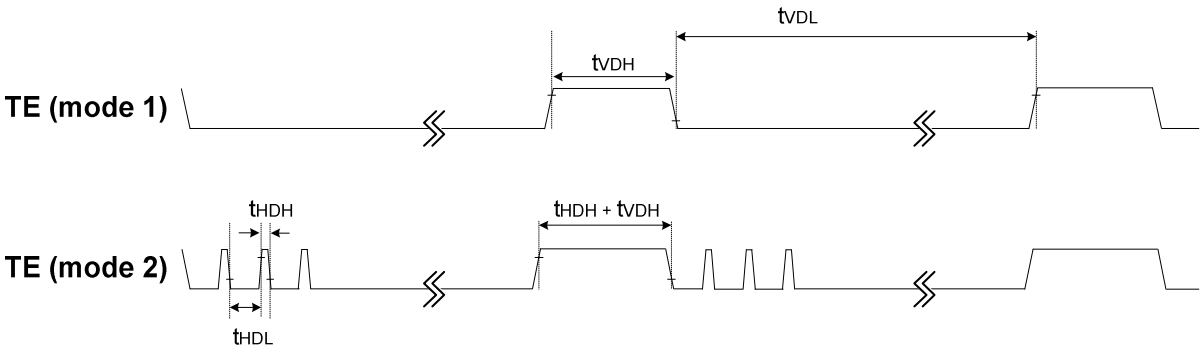


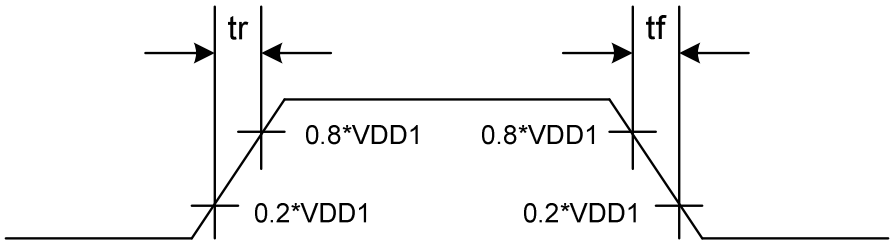
Table 7.3-1AC characteristics of Tearing Effect Signal

Idle Mode Off (Frame Rate = 77Hz)

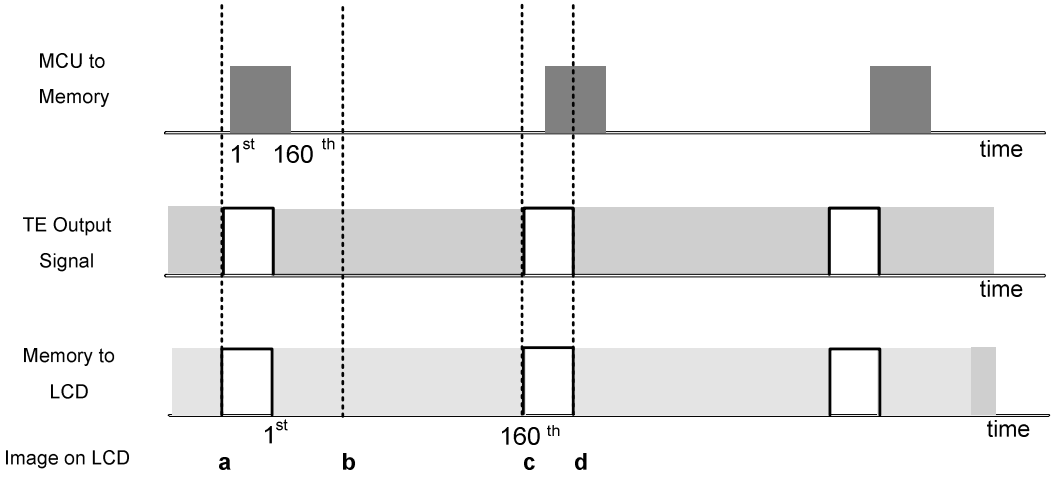
Symbol	Parameter	Min	Typ	Max	Unit	description
t_{VDL}	Vertical Timing Low Duration	--	11.4	12	ms	Mode1
t_{VDH}	Vertical Timing High Duration	1	1.6	2	ms	
t_{HDL}	Horizontal Timing Low Duration	--	75	80	us	Mode2
t_{HDH}	Horizontal Timing High Duration	3	5.17	5.5	us	

NOTE: The timings in Table 7.3-1 apply when MADCTR B4=0 and B4=1

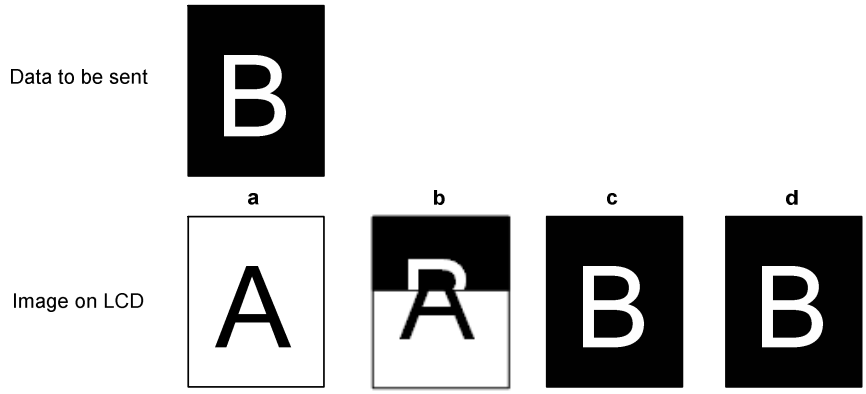
The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



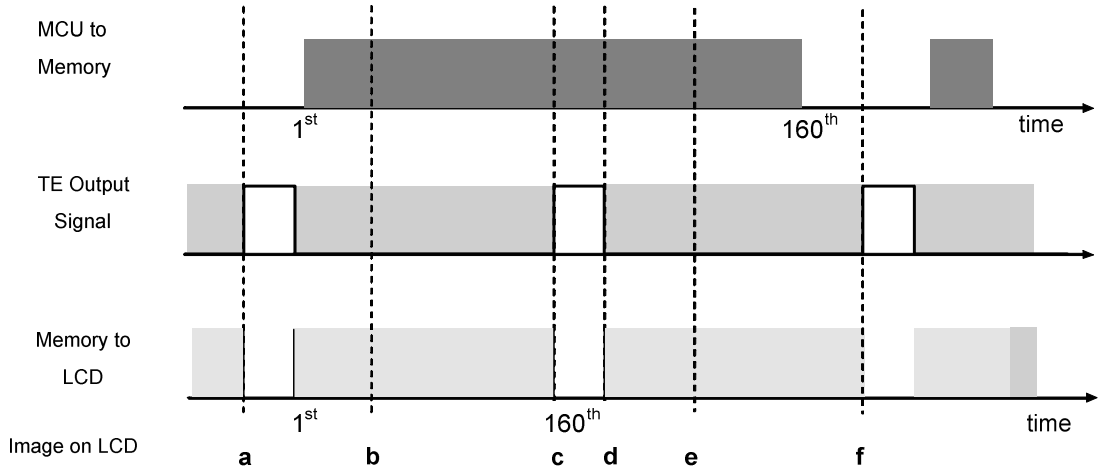
Example 1: MPU Write is faster than Panel Read.



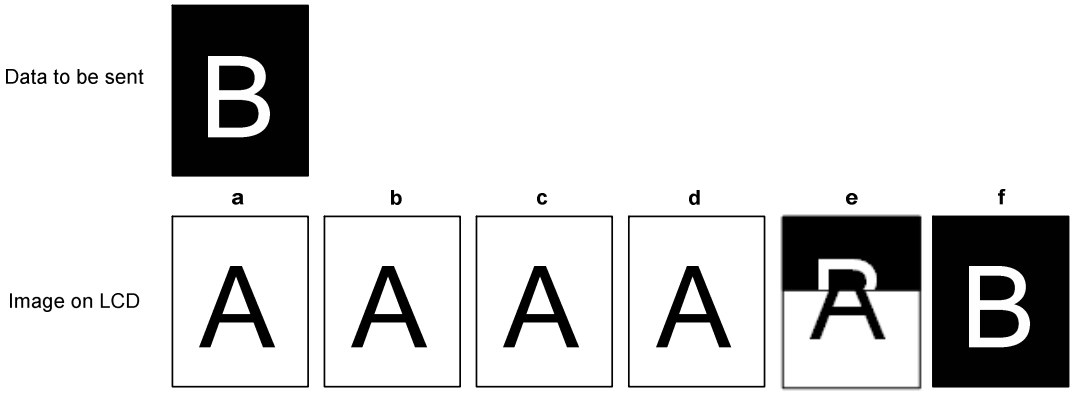
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



Example 2: MPU Write is slower than Panel Read.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



7.4 GRAY-SCALE DISPLAY

ST7669 incorporates a 4FRC & 31 PWM function circuit to display a 64 gray-scale display.

7.5 OSCILLATION CIRCUIT

This is on-chip oscillator without external resistor. When the internal oscillator is used, CLS must connect to VDD; when the external oscillator is used, CL could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

7.6 DISPLAY TIMING GENERATOR CIRCUIT

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), which is generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 96-bits display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M), which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.3-3.

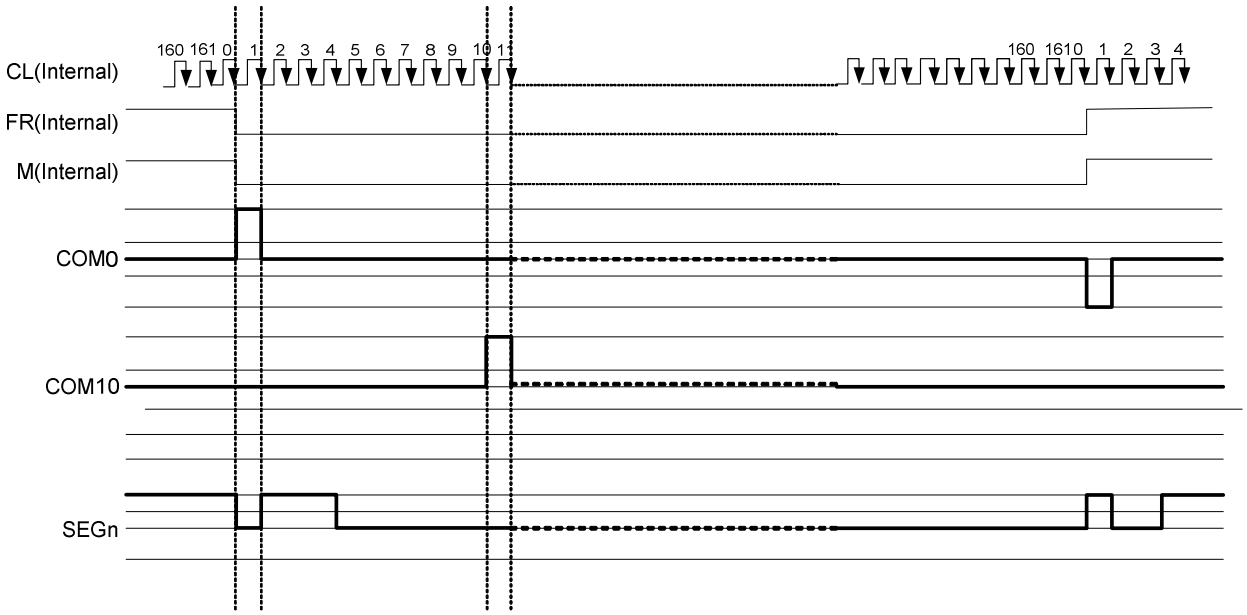


Figure 7.3-3 2-frame AC Driving Waveform (Duty Ratio: 1/162)

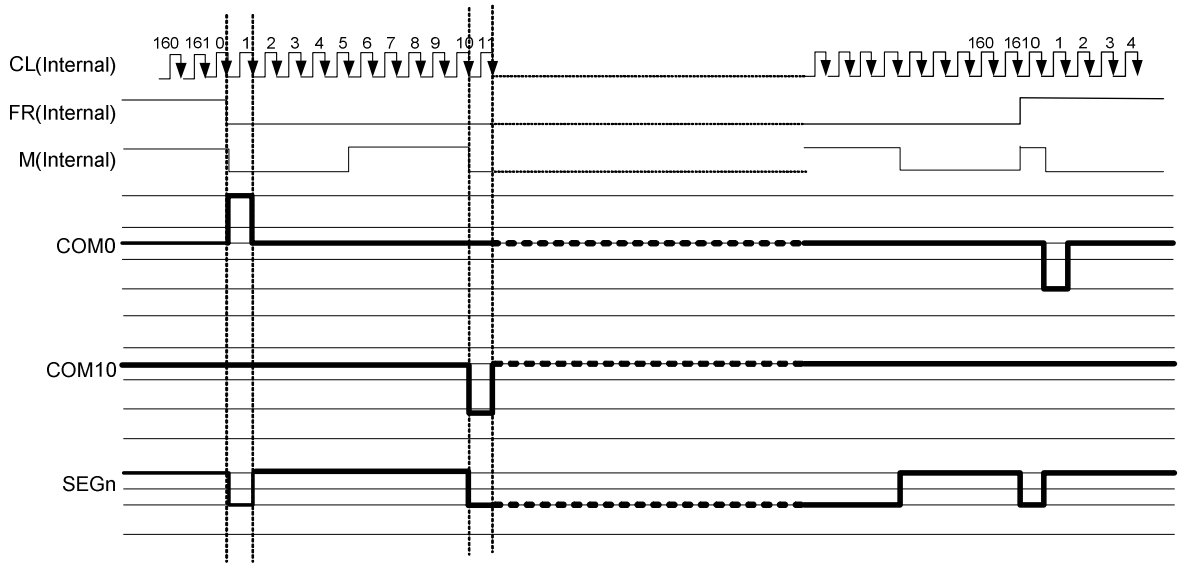


Figure 7.3-4 N-Line Inversion Driving Waveform (N=10, Duty Ratio=1/162)

7.7 POWER LEVEL DEFINITION

7.7.1 Power ON/OFF SEQUENCE

VDDI and VDDA can be applied in any order.**(VDDI=VDD , VDDA=VDD2,VDD3,VDD4,VDD5)**

VDDI and VDDA can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 200msec after /RST has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDDA can be powered down minimum 0msec after /RST has been released.

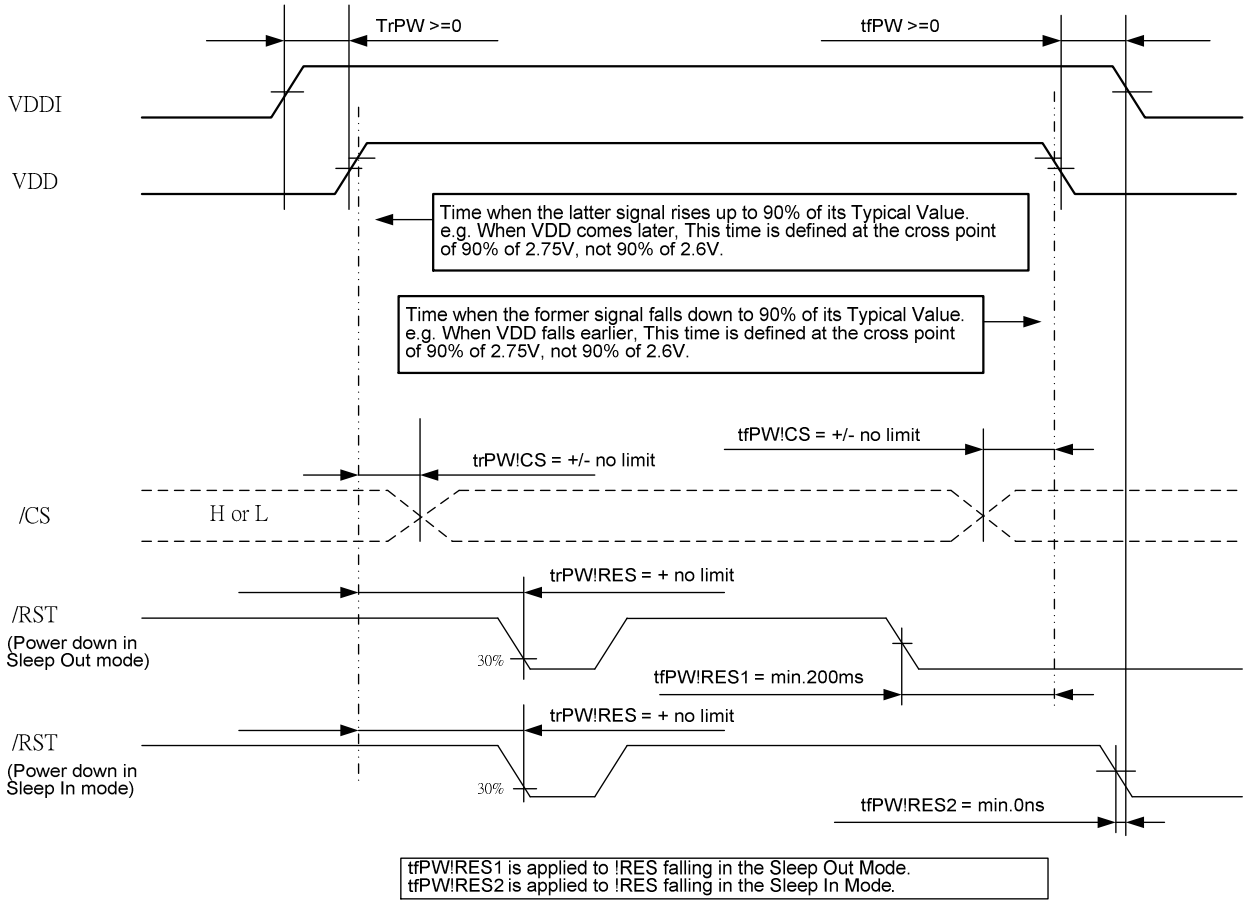
/CS can be applied at any timing or can be permanently grounded. /RST has priority over /CS.

If /RST line is not held stable by host during Power On Sequence as defined in Sections case1 and case2, then it will be necessary to apply a Hardware Reset (/RST) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

Case 1 – /RST line is held High or Unstable by Host at Power On

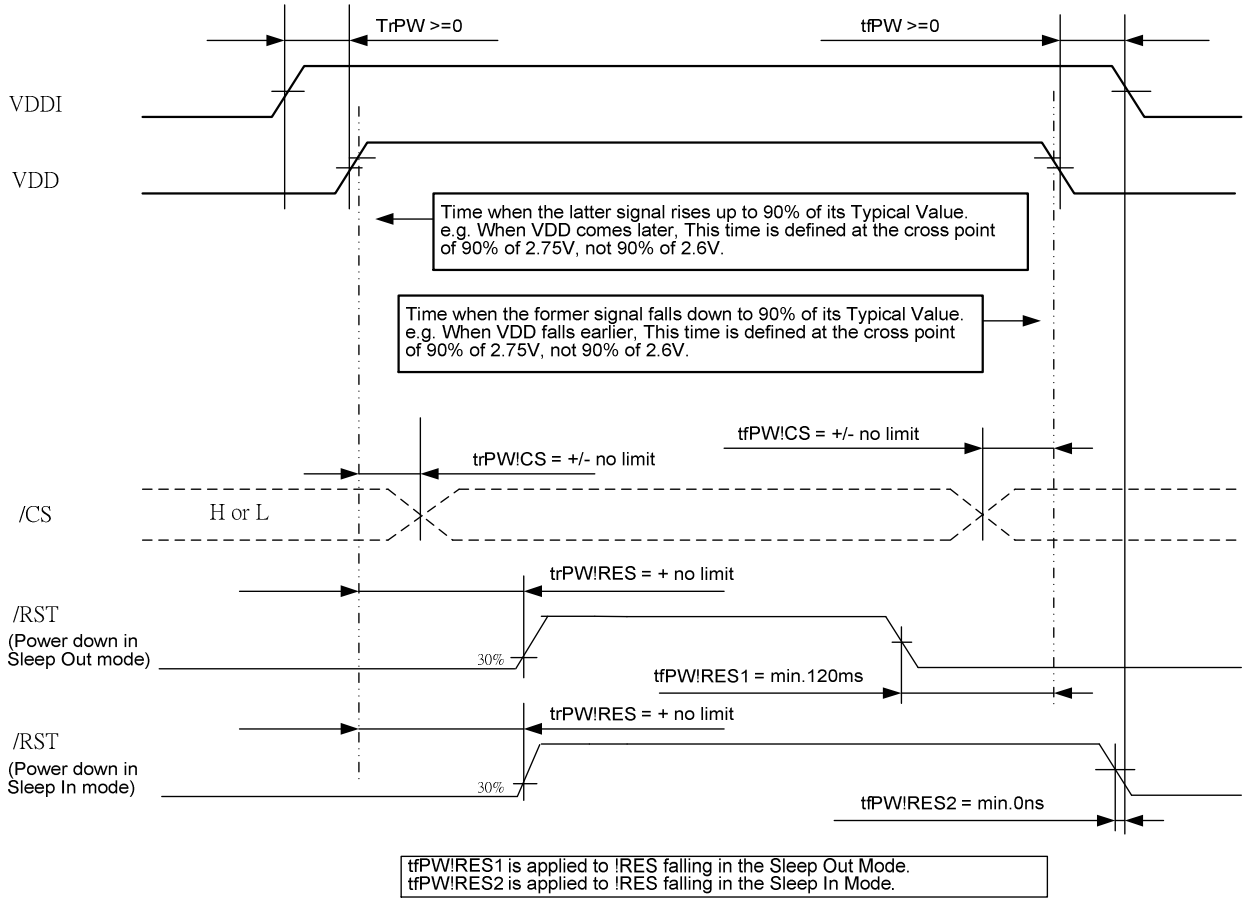
If /RST line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDDA and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Case 2 – /RST line is held Low by host at Power On

If /RST line is held Low (and stable) by the host during Power On, then the /RST must be held low for minimum 10µsec after both VDD and VDDI have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.7.2 Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out:

In this mode, the display is able to show maximum 262K colours.

2. Partial Mode On, Idle Mode Off, Sleep Out:

In this mode part of the display is used with maximum 262K colours.

3. Normal Mode On (full display), Idle Mode On, Sleep Out:

In this mode, the full display area is used but with 8 colours.

4. Partial Mode On, Idle Mode On, Sleep Out:

In this mode, part of the display is used but with 8 colours.

5. Sleep In Mode:

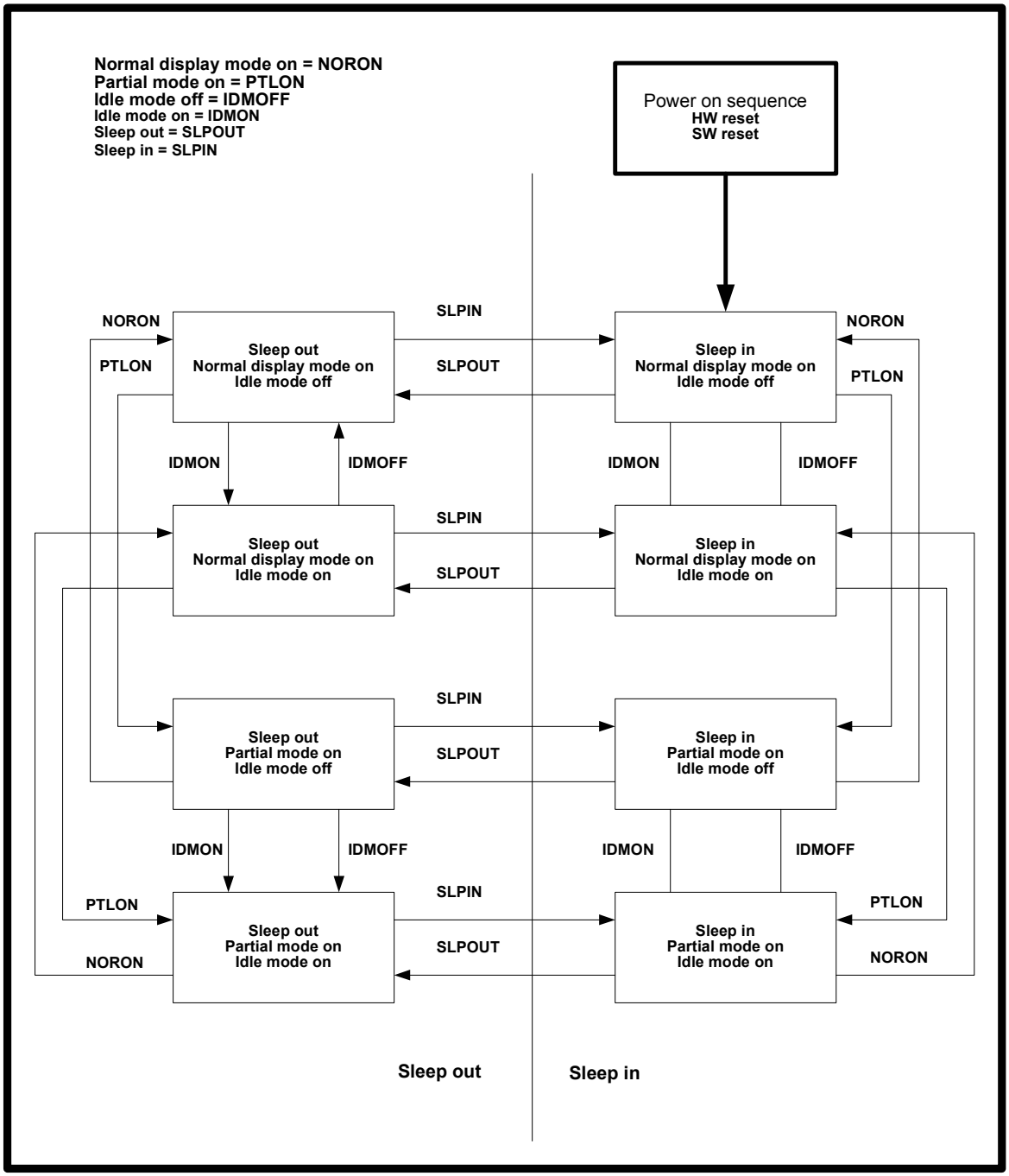
In this mode, the DC:DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with Digital VDDI power supply. Contents of the memory are safe.

6. Power Off Mode:

In this mode, both Analog VDDA and Digital VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

7.7.3 POWER FLOW CHART FOR DIFFERENT POWER MODES



Note

There is not any abnormal visual effect when there is changing from one power mode to another power mode.

7.8 COLOR DEPTH CONVERSION LOOK UP TABLE

R input (3bit) 256 colours 8 bit/pixel mode	R input (4bit) 4,096 colors 12 bit/pixel -mode	R input (5 bit) 65,536 colours 16 bit/pixel -mode	R output (6bit) 262,144 colours 18 bit/pixel -mode	RGBSET Parameter
000	0000	00000	R_{005} R_{004} R_{003} R_{002} R_{001} R_{000}	1
001	0001	00001	R_{015} R_{014} R_{013} R_{012} R_{011} R_{010}	2
010	0010	00010	R_{025} R_{024} R_{023} R_{022} R_{021} R_{020}	3
011	0011	00011	R_{035} R_{034} R_{033} R_{032} R_{031} R_{030}	4
100	0100	00100	R_{045} R_{044} R_{043} R_{042} R_{041} R_{040}	5
101	0101	00101	R_{055} R_{054} R_{053} R_{052} R_{051} R_{050}	6
110	0110	00110	R_{065} R_{064} R_{063} R_{062} R_{061} R_{060}	7
111	0111	00111	R_{075} R_{074} R_{073} R_{072} R_{071} R_{070}	8
Dummy Input	1000	01000	R_{085} R_{084} R_{083} R_{082} R_{081} R_{080}	9
Dummy Input	1001	01001	R_{095} R_{094} R_{093} R_{092} R_{091} R_{090}	10
Dummy Input	1010	01010	R_{105} R_{104} R_{103} R_{102} R_{127} R_{100}	11
Dummy Input	1011	01011	R_{115} R_{114} R_{113} R_{112} R_{111} R_{110}	12
Dummy Input	1100	01100	R_{125} R_{124} R_{123} R_{122} R_{121} R_{120}	13
Dummy Input	1101	01101	R_{135} R_{134} R_{133} R_{132} R_{131} R_{130}	14
Dummy Input	1110	01110	R_{145} R_{144} R_{143} R_{142} R_{141} R_{140}	15
Dummy Input	1111	01111	R_{155} R_{154} R_{153} R_{152} R_{151} R_{150}	16
Dummy Input	Dummy Input	10000	R_{165} R_{164} R_{163} R_{162} R_{161} R_{160}	17
Dummy Input	Dummy Input	10001	R_{175} R_{174} R_{173} R_{172} R_{171} R_{170}	18
Dummy Input	Dummy Input	10010	R_{185} R_{184} R_{183} R_{182} R_{181} R_{180}	19
Dummy Input	Dummy Input	10011	R_{195} R_{194} R_{193} R_{192} R_{191} R_{190}	20
Dummy Input	Dummy Input	10100	R_{205} R_{204} R_{203} R_{202} R_{201} R_{200}	21
Dummy Input	Dummy Input	10101	R_{215} R_{214} R_{213} R_{212} R_{211} R_{210}	22
Dummy Input	Dummy Input	10110	R_{225} R_{224} R_{223} R_{222} R_{221} R_{220}	23
Dummy Input	Dummy Input	10111	R_{235} R_{234} R_{233} R_{232} R_{231} R_{230}	24
Dummy Input	Dummy Input	11000	R_{245} R_{244} R_{243} R_{242} R_{241} R_{240}	25
Dummy Input	Dummy Input	11001	R_{255} R_{254} R_{253} R_{252} R_{251} R_{250}	26
Dummy Input	Dummy Input	11010	R_{265} R_{264} R_{263} R_{262} R_{261} R_{260}	27
Dummy Input	Dummy Input	11011	R_{275} R_{274} R_{273} R_{272} R_{271} R_{270}	28
Dummy Input	Dummy Input	11100	R_{285} R_{284} R_{283} R_{282} R_{281} R_{280}	29
Dummy Input	Dummy Input	11101	R_{295} R_{294} R_{293} R_{292} R_{291} R_{290}	30
Dummy Input	Dummy Input	11110	R_{305} R_{304} R_{303} R_{302} R_{301} R_{300}	31
Dummy Input	Dummy Input	11111	R_{315} R_{314} R_{313} R_{312} R_{311} R_{310}	32

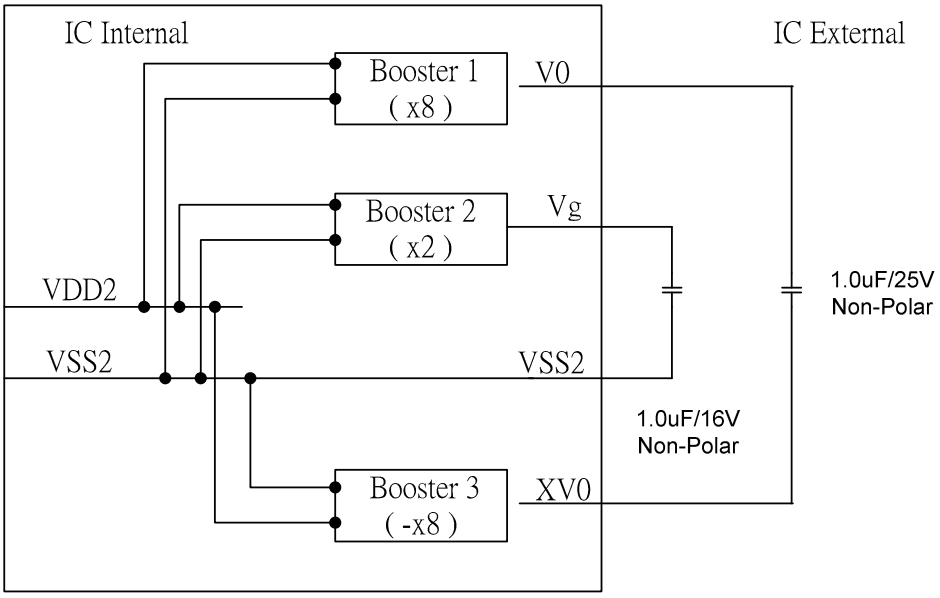
G input (3bit) 256 colours 8 bit/pixel mode	G input (4bit) 4,096 colors 12 bit/pixel -mode	G input (6 bit) 65,536 colours 16 bit/pixel -mode	G output (6bit) 262,144 colours 18 bit/pixel -mode	RGBSET Parameter
000	0000	000000	G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}	33
001	0001	000001	G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}	34
010	0010	000010	G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}	35
011	0011	000011	G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}	36
100	0100	000100	G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}	37
101	0101	000101	G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}	38
110	0110	000110	G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}	39
111	0111	000111	G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}	40
Dummy Input	1000	001000	G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}	41
Dummy Input	1001	001001	G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}	42
Dummy Input	1010	001010	G_{105} G_{104} G_{103} G_{102} G_{127} G_{100}	43
Dummy Input	1011	001011	G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}	44
Dummy Input	1100	001100	G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}	45
Dummy Input	1101	001101	G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}	46
Dummy Input	1110	001110	G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}	47
Dummy Input	1111	001111	G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}	48
Dummy Input	Dummy Input	010000	G_{165} G_{164} G_{163} G_{162} G_{161} G_{160}	49
Dummy Input	Dummy Input	010001	G_{175} G_{174} G_{173} G_{172} G_{171} G_{170}	50
Dummy Input	Dummy Input	010010	G_{185} G_{184} G_{183} G_{182} G_{181} G_{180}	51
Dummy Input	Dummy Input	010011	G_{195} G_{194} G_{193} G_{192} G_{191} G_{190}	52
Dummy Input	Dummy Input	010100	G_{205} G_{204} G_{203} G_{202} G_{201} G_{200}	53
Dummy Input	Dummy Input	010101	G_{215} G_{214} G_{213} G_{212} G_{211} G_{210}	54
Dummy Input	Dummy Input	010110	G_{225} G_{224} G_{223} G_{222} G_{221} G_{220}	55
Dummy Input	Dummy Input	010111	G_{235} G_{234} G_{233} G_{232} G_{231} G_{230}	56
Dummy Input	Dummy Input	011000	G_{245} G_{244} G_{243} G_{242} G_{241} G_{240}	57
Dummy Input	Dummy Input	011001	G_{255} G_{254} G_{253} G_{252} G_{251} G_{250}	58
Dummy Input	Dummy Input	011010	G_{265} G_{264} G_{263} G_{262} G_{261} G_{260}	59
Dummy Input	Dummy Input	011011	G_{275} G_{274} G_{273} G_{272} G_{271} G_{270}	60
Dummy Input	Dummy Input	011100	G_{285} G_{284} G_{283} G_{282} G_{281} G_{280}	61
Dummy Input	Dummy Input	011101	G_{295} G_{294} G_{293} G_{292} G_{291} G_{290}	62
Dummy Input	Dummy Input	011110	G_{305} G_{304} G_{303} G_{302} G_{301} G_{300}	63
Dummy Input	Dummy Input	011111	G_{315} G_{314} G_{313} G_{312} G_{311} G_{310}	64
Dummy Input	Dummy Input	100000	G_{325} G_{324} G_{323} G_{322} G_{321} G_{320}	65
Dummy Input	Dummy Input	100001	G_{335} G_{334} G_{333} G_{332} G_{331} G_{330}	66

Dummy Input	Dummy Input	100010	G_{345} G_{344} G_{343} G_{342} G_{341} G_{340}	67
Dummy Input	Dummy Input	100011	G_{355} G_{354} G_{353} G_{352} G_{351} G_{350}	68
Dummy Input	Dummy Input	100100	G_{365} G_{364} G_{363} G_{362} G_{361} G_{360}	69
Dummy Input	Dummy Input	100101	G_{375} G_{374} G_{373} G_{372} G_{371} G_{370}	70
Dummy Input	Dummy Input	100110	G_{385} G_{384} G_{383} G_{382} G_{381} G_{380}	71
Dummy Input	Dummy Input	100111	G_{395} G_{394} G_{393} G_{392} G_{391} G_{390}	72
Dummy Input	Dummy Input	101000	G_{405} G_{404} G_{403} G_{402} G_{401} G_{400}	73
Dummy Input	Dummy Input	101001	G_{415} G_{414} G_{413} G_{412} G_{411} G_{410}	74
Dummy Input	Dummy Input	101010	G_{425} G_{424} G_{423} G_{422} G_{421} G_{420}	75
Dummy Input	Dummy Input	101011	G_{435} G_{434} G_{433} G_{432} G_{431} G_{430}	76
Dummy Input	Dummy Input	101100	G_{445} G_{444} G_{443} G_{442} G_{441} G_{440}	77
Dummy Input	Dummy Input	101101	G_{455} G_{455} G_{453} G_{452} G_{451} G_{450}	78
Dummy Input	Dummy Input	101110	G_{465} G_{464} G_{463} G_{462} G_{461} G_{460}	79
Dummy Input	Dummy Input	101111	G_{475} G_{474} G_{473} G_{472} G_{471} G_{470}	80
Dummy Input	Dummy Input	110000	G_{485} G_{484} G_{483} G_{482} G_{481} G_{480}	81
Dummy Input	Dummy Input	110001	G_{495} G_{494} G_{493} G_{492} G_{491} G_{490}	82
Dummy Input	Dummy Input	110010	G_{505} G_{504} G_{503} G_{502} G_{501} G_{500}	83
Dummy Input	Dummy Input	110011	G_{515} G_{514} G_{513} G_{512} G_{511} G_{510}	84
Dummy Input	Dummy Input	110100	G_{525} G_{524} G_{523} G_{522} G_{521} G_{520}	85
Dummy Input	Dummy Input	110101	G_{535} G_{534} G_{533} G_{532} G_{531} G_{530}	86
Dummy Input	Dummy Input	110110	G_{545} G_{544} G_{543} G_{542} G_{541} G_{540}	87
Dummy Input	Dummy Input	110111	G_{555} G_{554} G_{553} G_{552} G_{551} G_{550}	88
Dummy Input	Dummy Input	111000	G_{565} G_{564} G_{563} G_{562} G_{561} G_{560}	89
Dummy Input	Dummy Input	111001	G_{575} G_{574} G_{573} G_{572} G_{571} G_{570}	90
Dummy Input	Dummy Input	111010	G_{585} G_{584} G_{583} G_{582} G_{581} G_{580}	91
Dummy Input	Dummy Input	111011	G_{595} G_{594} G_{593} G_{592} G_{591} G_{590}	92
Dummy Input	Dummy Input	111100	G_{605} G_{604} G_{603} G_{602} G_{601} G_{600}	93
Dummy Input	Dummy Input	111101	G_{615} G_{614} G_{613} G_{612} G_{611} G_{610}	94
Dummy Input	Dummy Input	111110	G_{625} G_{624} G_{623} G_{622} G_{621} G_{620}	95
Dummy Input	Dummy Input	111111	G_{635} G_{634} G_{633} G_{632} G_{631} G_{630}	96

B input (2bit) 256 colours 8 bit/pixel mode	B input (4bit) 4,096 colors 12 bit/pixel -mode	B input (5 bit) 65,536 colours 16 bit/pixel -mode	B output (6bit) 262,144 colours 18 bit/pixel -mode	RGBSET Parameter
00	0000	00000	B_{005} B_{004} B_{003} B_{002} B_{001} B_{000}	97
01	0001	00001	B_{015} B_{014} B_{013} B_{012} B_{011} B_{010}	98
10	0010	00010	B_{025} B_{024} B_{023} B_{022} B_{021} B_{020}	99
11	0011	00011	B_{035} B_{034} B_{033} B_{032} B_{031} B_{030}	100
Dummy Input	0100	00100	B_{045} B_{044} B_{043} B_{042} B_{041} B_{040}	127
Dummy Input	0101	00101	B_{055} B_{054} B_{053} B_{052} B_{051} B_{050}	102
Dummy Input	0110	00110	B_{065} B_{064} B_{063} B_{062} B_{061} B_{060}	103
Dummy Input	0111	00111	B_{075} B_{074} B_{073} B_{072} B_{071} B_{070}	104
Dummy Input	1000	01000	B_{085} B_{084} B_{083} B_{082} B_{081} B_{080}	105
Dummy Input	1001	01001	B_{095} B_{094} B_{093} B_{092} B_{091} B_{090}	106
Dummy Input	1010	01010	B_{105} B_{104} B_{103} B_{102} B_{127} B_{100}	107
Dummy Input	1011	01011	B_{115} B_{114} B_{113} B_{112} B_{111} B_{110}	108
Dummy Input	1100	01100	B_{125} B_{124} B_{123} B_{122} B_{121} B_{120}	109
Dummy Input	1101	01101	B_{135} B_{134} B_{133} B_{132} B_{131} B_{130}	110
Dummy Input	1110	01110	B_{145} B_{144} B_{143} B_{142} B_{141} B_{140}	111
Dummy Input	1111	01111	B_{155} B_{154} B_{153} B_{152} B_{151} B_{150}	112
Dummy Input	Dummy Input	10000	B_{165} B_{164} B_{163} B_{162} B_{161} B_{160}	113
Dummy Input	Dummy Input	10001	B_{175} B_{174} B_{173} B_{172} B_{171} B_{170}	114
Dummy Input	Dummy Input	10010	B_{185} B_{184} B_{183} B_{182} B_{181} B_{180}	115
Dummy Input	Dummy Input	10011	B_{195} B_{194} B_{193} B_{192} B_{191} B_{190}	116
Dummy Input	Dummy Input	10100	B_{205} B_{204} B_{203} B_{202} B_{201} B_{200}	117
Dummy Input	Dummy Input	10101	B_{215} B_{214} B_{213} B_{212} B_{211} B_{210}	118
Dummy Input	Dummy Input	10110	B_{225} B_{224} B_{223} B_{222} B_{221} B_{220}	119
Dummy Input	Dummy Input	10111	B_{235} B_{234} B_{233} B_{232} B_{231} B_{230}	120
Dummy Input	Dummy Input	11000	B_{245} B_{244} B_{243} B_{242} B_{241} B_{240}	121
Dummy Input	Dummy Input	11001	B_{255} B_{254} B_{253} B_{252} B_{251} B_{250}	122
Dummy Input	Dummy Input	11010	B_{265} B_{264} B_{263} B_{262} B_{261} B_{260}	123
Dummy Input	Dummy Input	11011	B_{275} B_{274} B_{273} B_{272} B_{271} B_{270}	124
Dummy Input	Dummy Input	11100	B_{285} B_{284} B_{283} B_{282} B_{281} B_{280}	125
Dummy Input	Dummy Input	11101	B_{295} B_{294} B_{293} B_{292} B_{291} B_{290}	126
Dummy Input	Dummy Input	11110	B_{305} B_{304} B_{303} B_{302} B_{301} B_{300}	127
Dummy Input	Dummy Input	11111	B_{315} B_{314} B_{313} B_{312} B_{311} B_{310}	128

7.9 Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". The diagram as below shows the referenced combinations in using Power Supply circuits.



DC/DC Booster Block Diagram

7.9.1 Voltage Regulator Circuits

There is a built-in voltage regulator circuits in ST7669 for generating V0. After internal voltage is regulated by voltage regulator circuit, V0 is generated. Detail explanation of V0 set is listed below:

◆ **SET V0 (Temperatue = 24℃)**

V0=3.6+{Vop[8:0] + VopOffset[8:0]+ (EV[6:0]-3Fh)}x0.04 (V)

Example1(V0 setting>12V):

Vop[8:0]=011010010 (D2h)

VopOffset[8:0]=0 00111001 (039h)

EV[6:0]=0111111 (3Fh)

V0=3.6 + { 210 + 57 + (63-63) } x 0.04 =14.28 (V)

Example2(V0 setting<12V):

Vop[8:0]=011010010 (D2h)

VopOffset [8:0]=1 11001110 (1CEh)

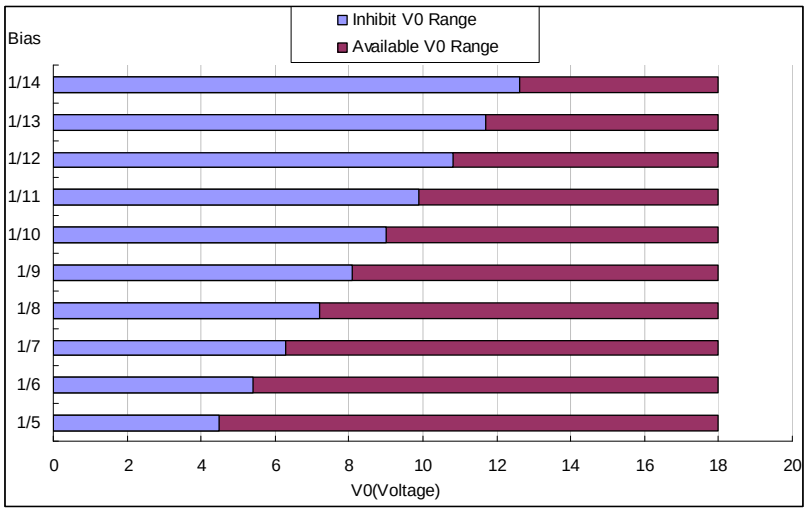
EV[6:0]=0111111 (3Fh)

V0=3.6 + { 210 -50 + (63-63) } x 0.04 =10 (V)

V0 restriction:

Because Vg should larger than 1.8V, ST7669 V0 value should be higher than 1.8 x Bias / 2 (V) and lower than 18V. V0 value outside the available range is undefined. Users has to ensure while selecting the temperature compensation that under all conditions and including all tolerances that the V0 voltage remains in the range.

	V0 setting	
	Min	**Max**
1/5	4.5	18.0
1/6	5.4	18.0
1/7	6.3	18.0
1/8	7.2	18.0
1/9	8.1	18.0
1/10	9.0	18.0
1/11	9.9	18.0
1/12	10.8	18.0
1/13	11.7	18.0
1/14	12.6	18.0



◆ **SET V0 with temperature compansation (Temperatue ≠ 24℃)**

There are 16-line slope in each temperature steps and customer can select one line slope of temperature compensation coefficiency for each temperature step. Each temperature step is 8°C. Please see Figure 7.9-1 as below.

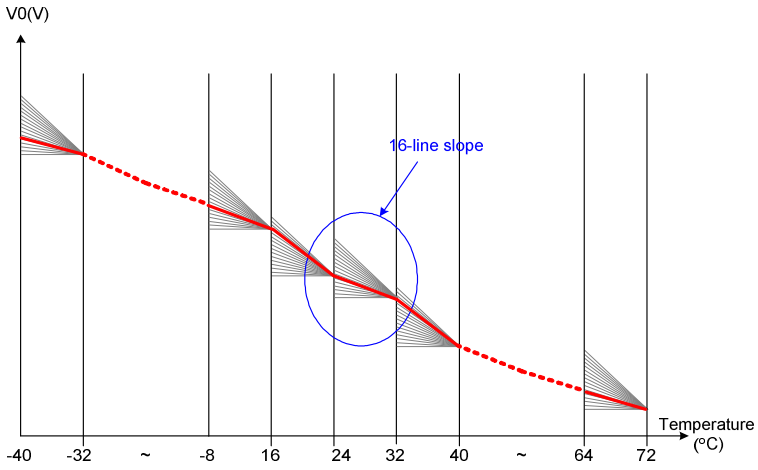
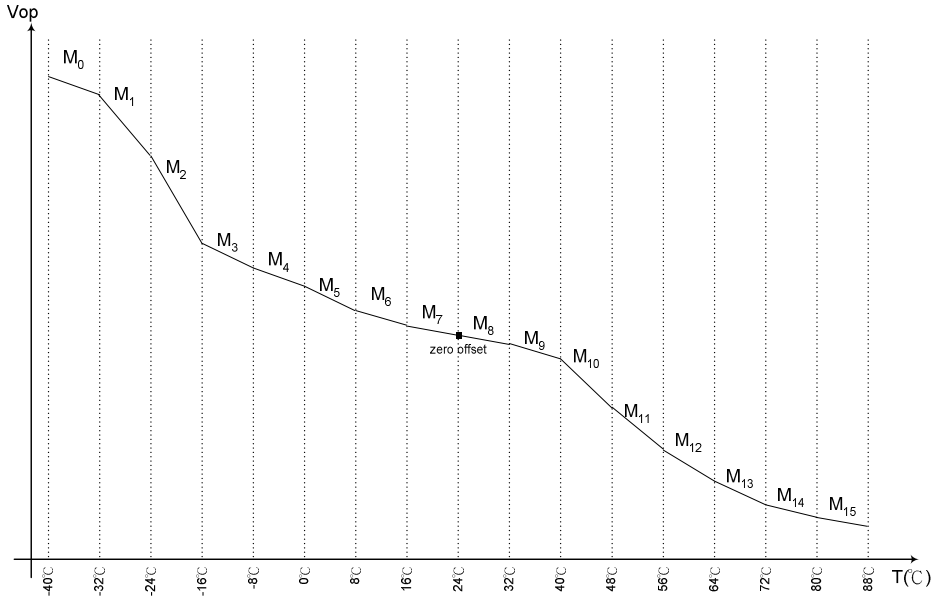


Figure 7.9-1

In command TEMPSET each MTx, where x=0, 1, 2,…, E, F, has a value between 0 and 15. MTx = 0 results in 0V increment on V0, MTx = 1 results in Mx=5mV increment, MTx = 15 results in Mx=15x5mV=75mV increment. Note that each MTx individually corresponds to a temperature interval; The relations between Mx and V0 quantity due to temperature V0(T) are described in the equations shown as follows:

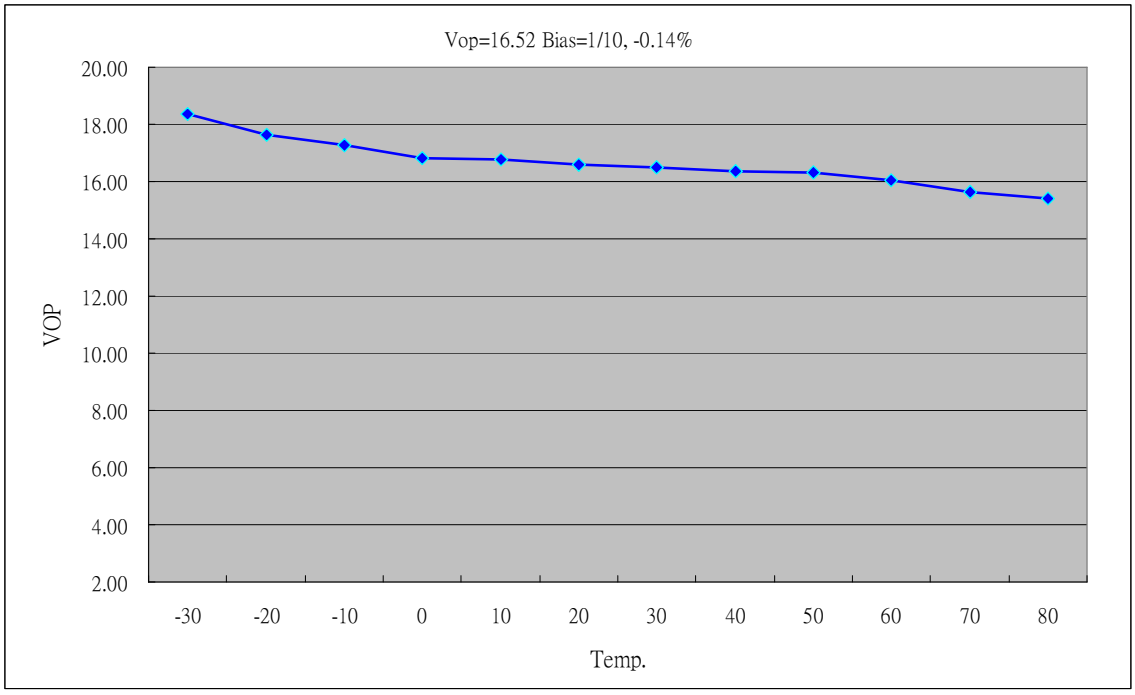
Temperature range	Equation V0(V) at temperature=T℃
-40℃ ≦ T ＜ -32℃	$V0(T) = V0(T_{24})+ (-32-T) \cdot M0 +(M1 + M2 + M3 + M4 + M5 + M6 + M7) \cdot 8$
-32℃ ≦ T ＜ -24℃	$V0(T) = V0(T_{24})+ (-24-T) \cdot M1 +(M2 + M3 + M4 + M5 + M6 + M7) \cdot 8$
-24℃ ≦ T ＜ -16℃	$V0(T) = V0(T_{24})+ (-16-T) \cdot M2 +(M3 + M4 + M5 + M6 + M7) \cdot 8$
-16℃ ≦ T ＜ -8℃	$V0(T) = V0(T_{24})+ (-8-T) \cdot M3 +(M4 + M5 + M6 + M7) \cdot 8$
-8℃ ≦ T ＜ 0℃	$V0(T) = V0(T_{24})+ (0-T) \cdot M4 +(M5 + M6 + M7) \cdot 8$
0℃ ≦ T ＜ 8℃	$V0(T) = V0(T_{24})+ (8-T) \cdot M5 +(M6 + M7) \cdot 8$
8℃ ≦ T ＜ 16℃	$V0(T) = V0(T_{24})+ (16-T) \cdot M6 + M7 \cdot 8$
16℃ ≦ T ＜ 24℃	$V0(T) = V0(T_{24})+ (24-T) \cdot M7$
24℃ ≦ T ＜ 32℃	$V0(T) = V0(T_{24}) - (T-24) \cdot M8$
32℃ ≦ T ＜ 40℃	$V0(T) = V0(T_{24}) - (T-32) \cdot M9 - M8 \cdot 8$
40℃ ≦ T ＜ 48℃	$V0(T) = V0(T_{24}) - (T-40) \cdot M10 - (M9 + M8) \cdot 8$
48℃ ≦ T ＜ 56℃	$V0(T) = V0(T_{24}) - (T-48) \cdot M11 - (M10 + M9 + M8) \cdot 8$
56℃ ≦ T ＜ 64℃	$V0(T) = V0(T_{24}) - (T-56) \cdot M12 - (M11 + M10 + M9 + M8) \cdot 8$
64℃ ≦ T ＜ 72℃	$V0(T) = V0(T_{24}) - (T-64) \cdot M13 - (M12 + M11 + M10 + M9 + M8) \cdot 8$
72℃ ≦ T ＜ 80℃	$V0(T) = V0(T_{24}) - (T-72) \cdot M14 - (M13 + M12 + M11 + M10 + M9 + M8) \cdot 8$
80℃ ≦ T ＜ 88℃	$V0(T) = V0(T_{24}) - (T-80) \cdot M15 - (M14 + M13 + M12 + M11 + M10 + M9 + M8) \cdot 8$



◆ The Example of TC Function

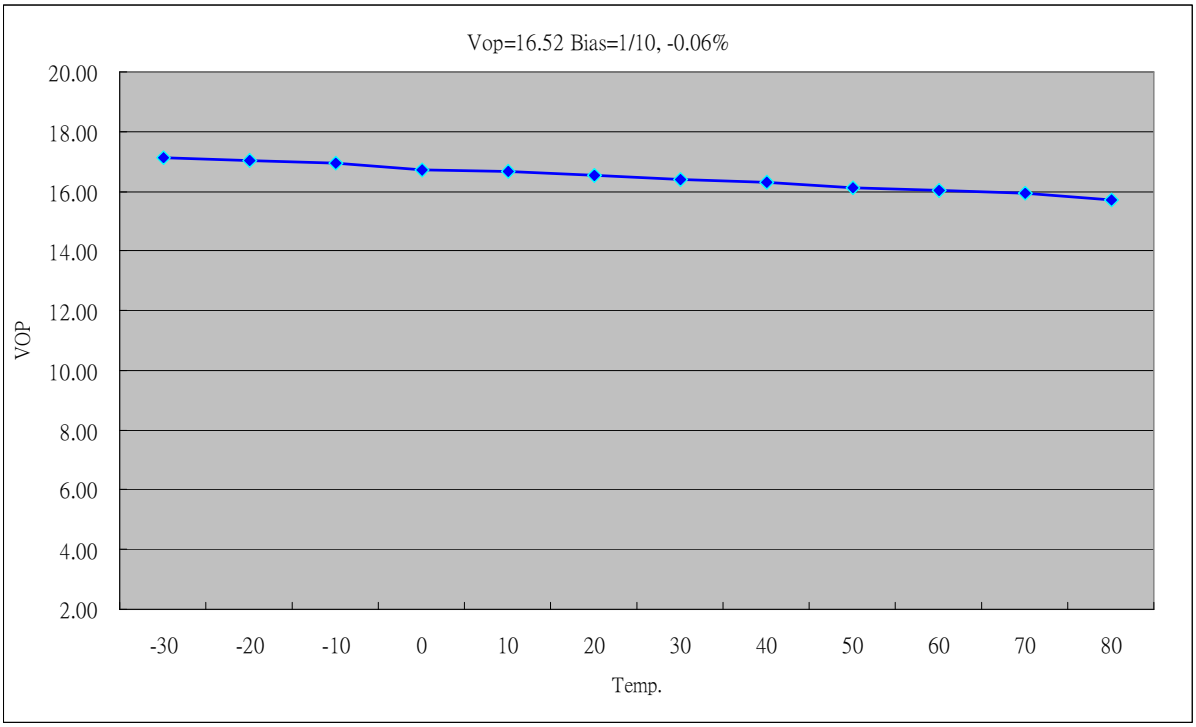
(1) Setting example for default TC curve

COMMAND	
0xF4	
DATA	
1st: 0Xff	2nd: 0x2F
3rd: 0x0A	4th: 0x35
5th: 0x31	6th: 0x40
7th: 0xA7	8th: 0x13



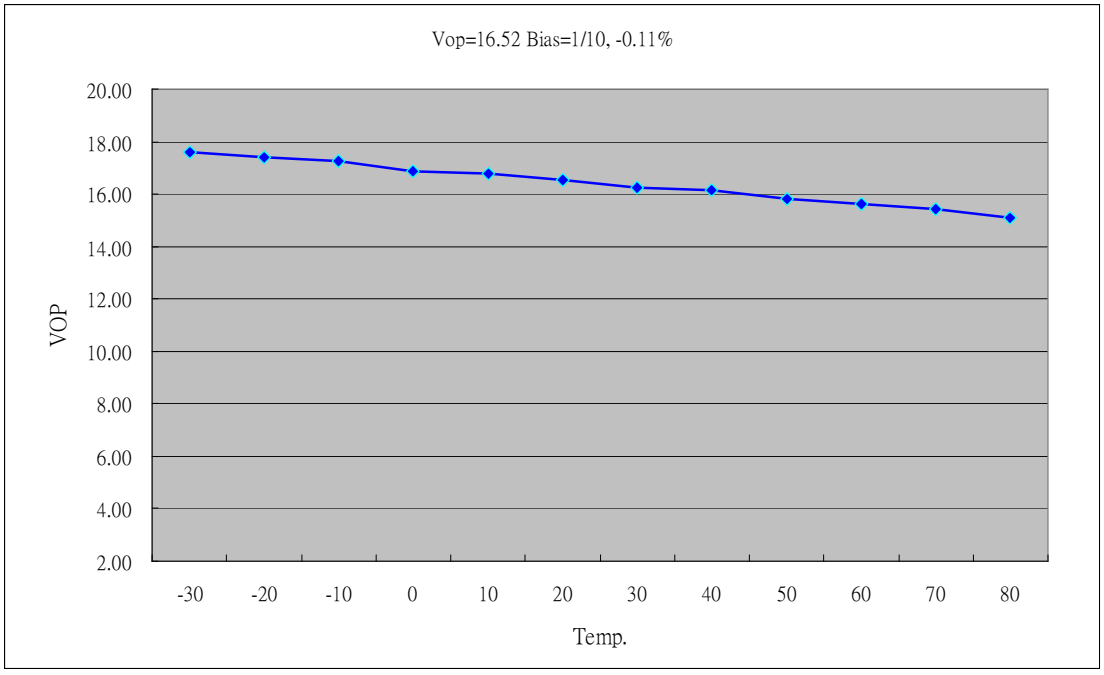
(2) Setting example for -0.06%/℃ TC curve

COMMAND	
0xF4	
DATA	
1st: 0x05	2nd: 0x05
3rd: 0x05	4th: 0x05
5th: 0x05	6th: 0x05
7th: 0x05	8th: 0x05



(3) Setting example for -0.11%/℃ TC curve

COMMAND	
0xF4	
DATA	
1st: 0x09	2nd: 0x09
3rd: 0x09	4th: 0x09
5th: 0x09	6th: 0x09
7th: 0x09	8th: 0x09



◆ **V0 fine tuning**

ST7669 has 2 commands for fine tuning V0. These commands are VopOfsetInc (see section 9.1.48) and VopOfsetDec (see section 9.1.49). When writing VopOfsetInc into IC for each time, V0 would increase 40mV; when writing VopOfsetDec into IC for each time, V0 would decrease 40mV.

Example:

Vop[8:0]=011010010

VopOffSet[7:0]=00111001

EV[6:0]=0111111

VopOfsetInc x2

→ V0=3.6 + { 210 + 57 + (63-63) } x 0.04 + 0.04x2 =14.36 (V)

7.9.2 Voltage Follower Circuits

There is a build-in voltage follower circuits in ST7669 for generating Vg and Vm. These voltages are decided by bias ratio selection circuitry which is set by users with software to control 1/5 to 1/14 bias ratios to match the optimum display performance of LCD panel. Bias driving rule is listed below:

LCD bias	Vg	Vm
1/N bias	(2/N) x V0	(1/N) x V0

N=5 to 14

7.9.3 OTP Setting Flow

ST7669 provides the Write and Read function to write the electronic control value and built-in resistance ratio into OTP (One-time programming register), and then read them from it. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attention the setting procedure. Please see the following diagram.

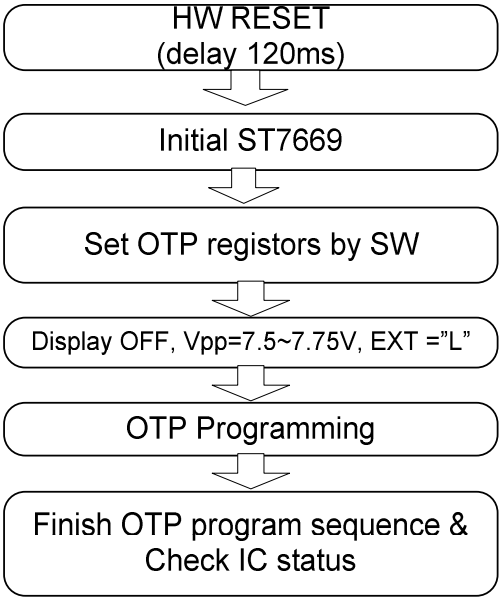


Figure 7.9-2 OTP programming flow

Note1: This setting flow is used for LCM assembler.

Note2: OTP shouldn't be written without preceding loading correctly from OTP in order to avoid some errors during IC operation.

Note3: When writing to OTP, the voltage of VPP must be 7.50~7.75V; the current of Ivpp must be more than 4 mA.

Note4: If the OTP is exposed to a high temperature for hours, data in the memory cell may probably be lost before the data retention guarantee period. To retain data in the memory cell, keep the memory cell below 90℃. The data retention guarantee period is specified including the retention period.

7.10 Frequency Temperature Gradient Compensation Coefficient

7.10.1 Register loading Detection

ST7669 will auto-switch frame rate on different temperature such as Figure 7.10-1. TA, TB and TC are frame rate switching temperatures which can be defined by customer with command TMPRNG. FA, FB, FC and FD are switched frame rate which also can be defined by customer with command FRMSEL. The frame rate range is from 37.5Hz to 170Hz.

When the temperature is in increasing state, frame rate changes to the higher step at TA/TB/TC+TH(℃). When the temperature is in decreasing state, frame rate changes to the lower step at TA/TB/TC. For example: TC=10℃ and TH=5℃, FC switches to FD at 15℃ but FD switches to FC at 10℃. Please take Figure 7.10-1 for reference.

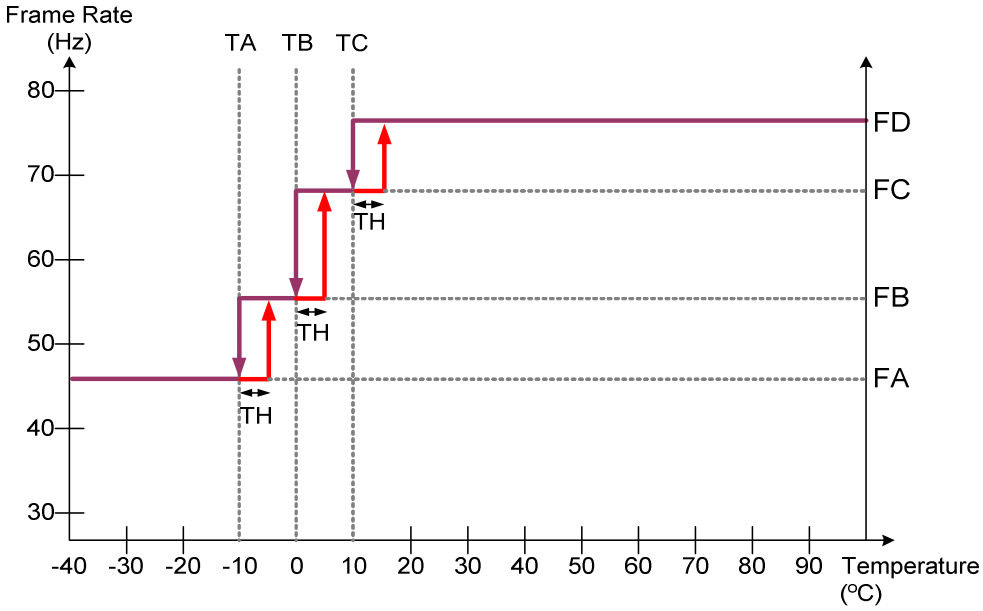


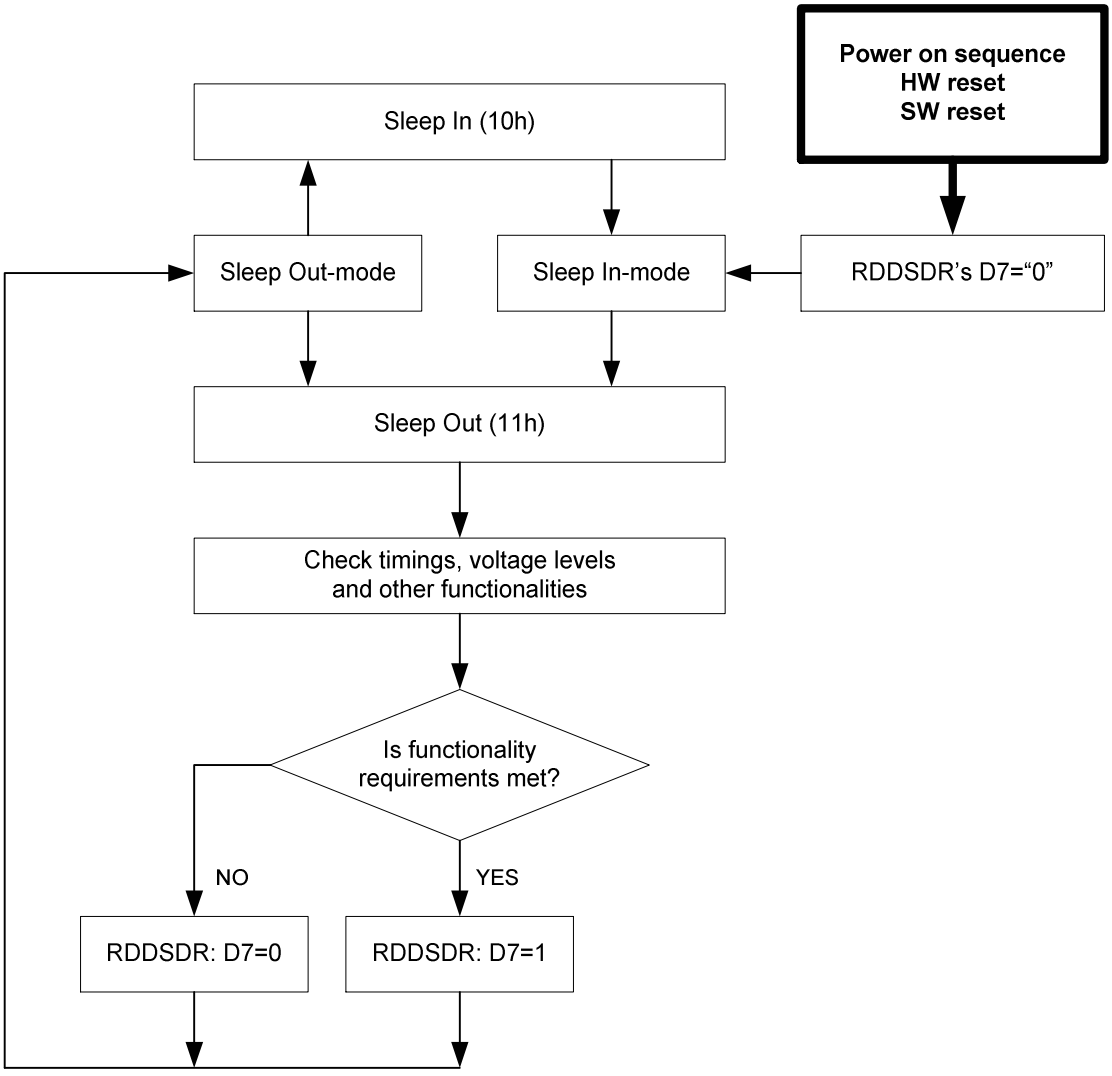
Figure 7.10-1

7.11 Sleep Out –Command and Self-Diagnostic Functions of the Display Module

7.11.1 Register loading Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP ROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the OTP ROM and register values of the display controller by the display controller (1st step: compare register and OTP ROM values, 2nd step: loads OTP ROM values to registers). If those both values (OTP ROM and register values) are same, bit-7 of RDDSDR is set to 1, which is defined in command RDDSDR (The used bit of this command is D7). If those both values are not same, this bit (D7) is set to 0.The flow chart for this internal function is following:

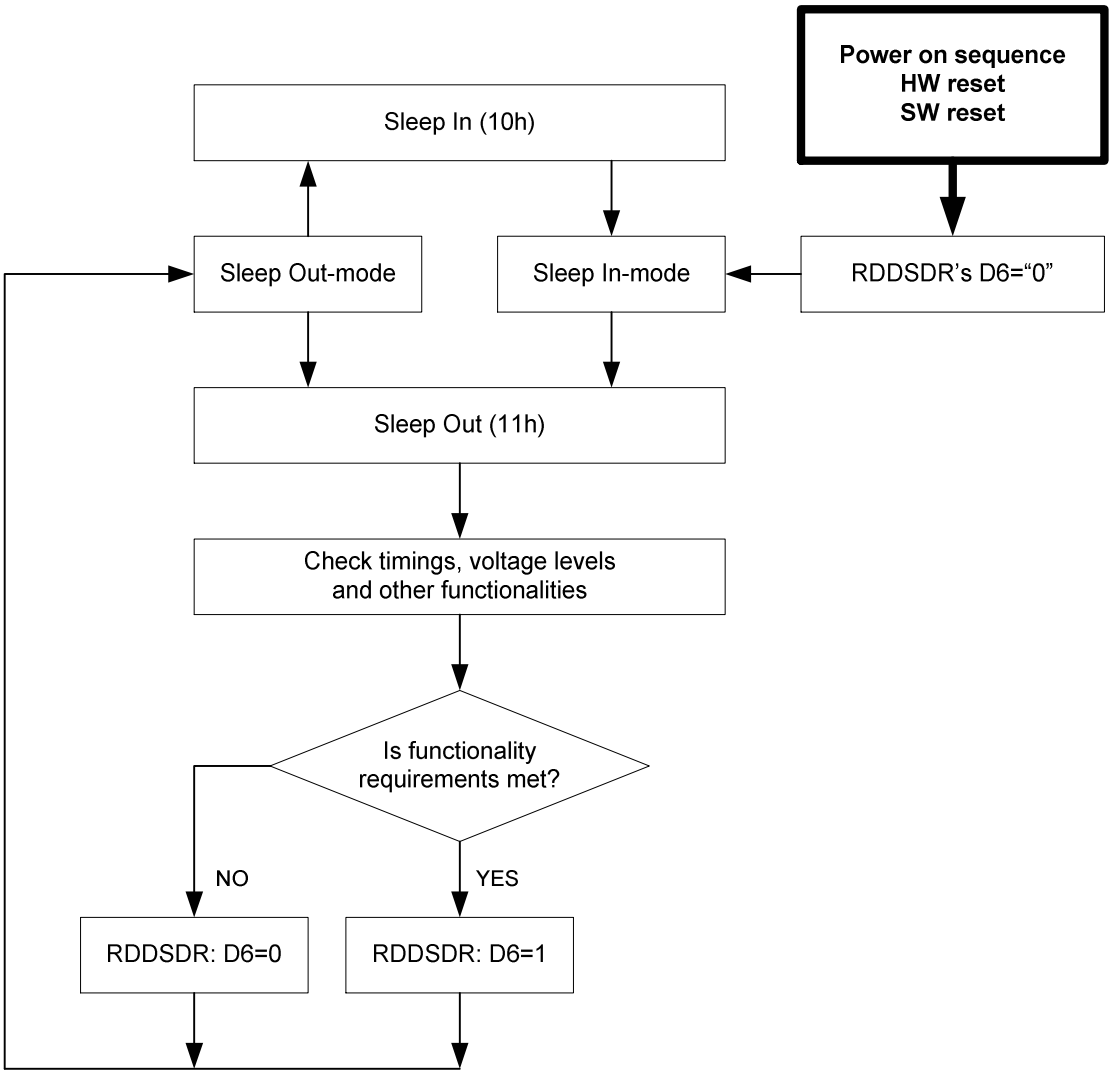


7.11.2 Functionality Detection

Sleep Out-command is a trigger for an internal function of the display module.

The internal function (= the display controller) is comparing if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, bit-6 of RDDSDR is set to 1, which defined in command Read Display Self-Diagnostic Result (RDDSDR). The used bit of this command is D6. If functionality requirement is not same, this bit (D6) is set to 0.

The flow chart for this internal function is following:



Note: There is needed 200msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.

7.11.3 Chip Attachment Detection (Reserved)

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if bump side of IC is attached to LCM glass ITO or not.

There is a bit, which is defined in command “Read Display Self-Diagnostic Result” (RDDSDR). The used bit of this command is D5. If IC is not attached to the circuit route of the flex or display glass, this bit (D5) is “0”. If IC is attached to the circuit route, the bit5 is “1”.

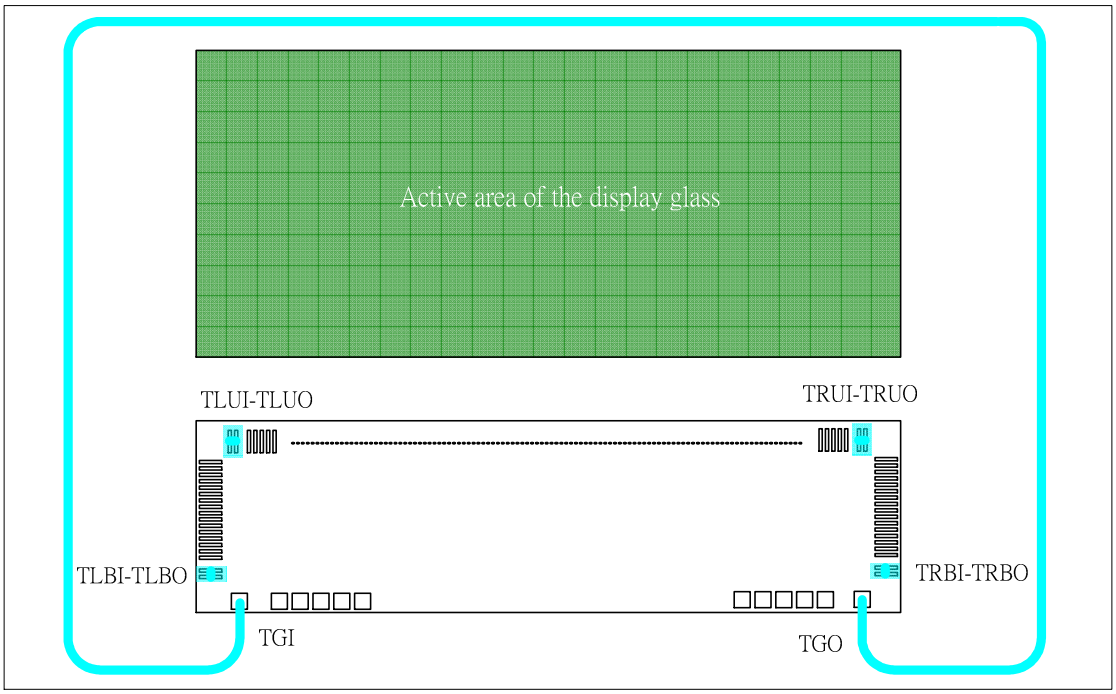
There are connected together 2 bumps via route of ITO on 4 corners of IC. TLBI connects to TLBO; TLUI connects to TLUO; TRUI connects to TRUO; TRBI connects to TRBO.

7.11.4 LCM Glass Detection (Reserved)

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display glass of the display module is broken or not.

There is a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR).The used bit of this command is D4. If this display glass is broken, this bit (D4) is “0”. If this display glass is OK, this bit (D4) is “1”.

The following figure is a reference of how this glass break detection can be implemented. For example, there is connected together 2 bumps(TGI and TGO) via route of ITO. This route of ITO is the nearest route of the edge of the display glass.



8 RESET CIRCUIT

The registers that are initialized are listed below.

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory (RAM data)	Random	No Change	No Change
RDDID	TBD	TBD	TBD
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	06h (18-Bit/Pixel)	06h (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
Sleep In/Out	In	In	In
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
All Pixel Off mode	Disable	Disable	Disable
All Pixel On mode	Disable	Disable	Disable
Contrast (EV)	3Fh	3Fh	3Fh
Display On/Off	Display Off	Display Off	Display Off
Column: Start Address (XS)	00h	00h	00h
Column: End Address (XE)	83h	83h	83h (when MV=0) A1h (when MV=1)
Row: Start Address (YS)	00h	00h	00h
Row: End Address (YE)	A1h	A1h	A1h (when MV=0) 83h (when MV=1)
Color set	Random	Random	Contents of the look-up table protected
Partial: Start Address (PS)	00h	00h	00h
Partial: End Address (PE)	A1h	A1h	A1h
Scroll: Top Fixed Area (TFA)	00h	00h	00h
Scroll: Scroll Area (VSA)	A2h	A2h	A2h
Scroll: Bottom Fixed Area (BFA)	00h	00h	00h
TE On/Off	Off	Off	Off
TE Mode	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control MY/MX/MV/ML/RGB)	0/0/0/0/0	No Change	No Change
Scroll Start Address (SSA)	00h	00h	00h
Idle Mode On/Off	Off	Off	Off
Interface Color Pixel Format (P)	06h (18Bit/Pixel)	06h (18Bit/Pixel)	No change
ID1	TBD	TBD	TBD
ID2	TBD	TBD	TBD
ID3	TBD	TBD	TBD
Drive Duty	A1h	A1h	A1h
First Common	00h	00h	00h
FOSC Divider	No division	No division	No division
Common scan direction	0→80, 81→161	0→80, 81→161	0→80, 81→161
Vop	042h, 01h	042h, 01h	042h, 01h
Vop Offset increase/decrease	Disable	disable	disable

Item	After Power On	After Hardware Reset	After Software Reset
Bias	1/11 Bias	1/11 Bias	1/11 Bias
Booster setting	8x	8x	8x
Booster Efficiency	01b	01b	01b
Vg source	From VDD2x2	From VDD2x2	From VDD2x2
EPCTIN	0	0	0
OTP selection	Disable	Disable	Disable
Frame Frequency in Normal Color (FA/FB/FC/FD)	46Hz/61.5Hz/72Hz/77Hz	46Hz/61.5Hz/72Hz/77Hz	46Hz/61.5Hz/72Hz/77Hz
Frame Frequency in 8-Color (Idle) (F8A/F8B/F8C/F8D)	46Hz/61.5Hz/72Hz/77Hz	46Hz/61.5Hz/72Hz/77Hz	46Hz/61.5Hz/72Hz/77Hz
Temperature Range (TA/TB/TC)	10℃/10℃/10℃	10℃/10℃/10℃	10℃/10℃/10℃
Temperature Hysteresis (TH)	5℃	5℃	5℃
TEMPSEL	0 mV/℃	0 mV/℃	0 mV/℃

9 COMMANDS

9.1 INSTRUCTION TABLE

Command Table-1 , /EXT= H or L

Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(00h)	NOP	0	1	0	0	0	0	0	0	0	0	0	No Operation	9.1.1
(01h)	SWRESET	0	1	0	0	0	0	0	0	0	0	1	Software reset	9.1.2
(04h)	RDDID	0	1	0	0	0	0	0	0	1	0	0	Read Display ID	9.1.3
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	ID1 read (D23-D16)	
-		1	0	1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	ID2 read (D15-D8)	
-		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	ID3 read (D7-D0)	
(09h)	RDDST	0	1	0	0	0	0	0	1	0	0	1	Read Display Status	9.1.4
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	(D31-D24)	
-		1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	(D23-D16)	
-		1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	(D15-D8)	
-		1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	(D7-D0)	
(0Ah)	RDDPM	0	1	0	0	0	0	0	1	0	1	0	Read Display Power Mode	9.1.5
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	D2	0	0	-	
(0Bh)	RDDMADCTR	0	1	0	0	0	0	0	1	0	1	1	Read Display MADCTR	9.1.6
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	0	0	0	-	
(0Ch)	RDDCOLMOD	0	1	0	0	0	0	0	1	1	0	0	Read Display Pixel Format	9.1.7
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	0	0	0	0	0	D2	D1	D0	-	
(0Dh)	RDDIM	0	1	0	0	0	0	0	1	1	0	1	Read Display Image Mode	9.1.8
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	0	D5	D4	D3	0	0	0	-	
(0Eh)	RDDSM	0	1	0	0	0	0	0	1	1	1	0	Read Display signal Mode	9.1.9
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	0	0	0	0	0	0	-	
(0Fh)	RDDSDR	0	1	0	0	0	0	0	1	1	1	1	Read Display Self-diagnostic result	9.1.10
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	D7	D6	D5	D4	0	0	0	0	-	

Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(10h)	SLPIN	0	1	0	0	0	0	1	0	0	0	0	Sleep in & booster off	9.1.11
(11h)	SLPOUT	0	1	0	0	0	0	1	0	0	0	1	Sleep out & booster on	9.1.12
(12h)	PTLON	0	1	0	0	0	0	1	0	0	1	0	Partial mode on	9.1.13
(13h)	NORON	0	1	0	0	0	0	1	0	0	1	1	Partial off (Normal)	9.1.14
(20h)	INVOFF	0	1	0	0	0	1	0	0	0	0	0	Display inversion off (normal)	9.1.15
(21h)	INVON	0	1	0	0	0	1	0	0	0	0	1	Display inversion on	9.1.16
(22h)	APOFF	0	1	0	0	0	1	0	0	0	1	0	All pixel off (Only for test purpose)	9.1.17
(23h)	APON	0	1	0	0	0	1	0	0	0	1	1	All pixel on (Only for test purpose)	9.1.18
(25h)	WRCNTR	0	1	0	0	0	1	0	0	1	0	1	Write contrast	9.1.19
-		1	1	0	0	EV6	EV5	EV4	EV3	EV2	EV1	EV0	EV = 0 to 127	
(28h)	DISPOFF	0	1	0	0	0	1	0	1	0	0	0	Display off	9.1.20
(29h)	DISPON	0	1	0	0	0	1	0	1	0	0	1	Display on	9.1.21
(2Ah)	CASET	0	1	0	0	0	1	0	1	0	1	0	Column address set	9.1.22
		1	1	0	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	X_ADR start: 0≦XS≦83h	
		1	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
		1	1	0	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	X_ADR end: XS≦XE ≦83h	
		1	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
(2Bh)	RASET	0	1	0	0	0	1	0	1	0	1	1	Row address set	9.1.23
		1	1	0	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	Y_ADR start: 0≦YS≦A1h	
		1	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
		1	1	0	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	Y_ADR end: YS≦YE≦A1h	
		1	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
(2Ch)	RAMWR	0	1	0	0	0	1	0	1	1	0	0	Memory write	9.1.24
		1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data	
(2Dh)	RGBSET	0	1	0	0	0	1	0	1	1	0	1	Color set for 256.4k.65K color display	9.1.25
-		1	1	0	-	-	R5	R4	R3	R2	R1	R0	Red tone (00000)	
-		1	1	0	:	:	:	:	:	:	:	:	: -	
-		1	1	0	-	-	R5	R4	R3	R2	R1	R0	Red tone (11111)	
-		1	1	0	-	-	G5	G4	G3	G2	G1	G0	Green tone (000000)	
		1	1	0	:	:	:	:	:	:	:	:	: -	
		1	1	0	-	-	G5	G4	G3	G2	G1	G0	Green tone (111111)	
		1	1	0	-	-	B5	B4	B3	B2	B1	B0	Blue tone (00000)	
		1	1	0	:	:	:	:	:	:	:	:	: -	
		1	1	0	-	-	B5	B4	B3	B2	B1	B0	Blue tone (11111)	

Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(2Eh)	RAMRD	0	1	0	0	0	1	0	1	1	1	0	Memory Read	9.1.26
		1	1	0	-	-	-	-	-	-	-	-		
		1	1	0	D7	D6	D5	D4	D3	D2	D1	D0		
(30h)	PTLAR	0	1	0	0	0	1	1	0	0	0	0	Partial start/end address set	9.1.27
-		1	1	0	PS15	PS14	PS13	PS12	PS11	PS10	PS9	PS8	Start address (0~161)	
		1	1	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0		
		1	1	0	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	End address (0~161)	
-		1	1	0	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0		
(33h)	SCRLAR	0	1	0	0	0	1	1	0	0	1	1	Scroll Area	9.1.28
-		1	1	0	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	TFA=0~162	
-		1	1	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	VSA=0~162	
-		1	1	0	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	BFA=0~162	
(34h)	TEOFF	0	1	0	0	0	1	1	0	1	0	0	Tearing effect line off	9.1.29
(35h)	TEON	0	1	0	0	0	1	1	0	1	0	1	Tearing effect mode set & on	9.1.30
-		1	1	0	-	-	-	-	-	-	-	M	“0”: mode1, “1”: mode2	
(36h)	MADCTR	0	1	0	0	0	1	1	0	1	1	0	Memory data access control	9.1.31
-		1	1	0	MY	MX	MV	ML	RGB	-	-	-	-	
(37h)	VSCSAD	0	1	0	0	0	1	1	0	1	1	1	Scroll start address of RAM	9.1.32
		1	1	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	SSA = 0~161	
(38h)	IDMOFF	0	1	0	0	0	1	1	1	0	0	0	Idle mode off	9.1.33
(39h)	IDMON	0	1	0	0	0	1	1	1	0	0	1	Idle mode on	9.1.34
(3Ah)	COLMOD	0	1	0	0	0	1	1	1	0	1	0	Interface pixel format	9.1.35
-		1	1	0	-	-	-	-	-	P2	P1	P0	Interface format	
(DAh)	RDID1	0	1	0	1	1	0	1	1	0	1	0	Read ID1	9.1.36
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	(D7-D0)	
(DBh)	RDID2	0	1	0	1	1	0	1	1	0	1	0	Read ID2	9.1.37
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	(D7-D0)	
(DCh)	RDID3	0	1	0	1	1	0	1	1	0	1	0	Read ID3	9.1.38
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	(D7-D0)	

Note 1: When /EXT connects to H or floating, commands which are not defined in “Command Table-1” are treated as NOP (00H) command.

Note 2: Commands 10H, 12H, 13H, 20H, 21H, 25H, 28H, 29H, 30H, 36H (Bit ML only), 38H and 39H are updated during V-sync when

Module is in Sleep Out Mode to avoid abnormal visual effects.

During Sleep In mode, these commands are updated immediately.

Read status (09H), Read Display Power Mode (0AH), Read Display MADCTR (0BH), Read Display Pixel Format (0CH), Read Display Image Mode (0DH), Read Display Signal Mode (0EH) and Read Display Self Diagnostic Result (0FH) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

Command Table-2 , /EXT= L

Hex	*Command*	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Function*	*Ref*
(B0h)	DutySet	0	1	0	1	0	1	1	0	0	0	0	Display Duty setting	9.1.39
		1	1	0	Du7	Du6	Du5	Du4	Du3	Du2	Du1	Du0		
(B1h)	FirstCom	0	1	0	1	0	1	1	0	0	0	1	First Com. Page address	9.1.40
		1	1	0	F7	F6	F5	F4	F3	F2	F1	F0		
(B3h)	OscDiv	0	1	0	1	0	1	1	0	0	1	1	FOSC divider	9.1.41
		1	1	0	-	-	-	-	-	-	CLD1	CLD0		
(B4h)	PTLMOD	0	1	0	1	0	1	1	0	1	0	0	Saving Power Mode Selection	9.1.42
		1	1	0	PTLM	0	0	1	1	0	0	0		
(B5h)	NLInvSet	0	1	0	1	0	1	1	0	1	0	1	N-line control	9.1.43
		1	1	0	M	N6	N5	N4	N3	N2	N1	N0		
(B7h)	ComScanDir	0	1	0	1	0	1	1	0	1	1	1	Com/Seg Scan Direction for Glass layout	9.1.44
		1	1	0	SMY	SMX	SINV	SML	SBGR	0	0	0		
(B8h)	RmwIn	0	1	0	1	0	1	1	1	0	0	0	read modify write control IN	9.1.45
(B9h)	RmwOut	0	1	0	1	0	1	1	1	0	0	1	read modify write control Out	9.1.46
(C0h)	VopSet	0	1	0	1	1	0	0	0	0	0	0	Vop setting	9.1.47
		1	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0		
		1	1	0	-	-	-	-	-	-	-	Vop8		
(C1h)	VopOfsetInc	0	1	0	1	1	0	0	0	0	0	1	+40mv/setp	9.1.48
(C2h)	VopOfsetDec	0	1	0	1	1	0	0	0	0	1	0	-40mv/setp	9.1.49
(C3h)	BiasSel	0	1	0	1	1	0	0	0	0	1	1	Bias selection	9.1.50
		1	1	0	-	-	-	-	-	Bias2	Bias1	Bias0		
(C4h)	BstBmpXSel	0	1	0	1	1	0	0	0	1	0	0	Booster setting	9.1.51
		1	1	0	-	-	-	-	-	BST2	BST 1	BST0		
(C5h)	BstEffSel	0	1	0	1	1	0	0	0	1	0	1	Booster efficiency selection	9.1.52
		1	1	0	-	-	1	0	-	-	BTF1	BTF0		
(C7h)	VopOffset	0	1	0	1	1	0	0	0	1	1	1	Vop offset fuse bit adjust	9.1.53
		1	1	0	VOS7	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0		
		1	1	0	-	-	-	-	-	-	-	VOS8		
(CBh)	VgSorcSel	0	1	0	1	1	0	0	1	0	1	1	Vg with Booster x2 control	9.1.54
		1	1	0	-	-	-	-	-	-	-	2BT0		

Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(CCh)	ID1Set	0	1	0	1	1	0	0	1	1	0	0	ID1 setting	9.1.55
		1	1	0	ID1_7	ID1_6	ID1_5	ID1_4	ID1_3	ID1_2	ID1_1	ID1_0		
(CDh)	ID2Set	0	1	0	1	1	0	0	1	1	0	1	ID2 setting	9.1.56
		1	1	0	1	ID2_6	ID2_5	ID2_4	ID2_3	ID2_2	ID2_1	ID2_0		
(CEh)	ID3Set	0	1	0	1	1	0	0	1	1	1	0	ID3 setting	9.1.57
		1	1	0	ID3_7	ID3_6	ID3_5	ID3_4	ID3_3	ID3_2	ID3_1	ID3_0		
(D0h)	ANASET	0	1	0	1	1	0	0	0	0	0	0	Analog circuit setting	9.1.58
		1	1	0	0	0	0	1	1	1	0	1		
(D7h)	AutoLoadSet	0	1	0	1	1	0	1	0	1	1	1	mask rom data auto re-load control	9.1.59
		1	1	0	EXTE	1	-	ARD	1	1	1	1		
(DEh)	RDTstStatus	0	1	0	1	1	0	1	1	1	1	0	read IC status	9.1.60
		1	0	1	-	-	-	-	-	-	-	-	Dummy Read	
(E0h)	EPCTIN	0	1	0	1	1	1	0	0	0	0	0	Control OTP WR/RD	9.1.61
		1	1	0	0	0	WR /XRD	0	0	0	0	0		
(E1h)	EPCTOUT	0	1	0	1	1	1	0	0	0	0	1	OTP control cancel	9.1.62
(E2h)	EPMWR	0	1	0	1	1	1	0	0	0	1	0	Write to OTP	9.1.63
(E3h)	EPMRD	0	1	0	1	1	1	0	0	0	1	1	Read from OTP	9.1.64
(E4h)	OTPSEL	0	1	0	1	1	1	0	0	1	0	0	Select OTP	9.1.65
		1	1	0	MS1	MS0	0	1	1	0	0	0		
(E5h)	ROMSET	0	1	0	0	1	1	1	0	1	0	1	Programmable rom setting	9.1.66
		1	1	0	0	0	0	0	1	1	1	0		
(EBh)	HPMSET	0	1	0	1	1	1	0	1	0	1	1	High power mode setting	9.1.67
		1	1	0	0	0	0	0	0	0	HP1	HP0		
		1	1	0	0	0	0	0	0	0	0	0		
(F0h)	FRMSEL	0	1	0	1	1	1	1	0	0	0	0	Frame Freq Temp range A,B,C and D	9.1.68
		1	1	0	-	-	-	FA4	FA3	FA2	FA1	FA0		
		1	1	0	-	-	-	FB4	FB3	FB2	FB1	FB0		
		1	1	0	-	-	-	FC4	FC3	FC2	FC1	FC0		
		1	1	0	-	-	-	FD4	FD3	FD2	FD1	FD0		

Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(F1h)	FRM8SEL	0	1	0	1	1	1	1	0	0	0	1	Frame Freq Temp range A,B,C and D (idle)	9.1.69
		1	1	0	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0		
		1	1	0	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0		
		1	1	0	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0		
		1	1	0	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0		
(F2h)	TMPRNG	0	1	0	1	1	1	1	0	0	1	0	Temp range A,B and C	9.1.70
		1	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0		
		1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0		
		1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0		
(F3h)	TMPHYS	0	1	0	1	1	1	1	0	0	1	1	Hysteresis value set	9.1.71
		1	1	0	-	-	-	-	TH3	TH2	TH1	TH0		
(F4h)	TEMPSEL	0	1	0	1	1	1	1	0	1	0	0	TEMPSEL	9.1.72
		1	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00		
		1	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20		
		1	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40		
		1	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60		
		1	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80		
		1	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0		
		1	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0		
		1	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0		
(F7h)	THYS	0	1	0	1	1	1	1	0	1	1	1	Temperature detection threshold	9.1.73
		1	1	0	THYS7	THYS6	THYS5	THYS4	THYS3	THYS2	THYS1	THYS0		
(F9h)	Frame Set	0	1	0	1	1	1	1	1	0	0	1	Set Frame RGB PWM value	9.1.74
		1	1	0	-	-	-	P14	P13	P12	P11	P10		
		1	1	0	-	-	-	P24	P23	P22	P21	P20		
		:	:	:	:	:	:	:	:	:	:	:		
		1	1	0	-	-	-	P154	P153	P152	P151	P150		
		1	1	0	-	-	-	P164	P163	P162	P161	P160		

9.1.1 NOP: No Operation (00H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	0	0	0	0	00H
Parameter	No parameter											

Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.
Restriction	
Register Availablility	
Default	
Flow Chart	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

9.1.2 SWRESET: Software Reset (01H)

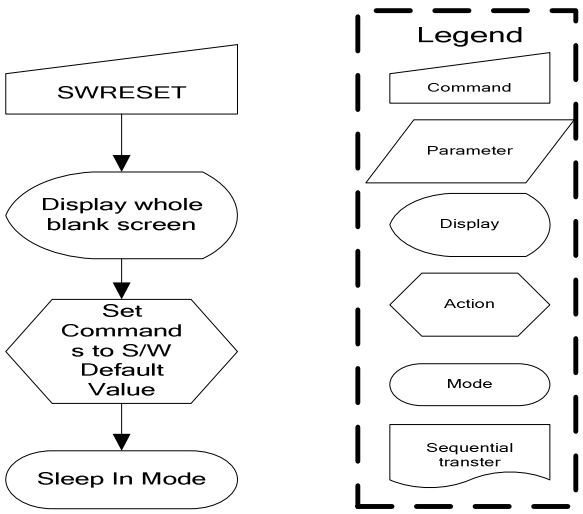
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	0	0	0	1	01H
Parameter	No parameter											

Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all segment & common outputs are set to Vm (display off: blank display). (See default tables in each command description) Note: The Frame Memory contents are unaffected by this command
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier's factory default values to the registers during 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 200msec before sending Sleep Out command. Software Reset command cannot be sent during Sleep Out sequence.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	

SWRESET
Display whole blank screen
Set Command s to S/W Default Value
Sleep In Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.3 RDDIDIF: Read Display Identification Information (04H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	0	1	0	0	04H
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
3rd parameter	1	0	1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
4th parameter	1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

Description

This read byte returns 24-bit display identification information.

1st Parameter: dummy read.

The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

The 3rd parameter (ID26 to ID20): LCD module/driver version ID

The 4th parameter (ID37 to ID30): LCD module/driver ID.

NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.

Restriction

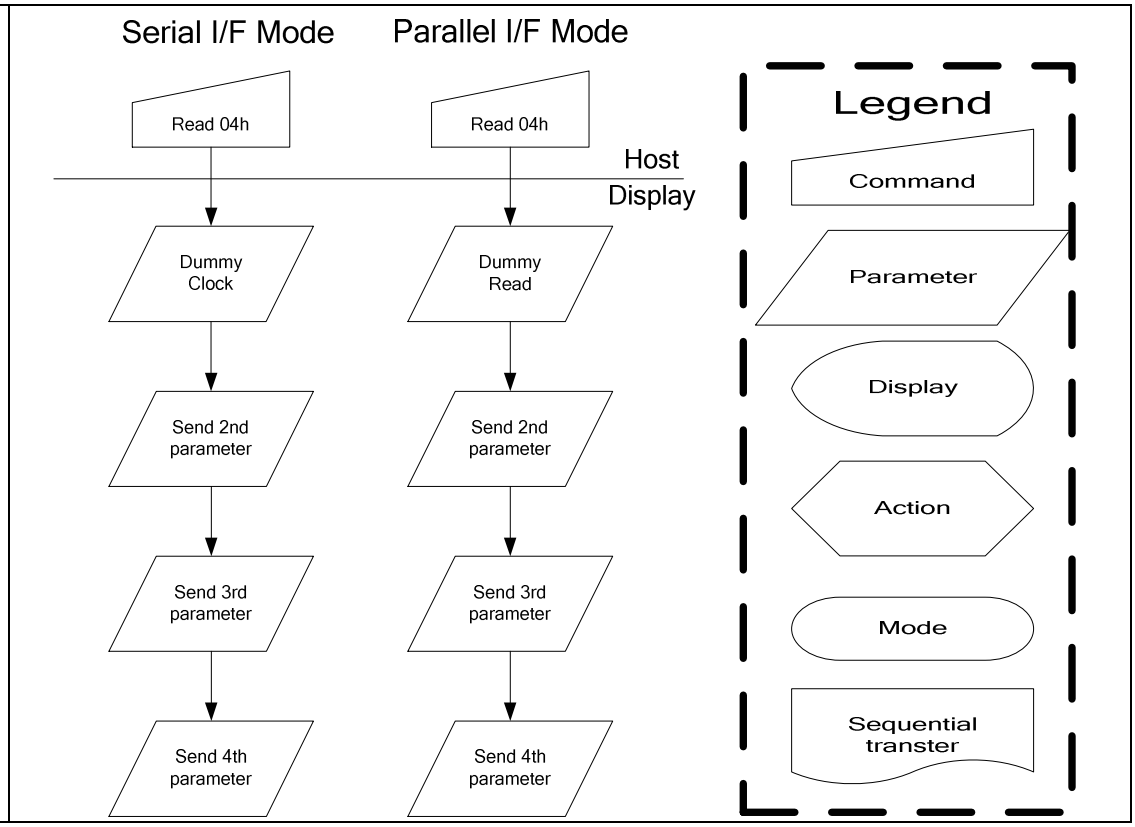
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	Not fixed	Not fixed	Not fixed
S/W Reset	Not fixed	Not fixed	Not fixed
H/W Reset	Not fixed	Not fixed	Not fixed

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read 04h
Read 04h
Host
Display
Dummy
Clock
Dummy
Read
Send 2nd
parameter
Send 2nd
parameter
Send 3rd
parameter
Send 3rd
parameter
Send 4th
parameter
Send 4th
parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential
transter

9.1.4 RDDST: Read Display Status (09H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	1	0	0	1	09H
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-
3rd parameter	1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-
4th parameter	1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-
5th parameter	1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
ST31	Booster Voltage Status	"1"=Booster on (Booster is OK), "0"=off
ST30	Row Address Order (MY)	"1"=Decrement, "0"=Increment
ST29	Column Address Order (MX)	"1"=Decrement, "0"=Increment
ST28	Row/Column Order (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
ST27	Scan Address Order (ML)	"1"=Decrement, "0"=Increment
ST26	RGB/BGR Order (RGB)	"1"=BGR, "0"=RGB
ST25	Not Used	"0"
ST24	Not Used	"0"
ST23	Not Used	"0"
ST22	Interface Color Pixel Format Definition	"010" = 8-bit / pixel, "011" = Reserve "100" = 12-bit / pixel "101" = 16-bit / pixel, "110" = 18-bit / pixel, "111" = 24-bit / pixel
ST21		
ST20		
ST19	Idle Mode On/Off	"1" = On, "0" = Off
ST18	Partial Mode On/Off	"1" = On, "0" = Off
ST17	Sleep In/Out	"1" = Out, "0" = In
ST16	Display Normal Mode On/Off	"1" = Normal Display, "0" = Partial Display
ST15	Vertical Scrolling Status	"1" = Scroll on, "0" = Scroll off
ST14	Not Used	"0"
ST13	Inversion Status	"1" = On, "0" = Off
ST12	All Pixels On	"1" = mode On, "0" = mode Off
ST11	All Pixels Off	"1" = mode On, "0" = mode Off
ST10	Display On/Off	"1" = On, "0" = Off
ST9	Tearing effect line on/off	"1" = On, "0" = Off
ST8	Not Used	"0"
ST7	Not Used	"0"
ST6	Not Used	"0"
ST5	Tearing effect line mode	"0" = mode1, "1" = mode2
ST4	Not Used	"0"
ST3	Not Used	"0"
ST2	Not Used	"0"

	ST1	Not Used	“0”
	ST0	Not Used	“0”

Restriction

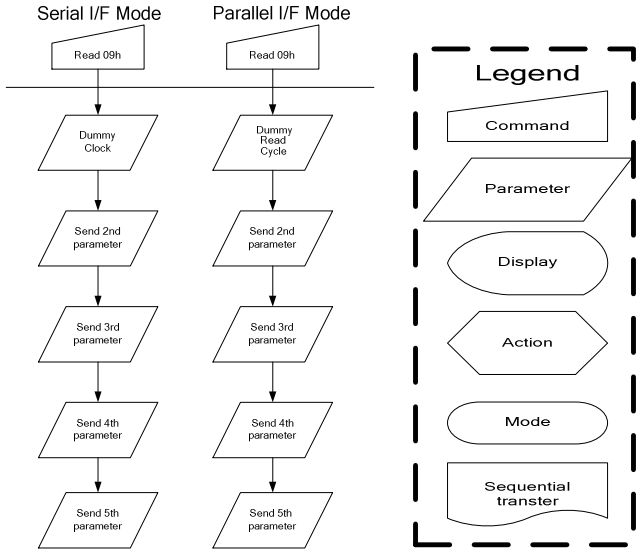
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000 0000_0101 0001_0000 0000_0000 0000
S/W Reset	0xxx xx00_0xxx 0001_0000 0000_0000 0000
H/W Reset	0000 0000_0101 0001_0000 0000_0000 0000

Flow Chart



9.1.5 RDDPM:Read Display Power Mode (0AH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	1	0	1	0	0AH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	D6	D5	D4	D3	D2	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Booster Voltage Status	“1”=Booster on, “0”=Booster off
D6	Idle Mode On/Off	“1” = Idle Mode On, “0” = Idle Mode Off
D5	Partial Mode On/Off	“1” = Partial Mode On, “0” = Partial Mode
D4	Sleep In/Out	“1” = Sleep Out, “0” = Sleep In
D3	Display Normal Mode On/Off	“1” = Normal Display, “0” = Partial Display
D2	Display On/Off	“1” = Display On, “0” = Display Off
D1	Not Used	“0”
D0	Not Used	“0”

Restriction

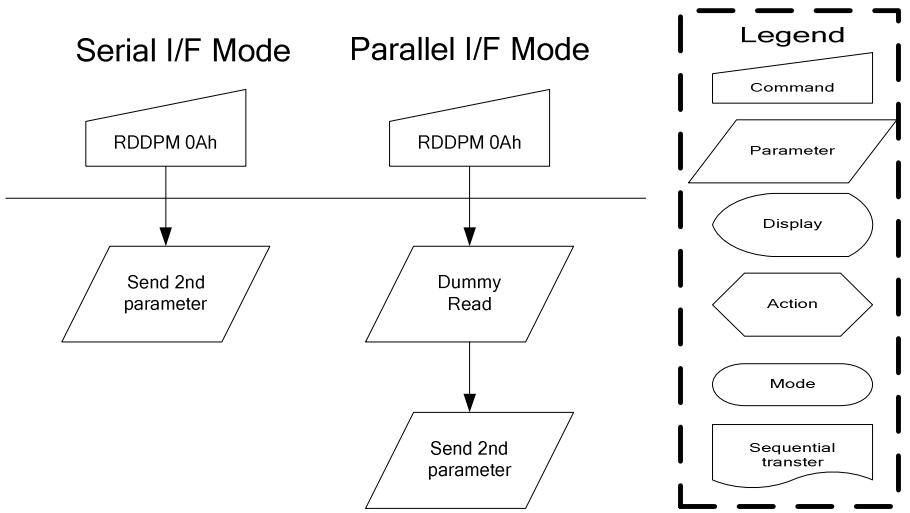
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_1000 (08h)
S/W Reset	0000_1000 (08h)
H/W Reset	0000_1000 (08h)

Flow Chart


Serial I/F Mode
Parallel I/F Mode
RDDPM 0Ah
RDDPM 0Ah
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.6 RDDMADCTL:Read Display MADCTL (0BH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	1	0	1	1	0BH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	D6	D5	D4	D3	0	0	0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Row Address Order (MY)	"1"=Decrement, "0"=Increment
D6	Column Address Order (MX)	"1"=Decrement, "0"=Increment
D5	Row/Column Order (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
D4	Scan Address Order (ML)	"1"=Decrement, "0"=Increment
D3	RGB/BGR Order (RGB)	"1"=BGR, "0"=RGB
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

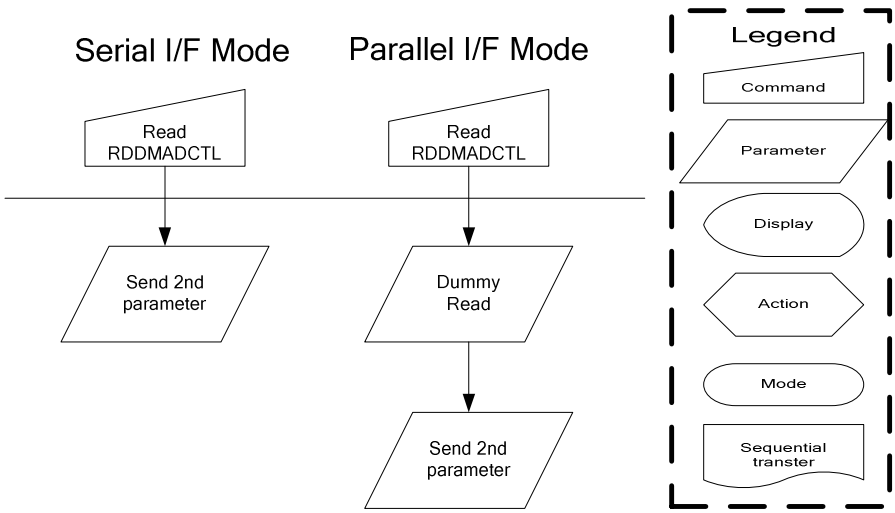
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	No change
H/W Reset	0000_0000 (00h)

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read RDDMADCTL
Read RDDMADCTL
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.7 RDDCOLMOD: Read Display Pixel Format (0CH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	1	1	0	0	0CH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	0	0	0	0	0	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	RGB Interface Color Format	"0" (Not Used)
D6		"0" (Not Used)
D5		"0" (Not Used)
D4		"0" (Not Used)
D3	Control Interface Color Format	"0"
D2		"010"=8 bit/pixel "011"=Reserve "100"=12 bit/pixel "101"=16 bit/pixel "110"=18 bit/pixel "110"=24 bit/pixel The others = not defined
D1		
D0		

Restriction

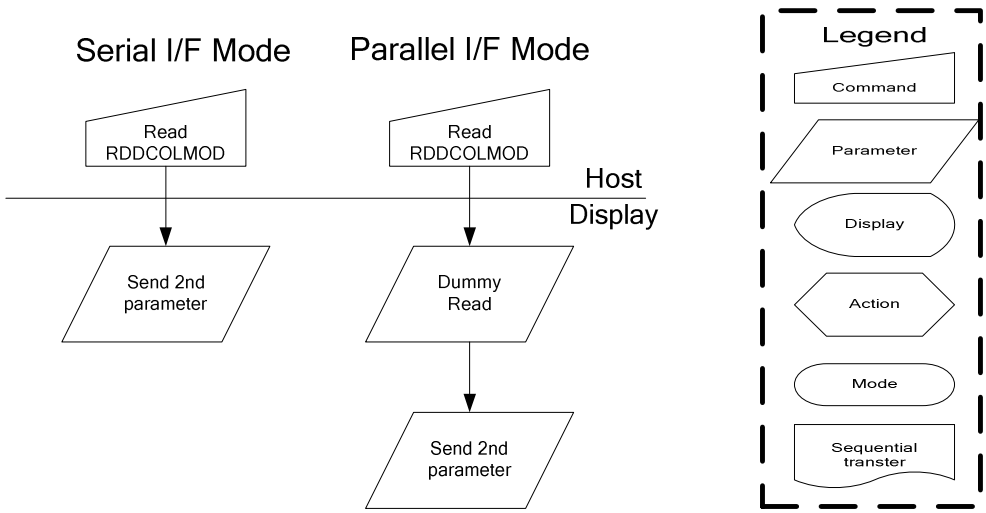
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	18 bit/pixel
S/W Reset	No change
H/W Reset	18 bit/pixel

Flow Chart	


Serial I/F Mode
Parallel I/F Mode
Read RDDCOLMOD
Read RDDCOLMOD
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.8 RDDIM: Read Display Image Mode (0DH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	1	1	0	1	0DH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	0	D5	D4	D3	0	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description		Command
D7	Vertical Scrolling On/Off	0	Vertical scrolling off
		1	Vertical scrolling is On,
D6	Horizontal Scrolling On/Off	0	No used
		1	No used
D5	Inversion On/Off	0	Inversion is Off
		1	Inversion is On
D4	All Pixels On	0	Normal Mode
		1	All Pixels are on
D3	All Pixels Off	0	Normal Mode
		1	All Pixels are off
D2	Gamma Curve Selection	0	No used
D1			
D0			

Restriction

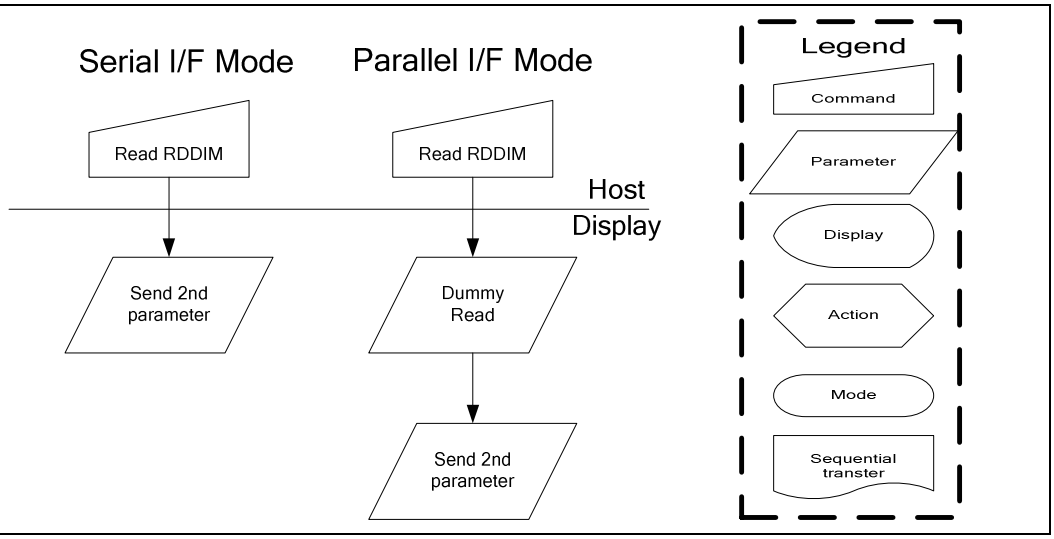
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read RDDIM
Read RDDIM
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.9 RDDCOLMOD: Read Display Signal Mode (0EH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	1	1	1	0	0EH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	D6	0	0	0	0	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description		Command
D7	Tearing Effect Line On/Off	0	Tearing Effect Line Off.
		1	Tearing Effect On.
D6	Tearing Effect Line Output Mode	0	Mode 1
		1	Mode 2
D5	Horizontal Sync. (RGB I/F) On/Off		“0” (Not Used)
D4	Vertical Sync. (RGB I/F) On/Off		“0” (Not Used)
D3	Pixel Clock (DCK, RGB I/F) On/Off		“0” (Not Used)
D2	Data Enable (ENABLE, RGB I/F) On/Off		“0” (Not Used)
D1	Not Used		“0”
D0	Not Used		“0”

Restriction

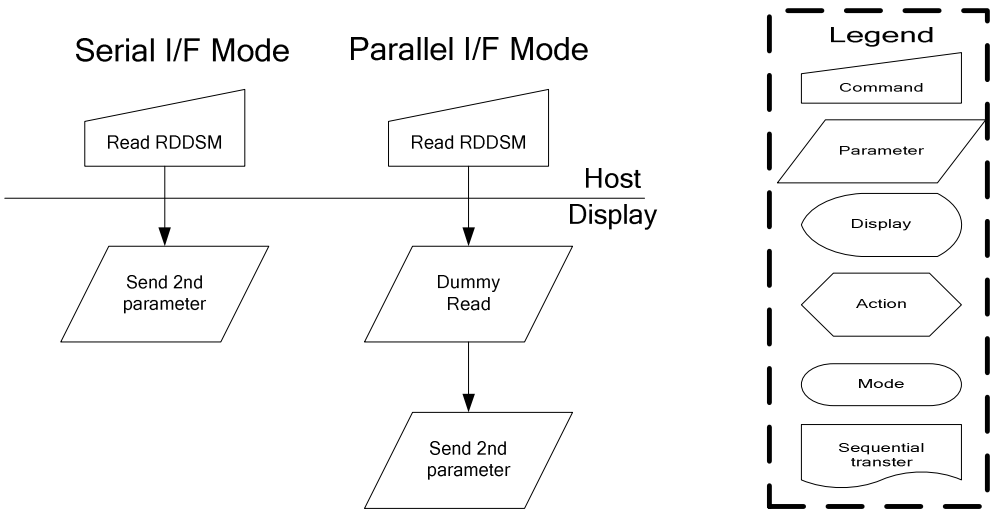
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart	


Serial I/F Mode
Parallel I/F Mode
Read RDDSM
Read RDDSM
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.10 RDDSDR: Read Display Self-Diagnostic Result (0FH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	1	1	1	1	0FH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	D6	D5	D4	0	0	0	0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Command
D7	Register Loading Detection	See section 7.12.1 , 7.12.2 , 7.12.3
D6	Functionality Detection	
D5	Chip Attachment Detection	
D4	LCM Glass Direction	
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

Register Availablility

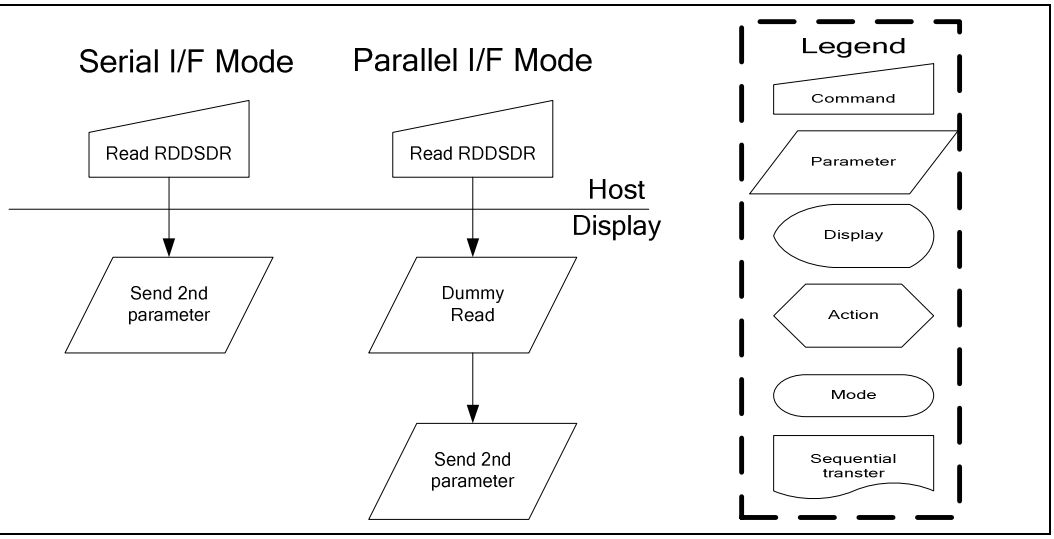
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read RDDSDR
Read RDDSDR
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

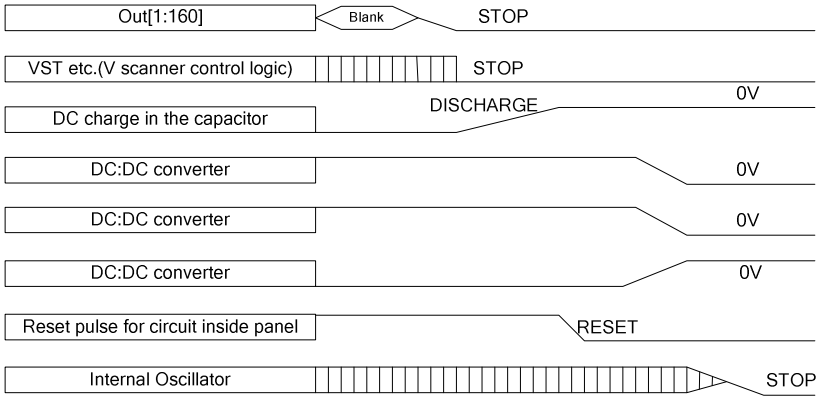
9.1.11 SLPIN : Sleep In(10H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	1	0	0	0	0	10H
Parameter	No parameter											

Description

This command causes the LCD module to enter the minimum power consumption mode.

In this mode the DC/DC converter, Internal oscillator, and panel scanning are all stopped.



MCU interface and memory are still working and the memory keeps its contents.

Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).

It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilise.

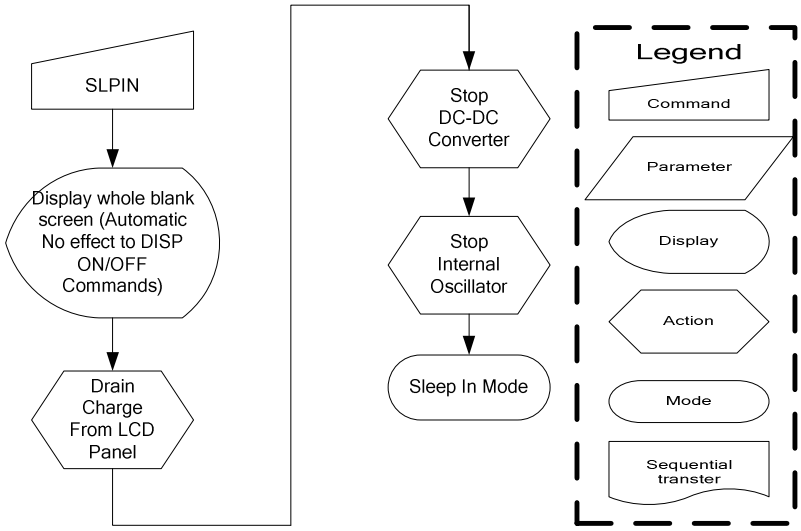
It will be necessary to wait 200msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

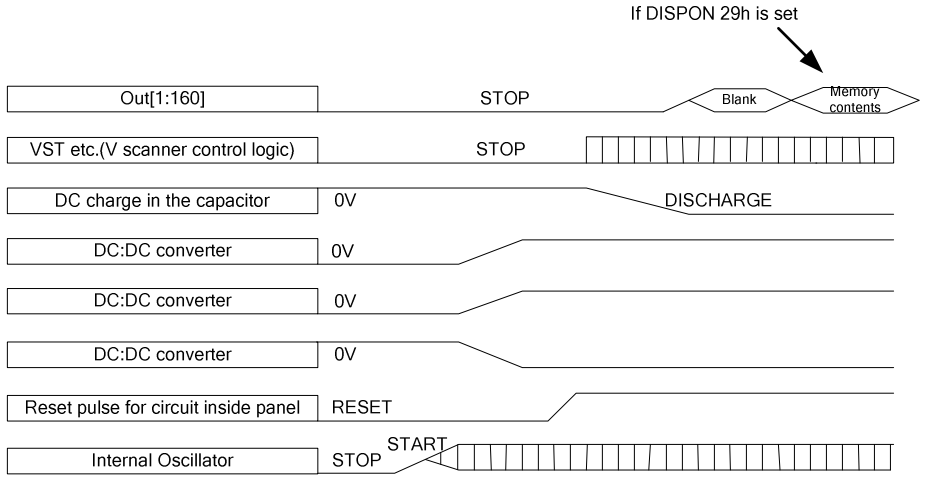
Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart	It takes about 200 msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be check by RDDST (09h) command Bit31. 

9.1.12 SLPOUT: Sleep Out (11H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	1	0	0	0	1	11H
Parameter	No parameter											

Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started. 
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilise. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec.. It will be necessary to wait 200msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

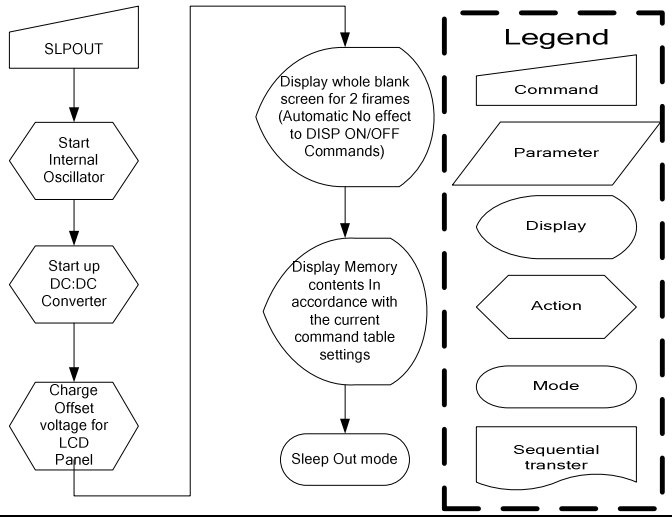
Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart

It takes 200msec to become Sleep Out mode (booster on mode) after SLPOUT command issued.

The results of booster on can be check by RDDST (09h) command Bit31.



9.1.13 PTLON : Partial Mode On (12H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	1	0	0	1	0	12H
Parameter	No parameter											

Description	This command turns on partial mode The partial mode window is described by the Partial Area command (30H). Exit from PTLON by Normal Display Mode On command (13H) There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Partial mode is active.
Register Availablility	
Default	
Flow Chart	See Partial Area (30h)

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Partial mode off
S/W Reset	Partial mode off
H/W Reset	Partial mode off

9.1.14 NORON: Normal Display Mode On (13H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	1	0	0	1	1	13H
Parameter	No parameter											

Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. Exit from NORON by the Partial mode On command (12h) There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Normal Display mode is active.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

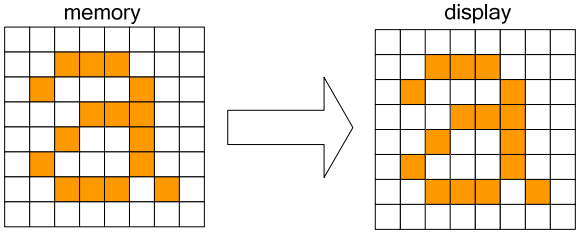
Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command

9.1.15 INVOFF: Display Inversion Off (20H)

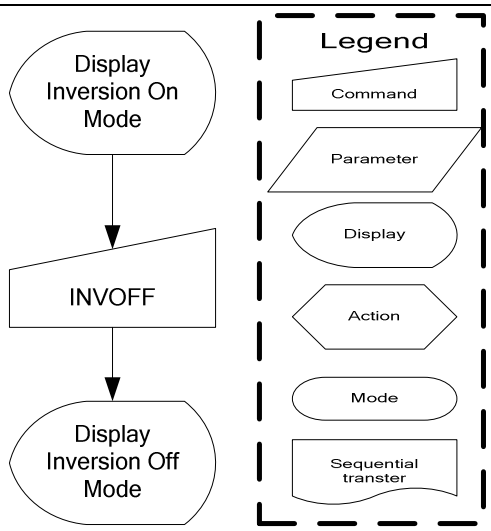
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	0	0	0	0	20H
Parameter	No parameter											

Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory → display 
Restriction	This command has no effect when IC is already in inversion off mode.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

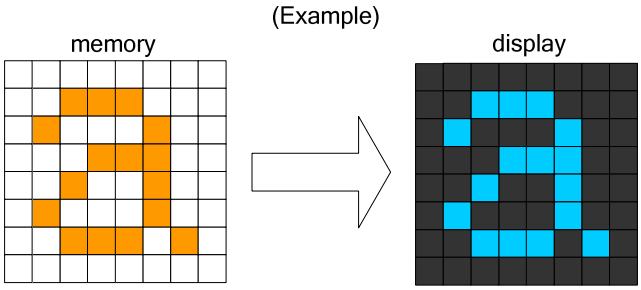
Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart	 Display Inversion On Mode INVOFF Display Inversion Off Mode Legend Command Parameter Display Action Mode Sequential transter

9.1.16 INVON: Display Inversion On (21H)

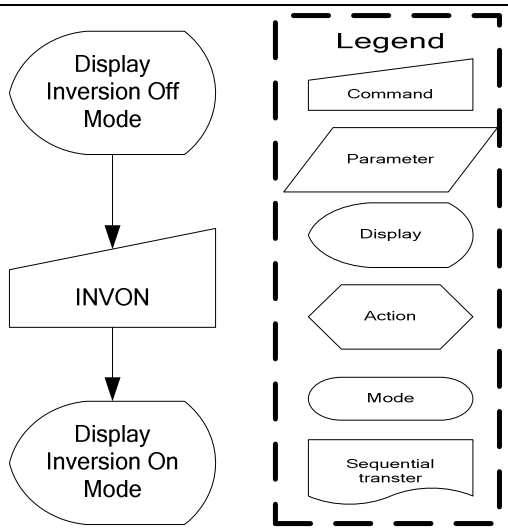
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	0	0	0	1	21H
Parameter	No parameter											

Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. 
Restriction	This command has no effect when IC is already in inversion on mode.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

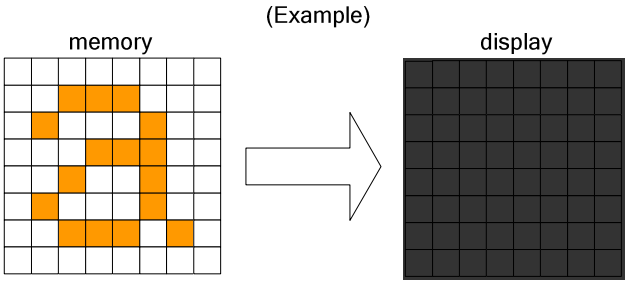
Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart	

Display Inversion Off Mode
INVON
Display Inversion On Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.17 ALLPOFF : ALL Pixels Off (22H)

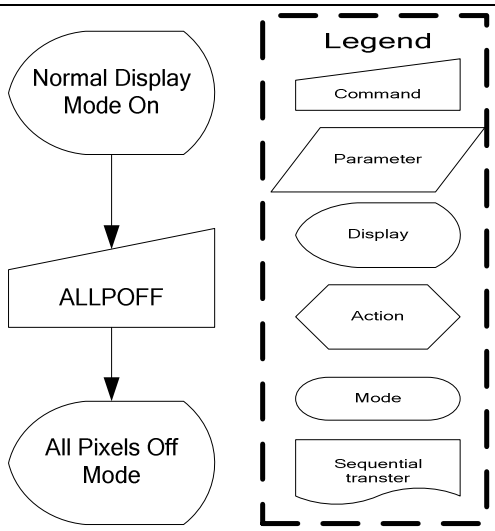
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	0	0	1	0	22H
Parameter	No parameter											

Description	This command is only used for test purposes e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software. There is not used PWM or Mixed FRC/PWM driving method on the display. All driver outputs become “Low” data state and display becomes black. This command makes no change of contents of display memory. This command does not change any other status. Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”. The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands. 
Restriction	This command has no effect when IC is already in all pixels off mode.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

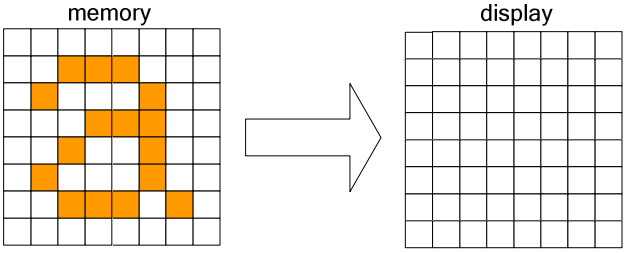
Default

Status	Default Value
Power On Sequence	All pixel off mode disable
S/W Reset	All pixel off mode disable
H/W Reset	All pixel off mode disable

Flow Chart	 Normal Display Mode On ALLPOFF All Pixels Off Mode Legend Command Parameter Display Action Mode Sequential transter

9.1.18 ALLPON: All Pixels On (23H) (Only for Test Purposes)

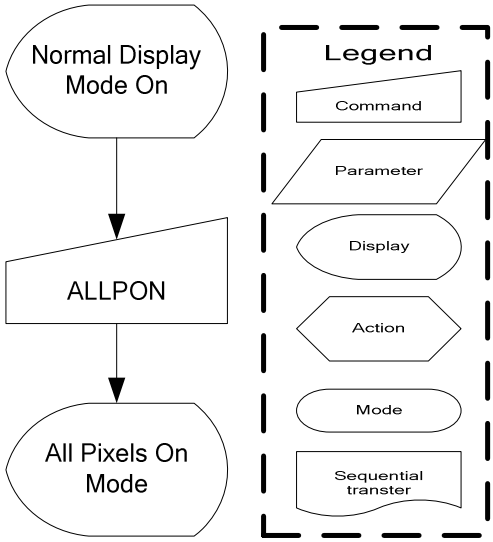
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	0	0	1	1	23H
Parameter	No parameter											

Description	This command is only used for test purposes e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software. There is not used PWM or Mixed FRC/PWM driving method on the display. All driver outputs become “High” data state and display becomes white. This command makes no change of contents of display memory. This command does not change any other status. Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”. The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands. (Example) memory → display 
Restriction	This command has no effect when IC is already in all pixels on mode.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All pixel on mode disable
S/W Reset	All pixel on mode disable
H/W Reset	All pixel on mode disable

Flow Chart	 Normal Display Mode On ALLPON All Pixels On Mode Legend Command Parameter Display Action Mode Sequential transter

9.1.19 WRCNTR: Write Contrast (25H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	0	1	0	1	25H
Parameter	1	1	0	0	EV6	EV5	EV4	EV3	EV2	EV1	EV0	00H~7FH

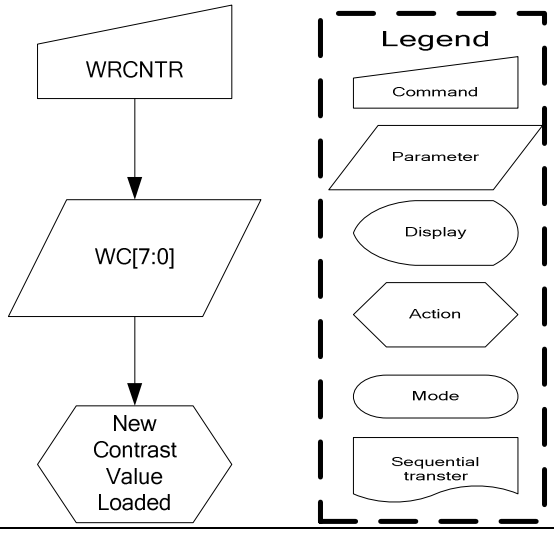
Description	This command is used to fine tuning the contrast of the current display. This contrast values can effect segment and common outputs. Parameter range: 0-127dec. MSB is EV6 and LSB is EV0. Default value: 63dec (3Fh)
Restriction	
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

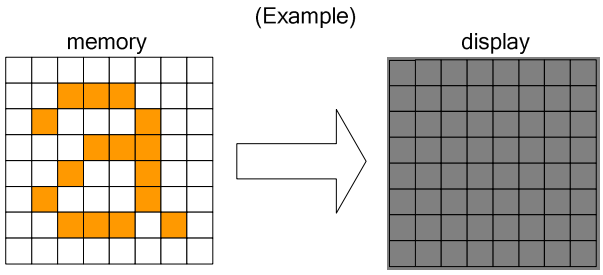
Status	Default Value
Power On Sequence	3Fh
S/W Reset	3Fh
H/W Reset	3Fh

Flow Chart



9.1.20 DISPOFF: Display Off (28H)

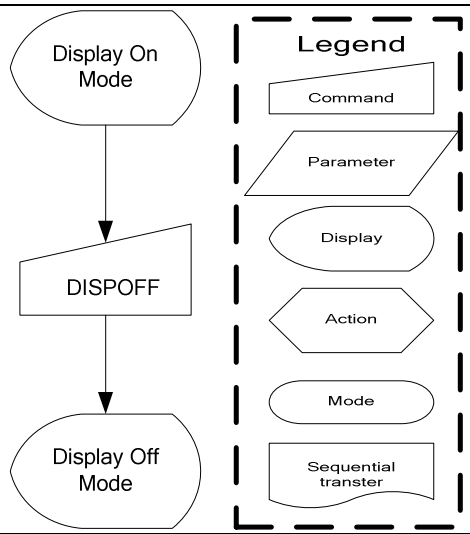
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	0	0	0	28H
Parameter	No parameter											

Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Exit from this command by Display On (29h) 
Restriction	This command has no effect when module is already in display off mode.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

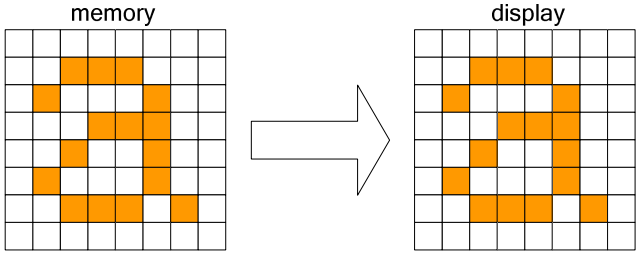
Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart	

Display On Mode
DISPOFF
Display Off Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.21 DISPON: Display On (29H)

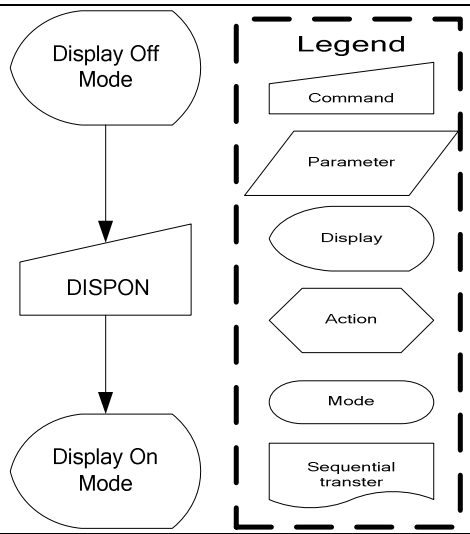
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	0	0	1	29H
Parameter	No parameter											

Description	Turn on the display screen according to the current display data RAM content and the display timing and setting. This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory display 
Restriction	This command has no effect when module is already in display on mode.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart	 Display Off Mode DISPON Display On Mode Legend Command Parameter Display Action Mode Sequential transter

9.1.22 CASET: Column Address Set (2AH)

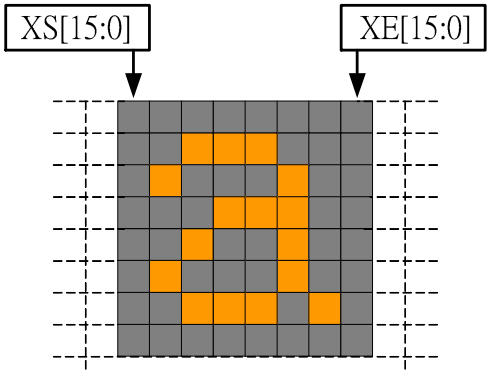
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	0	1	0	2AH
1st parameter	1	1	0	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	Note1
2nd parameter	1	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	Note1
3rd parameter	1	1	0	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	Note1
4th parameter	1	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	Note1

Description

This command is used to define area of frame memory where MCU can access.

This command makes no change on the other driver status.

The values of XS[15:0] and XE[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



Restriction

XS[15:0] always must be equal to or less than XE[15:0]

Note 1: When XS[15:0] or XE[15:0] is greater than 83h (when MADCTL's MV=0) or A1h (when MADCTL's MV=1), data of out of range will be ignored

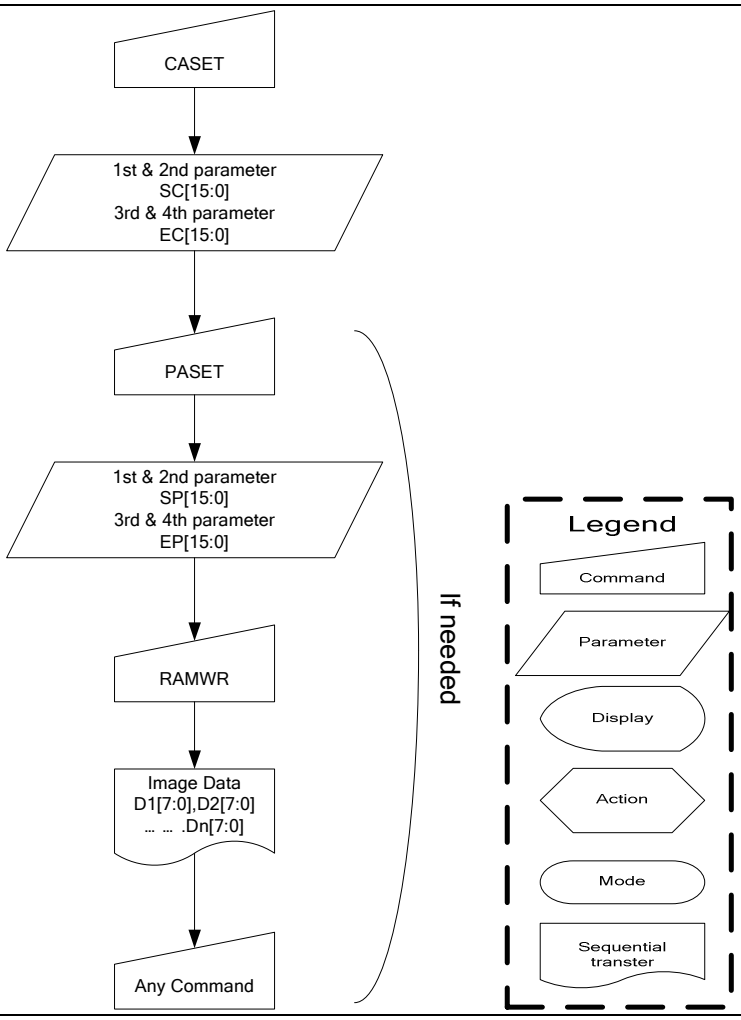
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	00h	83h	
S/W Reset	00h	83h	A1h
H/W Reset	00h	83h	

Flow Chart



9.1.23 RASET: Row Address Set (2BH)

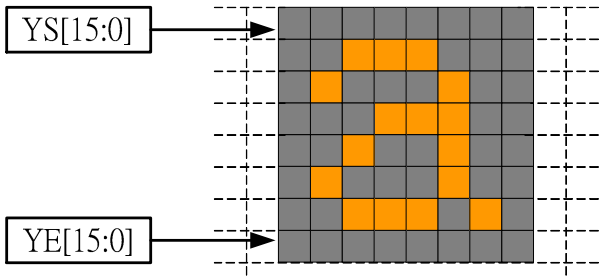
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	0	1	1	2BH
1st parameter	1	1	0	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	Note1
2nd parameter	1	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	Note1
3rd parameter	1	1	0	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	Note1
4th parameter	1	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	Note1

Description

This command is used to define area of frame memory where MCU can access.

This command makes no change on the other driver status.

The values of YS[15:0] and YE[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



Restriction

YS[15:0] always must be equal to or less than YE[15:0]

Note 1: When YS[15:0] or YE[15:0] is greater than A1h (When MADCTL's MV=0) or 83h (When MADCTL's MV=1), data of out of range will be ignored.

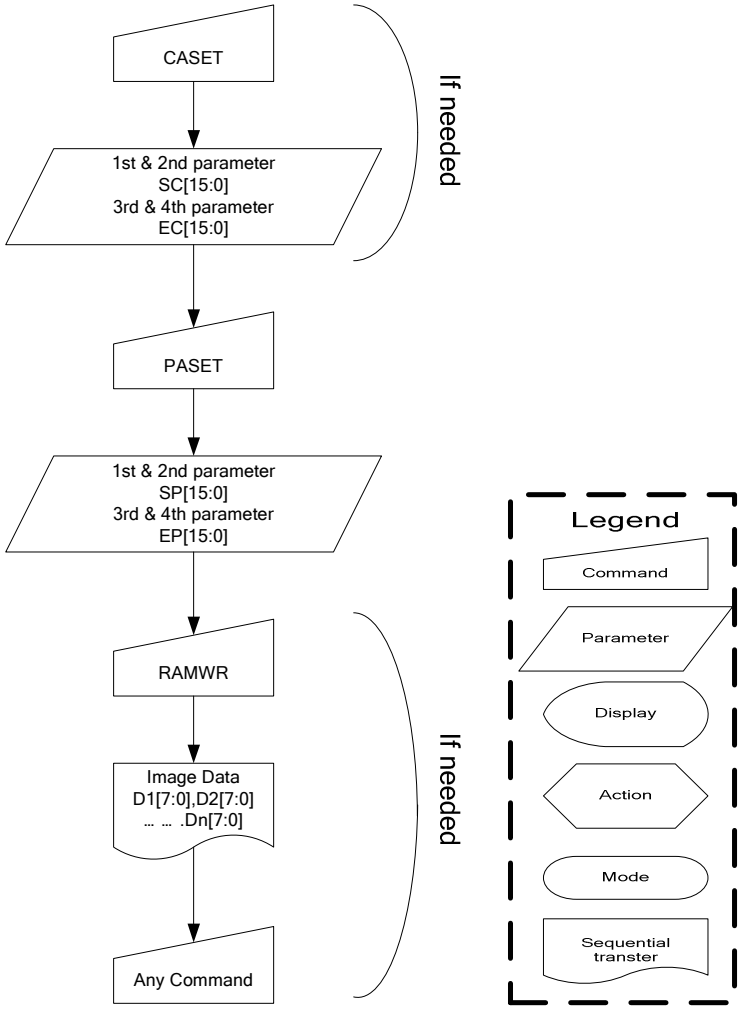
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	YS [15:0]	YE [15:0] (MV=0)	YE [15:0] (MV=1)
Power On Sequence	00h	A1h	
S/W Reset	00h	A1h	83h
H/W Reset	00h	A1h	

Flow Chart


CASET
1st & 2nd parameter
SC[15:0]
3rd & 4th parameter
EC[15:0]
If needed
PASET
1st & 2nd parameter
SP[15:0]
3rd & 4th parameter
EP[15:0]
RAMWR
Image Data
D1[7:0],D2[7:0]
... ... .Dn[7:0]
Any Command
If needed
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.24 RAMWR: Memory Write (2CH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	1	0	0	2CH
Write D1[7:0]	1	1	0	D17	D16	D15	D14	D13	D12	D11	D10	00H ~ FFH
…	1	1	0	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00H ~ FFH
Write Dn[7:0]	1	1	0	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00H ~ FFH

Description

This command is used to transfer data from MCU to frame memory.

This command makes no change to the other driver status.

When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.

The Start Column/Start Row positions are different in accordance with MADCTR setting.

Then D[7:0] is stored in frame memory and the column register and the row register incremented. as in Figure 8.3.

Frame Write can be canceled by sending any other command.

Restriction

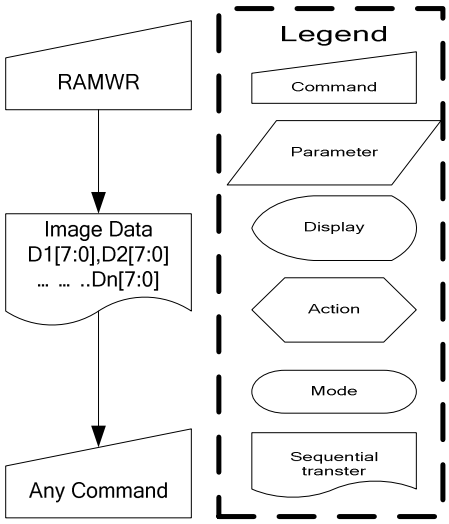
In all colour modes, there is no restriction on length of parameters.

Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is remained
H/W Reset	Contents of memory is remained

Flow Chart	

RAMWR
Image Data
D1[7:0],D2[7:0]
... .Dn[7:0]
Any Command
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

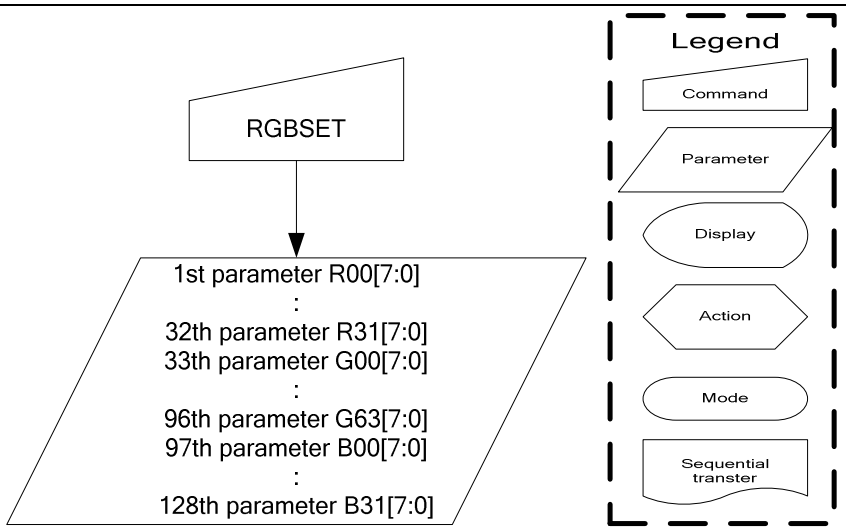
9.1.25 RGBSET : Color Set (2DH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	1	0	1	2DH
1st parameter	1	1	0	-	-	R005	R004	R003	R002	R001	R000	00H~FFH
…	1	1	0	-	-	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	00H~FFH
32nd parameter	1	1	0	-	-	R315	R314	R313	R312	R311	R310	00H~FFH
33rd parameter	1	1	0	-	-	G005	G004	G003	G002	G001	G000	00H~FFH
…	1	1	0	-	-	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	00H~FFH
96th parameter	1	1	0	-	-	G635	G634	G633	G632	G631	G630	00H~FFH
97th parameter	1	1	0	-	-	B005	B004	B003	B002	B001	B000	00H~FFH
…	1	1	0	-	-	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	00H~FFH
128th parameter	1	1	0	-	-	B315	B314	B313	B312	B311	B310	00H~FFH

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>This command is used to define the LUT for 8bit-to-18bit /12bit-to-18bit /16bit-to-18bit colour depth conversions. (See also section 7.8) 128 bytes must be written to the LUT regardless of the colour mode. Only the values in Section 7.8 are referred.
This command has no effect on other commands/parameters and Contents of frame memory. Visible change takes effect next time the Frame Memory is written to.</td></tr>
<tr><td>Restriction</td><td>Do not send any command before the last data is sent or LUT is not defined correctly.</td></tr>
<tr><td>Register Availablility</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Random values</td></tr>
<tr><td>S/W Reset</td><td>Contents of the look-up table protected</td></tr>
<tr><td>H/W Reset</td><td>Random values</td></tr>
</table>
</td></tr>
</table>

Flow Chart


RGBSET
1st parameter R00[7:0]
:
32th parameter R31[7:0]
33th parameter G00[7:0]
:
96th parameter G63[7:0]
97th parameter B00[7:0]
:
128th parameter B31[7:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.26 RAMRO : Memory Read (2EH)

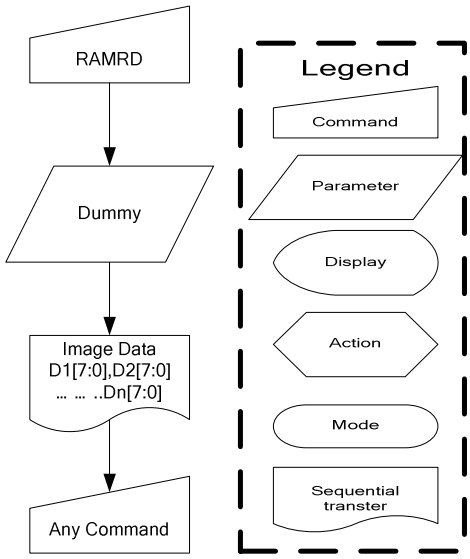
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	1	1	0	2EH
1st parameter	1	0	1	x	x	x	x	x	x	x	x	x
2nd parameter	1	0	1	D17	D16	D15	D14	D13	D12	D11	D10	00H ~ FFH
…	1	0	1	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00H ~ FFH
(N+1)th parameter	1	0	1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00H ~ FFH

Description	This command is used to transfer data from frame memory to MCU. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. (See 8.3) Then D[7:0] is read back from the frame memory and the column register and the page register incremented as in Table 8.3 Frame Read can be stopped by sending any other command.
Restriction	In all colour modes, the Frame Read is always 18bit so there is no restriction on length of parameters. Note – Memory Read is only possible via the Parallel Interface.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart	

RAMRD
Dummy
Image Data
D1[7:0],D2[7:0]
... .Dn[7:0]
Any Command
Legend
Command
Parameter
Display
Action
Mode
Sequential
transter

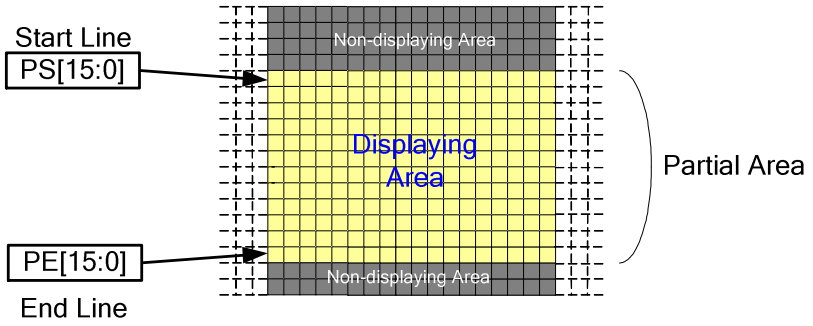
9.1.27 PTLAR: Partial Area (30H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	0	0	0	0	30H
1st parameter	1	1	0	PS15	PS14	PS13	PS12	PS11	PS10	PS9	PS8	00H ~ A1H
2nd parameter	1	1	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	
3rd parameter	1	1	0	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	00H ~ A1H
4th parameter	1	1	0	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	

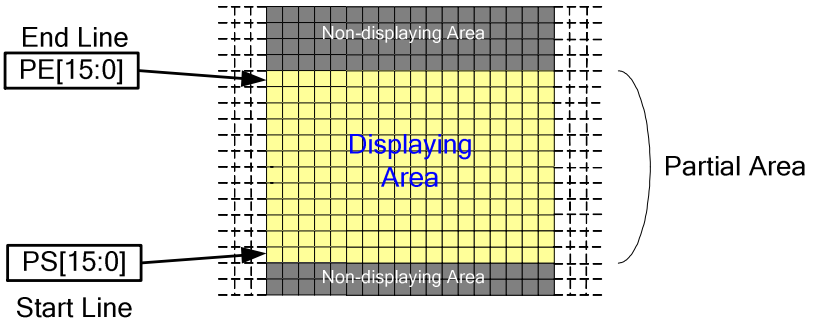
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Line (PS) and the second the End Line (PE), as illustrated in the figures below. PS and PE refer to the Frame Memory Line counter.

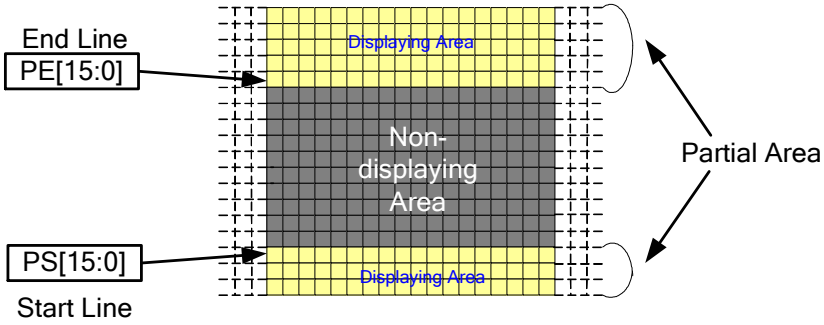
If End Line > Start Line when MADCTR ML=0:



If End Line > Start Line when MADCTR ML=1:



If End Line < Start Line when MADCTR ML=0:



* Row1: Frame memory row address 1.

If End Line = Start Line then the Partial Area will be one line deep.

Restriction

PS[15:0] and PE[15:0] cannot be greater than A1h.

Register Availablility

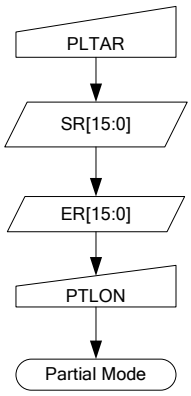
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

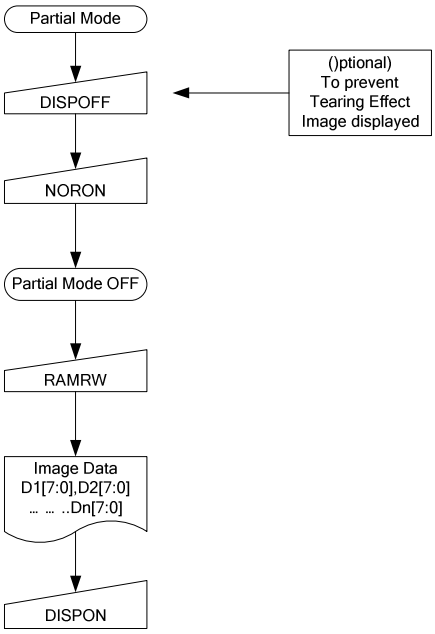
Status	Default Value	
Power On Sequence	PS[15:0]=0000H	PE[15:0]=00A1H
S/W Reset	PS[15:0]=0000H	PE[15:0]=00A1H
H/W Reset	PS[15:0]=0000H	PE[15:0]=00A1H

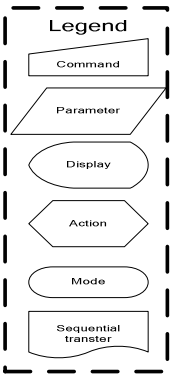
Flow Chart

1. TO Enter Partial Mode:



2. Leave Partial Mode

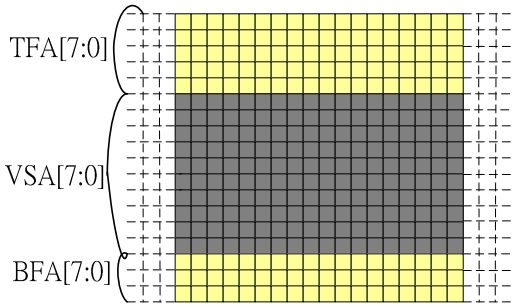




9.1.28 RLAR: Scroll Area (33h)

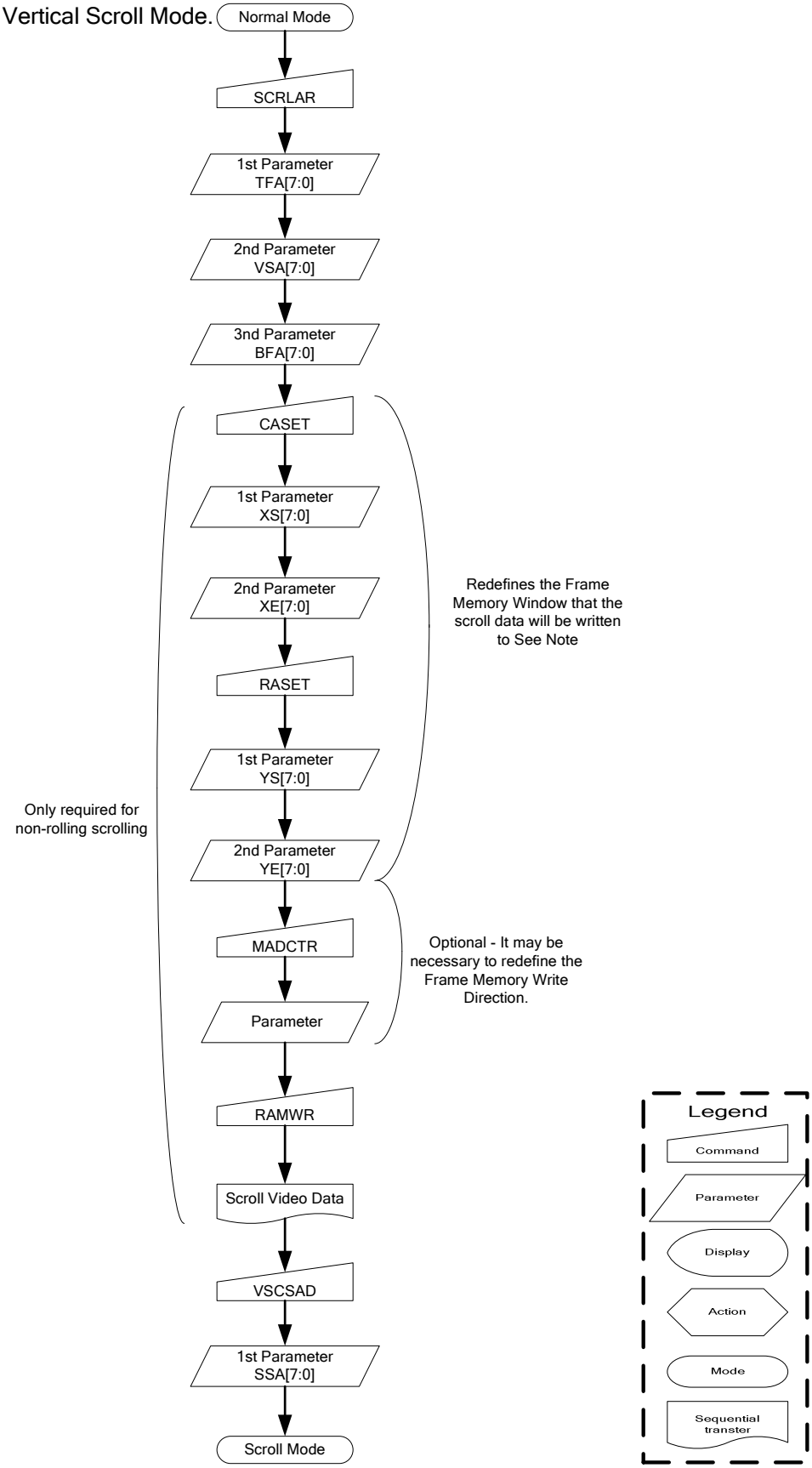
Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
SCRLAR	0	1	0	0	0	1	1	0	0	1	1	**(33h)**
1st parameter	1	1	0	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-
2nd parameter	1	1	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-
3rd parameter	1	1	0	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll.
When MADCTL ML=0
The 1st parameter TFA [7:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memoryand Display).
The 2nd parameter VSA [7:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area.
The 3rd parameter BFA [7:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
TFA, VSA and BFA refer to the Frame Memory Line Pointer.
 
</td></tr>
<tr><td>Restriction</td><td>The condition is (TFA+VSA+BFA) = 162, otherwise Scrolling mode is undefined.
In Vertical Scroll Mode, MADCTL parameter MV should be set to '0'-this only affects the Frame Memory Write.
TFA[7:0], VSA[7:0] and BFA[7:0] is based on line unit.
TFA[7:0]= 00h, 01h, 02h, 03h, … , A1h
VSA[7:0]= 00h, 01h, 02h, 03h, … , A1h
BFA[7:0]= 00h, 01h, 02h, 03h, … , A1h</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td>Default</td><td>
<table>
<tr><td rowspan="2">Status</td><td colspan="3">Default Value</td></tr>
<tr><td>TFA [7:0]</td><td>VSA [7:0]</td><td>BFA [7:0]</td></tr>
<tr><td>Power On Sequence</td><td>00h</td><td>A2h</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td><td>A2h</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td><td>A2h</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

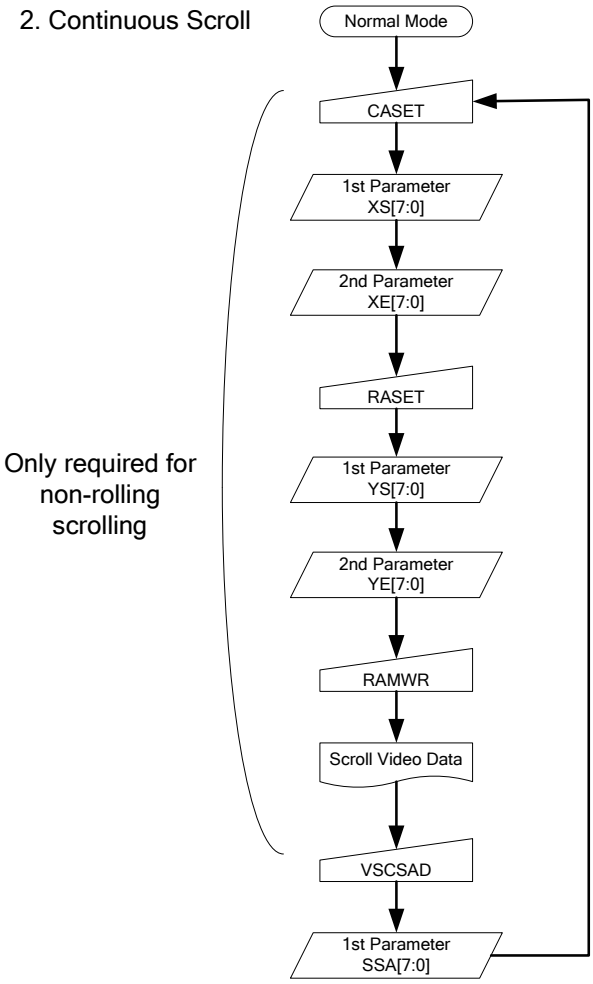
1.To enter Vertical Scroll Mode.



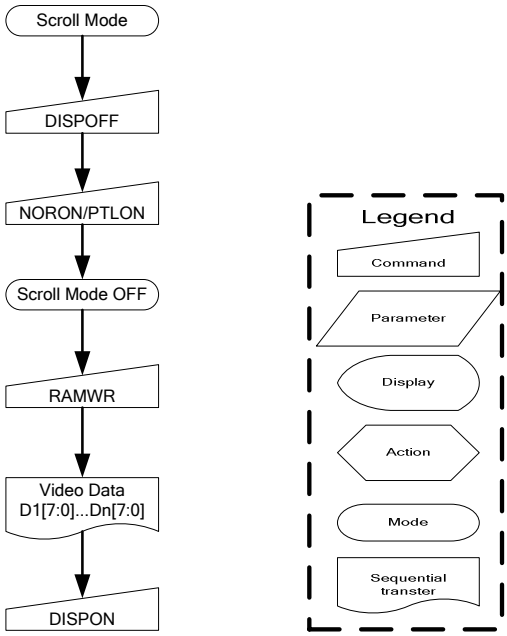
NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

low Chart

2. Continuous Scroll



3. To Exit Vetical Scroll mode



NOTE: Scroll Mode can be exit by both the Normal Display Mode On(13h) and Partial Mode On (12h) commands.

9.1.29 TEOFF: Tearing Effect Line Off (34H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	0	1	0	0	34H
Parameter	No Parameter											

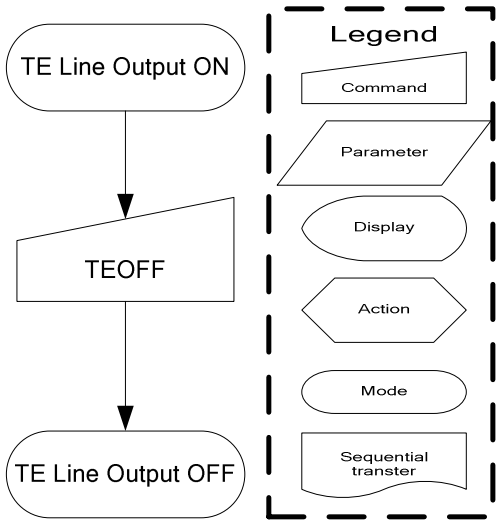
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	This command has no effect when Tearing Effect output is already OFF.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off
S/W Reset	Tearing effect off
H/W Reset	Tearing effect off

Flow Chart



9.1.30 TEON: Tearing Effect Line On (35H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	0	1	0	1	35H
1st parameter	1	1	0	-	-	-	-	-	-	-	M	-

NOTE: "-" Don't care

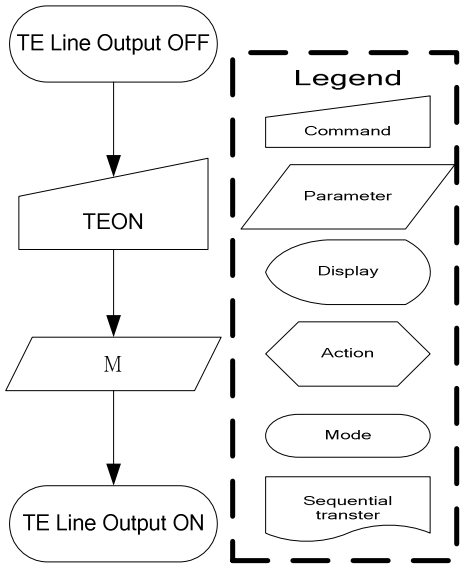
Description	This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care). *Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.*
Restriction	This command has no effect when Tearing Effect output is already ON.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off & M=0
S/W Reset	Tearing effect off & M=0
H/W Reset	Tearing effect off & M=0

Flow Chart



9.1.31 MADCTL: Memory Access Control (36H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	0	1	1	0	36H
1st parameter	1	1	0	MY	MX	MV	ML	RGB	-	-	-	-

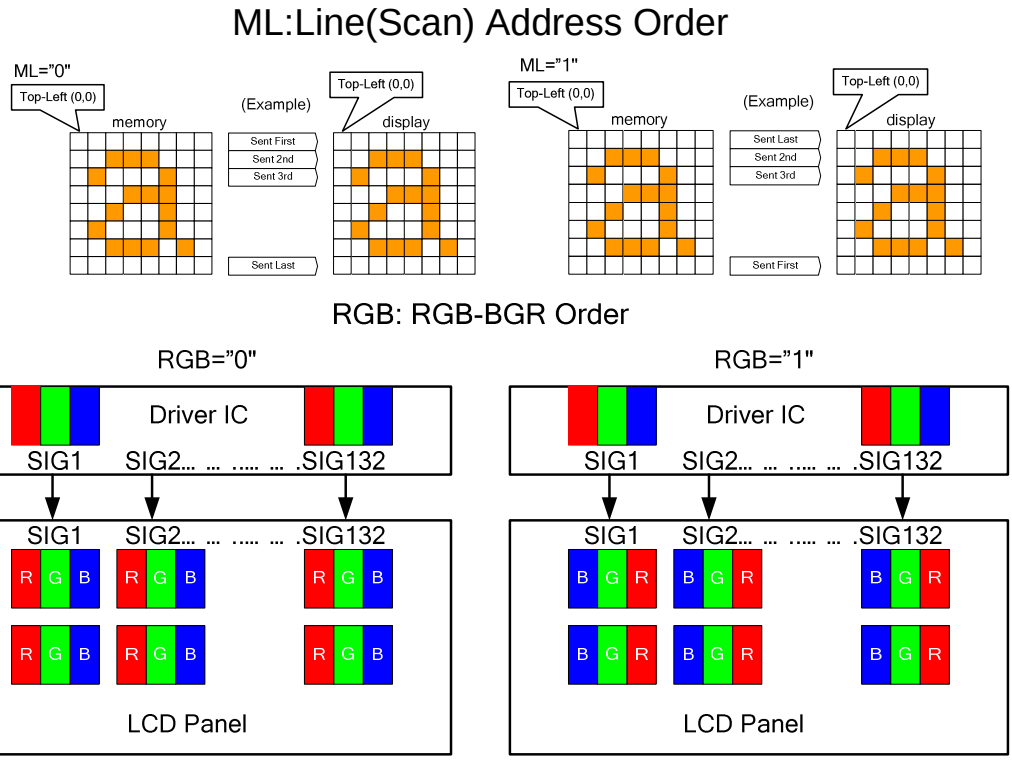
Description

This command defines read/write scanning direction of frame memory.

This command makes no change on the other driver status.

Note: ML affects to Partial Area (30h), Vertical Scrolling Definition (33h), Vertical Scrolling Start address (37h), Partial On (12h) commands

Bit	NAME	DESCRIPTION
MX	Page Address Order	These 3 bits controls MCU to memory write/read direction.
MY	Column Address Order	
MV	Page/Column Selection	
ML	Vertical Order	LCD vertical refresh direction control
RGB	RGB-BGR Order	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel) The contents of the frame memory are not changed.



Note: Top-Left (0,0) means a physical memory location.

Restriction

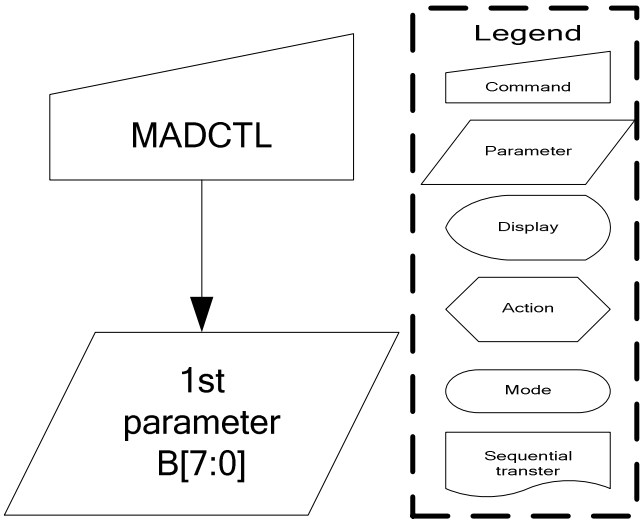
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MY=0,MX=0,ML=0,RGB=0
S/W Reset	No Change
H/W Reset	MY=0,MX=0,ML=0,RGB=0

Flow Chart



9.1.32 SCSAD: Vertical Scroll Start Address of RAM (37h)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
VSCSAD	0	1	0	0	0	1	1	0	1	1	1	**(37h)**
Parameter	1	1	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	

NOTE: "-" Don't care

Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.

The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

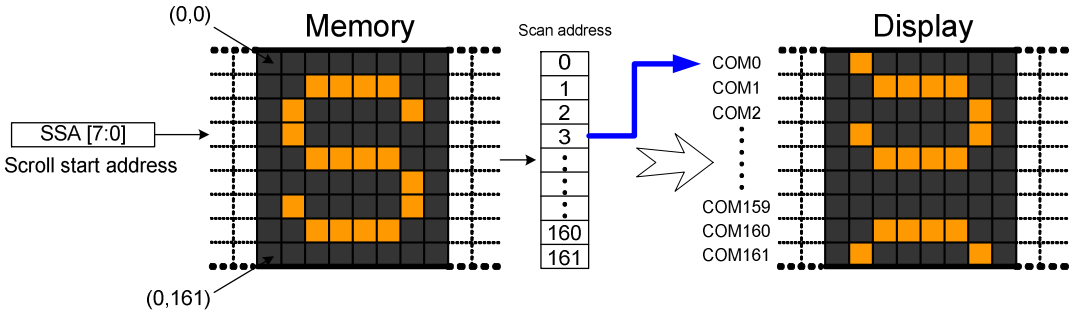
This command Start the scrolling.

Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).

When MADCTL ML=0

Example:

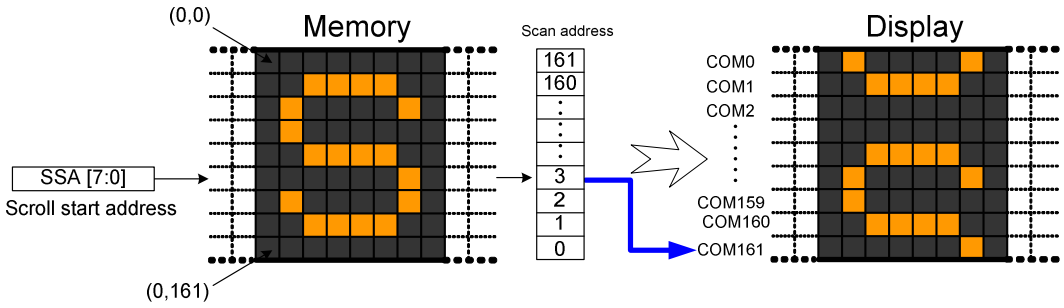
When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=162 and Vertical Scrolling Pointer SSA='3'.



When MADCTL ML=1

Example:

When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=162 and Vertical Scrolling Pointer SSA='3'.



NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

SSA refers to the Frame Memory line Pointer.

<table>
<tr><td>Restriction</td><td>Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.

SSA [7:0] is based on line unit.
SSA [7:0] = 00h, 01h, 02h, 03h, … , A1h</td></tr>
<tr><td>Register Availability</td><td><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

9.1.33 IDMOFF: Idle Mode Off (38H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	1	0	0	0	38H
Parameter	No Parameter											

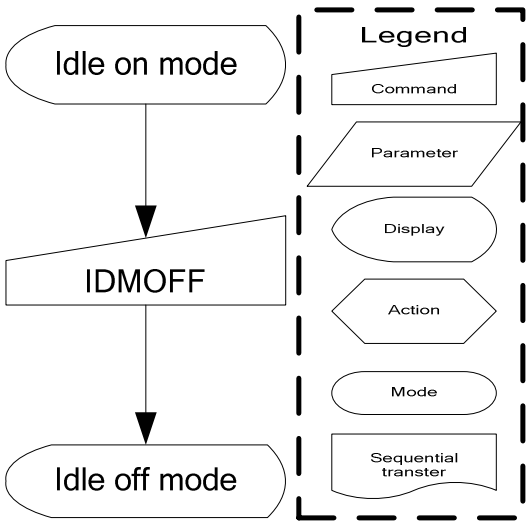
Description	This command is used to recover from Idle mode on. There will be no abnormal visible effect on the display mode change transition. In the idle off mode, 1. LCD can display maximum 262,144 colors. 2. Normal frame frequency is applied.
Restriction	This command has no effect when module is already in idle off mode.
Register Availablility	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Off Mode
S/W Reset	Idle Off Mode
H/W Reset	Idle Off Mode

Flow Chart



9.1.34 IDMON: Idle Mode On (39H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	1	0	0	1	39H
Parameter	No Parameter											

Description

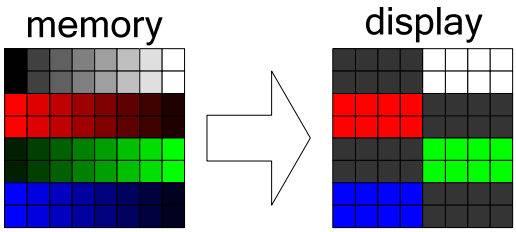
This command is used to enter into Idle mode on.

There will be no abnormal visible effect on the display mode change transition.

In the idle on mode,

1. Color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)



Memory contents V.S Display Colour

	R_5 R_4 R_3 R_2 R_1 R_0	G_5 G_4 G_3 G_2 G_1 G_0	B_5 B_4 B_3 B_2 B_1 B_0
Black	**0XXXXX**	**0XXXXX**	**0XXXXX**
Blue	**0XXXXX**	**0XXXXX**	**1XXXXX**
Red	**1XXXXX**	**0XXXXX**	**0XXXXX**
Magenta	**1XXXXX**	**0XXXXX**	**1XXXXX**
Green	**0XXXXX**	**1XXXXX**	**0XXXXX**
Cyan	**0XXXXX**	**1XXXXX**	**1XXXXX**
Yellow	**1XXXXX**	**1XXXXX**	**0XXXXX**
White	**1XXXXX**	**1XXXXX**	**1XXXXX**

X=don't care

Restriction

This command has no effect when module is already in idle on mode.

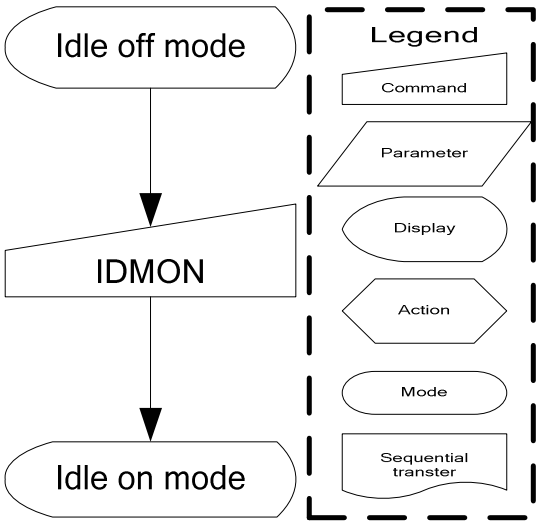
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Off Mode
S/W Reset	Idle Off Mode
H/W Reset	Idle Off Mode

Flow Chart



9.1.35 COLMOD: Interface Pixel Format (3AH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	1	0	1	0	3AH
1st parameter	1	1	0	-	-	-	-	-	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command is used to define the format of RGB picture data, which is transferred via the MCU Interface. The formats are shown in the table:

Interface Format	D2	D1	D0
Not Defined	0	0	0
Not Defined	0	0	1
8 Bit/Pixel	0	1	0
12 Bit/Pixel	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
24 Bit/Pixel	1	1	1

Note: In 8 bit/pixel , 8 bit/pixel or 16 bit/pixel mode, the LUT is applied to transfer data into the Frame Memory.

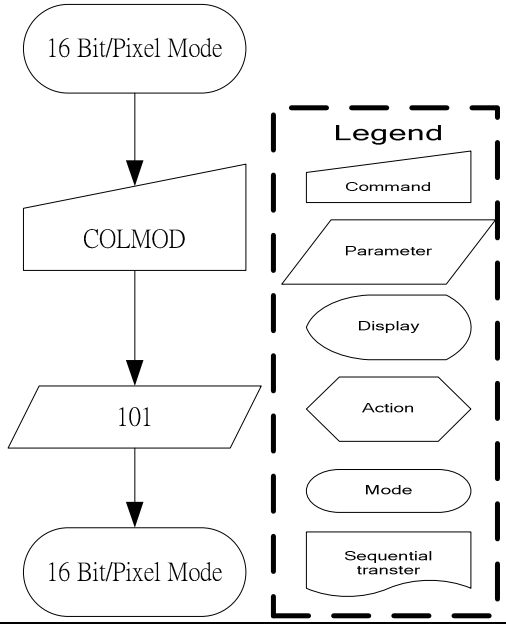
Restriction

Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	06h (18Bit/Pixel)
S/W Reset	No Change
H/W Reset	06h (18Bit/Pixel)

Flow Chart	

16 Bit/Pixel Mode
COLMOD
101
16 Bit/Pixel Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.36 RDID1: Read ID1 (DAH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	1	1	0	1	0	DAH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-

NOTE: "-" Don't care

Description

This read byte returns 8-bit LCD module's manufacturer ID

D7-D0 (ID17 to ID10): LCD module's manufacturer ID.

NOTE: See command RDDID (04h), 2nd parameter.

Restriction

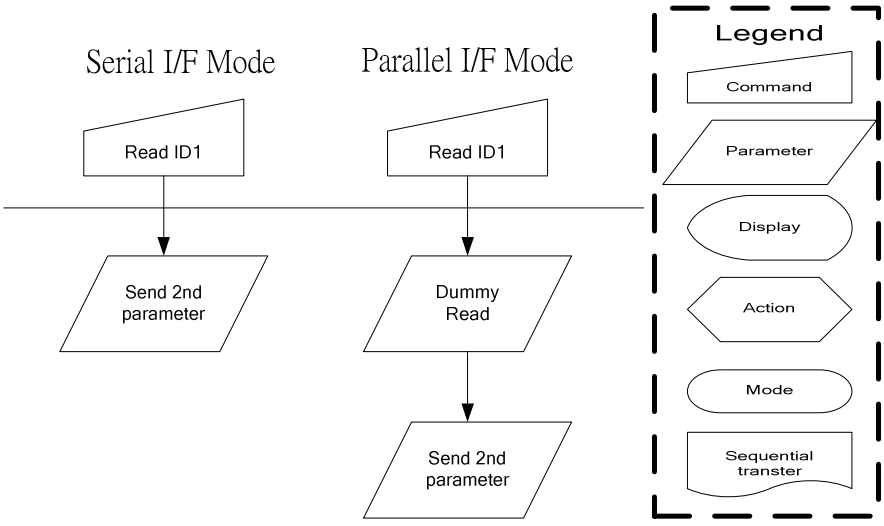
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not fixed
S/W Reset	Not fixed
H/W Reset	Not fixed

Flow Chart



9.1.37 RDID2: Read ID2 (DBH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	1	1	0	1	1	DBH
1st parameter	1	0	1	x	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: "-" Don't care

Description

This read byte returns 8-bit LCD module/driver version ID

D7-D0 (ID27 to ID20): LCD module/driver version ID

Parameter Range: ID=80h to FFh

NOTE: See command RDDID (04h), 3rd parameter.

Restriction

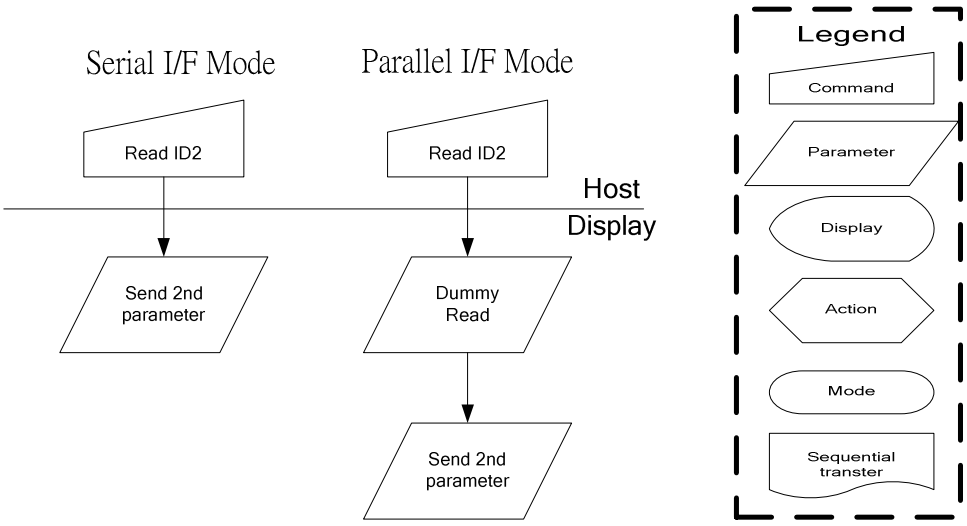
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not fixed
S/W Reset	Not fixed
H/W Reset	Not fixed

Flow Chart



9.1.38 RDID3: Read ID3 (DCH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	1	1	1	0	0	DCH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: "-" Don't care

Description

This read byte returns 8-bit LCD module/driver ID.

D7-D0 (ID37 to ID30): LCD module/driver ID.

NOTE: See command RDDID (04h), 4th parameter.

Restriction

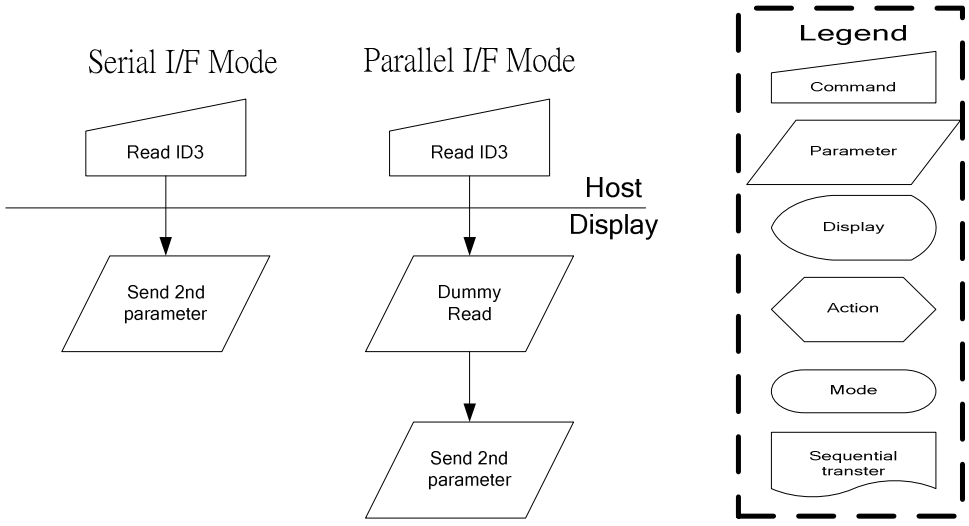
Register Availablility

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0Eh
S/W Reset	0Eh
H/W Reset	0Eh

Flow Chart



9.1.39 DutySet: Display Duty setting (B0H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
DutySet	0	1	0	1	0	1	1	0	0	0	0	**(B0h)**
Parameter	1	1	0	Du7	Du6	Du5	Du4	Du3	Du2	Du1	Du0	-

NOTE: "-" Don't care

Description

This command is used to set display duty. Command set = display duty numbers - 1.

Example:

Duty	Du6	Du5	Du4	Du3	Du2	Du1	Du0	Command set= Display duty numbers-1
Example: 1/128 duty	0	1	1	1	1	1	1	128-1=127

Restriction

Display duty must > 4 (1/4 duty)

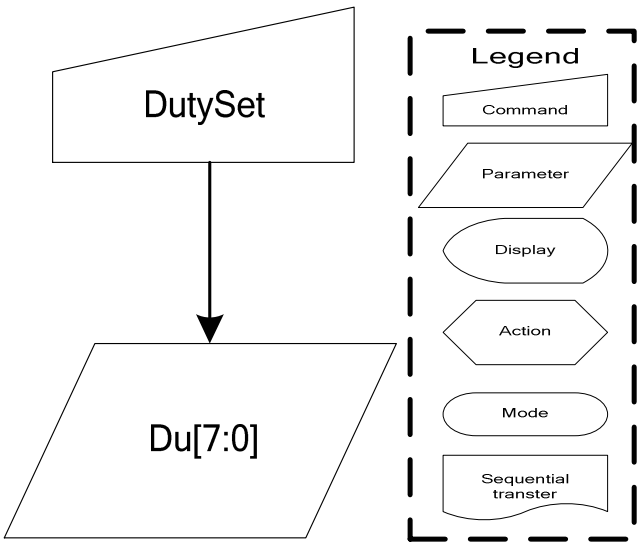
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Du[7:0])
Power On Sequence	10100001b (A1h)
S/W Reset	10100001b (A1h)
H/W Reset	10100001b (A1h)

Flow Chart



9.1.40 FirstCom: First Com. Page address (B1H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
FirstCom	0	1	0	1	0	1	1	0	0	0	1	**(B1h)**
Parameter	1	1	0	F7	F6	F5	F4	F3	F2	F1	F0	-

NOTE: "-" Don't care

Description

This command defines the first output COM number that mapping to the RAM page address 0. For detail setting value, please see the table as below.

F6	F5	F4	F3	F2	F1	F0	Line address
0	0	0	0			0	0
0	0	0	0			1	1
0	0	0	1			0	2
0	0	0	1			1	3
:	:	:	:			:	:
1	0	0	0	1	0	1	69

Example:

If FirstCom=8, common 8 would output the data of RAM page address 0.

Restriction

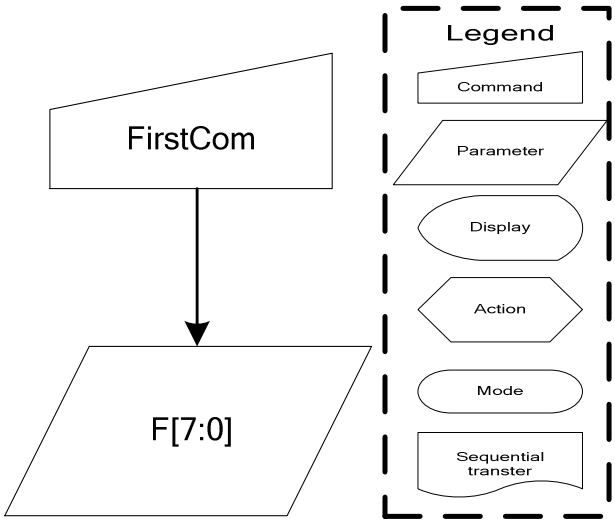
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (F[7:0])
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



9.1.41 OscDiv: FOSC Divider (B3H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
OscDiv	0	1	0	1	0	1	1	0	0	1	1	**(B3h)**
Parameter	1	1	0	-	-	-	-	-	-	CLD1	CLD0	-

NOTE: "-" Don't care

Description

This command is used to specify the CL dividing ratio.

CLD1, CLD0: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.

CLD1	CLD0	CL dividing ratio
0	0	Not divide
0	1	2 divisions
1	0	4 divisions
1	1	8 divisions

Restriction

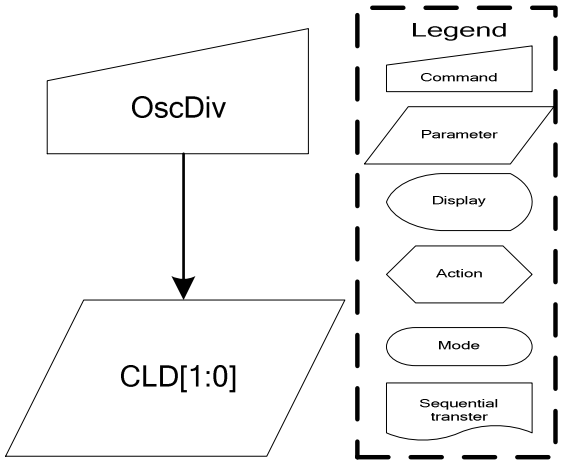
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (CLD[0:1])
Power On Sequence	00b
S/W Reset	00b
H/W Reset	00b

Flow Chart



9.1.42 PTLMOD: Partial Saving Power Mode Selection (B4H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
OscDiv	0	1	0	1	0	1	1	0	1	0	0	**(B4h)**
Parameter	1	1	0	PTLM	0	0	1	1	0	0	0	-

NOTE: "-" Don't care

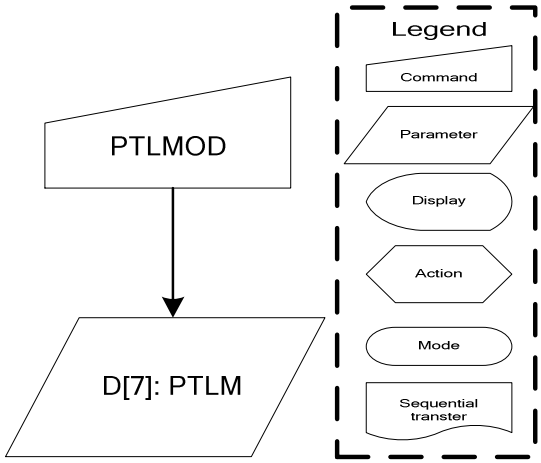
Description	Two type partial modes are built in ST7669. One is NORMAL MODE(PTLM=0) and another is POWER SAVING MODE(PTML=1). When entering power saving mode, IC would change bias, V0, booster pumping times special partial lines in order to save power consumptions.
Restriction	The power saving power mode is customerlized.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	18h
S/W Reset	18h
H/W Reset	18h

Flow Chart



9.1.43 NLInvSet: N-Line control (B5H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
NLInvSet	0	1	0	1	0	1	1	0	1	0	1	**(B5h)**
Parameter	1	1	0	M	N6	N5	N4	N3	N2	N1	N0	-

NOTE: "-" Don't care

Description

This command is used to set the inverted line number with range of 2 to (duty-1) to improve display quality. When M=0, inversion occurs in every frame; when M=1, inversion is independent from frames. If N[6:0]=0, N-line inversion function is disable.

Line inversion numbers=N[6:0] +1.

Example:

If N[6:0]=7, inversion occurs per 8 line.

Restriction

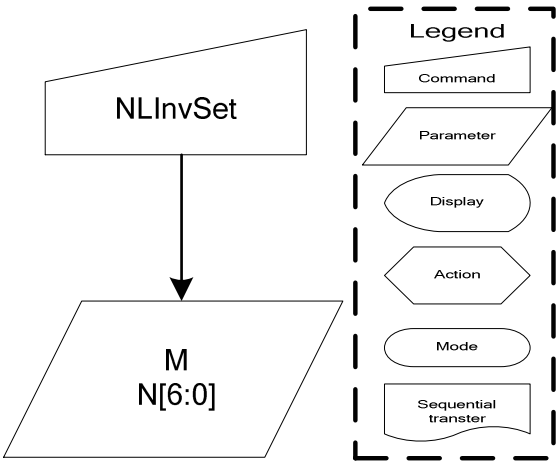
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	M	N[6:0]
Power On Sequence	0b	0000000b
S/W Reset	0b	0000000b
H/W Reset	0b	0000000b

Flow Chart



9.1.44 ComScanDir: Com/Seg Scan Direction for glass layout(B7H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
ComScanDir	0	1	0	1	0	1	1	0	1	1	1	**(B7h)**
Parameter	1	1	0	SMY	SMX	SINV	SML	SBGR	0	0	0	-

NOTE: "-" Don't care

Description

It is used to specify the common output direction in the pin of CSEL = L. This command helps to improve Common ITO layout tolerance on the LCM.

When CSEL=L configuration is selected, pins and common outputs are scanned in the order shown below.

	Function	0	1
SMY	Inverse the MY setting	Keep MY	Inverse MY
SMX	Inverse the MX setting	Keep MX	Inverse MX
SINV	Inverse the INVON setting	Keep INVON	Inverse INVON
SML	Inverse the ML setting	Keep ML	Inverse ML
SBGR	Inverse the BGR setting	Keep BGR	Inverse BGR

Restriction

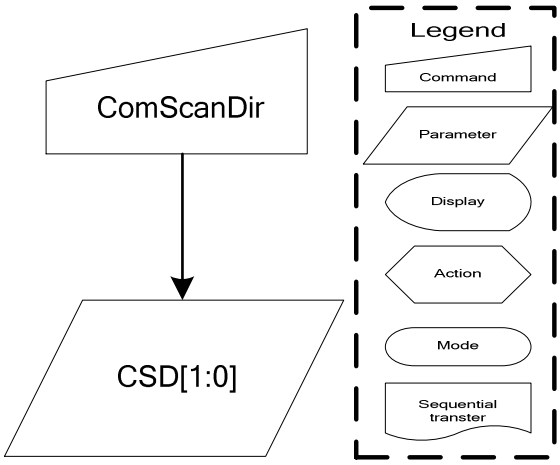
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (CSD[1:0])
Power On Sequence	00b
S/W Reset	00b
H/W Reset	00b

Flow Chart



9.1.45 RMWIN: Read Modify Write control in (B8H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RMWIN	0	1	0	1	0	1	1	1	0	0	0	**(B8h)**
Parameter	No Parameter											

NOTE: "-" Don't care

Description	Read modify write control IN
Restriction	
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes
Default	Status / Default Value Power On Sequence / -- S/W Reset / -- H/W Reset / --

9.1.46 RMWOUT: Read Modify Write control out(B9H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RMWOUT	0	1	0	1	0	1	1	1	0	0	1	**(B9h)**
Parameter	No Parameter											

NOTE: "-" Don't care

Description	Read modify write control OUT	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	--
	S/W Reset	--
	H/W Reset	--

9.1.47 VopSet: Vop set (C0H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
VopSet	0	1	0	1	1	0	0	0	0	0	0	**(C0h)**
1st parameter	1	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	-
2nd parameter	1	1	0	-	-	-	-	-	-	-	Vop8	

NOTE: "-" Don't care

Description	The command is used to program the optimum LCD supply voltage V0.
Restriction	

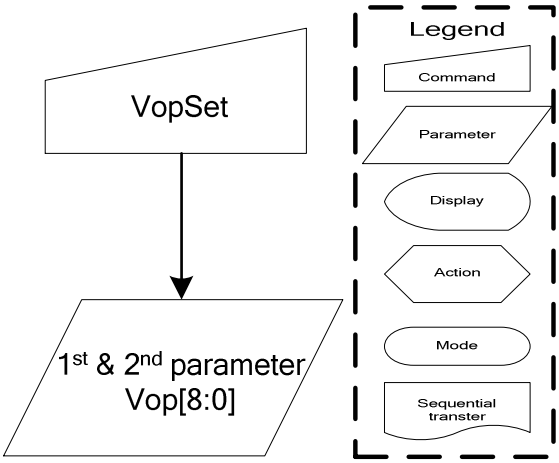
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Vop=12V)	
	Vop8	Vop[7:0]
Power On Sequence	0	11010010b (D2h)
S/W Reset	0	11010010b (D2h)
H/W Reset	0	11010010b (D2h)

Flow Chart



9.1.48 VopfsetInc: Vop Increase 1 (C1H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
VopOfsetInc	0	1	0	1	1	0	0	0	0	0	1	**(C1h)**

NOTE: "-" Don't care

Description

With the VopOfsetInc and VopOfsetDec command the V_{LCD} voltage and therewith the contrast of the LCD can be adjusted. This command increases the value of Vop offset register by 1.

If you set the electronic control value to 1111111, the control value is set to 0000000 after this command has been executed.

Restriction

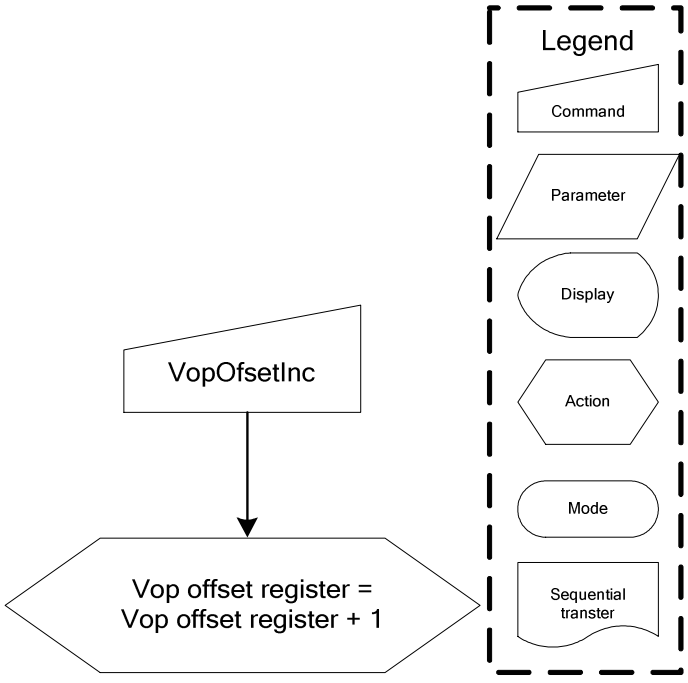
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



9.1.49 VopOfsetDec: Vop Decrease 1 (C2H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
VopOfsetDec	0	1	0	1	1	0	0	0	0	1	0	**(C2h)**

NOTE: "-" Don't care

Description

With the VopOfsetInc and VopOfsetDec command the V_{LCD} voltage and therewith the contrast of the LCD can be adjusted. This command decreases the value of Vop offset register by 1.

If you set the electronic control value to 0000000, the control value is set to 1111111 after this command has been executed.

Electronic Control Value	Decimal Equivalent	V0 Offset
0111111	63	+2520 mV
0111110	62	+2480 mV
0111101	61	+2440 mV
…	…	…
0000010	2	+80 mV
0000001	1	+40 mV
0000000	0	0 mV
1111111	-1	-40 mV
1111110	-2	-80 mV
…	…	…
1100010	-61	-2480 mV
1100001	-62	-2520 mV
1100000	-64	-2560mV

Possible Vop[6:0] values

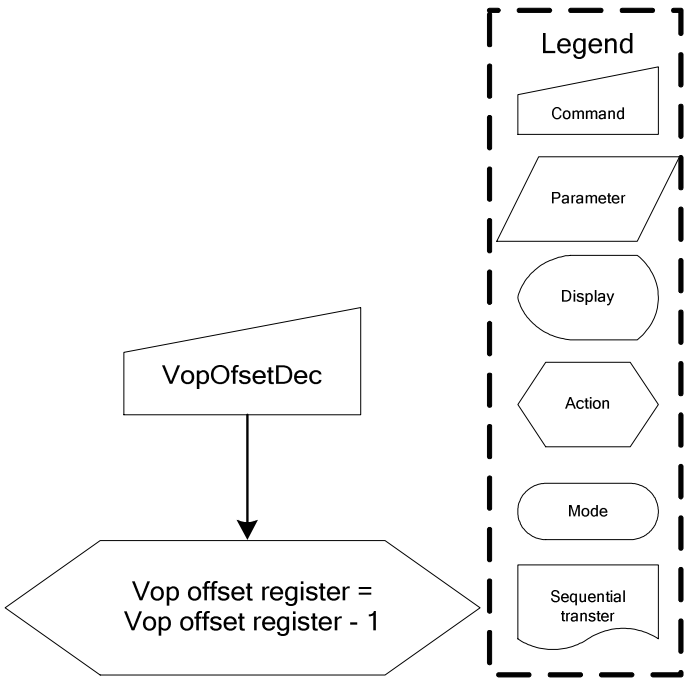
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart	

Legend
Command
Parameter
Display
Action
Mode
Sequential transter
VopOfsetDec
Vop offset register =
Vop offset register - 1

9.1.50 BiasSel: Bias Selection(C3H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
BiasSel	0	1	0	1	1	0	0	0	0	1	1	**(C3h)**
Parameter	1	1	0	-	-	-	-	-	Bias2	Bias1	Bias0	-

NOTE: "-" Don't care

Description

Select LCD bias ratio of the voltage required for driving the LCD.

Bais2	Bais1	Bais0	LCD bias
0	0	0	1/14
0	0	1	1/13
0	1	0	1/12
0	1	1	1/11
1	0	0	1/10
1	0	1	1/9
1	1	0	1/7
1	1	1	1/5

Restriction

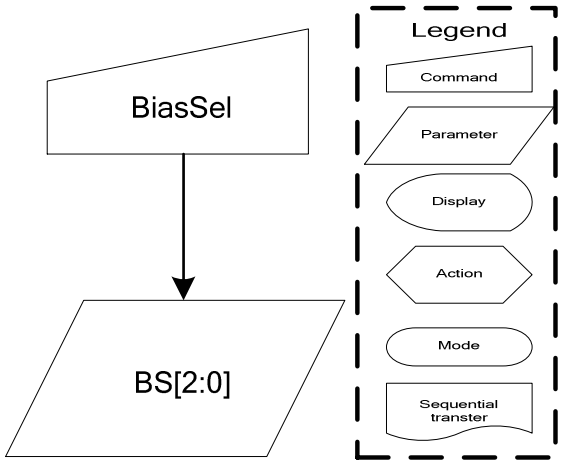
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Bias[2:0])
Power On Sequence	011b
S/W Reset	011b
H/W Reset	011b

Flow Chart



9.1.51 BstPmpXSel: Booster Set(C4H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
BstPmpXSel	0	1	0	1	1	0	0	0	1	0	0	**(C4h)**
Parameter	1	1	0	-	-	-	-	-	BST2	BST 1	BST0	-

NOTE: "-" Don't care

Description

Booster setting

BST2	BST1	BST0	
0	0	0	X1 boosting circuit (Booster off)
0	0	1	X2 boosting circuit
0	1	0	X3 boosting circuit
0	1	1	X4 boosting circuit
1	0	0	X5 boosting circuit
1	0	1	X6 boosting circuit
1	1	0	X7 boosting circuit
1	1	1	X8 boosting circuit

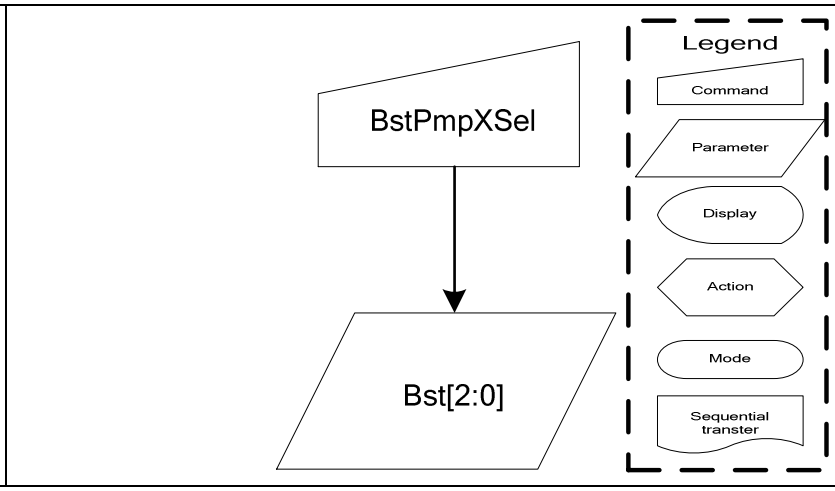
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (BST[2:0])
Power On Sequence	111b
S/W Reset	111b
H/W Reset	111b

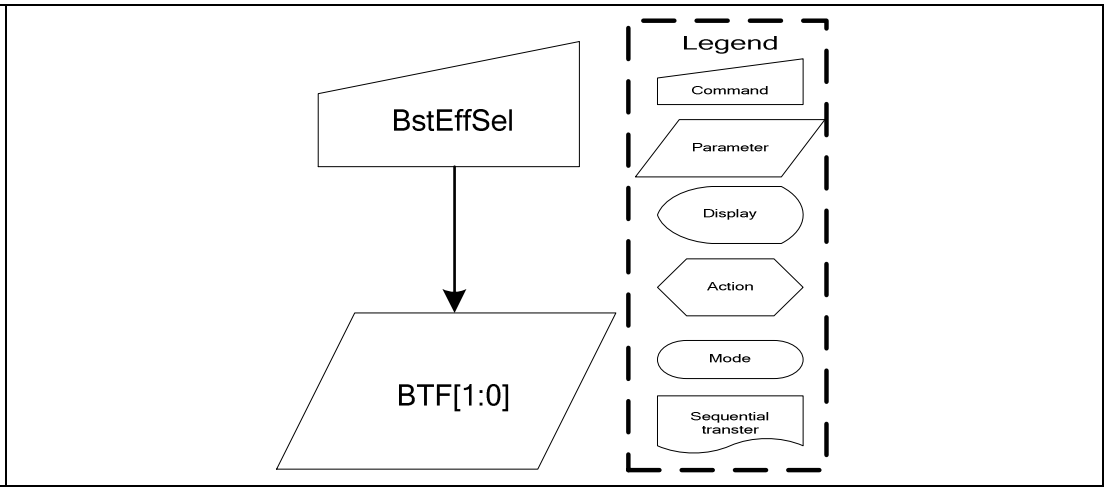
Flow Chart	 BstPmpXSel Bst[2:0] Legend Command Parameter Display Action Mode Sequential transter

9.1.52 BstEffSel: Booster Efficiency selection(C5H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
BstEffSel	0	1	0	1	1	0	0	0	1	0	1	**(C5h)**
Parameter	1	1	0	-	-	1	0	-	-	BTF1	BTF0	-

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>Booster Efficiency set
<table>
<tr><td>BTF1</td><td>BTF0</td><td>Frequency (Hz)</td></tr>
<tr><td>0</td><td>0</td><td>Level 1</td></tr>
<tr><td>0</td><td>1</td><td>Level 2 (default)</td></tr>
<tr><td>1</td><td>0</td><td>Level 3</td></tr>
</table>
By Booster Stages (2X, 3X, 4X, 5X, 6X, 7X, 8X) and Booster Efficiency (Level1~3) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level3 is higher than level1). The Boost Efficiency is better than lower level, and it just need few more power consumption current.</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value (BTF[1:0])</td></tr>
<tr><td>Power On Sequence</td><td>01b</td></tr>
<tr><td>S/W Reset</td><td>01b</td></tr>
<tr><td>H/W Reset</td><td>01b</td></tr>
</table></td></tr>
</table>

Flow Chart	

BstEffSel
BTF[1:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.53 VopOffset: Vop offset fuse bit adjust(C7H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
VopOffset	0	1	0	1	1	0	0	0	1	1	1	**(C7h)**
Parameter1	1	1	0	VOS7	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0	**-**
Parameter2	1	1	0	-	-	-	-	-	-	-	VOS8	**-**

NOTE: "-" Don't care

Description

The command is used to the Vop offset for V0. For VOS[8:0] setting, please see the following table:

VOS[8]	VOS[7:0]	(Dec)	V0 Offset
0	11111111	255	+10200 mV
	11111110	254	+10160 mV
	11111101	253	+10120 mV
	…	…	…
	00000010	2	+80 mV
	00000001	1	+40 mV
	00000000	0	0 mV
1	11111111	-1	-40 mV
	11111110	-2	-80 mV
	…	…	…
	00000010	-253	-10120 mV
	00000001	-254	-10160 mV
	00000000	-255	-10200 mV

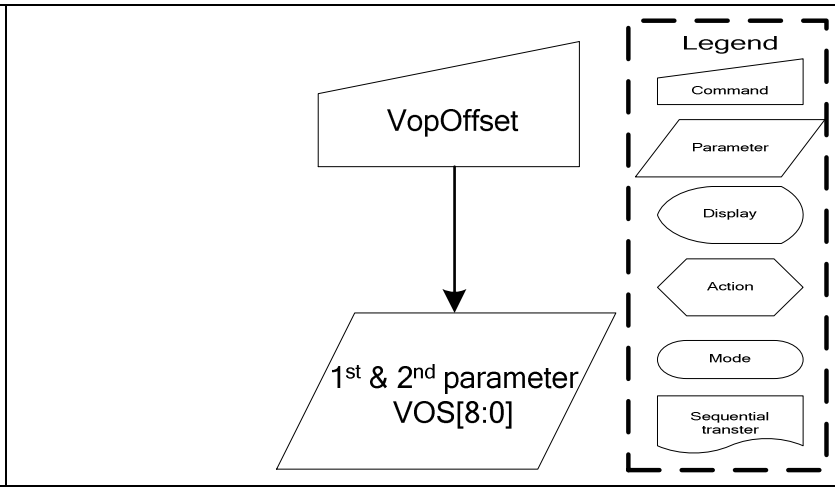
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

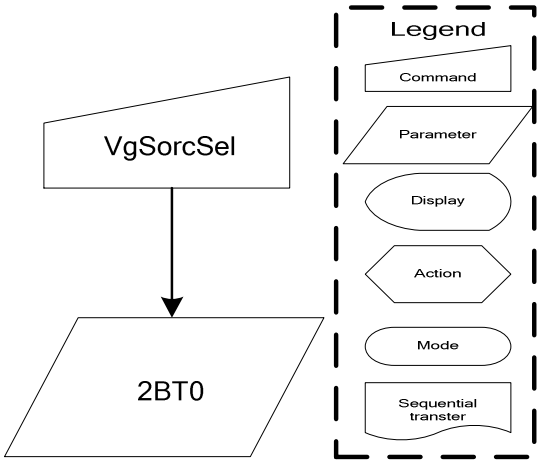
Status	Default Value	
	VOS8	VOS[7:0]
Power On Sequence	0	0
S/W Reset	0	0
H/W Reset	0	0

Flow Chart	 VopOffset 1st & 2nd parameter VOS[8:0] Legend Command Parameter Display Action Mode Sequential transter

9.1.54 V3SorcSel: FV3 with Bst2x control(CBH)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
V3SorcSel	0	1	0	1	1	0	0	1	0	1	1	**(CBh)**
Parameter	1	1	0	-	-	-	-	-	-	-	2BT0	-

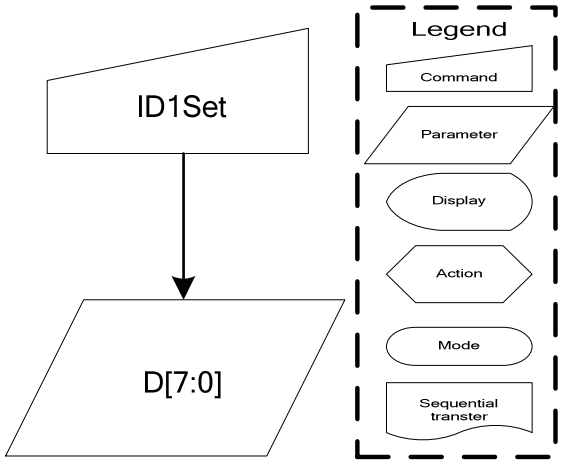
NOTE: "-" Don't care

Description	2BT0=0: Vg source comes from VDD2 ; 2BT0=1: Vg source comes from 2-times charge pump.
Restriction	
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value (2BT0) Power On Sequence: 0 S/W Reset: 0 H/W Reset: 0
Flow Chart	

9.1.55 ID1Set : ID1 setting(CCH)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
ID1Set	0	1	0	1	1	0	0	1	1	0	0	**(CCh)**
Parameter	1	1	0	ID1_7	ID1_6	ID1_5	ID1_4	ID1_3	ID1_2	ID1_1	ID1_0	-

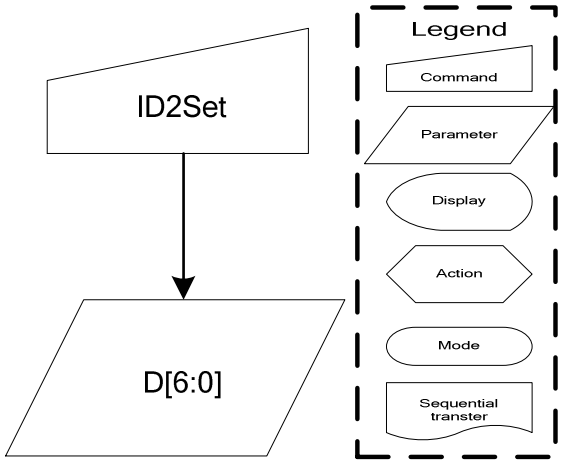
NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>ID1 setting for OPT program data input</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>45h</td></tr>
<tr><td>S/W Reset</td><td>45h</td></tr>
<tr><td>H/W Reset</td><td>45h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

9.1.56 ID2Set : ID2 setting(CDH)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
ID2Set	0	1	0	1	1	0	0	1	1	0	1	**(CDh)**
Parameter	1	1	0	1	ID2_6	ID2_5	ID2_4	ID2_3	ID2_2	ID2_1	ID2_0	**-**

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>ID2 setting for OPT program data input</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>0</td></tr>
<tr><td>S/W Reset</td><td>0</td></tr>
<tr><td>H/W Reset</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

9.1.57 ID3Set : ID3 setting(CEH)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
ID3Set	0	1	0	1	1	0	0	1	1	1	0	**(CEh)**
Parameter	1	1	0	ID3_7	ID3_6	ID3_5	ID3_4	ID3_3	ID3_2	ID3_1	ID3_0	-

NOTE: "-" Don't care

Description	ID3 setting for OPT program data input
Restriction	

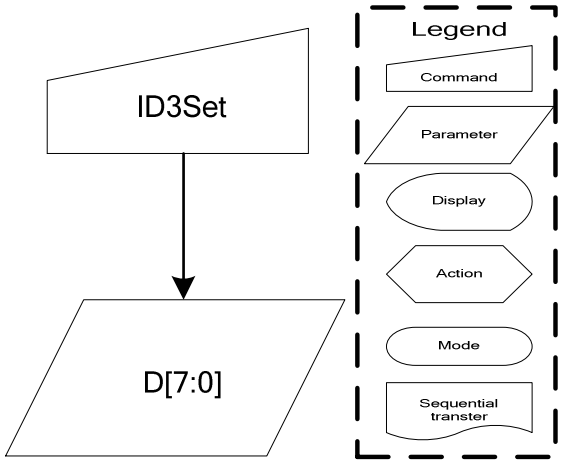
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0
S/W Reset	0
H/W Reset	0

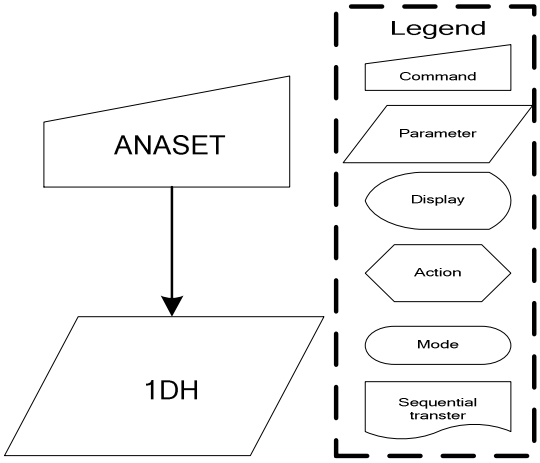
Flow Chart



9.1.58 ANASET: Analog circuit setting(D0H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
AutoLoadSet	0	1	0	1	1	0	1	0	0	0	0	**(D0h)**
Parameter	1	1	0	0	0	0	1	1	1	0	1	**-**

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>Analog circuit setting.</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value D[7:0]</td></tr>
<tr><td>Power On Sequence</td><td>1Dh</td></tr>
<tr><td>S/W Reset</td><td>1Dh</td></tr>
<tr><td>H/W Reset</td><td>1Dh</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

9.1.59 AutoLoadSet : mask rom data auto re-load control(D7H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
AutoLoadSet	0	1	0	1	1	0	1	0	1	1	1	**(D7h)**
Parameter	1	1	0	EXTE	OTPBE	-	ARD	-	-	-	-	**-**

NOTE: "-" Don't care

Description

Mask rom data auto re-load control

EXTE : External command enable (OTP input), 1: enable, 0: disable

OTPBE: OTPB auto-read enable (OTP input), 1: enable, 0: disable

ARD : OTP auto read enable control, 1: Disable OTP auto read,
0: Enable OTP auto read

Restriction

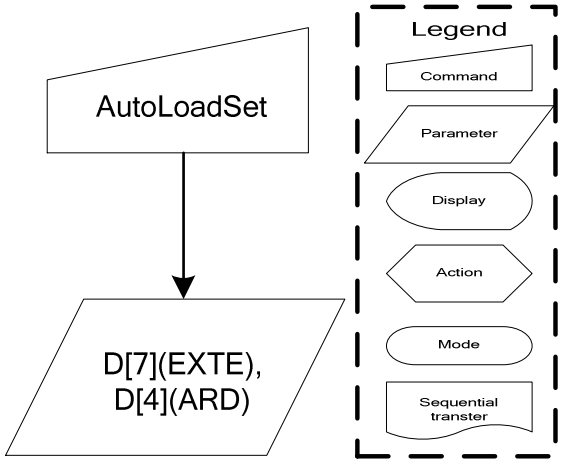
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	EXTE	ARD
Power On Sequence	0	0
S/W Reset	0	0
H/W Reset	0	0

Flow Chart



9.1.60 RDTstStatus : Read IC status(DEH)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
RDTstStatus	0	1	0	1	1	0	1	1	1	1	0	**(DEh)**
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	
Parameter	1	0	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	**-**

NOTE: "-" Don't care

Description	Read IC status. Contect of OTP / RDA / PWR_VOP read control (selection Byte by StusOutByteSel[3:0] control)
Restriction	

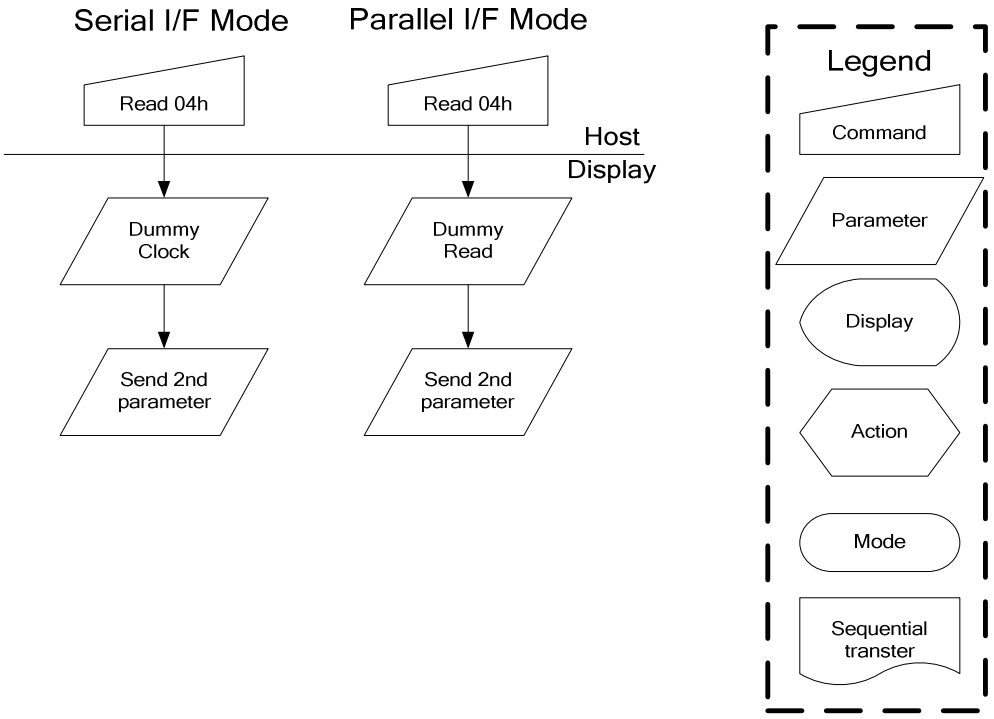
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	-
S/W Reset	-
H/W Reset	-

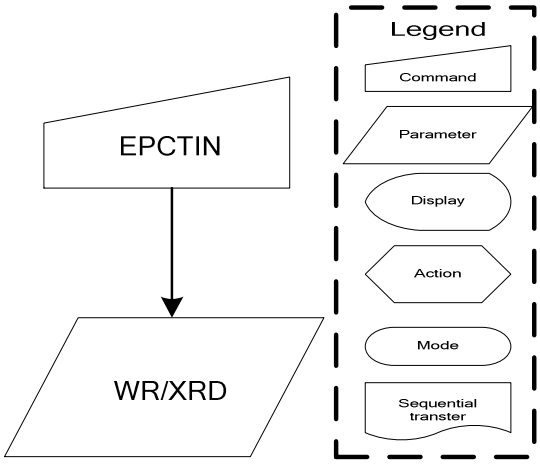
Flow Chart



9.1.61 EPCTIN: Control OTP WR/RD(E0H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
EPCTIN	0	1	0	1	1	1	0	0	0	0	0	**(E0h)**
Parameter	1	1	0	0	0	WR /XRD	0	0	0	0	0	-

NOTE: "-" Don't care

Description	WR/XRD: when setting "1" ➔ The Write Enable of OTP will be opened. WR/XRD: when setting "0" ➔ The Read Enable of OTP will be opened.
Restriction	
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value (WR/XRD) Power On Sequence: 0 S/W Reset: 0 H/W Reset: 0
Flow Chart	

9.1.62 EPCOUT: OTP control cancel(E1H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
EPCOUT	0	1	0	1	1	1	0	0	0	0	1	**(E1h)**

NOTE: "-" Don't care

Description	IC exits the OTP control circuit when executing this command.
Restriction	

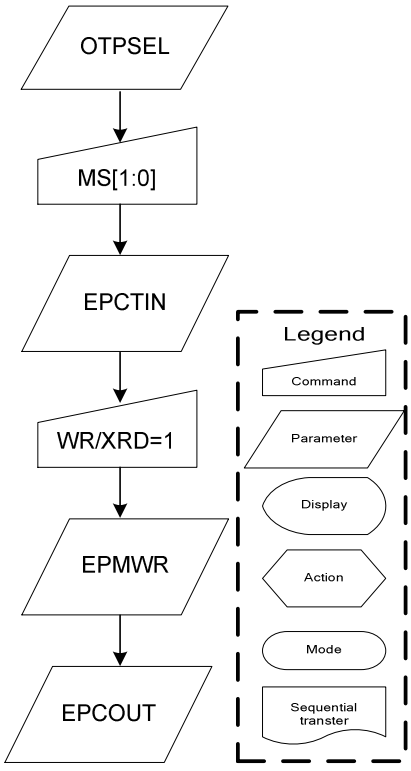
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



9.1.63 EPMWR: Write to OTP(E2H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
EPCOUT	0	1	0	1	1	1	0	0	0	1	0	**(E2h)**

NOTE: "-" Don't care

Description	IC actives trigger to start OTP programming when executing this command.
Restriction	

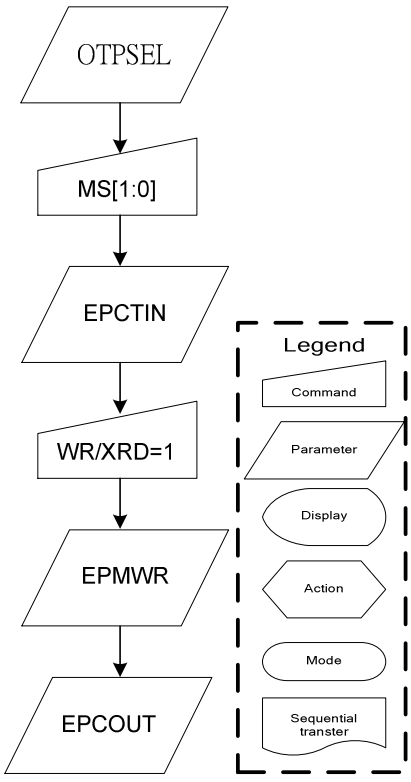
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



9.1.64 EPMRD: Read from OTP(E3H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
EPMRD	0	1	0	1	1	1	0	0	0	1	1	**(E3h)**

NOTE: "-" Don't care

Description	IC actives trigger to start OTP data download to circuit when executing this command.
Restriction	

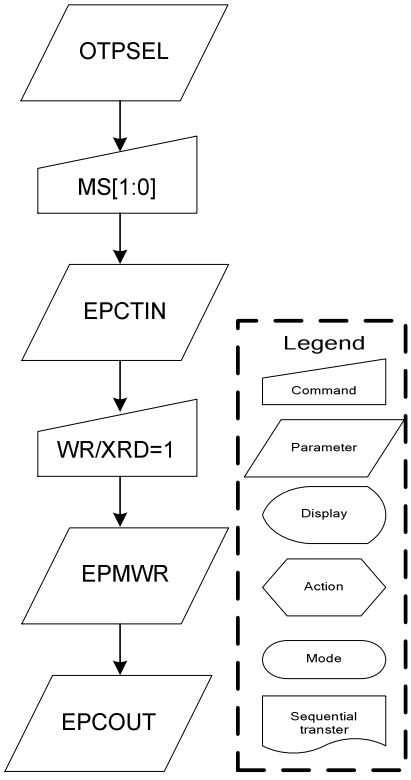
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart



9.1.65 OTPSEL: SEL OTP(E4H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
OTPSEL	0	1	0	1	1	1	0	0	1	0	0	**(E4h)**
Parameter	1	1	0	MS1	MS0	0	1	1	0	0	0	-

NOTE: "-" Don't care

Description

This command defines OTPA/OTPB selection for EEPROM control. Please see the table as below:

MS1	MS0	Mode
0	0	Disable
0	1	OTP
1	0	OTPA
1	1	OTPB

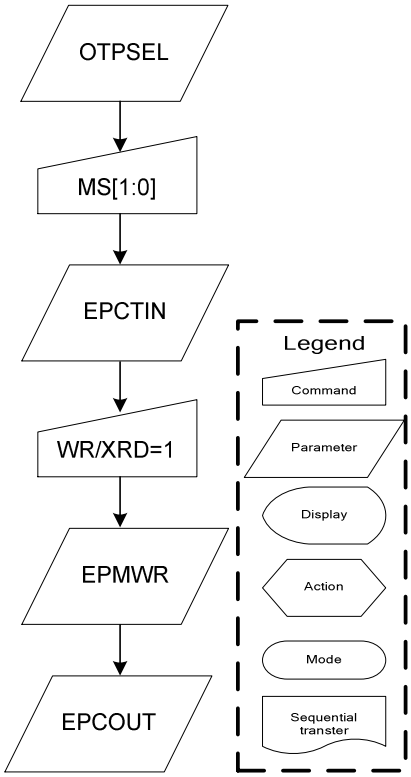
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

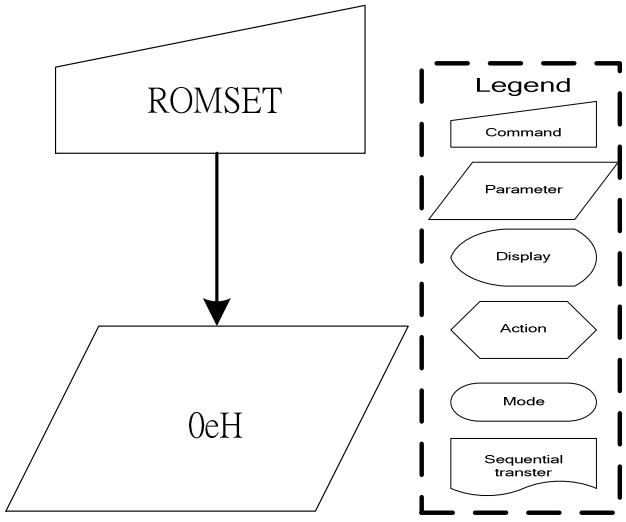
Status	Default Value (MS[1:0])
Power On Sequence	00
S/W Reset	00
H/W Reset	00

Flow Chart	 OTPSEL MS[1:0] EPCTIN WR/XRD=1 EPMWR EPCOUT Legend Command Parameter Display Action Mode Sequential transter

9.1.66 ROMSET: Programmable rom setting(E5H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
AutoLoadSet	0	1	0	0	1	1	1	0	1	0	1	**(E5h)**
Parameter	1	1	0	0	0	0	0	1	1	1	0	-

NOTE: "-" Don't care

<table>
<tr><td>Description</td><td>Set the OTP writing timing. Value 0x0e is the best value for ST7669.</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value D[7:0]</td></tr>
<tr><td>Power On Sequence</td><td>0Fh</td></tr>
<tr><td>S/W Reset</td><td>0Fh</td></tr>
<tr><td>H/W Reset</td><td>0Fh</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

9.1.67 HPMSET : High Power Mode Setting (EBH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	0	1	0	1	1	EBH
1st parameter	1	1	0	0	0	0	0	0	0	HP1	HP0	
2nd parameter	1	1	0	0	0	0	0	0	0	0	0	

Description

High power mode for volatage compensation.

HP1	HP0	Status
0	0	Level 1 (Default)
0	1	Level 2
1	0	Level 3

Restriction

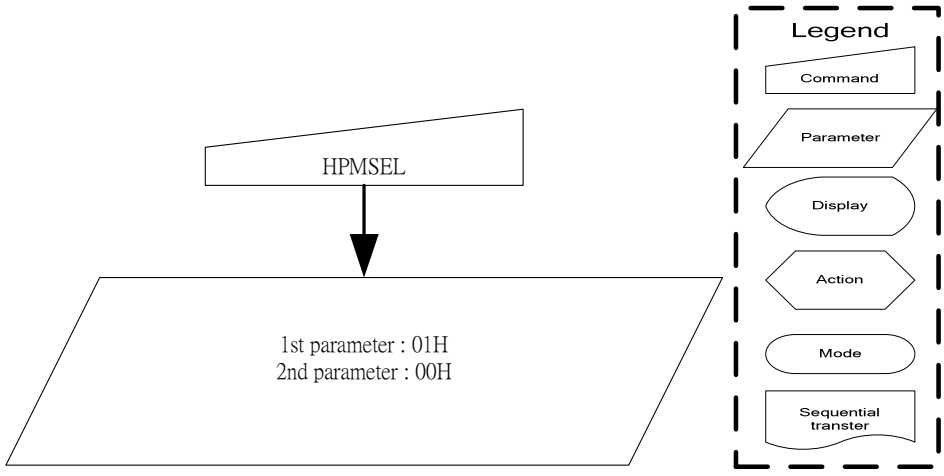
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	HP[3:0]
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



9.1.68 FRMSEL: Frame Freq. in Temp. range (F0H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	0	0	F0H
1st parameter	1	1	0	-	-	-	DIVA	FA3	FA2	FA1	FA0	Range A
2nd parameter	1	1	0	-	-	-	DIVB	FB3	FB2	FB1	FB0	Range B
3rd parameter	1	1	0	-	-	-	DIVC	FC3	FC2	FC1	FC0	Range C
4th parameter	1	1	0	-	-	-	DIVD	FD3	FD2	FD1	FD0	Range D

Description

Select Frame Freq. in normal display mode.

1st parameter : Frame freq. value set in temperature range 30(-30℃) to TA

2nd parameter : Frame freq. value set in temperature P range TA to TB

3rd parameter : Frame freq. value set in temperature range TB to TC

4th parameter : Frame freq. value set in temperature range TC to 145(90℃)

For command setting to frame rate value look-up-table, please see the following table:

DIVx	Fx[3:0]	Frame Rate (Hz) (+/- 10% tolerance)
1	0	75
	1	76
	2	77
	3	80
	4	84
	5	88
	6	92
	7	97
	8	102
	9	108
	A	115
	B	123
	C	133
	D	144
	E	155
	F	170
0	0~F	(Frame Rate)/2

Restriction

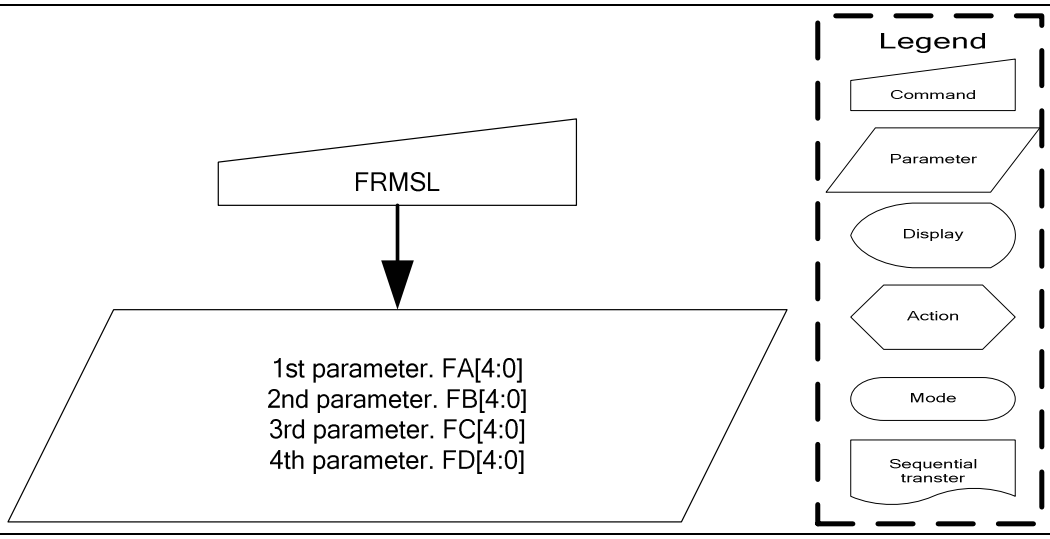
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	FA[4:0]	FB[4:0]	FC[4:0]	FD[4:0]
Power On Sequence	06h	0Bh	0Dh	12h
S/W Reset	06h	0Bh	0Dh	12h
H/W Reset	06h	0Bh	0Dh	12h

Flow Chart



9.1.69 FRM8SEL: Frame Freq. in Temp. range (idel-8 color) (F1H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	0	1	F1H
1st parameter	1	1	0	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0	Range A
2nd parameter	1	1	0	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0	Range B
3rd parameter	1	1	0	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0	Range C
4th parameter	1	1	0	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0	Range D

Description

Select Frame Freq. in normal display mode.(idle;8 color mode)

1st parameter : Frame freq. value set in TEMP range 30(-30℃) to TA

2nd parameter : Frame freq. value set in TEMP range TA to TB

3rd parameter : Frame freq. value set in TEMP range TB to TC

4th parameter : Frame freq. value set in TEMP range TC to 145(90℃)

Restriction

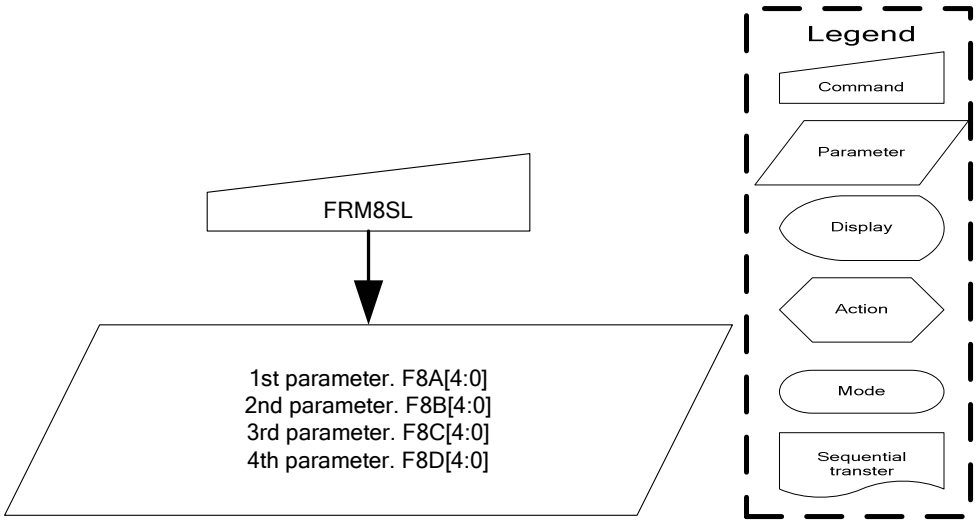
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	FA[4:0]	FB[4:0]	FC[4:0]	FD[4:0]
Power On Sequence	06h	0Bh	0Dh	12h
S/W Reset	06h	0Bh	0Dh	12h
H/W Reset	06h	0Bh	0Dh	12h

Flow Chart


FRM8SL
1st parameter. F8A[4:0]
2nd parameter. F8B[4:0]
3rd parameter. F8C[4:0]
4th parameter. F8D[4:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.70 TMPRNG: Temp. range set for Frame Freq. Adj. (F2H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	1	0	F2H
1st parameter	1	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	Range A
2nd parameter	1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	Range B
3rd parameter	1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	Range C

Description

Temp. range set for automatic frame freq. adj. operation according the current temp. value.

1st parameter: Temp. range A value set

2nd parameter: Temp. range B value set

3rd parameter: Temp. range C value set

TA/TB/TC Temperature(℃) + 40 = TA/TB/TC[6:0]

Example:

If TA wants to be set at 24℃, TA[6:0]=24+40=64(40h),

Restriction

-40℃≦TA≦TA+TH≦TB≦TB+TH≦TC≦87℃

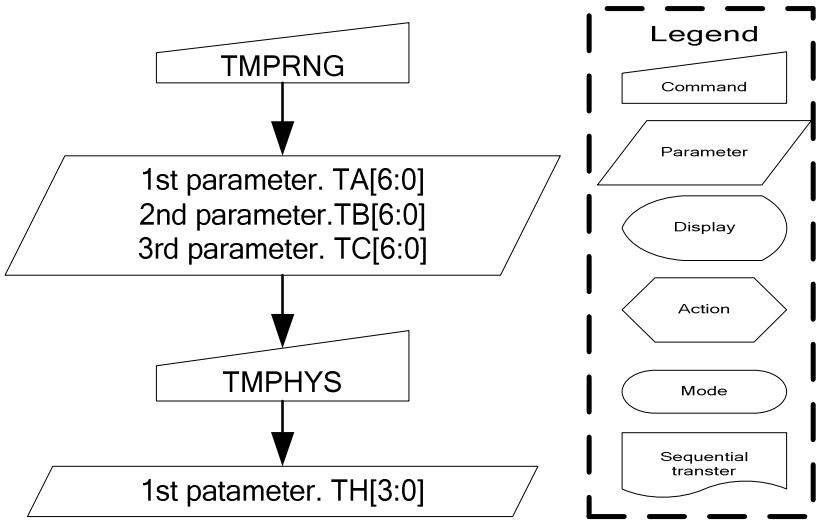
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	TA[6:0]	TB[6:0]	TC[6:0]
Power On Sequence	1Eh	28h	32h
S/W Reset	1Eh	28h	32h
H/W Reset	1Eh	28h	32h

Flow Chart	


TMPRNG
1st parameter. TA[6:0]
2nd parameter.TB[6:0]
3rd parameter. TC[6:0]
TMPHYS
1st patameter. TH[3:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.71 TMPHYS: Temp.Hysteresis Set for Frame Freq. Adj.(F3H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	1	1	F3H
1st parameter	1	1	0	-	-	-	-	TH3	TH2	TH1	TH0	

Description

Temp. hysteresis range set for frame freq. adj.

Parameter TH[3:0] is used to set Temp. hysteresis range.

The relationship between temp. state and temp. range value is shown below.

TEMP Range Value	TEMP Rising State	TEMP Falling State
Freq. changing point A	TA[6:0]+TH[3:0]	TA[6:0]
Freq. changing point B	TB[6:0]+TH[3:0]	TB[6:0]
Freq. changing point C	TC[6:0]+TH[3:0]	TC[6:0]

TH Temperature(℃) - 1 = TH[3:0]

Example:

If TH wants to set 5℃, TH[3:0]=5-1=4.

Restriction

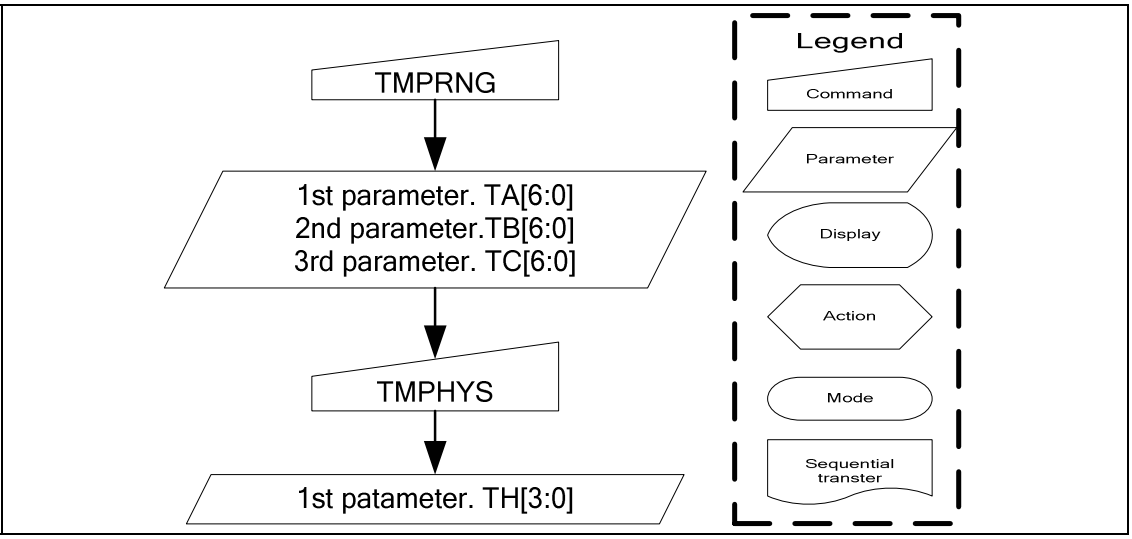
Temp. hysteresis value should be smaller than the gap of temp. range.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value(TH[3:0])
Power On Sequence	4H
S/W Reset	4H
H/W Reset	4H

Flow Chart	

TMPRNG
1st parameter. TA[6:0]
2nd parameter.TB[6:0]
3rd parameter. TC[6:0]
TMPHYS
1st patameter. TH[3:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.72 TEMPSEL: Temp. Set(F4H)

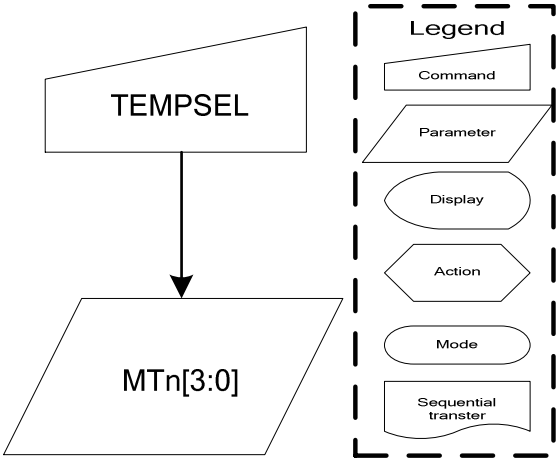
Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
TEMPSEL	0	1	0	1	1	1	1	0	1	0	0	**(F4h)**
1st parameter	1	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00	MT1x: (-24 °C to -32 °C) MT0x: (-32 °C to -40 °C)
2nd parameter	1	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	MT3x: (-8 °C to -16 °C) MT2x: (-16 °C to -24 °C)
3rd parameter	1	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	MT5x: (8 °C to 0 °C) MT4x: (0 °C to -8 °C)
4th parameter	1	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	MT7x: (24 °C to16 °C) MT6x: (16 °C to 8 °C)
5th parameter	1	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	MT9x: (40 °C to 32 °C) MT8x: (32 °C to 24 °C)
6th parameter	1	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	MTBx: (56 °C to 48 °C) MTAx: (48 °C to 40 °C)
7th parameter	1	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	MTDx: (72 °C to 64 °C) MTCx: (64 °C to 56 °C)
8th parameter	1	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	MTFx: (87 °C to 80 °C) MTEx: (80 °C to 72 °C)

NOTE: "-" Don't care

Description

This command defines temperature gradient compensation coefficient. For this command detail description and opearation, please see Section 7.10.

Parameter n	**MT n 3**	**MT n 2**	**MT n 1**	**MT n 0**	**Voltage / °C (+/- 3mv tolerance)**
0	**0**	**0**	**0**	**0**	**+5 mv / °C**
1	**0**	**0**	**0**	**1**	**0 mv / °C**
2	**0**	**0**	**1**	**0**	**-5 mv / °C**
3	**0**	**0**	**1**	**1**	**-10 mv / °C**
:	**:**	**:**	**:**	**:**	**:**
:	**:**	**:**	**:**	**:**	**:**
:	**:**	**:**	**:**	**:**	**:**
12	**1**	**1**	**0**	**0**	**-55 mv / °C**
13	**1**	**1**	**0**	**1**	**-60 mv / °C**
14	**1**	**1**	**1**	**0**	**-65 mv / °C**
15	**1**	**1**	**1**	**1**	**-70 mv / °C**

<table>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value (MTn[3:0])</td></tr>
<tr><td>Power On Sequence</td><td rowspan="3">1st parameter 0xFF
2nd parameter 0x2F
3rd parameter 0x0A
4th parameter 0x35
5th parameter 0x31
6th parameter 0x40
7th parameter 0xA7
8th parameter 0x13</td></tr>
<tr><td>S/W Reset</td></tr>
<tr><td>H/W Reset</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

9.1.73 THYS : Temperature detection threshold(F7H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
THYS	0	1	0	1	1	1	1	0	1	1	1	**(F7h)**
Parameter	1	1	0	THYS7	THYS6	THYS5	THYS4	THYS3	THYS2	THYS1	THYS0	-

NOTE: "-" Don't care

Description	Temperature detection threshold setting.
Restriction	

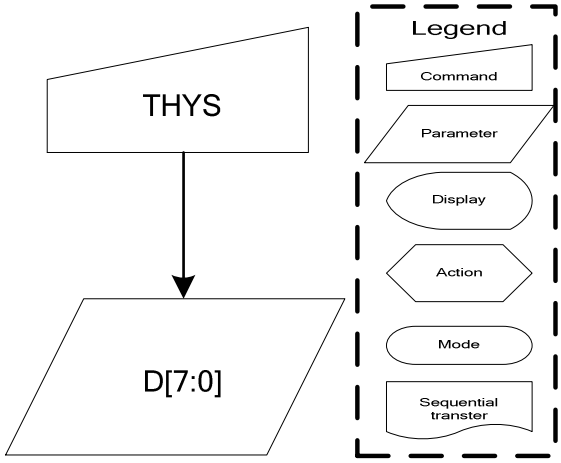
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value D[7:0]
Power On Sequence	06h
S/W Reset	06h
H/W Reset	06h

Flow Chart



9.1.74 Frame Set: Frame PWM Set (F9H)

Command	*A0*	*/RD*	*/WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Hex*
Frame1 Set	0	1	0	1	1	1	1	1	0	0	1	**(F9h)**
1st parameter	1	1	0	-	-	-	P14	P13	P12	P11	P10	-
2nd parameter	1	1	0	-	-	-	P24	P23	P22	P21	P20	-
:	:	:	:	:	:	:	:	:	:	:	:	-
15th parameter	1	1	0	-	-	-	P154	P153	P152	P151	P150	-
16th parameter	1	1	0	-	-	-	P164	P163	P162	P161	P160	-

NOTE: "-" Don't care

Description	This command is used to set frame PWM.
Restriction	

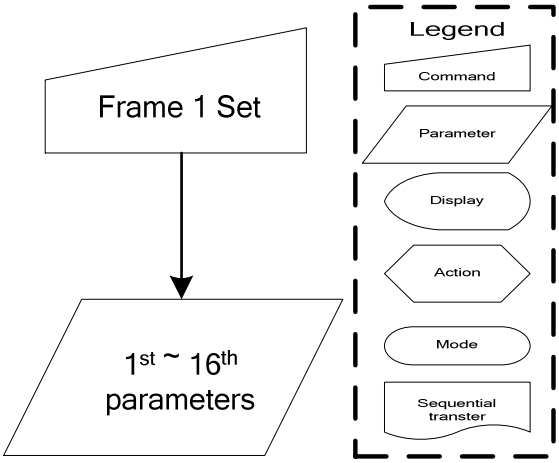
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



The default value of RGB level set

	FRAM SET
RGB level0	00
RGB level1	04
RGB level2	05
RGB level3	08
RGB level4	0B
RGB level5	0C
RGB level6	0E
RGB level7	0F
RGB level8	11
RGB level9	12
RGB level10	13
RGB level11	14
RGB level12	16
RGB level13	17
RGB level14	19
RGB level15	1B

1. All the modulation range of each level for each frame is from 00’H to 1F’H.

2. The setting value is base on LCD module state.

10. SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Item	Symbol	Value	Unit
Supply voltage (1)	V_{DD}	- 0.3 ~ + 3.0	V
Supply voltage (1)	$V_{DD2,VDD3,VDD4,VDD5}$	- 0.3 ~ + 4.2	V
Supply voltage (2)	V0 (V0-VSS)	- 0.3 ~ + 18.0	V
Supply voltage (3)	V_{MAX} (V0- XV0)	- 0.3 ~ + 18.0	V
Input voltage range	V_{IN}	- 0.3 ~ V_{DD} + 0.5	V
Output voltage range	V_O	- 0.3 ~ V_{DD} + 0.5	V
Operating temperature range	T_{OPR}	- 30 ~ + 85	℃
Storage temperature range	T_{STG}	- 40 ~ + 125	℃

NOTE:

(1). Voltages are all based on VSS = 0V.

(2). Voltage relationship: V0. Vg. Vm. VSS. XV0 must always be satisfied.

(3). For External Supply

(4).These is the stress ratings only above the table. "Absolute Maximum Ratings" may cause permanent damage to this device.

10.2 DC CHARACTERISTICS

10.2.1 Basic Characteristics

(V_{SS}=0V, Ta = -30 to 70℃)

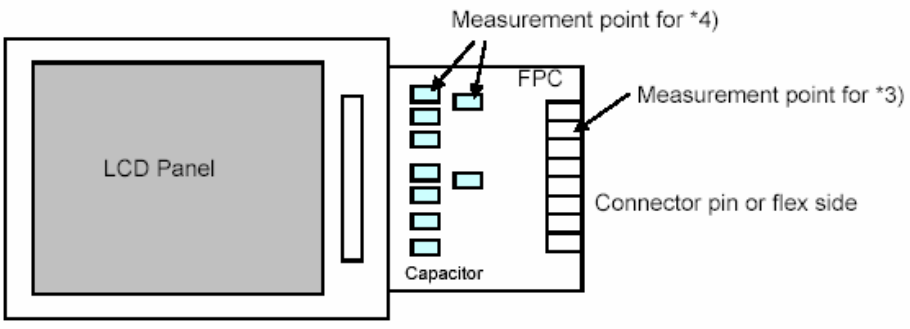
Parameter	Symbol	Conditions	Related Pins	MIN	TYP	MAX	Unit
Logic Operating voltage	V_{DDI}	-	*2) VDD	1.65	1.8	3.0	V
Analog Operating voltage	V_{DDA}	-	*2) VDD2,3,4,5	2.4	2.75	3.3	
Driving voltage input	V_{LCD}	V0 - VSS	*3) V0, VSS	-	-	18.0	
	XV_{LCD}	VSS – XV0	*3) VSS, XV0	-	-	18.0	
High level input voltage	V_{IH}		*1) *2)	0.7V_{DD}	-	V_{DD}	
Low level input voltage	V_{IL}	-	*1) *2)	V_{SS}	-	0.3V_{DD}	
High level output voltage	V_{OH}	I_{OH} = -1.0mA	*2) SI, TE	0.8V_{DD}	-	V_{DD}	
Low level output voltage	V_{OL}	I_{OL} = +1.0mA		V_{SS}	-	0.2V_{DD}	
Input leakage current	I_{IL}	V_{IN} = V_{DD} or V_{SS}	*1), *2)	-1.0	-	+1.0	μA
Driver on resistance (SEG)	R_{ONSEG}	Vg = 5.0V	S0 to S395	-	3.5	1.0	KΩ
Driver on resistance (COM)	R_{ONCOM}	V0 = 10.0V	C0 to C161	-	0.4	1.0	
External oscillator frequency	f_{OSC}	fFR=77Hz	CL	-	773.4	-	kHz
Booster1 output voltage range	V0		VDD2	-	-	18	V
Reference voltage	V_{REF}	No load	-	1.75	1.8	1.85	V
Voltage follower output voltage	Vm	Ta = 25℃	-	0.7	Vg/2	VDDA-0.7	V
Booster2 output voltage range	Vg		VDD2	1.8	-	VDDAX2	V
Booster3 output voltage range	XV0		VDD2	Vg-18	-	-	V

NOTE:

**1) Applies to IF0, IF1, IF3, /CS, /RST, /WR, /RD, A0 (SCL) and*

D15-D2, D1 (A0) ,D0(SI) pins

**2) *3) When the measurement are performed with LCD module, Measurement Points are like below.*



10.2.2 Current Consumption (Bare die)

Host I/F	Mode of operation	Frame Frequency	Image	Memory Data Access Control (MY:MX:MV)	Current consumption (mA)			
					Typical		Worst case	
					VDDA	VDDI	VDDA	VDDI
Host interface NOT active	- **Normal** Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	77Hz±10 %	Note 1	X;X;X	0.6	0.15	1.0	0.3
			Note 2	X;X;X	0.6	0.15	1.0	0.3
			Note 3	X;X;X	0.6	0.15	1.0	0.3
			Note 4	X;X;X	0.6	0.15	1.0	0.3
			Note 5	X;X;X	0.6	0.15	1.0	0.3
			Note 7	X;X;X	0.7	0.15	1.0	0.3
	- Normal Mode On - Partial Mode Off - **Idle** Mode On - Sleep Out Mode	77Hz±10 %	Note 5	X;X;X	0.6	0.15	1.0	0.3
	- Normal Mode Off - **Partial** Mode On (32 lines) - Idle Mode Off - Sleep Out Mode	77Hz±10 %	Grey Levels	X;X;X	0.4	0.1	1.0	0.3
	- Normal Mode Off - **Partial** Mode On (32 lines) - **Idle** Mode On - Sleep Out Mode	77Hz±10 %	Levels	X;X;X	0.4	0.1	1.0	0.3
			Note 6	X;X;X	0.6	0.15	1.0	0.3
	- Sleep In Mode	N/A	N/A	X;X;X	0.003	0.010	0.005	0.020
Host interface active	- **Normal** Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	77Hz±10 %	65536 Colors Note 8 CPU Access @ 10fps	0;0;0	1.4	0.6	2.0	1.0
				0;0;1	1.4	0.6	2.0	1.0
				0;1;0	1.4	0.6	2.0	1.0
				0;1;1	1.4	0.6	2.0	1.0
				1;0;0	1.4	0.6	2.0	1.0
				1;0;1	1.4	0.6	2.0	1.0
				1;1;0	1.4	0.6	2.0	1.0
				1;1;1	1.4	0.6	2.0	1.0

NOTE:

X Do not care

1. All pixels black

2. Checker board one by one

3. Checker board 4 by 4

4. Grey-scale from top to bottom

5. 20% Black, 80%White

6. Black & White Checker board 8 by 8.

7. Absolute Worst Case Patterns: Defined by Display Supplier

8. Absolute Worst Case Patterns and Sequences: Defined by Display Supplier

9. Absolute worst case VDDA current is less than 1mA in the case of Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.

10. Absolute worst case VDDI current is less than 0.2mA in the case of Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.

Typical Case:

TA = 25ºC

VDDA = 2.75V

VDD = 1.8V

Worst Case:

TA = 25ºC

VDDA = 2.4V to 3.3V

Includes Process Variance.

11 TIMING CHARACTERISTICS

11.1 Parallel Interface Characteristics bus (8080-series MCU)

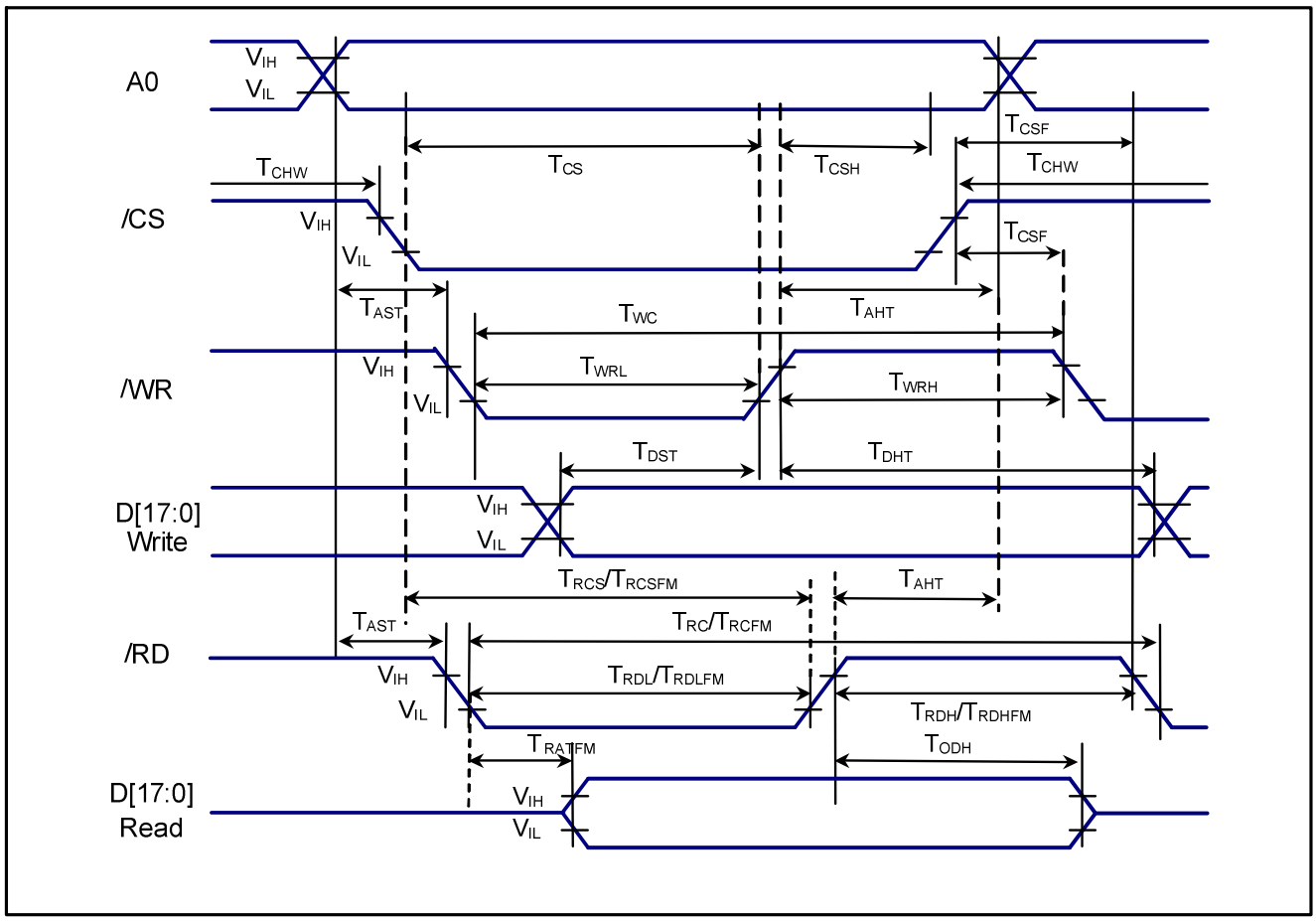


Figure 11.1-1 Parallel Interface Characteristics bus (8080-series MCU)

(V_{SS}=0V, V_{DDI}=1.80V, V_{DDA}=2.4V to 3.3V, Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
A0	T_{AST}	Address setup time	15	-	ns	-
	T_{AHT}	Address hold time (Write/Read)	15	-	ns	
/CS	T_{CHW}	Chip select “H” pulse width	10	-	ns	
	T_{CS}	Chip select setup time (Write)	50	-	ns	
	T_{CSH}	Chip select hold time (Write)	10	-	ns	
	T_{RCS}	Chip select setup time (Read ID)	60	-	ns	
	T_{RCSFM}	Chip select setup time (Read FM)	60	-	ns	
	T_{CSF}	Chip select wait time (Write/Read)	10	-	ns	
/WR	T_{WC}	Write cycle	230	-	ns	
	T_{WRH}	Control pulse “H” duration	130	-	ns	
	T_{WRL}	Control pulse “L” duration	80	-	ns	
/RD (ID)	T_{RC}	Read cycle (ID)	160	-	ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	20	-	ns	
	T_{RDL}	Control pulse “L” duration (ID)	80	-	ns	
/RD (FM)	T_{RCFM}	Read cycle (FM)	250	-	ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	80	-	ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	80	-	ns	
D[17:0]	T_{DST}	Data setup time	50	-	ns	For maximum CL=30pF For minimum CL=8pF
	T_{DHT}	Data hold time	0	-	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	10	80	ns	

(V_{SS}=0V, V_{DDI}= 2.8V, V_{DDA}=2.4V to 3.3V, Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
A0	T_{AST}	Address setup time	15	-	ns	-
	T_{AHT}	Address hold time (Write/Read)	15	-	ns	
/CS	T_{CHW}	Chip select “H” pulse width	0	-	ns	
	T_{CS}	Chip select setup time (Write)	30	-	ns	
	T_{CSH}	Chip select hold time (Write)	10	-	ns	
	T_{RCS}	Chip select setup time (Read ID)	60	-	ns	
	T_{RCSFM}	Chip select setup time (Read FM)	60	-	ns	
	T_{CSF}	Chip select wait time (Write/Read)	10	-	ns	
/WR	T_{WC}	Write cycle	150	-	ns	
	T_{WRH}	Control pulse “H” duration	80	-	ns	
	T_{WRL}	Control pulse “L” duration	50	-	ns	
/RD (ID)	T_{RC}	Read cycle (ID)	140	-	ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	20	-	ns	
	T_{RDL}	Control pulse “L” duration (ID)	60	-	ns	
/RD (FM)	T_{RCFM}	Read cycle (FM)	160	-	ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	50	-	ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	60	-	ns	
D[17:0]	T_{DST}	Data setup time	30	-	ns	For maximum CL=30pF For minimum CL=8pF
	T_{DHT}	Data hold time	10	-	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	10	80	ns	

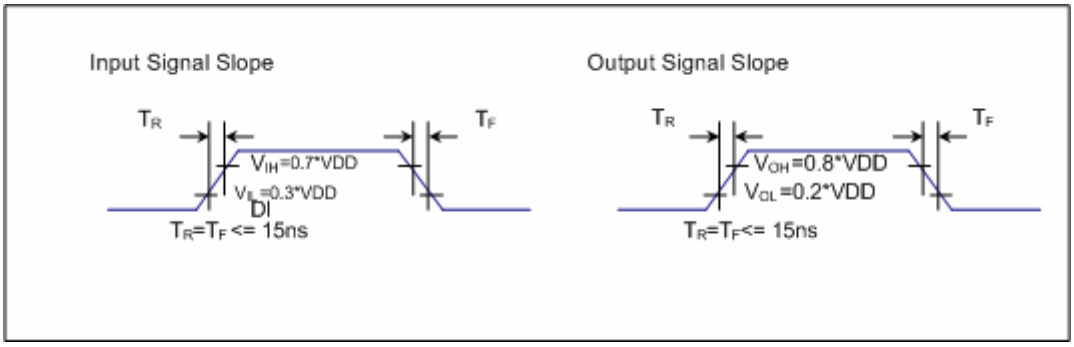


Figure 11.1-2 Rising and Falling timing for Input and Output signal

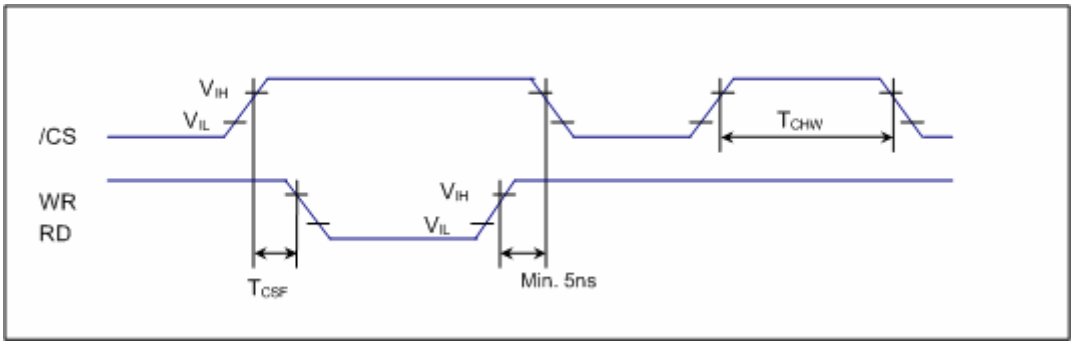


Figure 11.1-3 Chip selection (CSX) timing

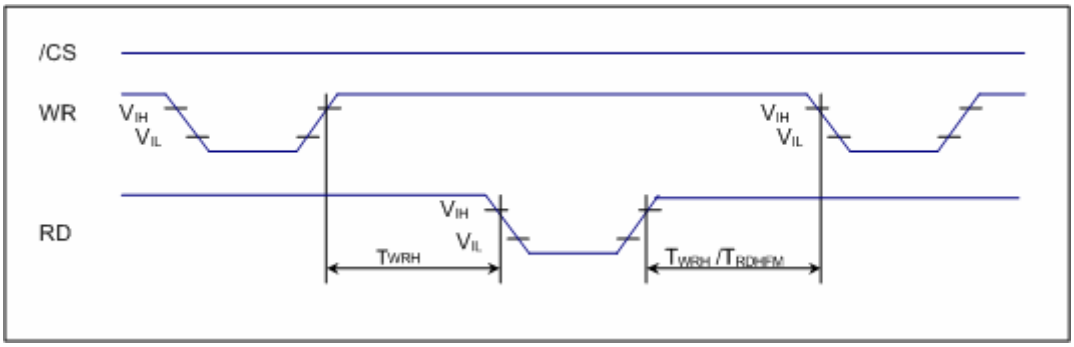


Figure 11.1-4 Write to read and Read to write timing

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDD for Input signals.

11.2 Parallel Interface Characteristics bus (6800-series MCU)

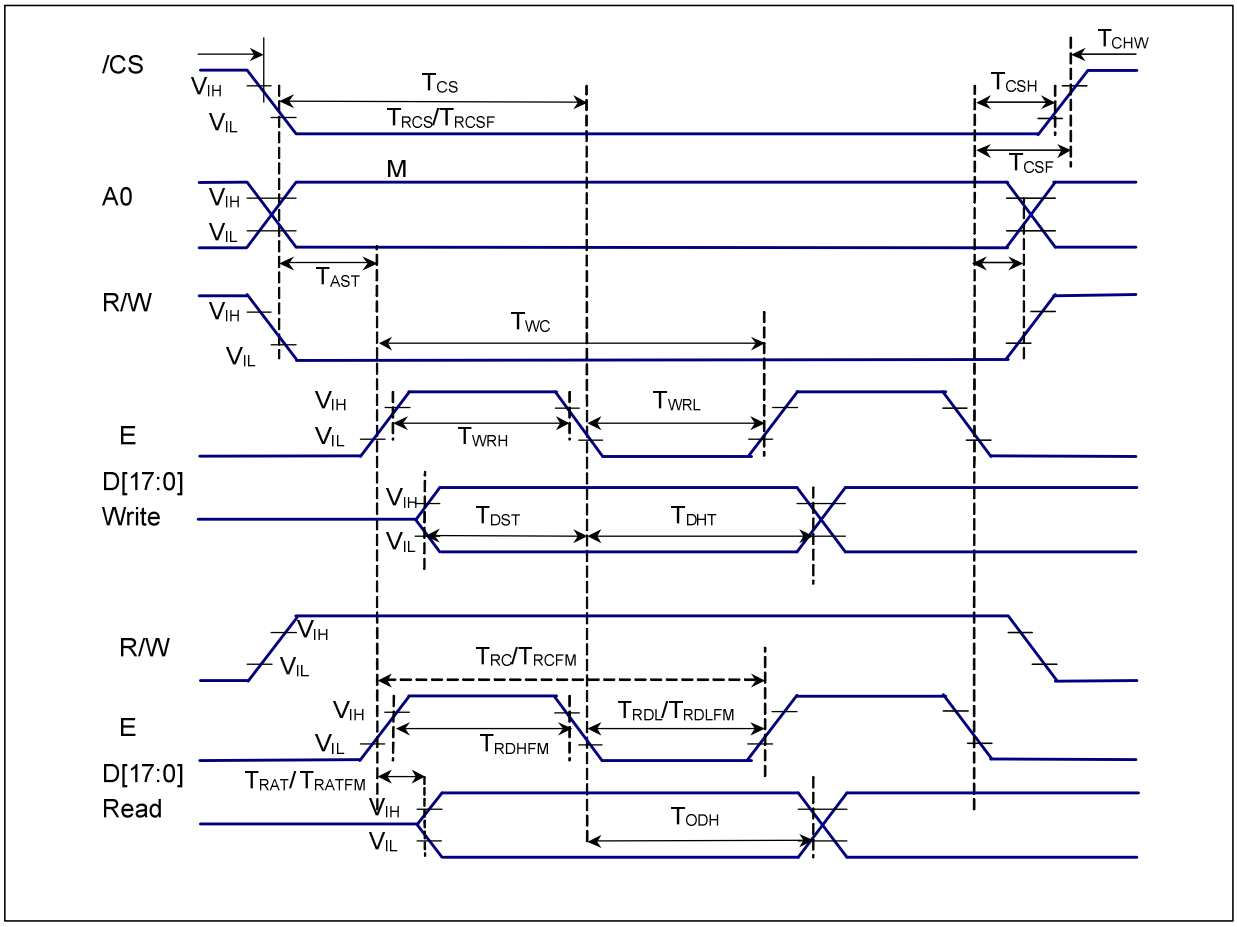


Figure 11.2-1 Parallel Interface characteristics (6800-Series MCU)

(V_{SS}=0V, V_{DDI}=1.80V, V_{DDA}=2.4V to 3.3V, Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
A0	T_{AST}	Address setup time	15	-	ns	-
	T_{AHT}	Address hold time (Write/Read)	15	-	ns	
/CS	T_{CHW}	Chip select "H" pulse width	10	-	ns	
	T_{CS}	Chip select setup time (Write)	50	-	ns	
	T_{RCS}	Chip select setup time (Read ID)	50	-	ns	
	T_{RCSFM}	Chip select setup time (Read FM)	50	-	ns	
	T_{CSF}	Chip select wait time (Write/Read)	10	-	ns	
	T_{CSH}	Chip select hold time	10	-	ns	
/R/W	T_{WC}	Write cycle	200	-	ns	
	T_{WRH}	Control pulse "H" duration	50	-	ns	
	T_{WRL}	Control pulse "L" duration	130	-	ns	
E (ID)	T_{RC}	Read cycle (ID)	130	-	ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	30	-	ns	
	T_{RDL}	Control pulse "L" duration (ID)	20	-	ns	
E (FM)	T_{RCFM}	Read cycle (FM)	300	-	ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	40	-	ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	80	-	ns	
D[17:0]	T_{DST}	Data setup time	50	-	ns	For maximum CL=30pF For minimum CL=8pF
	T_{DHT}	Data hold time	10	-	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	10	80	ns	

(VSS=0V, VDDI=2.8V, VDDA=2.4V to 3.3V,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
A0	T_{AST}	Address setup time	15	-	ns	-
	T_{AHT}	Address hold time (Write/Read)	15	-	ns	
/CS	T_{CHW}	Chip select “H” pulse width	10	-	ns	
	T_{CS}	Chip select setup time (Write)	30	-	ns	
	T_{RCS}	Chip select setup time (Read ID)	30	-	ns	
	T_{RCSFM}	Chip select setup time (Read FM)	50	-	ns	
	T_{CSF}	Chip select wait time (Write/Read)	10	-	ns	
	T_{CSH}	Chip select hold time	10	-	ns	
R/W	T_{WC}	Write cycle	140	-	ns	
	T_{WRH}	Control pulse “H” duration	30	-	ns	
	T_{WRL}	Control pulse “L” duration	100	-	ns	
E (ID)	T_{RC}	Read cycle (ID)	100	-	ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	30	-	ns	
	T_{RDL}	Control pulse “L” duration (ID)	30	-	ns	
E (FM)	T_{RCFM}	Read cycle (FM)	150	-	ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	30	-	ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	80	-	ns	
D[17:0]	T_{DST}	Data setup time	50	-	ns	For maximum CL=30pF For minimum CL=8pF
	T_{DHT}	Data hold time	10	-	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	10	80	ns	

11.3 Serial Interface Characteristics (3-pin Serial)

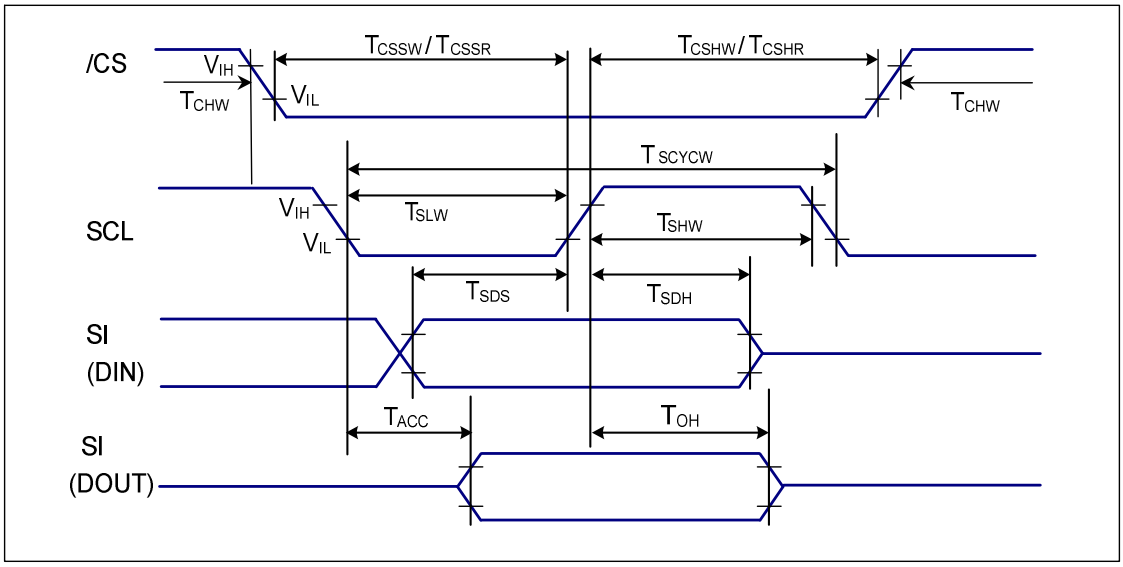


Figure 11.3-1 3-pin Serial Interface Characteristics

(V_{SS}=0V, V_{DDI}=1.80V, V_{DDA}=2.4V to 3.3V,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
/CS	T_{CHW}	/CS “H” pulse width	10	-	ns	
	T_{CSSW}	/CS-SCL setup time(Write)	10	-	ns	
	T_{CSHW}	/CS-SCL hold time(Write)	15	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	130	-	ns	
	T_{SHW}	SCL “H” pulse width (Write)	90	-	ns	
	T_{SLW}	SCL “L” pulse width (Write)	40	-	ns	
SI (DIN) (DOUT)	T_{SDS}	Data setup time	10	-	ns	
	T_{SDH}	Data hold time	15	-	ns	

(V_{SS}=0V, V_{DDI}=2.80V, V_{DDA}=2.4V to 3.3V,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
/CS	T_{CHW}	/CS “H” pulse width	10	-	ns	
	T_{CSSW}	/CS-SCL setup time(Write)	10	-	ns	
	T_{CSHW}	/CS-SCL hold time(Write)	15	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	80	-	ns	
	T_{SHW}	SCL “H” pulse width (Write)	50	-	ns	
	T_{SLW}	SCL “L” pulse width (Write)	30	-	ns	
SI (DIN) (DOUT)	T_{SDS}	Data setup time	10	-	ns	
	T_{SDH}	Data hold time	15	-	ns	

11.4 Serial Interface Characteristics (4-pin Serial)

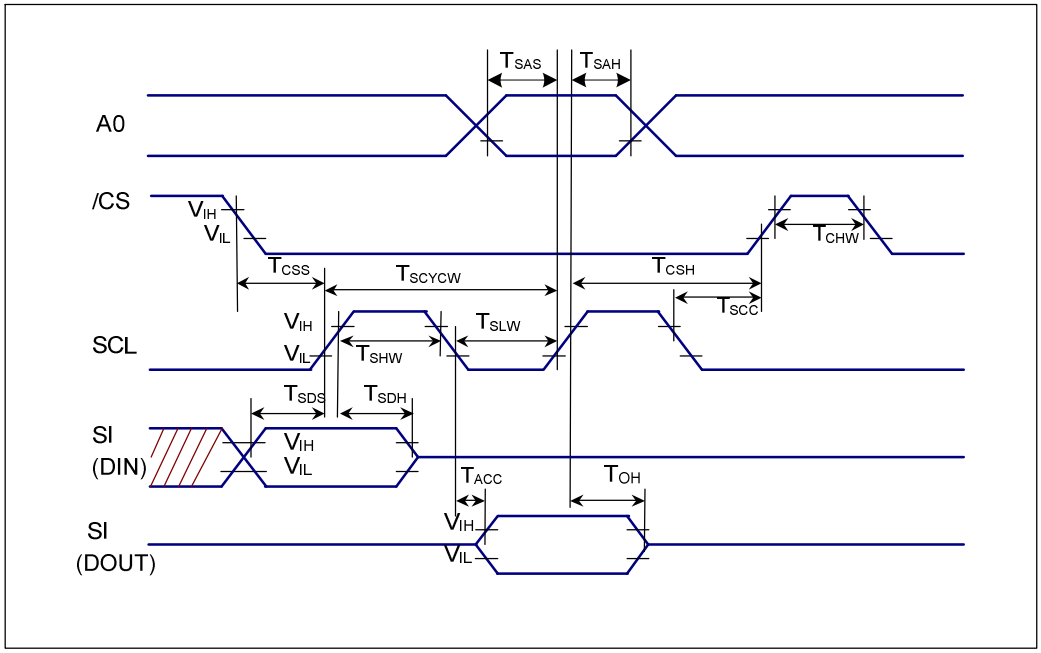


Figure 11.4-1 4-pin Serial Interface Characteristics

(V_{SS}=0V, V_{DDI}=1.80V, V_{DDA}=2.4V to 3.3V, Ta = -30 to 70℃)

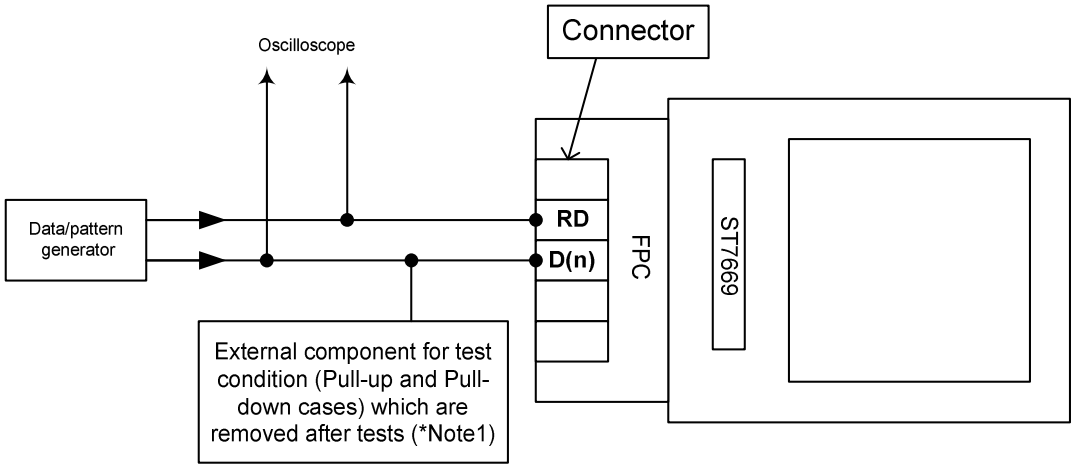
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
/CS	T_{CSS}	Chip select setup time	10	-	ns	
	T_{CSH}	Chip select hold time	15	-	ns	
	T_{SCC}	Chip select setup time	10	-	ns	
	T_{CHW}	Chip select setup time	10	-	ns	
A0	T_{SAS}	Address setup time	15	-	ns	
	T_{SAH}	Address hold time	15	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	130	-	ns	
	T_{SHW}	SCL “H” pulse width (Write)	90	-	ns	
	T_{SLW}	SCL “L” pulse width (Write)	40	-	ns	
SI (DIN) (DOUT)	T_{SDS}	Data setup time	15	-	ns	
	T_{SDH}	Data hold time	15	-	ns	

(V_{SS}=0V, V_{DDI}= 2.80V, V_{DDA}=2.4V to 3.3V, Ta = -30 to 70℃)

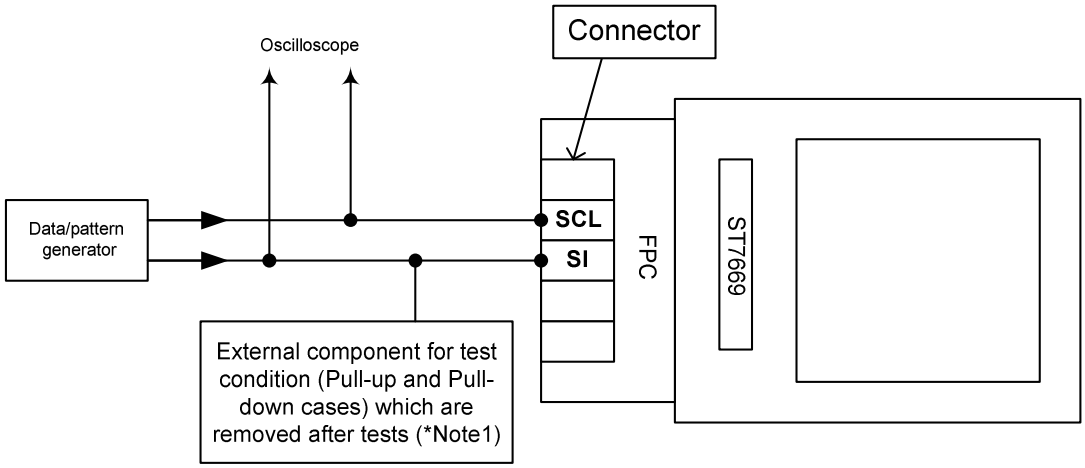
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
/CS	T_{CSS}	Chip select setup time	10	-	ns	
	T_{CSH}	Chip select hold time	15	-	ns	
	T_{SCC}	Chip select setup time	10	-	ns	
	T_{CHW}	Chip select setup time	10	-	ns	
A0	T_{SAS}	Address setup time	15	-	ns	
	T_{SAH}	Address hold time	15	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	80	-	ns	
	T_{SHW}	SCL “H” pulse width (Write)	50	-	ns	
	T_{SLW}	SCL “L” pulse width (Write)	30	-	ns	
SI (DIN) (DOUT)	T_{SDS}	Data setup time	15	-	ns	
	T_{SDH}	Data hold time	15	-	ns	

11.5 Ouput access/disable timing measurement method

◆ Parallel interface (8080-series)



◆ Serial interface (3-line)



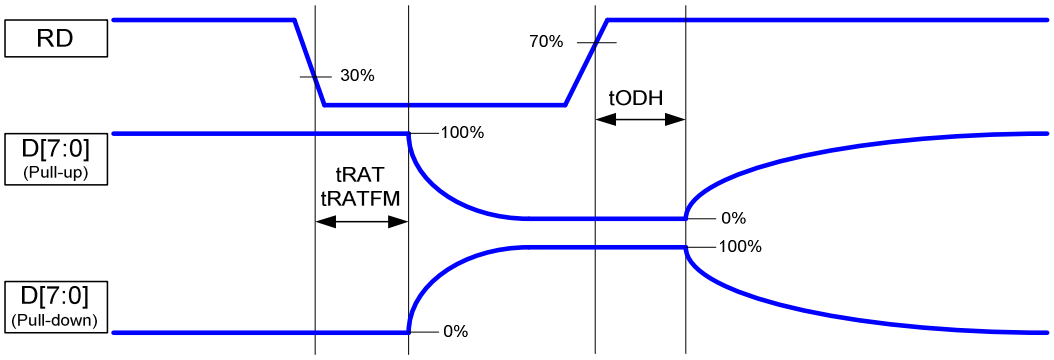
Note:

1. pull-up/pull-down resistor: ***3KΩ ± 5% ;*** *pull-up/pull-down capacitor:* ***8 or 30 pF ± 10%***

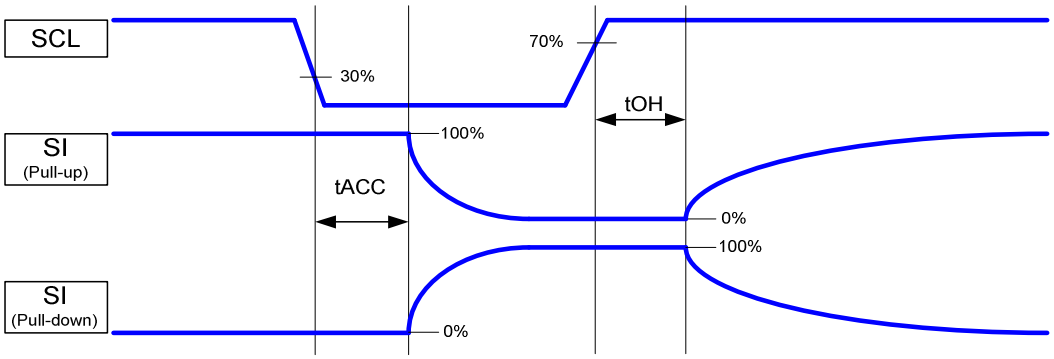
2. Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements.

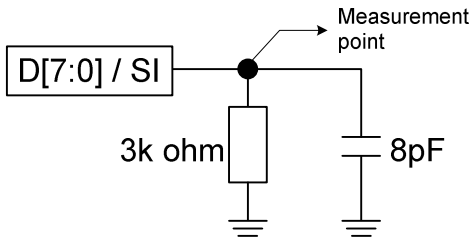
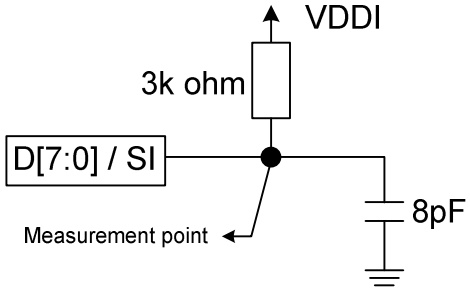
11.6 Minimum value measurement

◆ Parallel interface (8080-series)



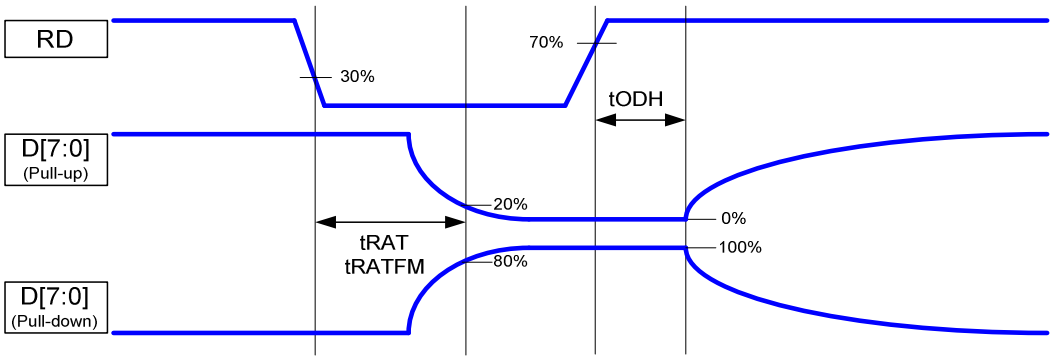
◆ Serial interface (3-line)



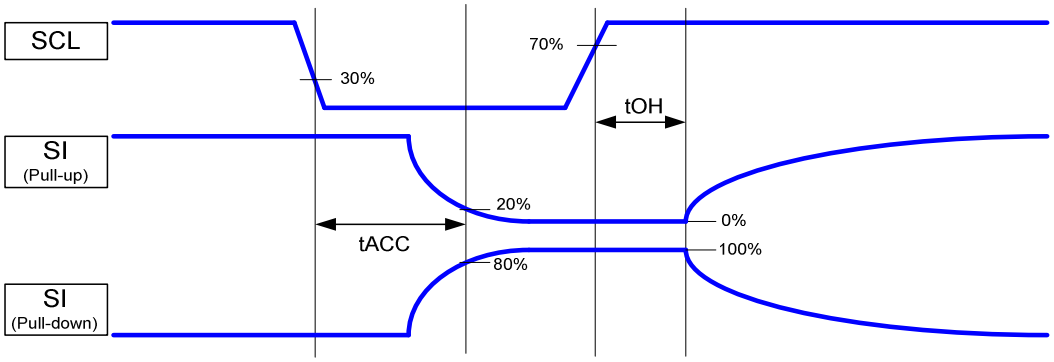
Measurement circuit pull down	Measurement circuit pull up
	

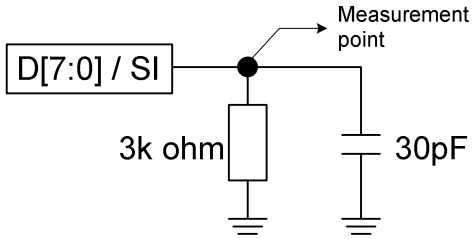
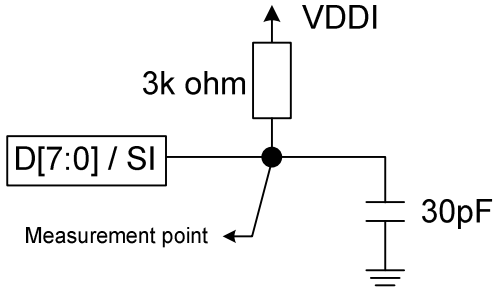
11.7 Maximum value measurement

◆ Parallel interface (8080-series)

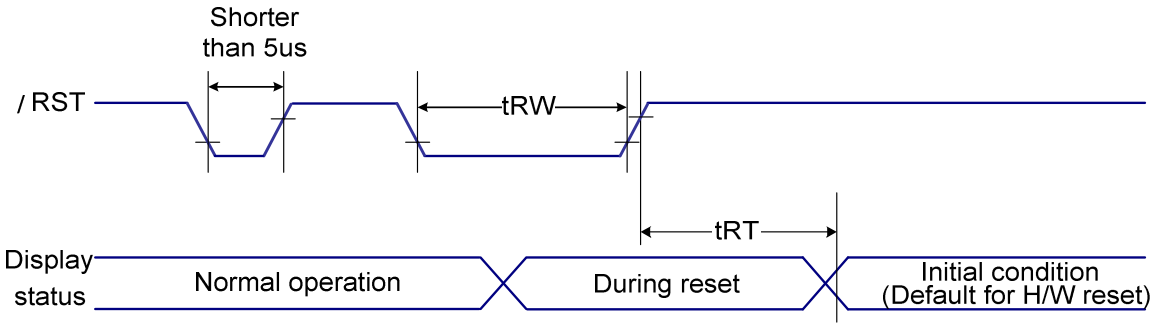


◆ Serial interface (3-line)



Measurement circuit pull down	Measurement circuit pull up
	

12 RESET TIMING



(V_{SS}=0V, V_{DDI}=1.65V to 3.0V, V_{DDA}=2.4V to 3.3V,Ta = -30 to 70℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Reset “L” pulse width	/RST	tRW		10	—	us
Reset time		tRT		—	5 (*note 5)	ms
				—	200 (*note 6,7)	ms

Notes:

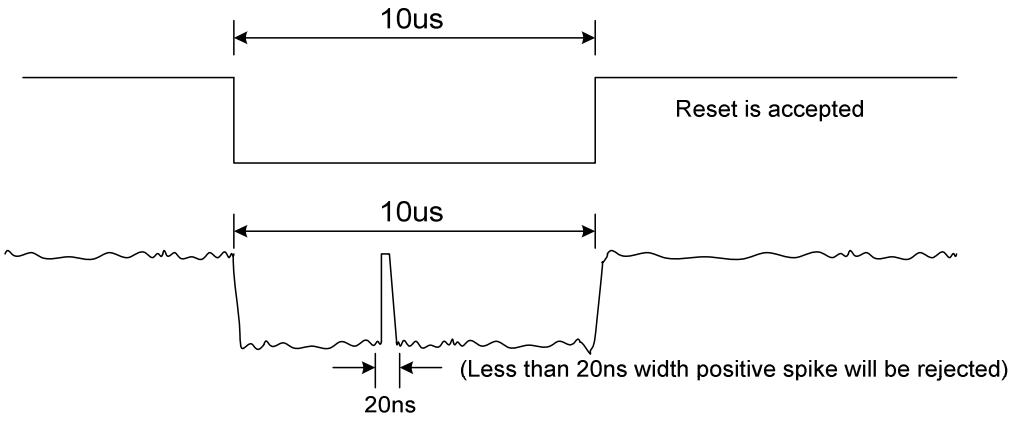
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RST

2. Spike due to an electrostatic discharge on RST line does not cause irregular system reset according to the table below:

RST Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 9μs	Reset
Between 5μs and 9μs	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 200 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

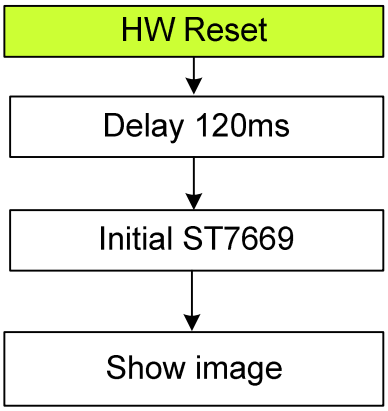
6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RST before sending commands. Also Sleep Out command cannot be sent for 200msec.

13 Instrunction Setup Flow

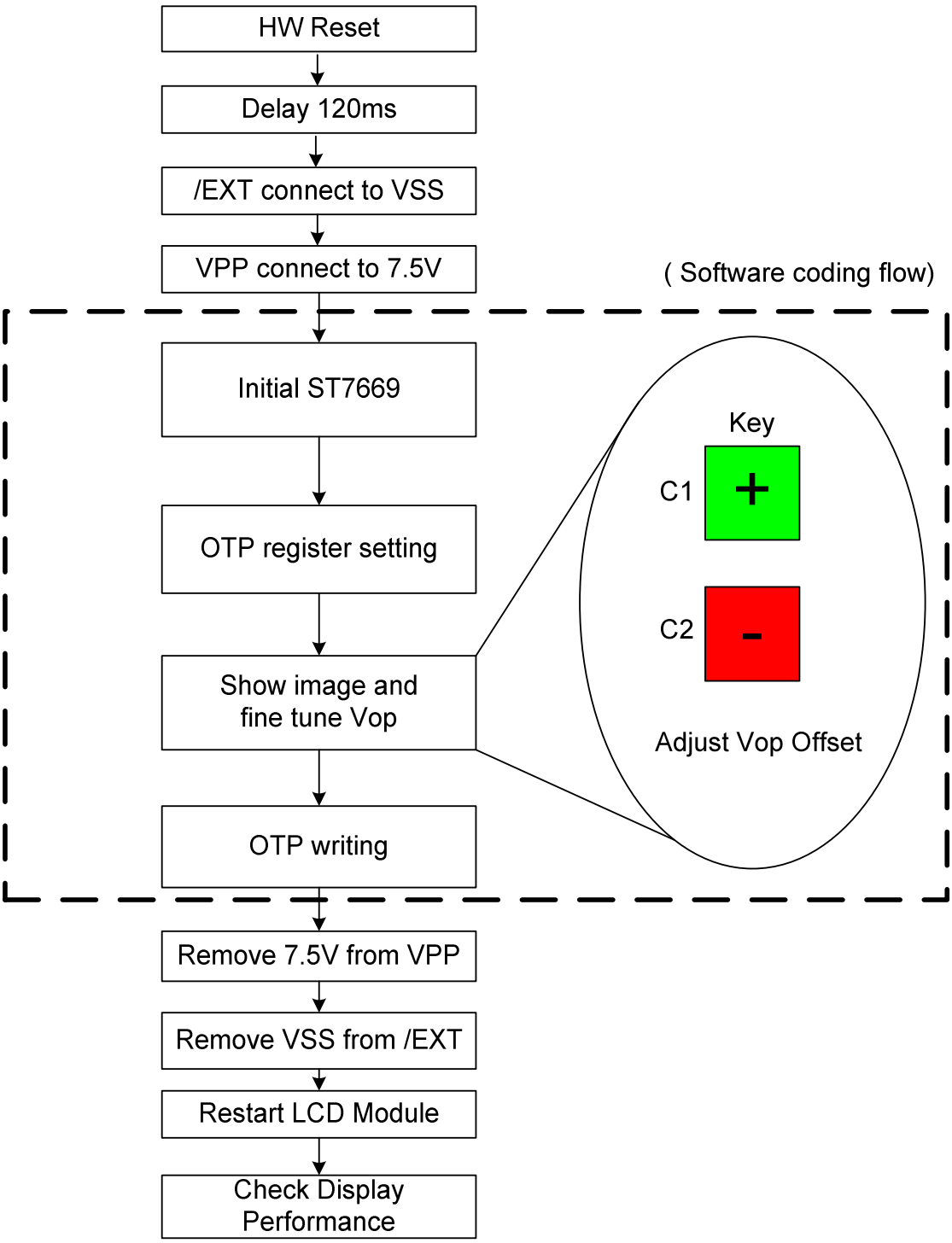
13.1 Command Table -- 2 enable Instruction Flow

13.1.1 Initial Flow (Command Table -- 2 ensable)



Note: About ST7669 Initial Code, please refer to "Initial ST7669" as below.

13.1.2 Burning Flow (Command Table -- 2 ensable)



```
void Initial_ST7669(void)
{
//----------disable autoread + Manual read once ----------------------------
      Write(COMMAND,0xd7);                    // Auto Load Set
      Write(DATA,0xdf);                       // Auto Load Disable
      Write(COMMAND,0xE0);                    // EE Read/write mode
      Write(DATA,0x00);                       // Set read mode
      delayms(10);                            // Delay 10ms
      Write(COMMAND,0xE3);                    // Read active
      delayms(20);                            // Delay 20ms
      Write(COMMAND,0xE1);                    // Cancel control

//---------------------------------- Sleep OUT ----------------------------------------
      Write(COMMAND, 0x11 );                  // Sleep Out
      Write(COMMAND, 0x28 );                  // Display OFF
      delayms(50);                            //Delay 50ms

//-------------------------------Vop setting-----------------------------------------
      Write(COMMAND,0xC0);                    //Set Vop by initial Module
      Write(DATA, 0x04);                      //Vop = 14V
      Write(DATA, 0x01);                      // base on Module

//--------------------------Set  Register--------------------------------------
      Write(COMMAND,0xC3);                    // Bias select
      Write(DATA,0x05);                       // 1/9 Bias, base on Module
      Write(COMMAND,0xC4);                    // Setting Booster times
      Write(DATA,0x07);                       // Booster X 8
      Write(COMMAND,0xC5);                    // Booster eff
      Write(DATA,0x21);                       // BE = 0x01 (Level 2)
      Write(COMMAND,0xCB);                    // Vg with booster x2 control
      Write(DATA,0x01);                       // Vg from Vdd2
      Write(COMMAND,0xCC);                    // ID1 = 00
      Write(DATA,0x00);                       //
      Write(COMMAND,0xCE);                    // ID3 = 00
      Write(DATA,0x00);
      Write(COMMAND,0xB7);                    // COM/SEG Direction for glass //
      Write(DATA,0x48);                       // Setting by LCD module
```

```
Write(COMMAND,0xD0);                    // Analog circuit setting
Write(DATA,0x1D);                       //
Write(COMMAND, 0xB5 );                  // N-Line
Write(DATA, 0x8D);                      // Non-RST, 14-line inversion
Write(COMMAND,0xD7);                    //Auto read Set
Write(DATA,0x9F);                       //OTP Disable

Write(COMMAND,0xB4);                    //PTL Mode Select
Write(DATA,0x18);                       //PTLMOD → Normal Mode
Write(COMMAND,0x3A);                    // Color mode = 65k
Write(DATA,0x05);                       //
Write(COMMAND,0x36);                    // Memory Access Control //
Write(DATA,0xC8);                       // Setting by LCD module

Write(COMMAND,0xB0);                    // Duty = 160 duty
Write(DATA,0x9F);

Write(COMMAND,0x20);                    // Display Inversion OFF

Write(COMMAND,0xF7 );                   // command for temp sensitivity.
Write(COMMAND,0x06);                    //
```

1. Set Gamma table for Module, please refer spec *ch 9.1.73*.

2. Set Temp compensation for Module, please refer spec *ch 9.1.71*.

```
Write(COMMAND,0x2A);                    // COL//
Write(DATA,0x00);                       // 0~127
Write(DATA,0x00);
Write(DATA,0x00);
Write(DATA,0x7F);

Write(COMMAND,0x2B);                    // Page //
Write(DATA,0x00);                       // 0~159
Write(DATA,0x00);
Write(DATA,0x00);
Write(DATA,0x9F);
}
```

```
void Set_OTP_Register(void)
{
//-------------------------------Set OTP register-------------------------------------
        Write(COMMAND, 0xC7 );                  //Vop offset = 0x00
        Write(DATA, 0x00);                      //
        Write(DATA, 0x00 );                     // apply by Module
        Note#1
        Write(COMMAND, 0xCD );                  //ID2
        Write(DATA, 0x80 );
        Write(COMMAND, 0xB5 );                  // N-Line
        Write(DATA, 0x8D);                      // Non-RST, 14-line inversion
        Write(COMMAND,0xD0);                    // Analog circuit setting
        Write(DATA,0x1D);                       //
        Write(COMMAND,0xD7);                    //Auto read Set
        Write(DATA,0x9F);                       //OTPB Disable

        Write(COMMAND,0xB4);                    //PTL Mode Select
        Write(DATA,0x18);                       //PTLMOD → Normal Mode
}

void Fine_Tune_Vop(void)
{
//---------------------------------- Show Map ----------------------------------------
        Show_Image();                           //Display a image
//---------------------------------- Display ON ----------------------------------------
        Write(COMMAND, 0x29 );                  // Display On
//-------------------------------Fine tune Vop offset-----------------------------------
        Write( COMMAND, 0xC1);                  //Fine tuning Vop here by command
        or                                      0xc1(VopOffsetInc),0xc2(VopOffsetDec).
        Write( COMMAND, 0xC2);
        Note#2
}
```

```
void OTP_Writing(void)
{
//--------------------------------Display OFF-------------------------------------
      Write(COMMAND, 0x28 );                    // Display Off
      Delayms(50);                              // delay 50ms
//---------------------------------OTP writing-------------------------------------
      Write( COMMAND, 0x00F0 );                 // Keep Frame Rate at 77Hz
      Write( DATA, 0x0012 );
      Write( DATA, 0x0012 );
      Write( DATA, 0x0012 );
      Write( DATA, 0x0012 );
      Write( COMMAND, 0x00E4 );                 //OTP selection
      Write( DATA, 0x0058 );                    // Select OTP
      Write( COMMAND, 0x00E5 );                 // Set OTP writing setup
      Write( DATA, 0x000E );
      Write( COMMAND, 0x00E0 );                 // Read/write mode setting
      Write( DATA, 0x0020 );                    // Set Write mode
      Delayms(100);                             // Delay 100ms
      Write( COMMAND, 0x00E2 );                 // Write active
      Delayms(100);                             // Delay 100ms
      Write( COMMAND, 0x00E1 );                 // Cancel control
}
```

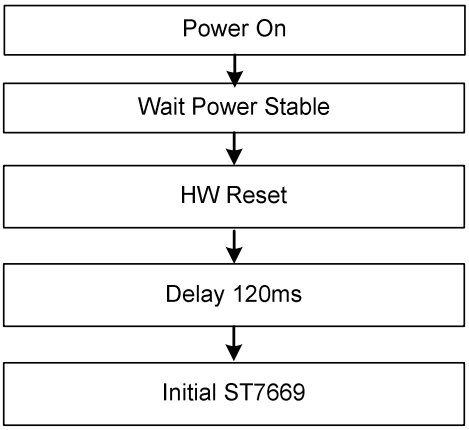
Note:

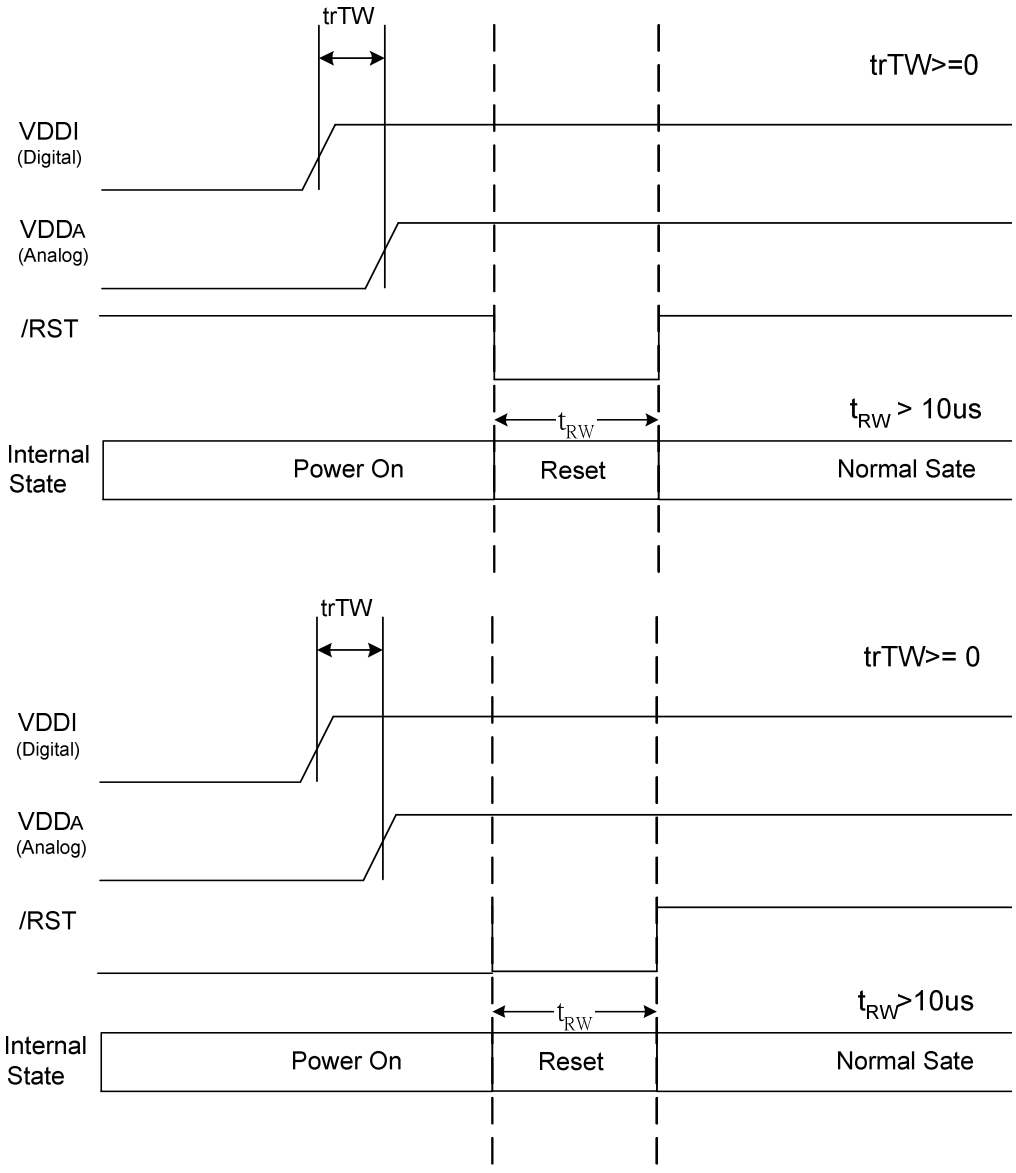
#1 If the Vop and display performace is not suitable after burning OTP，the Vop has to refine tune.

#2 In this section"+" & "-" key button, please execute Write(COMMAND,0xC1) to increase one step at Vop and execute Write(COMMAND,0xC2) to decrease one step at Vop, if necessary.

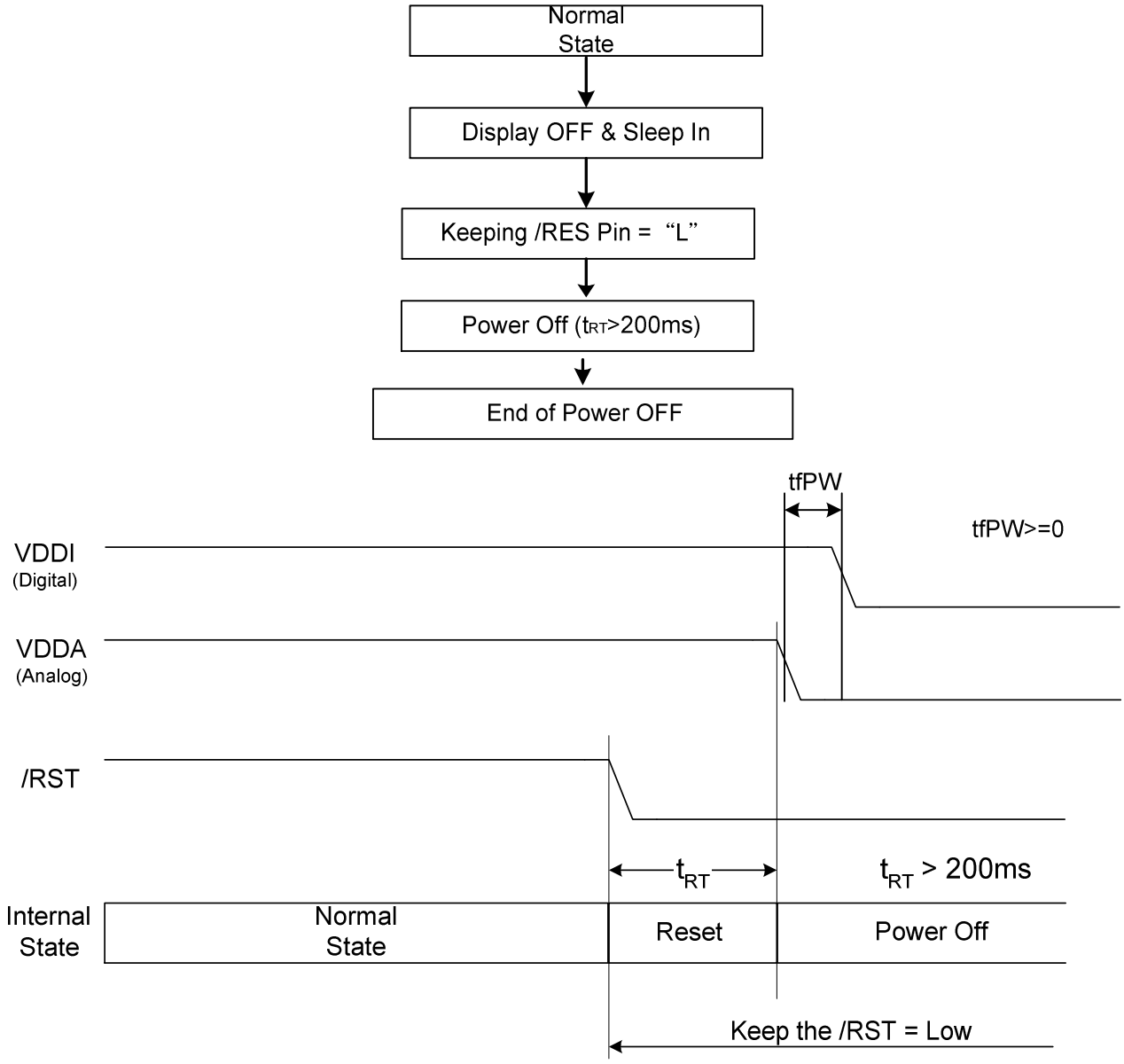
#3 The TC is turn on in burning flow. If LCD module is too dark or bright, it's an effect of backlight.

13.2 Power ON Flow





13.3 Power OFF Flow



14 ITO /FPC Layout Guide

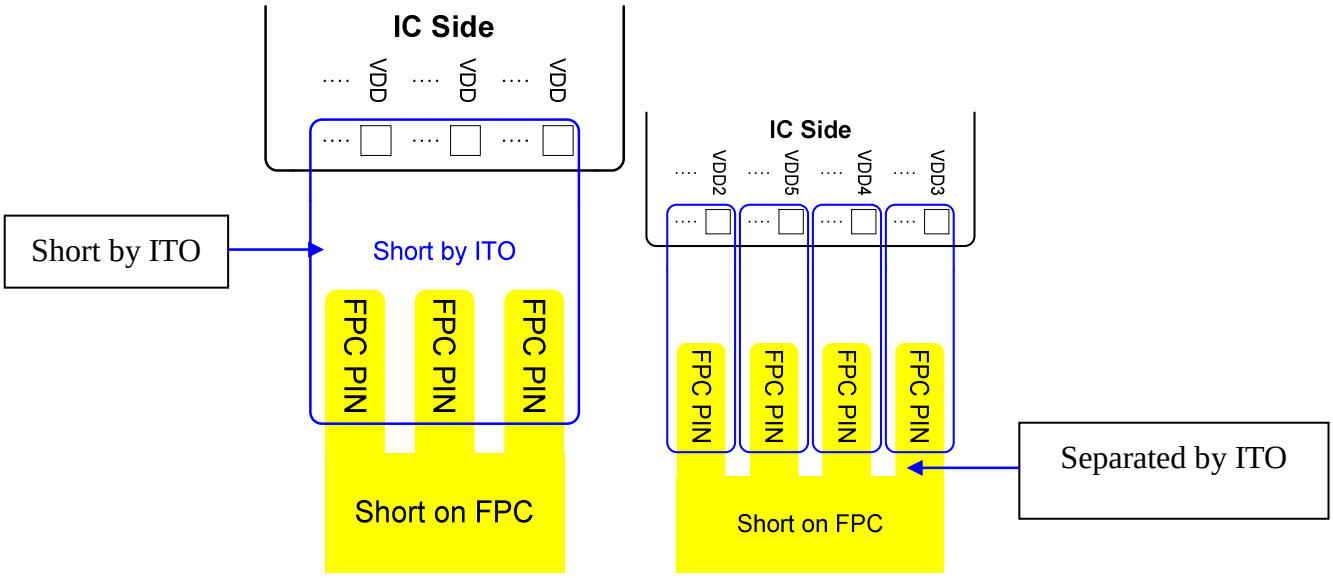
14.1 ITO Layout of Power

◆ **VDD, VDD2~VDD5, VSS, VSS1, VSS2 & VSS4:**

To avoid the noise in different power system affect other power system, please separate different power source on ITO layout (VDD can be short together to get better performance).

To reduce the ITO resistance, the power source should have enough trace width (includes ITO width and FPC trace width). So the separated ITO traces should be connected together by FPC.

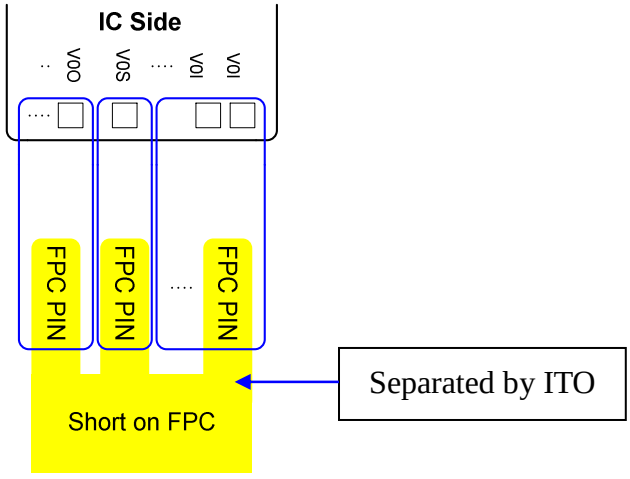
=> The recommended solution is shown below.



◆ **"Output", "Input" and "Sensor" of built-in power circuits:**

The V0, XV0 and Vg power circuits have output pins, input pins and a sensor input. To avoid the power noise affects the sensor input of internal power circuits. The trace should be separated by ITO and should be connected together by FPC. So that the "Sensor" pin has larger ITO resistance (for noise immunity).

The recommended layout topology is shown below: (XV0/Vg should use the same topology as V0)



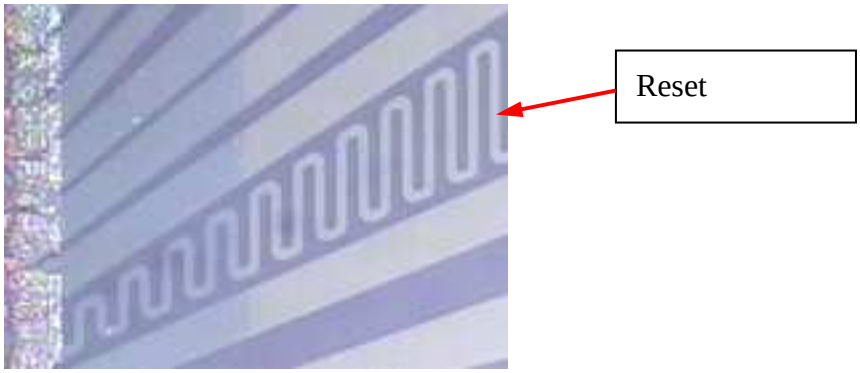
◆ **VPP:**

This is the power source for programming the internal OTP. If the ITO resistance is too high, the operation current will cause the voltage drop while programming OTP. Please try to keep the ITO resistance as low as possible.

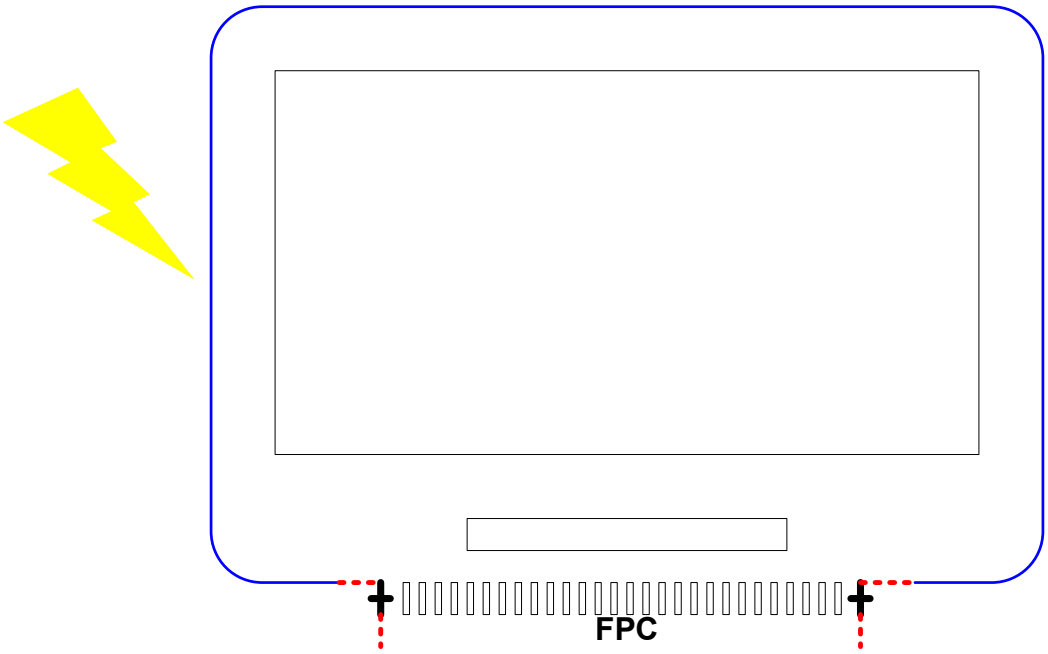
14.2 ESD Protection

◆ **For ESD protection of the LCM, here are some recommendations:**

1. RST (Reset pin): Please increase the resistance of this pin. Here is an example:

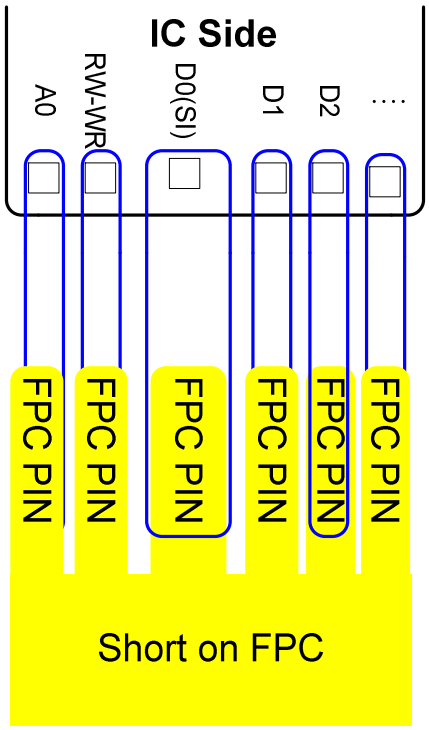


2. ESD Protection Ring: “Shielding Ground” is the first protection of ESD. By connecting the “Blue” (ITO) ring to the FPC, the protection ring is finished.



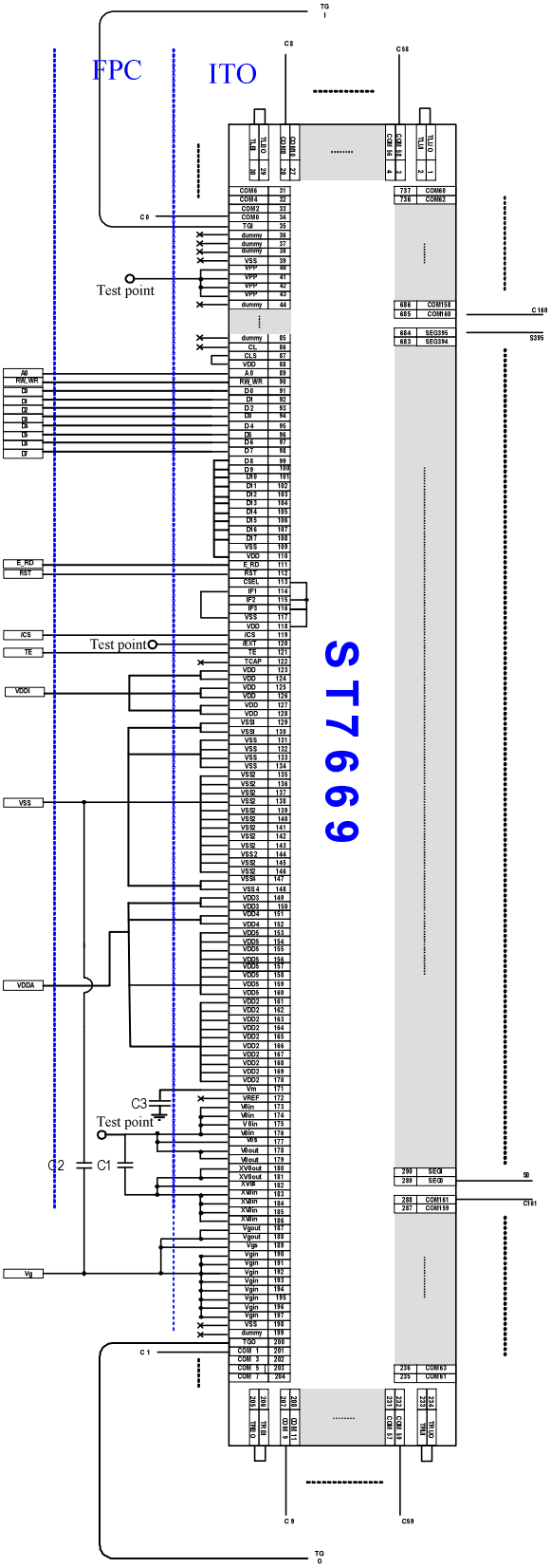
14.3 SPI ITO Suggestion

In order to get good transfer quality, the SI should have enough ITO width to reduce the ITO resistance (Interface → SPI 3/4 Line). The recommended layout topology is shown below:



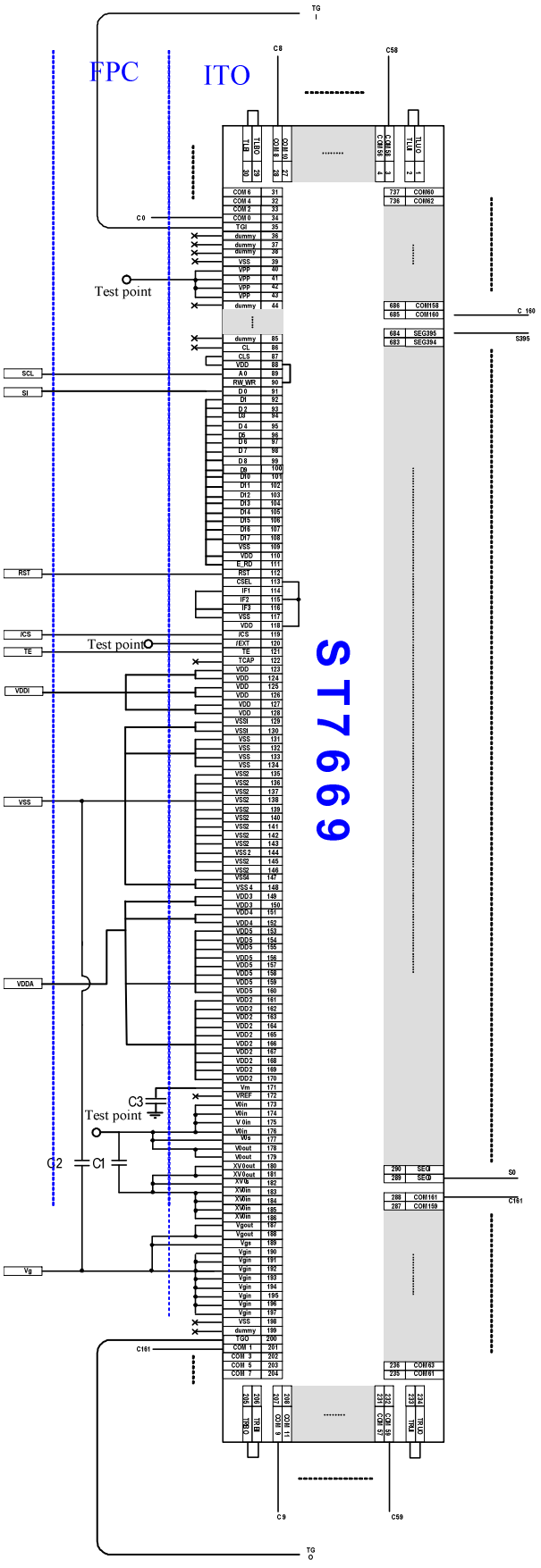
15 Application Note

15.1 8080 series 8-bit parallel



IF[3:1]	H H L
CLS	H (Internal OSC)
CSEL	H
C1	1uF/25V
C2	1uF/16V
C3	1uF/16V

15.2 9-bit SPI mode (3 line)



IF[3:1]	L H L
CLS	H (Internal OSC)
CSEL	H
C1	1uF/25V
C2	1uF/16V
C3	1uF/16V

ST7669 Serial Specification Revision History			
Version	**Date**	**Description**	**Author**
0.0	2005/12/22	-----	
1.0a	2007/01/31	Spec First Issue	
1.1a	2007/6/22	● Redefine the programming mechanism of non-volatility memory. ● Modify 3/4 -SPI timing chart.	
1.2a	2007/9/26	● Modify Power OFF Delay time = 200ms	
1.3a	2009/01	● Modify timing table	