THE EUROPEAN REFERENCE FAB

Blueprint For A Trustworthy And Transparent Manufacturing Network

Exposé:

The Transparent Reference Fab (TRF) is a modular 300-mm semiconductor reference-fab blueprint conceived as public-interest manufacturing infrastructure to strengthen Europe's security, resilience and technological sovereignty. It combines a 130-nm industrial baseline with an optional evolution path to 65 nm and a fully integrated assembly, packaging and chiplet integration flow, based on open PDKs/ADKs and auditable processes from design through manufacturing and test. This enables systematically auditable production of highly security-critical dies and systems in Europe, including co-integration of external leading-edge compute dies while keeping the final system-level trust anchor in a European TRF environment.

The model scales as a network of cloneable sites: front-end lines and/or assembly/test modules can be replicated, specialised and sized to national and sectoral needs. The TRF monetises via trust-premium manufacturing and integration services, with all cooperation remaining voluntary and fully compliant with EU law. Tranche-based financing links disbursements to milestones (construction and tool qualification, 130-nm PDK/MPW and audit go-live and – where pursued – 65-nm release); governance options (e.g. PPP, SPV, foundation or private with a public-service mandate) remain open. A planned Phase 0 validates site options, CAPEX/OPEX corridors and a realistic capacity range, demand anchors (e.g. long-term agreements with public and industrial users), and the RefFab Academy.

Recommendation: set up an EU-level task force to steer Phase 0 and, in parallel, negotiate concrete agreements with industry for MPWs and a packaging pilot.

From design via manufacturing to test.
Trustworthy by Design..

Norbert Herfurth; Arnd Weber; Steffen Reith; Anna Herfurth; Rene Scholz;
Torsten Grawunder
ref-fab@hep-alliance.org

Content

Transparent Reference Fab for Europe: Open, scalable semiconductor manufacturing as a strategic concept

Executive Summary

Europe faces, in 2025, the existential task of strengthening its technological sovereignty in semiconductor manufacturing. The European Chips Act of 2022 set the goal of increasing Europe's share of global chip fabrication by 2030 from under 10% to 20%—an ambitious undertaking intended to mobilise a total of around 43 bn € in investment[1]. Meanwhile, all 27 EU Member States, under a Semicon Coalition, are calling for an evolution towards a "Chips Act 2.0". Rather than focusing on market share alone, this aims to close critical gaps: availability of key technologies is to be secured, permitting procedures are to be accelerated, and competencies along the entire microelectronics value chain are to be deepened[2]. In parallel, the EU Agency for Cybersecurity (ENISA) warns of increasing cyberattacks on critical infrastructures—a wake-up call that trustworthy, auditable hardware has become a security imperative. Worldwide, other industrial nations are pushing ahead with semiconductor expansion: Japan is investing billions in the Rapidus initiative (target: 2-nm mass production by 2027)[3], and the United States launched the CHIPS and Science Act (52 bn $), followed by major investments such as Texas Instruments' plan exceeding 60 bn $ for new fabs in Texas and Utah[4,5]. China, too, has been flooding the sector with subsidies for years to build domestic fabs. Within Europe, there are isolated initiatives—e.g., Ireland's "Silicon Island" strategy (national semiconductor offensive since 2025)[6], the Swiss "Chip FabLab" project co-led by ETH Zurich[7], or plans around CSIC/CNM in Spain. These individual efforts matter but, lacking critical mass, cannot solve the root problem. Europe must consolidate its strategy and act as one to be

[1] https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/europe-fit-digital-age/european-chips-act_en

[2] https://digital-strategy.ec.europa.eu/en/news/semicon-coalition-calls-reinforced-chips-act

[3] https://www.rapidus.inc/en/tech/te0006

[4] https://bidenwhitehouse.archives.gov/briefing-room/statements-releases/2022/08/09/fact-sheet-chips-and-science-act-will-lower-costs-create-jobs-strengthen-supply-chains-and-counter-china

[5] https://www.ti.com/about-ti/newsroom/news-releases/2025/texas-instruments-plans-to-invest-more-than--60-billion-to-manufacture-billions-of-foundational-semiconductors-in-the-us.html

[6] https://enterprise.gov.ie/en/publications/silicon-island-a-national-semiconductor-strategy.html

[7] https://ee.ethz.ch/news-and-events/d-itet-news-channel/2025/08/boosting-swiss-semiconductors-plans-for-chip-factory-gain-media-attention.html

prepared against geopolitical risks, supply bottlenecks, and technological lag. Against this background, this paper presents the concept of a Transparent Reference Fab (TRF) as a proactive response and as a **piece of public-interest manufacturing infrastructure**.

The Transparent Reference Fab for Europe is a proposed reference semiconductor plant designed to be open, scalable, and production-ready. It serves as an open-source blueprint for the rapid build-out of additional fabs in Europe. Core principles of this approach are:

• **Series-capable manufacturing model instead of a pilot line:** Unlike typical pilot lines (which often have a demonstration character and, at best, capacities for small-series production), the Reference Fab is designed from the outset for industrial volumes and 24/7 operation. It is intended to shoulder real production loads and operate economically, so that any plant copied from this model is production-ready from day one and does not require a costly transition from pilot to series production. The dimensioning is expressed not as a single figure but as a capacity corridor on the order of a few thousand 300-mm wafer starts per month; the exact operating point will be refined and validated in Phase 0 together with anchor customers and partners.

• **Transparent open-source blueprint:** All key processes, equipment parameters, and fab operations are, in principle, openly documented and made accessible for re-use. This transparency allows European industrial actors and states to use the fab as a blueprint to build new plants autonomously with lower development risk. It also creates trust in the chips produced: security-relevant semiconductors can be examined down to the process level, ensuring **trustworthy electronics "Made in Europe"**. Any backdoors or manipulations are significantly harder to conceal in a transparent manufacturing process. Based on open design kits and reproducible, auditable toolflows (CI/CD) and reference IPs are provided openly; this measurably lowers entry barriers and audit times. The project thus aims for the **"Trustworthy EU Fab Network"** label—independent bodies should **certify the trustworthiness** of production on the basis of the open documentation and inspections – from the manufacturing process up to the manufactured Chip.

• **Integrated chiplet, packaging and test flow:** Performance, energy, reliability, and security targets are now decided in the back end/SiP/SoP. Therefore, advanced packaging is a core component from day 1: **Co-packaging of leading-edge compute dies** with 65-nm periphery (PMIC, mixed-signal, sensor IF or trust anchors), puts the last stage of **trustworthy manufacturing back to Europe**. We anchor chiplet standards (e.g., UCIe/BoW/OpenHBI), design-for-packaging, and qualified test flows. In this way, we do not widen the gap to the leading edge but **bridge the gap systemically**. Close exchange with EU-funded pilot lines (e.g., APECS) is required here. The Reference Fab is thus conceived as an **integrated front-end + packaging + test environment**, not as a packaging-only project.

• **Focus on 65-nm CMOS as a strategic technology node:** The Reference Fab targets the established 65-nm node, as it will be in demand for a long time and as it is sufficiently performant for many critical applications. Sectors such as automotive, industrial, med-

tech and aerospace can manufacture their microcontrollers, ASICs and mixed-signal components at 65 nm—robustly, cost-effectively, and in high volumes. Forecasts indicate that even after 2030, a significant share of global chip demand will fall to technologies ≥65 nm (especially analogue/power electronic chips), while <10 nm will account for only ~12%. As a bridging technology, operations will initially start on the proven 130-nm node, for which equipment and open process data and PDKs are immediately available in Europe. This bridging approach enables a rapid start of production with high yield, while the 65-nm line is ramped in parallel to maturity. The fab infrastructure is designed modularly so that a later upgrade to 65 nm (or smaller) is possible without fundamental replanning. The focus initially remains on 65 nm as the "sweet spot" between maturity, availability, and sovereignty gains. Importantly, selected platforms will be assured long-term availability (target corridor ≥ 15 years) with obsolescence pathways; certification and qualification pathways (e.g., AEC-Q100/IEC 61508/DO-254) are part of the offering. This **explicitly avoids** a **commodity-volume** model and instead pursues a trusted-premium approach with service and quality premiums. A key value add comes from advanced system integration – see the previous point on integrated chiplet, packaging and test flows.

• **Data-driven manufacturing, audit trails & automation:** Dense inline metrology, SPC/ML-assisted control, and end-to-end feedback from front-/back-end data shorten ramp-ups and create verifiable quality and trust metrics; this also includes robotics-based automation processes. Where sensible, selective single-wafer steps are used; furnace/batch processes remain economical.

• **Use of existing resources and expertise:** The Reference Fab should be located in close physical proximity to existing research and pilot lines such as IHP, CEA-Leti, or imec in order to translate existing process know-how directly into industrial implementation. This proximity enables a significantly accelerated ramp-up, as established teams, qualified equipment, and proven process modules can be used directly. At the same time, the Reference Fab remains institutionally independent—it is not an extension of a research institution but an industrial Reference Fab with its own mandate. RTOs and pilot lines remain the place where new materials, device concepts and process bricks are developed; the TRF industrialises mature bricks and turns them into standardised, auditable modules within a trusted manufacturing environment. By **purposefully integrating research know-how into an open production model**, Europe can become operational more quickly without starting from zero.

• **Governance & public-trust mandate:** There are several options, e.g. public ownership, PPP or a public-trust mandate—institutionally independent of R&D institutions, with physical proximity/co-location; non-discrimination, open audit interfaces (traceability down to lot/wafer level), clear access rules; industry co-investments in equipment/packaging. This ensures replicability, planability, and verifiable trust mechanisms. **The Fab is conceived as public-interest infrastructure.**

• **Talent, training & trusted personnel (RefFab Academy):** The TRF embeds qualification as a core task through a RefFab Academy that provides core curricula, micro-credentials aligned with the European Qualifications Framework (EQF) and a digital Skills-Passport linked to role-based access control and "comply-to-connect" mechanisms in the MES. Training follows the TRF's workflow – manufacturing, chiplet integration, advanced packaging and test – and is delivered via standardised Learning Cells and a "learning-workshop-in-a-box" for on- and off-the-job formats. Dual vocational and higher-education pathways are connected through memoranda of understanding, and rotations between the TRF network, OSAT & RTO partners, shorten time-to-competence. Active recruiting in Europe and beyond, reskilling and international hiring are combined with family-ready conditions such as shift-compatible childcare, language tracks, mentoring and a Just-Culture approach. Proportionate, risk-based background checks under the EU General Data Protection Regulation and a compliance gate for competition, foreign investment, dual-use, intellectual property and privacy safeguard publications and technical artefacts. Open design kits and EDA tools, together with freely available reference designs, documented manufacturing flows and toolchains, remain the instructional foundation. Talent dimensioning is likewise expressed not as a single figure but as a training corridor on the order of several dozen engineers and around one hundred technicians and operators to be trained per site and year in the build-up phase; the exact intake, skill mix and steady-state levels will be refined and validated in Phase 0 with regional education partners and anchor employers.

• **Scalable reference solution & network concept:** The overarching goal is a multiplicative effect: the Reference Fab serves as a blueprint that can be copied one-to-one and rolled out across several European regions. Each new fab built to this model immediately increases regional manufacturing capacity and supply-chain resilience. By standardising the architecture, even production lots and personnel can be exchanged between sites. If a fab fails in a crisis situation, others with identical equipment can temporarily step in—improving supply security. Such a network of identical, trustworthy fabs would reduce Europe's dependence on non-European suppliers while also serving as a platform for innovation (e.g., joint further development of new process modules, open IP libraries). The decision where and when to build additional sites remains policy- and demand-driven; the Reference Fab primarily validates the blueprint, governance and workforce model. Potential Fab clones can be driven by private companies and operated at higher volumes making use of the blueprint.

• **Specialisation for niche products:** Multiple fabs with an identical CMOS base can purposefully differentiate themselves through process-modular add-ons (e.g., RF, power, sensor modules, photonics)—without changing the base technology. In this way, we combine economies of scale with technological differentiation in higher-margin niches. The result is a flexible manufacturing ecosystem that promotes both innovation and specialisation in niche markets.

• **Demand anchors:** Public procurement (critical infrastructure, public administration, security, defence and space) secures a strategic base load in terms of guaranteed use cases, while trusted standard building blocks (e.g. secure controllers, gateways, mixed-signal hubs) and a dense SME-driven system-in-package (SiP) ecosystem are expected to generate most of the volume within the TRF capacity corridor on the order of a few thousand 300-mm wafer starts per month. Industry co-investments expand packaging and test capacities. Delineation: no EUV or leading-edge foundry, no commodity volume model — focus on trusted-premium manufacturing, SiP/chiplets and long product life cycles.

• **Financing & economic viability (brief overview):** The business model is built around a public-mission infrastructure operator with mixed public and private funding. Options include public–private partnership structures or publicly owned entities with long-term industrial co-investments and base-load contracts, combined with a subsidised share of CAPEX from site-level and EU programmes and staged funding tied to milestones (MPW start, 65-nm ramp-up, packaging pilot). The revenue mix would combine foundry, packaging and test, and value-added services (MPW, certification, obsolescence management). The TRF is framed as critical infrastructure with a clear public mission, not as a purely speculative stand-alone foundry project.

• **Guardrails (without hard promises):** MPW offers ≥ 4/year (130 nm) & ≥ 2/year (65 nm), SiP-MPW from Year 2; packaging targets: RDL pitch 10 → ≤ 5 µm, microbump ≤ 55 µm; long-term supply ≥ 15 years; trust KPIs: published yield/DPPM & traceability metrics.

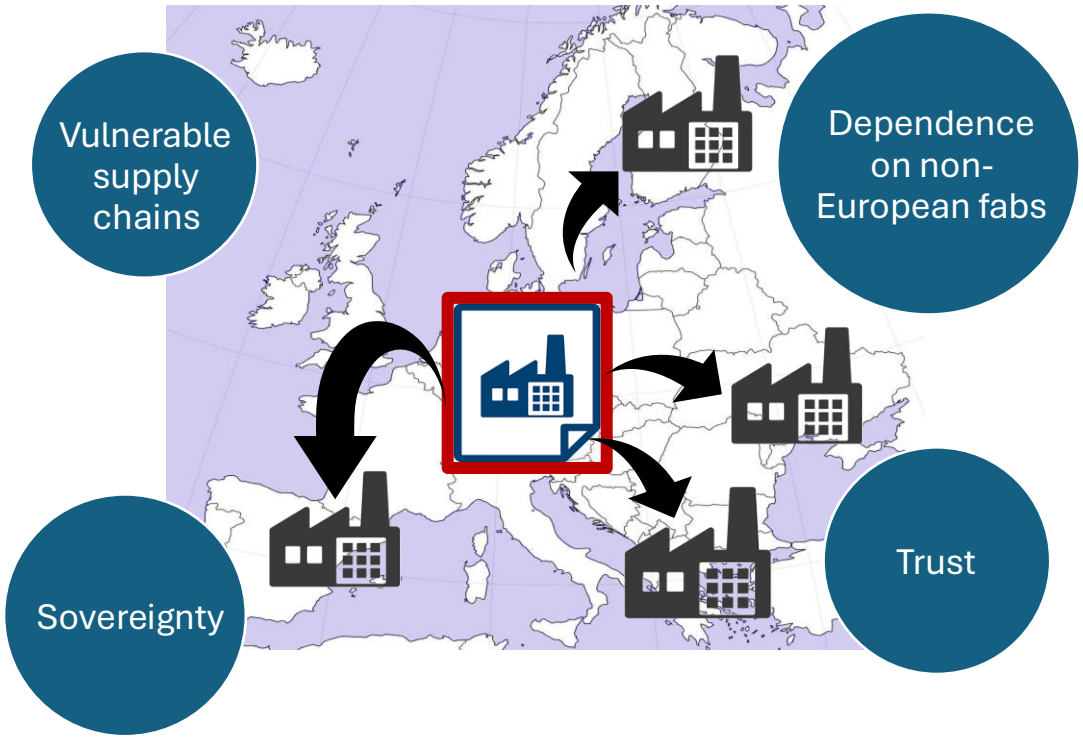
Perspective 2040+: The relevance of ≥ 65-nm classes will persist well beyond the 2030s due to analogue/mixed-signal content, power electronics, eNVM MCUs, RF front-ends, rad-hard/space electronics, and security requirements. Long-lifecycle industries (automotive/automation/med-tech/aerospace) and chiplet architectures further stabilise demand: 65 nm takes on peripheral functions, sensing, PMIC, safety MCU, while leading-edge compute is integrated via co-packaging. The network can—where sensible—shrink modularly or expand its SiP/OSAT footprint without changing the business model.

This Executive Summary addresses policymakers at EU and national level as well as potential funders in public administration and industry. It outlines, in compact form, the vision of a Transparent Reference Fab and its benefits. The recommendation is to advance this strategic concept swiftly with political backing and initial funding. In view of the ongoing reform efforts around the Chips Act, the heightened threat environment, and global investment dynamics, now is the right moment to lay the foundations for open and sovereign semiconductor manufacturing in Europe.

Note (disclaimer): This paper presents a concept and sketches initial proposals for implementation and financing. Delivering a robust realisation will require deeper analysis and a detailed execution plan. Developing these is an integral part of the concept and the subject of Phase 0.

Assumptions, Scope & Non-Goals

- This paper proposes a replicable TRF blueprint (scope, capabilities, governance, training) — not a site decision or an investment commitment.
- Core focus: packaging-first manufacturing (system-in-package, redistribution layers and fan-out) with co-integration to leading-edge nodes, test (ATE/SLT), open design-kit/EDA integration, auditability and workforce pipelines.
- Technology path: 130 nm and 65 nm as evergreen nodes for analogue/mixed-signal, microcontrollers, power-management ICs, RF and IoT; concrete volumes and product mixes are partner- and site-specific.
- Complementary to leading-edge fabs; targets resilience, qualification and SME access, not commodity volume competition.
- Implementation is phase-gated (Phase 0 → Go/No-Go) with measurable milestones, including validation of capacity and talent corridors.
- Quantitative figures (capacity, talent, CAPEX ranges) are scenario-based orders of magnitude; all numbers are indicative and subject to partner due diligence and site-specific design in Phase 0.



About the Authors:

Norbert Herfurth earned his PhD (TU Berlin, 2020) in semiconductor failure analysis. 2013–2019 he worked in TU Berlin's Semiconductor Devices group. Since 2020 at IHP—initially as cross-department postdoc/project coordinator, now research group lead. He initiated and still shapes IHP's open-source activities, including Europe's first open-source PDK. Currently he focuses on open source hardware and chiplet integration ecosystems.

Current employment is for identification only; views are personal.
Contact: ref-fab@hep-alliance.org

Arnd Weber is an economist and sociologist. Until retirement he was researcher at KIT, advising the EU Commission, EU Parliament and German government. His PhD traced the rise of public-key cryptography; he co-designed untraceable, loss-tolerant e-money, analysed the Dresden semiconductor cluster, and in 2003 predicted issues in European mobile data services. He founded "Quattro S" and helped initiate the HEP project on an open hardware security module. Currently he is subcontractor to IHP for the SIGN-HEP project (information is for identification only; views are personal). Contact: arnd.weber@alumni.kit.edu

Steffen Reith is Professor of Theoretical Computer Science at RheinMain University of Applied Sciences in Wiesbaden. During his work at Elektrobit Automotive, he developed products with cryptographic functions for use in current automobiles.

Contact: Steffen.Reith@hs-rm.de

Anna Herfurth is Head of Human Resources at IHP. She brings over six years of leadership experience in strategic HR, organizational development, and digital transformation. At IHP, she drives talent development, employer branding, and workforce structures for a high-tech research environment. In the Reference Fab initiative, she contributes expertise in HR strategy, skills pipelines, and dual education models for the semiconductor industry.

Current employment is for identification only; views are personal.

René Scholz earned a PhD in physics (MLU Halle-Wittenberg, 1999) after research on point-defect diffusion in Si and GaAs at the Max Planck Institute of Microstructure Physics. He joined IHP in 2001 for RF characterization and modeling, later leading the MPW Service and PDK development. He also holds an MBA (European University Viadrina, 2008). Recently, he contributes to IHP's open-source BiCMOS PDK.

Current employment is for identification only; views are personal.
www.linkedin.com/in/rene-scholz-86b4473

Torsten Grawunder is a hardware/security engineer. He studied physics of electronic components at TU Chemnitz, specializing in ASIC design for communication technology. Since 2021 he has worked at Swissbit Germany AG in system design/embedded solutions (APATS), creating and analyzing pre-development system concepts for future NAND-flash products and coordinating Swissbit's funding processes. Previously, for 20+ years, he developed encryption hardware for ISDN, ATM and Ethernet at Biodata, secunet and Rohde & Schwarz SIT.

Contact: torsten.grawunder@swissbit.com

List of Abbreviations (Executive Summary)

Abbreviation	Meaning
ADK	Assembly Design Kit
AMS	Analogue and Mixed-Signal
ATE	Automated Test Equipment
CAPEX	Capital Expenditure
CD/CI	Continuous Deployment / Continuous Integration
ENISA	European Union Agency for Cybersecurity
EQF	European Qualifications Framework
FDI	Foreign Direct Investment
IP	Intellectual Property
IQ/OQ	Installation Qualification / Operational Qualification
KRITIS	Critical Infrastructure (German: *Kritische Infrastrukturen*)
LTAs	Long-Term Agreements
MES	Manufacturing Execution System
ML	Machine Learning
MoU	Memorandum of Understanding
MPW	Multi-Project Wafer
OPEX	Operational Expenditure
OSAT	Outsourced Semiconductor Assembly and Test
PDK	Process Design Kit
PMIC	Power Management Integrated Circuit
PPP	Public–Private Partnership
RBAC	Role-Based Access Control
RDL	Redistribution Layer
SiP	System-in-Package
SLT	System-Level Test
SoC	System-on-Chip
SoP	System-on-Package
SPC	Statistical Process Control
SPV	Special Purpose Vehicle
TRF	Transparent Reference Fab
UCIe	Universal Chiplet Interconnect Express
VET	Vocational Education and Training
WSPM	Wafer Starts per Month

The European Reference Fab – Key Clarifications at a Glance

(For detailed answers, see the "Full Q&A" section at the end of this document.)

Q1 – Role of RTOs, EU pilot lines and OpenPDKs
The Reference Fab does not replace RTOs, national or EU pilot lines, or existing open PDK initiatives. It builds on and industrialises their results: RTOs and pilot lines remain the place where new technologies are developed; the Reference Fab turns mature bricks into trusted, repeatable manufacturing capacity at 130 → 65 nm.
→ Details: see **Q1 – Is the Reference Fab meant to replace existing RTO pilot lines, EU pilot lines or national initiatives?**

Q2 – Financial concept & infrastructure logic
The Reference Fab is conceived as public-interest infrastructure for security-relevant chips, not as a speculative stand-alone fab project. Strategically backstopped demand is expected from defence, critical infrastructure and public administration, while most wafer volume within a capacity corridor of roughly 3–7k WSPM should come from trusted standard building blocks and industrial/SME use. A certain amount of deliberate over-capacity is part of the resilience mission, not a planning error.
→ Details: see **Q2 – What is the business and public-interest rationale behind the Reference Fab?**

Q3 – Filling a 3–7k WSPM Reference Fab
We explicitly do not claim that high-security use cases will fill the fab on their own. Fully auditable defence/KRITIS chips form the political and strategic core, not the volume engine. Volume within the 3–7k-WSPM corridor is expected from two additional "rings": (i) trusted standard building blocks (secure MCUs, communication and control ASICs) used across many sectors, and (ii) an ecosystem ring (SMEs, MPWs, packaging-first SiPs, selected industrial ASICs) – plus future critical products that are not yet visible today but will require trusted manufacturing.
→ Details: see **Q3 – How do you plan to fill a 3–7k WSPM Reference Fab if defence and critical-infrastructure applications only need a few wafers per month?**

Q4 – "Packaging-First" vs "Packaging-Only"
"Packaging-First" does not mean "packaging-only". The main investment is a 300-mm CMOS front end at 130 → 65 nm; advanced packaging and test are treated as first-class design dimensions from day one so that trusted 130/65-nm chips can be combined with other dies (including leading-edge compute) in secure SiP and chiplet architectures.
→ Details: see **Q4 – Is this primarily a packaging initiative? What about the front end?**

Q5 – 200-mm lines vs a 300-mm Reference Fab
For the tiny, fully auditable security core alone, a 200-mm line would be technically sufficient. But the Reference Fab is meant to be a blueprint for a scalable, packaging-first

65-nm ecosystem, not a standalone niche line. Today, European 65-nm space/defence platforms, advanced packaging and fan-out flows, and likely future clone fabs all rely on 300-mm infrastructure. The concept therefore keeps 300-mm as the anchor blueprint, while 200-mm pilot lines at RTOs and IDMs remain complementary parts of the wider network.
→ Details: see **Q5 – Given that actual high-security volumes are small, wouldn't a 200-mm line be more appropriate than a 300-mm Reference Fab?**

Q6 – Origin and realism of the 65 nm process
The roadmap to 65 nm is phased and conditional. The first non-negotiable milestone is a full industrial reference at 130 nm; 65 nm is a target option that depends on securing suitable industrial partners, funding and demand. The concept already delivers substantial value at 130 nm and does not collapse if 65 nm arrives later or only at selected sites.
→ Details: see **Q6 – Where does the 65 nm process come from, and is it realistic to reach 65 nm within four years?**

Q7 – Timeline, permitting and local acceptance
The illustrated roadmap is an indicative scenario, not a detailed permitting plan. It assumes a brownfield approach for the first Reference Fab, with early site work in Phase 0 and a clear ESG concept for energy, water and chemicals. A pure greenfield project would require more time; the key point is the sequence of steps, not a fixed calendar year.
→ Details: see **Q7 – Is it realistic to move from "consortium and site agreed" to starting construction within roughly a year? What about permits and local green/eco opposition?**

Q8 – European dimension and avoiding a "two-speed" Europe
The Reference Fab is explicitly designed as a **network blueprint**, not a single Western flagship. The idea is to validate a trusted architecture, governance and workforce model that can be cloned in additional regions – including Central, Eastern and Northern Europe – once political and industrial conditions are right.
→ Details: see **Q8 – How does the Reference Fab concept address the risk of a "two-speed" Europe where only a few Western regions host advanced manufacturing?**

1. Role of RTOs, EU pilot lines and existing OpenPDKs

Q1: Is the Reference Fab meant to replace existing RTO pilot lines, EU pilot lines or national initiatives?

Longer answer: Europe already has:

- RTOs, national and EU pilot lines (e.g. FAMES, NanoIC, APECS), which
  - focus on low- to mid-TRL innovation (typically TRL 3–6),
  - explore new materials, device concepts, processes and packaging,
  - run demonstrators and experiments with evolving flows and equipment.
- Design access & open PDK initiatives (e.g. Europractice, Chips JU design platforms, IHP's open 130 nm PDK), which
  - enable academia, SMEs and start-ups to design ICs on various nodes,
  - increasingly support open-source tools and, in selected cases, open PDKs.

What is missing is an industrial, long-term, trusted manufacturing layer. This is where the Reference Fab comes in:

- It provides a stable, volume-capable environment at established nodes (130 → 65 nm) with long-term process baselines.
- It turns mature RTO/pilot-line results into standardised, documented, auditable process bricks that can be replicated across multiple sites.
- It acts as a reference implementation of trusted manufacturing, test and packaging, including open PDK/EDA integration, traceability and audit trails.
- It offers sustained capacity for security-relevant chips, which classic pilot lines and academic MPW services are not designed to provide.

In this logic:

- RTOs and pilot lines remain where new ideas are created and matured.
- Design-access initiatives and open PDKs ensure that more actors can design chips.
- The Reference Fab network is where the "best of" these ideas and designs become deployable infrastructure: trusted, repeatable manufacturing capacity.

Governance and participation of RTOs

The concept explicitly envisages RTOs as core partners, for example by:

- representing RTOs on strategic and technical advisory boards,
- assigning them lead roles for selected process, test or packaging modules,
- involving them in operating the Academy and training programmes,
- running joint projects that extend the capabilities of the network,
- involving them in Phase 0 (evaluation of technology options, site strategies and integration with existing pilot-line activities).

RTOs therefore do not "lose their role"; they gain a new outlet for mature technologies and a stronger voice in how trusted manufacturing infrastructure is designed and governed.

2. Financial concept & infrastructure logic

Q2: What is the business and public-interest rationale behind the Reference Fab?

Short answer: The Reference Fab is conceived as public-interest infrastructure for security-relevant chips, not as a speculative stand-alone fab project. Strategically mandated demand is expected to come from defence, critical infrastructure and public administration, while most wafer volume is expected to come from trusted standard building blocks and industrial/SME use – within a **capacity corridor of roughly 3–7k WSPM**. A certain amount of deliberate over-capacity is part of the resilience mission, not a planning error.

Longer answer: The core idea is to treat trusted manufacturing for certain chip classes as infrastructure, comparable to energy networks, rail hubs or secure communication systems. The "return" is twofold:

1. **Direct economic return**
    - Foundry revenue from producing MCUs, mixed-signal, RF, secure elements and other long-lifecycle chips at 130 → 65 nm.
    - Revenue from advanced packaging, SiP and test services.
2. **Indirect strategic return**
    - Reduced supply-chain risk for defence, security and critical infrastructure.
    - Higher resilience against geopolitical shocks and export controls.
    - A stable platform on which European SMEs and system integrators can build secure products.

After a more detailed internal volume analysis and first feedback on this paper, we moved from a single '5k WSPM' point estimate to a more realistic capacity corridor of roughly 3–7k WSPM. Within that corridor, fully auditable high-security niches (defence, space, very critical KRITIS controllers) form a small but indispensable sovereignty core: they only use a few wafers per month, but they justify the infrastructure politically and strategically.
To make the fab economically viable within this corridor, the concept adds:

- a ring of trusted standard building blocks (e.g. secure industrial/energy communication controllers, secure gateway SoCs, long-lifecycle MCUs with integrated hardware security, sensor/actuator hubs) that can be re-used across many verticals, and
- a broader ecosystem ring of SME customers, MPW runs, small-to-medium series and packaging-first SiPs, plus future critical product classes we cannot yet foresee but that will value trusted, transparent manufacturing.

Because of its infrastructure role, the financial concept is explicitly based on public–private risk sharing: public actors provide capital support, guarantees and long-term mandates; industrial partners provide co-investment, product commitments and know-how. The aim is not to finance a "mega fab" purely via speculative private volume, but to establish critical

infrastructure with a clear public mission, underpinned by a realistic mix of sovereignty core, scalable trusted products and a diversified industrial/SME ecosystem.

Q3: How do you plan to fill a 3–7k WSPM Reference Fab if defence and critical-infrastructure applications only need a few wafers per month?

Short answer: We explicitly do not claim that high-security use cases will fill the fab on their own. Fully auditable defence/critical chips are the political and strategic core, not the volume engine. Volume within the 3–7k WSPM corridor comes from two additional "rings": (i) trusted standard building blocks (secure MCUs, communication and control ASICs) used across many sectors, and (ii) a broader ecosystem ring (SMEs, MPWs, packaging-first SiPs, selected industrial ASICs) – plus future critical products that are not visible today but will require trusted manufacturing.

Longer answer: If you look at the wafer maths honestly, fully auditable, mission-critical applications – tactical radios, rad-hard controllers, secure substation SoCs, safety PLCs – only consume dozens to perhaps a few hundred 300-mm wafers per year, i.e. on the order of a low tens of WSPM. In our first feedback round on this concept, this led to define a capacity corridor of roughly 3–7k WSPM, with 5k WSPM as a design point inside that corridor, not a hard target.
Within this corridor:

- The inner sovereignty core (defence, high-end space, very critical KRITIS controllers) provides a small but contractable demand floor and the political rationale for the Fab.
- A second ring of trusted building blocks – secure communication and control ASICs, long-lifecycle MCUs with integrated hardware security, sensor/actuator hubs – can be re-used across energy, industry, med-tech, transport and public IT and is expected to generate most of the stable wafer volume.
- A third ecosystem ring – SMEs, MPWs, small/medium series and packaging-first SiPs – adds diversified demand and keeps the platform open for innovation.

Even so, we do not assume that the fab will always run at the upper end of the 3–7k corridor. A certain amount of unused capacity is deliberate:

- as a strategic buffer for crisis-induced ramp-ups and supply-chain shocks,
- as a scaling option for new trusted building blocks and future critical applications we cannot yet anticipate, and
- as a training and demonstration platform for potential clone sites.

In practice, the Reference Fab is therefore dimensioned as a flexible 3–7k WSPM module with 5k WSPM as a representative design point. The actual operating point will evolve over time with product portfolio, policy priorities and unforeseen critical-use cases, rather than being a fixed number on day one.

3. “Packaging-First” vs “Packaging-Only”

Q4: Is this primarily a packaging initiative? What about the front end?

Short answer: “Packaging-First” does not mean “packaging-only”. The main investment is a **300-mm CMOS front end at 130 → 65 nm**. Packaging and test are treated as first-class design dimensions from day one, so that trusted 130/65-nm chips can be combined with other dies (including leading-edge compute) in secure SiP and chiplet architectures.

Longer answer: The concept is based on two observations:

1. Many security-relevant chips (MCUs, RF front ends, mixed-signal, secure elements) are perfectly viable at mature nodes (≥ 65 nm).
2. System performance and functionality increasingly depend on how dies are integrated and packaged, not only on the node of individual dies.

Europe therefore needs both:

- control over mature-node front-end processes for security-relevant chips, and
- advanced packaging and test capabilities to integrate these chips with other dies.

What “Packaging-First” means in this context

The Reference Fab is conceived as a combined front-end + packaging + test environment:

- The front end offers
  - 300-mm CMOS at 130 → 65 nm as “evergreen” security nodes,
  - open PDKs and MPWs,
  - process baselines suitable for long-lifecycle, security-relevant products.
- The packaging and test side offers
  - advanced wafer-level packaging (e.g. RDL, fan-out, interposers, SiP/SoP),
  - secure test flows (ATE/SLT) with auditability,
  - chiplet/SiP integration paths that can combine trusted 130/65-nm dies with advanced compute manufactured elsewhere.

“Packaging-First” therefore means:

- packaging, test and system integration are designed in from the start, not added later,
- front-end decisions are taken with future SiP/chiplet and security requirements in mind,
- the network supports both
  - stand-alone 130-/65-nm products, and
  - multi-die systems with trusted control or security dies co-packaged with high-performance compute.

In short: the Reference Fab is a fab concept with integrated advanced packaging, not a packaging-only project.

Q5: Given that actual high-security volumes are small, wouldn’t a 200-mm line be more appropriate than a 300-mm Reference Fab?

Short answer: For the tiny, fully auditable security core alone, a 200-mm line would be technically sufficient. But the Reference Fab is meant to be a blueprint for a scalable, packaging-first 65-nm ecosystem, not a standalone niche line. Today, European 65-nm space/defence platforms already run on 300-mm, advanced packaging and fan-out are developed on 300-mm, and future clones and specialisations will almost certainly build on 300-mm infrastructure. The concept therefore keeps 300-mm as the anchor blueprint, while 200-mm pilot lines at RTOs and IDMs remain part of the wider network rather than the main reference.

Longer answer: From a pure device perspective, most high-security use cases we discuss – rad-hard FPGAs, secure controllers, crypto ASICs, safety PLC cores – could in principle be built on 200-mm 130/180-nm lines. Historically, that is exactly how many space and defence chips were manufactured, and given the very small absolute wafer volumes in these niches, 200 vs. 300 mm does not decide viability.
However, the Reference Fab is intended to solve a broader, system-level problem:

- provide an industrial-grade 65-nm node on 300-mm that is compatible with existing European platforms (e.g. C65-class technology),
- embed this node into a packaging-first, chiplet/SiP-capable backend (RDL, fan-out, 2.5D / 3D),
- and serve as a replicable blueprint for future clones and specialisations that are expected to operate in the 3–7k-WSPM corridor.

On all three axes, 300-mm is the relevant industrial reference today:

- European 65-nm space/defence platforms are implemented in 300-mm fabs; a 300-mm Reference Fab can align with that ecosystem (IP, libraries, qualification regimes).
- State-of-the-art fan-out, RDL and heterogeneous packaging flows are being developed and industrialised primarily on 300-mm wafers; panel-level initiatives also start from this base.
- Public and private investments (Chips Act, IPCEI, private foundries) focus on 300-mm infrastructure; future clone fabs that want to reach 2–5k WSPM per site will almost certainly be 300-mm sites.

This does not make 200-mm irrelevant. Quite the opposite: existing 200-mm lines at RTOs and IDMs remain the lab and pilot tier in the network:

- experimenting with new process bricks,
- supporting exotic technologies and low-volume prototyping,
- feeding successful bricks into the 300-mm Reference Fab once they are mature.

We therefore state openly:

- Yes, purely from a niche-volume perspective, a 200-mm line could support the high-security core.

- No, it would not be sufficient as a European reference blueprint for 65-nm-class, packaging-first, clone-ready manufacturing.

The RefFab design thus keeps 300-mm as the main reference platform, while treating 200-mm capacities at existing RTOs as complementary parts of the wider Trusted Manufacturing Network, not as a substitute for the Reference Fab itself.

4. Origin and realism of the 65 nm process

Q6: Where does the 65 nm process come from, and is it realistic to reach 65 nm within four years?

Short answer: The concept assumes a **phased approach**: first a full industrial reference at **130 nm**, then a **conditional** evolution path towards **65 nm**, depending on partners and funding. 65 nm is a *target option*, not a guaranteed milestone at a fixed date.

Longer answer: The paper sketches a roadmap from 130 nm to 65 nm because:

- many security-relevant products can run long-term at 130 nm,
- but some mixed-signal and integration use cases benefit from 65 nm,
- and a 65 nm baseline would strengthen Europe's position in chiplet and SiP architectures.

However, the path to 65 nm is non-trivial:

- In the EU there are only a few 130/110 nm CMOS baselines that could realistically be extended.
- A direct 130 → 65 nm shrink requires significant engineering effort and at least one strong industrial fab partner.
- Process transfer from outside Europe would need careful governance.

For this reason, the roadmap should be read as having two levels:

1. Core milestone: 130 nm industrial reference
    - Establish and stabilise a trusted, audited 130 nm manufacturing environment with open PDK, MPW and product platforms.
    - Integrate packaging and test, validate governance, security mechanisms and workforce concepts.

This is the non-negotiable foundation of the network.

2. Conditional evolution path: 65 nm
    - 65 nm would be pursued only if
        - a suitable industrial anchor partner is in place,
        - funding and demand justification exist,
        - and the 130 nm platform is stable.
    - Possible routes include co-development with a European fab that already has a 130/110 nm baseline or a well-governed transfer.

The Reference Fab network can already deliver substantial value at 130 nm:

- secure MCUs, mixed-signal, RF and sensors for defence and KRITIS,
- secure elements and roots of trust,
- control and interface chips for chiplet-based systems using external leading-edge compute.

Moving to 65 nm strengthens this model, but the concept does not depend on achieving 65 nm by a specific year. Whether this can be achieved within roughly four years depends on securing a suitable industrial partner, funding and a stable 130 nm baseline. It should be seen as an **ambitious scenario**, not a hard promise; the concept does not depend on hitting 65 nm by a particular calendar year.

5. Timeline realism, permitting and local acceptance

Q7: Is it realistic to move from "consortium and site agreed" to starting construction within roughly a year? What about permits and local green/eco opposition?

Short answer: The illustrated roadmap is an **indicative scenario**, not a detailed permitting plan. It assumes a **brownfield** approach for the first Reference Fab. A pure greenfield project would likely require more time and carry higher environmental and permitting risks.

Longer answer: The Gantt chart deliberately simplifies a complex reality. Key implicit assumptions are:

1. Brownfield rather than greenfield for the first site

The initial Reference Fab is assumed to be an expansion or deep modernisation of an existing industrial site, where

- basic utilities (power, water, logistics) are already available,
- the local ecosystem is familiar with industrial operations,
- permitting precedents exist.

A true greenfield fab on untouched land would require more extensive assessments, face greater exposure to local opposition and likely add several years to the schedule.

2. Early parallel work in Phase 0

Phase 0 ("consortium, site and financing agreed") is not purely contractual. It also includes:

- pre-selection and evaluation of candidate sites,
- early discussions with local authorities and communities,
- preparation of environmental and construction permit documentation.

In practice, part of the permitting groundwork starts before the formal "Phase 1.1" in the chart.

3. ESG as a design constraint

To mitigate "green/eco worst cases", the Reference Fab blueprint treats:

- energy efficiency,
- water use and recycling,

    - chemical handling and exhaust treatment

as design constraints from the outset, aligning with local regulation and EU sustainability goals. A credible ESG concept is essential for permits and acceptance.

How to read the timeline

The roadmap should be understood as:

- a plausible but optimistic scenario for an initial brownfield Reference Fab,
- assuming strong political backing, early site work in Phase 0 and a robust ESG concept.

In more conservative scenarios, Phase 0 could take longer and construction might shift by 12–24 months. The key point is the sequence, not the exact calendar year:

1. Agree consortium, site strategy and financing model.
2. Secure permitting and retrofit/expand at an appropriate site.
3. Establish a stable 130 nm reference manufacturing and governance model.
4. Then consider evolution to 65 nm and network roll-out.

6. European dimension and avoiding a “two-speed” Europe

Q8: How does the Reference Fab concept address the risk of a “two-speed” Europe where only a few Western regions host advanced manufacturing?

Short answer: The Reference Fab is explicitly conceived as a **network blueprint**, not a single Western European flagship. The goal is to create a model that can be cloned in additional regions – including Central, Eastern and Northern Europe – once political and industrial conditions are right.

Longer answer: Existing maps of European semiconductor capabilities tend to highlight a few established clusters in Western Europe. This risks reinforcing the perception – and the reality – of a “core” Europe with advanced fabs and a “periphery” without meaningful manufacturing capability.

The Reference Fab concept addresses this in three ways:

1. Blueprint, not one-off project
    - It defines a reference architecture (technology stack, governance, security and audit mechanisms, workforce model) that can be replicated.
    - The first site serves as a learning and validation hub, not as the only location.
2. Federated network, not central hub
    - The long-term vision is a federated network of sites that adhere to the same trust and governance principles.
    - Additional sites – including in Central, Eastern and Northern Europe – can join as they achieve the required capability and commit to the governance model.

3. Integration with existing competence centres
    - Chip Competence Centres (CCCs) and regional RTOs can act as bridgeheads: providing design and test expertise, workforce training and regional ecosystem building.
    - Over time, regions that start with design or test can upgrade to full or partial manufacturing sites based on the Reference Fab blueprint.

In this way, the Reference Fab is intended to reduce, not reinforce, the geographic imbalance in European manufacturing capabilities. It offers Member States a clear, trusted model to adopt when they decide to invest in security-relevant semiconductor capacity.

Further Information

Landing page & downloads: www.hep-alliance.org/Reference-Fab
(QR code resolves to this page)

Full RefFab Concept

Contact & briefing requests: ref-fab@hep-alliance.org
(or: nor.herfurth@gmail.com)

Suggested citation:
Herfurth, N., Weber, A., Reith, S., Herfurth, A., Scholz, R., & Grawunder, T. (2025). *The European Reference Fab – Blueprint for a* Trustworthy *and Transparent Manufacturing Network* (v2025-11-07). HEP Alliance. Available at: hep-alliance.org/Reference-Fab

Version & updates: v2025-11-27 · This executive summary and Q&A are living documents. Updated versions will be published on the landing page.