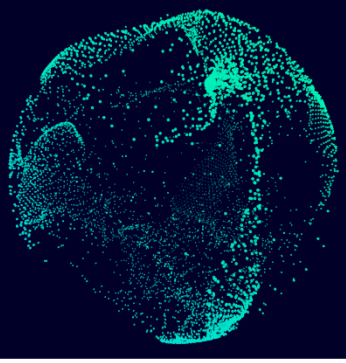

Siemens' Position on the EU Chips Act 2.0

Executive Summary

Siemens is uniquely positioned in the global semiconductor and electronics ecosystem. Siemens;

- designs its own chips and develops and manufactures electronics for its own products,
- is a large-scale user of semiconductors produced by others,
- is a key supplier of electrification, automation, digitalization and decarbonization solutions to the semiconductor and electronics ecosystem,
- is one of the top three globally leading EDA tool provider and the only tool provider from complex system level down to integrated circuits with the strongest footprint in Europe.

This paper outlines Siemens' position on the EU Chips Act 2.0 with the following policy recommendations:

- Pave the way for industrialization in Chips JU projects by involving large end-users from critical EU sectors (e.g., automotive, industrials, robotics, aerospace/defense, life sciences, energy) with attractive funding schemes.
- Improve the "lab-to-fab" concept to support both small-volume series production and mass production, ensuring direct industry involvement, including end-users, IDMs, and foundries.
- Expand Pillar 2's focus beyond frontend activities to address the broader supply chain including chip design, design enablement, backend activities and substrates/PCBs. In Pillar 2, address and secure the needs of end-users relying on mature chips.
- Provide public funding to existing semiconductor fabs and foundries via Pillar 2 to leverage Industrial AI accelerating productivity, digitalization and energy-efficiency to remain competitive.
- Redefine Pillar 3's focus to address politically driven challenges and restrictions on hardware/software technologies, moving beyond traditional supply-demand imbalances.
- Develop diverse reliable partnerships to secure access to all essential chip technologies (design tools, backend/frontend manufacturing, substrates/PCBs) for end-users.
- Refrain from imposing additional reporting burdens and mandatory sensitive/confidential information sharing on the semiconductor ecosystem.
- Increase the EU Semiconductor Board's visibility and foster regular, continuous engagement with industrial stakeholders, including end-users, to strengthen the ecosystem and develop a unified strategy.

The following part provides further details of Siemens' position on the EU Chips Act 2.0, based on the current 3-pillar structure.

Comments on Pillar 1 and IPCEIs

Industrialization & end-user involvement: The Chips JU initiative needs to strategically drive the industrialization of emerging technologies with attractive public funding (like quantum technologies, photonics, neuromorphic computing) where Europe can play a key role. This requires prioritizing solutions for real-world challenges, ensuring **scalability from R&D to industrial production**, and crucially, **involving large end-users from key EU sectors** (e.g., automotive, industrials, robotics, aerospace/defence, life sciences, energy...) early in the project lifecycle to define needs and guide development.

Improvements for "Lab-to-Fabs": The "lab-to-fab" concept needs improvements to move beyond research and pre-development to **support small-volume series production and mass production**, requiring direct industry involvement, including end-users, IDMs and foundries.

Competence Centers' focus: Such centers should adopt **a more focused, localized approach,** tailored to specific Member State needs, and actively support the valorization of Chips JU research results at local level.

Attractiveness of Chips JU projects: While Chips JU successfully supports even very large project consortia to grow ecosystems, its attractiveness should be improved with higher funding rates for all participants.

Streamlining IPCEIs: The process for IPCEs is overly complex and lengthy. The 2021 IPCEI communication needs revision to **allow faster approvals**, based on the current global market realities. A more centralized EU-level strategic framework and significant **EU budgetary contributions** will be essential for future IPCEIs in semiconductors.

Comments on Pillar 2

Europe's semiconductor resilience: The concept of resilience in the semiconductor industry extends far beyond the singular focus on frontend activities and increasing domestic wafer manufacturing capacity. **Broader supply chain security, including but not limited to** c**hip design, design enablement and backend activities and substrates/PCBs,** will be essential for Europe's semiconductor resilience, therefore should be within the scope of Pillar 2.

Focus on European end-users' needs: Public authorities' initial and largely current focus on leading-edge chip production in Europe overlooks the needs of end-users who also rely on mature chips. Pillar 2 should address European end-users' actual and future chip needs.

Leveraging Industrial AI: The Chips Act 2.0 is well-positioned to support **"Industrial AI"** in the EU semiconductor ecosystem (in particular in materials, equipment, IDM and foundry segments). In this regard, Pillar 2 could be extended to support schemes targeting existing semiconductor fabs in Europe to **leverage Industrial AI (including digital threads)** in boosting productivity, electrification, automation, digitalization, and energy-efficiency to increase Europe's competitiveness.

Substrates/PCBs: A chip, no matter how advanced, needs to be integrated into a system. PCBs are fundamental for packaging, interconnectivity, and the overall performance of electronic devices. Recognizing Europe's vulnerability in substrates/PCBs, Pillar 2 must operate beyond silicon manufacturing and **support resilient supply chains with innovation and investment in substrates/PCBs** in Europe.

Chip design and design enablement: Pillar 2's scope must be extended beyond wafer manufacturing and **broadened to design centers. Public funding should be provided for future and current fabless companies.** Such design centers should also receive support to access advanced EDA tools as well as incentives to use advanced foundry services (EU and non-EU) for prototyping and small-volume production. A new model for small-volume foundry access, like TSMC's "Value Chain Aggregators," which bundles orders and ensures design compliance, would be important to consider.

Pooling EU, national and private resources: Strengthening the EU semiconductor ecosystem, as Mario Draghi emphasized, requires **increased EU-level resources and a dedicated budget for Pillar 2 projects and IPCEIs.** The proposed EU Competitiveness Fund is ideally positioned to manage these resources, complementing national and private financing.

Comments on Pillar 3

Shortages: Pillar 3's current **focus on traditional "chip shortages" is insufficient for politically driven challenges**, where restrictions on hardware/software technologies are more complex than simple supply-demand imbalances. Pillar 3's current framework fails to detect such political events, leaving Europe vulnerable. And reactive intervention by public authorities after semiconductor crises is often too late and disruptive.

A new Pillar 3 approach: A crucial starting point is acknowledging that full autonomy or autarky in semiconductors is unattainable for Europe, as it is for other global players. The economic realities and cost structures of specific manufacturing segments, particularly for low-end chips and backend activities, mean **Europe will continue to depend on external chip technologies**. To master this intricate global landscape, Pillar 3 should also focus on **developing robust and diversified partnerships** with countries globally to maintain and facilitate further access to semiconductor and electronics technologies.

Building reliable partnerships: A fundamental redesign in Pillar 3 is needed, cultivating diverse **global partnerships with complementary strengths**. The focus should be on **securing access to all semiconductor and electronics technologies** (design tools, frontend/backend manufacturing...) for end-users through strong, reliable partnerships with diverse third countries, in particular in the APAC region.

Reporting and information sharing: Any new measures must rely on publicly available data or voluntary sharing of non-confidential information. Industry rejects mandatory disclosure (e.g., supply/demand planning) due to **risks of exposing confidential** or highly sensitive business data, creating competitive harm and increasing vulnerability to trade secret misappropriation and economic espionage. Furthermore, **additional reporting burdens** for the semiconductor ecosystem must be avoided. Finally, **interpreting** complex, context-specific supply chain **data requires deep industry expertise**, lack of which comes with the **risk of counter-productive policy interventions** by public authorities. This makes voluntary, collaborative approaches far more effective than mandatory reporting.

The EU Semiconductor Board: The Board's limited visibility impedes collaboration with industrial stakeholders. Greater transparency with regular and continuous engagement with industry (including end-users) is crucial for strengthening the European semiconductor ecosystem and developing a comprehensive, unified European strategy.