# Chips Act 2.0 – The Casimir Institute perspective

TU/e
EINDHOVEN UNIVERSITY OF TECHNOLOGY

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## The future of chips at TU/e's Casimir Institute

**Accelerating sustainable chips and high-tech systems innovation from research to impact**

Eindhoven University of Technology (TU/e) has been conducting pioneering research on chips for over fifty years. With its Casimir Institute, the university builds on its key position in the Brainport ecosystem and strengthens its role as an international frontrunner in chip research and development. The university's research institute brings together over 700 TU/e scientists focusing on semiconductors, quantum technology, photonics, advanced materials, high-tech systems, and fundamental research.

TU/e is also among the world's top institutions in research into new materials for chips. Major companies, such as Intel, TSMC, ASM, and ASML, collaborate with the university to leverage its unique expertise. In the cleanrooms, researchers work on layers only a few atoms thick and on promising new materials for chips, which may eventually replace traditional silicon.

These initiatives and projects are centrally coordinated and supported by TU/e's Casimir Institute, where researchers from various TU/e departments and services, as well as external partners, come together to work on the future of chips & high-tech systems.

Visit the Casimir Institute: www.tue.nl/casimir-institute

The institute is named after physicist Hendrik Casimir (1909–2000), one of the founding figures of the Dutch chip and high-tech industry. As a scientist and executive, Casimir played a key role in the development of fundamental physics and in the establishment of Philips NatLab in Eindhoven. With this name, TU/e honors Casimir's legacy and underlines that collaboration between science and industry is the key to technological progress.

## Vision - what trends do we see?

Chips are maybe the only truly exponentially scaling technology, as exemplified by Moore's Law. Although this narrowly refers to integration density, transistor size, and computing power, in a broader sense, this connects to an equally exponential scaling of memory, communication bandwidth, ubiquitousness of use, and energy-efficiency. This exponential scaling of 30× per decade is not about to end, but will trigger the need for new paradigms.

To scale *traditional computing*, also known as "More Moore", an increasingly interdisciplinary approach will be required, where new materials are to be embedded into the traditional silicon-based technologies, to push performance. Close collaboration with equipment suppliers is required to enable this at the nanometer-precision scale. It will become inevitable to consider the third dimension as well, which means that 2.5D and 3D heterogeneous integration paradigms will need to be leveraged more, again calling for close collaboration with equipment providers. Electronic design automation (EDA) tools will develop further to accommodate the co-simulation and co-design of multiple technologies in one seamless design platform. AI is increasingly leveraged to enhance EDA tools and to improve yield and fabrication lead times.

To scale computing power further, different *novel computing paradigms* are being considered. These include, among others, neuromorphic computing, quantum computing, photonic and optical computing, and oscillatory computing. Although many efforts are still exploratory and conceptual, a main trend is that many of these leverage existing semiconductor technologies and infrastructure, creating an outlook for true scaling and actual real-world impact. Applications can be specific, such as AI processors or compressed sensing at the edge, but are still extremely impactful.

The *network* to connect all of us and all these chips is equally exponentially growing in bandwidth and bandwidth density. For wireless communications, this means a push towards higher frequencies, going up to, and eventually beyond, 100 GHz. Optical wireless is complementing this now, for shorter and more secure links, and for space-based communications. The trend in wired communications is a slow but steady replacement of copper with fiber, leading to increasingly shorter interconnect lengths. Most datacenters use optical interconnects, and these interconnects are now reaching the processors. Co-packaged optics are seriously considered for high-end processors. All this means that electronic chips need to operate at millimeter-waves, a distinctly different field than digital electronics, and the use of integrated photonics is increasingly required. This also means that high-speed, analog, and digital electronics, antennas, and integrated photonics become increasingly intertwined, and fields such as co-design, co-simulation, and (heterogeneous) co-integration are key.

Finally, by leveraging and building on all these semiconductor technologies, a plethora of *sensors* that have the potential for ubiquitous use are already being developed and will continue to grow massively. This includes radar chips, all-solid-state lidar, optical gyroscopes, integrated quantum clocks, fiber-optics structural sensors, personal health monitoring, and many more. These are often at the edge, most notably in high-tech equipment, handhelds and wearables, automotive, aerospace, home appliances, and, ultimately, implantables.

## What are the specific relevant research challenges for Europe?

Chips are a global economy and technology. Europe should always consider global roadmaps and trends, and make clear choices about where to become competitive within its borders and where to build and rely on a global value chain. Some of the primary research challenges that Europe can and should address are as follows.

- Chips, including computing and communication, become faster and more energy-efficient. Industrial research should target 10x-30x improvements (7-10 years ahead), while academic research should target 100x-1000x improvements (up to 20 years ahead). This is from an overall system perspective, but drives the roadmaps. Furthermore, such research should keep credibility, feasibility, and scalability of technologies in mind, with a path to uptake by mainstream fabrication and simulation tools.
- One driver for increased performance is the seamless synergy and interplay that can be achieved between various technologies, and that can be realized using heterogeneous integration. The lack of high-end fabs and OSATs puts Europe at a disadvantage; however, new opportunities arise by leveraging our advanced ecosystem of semiconductor high-tech systems and by leveraging our leadership in novel technologies, e.g., photonics and spintronics. The challenge is to build on these strengths to achieve a strategic position in this field of heterogeneous integration.
- Europe still has a strong position in analog, mixed-signal, and RF chips. These are becoming increasingly important for, e.g., 6G, automotive, and defense and security applications. It's important to retain that position by continuing to push for higher frequencies and more broadband operation, higher powers, and more accurate signal processing and generation. Besides pushing for increased performance in silicon, a strong effort in compound semiconductors for high-frequency and high-power applications, and an integration with photonics, i.e., microwave and terahertz photonics, for low-noise and ultra-broadband applications, is required.

Europe should have control over all technologies that are key to critical infrastructure, e.g., communications. Paradigms like quantum communication and post-quantum communication are only as safe as the hardware, which should ideally be made in Europe. We need to have the required skills for that.

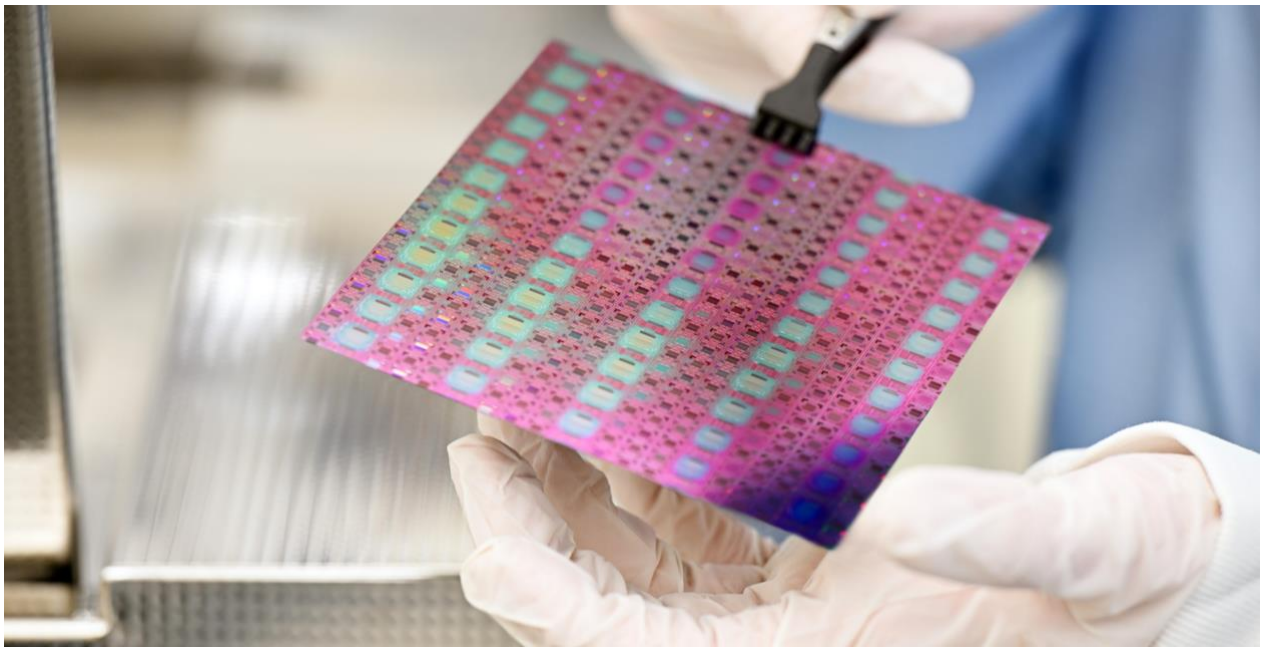
- Open-source hardware and software might be a solution to counter the exponentially rising cost of chip development.
- Europe has leading efforts in alternative computing paradigms, including, for example, neuromorphic and quantum computing. However, care should be taken to align these efforts with scalable technology platforms, thereby creating a path to real impact. Enabling technologies should be developed hand-in-hand with these computing paradigms and lab-based proofs-of-concept, to ensure that (future) companies can have their supply chain in Europe. Such technologies can include cryogenic electronics, integrated photonics, MEMS, and novel memory and nonlinear technologies.
- A seamless system of university labs, open prototyping facilities, industrial Pilot Lines, and volume production is required for (certain) existing and upcoming technologies. Low-TRL work is ideally conducted in an industrially relevant manner to ensure technology transfer opportunities and the education and training of relevant talent. The field of (fabless) "chip design", as known in silicon-based electronics, needs to be strengthened and expanded with fields in compound semiconductor, integrated photonics, and/or selected quantum technologies.

- The United States, Japan, and the Netherlands dominate the worldwide production of manufacturing equipment. The challenge is how to preserve this established high-tech ecosystem and ensure that we train the future engineers that the high-tech industry is seeking. Paradigms such as heterogeneous integration and the ever-increasing integration density push the envelope of manufacturing equipment, and targeted research on this equipment is required to stay at the leading edge and maintain our position. To maintain EU's leadership by 2040, four critical challenges must be tackled:
    - ensure the high-tech industry in the EU retains its operational license;
    - maintaining successful operations in global, highly competitive markets necessitates ongoing investments in competitive capabilities and innovation;
    - the growing shortage of highly skilled individuals needs to be addressed;
    - ensure the supply chain's resilience; at present, the necessary knowledge and technologies are threatened by substantial investments in China and the US, and risks like knowledge leaks.
- Enhance the digitization and automation of production and design processes. Ensure that digital twins, AI-driven manufacturing, embodied AI, and robotics are widely accessible, including to small and medium-sized enterprises (SMEs). Establish European initiatives focused on smart manufacturing and data-driven innovation, incorporating the necessary standardizations.

## Where should we invest, in the coming 10-20 years

Important boundary conditions for a future European strategy are the following:

- Embedding in a long-term strategy, with commitments of over 10 years, ideally 20 years;
- Setting up and following credible and useful research and industry roadmaps that are globally aligned;
- Relevant and in-depth deep tech expertise in program, strategy, and review committees, to ensure high-quality policies and execution;
- Careful balance between vested interests and new initiatives, both academic and industrial, to consolidate strengths and to catch up with global opportunities, respectively. Develop public-private investment initiatives to support the rise of new leaders at both national and EU levels;
- Invest significantly in STEM education and workforce (re)training, and attracting global talent;
- Develop sustainable and strategically independent supply chains by enhancing local and European networks to lessen reliance on other regions. Ensure that circularity and energy efficiency are essential criteria for all high-tech innovations.



Research in the context of chips should be aligned with an overarching strategy. Of course, there always needs to be room for free exploratory and blue-sky research, but we also need targeted research that focuses on strategic targets. Chips Act 2.0 could be the vehicle for that. This is quite often still fundamental research, as it targets timelines up to 20 years away, and improvements on the state of the art of 10x to 1000x.

## Universities have a key role in a chips strategy

- They are the talent pipeline for graduate and PhD-level talent. Care should be taken that universities educate their students (also) for the industry, also at the PhD level, without sacrificing the academic education. Opportunities are the "hard" transferable skills, e.g., expertise with 1) relevant EDA software, 2) industrially relevant fabrication processes and tools, and 3) technologies that are relevant in the real world. Close and early interaction between students and industry should be encouraged. Chips Act 2.0 should offer ubiquitous opportunities for universities to take this role.
- New startups often originate from universities. This means that universities should get the space to work on transformative and disruptive ideas that are also relevant. In other words, room for ideas that are not yet of interest for industry, but are too concrete to qualify as blue-sky research. Funding schemes could pay more attention to enabling such startups, i.e., by focusing more on team building and potential value chains with clear open and missing links that would enable opportunities and stimulate materialization.
- Embrace regional ecosystems more and use them better as building blocks of European collaboration. It appears that technology and talent transfer between universities and industry works best in a regional setting, for several reasons. We need to define such strengths and leverage these in a wider European context. We need to avoid talent leaving the field (or Europe) and ensure that technology lands with the European industry.

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