In-Depth Report

SEMI Europe – Chips Act Report

30 SEMI Recommendations for a Chips Act 2.0

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Foreword

Europe's Future in the Global Semiconductor Race

Semiconductors are the foundation of the modern digital economy. They power everything from smartphones, electric vehicles, and medical devices to the data centres and supercomputers that enable artificial intelligence and advanced research. In an increasingly interconnected and technologically driven world, secure and resilient access to semiconductors has become not only an industrial priority but a strategic imperative.

Over the past few years, the global semiconductor landscape has evolved rapidly, shaped by geopolitical tensions, supply disruptions, and unprecedented technological progress. These shifts have underscored both the opportunities and vulnerabilities that define Europe's position in the global value chain. While Europe remains a world leader in equipment, materials, and research, its share of global chip manufacturing has fallen over the past two decades, exposing critical dependencies on foreign production.

The European Chips Act marked a bold and timely response to these challenges. By combining strategic investment, public–private cooperation, and a coordinated policy framework, the Act has already mobilized significant resources to strengthen Europe's semiconductor ecosystem and reduce its exposure to external shocks. Its ambition to make Europe a global hub for innovation, design, and advanced manufacturing was both visionary and necessary.

Yet, the implementation of the Chips Act also reveals the complexity of translating ambition into lasting impact. To fully realize its potential, the policy must evolve to reflect new market dynamics as well as geo-political realities, ensure coherence across industrial and technological strategies, and create an environment that encourages both domestic innovation and international investment.

In our 30 SEMI recommendations for a Chips Act 2.0 we underline that it is important to build on Europe's strong foundations with pragmatic reforms that enhance efficiency, inclusiveness, and competitiveness. By aligning policy instruments, deepening cooperation with industry, and maintaining openness to global partnerships, Europe can secure its place at the forefront of semiconductor innovation and ensure that its technological sovereignty is rooted in strength, collaboration, and long-term competitiveness.

Laith Altimime
President, SEMI Europe

Introduction and Background Information

The European Chips Act, which has been in force since September 2023, had been a landmark legislation for the semiconductor industry in Europe. This unprecedented political effort by the European Union (EU) was spurred by the global chip shortage that took place as a result of the supply chain disruptions experienced during the COVID-19 pandemic. The chip shortage experienced in the aftermath of the pandemic highlighted the significant strategic dependencies and supply chain vulnerabilities of the EU's key manufacturing industries (Automotive, medical technologies, telecommunications, machinery and robotics), thereby leaving the EU overly reliant on foreign chips and excessively exposed to unpredictable exogenous factors (Geopolitical tensions, natural disasters, pandemics and climate crises).

For these reasons, the EU drafted a European Chips Act that could support technological capacity building and innovation in the EU, attract investments and enhance production capacity in semiconductor manufacturing and in advanced test, assembly and packaging (ATP).

The Chips Act has been instrumental in reinforcing the EU's capabilities in the sphere of semiconductors, bringing up to €45.2 billion in public and private investments, notably for manufacturing capacity investments (Pillar II) with the approval of six First-of-a-Kind (FOAK) semiconductor facilities. It has also implemented an ambitious pilot line framework (Pillar I) to further strengthen the EU's research and development (R&D) capabilities. As of October 2025, **the European Chips Act has catalysed a total of €69 billion in public and private investments,** powering new research and manufacturing capacity across Europe, and positioning the EU as the **third-largest global destination for semiconductor investments**[1].

While the 2023 European Chips Act was a great step towards mobilising investments in semiconductor manufacturing and R&D activities, a second Chips Act – "Chips Act 2.0" – will need to capitalise upon these successes, and **support the entire semiconductor supply chain in Europe, from R&D and design to materials, equipment and components, back-end and front-end manufacturing.** A well-functioning supply chain will be essential to sustain the EU's Chips Act ambitions, particularly with regards to advanced capabilities and resilience.

I.1 Scope and Methodology

SEMI Europe, the industry association **representing 3,500+ companies globally and 300+ companies in Europe** from the entire semiconductor supply chain, has undertaken an extensive consultation among its member companies to provide an in-depth assessment of the Chips Act implementation, and to outline concrete policy recommendations ahead the publication of the upcoming Chips Act 2.0.

[1] Investment value estimated by SEMI Europe based on its own data collection and corroborated by: ICOS (101092562), Monitoring semiconductor value chains: Implications for International Cooperation. URL: https://www.decision.eu/wp-content/uploads/2025/08/ICOS-D2.3-Deliverable_final-PUBLIC.pdf

For this crucial endeavour, SEMI Europe has conducted a significant information-gathering exercise, consisting of the following key elements:

- **SEMI Europe Survey** deployed across entire membership.
- **Bilateral interviews** with representatives from leading research and technology organisations, companies operating across the semiconductor value chain, including chip design and design tools, materials and components suppliers, equipment makers, back-end and front-end semiconductor manufacturers and innovative startups.
- **Three in-depth Chips Act workshops** with member companies and research and technology organisations (RTOs).

In total, input from **more than 60 companies and organisations** contributed to the development of this report. This group includes 44 European companies and 17 non-EU–headquartered companies, comprising 4 start-ups, 20 SMEs, and 37 large enterprises. The sample represents actors from across the entire semiconductor value chain: 9 public and private entities active in research, 5 in design, 14 materials suppliers, 16 equipment suppliers, and 9 front-end and back-end manufacturers, including 5 European and non-European IDMs. The picture is further complemented by contributions from independent experts, trade associations, and EU government agencies.

The extensive information that was gathered in the aforementioned process has been consolidated into the **SEMI Europe Chips Act Report** to provide a comprehensive overview of the Chips Act, with the aim of assessing the Chips Act implementation and its impact on the European semiconductor ecosystem, and proposing concrete policy recommendations for a Chips Act 2.0 that supports the entire semiconductor supply chain in Europe.

SEMI Europe kindly invites all policymakers and industry stakeholders involved in the revision of the Chips Act to carefully consider the assessments, observations and policy recommendations presented in this document.

Section 1 - Industry Impact Assessment

The objectives established in the Chips Act were primarily defined to tackle long-lasting supply chain vulnerabilities of the European Union and to strengthen Europe's research, innovation and industrial capacities in the sector. Accordingly, SEMI Europe respondent members (100%) deem it appropriate to strengthen Europe's technology leadership by reinforcing its innovation capacities in all segments of the semiconductor supply chain, in order to overcome current global challenges. On average, **87% of SEMI Europe respondent members agree with the general objectives of the Chips Act and 77% consider that they can be achieved in the medium and long-term.** These results exclude the Digital Decade target to achieve a 20% share of global production capacity by 2030, which is deemed unachievable by 90% of SEMI **Europe respondent members** and endorsed by only 13% of them. The support from the semiconductor industry that is expressed here, representing public and private organisations and companies from all segments of the supply chain, is to be read as a statement of support for the end-goals of the Chips Act.

Thus, **96% of SEMI Europe respondent members endorse the goal to develop next generation chip production,** bringing large-scale innovation and critical technologies via pilot lines public-private investments. However, fears remain that the lack of integration of the European Chips Act with relevant third-policy initiatives dedicated to AI, quantum, mobility, energy and defence, among others, will not coordinate future supply and demand for semiconductors in Europe.

If the supply and demand of advanced semiconductor technologies do not align, the Chips Act will bring limited benefits to the EU. So far, **the lack of market demand is the primary concern of SEMI Europe respondent members when exploring the possibility of investing in Europe** and building new facilities. The market uncertainties revolving around the European market have disincentivised companies to invest in Europe. Equally, impediments to the uptake of pilot lines' results, the limited attractiveness of the Chips Act's state aid framework compared to similar programs in third countries and the lack of a holistic support towards the entire semiconductor supply chain require the EU to adjust its policy approach.

SEMI Europe widely support the structure and objectives of the Chips Act. However, **its execution and numerous structural challenges will limit its success** and its spillover benefits for Europe's semiconductor ecosystem. The EU has designed a good and coherent policy tool in a time of emergency where a quick response was required. At this point in time, the EU should build upon the strengths of the first Chips Act, enhancing its framework and offering adequate framework conditions for the emergence of a strong semiconductor ecosystem in Europe.

1.1. Two Years On: Chips Act Investments' State of Play

The Chips Act was adopted with the stated objective of unlocking total investments of €86 billion towards the European semiconductor industry by 2030. Half of this amount was planned to originate from public funding, combining a €4.5 billion budget line from EU funding programmes

(Ex. Horizon Europe and Digital Europe Programme), €35.3 billion in state aid from Member States, €1.4 billion from other EU funding programmes and €2.1 billion in equity support. The remaining half of the investments (€43 billion) were expected to be leveraged from private investments from semiconductor companies and research organisations[2].

Approved semiconductor investments and funding in Europe have come under three main streams: **€21.8 billion** under the *Important Project of Common European Interest* (IPCEI) ME-CT, **€5.1 billion** for R&D pilot lines and **€53.8 billion** in confirmed/pending public–private investments for *First-of-a-Kind* (FOAK) and non-FOAK facilities. An additional funding of **€150 million** for other related projects were approved by the Chips Joint Undertaking (Chips JU). It should be noted that part of the IPCEI ME-CT investments, about **€12 billion**, are also included in the FOAK stream, reflecting overlapping project scopes.

Overall, as of October 2025, two years since the final adoption of the *Chips Act*, the initiative has **catalysed €69 billion across R&D projects and facility investments in Europe[3].**

1.1.1. IPCEIs

IPCEIs are transnational projects whereby EU Member States are allowed to provide state aid to projects that are highly strategic, innovative and cross-border in scope[4]. Characterised by their large-scale nature, IPCEIs involve public and private actors via collaborative projects that address major market failures in critical supply chains and compensate their associated risks (Technological and financial)[5].

Accordingly, in June 2023, 14 Member States adopted the **IPCEI on Microelectronics and Communication Technologies (ME-CT), bringing together 56 companies in 68 projects[6].** The IPCEI ME-CT represents a total investment of €21.8 billion, €8.1 billion leveraged by private investments and the remaining €13.7 billion provided via state aid. The joint programme supports R&D projects covering the entire semiconductor supply chain, from materials and chip design to manufacturing and end-user integration (Ex. 5G / 6G, autonomous driving, AI and quantum).

Following this considerable IPCEI, the largest to date, **15 Member States started to elaborate the next IPCEI on Advanced Semiconductor Technologies (AST).** This initiative will focus on the development of next-generation semiconductor technologies with a focus on AI, quantum, advanced packaging, photonics and power electronics, to support Europe's critical end-user industries. The level of public funding and private investment remains to be confirmed as Member States are now identifying relevant projects and actors that could be included in this next IPCEI.

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[2] Special report 12/2025: The EU's strategy for microchips – Reasonable progress in its implementation but the Chips Act is very unlikely to be sufficient to reach the overly ambitious Digital Decade target, European Court of Auditors. URL: https://www.eca.europa.eu/en/publications?ref=SR-2025-12

[3] Investment value estimated by SEMI Europe based on its own data collection and corroborated by: ICOS (101092562), Monitoring semiconductor value chains: Implications for International Cooperation. URL: https://www.decision.eu/wp-content/uploads/2025/08/ICOS-D2.3-Deliverable_final-PUBLIC.pdf

[4] Article 107(3)(b) of the Treaty on the Functioning of the European Union (TFEU).

[5] Communication (2021/C 528/02) on the Commission Criteria for the analysis of the compatibility with the internal market of State aid to promote the execution of important projects of common European interest. URL: EUR-Lex - 52021XC1230(02) - EN - EUR-Lex

[6] Press Release (June 8, 2023) on the Commission approval of €8.1 billion of public support by fourteen Member States for an Important Project of Common European Interest in microelectronics and communication technologies, European Commission. URL: Important Project of Common European Interest

1.1.2. Pilot Lines

Pilot lines are research and development (R&D) projects aiming to develop cutting-edge and next-generation semiconductor technologies in Europe. Pilot lines, falling under Pillar I of the Chips Act, are financially supported by the Horizon Europe and the Digital Europe Programme together with public-private investments[7]. Since the adoption of the text, **9 pilot line projects have been approved for a total of €4.8 billion,** where €3.7 billion are provided from EU funding programmes and complemented by a €1.1 billion investment.

The following pilot line projects have been approved or are currently being discussed under Pillar I of the Chips Act:

- **5 pilot lines on leading-edge semiconductors and related technologies** from 10nm to 2nm, advanced packaging, wide-bandgap semiconductors and advanced photonics.
- **4 joint pilot lines** between the EU and South Korea.
- **6 pilot lines for quantum technologies** with a funding of €50 million each.

This raises the total level of investments towards pilot line projects up to €5.1 billion, with approx. €4 billion funded from the EU budget and a €1.1 in other investment.

1.1.3. FOAK and non-FOAK investments

A central objective of the Chips Act is to attract European and non-European investments towards the semiconductor ecosystem in Europe, including public-private investments, support for manufacturing capacity building for technologies that are not yet present in Europe (*First-of-a-Kind*)[8]. As of October 2025, seven FOAK projects were confirmed and validated both at the EU and Member States level, representing **a total investment of nearly €31.4 billion, 40% of which are provided via state aid.** A seventh project is currently being negotiated in Czech Republic, with Onsemi planning to build a €2 billion end-to-end silicon carbide wafer facility. Besides FOAK projects, Intel and Bosch have both decided to upgrade and extend some of their existing facilities in Europe, investing respectively €12 billion and €3 billion.

Diamond Foundry Europe have also received the Commission's greenlight for a non-FOAK €675 million plant in Spain while Global Foundries has announced it will invest €1.1 billion in the expansion of its production capacities at the Dresden site. On top of these, NXP has obtained a €1 billion loan from the European Investment Bank (EIB) to finance its R&D activities across Europe, while ASML, together with the regional and governmental authorities of the Netherlands, will invest nearly €3 billion to strengthen its ecosystem in Eindhoven and its workforce development programs. The total **FOAK and non-FOAK public-private investments confirmed under the Chips Act account to €53.8 billion**. Four of these investments were made by non-EU companies, representing **a total foreign direct investment (FDI) of €20.5 billion,** on top of which a €10 billion joint venture between Taiwan's TSMC and three European companies (Infineon, Bosch, NXP) and a €7.5 billion joint venture between STMicroelectronics and Global Foundries (UAE) were approved.

[7] Regulation (2023/1781) establishing a framework of measures for strengthening Europe's semiconductor ecosystem (Chips Act). URL: Regulation - 2023/1781 - EN - EUR-Lex
[8] Chips Act (2023/1781). URL

1.2. Looking at the Big Picture

Two years after its adoption, the Chips Act has already **mobilised €69 billion in investments and public funding across R&D, front-end, and back-end manufacturing projects in Europe.** The third IPCEI under preparation is expected to further boost this figure. The EU is now approaching its €86 billion investment target, with contributions split between 48% public funding from Member States and EU funding, and 52% from private actors.

To complement this quantitative outlook, it is necessary to stress the internal and external challenges that the Chips Act is facing. The semiconductor industry, including private companies and public research organisations (RTOs) expresses concern about the **growing disconnect between the first and second pillars of the Chips Act,** particularly the lack of mechanisms to ensure the effective uptake of technological outputs from the pilot lines. In addition, investment concentration, the restrictive scope of the FOAK state aid, administrative burden, the limited policy toolbox available to Member States as well as insufficient end-market demand threaten the success of the Chips Act's second Pillar.

The Chips Act has undoubtedly incentivised and attracted strategic investments. The aforementioned external and internal challenges will however need to be overcome in the ongoing revision of the Act. For this reason, this Report aims to assess and analyse these underlying issues in-depth, in order to provide concrete policy recommendations that support policymakers in the formulation of a future Chips Act 2.0.

Section 2 - Strengthening the European Chips Act Framework

This section provides a comprehensive overview of the Chips Act's three pillars and their respective initiatives, highlighting key achievements, persistent challenges and forward-looking policy recommendations for a Chips Act 2.0.

Starting from **Pillar I of the Chips Act, the section examines the implementation of the pilot lines,** focusing on their administrative processes, industrial integration, and the need for stable, long-term funding to sustain Europe's leadership in semiconductor research and development. It also considers the ongoing development of the **Chips Design Platform**, a cornerstone for advancing design innovation, fostering collaboration across borders, and strengthening Europe's strategic capabilities in chip design architecture.

Following the analysis of Europe's R&D and design capabilities, the section then turns **to Pillar II and First-of-a-Kind (FOAK) investments,** assessing the current state of industrial projects, the sectorial concentration of investments, and the gaps that remain in supporting the broader semiconductor ecosystem. This part delves into the administrative and procedural barriers that delay project realisation and proposes measures to create a more flexible, coordinated and robust semiconductor ecosystem in Europe. Alongside, it explores one of the most critical themes of the semiconductor industry, **workforce development**, by assessing skill shortages, ongoing educational initiatives, and policy actions needed to secure a sustainable talent pipeline for Europe's rapidly evolving semiconductor landscape.

Lastly, the section evaluates **Pillar III**, emphasising the optimisation of **public–private collaboration for supply chain monitoring and crisis response**. It reviews the ongoing work of the European Semiconductor Board and the Industrial Alliance in developing effective governance structures, early warning indicators, and mapping tools to better anticipate and manage potential disruptions.

2.1. Pillar I - Pilot Lines

This part examines the implementation and evolution of **Pillar I of the Chips Act**, focusing on the pilot lines as a cornerstone of Europe's semiconductor R&D and industrial strategy. It explores how these pilot lines have become key instruments for bridging fundamental research and industrial application, enabling the development of advanced and next-generation semiconductor technologies. The section highlights their technological scope, early achievements, and the need to strengthen their operational efficiency, industrial uptake, and long-term funding within the EU framework.

Beyond their technological dimension, the section addresses **the administrative and structural challenges** that limit the accessibility and efficiency of pilot lines. It assesses procedural hurdles, funding eligibility gaps, and the barriers faced by smaller firms such as SMEs and

startups. Building on these findings, it proposes targeted policy measures to simplify procedures, foster collaboration between Research and Technology Organisations (RTOs) and industry, and accelerate the transition "from lab to fab to market." Ensuring that pilot lines deliver not only scientific excellence but also tangible industrial outcomes remains a central objective.

Finally, the section introduces the **European Chips Design Platform**, a strategic initiative aimed at reinforcing Europe's semiconductor design capabilities through a cloud-based, collaborative environment. Closely linked to the pilot lines and manufacturing infrastructures, this platform will play a critical role in strengthening design-to-fabrication synergies, fostering cross-border collaboration, and enhancing Europe's position in global semiconductor innovation.

2.1.1. Pilot Lines: A Coherent and Market-Oriented R&D Tool

Grounded in market realities, the Chips Act aims to equip Europe with the technological and manufacturing capacity needed to meet the rising demand for advanced and next-generation semiconductors. The R&D projects launched under Pillar I address growing needs in consumer electronics – such as personal computers and smartphones – while also supporting emerging demand from end-user industries (Autonomous driving, renewable energy, 5G / 6G, AI and quantum)[9]. To meet the technical, power, and energy requirements of these applications, the pilot lines focus on key enabling technologies like advanced packaging, chiplet architectures, photonics, and wide-bandgap semiconductors, essential for producing both sub-8nm and mature-node chips.

SEMI Europe welcomes the technological focus and the implementation of the pilot lines under Pillar I of the Chips Act. Since the adoption of the text, pilot lines have appropriately targeted semiconductor technologies that are pivotal to match the future market trends of the semiconductor and relevant end-user industries. To date, nine pilot lines have been approved for semiconductor technologies, representing a total investment of €4.8 billion. These include five focused on leading-edge semiconductors and related technologies – from 10nm down to 2nm – as well as advanced packaging, wide-bandgap semiconductors, and advanced photonics. In addition, four joint pilot lines are being developed in collaboration with South Korean researchers. The European Commission will soon announce six new pilot lines dedicated to quantum technologies, each worth €50 million, bringing total EU funding for pilot line projects to €5.1 billion.

SEMI Europe has observed that the implementation of the pilot lines has **increased businesses' interest in R&D projects** and, most importantly, **encouraged cross-segment** collaboration between RTOs and industrial actors – 70% of SEMI Europe respondent members acknowledge that the Chips Act incentivises collaboration between companies and RTOs. The effectiveness of the pilot lines is also visible in the global context, where these projects remain unique compared to the R&D programs implemented across different countries (Ex. U.S., China, Taiwan, South Korea and Japan).

[9] Future market trends on which this assessment relies can be retrieved in: SEMI & Kearney PERLab Report "*Braving the storm: navigating an uncertain future. State of Semiconductors 2025*". URL: State of Semiconductors 2025 | Kearney

Pillar I has effectively built upon one of Europe's major strengths in the semiconductor sector, relying on the advanced position of RTOs within global semiconductor R&D. While Europe has a competitive advantage in R&D, it remains vital to capitalise on its own program's effectiveness and successes by strengthening the pilot lines' architecture. This improvement must focus on the creation, facilitation and effective deployment of **synergies and collaboration between RTOs and the industry**, guaranteeing the effective industrial uptake of pilot lines' output, notably via swifter approval procedures.

2.1.2. From Lab-to-Fab-to-Market

In the September 29th declaration of the Semicon Coalition, signed by all 27 Member States, EU Council Members have insisted on the indispensable need to foster "complementary European collaboration between industries, RTOs, public research, SMEs and startups". To "strengthen the technology pipeline", Member States insist on guaranteeing **technology readiness and uptake** from lower R&D levels up to their industrial deployment. Despite the appropriate framing of the pilot lines and the targeting of prioritised technologies, there are already signals that structural challenges will hinder Europe's ability to translate the research results of pilot lines into commercially viable industrial opportunities.

2.1.2.1. From Lab-to-Fab-to-Market in Practice

Pilot lines encompass all R&D stages, from fundamental technology research (TRL 1) to the operationalisation of the developed systems (TRL 6). However, their outputs are not immediately ready for industrial use. So far, Chips Act pilot lines are "*research*" pilot lines that provide funding exclusively to public organisations, namely RTOs and academia. Under the current Chips Act framework, participating **companies must cover all associated costs**. To adopt pilot line results, they must adapt the technology's design and fabrication processes to their own equipment, taking on the additional work of advancing from TRL 7 to TRL 9 where products are refined and qualified for industrial production and commercialisation. This poses significant challenges, as semiconductor manufacturing equipment and related machine-specific software vary widely between companies and often differ from those used in the pilot lines.

Outside the pilot lines, the R&D success rate for semiconductor technologies developed by European RTOs ranges from **40% to 60% when companies are fully involved in the process**. Typically, RTOs must demonstrate both the quality and industrial potential of their technologies, often dedicating a full-time expert to help a company adapt the innovation to its production line. However, under the current framework, limited industry participation in pilot lines is expected to reduce their success rate and place significant financial burdens on RTOs.

Under the current system, companies bear the full cost of participation in and industrialising pilot line technologies. These expenses include accessing developed systems, completing product prototyping and development, integrating technologies into industrial applications, and ensuring their commercial viability, often requiring substantial material and logistical resources. Moreover, pilot lines depend on a skilled workforce familiar with specific company operations and facilities, a capability increasingly scarce in Europe. The significant time and resources required for both RTOs and industry to adopt new technologies have often **discouraged participation and limited the success of R&D projects**. Within the pilot line framework, this lack of synergy is likely to be amplified, resulting in suboptimal outcomes.

The **limited interoperability of raw technologies** emerging from pilot lines further complicates their industrial adoption and commercialisation, a process that is already resource-intensive, time-consuming, and uncertain. If these technologies fail to be integrated into industrial applications, their impact on Europe's semiconductor sector will remain minimal, if not negligible. Therefore, the success of pilot lines should not be measured solely by the development of new technologies, but by the combination of technological achievement and effective industrial uptake.

2.1.2.2. SMEs, Startups and Scaleups

For SMEs, startups, and scale-ups, the costs associated with accessing pilot line outputs are prohibitively high, effectively excluding them from benefiting from Pillar I advancements. The Chips Fund was designed to close this gap by improving access to capital through Horizon Europe's Innovation Council Accelerator and the InvestEU Fund. Yet in practice, **accessibility remains limited**. These smaller firms, despite their strong innovation potential, often lack dedicated funding or project management departments. As a result, many must outsource application and reporting processes to expensive consultancies, creating additional financial barriers that discourage participation. Instead of lowering barriers to innovation, pilot lines have inadvertently reinforced them, sidelining the very actors the Chips Act was meant to empower.

Strengthening collaboration between RTOs and smaller semiconductor companies is therefore essential. These firms often occupy specialised niches within the semiconductor value chain, supplying materials, components, and subsystems to larger manufacturers. Since major companies depend on extensive networks of sub-suppliers – sometimes numbering in the hundreds – limited SME access to pilot line outputs risks creating technological gaps across the ecosystem. This disconnect could slow the adoption of new technologies, as suppliers struggle to align their capabilities with the advanced outputs of pilot lines. Reducing access costs and **ensuring fair participation for SMEs, startups and scale-ups** is thus crucial to building a cohesive, multi-layered semiconductor innovation ecosystem in Europe.

2.1.2.3. Increasing R&D Synergies in the Pilot Lines

The Chips Act has successfully encouraged RTOs and industry to strengthen their collaborations. However, its current structure and European competition rules limit industrial participation in pilot lines, forcing companies to either cover all adoption costs themselves or rely on national support through Important Projects of Common European Interest (IPCEIs). As a result, while pilot lines are underway, the industrial uptake of these technologies – whether via IPCEIs or company resources – will take several years to yield tangible results. For SMEs, startups, and scale-ups, who currently lack access to pilot line outputs, additional time is required to develop compatible technologies or adapt existing solutions to meet these new systems and demands.

To achieve a fast, efficient, and cost-effective uptake of pilot line outputs, it is essential to recognise that **R&D is a multi-actor process involving RTOs, academia, and all industrial stakeholders**, spanning the full spectrum from basic research (TRL 1) to industrial adaptation and commercialisation (TRL 9). Active participation from both industry and academia is therefore critical to the success of pilot lines. Pillar I of the Chips Act faces two key challenges: first, ensuring that current pilot lines are successfully industrialised and commercialised; and second, building Europe's long-term advanced capacities by sustaining continuous investment in R&D to support the emergence of next-generation semiconductor technologies.

2.1.2.4. Industrialising Existing Pilot Lines and Creating Industrial Cycles

To support the uptake of Pillar I pilot lines, it is essential to bridge the industrialisation gap between pilot line outputs and their future users by implementing measures that maximise R&D success. One approach is the **creation of "*industrial*" pilot lines** that build on the results of existing "*research*" pilot lines from the first Chips Act, with a focus on industrialisation[10]. These "industrial" pilot lines would pool prototyping projects from companies of all sizes (large firms, SMEs, and startups) under a single framework to develop a single technology. This approach can reduce access costs, streamline the use of pilot line results, and accelerate industrialisation and commercialisation.

This strategy should be complemented by **preferential access to Pillar II state aid** for all semiconductor ecosystem investment projects linked to pilot lines, covering design, materials, components, equipment, chip manufacturing, and ATP operations. Together, these measures would create a more inclusive and efficient pathway from R&D to market-ready technologies, ensuring the full potential of Europe's pilot lines are realised.

SEMI Europe Recommendations – Pillar I and Pilot Lines (Cross-segment R&D)

Policy recommendation 1: Establish industrial pilot lines, supported by an EU budget line, that integrate projects from companies of varying sizes (large firms, SMEs, and startups) in research pilot line products' prototyping, development, and industrialisation, thereby accelerating industrialisation and commercialisation.

Policy recommendation 2: Guarantee a preferential access to Pillar II state support measures for all investment projects across the semiconductor ecosystem which are linked to the research and industrialisation pilot lines, including suppliers of, and operators in research, design, materials, components, equipment, chips manufacturing and assembly, test and packaging.

2.1.2.5. Chips Act 2.0: Pilot Lines' Funding in the Long-Term EU Budget

While Pillar II state aid exemptions provide ongoing and stable support for the industry, Pillar I currently appears more limited in scope and duration. Although the Chips Act provisions may assume that the European Commission will continue to develop and launch future pilot lines, significant uncertainty remains. Existing pilot lines focus on advanced technologies already being pursued globally, underscoring the need for sustained long-term investment in European R&D to maintain a leading position and keep pace with the sector's rapid evolution. Emerging technologies, including AI, quantum computing, and increasingly complex consumer devices, electric vehicles, and renewable energy systems, will drive new semiconductor demand, requiring capabilities that are not yet fully realised.

[10] So far, Chips Act pilot lines are "*research*" pilot lines that provide funding exclusively to public organisations, namely RTOs and academia.

To anticipate future demand and reinforce Europe's research leadership, the Chips Act 2.0 should establish a **cyclic renewed budget** line within the EU budget. Compared to global competitors channelling tens or even hundreds of billions of euros into domestic semiconductor investment, the current European framework lacks sufficient financial capacity. Securing a continuously renewed budget for pilot lines (Pillar I), alongside a stable state support framework (Pillar II), would provide the **policy predictability and stability** that the semiconductor industry needs. This approach would not create new funding mechanisms but would leverage existing programs for semiconductors. Allocating a portion of the pilot lines' budget specifically to industrial and academic actors, including dedicated support for SMEs, startups, and scale-ups, would further strengthen cross-segment collaboration, accelerating the industrialisation and commercialisation of pilot line outputs.

SEMI Europe Recommendations – Pillar I and Pilot Lines (Cross-segment R&D)

Policy recommendation 3: Amend Article 3 to secure future budget lines for financing future pilot lines for semiconductor technologies, anchored in the cyclic negotiations of the Multiannual Financial Framework (MFF) and relying on the existing Horizon Europe and Digital Europe Programme.

Policy recommendation 4: Dedicate a specific budget line in pilot lines projects to support industry's participation (Large multinational companies, SMEs, startups and scaleups) and to provide specific support to smaller players, mostly via pilot line vouchers, R&D vouchers and a specific budget line in pilot lines for SMEs, startups and scaleups.

2.1.3. Working Towards Swift Pilot Lines' Processes

Pilot lines are financially supported by the Chips for Europe Initiative, combining funding from Horizon Europe and the Digital Europe Programme, aiming to "achieve large-scale technological capacity building [...], advanced design, system integration and chip production capabilities in the Union"[11]. Although non-public actors have the possibility to be involved in the pilot lines, assuming that they bear the associated costs, pilot lines remain rather unattractive for a dominant share of the industry.

One barrier to pilot lines' attractiveness is the **administrative burden** associated with accessing the pilot lines. Application dossiers are lengthy, complex, and disproportionate to the level of funding requested. Applicants must navigate repetitive documentation and fulfil multiple procedural requirements, diverting significant human resources away from innovation processes. Once projects are approved, the reporting obligations represent another heavy hurdle. Financial reports, technical updates and compliance checks are often overly frequent and time-consuming, creating inefficiencies for the actors involved and forcing them to prioritise paperwork over genuine R&D activities.

In addition, the procedures themselves are **fragmented and rigid**. Single pilot line projects have led to the multiplication of contracts and tendering processes, delaying implementation. In practice, even the procurement of basic goods such as office supplies is subject to extensive

[11] Chips Act (2023/1781), article 4.1. URL

tendering, with no flexibility for early communication or coordination with suppliers. To go through the corresponding administrative processes, companies must commission additional full-time employees to the task. The direct **effect on smaller companies' resources (SMEs, start-ups and scale-ups) is disproportionally higher** while they remain essential for disruptive R&D. This procedural rigidity slows down project launches and adds layers of bureaucracy with little added value. It is worth stressing that an administrative simplification of the pilot lines must preserve the current framework for the Hosting Agreement and Joint Procurement Agreement, which were jointly developed by the European Commission and the RTOs to fit the specificities of the industry.

Finally, the **eligibility framework for funding** is not fully aligned with operational needs. While investments in equipment, tools and components are supported, other equally essential elements required for cleanroom operations (Ex. Energy, materials sourcing and storage) remain excluded from eligibility. This creates **funding gaps** that make participation impractical for many actors and could potentially undermine the long-term economic viability and industrial uptake of pilot lines' outputs. With regards to these challenges, SEMI Europe and its members have identified key targeted policy recommendations to fully mobilise Europe's semiconductor ecosystem and make pilot lines a greater success.

SEMI Europe Recommendations – Pillar I and Pilot lines (Simplification)

Policy recommendation 5: Introduce standardised templates across the pilot lines and a two-stage application process with a significantly shorter pre-proposal phase to reduce effort and streamline applications and reporting.

Policy recommendation 6: Set reporting requirements proportional to the size of the company, with lighter, more spaced and measurable reporting requirements centred on the outcome of R&D, for SMEs.

Policy recommendation 7: Reduce the number of required contracts for a single pilot line, exempting basic goods and services from extensive tendering rules, and allowing for early supplier engagement to reduce delays.

Policy recommendation 8: Extend eligibility criteria to cover essential cleanroom costs such as energy, materials sourcing, and storage, while introducing simplified cost models like lump sums and unit costs to reduce the administrative load on participants.

2.1.4. Chips Design Platform

The **Design Platform** established under the *European Chips Act* is a cornerstone initiative under Pillar I ("Chips for Europe") aimed at strengthening Europe's semiconductor design capabilities, by providing a virtual, cloud-based environment that integrates electronic design automation (EDA) tools, intellectual property (IP) libraries, and design facilities accessible to users across the EU.

A consortium of twelve European research and technology organisations (RTOs), coordinated by IMEC, CEA-Leti, Fraunhofer and Fondazione Chips, has been selected to build and operate the

platform under the Chips Joint Undertaking (Chips JU). The grant agreement is expected to run from 2025 to 2028. The technical development phase now focuses on constructing the cloud environment, populating it with EDA tools and IP libraries, and creating seamless design-to-fabrication routes through integration with pilot lines and packaging/test infrastructures.

In the coming months, the **main priorities include finalising funding arrangements, implementing the digital infrastructure, and defining access and cost models** for participants across Member States. The success of the Design Platform will ultimately depend on the effective collaboration between academia, industry, and national competence centres, ensuring that design activity is well connected to Europe's emerging pilot manufacturing lines and foundries.

2.2. Pillar II – First-of-a-Kind (FOAK) Facilities

The European Chips Act has incentivised EU Member States to provide direct financial support to companies for the construction of new semiconductor manufacturing facilities or the upgrade of existing ones. This measure has been central to the Act's success, improving the attractiveness of Europe's semiconductor ecosystem and encouraging strategic investments from both EU and non-EU actors. This section examines the implementation of Pillar II, including the **First-of-a-Kind (FOAK) framework**, and provides an in-depth analysis of the state of play, sectoral and geographical coverage, and the broader implications for Europe's semiconductor supply chain.

While Pillar II has been instrumental in supporting manufacturing activities, **a majority of SEMI Europe respondent members (60%) have expressed concerns** regarding the scope of strategic investments and the associated administrative burden. The sub-section explores these challenges in detail, including the exclusion of critical segments such as private R&D centres, chip design and design tools, semiconductor equipment, materials, and component suppliers. It highlights the need to extend support to these essential actors to strengthen Europe's semiconductor ecosystem, foster innovation, and ensure technological sovereignty.

Finally, this sub-section addresses **administrative and procedural challenges** that affect investment attractiveness and industrial uptake. Overlapping processes at both EU and national levels, lengthy validation timelines, and complex reporting obligations create resource-intensive hurdles for companies. The sub-section provides targeted recommendations to simplify FOAK, IPF, and OEF procedures, enhance coordination between Member States and EU authorities, and improve the overall flexibility of the policy framework. Together, these analyses form a comprehensive overview of Pillar II's strengths, limitations, and potential improvements, setting the stage for a more inclusive and competitive European semiconductor ecosystem.

2.2.1. First-of-a-Kind (FOAK) Investments' State of Play

Since the adoption of the Chips Act, six FOAK investment projects have been approved, totalling nearly **€24 billion** (as of October 2025). Five of these projects, amounting to €20.7 billion, focus on front-end manufacturing and target key end-user sectors such as automotive, medical devices, renewable energy, and consumer products. One project, valued at €3.2 billion, is dedicated to expanding back-end capacities in Europe, providing advanced packaging and testing solutions that integrate panel chiplets. Additionally, two other projects are being developed. Discussion between Onsemi and the Czech government to establish a €2 billion front-

end SiC wafer facility and a Global Foundry FD-SOI Wafer project in Dresden, Germany, are ongoing (see Annex I for a detailed overview).

The FOAK instrument should move beyond a short-term impulse to becoming a long-term strategic industrial policy instrument. Overall, the FOAK projects show a clear **sectoral concentration**, primarily focused on chips and specialised wafer fabrication, and geographically limited to a few countries, including Germany, Italy, and Austria. Notably, these investments largely **exclude R&D, design, semiconductor-related equipment, and materials and components production**. Combined with lengthy EU-level administrative procedures, these factors have delayed project launches compared to global competitors, limiting Europe's ability to attract and secure strategic investments in the semiconductor sector.

2.2.2. Shortcomings of the First-of-a-Kind Criteria

The sizeable investments that have been incentivised under Pillar II of the Chips Act have focused on increasing Europe's front-end semiconductor manufacturing capabilities in the most advanced segments. That said, numerous companies active in **other critical segments** of the semiconductor supply chain could have brought highly beneficial investments to the European Union and the growth of its semiconductor industrial capacities. However, their technologies did not qualify as FOAK projects and were therefore ineligible to receive state aid from their national governments. The current framework of the **Chips Act excludes companies that are critical for the European semiconductor ecosystem**, namely including private R&D centres, chip design and design tool, equipment, materials and components' suppliers, despite their strategic importance to achieve the overarching Chips Act objective to "strengthen the semiconductor ecosystem at Union level"[12].

This strategic gap in the definition and application of the FOAK criteria has prevented Europe's broad semiconductor ecosystem of private R&D centres, chip design and design tool companies, as well as semiconductor equipment, materials, and component suppliers, from benefiting from FOAK state aid and Pillar II support.

2.2.2.1. Semiconductor Supply Chain: A Missing Piece in FOAK

In pursuit of the EU's Digital Decade target to reach 20% share of global chip production by 2030, the Chips Act has so far prioritised strategic investments towards front-end manufacturing facilities. Among the 13 confirmed, paused and cancelled FOAK investments, ten projects are **focusing on front-end semiconductor manufacturing**, and three projects **focus on back-end manufacturing** (see Annex I).

The Chips Act' focus on increasing semiconductor manufacturing capacity in Europe rationally reflects the European Commission's and the Member States' policy priorities when the legislation was formulated. Following the global chip shortage that was caused by the COVID-19 pandemic, there was an unprecedented political momentum to support the EU's key manufacturing industries (Automotive, medical technologies, telecommunications, machinery and robotics), aiming to reduce strategic dependencies on foreign chips.

[12] Chips Act (2023/1781), article 1.1. URL

At this point in time, however, Europe's semiconductor ecosystem is strongly advocating for an **expansion of the Pillar II framework**, to ensure that the foreseen support measures can target the other critical segments of the supply chain, including private R&D centres, design and design tools as well as semiconductor equipment (Photolithography, metrology, inspection and testing), materials (Specialty gases, photoresists, polysilicon) and components suppliers (Photomasks, ultra-precise optics and photonics, raw wafers).

2.2.2.1.1. Private Research and Development Centres

Pillar I of the Chips Act created a framework for emerging semiconductor technologies in Europe, setting up dedicated funding schemes and pilot lines for the semiconductor industry. The considerable investments made by the EU have directly benefited public research organisations, namely RTOs and academia. **Private R&D centres and labs are not entitled to receive public support** from the EU, neither under Pillar I, nor under Pillar II from their respective national governments.

Semiconductor companies across the supply chain are highly R&D intensive, with an average R&D spending of 15%-20% of their total revenues. Multiple companies, including Intel and Bosch, are carrying out significant investments towards the expansion and upgrade of their existing R&D labs across Europe, to develop new technologies (Ex. 7nm chips). Nonetheless, the current Chips Act framework does not allow these crucial projects to receive public support at the EU or national level.

Private R&D activities are essential for companies to adapt to the rapidly changing technological evolutions and complex innovation cycles, particularly in the semiconductor industry, where there is a constant drive towards smaller, faster, and more energy-efficient chips. Besides the clear benefits towards our industry, these activities generate powerful spillover benefits across multiple end-user industries. As a matter of fact, advances in chip performance can facilitate the development of AI systems, safer and autonomous vehicles, smarter and connected factories, thereby fuelling innovation across the entire economy and enabling the green and digital transition.

2.2.2.1.2. Chip Design and Design Tools

Under the current Pillar II framework, facilities involved in the "design and production of equipment or key components for equipment" are eligible for support under the FOAK criteria. However, since the Chips Act's inception, **no investments in these segments** have materialised. Chip capabilities are primarily determined during the design phase, which involves critical architectural decisions to anticipate operational, sustainability, and energy efficiency requirements throughout a product's lifetime, as well as compliance with market regulations and supply chain resilience. This phase generates substantial intellectual property and advances Europe's capacities in strategic sectors, including AI, IoT, quantum computing, advanced automotive systems, and industrial automation.

The **lack of targeted support for the design segment** remains a significant challenge, particularly given Europe's relatively limited design capabilities compared to global leaders. Nonetheless, Europe maintains a strong industrial base that could bolster sovereign design capabilities. World-class RTOs such as **IMEC**, **CEA-Leti**, and **Fraunhofer** provide advanced design infrastructure and expertise. On the industrial side, **ARM** leads in processor architecture

and IP licensing, while **Siemens EDA** delivers software for designing complex integrated circuits and systems-on-chip (SoCs), supporting applications from automotive electronics and industrial automation to AI and data centres. Coordinated investments and shared infrastructure connecting design companies, research institutes, and semiconductor manufacturers could fully leverage these capabilities.

In this context, the Chips Act offers specific policy support (Art. 17) for the design segment by encouraging Member States to support facilities awarded the "Design Centre of Excellence" label by the European Commission. Yet, no facilities have received the label, and the Delegated Act outlining the application procedure and criteria has not been published. This legal uncertainty discourages companies from applying and Member States from granting state aid, effectively stalling investments in the critical design segment of the semiconductor supply chain.

2.2.2.1.3. Semiconductor Equipment

Although semiconductor equipment is falling under the framework of the Chips Act, there has been a **considerable lack of investment and public support** for this segment. This is linked to the fact that the very definition strictly covers equipment that is "utilised in semiconductor manufacturing," thereby reducing the scope of technologies that could be supported under Pillar II. One could argue that semiconductor equipment is implicitly covered under the FOAK definition; however, **this lack of clarity undermines the legal certainty companies require** to plan multi-billion-euro investment projects, which risk being halted at the administrative level due to regulatory ambiguity.

The European semiconductor manufacturing equipment ecosystem retains excellence at the global level, demonstrated by a number of highly active EU and non-EU companies. **ASML** (Netherlands) dominates lithography equipment, crucially including extreme ultraviolet (EUV) systems, while **ASM International** (Netherlands) and **Aixtron** (Germany) provide deposition technologies (ALD and CVD). **Trumpf** (Germany), a world leader in machine tool production, delivers high-power lasers for micromachining and various lithography applications. Complementing these European players, non-EU companies including Applied Materials, **LAM Research** and **Tokyo Electron** operate production, service, and R&D facilities in Europe.

Europe's semiconductor manufacturing equipment ecosystem, anchored by the aforementioned industry leaders, is strategically vital, as its advanced lithography, deposition, and precision tools are indispensable for chip production worldwide. Strengthening the **equipment ecosystem will enhance Europe's position in the semiconductor value chain**, sustain long-term technological sovereignty and competitiveness, and ultimately make it less vulnerable to global supply disruptions. Beyond core semiconductor manufacturing equipment, the semiconductor industry vitally depends on metrology and inspection systems, test and packaging equipment (Ex. Wafer probers and die bonders), and process control tools (Ex. Vacuum pumps and gas delivery systems). These equipment types are strategic enablers of semiconductor manufacturing, since they underpin yield optimisation, reliability assurance and process stability, where Europe remains highly dependent on non-EU suppliers particularly from the US and Japan.

2.2.2.1.4. Materials

Besides semiconductor equipment, a wide range of materials, such as specialty gases, photoresists and polysilicon, used across the front-end and back-end of the supply chain are

entirely excluded from the FOAK criteria and the scope of Pillar II. These materials are fundamental building blocks of semiconductor manufacturing:

- **Photoresists** are light-sensitive materials that define circuit patterns during lithography, directly impacting feature resolution and yield, including chemically amplified resists for EUV or DUV processes and thick-film resists for MEMS applications.
- **Specialty gases** (Ex. Silane, ammonia, nitrogen trifluoride) are essential for deposition, etching, and doping processes, enabling precise control over layer composition and electrical properties.
- **Polysilicon** serves as a key conductor in transistors and gate structures, providing the high-purity foundation required for wafer manufacturing.

Europe hosts several key producers and suppliers of these critical materials, including both EU and non-EU companies, which are indispensable for building the continent's chip and wafer production capacities. In specialty gases, leading firms such as **Air Liquide** (France), **Messer Group**, and **Linde** (Germany) supply ultra-high-purity gases vital for deposition and etching processes. For photoresists and lithography chemicals, **Merck KGaA** (Germany) and **Syensqo** (Belgium) provide advanced resists, developers, and specialty electronic materials for next-generation lithography, complemented by non-EU companies like **JSR** and **Fujifilm Electronic Materials**, which maintain production and R&D facilities in Europe. In polysilicon production, **Wacker Chemie** (Germany) remains the world's dominant manufacturer of semiconductor-grade polysilicon, representing a strategic asset for the European ecosystem.

Supporting Europe's capabilities to produce these critical materials is essential to ensure competitiveness and supply chain resilience. These materials are indispensable for high-yield, high-performance chip and wafer production, and any disruption in their supply could halt fabrication entirely, regardless of advances in equipment or design capabilities.

2.2.2.1.5. Components

Complementing Europe's critical capabilities in equipment and materials, a range of EU and non-EU companies produce the **key components that enable semiconductor manufacturing equipment to operate** efficiently. These suppliers provide specialised tools, optical components, photomasks, and precision machinery that are essential for chip production across various technology nodes. Their contributions underpin the long-term strength, resilience, and technological independence of Europe's semiconductor ecosystem. Despite their strategic importance, these companies are currently excluded from the FOAK criteria and the scope of Pillar II, meaning they cannot receive direct public support under the current Chips Act framework.

Notable examples include **Carl Zeiss SMT (Germany)**, a leading provider of high-precision and unique lenses and optical systems critical for ASML's lithography machines and the global industry. **SÜSS MicroTec (Germany)** supplies photomask aligners and related equipment for both R&D and high-volume production, while **Tekscend Photomask** operates significant facilities in Europe, including Dresden and Corbeil-Essonnes, supporting advanced photomask production.

Looking ahead, a future Chips Act framework should prioritise nurturing this network of equipment component providers, including smaller companies, to strengthen Europe's semiconductor ecosystem. Supporting these actors will be crucial to maintain technological sovereignty, foster innovation, and ensure supply chain resilience in critical segments, reducing reliance on non-EU suppliers and safeguarding the continent's ability to produce next-generation chips.

2.2.3. Chips Act 2.0: Building a European Ecosystem

Pillar II of the Chips Act exclusively authorises state aid provision for FOAK facilities, meaning "new or substantially upgraded semiconductor manufacturing facilities providing a dimension of innovation not yet present in the EU"[13]. This approach was coherently and appropriately designed to support the emergence of cutting-edge semiconductor technologies and to contribute towards building new manufacturing capabilities in Europe. There is, however, a need for an **expanded strategic outlook** that focuses not only on attracting new technologies, particularly in the leading-edge chips, but also supports the growth of strategically relevant segments of the value chain in Europe.

The focus of Pillar II was not designed to support existing European industrial capacities, and did not aim to secure segments of the supply chain where Europe already has capacity. Although supporting leading-edge technologies is important to compete globally, a **lack of emphasis towards the consolidation of existing capacities** may endanger Europe's position in the medium- and long-term. Supporting European industry indeed requires securing and strengthening existing capacities for legacy chips, as well as for R&D activities, design, equipment and materials production, which can strengthen the overall semiconductor ecosystem.

Pillar II of the European Chips Act provides incentives to investments in two ways. First, it provides the criteria to recognise a facility project as eligible to receiving state aid. While the state aid provided to semiconductor companies relies on Article 107(3) of the of the Treaty on the Functioning of the European Union ('TFEU'), the validation of this aid by the Commission strongly considers the "First-Of-A-Kind" dimension of the project[14]. Second, it "entitles undertakings to a streamlined approach to administrative applications and a priority access to the pilot lines"[15] to facilities recognised as "Integrated Production Facility" (IPF) or "Open EU Foundry" (OEF). To guarantee the legal coherence of the FOAK with the IPF and OEF, and with Chapter III of the Chips Act in general, their definitions and scope are fully aligned in the Act. Hence, any amendment to one of these definitions must be reflected in the other definitions.

One way to best guarantee this coherence of the text is to directly insert the missing segments of the supply chain (i.e. private R&D, design, materials, component and equipment suppliers) in the definitions of the IPF (Article 13) and OEF (Article 14). However, these two types of facilities were established to reflect the two common business models of semiconductor manufacturing

[13] European Commission, European Chips Act: Security of supply and resilience | Shaping Europe's digital future
[14] Communication (C/2024/4911) on the Guidance on the application for an undertaking to obtain the status of integrated production facility and open EU foundry. URL: https://eur-lex.europa.eu/legal-content/EN/TXT/PDF/?uri=OJ:C_202404911
[15] European Chips Act: Security of supply and resilience. URL

facilities (i.e. Integrated Device Manufacturers and Foundries) and are quite specific in scope[16]. This might require a more flexible approach via the creation of **new categories evolving next to the IPF and OEF** under Chapter III of the Act. These categories could be delimited as follow:

- **Research and Development Centre of Excellence:** Private R&D centres contributing to the upgrade of existing semiconductor-related facilities' production and the development of new production solutions and systems, and the emergence of new and future cutting-edge technologies.
- **Design Centre of Excellence**: Revision of Article 17 establishing a "Design Centre of Excellence" label based on the same criteria of IPF and OEF to simplify the framework.
- **Critical Supply Chain Facility**: Suppliers of critical materials (Ex. Gases, chemicals, raw and critical materials, raw wafers), components (Ex. Photomasks, high-precision lenses and optical systems) and semiconductor-related equipment (Ex. Metrology and inspection systems, test and packaging and process control).

SEMI Europe Recommendations – Pillar II and FOAK (Enabling Cross-Segment Investments)

Policy recommendation 9: Widen the scope of the FOAK definition to include the whole semiconductor supply chain, from private R&D, chip design and design tools, to the supply of materials (gases, chemicals, raw and critical materials), components and semiconductor-related equipment (Ex. Metrology and inspection systems, test and packaging and process control), avoiding any additional administrative burden for companies.

Policy recommendation 10: Amend Chapter III of the Chips Act to include other critical supply chain segments for semiconductor manufacturing, including private R&D, chip design and design tools, materials (Ex. Gases, chemicals, raw and critical materials), components (Ex. Photomasks, high-precision lenses and optical systems, raw wafers) and semiconductor-related equipment (Ex. Metrology and inspection systems, test and packaging and process control).

2.2.4. Centralising and Fast-Tracking Pillar II Processes

The processes required for the verification and attribution of the First-of-a-Kind (FOAK), Integrated Production Facility (IPF) and Open EU Foundry (OEF) certification have often put significant time and resource constraints on companies. This challenge has highlighted a tension between guaranteeing swift procedures for companies, while safeguarding the Single Market and the EU competition framework. To receive authorisation from the European Commission on the provision of state aid, the concerned facility project must be acknowledged as a First-Of-A-Kind (FOAL) facility. Hence, the FOAK label is a prerequisite for companies to receive state aid from EU Member States, granted by the European Commission's Directorate-General for Competition (DG COMP). The IPF and OEF labels are granted by the Directorate-General for Communications Networks, Content and Technology (DG CONNECT) based, notably but not exclusively, on the FOAK nature of the project. While those labels give access to different set of benefits, they

[16] Communication (C/2024/4911). URL

overlap significantly in their attribution processes and criteria. In addition to these procedures at the EU level, companies are subject to overlapping resource-intensive and time-intensive national processes for projects' authorisation.

2.2.4.1. Multi-Level Administrative Challenges for FOAK Investments

The processes to submit dossiers to DG CONNECT and DG COMP for the respective IPF/OEF and FOAK labels remain decoupled, even though their requirements are strongly similar. Administratively, this forces companies to prepare and submit two **separate, but largely overlapping, proposals** to the two Directorates. On average, the application, processing, and validation of these dossiers at the **EU level takes 9–12 months**. Once the FOAK label is granted, additional months are required to finalise agreements between companies investing in Europe and the Member State providing state aid. By comparison, grant validation and related administrative processes for semiconductor investments take just **5–6 months in the U.S., 6 months in China, and less than a month in South Korea and Taiwan**.

European and non-European companies looking to invest in Europe must navigate a layered set of administrative requirements at national and EU levels. Delays in obtaining FOAK validation and state aid approvals add to often lengthy national negotiations, permitting processes, and other administrative steps, all of which are **complex, repetitive, and resource-intensive**. In addition, national co-funding is often being delayed or withdrawn due to national budget constraints, bringing further constraint at both the EU and national levels. **Coherent implementation** at both EU and national levels to minimise the risk of cancellations by Member States, delays, or inconsistencies in national funding programs must be achieved to reduce uncertainties for FOAK beneficiaries.

Many companies applying for FOAK state aid simultaneously pursue investment plans in other regions of the world, which can come into direct competition with the European projects. In these cases, countries that can grant permits and finalise approval processes more quickly are prioritised, often at the expense of European investments. These **cumulative delays** directly affect the operationalisation of facilities and the commercialisation of new technologies, potentially leading to lower or unplanned losses of market share.

2.2.4.2. Guaranteeing Competition Rules and Facilitating Semiconductor Investments

One important factor contributing to this delay lies in the time and resources that companies must allocate to respond to the inquiries of the European Commission, with regards to their application dossier and technical specificities of the projects.

The number of questions from the Commission has ranged from 50 up to 100. The nature and scope of these questions have often influenced the validation timeline of FOAK projects. While questions have reportedly been repetitive and sometimes not specific, and not applicable, to the semiconductor industry, others have touched upon highly sensitive competitive information where possible leak of information was a very high concern for foreign and EU companies.

SEMI Europe fully acknowledges that this process is an unavoidable condition to safeguard the EU's competition rules, its internal market and the level playing field for all companies operating in Europe. A **right balance** can be found to maintain the European acquis and simplify the abovementioned procedures, by streamlining FOAK and IPF/OEF processes and making them more industry-specific. This harmonisation and simplification must be achieved in collaboration with the semiconductor ecosystem, both at the horizontal level within the European Commission and the vertical level with EU Member States, to streamline dialogue and overlapping processes between national governments and EU authorities.

SEMI Europe Recommendations – Pillar II and FOAK (Simplification)

Policy recommendation 11: Establish a single point of contact (one-stop-shop) within the European Commission to receive and horizontally dispatch required information to the different services of the European Commission, ensuring coordination with the Member States via the European Semiconductor Board (ESB).

Policy recommendation 12: Recommend Member States to establish a single point of contact in charge of coordinating sub-national and national services involved in semiconductor investment projects and guaranteeing vertical communication and coordination with EU authorities via the European Semiconductor Board (ESB).

Policy recommendation 13: Harmonise administrative processes and information requirements between DG Connect and DG COMP for the approval of the Integrated Production Facility/Open EU Foundry status and the First-of-a-Kind status, with a strictly defined timeline for the processing of the respective applications.

Policy recommendation 14: Harmonise Member States' permitting processes to provide a clearer administrative picture of the investment processes and opportunities across the Union.

2.3. Workforce Development

2.3.1. Addressing the issue

The European semiconductor industry is facing a significant labour shortage. While the current workforce is approximately 382,000 employees (of which 49% are employed in integrated device manufacturers, IDMs), it is expected to grow by 156,000 new positions, reaching nearly 540,000 workers by 2030. Taking into account factors such as investment scale and retirement rates, overall employment growth in the sector is projected at around 4.5% by 2030. However, the rapid increase in job openings is outpacing the supply of graduates, further exacerbating the gap over time. According to the ECSA Skills Strategy 2025[17], the European Union is expected to face a shortage of more than 65,000 skilled professionals by that time.

The **industry's core workforce is highly technical**, with hardware engineers, technicians, software engineers, and data specialists comprising roughly 75% of all roles and, indeed, the

[17] Skills Strategy 2025, European Chips Skills Academy. URL: https://chipsacademy.eu/wp-content/uploads/2025/11/2025-ECSA-Skills-Strategy-final.pdf

majority of the projected talent gap. Over the past five years, shortages have become particularly critical in three profiles: data specialists, system designers, and analog designers. The rapid development of artificial intelligence is also expected to drive high demand for machine learning engineers and related skills profiles. By 2030, the most critical talent gaps are projected to include hardware engineers (40,000 positions), technicians (23,500 positions), and software engineers / data specialists (11,000 positions).

On the academic side, the EU ranks third globally[18] in terms of Science, Technology, Engineering, and Mathematics (STEM) graduates, producing 1.2 million STEM graduates in 2022. However, only 28% of STEM students graduate in the semiconductor-related domains (electrical engineering, physics, and so on); and less than 18,000 of those graduates entered the EU semiconductor industry. Already today, employers report difficulty in finding skilled talent, which is exacerbated by the stagnating rate of new graduates as well as the ambition and investment stemming from the EU Chips Act. There is a clear need to comprehensively fix the 'leaky pipeline' by increasing the **attractiveness and awareness of career opportunities** for young students, strengthening collaboration between industry and education, and improving lifelong learning opportunities to ensure professionals can grow in their roles as technology evolves.

The extent of the skills shortage varies across Member States and is closely linked to the semiconductor investment patterns across the EU. Countries with advanced semiconductor infrastructure, such as Germany, Belgium, the Netherlands, are experiencing growing demand for skilled workers. On the other hand, countries such as Spain, Romania, Greece, Croatia and Bulgaria report a surplus of electrical engineering graduates relative to the size of their national semiconductor ecosystems. Strengthening **cross-border collaboration** between Member States is essential to ensure employers can tap into a pool of skill talent regardless of location and mitigate the risks associated with failed or withdrawn investments from the European market.

2.3.1.1. Structural Challenges

Several structural challenges underpin the current skills and workforce challenges. These include a lack of specialised higher education and vocational training, limited training opportunities and support for teachers, and failure to structurally anticipate and proactively address increasingly critical job profiles. Many small-scale initiatives at local, national, and even European level try to address these shortcomings, but without a **defined coordinating body** it is impossible for these activities to make a large impact and easy to duplicate efforts or miss opportunities to unite and scale.

The European Chips Act elevates the issue by explicitly defining as one of its priorities the need to "address the skills shortage, attract new talent and support the emergence of a skilled workforce."[19] . To this end, the Act has established a framework of projects and partnerships dedicated to addressing the talent gap and strengthening the skills pipeline across the semiconductor ecosystem. These initiatives are primarily financed through the Chips Joint Undertaking, with additional support provided by Horizon Europe and the Digital Europe

[18] Behind China and India, but above the US.
[19] Chips Act (2023/1781). URL

Programme. However, these initiatives have largely operated in silo, all but missing out on synergies with projects funded through other instruments such as Erasmus+ with identical or complementary goals.

The European Semiconductor Board (ESB was) introduced to govern the Chips Act, comprising representatives of the Member States and chaired by the Commission, and providing advice, assistance and recommendations across the three action pillars. The ESB is connected to only one DG (CNECT), and it derives its authority from the important Chips Act and the CHIPS JU. So far, the ESB is composed of representatives of the EC and the public authorities – i.e. without representatives from the education field, nor from industry – and any steering on skills and workforce is currently missing. Building on this, the Industrial Alliance on Processors and Semiconductor Technologies was established supported by the ALLPROS project to operationalise work across three topics: PFAS, Supply Chain, and Skills. These working groups ostensibly report directly to the ESB, however, particularly in the case of the Skills working group, the lack of representatives from industry and education have made it difficult for the ESB to function as a supervisory body on this topic.

2.3.1.2. Implementation State of Play

2.3.1.2.1. Early Education, University, and Technical Training

While the imminent talent shortages demand urgency, a **long-term vision** is required to ensure sustained access to skilled professionals as the industry grows. This means also taking steps to better incorporate technology and engineering skills already in primary and secondary school curriculum. Effective strategies to implement STEM education in schools involve: (i) stimulating an interdisciplinary approach which involve breaking down the silos between the various STEM components, and mimicking real-world scenarios; (ii) providing teachers with continuous training in STEM for schools, offer them content knowledge, and train them to implement technology in their subjects; (iii) setting up dedicated spaces or labs to encourage designing, developing prototypes, and creating innovative products (possible in partnership with local companies); (iv) setting up STEM clubs aimed at supporting students groups to foster passion and explore beyond the classroom.

One of the few initiatives addressing this gap and which could be replicated is the **STEM Teacher Internship Program in Ireland**, developed in collaboration with Intel and other partners, which offers paid placements for primary and secondary school teachers in technology and microelectronics companies[20]. These internships provide teachers with hands-on experience in real STEM environments and equip them with necessary skills and industry knowledge to inspire students and bring gained insights into classrooms. To date, more than 300 teachers have completed internships across 70 companies, with an estimated impact on over one million students[21]. Scaling similar initiatives at the European level could strengthen early STEM engagement and support a strong foundation for later high-tech careers.

In this respect, the EU STEM Coalition should also be noted as an important partner. This is the EU's main network of 35 national/regional STEM platforms, European members, and national (associate) members. The Coalition started its activities in 2015 and covers a large range of

[20] https://stemteacherinternships.ie
[21] STInt launches tenth year of education-industry partnerships | Dublin City University

activities, which also include chip technology. In principle the "golden triangle" of stakeholders consisting of Schools + Industry + Ministries of Education are necessary to be successful in promoting STEM education

In order to motivate students with the right qualifications to actually embark on STEM studies, the image of the semiconductor industry as an attractive job environment needs to be boosted through communication campaigns (i) addressing the general public and the students; and (ii) driven/supported by the companies and research institutes.

Apprenticeships are a cornerstone of vocational education and training (VET) systems across Europe. They combine company-based training with school-based education, and lead to a nationally recognised qualification when completed. Member states across Europe, notably Germany, have long recognised the value of apprenticeships, as the work-study combination is an excellent preparation for the subsequent work environment. However, the apprenticeship programme strategy in Europe faces several challenges, including (i) scalability issues for SMEs that lack resources to develop comprehensive programmes, and (ii) the need for continuous curriculum updates to keep pace with evolving industry standards, particularly in high-tech sectors.

2.3.1.2.2. Lifelong Learning

Companies will have to cut through the complexities of up- and reskilling workers. Available programs often focus on back-office workers, neglecting the critical need for skilled fab workers where the shortage is more severe. Recent research has pointed out that while 74% of manufacturers are looking at upskilling existing workers as a strategy to address labour shortages, 67% of manufacturing workers are not satisfied with the existing training programs[22].

Educators agree that the most effective learning strategy is person**alised and contextualised to the needs of the learner and the environment** where the learning will be applied. In 2022 the Council of the EU adopted a recommendation on micro-credentials advocating their development, implementation and recognition across institutions, businesses, sectors and borders. Industry recognised micro-credentials offer a model by which companies and training providers can offer targeted re-skilling and upskilling programs to address emerging skills demands.

2.3.1.2.3. Regional Ecosystem Programs

As workforce needs are concentrated in regional "talent ecosystems", the local regions have a pressing need - hence a crucial commensurate role - to develop the talent and workforce. The Brainport Eindhoven region is an excellent example in this respect: the region has been coming up against limits in terms of personnel, space and energy. The Dutch central and regional governments have made agreements aimed at addressing the problems in the Dutch semiconductor sector. Through the **"Project Beethoven"**, the authorities have worked out a substantial package amounting to €2.5 billion involving measures for education and infrastructure for the sector.[i] The package includes investment in vocational and professional talent, and in sufficient space, good accessibility and affordable housing in the Brainport area. As part of this package, the government will be making additional investments in talent

[22] Accenture, "*Bridging the gap – Navigating the talent shortage in the semiconductor industry*", 2025, https://www.accenture.com/content/dam/accenture/final/accenture-com/document-4/Bridging-Talent-Gap-...

development amounting to €450 million to the end of 2030 (of which €275 million go to Brainport) and €80 million annually thereafter. The TU Eindhoven will contribute considerably to the Project, establishing 140+ additional scientific staff positions, 15 new MSc tracks, new semiconductor labs and a new clean room. Through effective recruitment campaigns and scholarships TU Eindhoven anticipates growing the student enrolment by 1900 in 2300, leading to 900+ graduates annually from 2030 onwards.

Pilot projects to demonstrate solutions to specific issues related to the workforce often (i) have somewhat opportunistically-composed project teams with participants from across Europe; and (ii) in view of the restricted funding will inevitably have a limited scope. If judged successful upon completion the project team will compete for scale-up or - at best - continuation funding. But such an approach will not be sufficient to meet the complex, tenacious and urgent challenges which the semiconductor sector has faced across Europe in terms of workforce development. The Project Beethoven is a "lighthouse" project that deserves to be replicated in regions with a similar semiconductor "talent ecosystem" with high growth needs such as Saxony, Crolles, Catania, Northern Italy, Ireland.

2.3.2. Looking Ahead

One of the aims of the network of competence centres, established under the Chips Act by Chips Joint Undertaking (Chips JU), is to '*address the knowledge and skills shortage and mismatch by attracting, mobilizing and retaining new talent on research, design and production and supporting the emergence of a suitably skilled workforce in STEM*'[23].

The European network of Chips Competence Centres (aCCCess) brings together around 30 competence centres, in close coordination with Chips Pilot Lines, and the Design platform. Among its five thematic focus groups, the Training and Skills Development groups is tasked with mapping available training opportunities, creating and promoting a European training catalogue and facilitating SMEs access to relevant education and training offers.

Each national competence centre acts as a "one-stop shop", a unique connection point between companies, research institutions and academia. They accumulate resources for semiconductor development, provide companies with access to technical knowledge and training such as hands-on training for professionals, orientation activities for young talent, and reskilling and upskilling initiatives for the existing workforce.

While the national Chip Competence Centres already cooperate within a common network, coordination of joint activities remains complex. Theres is a clear **need for harmonised curricula and standardised micro-credential system** to ensure mutual recognition of training across borders. The idea of developing a pan-European educational programme in collaboration with the aCCCess network may seem promising; however, it would require substantial additional resources and staffing to be implemented effectively.

Within the framework of the NanoIC pilot line project, a skills-related workstream addresses workforce development, with a focus on (i) bridging the gap between academic knowledge and industrial needs; and (ii) growing the cohort of experts with an industry mindset. Research centres Imec and Tyndall offer (i) internships and dual-learning programs for students from

[23] Chips Act (2023/1781), article 5(d) and article 4(d). URL

regular curricula at Master's and PhD level; and (ii) expert courses and bootcamps for faculty on beyond-2nm advanced semiconductor technologies. These offerings will be supported and expanded through cooperation with the Chip Competence Centres

By establishing national Chip Competence Centres and **aligning their activities at the European level**, the EU can potentially address growing skills shortages and surpluses within the EU by creating a more balanced semiconductor talent pipeline across regions. This way, the Chip Competence Centres will have a central role in implementing the Act's skills and workforce development agenda.

2.3.2.1. Paving the Way for a Skilled European Semiconductor Workforce

Addressing the semiconductor talent shortage across the value chain has become a matter of strategic importance, if Europe wants to regain and defend its competitive position. The skills gap has been widening over many years and in spite of a plethora of laudable initiatives – at regional, national and European level – the general impression is that – even against the background of the industry's uncertainty and volatility – the problem has remained excruciatingly constant and - if anything - is becoming more pressing.

Most if not all current or planned workforce initiatives make a valuable contribution to at least one aspect of growing the semiconductor workers' pipeline. But a **coordinating body** with sufficiently large authority, outlining an *integrated* approach and setting clear KPIs for the various action lines is missing. The number of additional workers or students on the "demand side" should be quantified clearly and set along a specific timeline. The actions on the "supply side" (undertaken or being planned) should be classified according to a timeline (short-term, medium-term or long-term effect); to resources required (budget, staff, infrastructure); and to impact (Ex. number of additional students registered; number of workers reskilled or hired).

According to these challenges, SEMI Europe has determined three sets of recommendations below, which aim to provide a coherent strategy for semiconductor skills development in Europe. The three sets of recommendations are complementary and provide an EU-wide framework to harmonise efforts to tackle skills shortages at different governance levels.

2.3.2.1.1. A new Chips Skills Academy Umbrella Organisation

Under the Chips Act 2.0., the European Commission must suggest ***creating a fully realised Chips Skills Academy umbrella organisation***, that is endorsed under the Chips Act 2 and recognised by all relevant stakeholders, including the Chips Competence Centres. The Academy shall coordinate joint initiatives and efforts aimed at bridging the skills gap in the semiconductor industry and carefully consider the following points:

- Use the earmarked 'digital skills academies' call under Digital Europe to build on existing initiatives and to ensure the coordinating nature of the Academy.
- The Academy should install a permanent Chips Skills Observatory at EU level. The observatory should provide regular updates on the skills needs across the EU – broken down to regional level and monitor KPIs towards progress.
- In its governance structure the Academy should comprise of a high-level body dedicated to semiconductor skills and workforce development. This board should integrate and upgrade all existing structures, such as the Pact for Skills Executive Board, the Skills working group of the industrial Alliance or the Board of the ESCA project.

- Ensure that the Academy is closely linked to the national chips competence centres. The Academy should provide services to the competence centres to facilitate their efforts on skills - such as certification, summer schools and materials for image campaigns. At the same time the competence centres as well as the other initiatives funded by the Chips JU or the Microelectronics IPCEI should contribute to the Academy. To strengthen the role of Chips Competence Centres in delivering targeted training programs and outreach initiatives. They should be further empowered to act as regional and national semiconductor knowledge hubs, as well as coordinate with education and industry to create and distribute specialised training.

2.3.2.1.2. A European Chips Education Roadmap

The European governance structure of the Chips Act does not fully reflect skills needs of the industry. Neither the Chips JU nor the European Semiconductor Board currently address skills with dedicated structures or strategic processes or roadmaps. Within the realm of the Chips Skills Academy, industry, academia and government agencies should co-develop and regularly update a chips education roadmap. This roadmap should provide a longer-term guidance for upcoming European calls, initiatives as well as recommend national and regional actions. In order to ensure a comprehensive, future-proof strategy, the roadmap should consider at least the following intervention points along the semiconductor talent pipeline:

- **Growing the STEM talent pool**, targeting young people in primary and secondary school. Sustained intervention in this area is essential for safeguarding the long-term talent pipeline as these efforts will come to fruition only 10 to 15 years after implementation. Failure to address systemic challenges in STEM education from an early age will ultimately limit the prospective recruitment pool as the growth of graduates in semiconductor related disciplines is stagnating as well as overall population growth. On the one hand this can mean direct involvement of industry in schools, however initiatives which can support current and future teachers will act as multipliers for the next generation.

- **Encouraging the student-population** (university and higher technical education) **towards semiconductor-related degree paths and industry careers.** Building on a strong STEM talent pool, the industry must continue to ensure access and visibility of attractive career opportunities. Many projects currently active on this topic pay particular attention to this subset of the talent pipeline as results can be realised in a relatively short period of time. Data on the shocking lack of graduates with relevant degrees who ultimately do *not* find their way into the semiconductor industry speaks to the need to improve the image of the sector and the mechanisms by which new graduates and young professionals develop their careers. For example, this includes better career guidance at university level – if professors and counsellors are unaware of the opportunities it is difficult to expect students to find them wholly on their own – or summer schools / boot camps and similar activities which offer a low barrier to entry for students and introduce them to a wide spectrum of paths. Vocational education should also receive particular attention to harmonise quality standards across Member States and increase the appeal of VET programs by creating financial and social incentives such as scholarships, housing grants, and language support.

- **Expanding available talent sources and retaining current workforce.** It is imperative to make targeted interventions to triage the most pressing workforce needs. Actions which can

manifest concrete results within a relatively short time horizon (1-5 years) include streamlining visa procedures for job profiles in critical demands and investing in training programs which target transferable skills in adjacent industries who can be effectively re-trained for semiconductor careers. The industry can also benefit enormously from tapping into unrecognised or underrepresented populations, for example liberalising hiring processes to include non-traditional educational backgrounds with relevant skills. Finally, upskilling those currently active in the sector is a meaningful way to ensure the workforce adapts to technological changes and can enable productivity increases. Recent research has pointed out that while 74% of manufacturers are looking at upskilling existing workers as a strategy to address labour shortages, 67% of manufacturing workers are not satisfied with the existing training programs[24].

2.3.2.1.3. National Education Roadmaps

Under a Chips Act 2 strategy the European Commission should strongly ***encourage the member states to establish education roadmaps as part of national chips strategies***. The various Ministries of Education throughout Europe should commit to contributing to the Academy and the Skills Observatory providing, on a regular basis, data for the student population in secondary, higher and adult education. The national education roadmaps should show clear links to the Chips Academy and other European initiatives. At the regional level, it is strongly advised that all stakeholders allocate sufficient resources to workforce development efforts, including the monitoring of supply and demand, in the areas that benefit from Chips Act funding. New investments necessarily will bring future workforce demands which are important to account for in tandem with any infrastructure development.

- To effectively implement the European Semiconductor Skills Strategy, ensuring Member States adoption of coherent national roadmaps or actions plans that reflect the alignment of common priorities. It may include but is not limited to integrating semiconductor-related skills into curricula at all educational levels, from as early as secondary and elementary school to higher education and vocational training, as well as expanding and aligning funding streams, and common monitoring of progress on the implementation of the strategy.
- At the regional level, it is strongly advised that all stakeholders allocate sufficient resources to workforce development efforts, including the monitoring of supply and demand, in the areas that benefit from Chips Act funding. New investments necessarily will bring future workforce demands which are important to account for in tandem with any infrastructure development.
- Encourage Member States to implement a common accreditation and recognition system for semiconductor education (covering university and VET degrees, as well as micro-credentials). A harmonised accreditation framework would improve transparency of skills and facilitate inter- and cross-border mobility.

[24] Accenture, “Bridging the gap – Navigating the talent shortage in the semiconductor industry”, 2025. URL: https://www.accenture.com/content/dam/accenture/final/accenture-com/document-4/Bridging-Talent-Gap-in-The-Semiconductor-Industry-Final.pdf#zoom=50

- There has been a continuing expansion of tertiary education over the last decade across the EU. In 2023 the tertiary educational attainment rate of 25-34-year-olds was 43.1% and the EU-level 2030 target for that share is at least 45%[25]. Tertiary educational attainment varies a lot within countries, with regional differences pronounced (higher in more developed regions than in less developed ones). This creates imbalances in the availability of highly qualified people across regions, undermining economic, social, and territorial cohesion. Similarly, having a tertiary degree is less common in rural areas (31.7%) than in cities (53.3%).

SEMI Europe Recommendations – Workforce Development

Policy recommendation 15: Create a fully realised Chips Skills Academy umbrella organisation, that is endorsed under the Chips Act 2 and recognised by all relevant stakeholders, including the Chips Competence Centres. The Academy shall coordinate joint initiatives and efforts aimed at bridging the skills gap in the semiconductor industry.

Policy recommendation 16: The Chips Skills Academy, industry, academia and government agencies must co-develop and regularly update a chips education roadmap that provides a longer-term guidance for upcoming European calls, initiatives as well as recommend national and regional actions.

Policy recommendation 17: Recommend the Member States to establish education roadmaps as part of national chips strategies and commit to contributing to the Academy and the Skills Observatory providing, on a regular basis, data for the student population in secondary, higher and adult education.

2.4. Pillar III - Coordination and Crisis Management

Pillar III of the European Chips Act establishes a comprehensive policy framework for monitoring semiconductor production capacities and implementing crisis response measures in the event of actual or potential supply disruptions within the Union. Under this framework, the European Commission and Member States, acting through the European Semiconductor Board (ESB), may activate a *crisis stage* when necessary. Once activated, the Commission is empowered to: 1) request companies to share information about their operations; 2) require them to prioritise orders for crisis-relevant products (priority-rated orders); and 3) conduct joint procurement on behalf of several Member States for critical semiconductor products needed by essential sectors. To further strengthen the EU's crisis preparedness and response, Pillar III also introduces a strategic mapping mechanism designed to closely monitor the semiconductor value chain across Europe.

Since the adoption of the Chips Act in 2023, the European Union has not faced any semiconductor shortages severe enough to endanger its local ecosystem. Consequently, the crisis stage and its related response measures have not yet been activated, and their efficiency and effectiveness remain untested. Nonetheless, the European Commission has made **steady**

[25] Government of the Netherlands, 2024. URL: https://www.government.nl/latest/news/2024/03/28/the-netherlands-to-invest-€2.5-billion-to-strengthen-business-climate-for-chip-industry-in-brainport-eindhoven

progress in establishing its strategic mapping and monitoring system, including the development of early warning indicators. This system will be instrumental in enabling Europe to swiftly identify and respond to emerging risks in the global semiconductor supply chain, allowing policymakers and industry stakeholders to take proactive and well-coordinated risk management measures.

2.4.1. An Optimised Public-Private Monitoring Collaboration

The strategic mapping of the semiconductor industry aims to identify Europe's main strengths and weaknesses within the global semiconductor value chain, highlight key market actors, and assess potential risks to the resilience of the European semiconductor ecosystem. To achieve this, the European Commission is collaborating with private partners – including the semiconductor industry through the Industrial Alliance on Processors and Semiconductor Technologies – as well as with external experts. This collaboration must ensure an efficient and well-balanced allocation of resources to effectively deliver on Pillar III objectives.

Within this framework, the Alliance's Working Group on Supply Chain (SCWG) has been entrusted by the Commission and the European Semiconductor Board (ESB) with developing monitoring and mapping tools, along with related guidance. The SCWG is currently working on the creation of a *Digital Twin* that will mirror and map the current structure and latest developments of Europe's semiconductor ecosystem. To guarantee acce**ss to accurate and up-to-date information**, a dedicated survey group has been established to build and maintain a comprehensive database of Europe's semiconductor capacities across all segments of the value chain. This database will form the foundation for future periodic and continuous stress tests assessing vulnerabilities and dependencies within the EU supply chain, thereby directly contributing to the objectives of Pillar III.

In parallel, the European Commission has internally operationalised its *Supply Chain Alert Notification* (SCAN) System — an indicator-based mechanism designed to monitor market dynamics and supply chain developments. SCAN enables the tracking of trade flows for sensitive and critical items, such as semiconductors. The Commission's Joint Research Centre (JRC) has notably published a working paper demonstrating the application of the SCAN methodology to the semiconductor supply chain. However, the system remains restricted to internal use within the Commission and is currently inaccessible to external stakeholders, despite its potential value for identifying strategic bottlenecks and monitoring the semiconductor value chain. The ongoing collaboration between the European Commission, the Industrial Alliance, and private experts should therefore continue in a manner that ensures a **coherent and efficient allocation of resources,** supporting the delivery of a comprehensive and adaptable monitoring system.

SEMI Europe Recommendations – Pillar III and Supply Chain Monitoring

Policy recommendation 18: Develop a coordinated, adequately resourced semiconductor monitoring and mapping framework under Pillar III of the Chips Act, strengthening collaboration between the European Commission, the Industrial Alliance and private, and building on existing instruments (Ex. SCAN System).

Section 3 – Enhanced Policy Toolbox for Europe's Global Competitiveness

This section presents an overview of key policy instruments and strategic initiatives that are potentially relevant for Europe's semiconductor ecosystem, highlighting their objectives, benefits, and lessons from international case studies. Starting from an examination of tax credits, exploring their design, eligibility, and effectiveness in promoting investment and R&D activities, particularly for large companies, SMEs, and start-ups. The section then addresses the specific needs of smaller actors in the semiconductor sector, presenting tailored measures to improve access to pilot lines, reduce financial and administrative barriers, and foster inclusive growth and innovation.

Furthermore, the section reviews prominent international approaches, including **Japan's Rapidus consortium, the U.S. CHIPS and Science Act, and South Korea's K-Chips Act**, illustrating how public-private collaboration, strategic subsidies, and targeted incentives can accelerate R&D, manufacturing, and technological leadership. These case studies provide insights for the **EU's replicability** and the design of future policies to strengthen Europe's semiconductor capabilities, particularly through coordinated public-private investments, infrastructure support, and the development of advanced pilot lines.

Finally, the section explores cross-cutting enabling factors that are critical for the success of Europe's semiconductor ecosystem. These include **guarantees on water and energy supply**, the establishment of a **coordinated governance structure**, and the integration of **economic security considerations** into semiconductor strategy.

3.1. Tax Credits

3.1.1. Overview of Instrument

Tax credits are a type of financial incentive provided by governments to reduce the amount of tax that a company owes to the local government. These are widely utilised by governments to reduce the tax burden on businesses, thereby attracting greater investments towards the domestic economy. Tax credits typically target investments towards specific business activities, including R&D, manufacturing and workforce training, and thus may be subject to specific eligibility criteria and application procedures.

3.1.2. Industry Benefits

Tax credits can be highly beneficial for large companies, particularly when it comes to alleviating operating expenditures (OpEx), by reducing the amount of tax owed and providing immediate financial relief. On the other hand, their effectiveness is limited for start-ups and scale-ups, where their revenues and profits streams are often not sufficient to fully benefit from tax credits.

While tax credits can serve as a valuable tool to encourage investment and support business growth, they cannot, on their own, sustain or stimulate the broader industrial ecosystem. For

start-ups and scale-ups, the absence of immediate revenue streams means that tax credits may not provide the necessary financial support. For this reason, tax credits need to be strategically designed and complemented by other supportive instruments, including grants, subsidies, or access to venture capital, in order to create a more holistic and sustainable environment for these emerging businesses to thrive.

Refundable or carry-forward tax credits can provide significant benefits for start-ups, allowing them to receive a refund or carry unused credits forward when they are not yet profitable. This flexibility can offer immediate relief and support their growth in the early stages. However, the design and targeting of tax credits are crucial factors in determining the beneficiaries. If not carefully designed, tax credits may not support the businesses that need them most. Therefore, **the way in which tax credits are structured and targeted plays a key role** in ensuring that both established companies and emerging start-ups benefit from these incentives.

3.1.3. Case Studies

The **U.S. CHIPS and Science Act** in the U.S. includes a 25% tax credit for investments in semiconductor manufacturing facilities[26]. The tax credit, estimated at USD 46 billion, is designed to attract private investment into semiconductor manufacturing, boosting domestic production. This measure complements the grants, loans, and loan guarantees that are also allocated under the Chips Act. These tax credits aim to alleviate part of the sizeable costs associated with setting up semiconductor manufacturing facilities, thus enabling companies to invest in cutting-edge technologies and infrastructure in the U.S.

South Korea's K-Chips Act introduces a tiered tax credit system designed to attract domestic and foreign investments towards South Korea's semiconductor ecosystem[27]. The tax credit rate for facility investments has been raised from 15% to 20% for large and medium-sized enterprises, and from 25% to 30% for small and medium-sized enterprises (SMEs), while R&D tax credits were extended until 2031 to further strengthen R&D capabilities.

3.1.4. EU Replicability

The EU does not have direct competence over tax policy, meaning EU-level tax credits are not an option, however, the EU can establish guidelines and provide incentives within the state aid rules. This could be reinforced under the Important Projects of Common European Interest (IPCEI) framework and within the revised Chips Act. In this context, it is crucial for the EU to create the necessary framework conditions that allow national governments to design and use tax credits as a policy tool to foster growth and innovation within their semiconductor ecosystems.

[26] CHIPS and Science Act (Public Law 117–167), U.S. Congress. URL: https://www.congress.gov/bill/117th-congress/house-bill/4346/text; CSIS, A World of Chips Acts: The Future of U.S.-EU Semiconductor Collaboration. URL: https://www.csis.org/analysis/world-chips-acts-future-us-eu-semiconductor-collaboration

[27] ChosunBiz (February 2025), K-Chips Act passes National Assembly, increasing semiconductor tax credit rates. URL: https://biz.chosun.com/en/en-policy/2025/02/27/FZ5DBVBG25CR7A2BUUXWKVVCBU/

SEMI Europe Recommendations – Tax Credits

Policy recommendation 19: Encourage EU Member States to adopt targeted fiscal incentives (Ex. Tax credits) within a harmonised EU framework to stimulate investment and innovation across their semiconductor ecosystems, with differentiated measures based on company size.

3.2. Specific Measures for SMEs, Start-ups and Scale-ups

3.2.1. Overview of Instrument

Small and medium-sized enterprises (SMEs) and startups require specific, tailored measures adapted to their size and scale of business operations. These measures should be designed to support their growth and address their specific challenges, including high costs, excessive administrative burden, limited revenues and profits streams.

3.2.2. Industry Benefits

Tailored measures for SMEs and startups can make it more affordable for smaller companies to access semiconductor pilot lines and cutting-edge R&D facilities. Lowering these entry costs allows start-ups to conduct trials, develop prototypes, and refine their technologies without the financial strain typically associated with these processes. Additionally, streamlining administrative processes and providing targeted public funding, including grants and tax incentives, can simplify engagement with government-backed facilities and funding programs.

Therefore, reducing these financial and bureaucratic barriers can enable start-ups and SMEs to thrive, fostering greater innovation and competitiveness. This targeted support can also help create a more level playing field, allowing smaller players to benefit from technological advancements alongside the established industry leaders.

3.2.3. Case Studies

South Korea's K-Chips Act offers tax incentives specifically tailored for SMEs, with increased tax credits for facility investments (Up to 30% for SMEs) and extended periods for R&D tax credits[28]. Additionally, South Korea's government has launched further initiatives, including a USD 750 million fund dedicated to assisting fabless companies and equipment manufacturers, which also supports smaller players across the semiconductor supply chain.

Japan's semiconductor strategy promotes SME participation in the supply chain by offering a mix of subsidies and financial incentives. On 13th June 2025, Japan's Cabinet approved the annual Basic Policy on Economic and Fiscal Management and Reform, which reaffirmed its commitment to large-scale production of next-generation semiconductors through capital investment,

[28] ChosunBiz (February 2025), K-Chips Act passes National Assembly, increasing semiconductor tax credit rates. URL: https://biz.chosun.com/en/en-policy/2025/02/27/FZ5DBVBG25CR7A2BUUXWKVVCBU/

infrastructure development, design support and workforce development[29]. The strategy aims to establish a domestic ecosystem, comprising chip design and manufacturing, server operations and AI technological sovereignty. Under this strategy, the government is seeking to encourage SME participation in the supply chain through regional consortia and ongoing private-sector engagement.

3.2.4. EU Replicability

The EU should adopt a model that better supports start-ups and SMEs in the semiconductor sector, introducing greater simplification and addressing key concerns from smaller players, particularly with regards to the administrative burden and long procedures for the industrial pilot lines.

In the current framework, the costs to access pilot lines for SMEs, start-ups, and scale-ups are prohibitively high as these actors often lack dedicated funding and project teams, forcing them to outsource applications and reports to costly consultancies. This financial burden discourages participation, effectively excluding them from benefiting from Pillar I advancements and reinforcing the existing barriers to innovation. Based on our previous assessment in Section 2, SEMI Europe suggests the following:

SEMI Europe Recommendations – Tailored Measures for SMEs, Startups and Scaleups

Policy recommendation 1: Establish industrial pilot lines, supported by an EU budget line, that integrate projects from companies of varying sizes (large firms, SMEs, and startups) in research pilot line products' prototyping, development, and industrialisation, thereby accelerating commercialisation across the entire supply chain.

Policy recommendation 4: Dedicate a specific budget line in pilot lines projects to support industry's participation (Large multinational companies, SMEs, startups and scaleups) and to provide specific support to smaller players, mostly via pilot line vouchers, R&D vouchers and a specific budget line in pilot lines for SMEs, startups and scaleups.

3.3. Japan's RAPIDUS Model

3.3.1. Overview of Instrument

Japan has worked to develop its own advanced semiconductor technologies with the creation of Rapidus, founded in 2022 as a consortium of eight major Japanese companies, including Toyota, Sony, and NTT, aiming to develop and mass-produce advanced 2-nanometer semiconductors by 2027. Rapidus aims to enter the advanced-node foundry business, with its focus on building both domestic R&D and manufacturing capabilities. The company employs a dual-track strategy: collaborating with Japan's Leading-edge Semiconductor Technology Centre (LSTC) and partnering with global leaders like IBM and IMEC for technology licensing and joint research.

[29] Japan's Basic Policy on Economic and Fiscal Management and Reform 2025. URL: https://www5.cao.go.jp/keizai-shimon/kaigi/minutes/2025/0606shiryo_01.pdf

Rapidus is currently constructing a 2nm pilot production line in Hokkaido, with plans to begin mass production by 2027.

The Japanese government has committed substantial resources to Rapidus. In April 2024, the Japanese government announced an additional subsidy of JPY 590 billion (approximately USD 3.9 billion) to Rapidus, supplementing the USD 2.2 billion allocated in 2022. In March 2025, it announced an additional subsidy of USD 5.54 billion for Rapidus, which includes funding for both front-end advanced semiconductor processes (USD 4.7 billion) and back-end processes such as packaging and testing (USD 0.88 billion). Japan's government has since outlined, in May 2025, its future semiconductor policy, centred around full-scale support and strict monitoring of the Rapidus project in order to meet the 2027 target date.

The Rapidus approach can be considered a strategic, collaborative approach designed to foster national leadership in advanced semiconductor manufacturing, bringing together major industry players, collaborating to advance the development and production of next-generation semiconductor technologies. Central to this model is the combination of private sector efforts with large-scale public support, with substantial public investments to support R&D and infrastructure.

3.3.2. Industry Benefits

The industry benefit of the Rapidus approach to national semiconductor advancement is its ability to strengthen cutting-edge technological leadership, foster industry-wide collaboration, and drive economic growth, ultimately benefiting all participants within the national semiconductor ecosystem.

This inclusivity not only drives innovation but also provides SMEs with access to vital resources, infrastructure, and funding, enabling them to scale-up within the semiconductor industry. If successful, the approach would further solidify the country's position as a global semiconductor hub, attracting investment, talent, and forging international partnerships that reinforce its technological and economic standing.

3.3.3. EU Replicability

While the direct replication of the Rapidus model may not be fully applicable to the EU context, the EU could adapt this approach and encourage European Semiconductor Consortiums in critical value chain segments where European capacities are needed and which offer significant opportunities for growth and matter to the bloc's technological sovereignty. In this regard, the ESMC joint venture provides a useful blueprint. Europe could bring together national governments, research institutes, and industry leaders to co-invest (Public-private partnership) in critical technologies needed in Europe.

Furthermore, Europe could also adapt the Rapidus model by leveraging IMEC's NanoIC pilot line to develop a central hub for advanced semiconductor R&D and manufacturing, with the involvement of key European players across the semiconductor supply chain. The success of the initiatives would ultimately require strong leadership and coordination (Governance structure) to

ensure a coherent strategic direction or otherwise result in uncoordinated and inefficient projects.

SEMI Europe Recommendations – European Semiconductor Consortiums

Policy recommendation 20: Foster and encourage coordinated public-private semiconductor consortiums to co-invest in critical semiconductor-related technologies, building on existing models (Ex. ESMC and IMEC's NanoIC) supported by strong EU-level governance and strategic coordination.

3.4. Water and Energy Supply Guarantees

3.4.1. Overview of Instrument

Ensuring reliable water and energy supplies is essential for semiconductor manufacturing, given its highly resource-intensive processes. Governments can address this by upgrading the relevant infrastructure and securing the necessary investments from regional authorities on the one hand, and EU Member States on the other. Targeted investments in specific areas would help maintain and expand the availability of water and energy to meet the growing demands of the semiconductor industry.

3.4.2. Industry Benefits

Guaranteed water and energy supplies provide stability to the semiconductor industry by preventing supply chain disruptions that could halt production. Reliable access to these resources is vital for maintaining consistent output, particularly in regions with limited infrastructure or specific resource challenges, including but not limited to Grenoble, Malaga, Dresden and Catania.

3.4.3. Case Studies

South Korea's K-Chips Act includes plans to improve infrastructure, including the water supply and power systems around key semiconductor hubs (Ex. Pyeongtaek and Yongin), where new large-scale semiconductor fabs are under construction[30]. South Korea's National Assembly has also passed three energy-related acts, aiming to tackle key energy supply issues, and ensuring that nuclear power plants at risk of closure can continue operating until 2030[31]. These laws are part of a larger strategy to foster the growth of South Korea's energy-intensive semiconductor industry, by securing a stable and adequate energy supply.

3.4.4. EU Replicability

It will be essential for future EU water and energy policy to explicitly reflect the unique requirements of the European semiconductor industry, given its strategic importance and

[30] AIInvest (April 2025), South Korea's Semiconductor Tax Credit: A Blueprint for Global Dominance?. URL: https://www.ainvest.com/news/south-korea-semiconductor-tax-credit-blueprint-global-dominance-2504/

[31] BusinessKorea (February 2025), Korea Passes 'K-Chips Act' and 3 Energy Laws to Boost Semiconductor and Energy Sectors. URL: https://www.businesskorea.co.kr/news/articleView.html?idxno=236425#google_vignette

resource-intensive nature. With the advancement of the green transition and the Clean Industrial Deal, policy implementation should include targeted measures that enable the semiconductor sector to address its water and energy challenges while progressing toward sustainability goals.

This should involve integrating semiconductor manufacturing into broader infrastructure planning, incentivising the adoption of energy-efficient and water-recycling technologies, and ensuring that regulatory frameworks support both environmental objectives and industrial competitiveness.

SEMI Europe Recommendations – Water and Energy Supply Guarantees

Policy recommendation 21: Recommend EU Member States to integrate the semiconductor industry's specific water and energy needs into their respective national strategy for semiconductors and advanced technologies, enhancing domestic attractiveness for semiconductor investments.

3.5. Chips Act Governance Structure

3.5.1. Overview of Instrument

The major semiconductor initiatives around the world have been supported by robust institutional frameworks that allow for greater coordination between industry and government priorities. Public administrations have established dedicated agencies or inter-ministerial bodies with specialised staff and strategic planning capabilities to oversee investments, R&D programs, and respond to market or geopolitical shifts.

3.5.2. Industry Benefits

Dedicated government agencies and bodies provide industry with clear points of contact, streamlined regulatory guidance, and coordinated support for R&D and investment initiatives. The alignment of public resources and government planning with industrial priorities can reduce uncertainty, accelerate project execution, and enable companies to scale innovation more efficiently while navigating complex policy and security requirements.

3.5.3. Case Studies

Under the **U.S. CHIPS and Science Act**, the White House has centralised decision-making by creating the Subcommittee for Microelectronics Leadership within the President's National Science and Technology Council[32]. This subcommittee is responsible for shaping the national strategy on microelectronics research, development, manufacturing, and supply chain security. Additionally, the White House formed the CHIPS Innovation Steering Council to oversee and coordinate the development and implementation of policies necessary for the effective execution of the CHIPS Act within the executive branch.

[32] CHIPS and Science Act (Public Law 117–167), U.S. Congress. URL: https://www.congress.gov/bill/117th-congress/house-bill/4346/text

3.5.4. EU Replicability

The EU could strengthen existing bodies like the European Semiconductor Board (ESB) by incorporating stronger and more systematic representation from industry, ensuring that decision-making reflects the practical needs and priorities of semiconductor companies.

Furthermore, a renewed commitment to the Alliance on Processors and Semiconductor Technologies (ALLPROS) would provide a structured forum for continuous dialogue between policymakers and industry stakeholders, helping to align EU strategies with technological trends and market realities.

SEMI Europe Recommendations – Chips Act Governance Structure

Policy recommendation 22: Establish an overarching governance structure for the implementation of the Chips Act 2.0, strengthening industry representation within decision-making bodies, consolidating existing platforms and initiatives (Ex. Industrial Alliance, ESB, and Chips JU) under a single, coordinated framework.

3.6. Economic Security in the Chips Act

3.6.1. Overview of Instrument

National semiconductor strategies and economic security policies can be effectively integrated as part of a broader strategic policy nexus. This integration is critical for ensuring that semiconductor production and other strategic supply chains remain resilient, competitive, and aligned with national interests in a rapidly changing global context. Given the strategic importance of semiconductors across vital sectors (Ex. Defence, telecommunications, energy and AI), governments must consider their semiconductor strategies not in isolation, but as part of a larger framework focused on economic security, technological sovereignty, and geopolitical stability. This is especially the case nowadays, where semiconductors are at the centre of global geopolitical competition, with major players working to secure supply chains and leveraging their strengths to exert pressure on competitors.

3.6.2. Industry Benefits

Integrating industrial policy with broader economic security objectives provides companies with a relatively more stable and secure business environment. Considering the current extent of global geopolitical competition, a more coordinated policy can strengthen supply chain resilience, support companies in navigating export controls and facilitate access to critical raw materials. Particularly in the sphere of semiconductors, this integrated approach will be fundamental to ensure competitiveness and economic security simultaneously.

3.6.3. Case Studies

Under the **U.S. CHIPS and Science Act**, the White House has centralised decision-making by creating the Subcommittee for Microelectronics Leadership within the President's National

Science and Technology Council[33]. Complementing this, the CHIPS Innovation Steering Council to oversee and coordinate the development and implementation of policies necessary for the effective execution of the CHIPS Act within the executive branch. These structures are crucial to align national security and technological competitiveness objectives, providing the U.S. government with a comprehensive strategic view on its semiconductor industry.

3.6.4. EU Replicability

The EU could adopt a more integrated approach by ensuring that the updated Chips Act is aligned with the EU's economic security strategy. This would include strategic measures to reduce external dependencies and increase Europe's technological sovereignty in critical sectors. With the forthcoming Economic Security Doctrine to be presented by DG TRADE before year end, there is an opportunity for the EU to more explicitly integrate semiconductors withing the EU's economic security strategy thinking. Based on our assessment in Section 4, SEMI Europe suggests the following:

SEMI Europe recommendations – EU Economic Security Strategy and Doctrine

Policy recommendation 27: To develop a coherent, risk-based and harmonised EU economic security doctrine that safeguards strategic technologies and attracts high-value semiconductor investments, while enhancing Europe's competitiveness by supporting inbound and outbound investments, cross-border R&D partnerships, and high-value industrial projects.

[33] CHIPS and Science Act (Public Law 117–167), U.S. Congress. URL: https://www.congress.gov/bill/117th-congress/house-bill/4346/text; CSIS, A World of Chips Acts: The Future of U.S.-EU Semiconductor Collaboration. URL: https://www.csis.org/analysis/world-chips-acts-future-us-eu-semiconductor-collaboration

Section 4 – Building a Comprehensive Policy Framework for Semiconductors

The European Chips Act should not be viewed in isolation but as part of a **broader policy ecosystem** in which complementary legislation can significantly influence its implementation and outcomes, both positively and negatively.

Vertically, the Chips Act must be supported by a robust policy framework that guarantees a coherent budget aligned with its ambitions, an enabling environment that strengthens Europe's attractiveness to both domestic and foreign investors and a stable global trade environment and steady supply of critical minerals.

Horizontally, market demand must be stimulated to absorb future semiconductor production capacities and unlock new investment opportunities. If the supply and demand of advanced semiconductor technologies do not align, the European Chips Act fund will bring limited benefits to the EU. So far, the lack of market demand is the primary concern when exploring the possibility of investing in Europe and building new facilities. The market uncertainties revolving around the European market have disincentivised companies to invest in Europe.

4.1. Vertical Alignment – Policy Foundations for Semiconductor Growth

Vertically, the Chips Act must be supported in terms of financial, market and trade measures. Building synergies across these policies is essential to foster a competitive and resilient semiconductor ecosystem in Europe.

4.1.1. Multiannual Financial Framework and European Competitiveness Fund (2028-2034)

The European Commission's proposal for the 2028–2034 Multiannual Financial Framework (MFF) and the creation of the European Competitiveness Fund (ECF) represent a pivotal opportunity to strengthen Europe's technological and industrial base. SEMI Europe welcomes the ECF's focus on simplifying access, increasing coherence, and introducing flexible financial tools. However, to ensure real strategic impact, the EU must clearly prioritise **semiconductors** within the ECF, recognising their foundational role in all major industrial sectors and their importance to Europe's digital sovereignty.

To close the investment gap with the U.S. and Asia, SEMI Europe calls for a **dedicated semiconductor budget** that sends a strong signal of commitment towards this critical industry. In this context, the EU should ensure **harmonised coordination** between Horizon Europe and the ECF to create a seamless "**lab-to-fab-to-market**" pathway, allowing continuous support from research through industrial deployment. This is especially important given that the success of pilot lines will depend on companies' ability to **absorb and scale RTO-developed**

technologies, which remains prohibitively expensive for SMEs and start-ups. Policy measures should therefore focus on **cross-segment R&D collaboration** to accelerate technology transfer and reduce the industrialisation gap.

Furthermore, a funding programme tailored to SMEs within the ECF should be created to provide equity-based financing, easier access to first-of-a-kind facilities, and simplified application procedures. To ensure long-term impact, the EU should also establish a **sustainable governance and funding structure for pilot lines** – ensuring their viability beyond initial Chips Act funding and enabling them to become self-sustaining innovation hubs integrated with industry demand.

Finally, SEMI Europe calls for a comprehensive approach to infrastructure, sustainability, and resilience. The ECF should prioritise investment in **power, water, and transport infrastructure** for semiconductor clusters, support **PFAS substitution and circular manufacturing**, and create a **Supply Chain Resilience Facility** to strengthen access to **critical raw materials**. By strategically aligning the Chips Act and the ECF, Europe can build an integrated, competitive, and future-proof semiconductor ecosystem that can enhance sustainability and innovation.

SEMI Europe recommendations – Multiannual Financial Framework (2028-2034)

Policy recommendation 23: Prioritise semiconductors within the European Competitiveness Fund (ECF) by establishing a dedicated budget and ensuring coordination with Horizon Europe to create a seamless "lab-to-fab-to-market" pathway.

Policy recommendation 24: Establish targeted funding mechanisms within the ECF—including a Semiconductor SME Accelerator and a sustainable governance structure for pilot lines—to enhance SME participation, ensure long-term viability of innovation infrastructures, and invest in critical enablers such as resilient supply chains, sustainable manufacturing, and essential infrastructure for semiconductor clusters.

4.1.2. Capital Markets Union

The Capital Markets Union (CMU) is a key EU initiative aimed at **integrating and deepening Europe's financial markets**, **reducing fragmentation**, and improving **access to finance** for companies across the continent. By harmonising rules, simplifying cross-border investment, and fostering a more diversified funding ecosystem, the CMU seeks to complement traditional bank lending with robust venture, growth, and equity financing.

In this context, Europe's semiconductor ecosystem faces a critical challenge in its ability to scale up **breakthrough innovations to large-scale industrialisation and commercialisation**. The Capital Markets Union can play a critical role in bridging this gap by providing harmonised, cross-border access to financing that complements traditional bank lending. By enabling startups and scale-ups to tap into venture, growth, and equity capital across the EU, the CMU can help Europe translate its R&D strengths into commercially viable semiconductor technologies and technology-focused chip solutions (Ex. AI, quantum, renewables, EVs).

A fully functional CMU would also help create a more dynamic and vibrant venture capital ecosystem in Europe, similar to that which drives US semiconductor innovation. Today, Europe's venture funding is fragmented across national borders and often risk-averse, limiting the ability of startups to scale rapidly. By **integrating capital markets, harmonising investment rules, and facilitating cross-border flows**, the CMU would attract larger pools of private investment willing to support high-risk, high-reward projects. This would allow European semiconductor innovators to grow faster, commercialise advanced chips at scale, and capture value domestically, ensuring that breakthroughs in advanced technologies, HPC, and leading-edge semiconductors remain anchored in Europe.

SEMI Europe Recommendations – Capital Markets Union

Policy recommendation 25: Advance the completion of a fully integrated and harmonised Capital Markets Union (CMU) to stimulate cross-border private investment and support the growth of SMEs, startups, and scaleups in commercialising advanced and leading-edge semiconductor technologies.

4.1.3. Global Trade and Economic Security

The semiconductor industry depends on an intricate global supply chain spanning multiple continents. This interconnectedness makes it particularly vulnerable to trade and geopolitical tensions. In recent years, countries have increasingly used trade policy as a strategic tool to advance industrial and security objectives, often at the expense of open markets and global cooperation. As a result, Europe faces a more fragmented, politicised, and uncertain global trade environment. The European semiconductor ecosystem is considerably influenced by these trade and geopolitical instabilities, and the upcoming Chips Act 2.0. must be framed with regards to these challenges.

4.1.3.1. Global Trade Tensions

4.1.3.1.1. EU-US Trade Dispute

As the European Union is holding close negotiations with the United States to find the future terms of their partnerships, the European Union has given **careful attention to the semiconductor industry and the strong global interdependencies** underpinning its value chain. The latest US-EU framework agreement of August 21, 2025, has most notably capped U.S. tariffs on EU-originating semiconductors at a maximum of 15%. The measure is meant to hold regardless of the future results of the Section 232 investigation on semiconductors and manufacturing equipment. A potential exemption for semiconductor manufacturing equipment is also included in the agreement.

The EU-US agreement has defined the framework of the tariff negotiations, but numerous challenges are still paving the way to a final trade agreement. The **steel and aluminium tariffs** imposed by the U.S. under Section 232 of the Trade Expansion Act continue to affect transatlantic trade and have direct implications for the semiconductor industry. Semiconductor companies are facing **complex due diligence** required to determine the precise steel and aluminium content in products exported to the US. While the direct impact on chipmakers is minimal, suppliers of semiconductor manufacturing equipment face **tens of millions of euros in**

compliance costs. These challenges stem from reliance on third-party suppliers across different jurisdictions, limited transparency due to confidentiality and intellectual property constraints, and the administrative burden of collecting sensitive data, all of which weigh heavily on profitability and competitiveness.

The U.S. Steel and Aluminium Tariffs directly hinders European companies' ability to compete on the global market. Given that semiconductor-related equipment often costs several million euros, suppliers are **unable to absorb such price increases** and are therefore compelled to pass these additional costs on to their customers.

4.1.3.1.2. China's Export Controls

China has responded by introducing its own export controls on rare earths and critical minerals. In April 2025, China expanded its Export Control Law to include seven additional rare earth elements (dysprosium, gadolinium, lutetium, samarium, scandium, terbium, and yttrium) further tightening its control over critical inputs for semiconductor and high-tech manufacturing.

These measures marked the third round of Chinese export restrictions following earlier controls on gallium and germanium in late 2024 and early 2025. The new restrictions are used in metals and specialised magnets made from these rare earths, which are used in motors, transistors, and components of semiconductor manufacturing equipment. Given that China is the sole or dominant global supplier for most of these materials, the move significantly heightens concerns about Europe's supply security and long-term industrial resilience.

If export controls persist or intensify, **medium- and long-term disruptions** could emerge, particularly for R&D, semiconductor manufacturing equipment and advanced packaging. The European semiconductor value chain faces specific challenges in **tracing the origin and content** of these materials. Supply-chain opacity, driven by intellectual property protection and commercial confidentiality, makes it difficult to anticipate disruptions or identify exposure to restricted inputs. This lack of transparency also complicates compliance with export control regimes and hampers strategic planning.

Gallium and germanium remain particularly sensitive due to their critical role in semiconductor performance. Although the semiconductor sector uses relatively small quantities, the absence of substitutes and China's dominant global share (over 90% for gallium and 83% for germanium[34]) expose the industry to systemic risks. Together, these developments underline the **growing geopolitical fragility** of Europe's semiconductor supply chain and reinforce the need for diversification, strategic stockpiling, and deeper alignment between international trade policies and industrial policies such as the forthcoming Chips Act 2.0 and the Critical Raw Materials Act.

SEMI Europe Recommendations – Global Trade

Policy recommendation 26: Enhance the EU's appeal for semiconductor investment and research by further aligning industrial and trade policies, ensuring coherent incentives, and fostering a predictable regulatory environment.

[34] European Commission Study on the Critical Raw Materials for the EU (ET-07-23-116-EN), 2023. URL: https://op.europa.eu/en/publication-detail/-/publication/57318397.

4.1.3.2. EU Economic Security Strategy and Doctrine

The next iteration of the EU Chips Act should not only focus on boosting manufacturing capacity and R&D but also on mitigating trade-related vulnerabilities. The Act should be better aligned with the EU's broader Economic Security Strategy and the forthcoming Economic Security Doctrine, particularly in three key areas: export controls, foreign direct investment (FDI) screening, and outbound investment monitoring.

4.1.3.2.1. Screening of Foreign Direct Investments

The ongoing review of the EU's FDI Screening Regulation risks introducing additional administrative layers that could undermine Europe's investment attractiveness compared to faster and more predictable systems in major semiconductor regions such as South Korea and Taiwan. SEMI Europe stresses that the framework should support, not hinder, the Chips Act's objectives by **facilitating high-value foreign investment** and **technology partnerships** essential for scaling Europe's semiconductor capabilities.

Excessively rigid deadlines and broad notification obligations, as proposed by the European Parliament, could delay decisions on acquisitions, joint ventures, and R&D partnerships that the Chips Act tries to incentivise. SEMI Europe supports the Council's position to exclude greenfield investments and to limit the Regulation's scope to dual-use and military goods, avoiding unnecessary coverage of low-risk sectors. Likewise, Annex II should focus only on investments involving export-controlled or defence-related items, or include narrow, clearly defined sectoral criteria to ensure predictability.

To provide legal certainty, the definition of "control" should align with that used in the EU Merger Regulation and the Foreign Subsidies Regulation, ensuring consistency across instruments. Policymakers should also consider how ongoing EU-US trade negotiations and tariff discussions might influence the design of the new FDI framework, particularly in sensitive technology sectors like semiconductors.

4.1.3.2.2. Outbound Investment Screening

While attention to outbound investments is part of Europe's growing economic security focus, SEMI Europe underlines that outward FDI plays a crucial role in strengthening the competitiveness of the European semiconductor industry. Outbound investments enable European firms to access new markets, expand production capacity, and participate in international R&D ecosystems, all of which reinforce long-term economic resilience. Many European semiconductor companies have built significant operations in China, particularly in the automotive chips segment, which represents an essential market and innovation base.

SEMI Europe supports a **risk-based and proportionate approach** that would allow companies to **maintain global partnerships** while addressing **legitimate security concerns**. SEMI Europe supports a 'China-for-China' strategy, enabling firms to maintain separate operations in China to serve the local market without undermining European technological leadership or security interests.

4.1.3.2.3. Export Control Framework

As demonstrated in the recent German Microelectronics Strategy, which hints at stricter, continuously updated export controls and research-security measures across microelectronics, there is increasingly a clear will from Member States to prevent critical technology leakage and misuse. The proliferation of national export control frameworks, however, may inhibit the formation of a **cohesive EU-level approach**.

SEMI Europe strongly supports better coordination at EU level on the export controls of dual-use items and a clearer, harmonised definition of controlled goods. SEMI Europe encourages the development of a single, **unified EU risk assessment system**, replacing the current patchwork of national regimes that create uncertainty and administrative burdens for exporters. Such a system would facilitate compliance and provide predictability for semiconductor companies operating across multiple Member States.

A harmonised European approach to export controls would also strengthen the EU's position globally, ensuring that its measures are coordinated and proportionate, rather than reactive to unilateral U.S. actions such as the 2022 export controls on advanced semiconductor equipment. This would help protect Europe's technological competitiveness while ensuring the responsible trade of sensitive technologies.

SEMI Europe Recommendations – EU Economic Security Strategy and Doctrine

Policy recommendation 27: To develop a coherent, risk-based and harmonised EU economic security doctrine that safeguards strategic technologies and attracts high-value semiconductor investments, while enhancing Europe's competitiveness by supporting inbound and outbound investments, cross-border R&D partnerships, and high-value industrial projects.

4.2. Horizontal Alignment – Cross-Industrial Coordination

Crucially, the Chips Act should be horizontally aligned with other EU industrial and technology policies such as for quantum and Artificial Intelligence (AI) technologies to ensure strategic coherence and favour cross-market alignment.

4.2.1. Technological Prioritisation

The design of the Chips Act 2.0. must be performed in accordance with the European Union's technological priorities set in third industrial and tech legislations, ensuring that these initiatives are mutually reinforcing each other and well-coordinated. **Technological priorities** are driven by future market needs, such as AI, quantum, automotive, or energy technologies, but also factors related to strategic autonomy, supply chain resilience, economic security, and geopolitical leverage. Such a focus will help guide investment and innovation towards areas of strategic importance, ensuring that the industry is competitive in emerging fields.

Third countries have already defined their priorities for the semiconductor industry. China has, for instance, prioritised advanced semiconductor technologies crucial for AI and high-bandwidth

memory (HBM), addressing bottlenecks that have historically constrained its industry. Going a step further, Taiwan has decided to combining semiconductor and AI technologies to develop innovative applications across multiple sectors such as food, medicine, and transportation. Industrial policies in the field of semiconductors were adopted accordingly.

By aligning EU semiconductor policies with the future demand for critical technologies like AI, quantum, automotive, and energy, the EU could create a more focused and competitive industry. This would require a thorough **assessment of Europe's strengths and market needs** over the next decade to identify the most promising areas for investment. It will be important for the EU to clearly define which semiconductor technologies and segments of the semiconductor value chain it aims to support, as part of discussions on the updated Chips Act. This work must consider the whole value chain necessary to the supply of these priority technologies and not only their final producer. These discussions must take account of Europe's prosperity, indispensability and resilience.

SEMI Europe Recommendations – Prioritisation of Key Technologies

Policy recommendation 28: Identify future European market trends and technological needs in semiconductors to strategically prioritise investments and R&D, taking into account the entire supply chain, from private and public research entities, design, equipment, materials and components suppliers as well as back-end and front-end chip manufacturers.

4.2.2. Artificial Intelligence (AI)

The EU AI Continent Action Plan and AI Package are strategic initiatives to strengthen Europe's technological sovereignty, aiming to deliver investments in AI factories, AI gigafactories and sustainable data centres, which will ultimately generate **sustained demand for leading-edge semiconductor technologies** produced in Europe. While these initiatives anticipate strong synergies between the semiconductor and AI sectors, realising this potential depends on creating an enabling environment that promotes coordination and collaboration across these industries.

The expansion of AI factories, AI gigafactories, and sovereign data centres will dramatically raise Europe's demand for cutting-edge semiconductors such as high-performance GPUs, AI accelerators, advanced logic, power-efficient memory and interconnect technologies. Each large-scale AI facility may require hundreds of thousands of advanced chips, creating a powerful domestic demand driver that can justify and sustain local semiconductor R&D and manufacturing investments. This scale of computing infrastructure, if paired with the EU Chips Act, can anchor Europe's next wave of semiconductor production capacity.

However, this opportunity comes with critical **implementation challenges**. Europe must secure sufficient access to manufacturing at advanced process nodes, ensure supply of critical materials and packaging capacity, and expand its design and verification ecosystem. Building AI infrastructures also places intense pressure on **energy availability, sustainability, and cooling systems**, areas where chip design efficiency and data-centre hardware innovation are closely intertwined. Without coordinated planning, Europe risks increasing dependency on the very

chips that power its AI infrastructure, missing the chance to capture the full industrial value chain.

For these reasons, targeted investments towards leading-edge semiconductor capacity are essential if Europe is to reduce dependency on non-EU suppliers and power its own AI infrastructure with **European-made technology**. This requires scaling up Chips Act pilot lines towards higher TRL levels (7 to 9) and supporting their industrialisation, strengthening design ecosystems and fostering partnerships with all the key players across the supply chain.

SEMI Europe Recommendations – Artificial Intelligence

Policy recommendation 29: Ensure coherent integration of Europe's AI industrial policies with the Chips Act 2.0 by enhancing coordination and collaboration between the AI and semiconductor sectors to attract investment, foster innovation and support the industrial deployment of next-generation AI chips.

4.2.3. EU Quantum Strategy and Quantum Act

The EU Quantum Strategy and the proposed Quantum Act represent critical steps to position Europe as a global leader in quantum technologies. Over the past decade, initiatives such as the Quantum Flagship have nurtured European startups enabling primitive industrial deployment of superconducting quantum computers and other platforms. With a growing demand for quantum processors, the strategy emphasises transitioning from lab-scale experiments to large-scale, commercially viable quantum systems. This includes the Quantum Europe Research and Innovation Initiative, the Quantum Chips Industrialisation Roadmap, and a network of open-access testbeds. They are designed to accelerate innovation, industrialisation, and adoption across sectors including AI, HPC, materials science, finance, and defence. The semiconductor industry is a critical enabler of this transition.

Superconducting quantum processors rely on traditional semiconductor manufacturing techniques, but with unique materials satisfying precise technical requirements, including for the reduction of interferences in qubits operations. These specificities in quantum chips require accurate adaptation of the equipment and materials used in their production as well as the use of new materials in quantum chips. The upcoming Quantum Act will deliver support for research and industrialisation of quantum technologies. **Chips Act 2.0 must be closely coordinated and articulated with the future quantum initiatives** to avoid duplicative measures and overlapping instruments, notably for quantum chips development and industrialisation. Given that SMEs and start-ups dominate the quantum business landscape, further alignment will be required to ensure both instruments include specific funding and scale-up support for European quantum chip developers.

The equipment and tools used in the development of quantum technologies are similar and have low usage rates. This makes it possible to share these tools among multiple start-ups, notably via a foundry-style approach. In practice, this foundry model for quantum chips could be achieved by the creation of a dedicated quantum chip production facility in Europe. Such a facility will de facto qualify as FOAK under the second pillar of the Chips Act and be eligible for receiving state

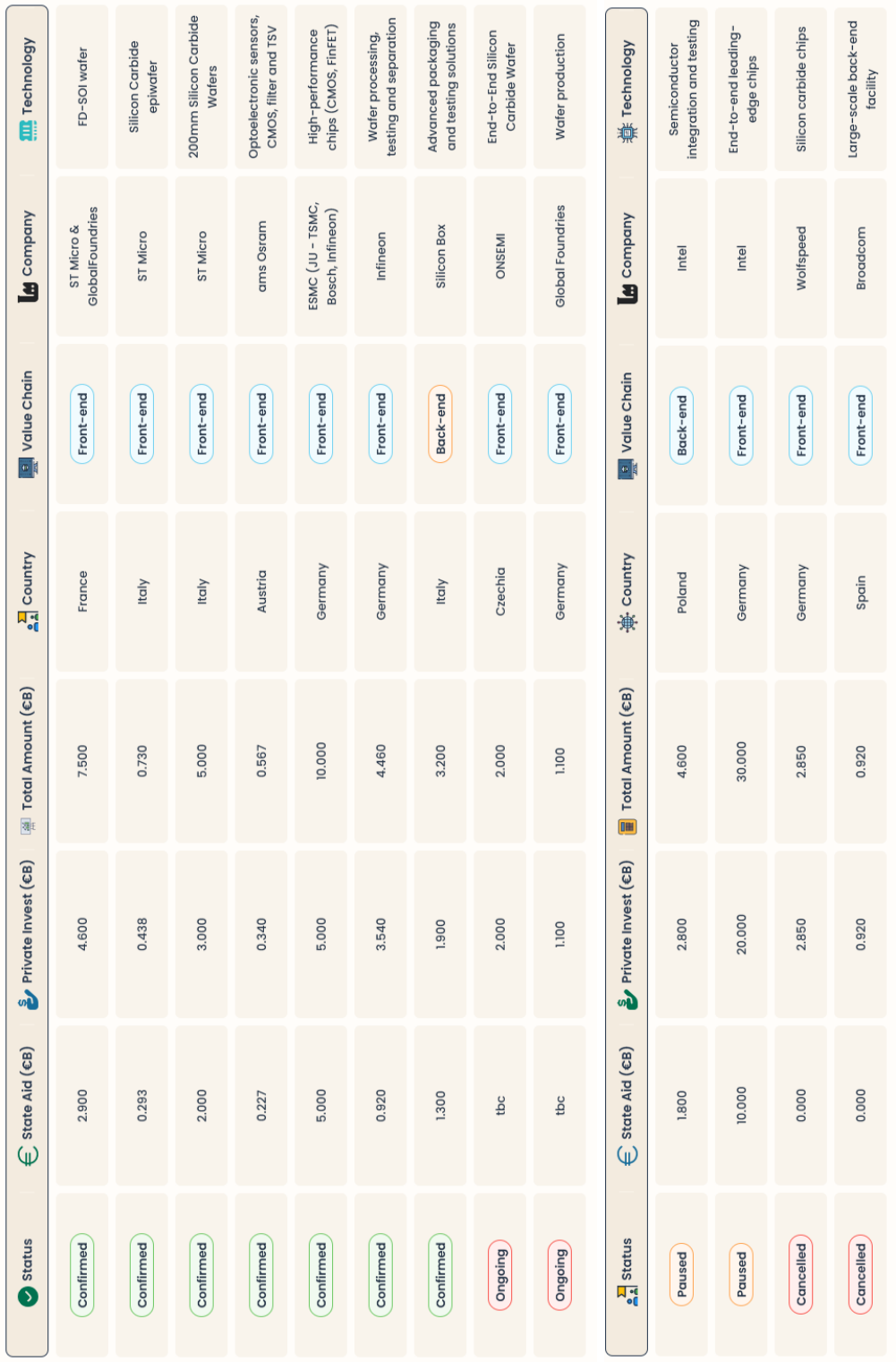
aid. Instead of strictly defining the boundaries between the Quantum Act and Chips Act, a flexible approach will ensure that quantum chips projects contributing to EU-wide capacity building can benefit from multiple European policy instruments and supportive measures.

By **aligning the Chips Act 2.0 with the Quantum Act**, Europe can create a coordinated ecosystem where public funding, industrial-scale semiconductor infrastructure, and startup innovation work together. This integration ensures that quantum chip manufacturing benefits from established semiconductor know-how, fosters a secure and sovereign supply chain, and strengthens synergies between classical and quantum computing.

SEMI Europe Recommendations – Quantum

Policy recommendation 30: Ensure close coordination between the Chips Act 2.0 and the Quantum Act that supports shared use of semiconductor infrastructure, promotes a foundry-style model for quantum chip production, and provides targeted funding and scale-up support for SMEs and start-ups, fostering a competitive and integrated European quantum-semiconductor ecosystem.

Annex I – Confirmed, Ongoing and Paused, Cancelled First-of-a-Kind Investments (November 2025)



Status	State Aid (€B)	Private Invest (€B)	Total Amount (€B)	Country	Value Chain	Company	Technology
Confirmed	2.900	4.600	7.500	France	Front-end	ST Micro & GlobalFoundries	FD-SOI wafer
Confirmed	0.293	0.438	0.730	Italy	Front-end	ST Micro	Silicon Carbide epiwafer
Confirmed	2.000	3.000	5.000	Italy	Front-end	ST Micro	200mm Silicon Carbide Wafers
Confirmed	0.227	0.340	0.567	Austria	Front-end	ams Osram	Optoelectronic sensors, CMOS, filter and TSV
Confirmed	5.000	5.000	10.000	Germany	Front-end	ESMC (JU – TSMC, Bosch, Infineon)	High-performance chips (CMOS, FinFET)
Confirmed	0.920	3.540	4.460	Germany	Front-end	Infineon	Wafer processing, testing and separation
Confirmed	1.300	1.900	3.200	Italy	Back-end	Silicon Box	Advanced packaging and testing solutions
Ongoing	tbc	2.000	2.000	Czechia	Front-end	ONSEMI	End-to-End Silicon Carbide Wafer
Ongoing	tbc	1.100	1.100	Germany	Front-end	Global Foundries	Wafer production

Status	State Aid (€B)	Private Invest (€B)	Total Amount (€B)	Country	Value Chain	Company	Technology
Paused	1.800	2.800	4.600	Poland	Back-end	Intel	Semiconductor integration and testing
Paused	10.000	20.000	30.000	Germany	Front-end	Intel	End-to-end leading-edge chips
Cancelled	0.000	2.850	2.850	Germany	Front-end	Wolfspeed	Silicon carbide chips
Cancelled	0.000	0.920	0.920	Spain	Front-end	Broadcom	Large-scale back-end facility

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