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CDS Position Statement on the European Commission's

Call for Evidence for an Evaluation and Impact Assessment on the EU Chips Act 2

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Abstract

On 5th September 2025, the European Commission published a *Call for Evidence for an Evaluation and Impact Assessment* concerning the review of the EU Chips Act (Chips Act 2). The initiative is aimed at strengthening the EU's resilience and technological sovereignty in semiconductor technologies and applications, in particular by:

- Reducing the EU's dependency on other parts of the world for leading-edge chips, notably by increasing the EU's manufacturing capacity in advanced semiconductors for critical sectors, and
- Increasing systemic insight into the resilience of key market actors, supply chains, and the overall EU semiconductor ecosystem to enable more effective monitoring and crisis preparedness.

The Centre for a Digital Society (CDS) at the European University Institute (EUI) welcomes the opportunity to contribute to this consultation. The submission addresses the three issues highlighted in the Call for Evidence:

- The EU's persistent dependence on non-EU suppliers for sub-10 nm chips;
- The erosion of Europe's competitive edge in essential and mainstream semiconductors;
- The limited visibility over the resilience and vulnerabilities of the semiconductor ecosystem.

Our analysis aims to support a forward-looking policy debate by identifying institutional, economic, and governance gaps that hinder the effective implementation of the Chips Act and by outlining evidence-based options to strengthen the framework. In evaluating the Commission's policy options, the CDS identifies targeted amendments to the Chips Act (Option 2) as the more effective and strategically coherent avenue for addressing Europe's structural vulnerabilities.

In its conclusions, the CDS recommends:

- Designing targeted instruments to secure EU's access to leading edge chips for strategic sectors and participation in their manufacturing while safeguarding competition and innovation;
- Reinforcing long-term support for Europe's competitive strengths in essential and mainstream semiconductors;
- Establishing a structured, proportionate, and enforceable EU-level data gathering framework, integrated with Member State and selected firm-level reporting to improve ecosystem mapping and risk assessment.

Keywords: semiconductors, chips, industrial policy, State aid policy, innovation, economic security, supply chain, resilience, Chips Act 2.

Florence, 28th November 2025

On 5th September 2025, the European Commission launched a Call for Evidence for an Evaluation and Impact Assessment concerning the review of the Chips act (Chips Act 2). The Centre for a Digital Society (CDS) at the European University Institute (EUI) welcomes the opportunity to contribute to this important consultation and to share its academic insights in the field.

This contribution builds upon the CDS' engagement with regulation, innovation competition, and industrial policies, and digital markets. These lines of research, together with the Centre's interdisciplinary expertise in law, economics, and political science, underpins the CDS interest to contribute to policymaking discussions concerning Europe's evolving technological landscape.

The Centre for a Digital Society is funded by the European Commission (via structural funding, service contracts and grants, awarded via competitive tender procedures), other public institutions, and market donors. In accepting private funding, in the form of unrestricted contributions to the CDS budget, the Centre observes the highest academic standards, in terms of intellectual rigor and independence.

Through this Position Statement, the CDS seeks to contribute to the policy debate on the future of Europe's semiconductor strategy, supporting a debate that is analytically grounded, forward-looking, and reflective of the diverse industrial and institutional realities across Member States. The CDS remains at the European Commission's disposal for any further questions, and is ready to jointly organize workshops, engage in research collaboration or other activities that may assist in designing a more robust semiconductor framework for the European Union.

1. Introduction and Rationale

Semiconductors have become a central concern of European economic, technological, and security policy. As the EU prepares its mandatory 2026 review of the Chips Act, the Commission's Call for Evidence comes at a moment when the global industry undergoes profound geopolitical realignment, especially in view of the rapid deployment of AI, the acceleration of high-performance computing, the growing semiconductor intensity of sectors such as defence, space, and automotive, and the impact of trade restrictions. More than EUR 80 billion in announced

semiconductor investments and recent State aid approvals for first-of-a-kind facilities underscore the strategic weight attached to this policy domain. The Chips Act itself acknowledges that "no single geography dominates all steps of the value chain", pointing to the structural interdependence that characterises the semiconductor value chain.

The Commission's Call for Evidence highlights three persistent challenges:

a) Europe's dependence on external suppliers for advanced-node chips (<10 nm);
b) Pressures on its leadership in essential semiconductors; and
c) The absence of a sufficiently granular insight into supply-chain vulnerabilities and technology-leakage risks.

This Position Statement examines the challenges identified in the Call for Evidence against the evidence emerging from recent policy and academic analysis, available mapping exercises, and market analyses.

The analysis moves from a diagnosis of the most apparent vulnerabilities of the Chips Act, informed by an overview of recent policy and academic contributions. As is well known, the Chips Act was adopted in response to several crises: Europe reacted to the COVID-19 supply shocks, to simultaneous U.S. industrial policy initiatives, and to what the CDS believes to be an inaccurate political narrative emphasizing that Europe share of global chip manufacturing declined significantly. The CDS therefore considers this review as an important opportunity to improve a trajectory shaped by emergency responses and potentially misinterpreted benchmarks, and to re-anchor policy in a more realistic assessments of Europe's structural position in the global value chain.

Europe retains globally indispensable strengths in semiconductor equipment and specialised industrial inputs, where it is a net exporter with low exposure to foreign supply. By contrast, the EU has limited domestic capacity in logic and memory chips, with extra-EU imports accounting for nearly 60% of supply and severe concentration in certain World Semiconductors Trade Statistics categories (JRC, 2025). Moreover, Europe's semiconductor demand is structurally distinct: automotive and industrial users absorb the majority of shipments to Europe, with the automotive sector alone accounting for 37%, thereby shaping the continent's vulnerability profile and its opportunities for strategic specialisation.

A credible strategy requires, first, **a granular understanding of Europe's domestic semiconductor ecosystems**. As Kleinhans (2024) notes, while the United States has on several

occasions requested information and conducted surveys to map its semiconductor capabilities, most EU Member States have not carried out comparable exercises. The Commission's own mapping remains insufficiently detailed to inform strategic decision-making, in part because national ecosystems differ significantly: some Member States have substantial manufacturing capacity, while others host important research and technology organisations and equipment suppliers. Without Member-State-level ecosystem data intelligence, it is impossible to formulate meaningful long-term objectives or to design interventions that could lead to genuine comparative advantage.

Second, Member States and the EU must have **a clear understanding of why they support this sector and what long-term outcomes they pursue.** Industrial, foreign policy and economic-security objectives presently differ across Member States; without explicit co-ordination of national aims, Europe risks policy fragmentation and inconsistency in the response to shifts in the U.S.-China rivalry.

Third, **attention should be paid to ensure adequate resources to the EU administrative capacity**. At present, apparently only a handful of officials at a single Directorate (DG CNECT) work full-time on semiconductors, while most Member States have minimal dedicated governmental capacity, despite the complexity of the value chain and the scale of the policy challenges (Kleinhans, 2024). A credible long-term strategy requires the development of a greater analytical, technical, and geopolitical expertise within both the Commission and Member States.

2. Problem-Structured Analysis

Semiconductor markets are characterized by steep but also highly differentiated barriers to entry: the resource intensity, technological complexity, and economies of scale required vary significantly across segments of the value chain. These structural differences mean that Europe's opportunities and vulnerabilities are not homogenous but segment specific. This section therefore examines the problems identified in the Commission's Call for Evidence through two distinct lenses:

- Europe's dependence on non-EU countries for leading-edge chips, and
- The preservation of Europe's competitive edge in mainstream and essential semiconductors.

Treating these problems separately reflects the markedly different industrial dynamics, policy levers, and strategic risks associated with each segment of the semiconductor value chain.

2.1. Europe's dependence on non-EU countries for the supply of leading-edge (<10 nm) chips

Europe's continued dependence on non-EU suppliers for the most advanced <10nm chips reflects a deep structural misalignment between the requirements of advanced-node manufacturing and the EU's economic, institutional, and industrial conditions. Activities across the semiconductor value chain demand very different types of inputs: some segments, such as pre-competitive R&D, chip design, and equipment production, are knowledge- and innovation-intensive, whereas others, notably front-end wafer fabrication, are capital- and labour-intensive. As these stages draw on distinct resource endowments, countries tend to specialize where their labour markets, capital availability, and institutional settings allow them to compete more efficiently. Differences in resource intensity therefore play a central role in shaping the global distribution of semiconductor activities (An and Yin, 2025).

The location choices of semiconductor manufacturers are also strongly influenced by proximity to major downstream end-user markets. The U.S. reins in logic chip design (especially those used in ICT and large PCs), East Asian countries dominate memory chip design and assembly, test, and packaging (ATP) operations (fundamental for smartphones and other consumer electronics), while Europe specializes in chips used for automotive and industrial manufacturing, which mirrors its own industrial strengths (An and Yin, 2025).

Finding effective solutions to Europe's dependence on non-EU countries for the supply of leading edge <10 nm chips thus requires understanding structural limits that this demand profile places on Europe's ability to sustain certain areas of production domestically.

First, Europe lacks a large consumer-electronics sector that could generate the scale of logic- and memory-chip demand that anchors such facilities elsewhere. Second, advanced node fabs require massive, continuous throughput to amortise high capital costs. This mismatch is compounded by the extreme capital intensity of front-end fabrication: in 2020, 64% of global semiconductor capital expenditure was concentrated in wafer-fabrication facilities,[1] while combined R&D and capex oscillated around 35% of semiconductor sales between 2021-2023 (SIA, 2025). For more than twenty years, U.S. semiconductor firms have sustained capital expenditures above 10% of sales in

[1] Draghi Report (2024), citing *Capital IQ, 2020. Gartner, 2020.*

nearly every year (except for 2009-2010), and R&D expenditures above 15% of sales for twenty-four consecutive years (SIA, 2025).

The structural demand constraints imply that moving into advanced-node fabrication in Europe would require high volumes of mid- to long-term, high-risk capital. However, Europe's financial system may be not yet be providing the amount of capital and risk-tolerance needed to support such investment at scale, making adaptation necessary if Europe aims to compete in advanced-node fabrication.

Survey data from the EIB (2023) show that access to finance remains a major constraint for EU firms, particularly SMEs, and that European firms rely far more on bank lending than on equity or bond markets. Also, Europeans have important savings, but 31% of EU-27 household assets remain in currency and deposits, compared with 12% in the US, leaving only 35% of savings available for risk-bearing investment, versus 54% in the U.S. (Marcus and Rossi, 2024).[2] This weakens Europe's capacity to mobilise long-term, high-risk capital.

Third, labour market conditions, which also play a relevant role in semiconductor firms' investment decisions, further constrain Europe's competitiveness. Even with subsidies accounted for, Europe's operating cost for a standard mature logic fab are comparable to U.S. levels but significantly higher than those in Taiwan or China, driven by labour costs that are 2-3x higher than in Asia and utility prices that are 2x those in the U.S. Furthermore, European construction timelines (40-50 months to reach volume production) are far slower than Taiwan's 28-32 months, reflecting qualified labour shortages, lower productivity, and protracted timelines for obtaining permits (McKinsey, 2025).

Finally, semiconductor production is also cyclical, characterised by alternating periods of capacity shortages and oversupply. It is thus important to understand the financial impact of cyclical downturn on EU-based facilities. During downturns, when utilisation rates may fall sharply, fabs must absorb substantial fixed costs. These cycles can create strong asymmetric pressures across regions if capital, labour markets and regulatory environments differ significantly in the extent to which they allow flexibility in adjusting capacity utilisation.

Geopolitical analysis reinforces these structural constraints. Wong et al. (2024) show that advanced-node manufacturing operators under a highly cumulative technological regime in which process knowledge, yield optimisation, and organisational learning compound over decades. Leading-edge fabs integrate over 1,000 interdependent process steps and rely on a handful of critical tools, most prominently Dutch ASML's EU lithography machines, that operate as global chokepoints. Latecomers face not only capital constraints but also restricted access to lithography, deposition, inspection equipment and EDA tools due to U.S.-led export controls. Despite

[2] Marcus and Rossi link these financial constraints to deeper EU's system-level weakness: fragmented capital markets, heterogenous national regulation, persistent Single Market fragmentation.

exceptional policy support, China – possessing the world's largest domestic semiconductor market – remains two to three generations behind the global frontier in advanced logic and memory (Grimes, 2022). SMIC's limited progress beyond 28nm and the continued dominance of Taiwan and Korean at <10nm illustrate how first-mover advantages and cumulative tacit knowledge lock in the technological leaders. Taiwanese and Korean firms increasingly pursue a 'high-end at home, lower-end abroad' strategy, maintaining cutting-edge production domestically

All these structural realities underscore why Europe's gap cannot be easily closed through subsidies or isolated national investments. Europe's dependence on non-EU suppliers for <10nm chips is not merely a function of insufficient demand or short-term cost disadvantages; it reflects systemic limitations. Limited domestic demand, insufficient capital-market depth, labour-market rigidity, and the absence of cumulative learning process represent a series of decisive factors that market forces alone cannot overcome.

The structural constraints identified above, however, could be affected and probably alleviated by recent technological trends in advanced-node manufacturing. Even for frontier producers such as TSMC and Samsung, continued 'planar scaling' has entered a phase of sharply diminishing returns. Industry analyses show that node shrinkage in the 5nm, 3nm, and 2nm progression is characterised by escalating current leakage, thermal-management difficulties, more challenging yield control, and increasing per-transistors cost despite non-linear performance gains (Ma et al., forthcoming, 2026). These technological and economic dynamics indicate that the economics of leading-edge logic have fundamentally shifted: the traditional assumption that smaller nodes automatically improve cost-performance ratios no longer holds.

In this context, attempts by latecomers to replicate frontier logic production face not only structural disadvantages but also enter a segment whose cost curve increasingly favours incumbents with deep cumulative process knowledge. Particularly, considering that global innovation trajectories are moving away from pure planar scaling toward 'system-level collaboration': chiplet architecture, 3D stacking, and heterogenous integration capable of delivering performance improvements without relying on ever finer lithography. These developments could enhance Europe's existing comparative advantages in upstream equipment, advanced materials, power electronics, as well as its strong position in system-level integration for automotive and industrial applications. **The technological shift towards system coordination seems to reinforce the argument that Europe's strategy should focus on limited mission-critical access to leading-edge capacity while deepening the technology domains where it already possesses global strengths.**

These technological dynamics have a direct counterpart on the innovation side. Patent-related evidence, explored by CDS research, indicates that semiconductor innovation exhibits the characteristics of a mature and path-dependent technology, with only marginal growth in technological-class diversity over the past decade and innovation activity remaining

predominantly nationally concentrated rather than including international collaborations (Pisarkiewicz et al, 2024). Leadership in the most complex semiconductor classes is held by a small group of long-established incumbents, reinforcing the cumulative capabilities and entrenched advantages described above and further narrowing the scope for latecomers to gain a foothold at the frontier.

Given both the structural constraints identified above and the global shift from planar scaling to system-level integration, Europe should carefully assess its future strategy for developing advanced-node ecosystem that seems to be increasingly uneconomic for latecomers and dominated by incumbents with deep cumulative process knowledge. **A realistic strategy therefore requires coordinated public intervention, strategic financing instruments, close alignment with trusted partners, and an economic-security-driven approach to negotiating long-term guaranteed access to leading-edge capacity.**

2.2. Preserving Europe's competitive edge in mainstream/essential semiconductor industry

Europe retains globally significant strengths in several segments of the mainstream and essential semiconductor value chain: power electronic, analog and mixed-signal devices, microcontrollers, sensors, photonics, and specialized industrial chips. These activities draw on Europe's comparative advantages in R&D-intensive upstream technologies, diversified industrial demand (notably automotive and industrial automation), and deep ecosystems in equipment, materials, and design. The Joint Research Centre (2025) notes that Europe is a net exporter of semiconductor manufacturing equipment, with global leadership in microlithography and mask-making systems, segments that accounted for 30% of worldwide wafer-fabrication equipment sales in 2023 (JRC, 2025). These upstream strengths also underpin the competitiveness of European producers in DOSA (discrete, optoelectronic, sensors, actuators), analog, and microcontroller chips; core inputs for Europe's strategic manufacturing sectors.

Yet, the sustainability of this position is under growing pressure. The Call for Evidence stresses that Europe's competitive edge in mainstream chips is challenged by 'potential non-market policies and practices in third countries' and warns that continuous innovation is required to maintain security-relevant and energy-efficient components.

Several studies point to structural risks in the European industrial chain. Among these studies, Huggins et al. (2023) show that Europe's cluster-based semiconductor industry suffers from fragmented innovation networks and underinvestment in open-innovation capabilities, limiting the scaling of next-generation technologies and constraining the diffusion of R&D between regional clusters such as Leuven, Dresden, Grenoble, and Eindhoven. Poitiers and Weil (2021) argue that EU policy remains overly focused on advanced-node fabrication, despite Europe's

limited domestic demand for leading-edge logic and its clear strengths in equipment, materials, and mid-range manufacturing; they warn that diverting public resources towards costly advanced fabs risks weakening Europe's competitive position in the mainstream segments where it already leads.

Additional vulnerabilities arise from global demand shifts and supply-chain exposure. JRC data show that European end-users depend heavily on imports for certain memory and logic components, with limited substitutability from domestic production; at the same time, the highest share of chip segments to Europe goes to the automotive and industrial sectors (37%), both structurally reliant on mainstream technologies. Xiong et al. (2025) highlight that global shocks (pandemics, geopolitical tensions, and bottlenecks in ATP and materials) disproportionately affect mature-node chips, which often have single-sourced supply chains and long recovery times, increasing Europe's exposure to disruptions in Asia-centred ATP networks.

While an EU-level chips strategy is indispensable, its effectiveness ultimately depends on fully understanding the heterogeneity of structural weaknesses that exist within individual Member States. As Pierleoni (2023) notes for the Italian case, a significant limitation is the shortage of large-scale applied-research centres. This challenge is not unique to Italy. Some recent national assessments, such as Poland's 2025 semiconductor Strategy (Polish Ministry of Digital Affairs, 2025) similarly highlight gaps in front-end and back-end infrastructure, limited pilot-line capacity, and fragmented national data on semiconductor capabilities, despite areas of excellence in design, photonics, and materials. Recognising these heterogenous national constraints is essential for designing a long-term European chips strategy that strengthens Europe's collective capabilities while supporting Member States in overcoming existing deficits that impede the emergence of a competitive European semiconductor ecosystem.

A forward-looking strategy, therefore, suggests to concentrate policy and resources with the aim to reinforce Europe's long-term comparative advantages in the areas of consolidated excellence.

2.3. Supply-chain resilience and economic-security risks: mapping and monitoring tools

The current monitoring framework under the Chips Act remains limited in its capacity to provide the EU with continuous, granular insights into vulnerabilities across the semiconductor supply chain. As the Court of Auditors (April 2025) notes, although the Chips Act mandates a strategic mapping of Europe's strengths and weaknesses (Article 19) and monitoring (Article 20), it did not include a clear timetable for the implementation of these actions. Preparatory work began only after the Act's entry into force in September 2023, and its operationalization depends on external technical expertise that seems to not have yet been procured at the time of the audit (Court of Auditors, 2025, para. 85). However, the importance of the assessment contained in the JRC Report

'EU's strengths and weaknesses in the global semiconductor sector' published in March 2025 must be mentioned in this regard.[3]

Another gap concerns the Commission's limited visibility over public and private investments. Financial support for semiconductors flows through a wide range of EU and national channels (EU Horizon programmes, ESIF, InvestEU, EFSI, EIB lending, national grants, tax incentives, and the Recovery and Resilience Facility; Court of Auditors, 2025, para. 36). Yet, the Commission cannot form a complete picture of total funding, because Member State contributions and private investment decisions are only partially visible, and many funding streams fall outside the Commission's direct oversight (Court of Auditors, 2025, paras. 37-40).

This visibility gap extends to implementation. The Commission does not receive systematic reporting on FOAK or IPCEI projects. It had limited information on semiconductor-relevant projects for the 2014-2020 period (Court of Auditors, 2025, para. 63). Although DG CNECT's involvement in state-aid assessments increased in the 2021-2027 cycle (para. 64), there are still no requirements for national authorities or beneficiaries to report progress or results to the Commission (para. 66). For the Chips Act itself, information on expected FOAK investment is derived largely from "press releases, negotiations underway, and notifications from national authorities" (para. 45). This leaves the Commission without structured, recurrent access to information that would allow it to monitor risks in real time or assess how State-aid-funded projects and new manufacturing investments contribute to resilience.

Furthermore, the report highlights several geopolitical and regulatory risks that affect the EU's access to critical technologies and materials and therefore fall squarely within the economic-security concerns that a monitoring system should capture. Geopolitical tensions, including Russia's war of aggression against Ukraine, have already disrupted supplies of neon gas essential for lithography (para. 109). Export controls imposed by third countries may "limit access to critical materials and advanced technology" (para. 110), raising costs and delaying access to key equipment. Negotiations on such export controls often occur at the Member States rather than EU level. The recent example of the United States, pressuring the Netherlands to restrict ASML's exports to China, well illustrates how external decisions can directly affect the EU's technological position.

Although the Call for Evidence does not explicitly refer to risks such as intellectual property theft, forced technology transfer, or economic espionage, these forms of unauthorized diffusion of know-how fall squarely within the broader category of vulnerabilities that the Commission seeks to address through enhanced monitoring and economic-security analysis. The Chips Act Regulation itself recognises in recitals 27 and 43 "practices aiming to misappropriate confidential information, trade secrets, and protected data, such as IP theft, forced technology transfers and

[3] See also OECD (2023), Vulnerabilities in the semiconductor supply chain.

economic espionage" as a threat to Europe's R&D efforts. In segments where Europe retains critical strengths (particularly equipment, materials, power semiconductors, sensors, and photonics) or is heavily investing to develop new ones, unauthorized transfer of know-how would erode or put at risk Europe's competitive edge and conversely deepen strategic dependencies on non-EU suppliers. In this regard, it is worth to point out that the SCAN methodology used to map trade dependencies (JRC, 2023, 2025), while useful at the product level, is not designed to detect vulnerabilities linked to proprietary process technologies or exposure of strategic intellectual assets. Also, as the authors of the report themselves emphasise, customs classifications used in the SCAN methodology suffer from several limitations, including limited granularity and noise information that lead to potential challenges when interpretating the data.

Addressing the variety of risks faced by the semiconductors ecosystem requires a monitoring framework that is not only sufficiently granular, continuous and coordinated across Member States, but also capable of integrating multiple forms of vulnerability: supply-chain disruptions, chokepoints in materials and equipment, exposure of proprietary process technologies, and the impact of foreign direct investment and merger-related remedies. Crucially, as the JRC (2025) underscores, such a framework depends on systematic input from field experts to validate product relevance, and on structured cooperation with Member States to ensure comprehensive coverage of the value chain.

For example, competence centres (Article 11 of the Chips Act) could play a structured role in addressing existing intelligence gaps. Their technical expertise, proximity to industry, and ability to gather specialised knowledge communities could allow them, if adequately equipped, to support the Commission and Member States in validating SCAN-based mappings and interpreting technological developments that are not captured by trade data. If integrated into a formal monitoring architecture, with clearly defined analytical tasks, reporting channels, and confidentiality safeguards, competence centres could contribute to the continuous, more granular technical insight required to assess supply-chain choke points, technology leakage risks, and emerging sights in the semiconductor landscape.

The weaknesses of the current monitoring framework also seem to contrast with two examples of EU oversight regimes in other critical sectors, where the EU has imposed compulsory, structured, and recurrent data-gathering duties on private actors for the purpose of risk monitoring, market surveillance, and crisis-response; functions closely aligned with what a reinforced Chips Act may require:

- In energy markets, the REMIT Regulation obliges all wholesale market participants to provide standardized, continuous transaction-level data to ACER for real-time market integrity surveillance. (See Regulation EU No. 1227/2011 on wholesale energy market integrity and transparency (REMIT), Articles 4, 7, 8, REMIT Annual Report).

- Under the Critical Raw Materials Act, large companies manufacturing strategic technologies must provide supply-chain, risk exposure, and supplier-concentration data to the Commission on a compulsory and recurring basis. The mechanism is explicitly framed as an early-warning economic-security tool and allows the Commission to request data from specific firms when supply-risk conditions emerge. See Regulation (EU) 2024/1252, Articles 20-23.

These frameworks demonstrate that when systemic risks and cross-border interdependencies justify intervention, the EU already operates by creating binding and enforceable data collection architectures.

Drawing on Article 24 of the Critical Raw Materials Act, the revised Chips Act could introduce a proportionate, company-level risk-preparedness obligation for large and strategic firms in the semiconductors supply and value chain. Periodic assessments of the critical semiconductor dependencies would provide the Commission and Member States with structured and recurring insights. Any obligation should be designed to avoid undue administrative burden - applying only to firms whose scale and/or systemic relevance justify such reporting - respect existing corporate risk-management processes and remain strictly proportionate.

Finally, beyond addressing present-day supply-chain vulnerabilities, an effective monitoring must incorporate a structured horizon-scanning function, similar to the exercise carried out by the UK CMA (2023) in its Trends in Digital Markets: A CMA Horizon Scanning Report. Semiconductors evolve along technological trajectories where critical inflection points, such as breakthroughs in patterning, materials, or lithography, can rapidly alter cost structures, competitive positions, and the geographical distribution of manufacturing. For example, Hung (2024) discusses innovations such as multiple patterning or potential particle-accelerator-based lithography, which seem to have the capacity to reshape future lithography roadmaps and shift chokepoints within the value chain, directly affecting Europe's strategic strengths in equipment and advanced materials. Without a forward-looking analytical capability, the EU risks basing policy on today's bottlenecks while missing emerging technological transitions that could determine future dependence or competitiveness. Integrating 'horizon scanning' methodologies into the Chips Act monitoring architecture would therefore align with the economic-security objectives, identified by the Court of Auditors, filling the current gap between reactive crisis-oriented data collection and the anticipatory intelligence required to guide long-term strategic investment, supply-chain resilience planning, and capability development.

In summary, the current monitoring system is fragmented, incomplete, and overly dependent on voluntary or ad hoc information flows. **A revised Chips Act should therefore establish continuous, proportionate, and compulsory data collection, integrated with early-warning indicators and a horizon-scanning capability.** Only with an efficient, complete, and mandatory

information tool can the EU aim to anticipate supply shocks, evaluate the effects of public investment, identify emerging technologies and their impact on the current supply chain, and support a durable and strategic semiconductor policy framework.

3. Assessment of the Commission's policy options

The Call for Evidence presents two distinct options for the revision of the Chips Act. Their feasibility and desirability depend on Europe's structural position in the semiconductor value chain and the shortcomings identified in the current framework. The CDS considers that each option addresses parts of the problem, but their effectiveness diverges substantially given economic, institutional, and geopolitical constraints.

3.1. Option 1: Maintaining the current framework

Under this option, the regulatory structure and the state-aid principles established in the Chips Act would be preserved, without additional investments from the EU or enhanced mandatory monitoring regime. Data gathering from private actors would remain voluntary (except in crisis situations under Article 25 in relation to Article 23).

Option 1 risks preserving the weaknesses already identified (limited impact on leading-edge dependence, insufficient monitoring capability, and a strategic framework too weak to guide future interventions). Also, evidence from the Court of Auditors confirms that the current voluntary and fragmented data-gathering system leaves the Commission without the complete information set needed to implement the Act effectively. Under Option 1, these structural deficiencies would remain unaddressed.

3.2. Option 2: Targeted amendments to the Chips Act

This option would amend the Chips Act Regulation to (i) elevate the strategic nature of both leading-edge and legacy manufacturing; (ii) define strategic projects and selection criteria; (iii) expand future funding possibilities beyond State aid, and (iv) introduce enhanced, potentially mandatory, data-gathering tools for resilience and economic-security monitoring.

- ***Greater realism and strategic coherence:*** Unlike Option 1, this solution seems to better reflect that Europe's vulnerabilities extend beyond dependence in terms of leading-edge chips to critical legacy nodes. A revised Act that would foresee strategic projects could

focus support where Europe has a plausible comparative advantage and avoid misallocation toward structurally uncompetitive advanced node fabs.

- **Scope for differentiated interventions:** Option 2 explicitly allows for tailored instruments, from small-scale, security-oriented production for defence, space, and automotive, to (where justified) participation in high-volume advanced-node projects. This flexibility aligns with the CDS' view that Europe's requirements for leading-edge chips are mission-critical, and sector-specific, but most importantly relatively low-volume, and hence largely incompatible with a purely commercial big foundry model. The case for Option 2 is further reinforced by the market heterogeneity of national semiconductor ecosystems, briefly recalled in section 2.2. A framework built around strategic projects and differentiated instruments is therefore better suited to Europe's existing heterogeneity.
- **Strengthening monitoring and economic-security intelligence:** Introducing improved, potentially mandatory, data collection could be a significant impactful improvement as it would address the core weakness identified throughout section 2.3: the absence of continuous, structured, and Member-State-integrated intelligence necessary for resilience and economic-security assessments.

Option 2, therefore, seems to be more suitable for correcting the structural weaknesses identified in the current Chips Act.

4. CDS Recommendations

The revision of the Chips Act should strengthen Europe's semiconductor strategy by combining greater industry initiative with more strategically targeted public intervention. Europe's semiconductor capabilities must be developed not in isolation but as part of a broader, layered digital ecosystem: from raw materials and energy, through chips, networks, connected devices, cloud infrastructure, software, data, and AI. Strengthening any one layer depends on coordinated progress across the others. This perspective, which illustrates the vast need for future investment, reinforces the view that while Europe must enable its industry to act with greater autonomy and ambition, public resources must be deployed where market forces alone cannot deliver the necessary capabilities.

Our recommendations are threefold:

First, the revised Chips Act should adopt a realistic approach to leading-edge logic. A credible European strategy for advanced nodes must be grounded in the structural realities that have shaped the evolution of the global semiconductor supply and value chain. As section 2.1. explained, successful participation in leading-edge manufacturing depends on cumulative process know-how, high-volume demand, specialised labour, deep capital markets, and secure access to

critical materials and tools. Investment in advanced nodes is possible, but only if it is paired with an industrial and economic-security strategy that addresses these underlying conditions, builds the necessary complementary capabilities, and secures strategic partnerships that mitigate structural constraints. **A revised Chips Act should therefore support advanced-node investments only where technically and economically justified, while ensuring that they are embedded in a broader strategic framework that reflects the full complexity of leading-edge manufacturing.**

Second, as discussed in Section 2.2, a revised Chips Act should explicitly recognise the heterogeneity of national semiconductor ecosystems, so that public resources (both national and EU) can be deployed more effectively. Deploying Chips Act instruments aligning them with these heterogenous conditions would ensure that funding, state aid, and EU-level support reinforce national strengths and avoid distributing resources thinly across areas where complementary capabilities are missing and where their development requires substantial investment over a sustained period of time. **In particular, an effective and forward-looking strategy should concentrate available EU resources, and guide member states efforts, towards the areas where Europe's long-term comparative advantages are at the same time strategic and realistic.**

Third, a revised Chips Act should establish a structured, proportionate, and compulsory EU-level data-gathering framework. As discussed in Section 2.3., voluntary reporting has left the Commission without the complete information required for risk assessment, investment monitoring, or crisis preparedness. Drawing on mechanisms foreseen by the REMIT and the Critical Raw Materials Act, the improved monitoring framework could integrate SCAN-based mapping, with firm-level reporting for large and strategically relevant actors, complemented by structured cooperation with Member States and competence centres. **Without an improved mapping and monitoring framework, other policy interventions risk being misaligned or misallocated.**

The overarching message is that Europe's semiconductor policy must combine a more active industry with a more strategic state. Industry must act, and must be enabled to act, but public resources must be directed where they can have the greatest impact, informed by a much clearer picture of Europe's and its Member State's position in the global value chain, and by a monitoring framework capable of informing long-term strategic decisions rather than simply reacting to crises.

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