Policy suggestions for the EU Chips ACT 2.0

University of Zurich – November 2025

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The implementation of the first EU Chips Act has marked an essential turning point for Europe's semiconductor landscape, providing long-awaited political momentum and enabling the first steps toward industrial consolidation. The establishment of the European Semiconductor Manufacturing Company (ESMC), jointly backed by Infineon, NXP, Bosch and TSMC, represents a decisive step toward rebuilding advanced fabrication capabilities on European soil. Yet despite this progress, the measures enacted so far remain insufficient to secure the European Union's strategic objective of reaching 20% global market share by 2028 and ensuring the long-term resilience of its semiconductor supply chains. With private-sector projects facing postponements or cancellations—including Intel's planned investments in France and Germany—alongside uncertainty regarding STMicroelectronics' long-term European employment footprint and the progressive decline of legacy manufacturing capacity such as NXP's Nijmegen line, Europe's semiconductor ecosystem remains fragile, fragmented, and incomplete.

A central reason for this fragility is that, unlike commercial aircraft manufacturing where the Airbus model succeeded through the production of a standardized, certifiable product with naturally stable demand, the semiconductor sector is intrinsically heterogeneous. Its products vary across applications, lifecycles are short, and innovation cycles are rapid. Capacity alone does not generate demand. Unlike aviation, where political coordination was sufficient to secure long-term orders, semiconductor manufacturing requires deliberate, structured mechanisms to channel European research, design activity, industrial needs, and public procurement toward domestic fabrication. Without such demand-shaping interventions, the capacity created under Chips Act 1 risks underutilization.

In this context, the University of Zurich proposes an integrated set of actions intended to structure the next phase of the Chips Act and to ensure that research, infrastructure, workforce development, and industrial activity evolve not independently but as a coordinated ecosystem. A first component is the establishment of regular multi-project wafer (MPW) research runs within ESMC at mature technology nodes. Although the planned 12–10 nm capability at the Dresden facility is of high strategic value, innovation across Europe depends predominantly on accessible production at 135, 80, 65 and 28 nm nodes, where most mixed-signal, power, automotive and industrial electronics are still manufactured. Integrating quarterly MPW runs and developing open-source PDKs modeled

on the SkyWater approach would allow universities, SMEs and research groups to prototype rapidly while cultivating a broad and sustainable design ecosystem. To reinforce this integration, EU-funded research projects—particularly ERC, Pathfinder and Synergy grants involving semiconductor design or fabrication—should be required to use European manufacturing infrastructure whenever technically feasible. Such alignment is a crucial mechanism for generating the structured, predictable demand that purely market-driven conditions cannot provide.

A further long-term strategic imperative is consolidating a fully European semiconductor supply chain covering substrate and wafer production, post-processing, packaging and testing. While such a distributed supply chain is more complex than the geographically dense clusters that dominate in East Asia, it is nonetheless achievable under an Airbus-style governance framework—provided that the EU actively engineers the necessary demand and coordination mechanisms. Relocating vulnerable supply-chain segments to or initiating them within Europe, with particular attention to underrepresented northern or southern European member states with strong industrial capacity, would substantially enhance resilience. Defence procurement should likewise be aligned with Europe's semiconductor strategy, with a requirement that at least a portion of defence-related integrated circuits be produced domestically. A phased approach beginning with low-complexity components would enable manageable technology transfer while strengthening security of supply and guaranteeing baseline orders for domestic facilities.

Reform of EUROPRACTICE is also necessary. Its longstanding role as an intermediary for commercial EDA tool licensing must evolve into a broader function as a design-knowledge hub supporting open-source toolchains. Rather than directing public funds toward commercial license agreements, the European research community would benefit from engineering support, shared expertise, and educational frameworks enabling students and SMEs to adopt open EDA flows. Complementing this shift, the development of open PDKs should be systematically supported through zero-cost MPW runs for open designs, allowing early-stage innovators to transition from conceptual work to manufacturable prototypes without prohibitive financial barriers. These measures directly expand the base of designers who can realistically bring work into European fabs, thereby contributing to the sustained demand that such facilities require.

Further lowering entry barriers will require advances in automation. Europe should encourage the development of AI-assisted IC design tools capable of translating higher-level descriptions into manufacturing-compatible layouts using open PDKs. Although full automation of RTL-to-GDS flows is not yet mature, partial automation can already broaden access to semiconductor design across academic and industrial domains, helping to

generate the design activity needed to sustain a diverse user base. In parallel, Chips Act 2.0 must address the persistent shortage of skilled fab operators by subsidizing apprenticeships and technician training programs, especially in lithography, etching, deposition, implantation and packaging. Such skills are indispensable and cannot be replaced easily by automation, making them crucial for operational stability and manufacturing yield.

A final strategic dimension concerns cryogenic electronics, which have become essential components of quantum sensing and quantum computing systems. Although the EU has invested heavily in quantum hardware through initiatives such as Quantum Flagship and IPCEI Quantum, the development of cryogenic CMOS electronics remains insufficiently supported. Chips Act 2.0 should therefore subsidize the development and fabrication of cryo-optimized circuits, in particular leveraging the GlobalFoundries 65 nm platform, which already possesses device models suitable for temperatures down to a few kelvin. Integrating such capabilities with ESMC and European quantum research consortia—and establishing MPW runs dedicated to cryogenic applications—would ensure that Europe retains leadership in quantum science while developing industrial capabilities that are otherwise emerging predominantly in the United States and East Asia. This represents yet another domain where demand must be deliberately shaped: quantum technologies will not naturally gravitate toward European fabs unless the necessary incentives and infrastructure are in place.

Collectively, these measures would help ensure that Europe's semiconductor ecosystem becomes more resilient, more integrated, and more strategically aligned with long-term scientific and industrial needs. Crucially, they move beyond the supply-side logic of the first Chips Act—where capacity was created but demand left largely uncoordinated—and instead establish the foundation for a sustainable, self-reinforcing semiconductor value chain. They respond to systemic weaknesses in the current industrial landscape and offer concrete pathways for securing technological sovereignty while enabling research and innovation to flourish within a European manufacturing infrastructure.