2:1 MULTIPLEXER IN CMOS TRANSMISSION GATE

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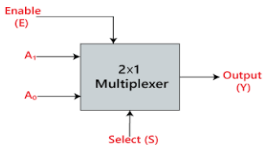
Abstract— A multiplexer, sometimes known as a "mux," is a device that chooses one of several input signals. It is a circuit with combinational logic. It is utilised in applications where data needs to be switched from numerous sources to a destination and is a unidirectional device. In this study, various 2:1 Multiplexer Structures are simulated, compared, and applied to a 1 bit full adder cell. The factors considered include power supply voltage, operation frequency, temperature, and area efficiency. Tanner EDA tool has performed all simulations on BSIM 3V3 90nm technology. General terms Speed, Power-delay product, and 2:1 multiplexer.

DESCRIPTION

Today's electronics sector has made low power a central feature. Power dissipation has changed significantly as a result of the requirement for low power, becoming just as crucial a factor as performance and size. The "switch logic fundamental "'s building piece is a 2:1 multiplexer.

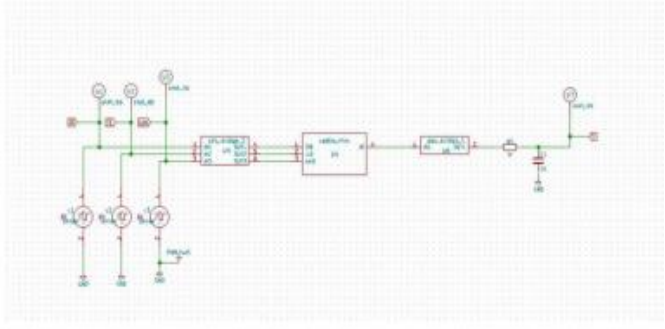


The idea behind switch logic is that rather of using logic gates, logic circuits are implemented as combinations of switches. As programmable logic devices, multiplexers are utilised in the construction of digital semiconductors like CPUs and graphics controllers, in telecommunications, in computer networks, and in digital video. The area efficiency of the circuit, power dissipation, speed, operating frequency range, and temperature dependence of the various 2:1 multiplexer circuits are compared in this research.

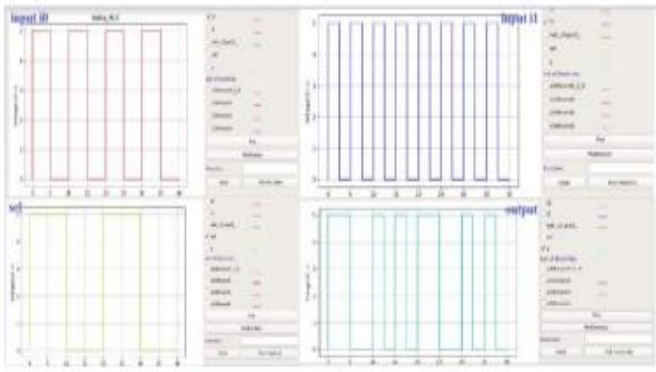
CIRCUIT DETAILS:

Multiplexer (MUX) is a data selector which will send single input data at the output based on select line input. Here we have implemented a 2:1 MUX which has 2 inputs (A and B), 1 output (Y) and 1 select line (S). Output Y will be A or B based on 0 or 1 input at the select line (S). If the select line is “0” output Y will be A and if the select line is “1” then output Y will be B. 2:1. The equation for output Y will be Y=AS^BAR + BS. The complete design is divided into two parts Digital Block and Analog Block. Here, we will be using Verilog Hardware Description Language for implementation. We will implement the code using Makerchip software and implement the Circuit schematic using esim software. We know that mixed signals contain both analog and digital blocks hence we need ADC and DAC blocks to convert the signals from analog to digital. Figure 1 shows the final circuit diagram designed using esim software and Figure 2 shows final circuit waveform containing 4 waveforms 2 inputs, select line and output. In the Circuit Waveform, we will verify the above implementation using clock pulse. Output Y will have the same clock pulse sequence as A when S will be “0” and it will have the same clock pulse sequence as B when S will be “1”.

FINAL CIRCUIT DIAGRAM



FINAL CIRCUIT WAVEFORM



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