Universal Serial Bus Type-C Cable and Connector Specification

Release 2.0
August 2019

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

通用串行总线 Type-C 电缆和连接器规范

2019 年 8 月
发布 2.0 版

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Copyright © 2014-2019, USB 3.0 Promoter Group:
Apple Inc., Hewlett-Packard Inc., Intel Corporation, Microsoft Corporation, Renesas, STMicroelectronics, and Texas Instruments
All rights reserved.

NOTE: Adopters may only use the USB Type-C® cable and connector to implement USB or third party functionality as expressly described in this Specification; all other uses are prohibited.

LIMITED COPYRIGHT LICENSE: The USB 3.0 Promoters grant a conditional copyright license under the copyrights embodied in the USB Type-C Cable and Connector Specification to use and reproduce the Specification for the sole purpose of, and solely to the extent necessary for, evaluating whether to implement the Specification in products that would comply with the specification. Without limiting the foregoing, use of the Specification for the purpose of filing or modifying any patent application to target the Specification or USB compliant products is not authorized. Except for this express copyright license, no other rights or licenses are granted, including without limitation any patent licenses. In order to obtain any additional intellectual property licenses or licensing commitments associated with the Specification a party must execute the USB 3.0 Adopters Agreement. NOTE: By using the Specification, you accept these license terms on your own behalf and, in the case where you are doing this as an employee, on behalf of your employer.

INTELLECTUAL PROPERTY DISCLAIMER

THIS SPECIFICATION IS PROVIDED TO YOU "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE. THE AUTHORS OF THIS SPECIFICATION DISCLAIM ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OR IMPLEMENTATION OF INFORMATION IN THIS SPECIFICATION. THE PROVISION OF THIS SPECIFICATION TO YOU DOES NOT PROVIDE YOU WITH ANY LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS.

All implementation examples and reference designs contained within this Specification are included as part of the limited patent license for those companies that execute the USB 3.0 Adopters Agreement.

USB Type-C®, USB-C® and USB4™ are trademarks of the Universal Serial Bus Implementers Forum (USB-IF). DisplayPort™ is a trademark of VESA. All product names are trademarks, registered trademarks, or service marks of their respective owners.

Thunderbolt™ is a trademark of Intel Corporation. You may only use the Thunderbolt™ trademark or logo in conjunction with products designed to this specification that complete proper certification and executing a Thunderbolt™ trademark license – see usb.org/compliance for further information.

版权所有 © 2014-2019，USB 3.0 推广组织：Apple Inc.、Hewlett-Packard Inc.、Intel Corporation、Microsoft Corporation、Renesas、STMicroelectronics 和 Texas Instruments 保留所有权利。

注意：采用者只能使用 USB Type-C® 电缆和连接器来实现本规范中明确描述的 USB 或第三方功能；禁止所有其他用途。

有限版权许可：USB 3.0 推广者根据 USB Type-C 电缆和连接器规范所体现的版权授予有条件版权许可，以仅用于评估是否在符合规范的产品中实施规范的目的和必要范围内使用和复制规范。在不限制上述条款的情况下，不得将规范用于提交或修改任何专利申请以针对规范或符合 USB 规范的产品。除此明确版权许可外，不授予任何其他权利或许可，包括但不限于任何专利许可。为了获得与规范相关的任何其他知识产权许可或许可承诺，一方必须执行 USB 3.0 采用者协议。注意：通过使用规范，您代表自己接受这些许可条款，如果您以员工身份这样做，则代表您的雇主接受这些许可条款。

知识产权免责声明

本规范“按原样”提供给您，不附带任何担保，包括对适销性、非侵权或适用于任何特定用途的任何担保。本规范的作者拒绝承担与使用或实施本规范中的信息有关的所有责任，包括侵犯任何专有权利的责任。向您提供本规范并不表示以明示或暗示、禁止反言或其他方式向您提供任何知识产权的许可。

本规范中包含的所有实施示例和参考设计均属于执行 USB 3.0 采用者协议的公司的有限专利许可的一部分。

USB Type-C®、USB-C® 和 USB4™ 是通用串行总线实施者论坛 (USB-IF) 的商标。DisplayPort™ 是 VESA 的商标。所有产品名称均为其各自所有者的商标、注册商标或服务标志。

Thunderbolt™ 是英特尔公司的商标。您只能将 Thunderbolt™ 商标或徽标与按照此规范设计且已完成适当认证并执行 Thunderbolt™ 商标许可的产品结合使用 - 请参阅 usb.org/compliance 了解更多信息。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

CONTENTS

Specification Work Group Chairs / Specification Editors 16
Specification Work Group Contributors 16
Pre-Release Draft Industry Reviewing Companies That Provided Feedback 22
Revision History 22
1 Introduction 23
1.1 Purpose 23
1.2 Scope 23
1.3 Related Documents 24
1.4 Conventions 24
1.4.1 Precedence 24
1.4.2 Keywords 24
1.4.3 Numbering 25
1.5 Terms and Abbreviations 25
2 Overview 30
2.1 Introduction 30
2.2 USB Type-C Receptacles, Plugs and Cables 31
2.3 Configuration Process 32
2.3.1 Source-to-Sink Attach/Detach Detection 33
2.3.2 Plug Orientation/Cable Twist Detection 33
2.3.3 Initial Power (Source-to-Sink) Detection and Establishing the Data (Host-to-Device) Relationship 33
2.3.4 USB Type-C VBUS Current Detection and Usage 34
2.3.5 USB PD Communication 35
2.3.6 Functional Extensions 35
2.4 VBUS 35
2.5 VCONN 36
2.6 Hubs 36
3 Mechanical 37
3.1 Overview 37
3.1.1 Compliant Connectors 37
3.1.2 Compliant Cable Assemblies 37
3.1.3 Compliant USB Type-C to Legacy Cable Assemblies 37
3.1.4 Compliant USB Type-C to Legacy Adapter Assemblies 38
3.2 USB Type-C Connector Mating Interfaces 39
3.2.1 Interface Definition 39
3.2.2 Reference Designs 61
3.2.3 Pin Assignments and Descriptions 68
3.3 Cable Construction and Wire Assignments 69
3.3.1 Cable Construction (Informative) 69
3.3.2 Wire Assignments 71
3.3.3 Wire Gauges and Cable Diameters (Informative) 72

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

内容

规范工作组主席/规范编辑 ..... 16 规范工作组贡献者 ..... 16 提供反馈的预发布草案行业评审公司 ..... 22 修订历史 22

1 引言 ..... 23 1.1 目的 ..... 23 1.2 范围 ..... 23 1.3 相关文件 ..... 24 1.4 约定 24

1.4.1 优先级 24
1.4.2 关键字 24
1.4.3 编号 25
1.5 术语和缩写 25
2 概述 30
2.1 简介 ..... 30 2.2 USB Type-C 插座、插头和电缆 31
2.3 配置过程 ..... 32 2.3.1 源到接收器连接/断开检测 ..... 33 2.3.2 插头方向/电缆扭曲检测 ..... 33 2.3.3 初始电源（源到接收器）检测和建立数据（主机到设备）关系 ..... 33 2.3.4 USB Type-C VBUS 电流检测和使用 ..... 34 2.3.5 USB PD 通信 ..... 35 2.3.6 功能扩展 ..... 35 2.4 VBUS ..... 35 2.5 VCONN ..... 36 2.6 集线器 36

3 机械 37
3.1 概述 ..... 37 3.1.1 兼容连接器 ..... 37 3.1.2 兼容电缆组件 ..... 37 3.1.3 兼容 USB Type-C 转传统电缆组件 ..... 37 3.1.4 兼容 USB Type-C 转传统适配器组件 ..... 38 3.2 USB Type-C 连接器配接接口 ..... 39 3.2.1 接口定义 ..... 39 3.2.2 参考设计 ..... 61 3.2.3 引脚分配和说明 ..... 68 3.3 电缆结构和电线分配 ..... 69 3.3.1 电缆结构（参考） ..... 69 3.3.2 电线分配 ..... 71 3.3.3 线规和电缆直径（参考） 72

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.4 Standard USB Type-C Cable Assemblies 74
3.4.1 USB Full-Featured Type-C Cable Assembly 74
3.4.2 USB 2.0 Type-C Cable Assembly 75
3.4.3 USB Type-C Captive Cable Assemblies 76
3.5 Legacy Cable Assemblies 76
3.5.1 USB Type-C to *USB 3.1* Standard-A Cable Assembly 77
3.5.2 USB Type-C to *USB 2.0* Standard-A Cable Assembly 78
3.5.3 USB Type-C to *USB 3.1* Standard-B Cable Assembly 79
3.5.4 USB Type-C to *USB 2.0* Standard-B Cable Assembly 80
3.5.5 USB Type-C to *USB 2.0* Mini-B Cable Assembly 81
3.5.6 USB Type-C to *USB 3.1* Micro-B Cable Assembly 82
3.5.7 USB Type-C to *USB 2.0* Micro-B Cable Assembly 84
3.6 Legacy Adapter Assemblies 85
3.6.1 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly 85
3.6.2 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly 87
3.7 Electrical Characteristics 88
3.7.1 Raw Cable (Informative) 88
3.7.2 USB Type-C to Type-C Passive Cable Assemblies (Normative) 89
3.7.3 Mated Connector (Informative – USB 3.2 Gen2 and USB4 Gen2) 108
3.7.4 Mated Connector (Normative – USB4 Gen3) 112
3.7.5 USB Type-C to Legacy Cable Assemblies (Normative) 113
3.7.6 USB Type-C to USB Legacy Adapter Assemblies (Normative) 117
3.7.7 Shielding Effectiveness Requirements (Normative) 119
3.7.8 DC Electrical Requirements (Normative) 122
3.8 Mechanical and Environmental Requirements (Normative) 125
3.8.1 Mechanical Requirements 126
3.8.2 Environmental Requirements 131
3.9 Docking Applications (Informative) 132
3.10 Implementation Notes and Design Guides 133
3.10.1 EMC Management (Informative) 133
3.10.2 Stacked and Side-by-Side Connector Physical Spacing (Informative) 136
3.10.3 Cable Mating Considerations (Informative) 136
4 Functional 138
4.1 Signal Summary 138
4.2 Signal Pin Descriptions 138
4.2.1 SuperSpeed USB Pins 138
4.2.2 USB 2.0 Pins 139
4.2.3 Auxiliary Signal Pins 139
4.2.4 Power and Ground Pins 139
4.2.5 Configuration Pins 139
4.3 Sideband Use (SBU) 139
4.4 Power and Ground 140
4.4.1 IR Drop 140

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.4 标准 USB Type-C 电缆组件 ..... 74 3.4.1 USB 全功能 Type-C 电缆组件 ..... 74 3.4.2 USB 2.0 Type-C 电缆组件 ..... 75 3.4.3 USB Type-C 固定电缆组件 ..... 76 3.5 传统电缆组件 ..... 76 3.5.1 USB Type-C 至 *USB 3.1* 标准 A 电缆组件 ..... 77 3.5.2 USB Type-C 至 *USB 2.0* 标准 A 电缆组件 ..... 78 3.5.3 USB Type-C 至 *USB 3.1* 标准 B 电缆组件 ..... 79 3.5.4 USB Type-C 至 *USB 2.0* 标准 B 电缆组件 ..... 80 3.5.5 USB Type-C 至 *USB 2.0* Mini-B 电缆组件 ..... 81 3.5.6 USB Type-C 至 *USB 3.1* Micro-B 线缆组件 ..... 82 3.5.7 USB Type-C 至 *USB 2.0* Micro-B 线缆组件 ..... 84 3.6 传统适配器组件 ..... 85 3.6.1 USB Type-C 至 *USB 3.1* 标准 A 型插座适配器组件 85 3.6.2 USB Type-C 至 *USB 2.0* Micro-B 型插座适配器组件 ..... 87 3.7 电气特性 ..... 88 3.7.1 原始线缆（参考） ..... 88 3.7.2 USB Type-C 至 Type-C 无源线缆组件（规范性） ..... 89 3.7.3 配对连接器（参考 - USB 3.2 Gen2 和 USB4 Gen2） 108 3.7.4 配对连接器（规范性 - USB 4 Gen3） ..... 112 3.7.5 USB Type-C 转传统电缆组件（规范性） ..... 113 3.7.6 USB Type-C 转 USB 传统适配器组件（规范性） ..... 117 3.7.7 屏蔽效能要求（规范性） ..... 119 3.7.8 直流电气要求（规范性） ..... 122 3.8 机械和环境要求（规范性） ..... 125 3.8.1 机械要求 ..... 126 3.8.2 环境要求 ..... 131 3.9 对接应用（信息性） ..... 132 3.10 实施说明和设计指南 ..... 133 3.10.1 EMC 管理（信息性） ..... 133 3.10.2 堆叠和并排连接器物理间距（参考） ..... 136 3.10.3 电缆配接注意事项（参考） 136

4功能..... 138 4.1 信号摘要 ..... 138 4.2 信号引脚说明 ..... 138 4.2.1 超高速 USB 引脚 ..... 138 4.2.2 USB 2.0 引脚 ..... 139 4.2.3 辅助信号引脚 ..... 139 4.2.4 电源和接地引脚 ..... 139 4.2.5 配置引脚 ..... 139 4.3 边带使用 (SBU) ..... 139 4.4 电源和接地 ..... 140 4.4.1 IR 压降..... 140

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.4.2 VBUS ... 141
4.4.3 VCONN ... 143
4.5 Configuration Channel (CC) ... 147
4.5.1 Architectural Overview ... 147
4.5.2 CC Functional and Behavioral Requirements ... 161
4.5.3 USB Port Interoperability Behavior ... 197
4.6 Power ... 216
4.6.1 Power Requirements during USB Suspend ... 217
4.6.2 VBUS Power Provided Over a USB Type-C Cable ... 218
4.7 USB Hubs ... 224
4.8 Power Sourcing and Charging ... 224
4.8.1 DFP as a Power Source ... 224
4.8.2 Non-USB Charging Methods ... 227
4.8.3 Sinking Host ... 227
4.8.4 Sourcing Device ... 227
4.8.5 Charging a System with a Dead Battery ... 227
4.8.6 USB Type-C Multi-Port Chargers ... 228
4.9 Electronically Marked Cables ... 231
4.9.1 Parameter Values ... 232
4.9.2 Active Cables ... 232
4.10 VCONN-Powered Accessories (VPAs) and VCONN-Powered USB Devices (VPDs) ... 232
4.10.1 VCONN-Powered Accessories (VPAs) ... 233
4.10.2 VCONN-Powered USB Devices (VPDs) ... 233
4.11 Parameter Values ... 235
4.11.1 Termination Parameters ... 235
4.11.2 Timing Parameters ... 237
4.11.3 Voltage Parameters ... 240
5 USB4 Discovery and Entry ... 242
5.1 Overview of the Discovery and Entry Process ... 242
5.2 USB4 Functional Requirements ... 243
5.2.1 USB4 Host Functional Requirements ... 243
5.2.2 USB4 Device Functional Requirements ... 243
5.2.3 USB4 Alternate Mode Support ... 243
5.2.3.1 USB4 Alternate Mode Support on Hosts ... 243
5.2.3.2 USB4 Alternate Mode Support on Hubs and USB4-based Docks ... 243
5.3 USB4 Power Requirements ... 244
5.3.1 Source Power Requirements ... 244
5.3.2 Sink Power Requirements ... 244
5.3.3 Device Power Management Requirements ... 245
5.4 USB4 Discovery and Entry Flow Requirements ... 245
5.4.1 USB Type-C Initial Connection ... 245
5.4.2 USB Power Delivery Contract ... 245
5.4.3 USB4 Discovery and Entry Flow ... 246

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.4.2 总线电压..... 1
41 4.4.3 连接电压.....
143
4.5 配置通道 (CC) 147 4.5.1
架构概述 ..... 147 4.5.2 CC 功能和行
为要求 ..... 161 4.5.3 USB 端口互操作性行为 ...
..... 197 4.6 电源.....
..... 216 4.6.1 USB 暂停期间的电源要求 .....
..... 217 4.6.2 通过 USB Type-C 电缆提供的 VBUS 电源 .....
..... 218 4.7 USB 集线器 .....
..... 224 4.8 电源供应和充电 .....
..... 224 4.8.1 DFP 作为电源 .....
..... 224 4.8.2 非 USB 充电方法 .....
..... 227 4.8.3 接收主机 .....
227 4.8.4 供电设备 ..... 227 4.8.5 为
电池电量耗尽的系统充电 ..... 227 4.8.6 USB Type-C 多
端口充电器 ..... 228 4.9 电子标记线缆 .....
..... 231 4.9.1 参数值 .....
..... 232 4.9.2 有源线缆 .....
..... 232 4.10 VCONN 供电配件 (VPA) 和 VCONN 供电 USB 设备

（VPD） .....
232 4.10.1 VCONN 供电配件（VPA） .....
233 4.10.2 VCONN 供电 USB 设备（VPD） .....
233
4.11 参数值..... 235
4.11.1 终止参数 ..... 235 4.11.
2 时序参数 ..... 237 4.11.3 电
压参数 240
5USB4 发现和进入 .....
. 242 5.1 发现和进入过程概述 .....
... 242 5.2 USB4 功能要求 .....
.... 243 5.2.1 USB4 主机功能要求 .....
243 5.2.2 USB4 设备功能要求 24
3 5.2.3 USB4 备用模式支持 243
5.2.3.1 主机上的 USB4 备用模式支持 ..... 243 5.2.
3.2 集线器和基于 USB4 的扩展坞上的 USB4 备用模式支持 .....
..... 243 5.3 USB4 电源要求 .....
..... 244 5.3.1 源电源要求 .....
..... 244 5.3.2 接收器电源要求 .....
..... 244 5.3.3 设备电源管理要求 .....
..... 245 5.4 USB4 发现和进入流程要求 .....
..... 245 5.4.1 USB Type-C 初始连接 .....
..... 245 5.4.2 USB 电力输送合同 .....
..... 245 5.4.3 USB4 发现和进入流程 .....
..... 246

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

5.4.3.1 USB4 Device Discovery (SOP) ... 246
5.4.3.2 USB4 Cable Discovery (SOP') ... 247
5.4.3.3 USB4 Operational Entry ... 249
5.4.4 USB4 Post-Entry Operation ... 249
5.4.4.1 During USB4 Operation ... 249
5.4.4.2 Exiting USB4 Operation ... 250
5.5 USB4 Hub Connection Requirements ... 250
5.5.1 USB4 Hub Port Initial Connection Requirements ... 250
5.5.2 USB4 Hub UFP and Host Capabilities Discovery ... 250
5.5.3 Hub DFP Connection Requirements ... 251
5.5.3.1 Speculative Connections ... 251
5.5.3.2 Operational Connections ... 251
5.5.4 Hub Ports Connection Behavior Flow Model ... 252
5.5.5 Connecting to Downstream USB4 Hubs ... 258
5.5.6 Fallback Functional Requirements for USB4 Hubs ... 258
5.6 USB4 Device Connection Requirements ... 259
5.6.1 Fallback Mapping of USB4 Peripheral Functions to USB Device Class Types ... 259
5.7 Parameter Values ... 260
5.7.1 Timing Parameters ... 260
6 Active Cables ... 261
6.1 USB Type-C State Machine ... 262
6.2 USB PD Requirements ... 263
6.2.1 Active Cable USB PD Requirements ... 264
6.2.2 USB PD Messages for OIAC ... 264
6.2.3 Short Active Cable Behaviors in Response to Power Delivery Events ... 276
6.3 OIAC Connection Flow and State Diagrams ... 276
6.3.1 OIAC Connection Flow – Discovery – Phase 1 ... 277
6.3.2 OIAC Connection Flow – Reboot – Phase 2 ... 278
6.3.3 OIAC Connection Flow – Configuration – Phase 3 ... 279
6.3.4 OIAC Connection State Diagram Master ... 282
6.3.5 OIAC Connection State Diagram Slave ... 290
6.4 Active Cable Power Requirements ... 295
6.4.1 VBUS Requirements ... 295
6.4.2 OIAC VBUS Requirements ... 295
6.4.3 USB PD Rules in Active State ... 297
6.4.4 VCONN Requirements ... 298
6.5 Mechanical ... 298
6.5.1 Thermal ... 298
6.5.2 Plug Spacing ... 299
6.6 Electrical Requirements ... 299
6.6.1 Shielding Effectiveness Requirement ... 299
6.6.2 Low Speed Signal Requirement ... 299

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

5.4.3.1 USB4 设备发现 (SOP) 24
6 5.4.3.2 USB4 电缆发现 (SOP ’) ..... 247 5.4.
3.3 USB4 操作入口 ..... 249 5.4.4 USB
4 进入后操作 ..... 249 5.4.4.1 USB4 操
作期间 ..... 249 5.4.4.2 退出 USB4 操
作 ..... 250 5.5 USB4 集线器连接要求 .
..... 250 5.5.1 USB4 集线器端口初始连
接要求 ..... 250 5.5.2 USB4 集线器 UFP 和主机
功能发现 ..... 250 5.5.3 集线器 DFP 连接要求 ...
..... 251 5.5.3.1 推测连接.....
..... 251 5.5.3.2 操作连接 .....
..... 251 5.5.4 集线器端口连接行为流模型 .....
..... 252 5.5.5 连接到下游 USB4 集线器 ..... 258 5.5.
6 USB4 集线器的回退功能要求 258 5.6 USB4
设备连接要求 ..... 259 5.6.1 USB4 外
设功能到 USB 设备类类型的回退映射 .....
..... 259 5.7 参数值 .....
..... 260 5.7.1 时序参数 2
60

6有源线缆 .....
.. 261 6.1 USB Type-C 状态机 .....
.... 262 6.2 USB PD 要求 .....
..... 263 6.2.1 有源电缆 USB PD 要求 26
4 6.2.2 OIAC 的 USB PD 消息 2
64 6.2.3 响应电力输送事件的短有源电缆行为 .....
..... 276
6.3 OIAC 连接流程和状态图 276
6.3.1 OIAC 连接流程 – 发现 – 阶段 1 ..... 277 6.
3.2 OIAC 连接流程 – 重启 – 阶段 2 ..... 278 6.3.
3 OIAC 连接流程 – 配置 – 阶段 3 ..... 279 6.3.4
OIAC 连接状态图主机 ..... 282 6.3.5 OIAC 连
接状态图从机 290
6.4 有源电缆功率要求.....295
6.4.1 VBUS 要求 295 6.4
.2 OIAC VBUS 要求 ..... 295 6.
4.3 活动状态下的 USB PD 规则 297
6.4.4 VCONN 要求 298
6.5 机械 ..... 298 6.5.1 热 ....
..... 298 6.5.2 插头间距 .....
..... 299 6.6 电气要求 .....
..... 299
6.6.1 屏蔽效能要求 ..... 299 6.6.2 低
速信号要求 299

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.6.3 USB 2.0 ... 300
6.6.4 USB 3.2 ... 301
6.6.5 Return Loss ... 308
6.7 Active Cables That Support Alternate Modes ... 308
6.7.1 Discover SVIDs ... 308
6.7.2 Discover Modes ... 308
6.7.3 Enter/Exit Modes ... 308
6.7.4 Power in Alternate Modes ... 308
A Audio Adapter Accessory Mode ... 309
A.1 Overview ... 309
A.2 Detail ... 309
A.3 Electrical Requirements ... 310
A.4 Example Implementations ... 312
A.4.1 Passive 3.5 mm to USB Type-C Adapter – Single Pole Detection Switch ... 312
A.4.2 3.5 mm to USB Type-C Adapter Supporting 500 mA Charge-Through ... 312
B Debug Accessory Mode ... 314
B.1 Overview ... 314
B.2 Functional ... 314
B.2.1 Signal Summary ... 315
B.2.2 Port Interoperability ... 315
B.2.3 Debug Accessory Mode Entry ... 315
B.2.4 Connection State Diagrams ... 316
B.2.5 DTS Port Interoperability Behavior ... 325
B.2.6 Orientation Detection ... 334
B.3 Security/Privacy Requirements: ... 335
C USB Type-C Digital Audio ... 336
C.1 Overview ... 336
C.2 USB Type-C Digital Audio Specifications ... 336
D Thermal Design Considerations for Active Cables ... 338
D.1 Introduction ... 338
D.2 Model ... 338
D.2.1 Assumptions ... 338
D.2.2 Model Architecture ... 339
D.2.3 Heat Sources ... 340
D.2.4 Heat Flow ... 340
D.3 USB 3.2 Single Lane Active Cable ... 341
D.3.1 USB 3.2 Single-Lane Active Cable Design Considerations ... 341
D.4 Dual-Lane Active Cables ... 344
D.4.1 USB 3.2 Dual-Lane Active Cable Design Considerations ... 344
D.4.2 USB 3.2 Dual-Lane Active Cable in a Multi-Port Configuration ... 346
D.5 USB 3.2 Host and Device Design Considerations ... 348
D.5.1 Heat Spreading or Heat Sinking from Host or Device ... 348

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.6.3 USB 2.0 ..... 300 6.
6.4 USB 3.2 ..... 301 6.6.
5 回波损耗 308
6.7 支持交替模式的有源电缆..... 308
6.7.1 发现 SVID 308 6.7.2
发现模式 ..... 308 6.7.3 进入/
退出模式 ..... 308 6.7.4 备用模
式下的电源 308
音频适配器附件模式 309
A.1 概述 309
A.2 详细信息 309
A.3 电气要求 310
A.4 示例实现 312
A.4.1 无源 3.5 毫米至 USB Type-C 适配器 – 单极检测开关 .....
..... 312 A.4.2 支持 500 mA 充电的 3
.5 毫米至 USB Type-C 适配器 .....
..... 312
B 调试附件模式 314
B.1 概述..... 314
B.2 功能..... 314
B.2.1 信号摘要 315 B.2.2
端口互操作性 ..... 315 B.2.3 调
试附件模式进入 ..... 315 B.2.4 连接状
态图 ..... 316 B.2.5 DTS 端口互
操作性行为 ..... 325 B.2.6 方向检测 .....
..... 334
B.3 安全/隐私要求： ..... 335 C USB
Type-C 数字音频 336
C.1 概述 336
C.2 USB Type-C 数字音频规范 336
D 有源电缆的热设计注意事项 ..... 338 D.1 简
介 ..... 338 D.2 模型 .....
..... 338 D.2.1 假设 .....
..... 338 D.2.2 模型架构 .....
..... 339 D.2.3 热源 .....
..... 340 D.2.4 热流 .....
..... 340 D.3 USB 3.2 单道有源电缆 341
D.3.1 USB 3.2 单道有源电缆设计注意事项 ..... 341 D.4 双道
有源电缆 ..... 344 D.4.1 USB 3.2
双道有源电缆设计注意事项 ..... 344 D.4.2 多端口配置中的 U
SB 3.2 双道有源电缆 ..... 346 D.5 USB 3.2 主机和设
备设计注意事项 ..... 348 D.5.1 主机或设备的散热或散热 .....
..... 348

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

D.5.2 Motherboard Temperature Control ... 349
D.5.3 Wider Port Spacing for Multi-Port Applications ... 349
D.5.4 Power Policies ... 349
E Alternate Modes ... 350
E.1 Alternate Mode Architecture ... 350
E.2 Alternate Mode Requirements ... 350
E.2.1 Alternate Mode Pin Reassignment ... 351
E.2.2 Alternate Mode Electrical Requirements ... 352
E.3 Parameter Values ... 354
E.4 Example Alternate Mode – USB DisplayPort™ Dock ... 355
E.4.1 USB DisplayPort Dock Example ... 355
E.4.2 Functional Overview ... 356
E.4.3 Operational Summary ... 357
F Thunderbolt 3 Compatibility Discovery and Entry ... 359
F.1 TBT3 Compatibility Mode Functional Requirements ... 359
F.1.1 TBT3-Compatible Power Requirements ... 359
F.1.2 TBT3-Compatible Host Requirements ... 359
F.1.3 TBT3-Compatible Device Upstream Requirements ... 359
F.1.4 TBT3-Compatible Device Downstream Requirements ... 359
F.1.5 TBT3-Compatible Self-Powered Device Without Predefined Upstream Port Rules ... 360
F.1.6 TBT3-Compatible Devices with a Captive Cable ... 360
F.2 TBT3 Discovery and Entry Flow ... 360
F.2.1 TBT3 Passive Cable Discover Identity Responses ... 362
F.2.2 TBT3 Active Cable Discover Identity Responses ... 364
F.2.3 TBT3 Device Discover Identity Responses ... 367
F.2.4 TBT3 Discover SVID Responses ... 368
F.2.5 TBT3 Device Discover Mode Responses ... 369
F.2.6 TBT3 Cable Discover Mode Responses ... 370
F.2.7 TBT3 Cable Enter Mode Command ... 371
F.2.8 TBT3 Device Enter Mode Command ... 372
F.2.9 TBT3 Cable Functional Difference Summary ... 373

FIGURES

Figure 2-1 USB Type-C Receptacle Interface (Front View) ... 30
Figure 2-2 USB Full-Featured Type-C Plug Interface (Front View) ... 31
Figure 3-1 USB Type-C Receptacle Interface Dimensions ... 42
Figure 3-2 Reference Design USB Type-C Plug External EMC Spring Contact Zones ... 45
Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions ... 46
Figure 3-4 Reference Footprint for a USB Type-C Vertical Mount Receptacle (Informative) ... 49
Figure 3-5 Reference Footprint for a USB Type-C Dual-Row SMT Right Angle Receptacle (Informative) ... 50
Figure 3-6 Reference Footprint for a USB Type-C Hybrid Right-Angle Receptacle (Informative) ... 51
Figure 3-7 Reference Footprint for a USB Type-C Mid-Mount Dual-Row SMT Receptacle (Informative) ... 52

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

D.5.2 主板温度控制 ..... 349 D.5.3 为多端口应用提供更宽的端口间距 ..... 349 D.5.4 电源策略 349

E 备用模式 ..... 350 E.1 备用模式架构 ..... 350 E.2 备用模式要求 ..... 350 E.2.1 备用模式引脚重新分配 ..... 351 E.2.2 备用模式电气要求 ..... 352 E.3 参数值 ..... 354 E.4 备用模式示例 – USB DisplayPort™ 基座 ..... 355 E.4.1 USB DisplayPort 基座示例 ..... 355 E.4.2 功能概述 ..... 356 E.4.3 操作摘要 357

F Thunderbolt 3 兼容性发现和输入 359

F.1 TBT3 兼容模式功能要求 ..... 359 F.1.1 TBT3 兼容电源要求 ..... 359 F.1.2 TBT3 兼容主机要求 ..... 359 F.1.3 TBT3 兼容设备上行要求 ..... 359 F.1.4 TBT3 兼容设备下行要求 ..... 359 F.1.5 无预定义上行端口规则的 TBT3 兼容自供电设备 ..... 360 F.1.6 带有固定电缆的 TBT3 兼容设备 ..... 360 F.2 TBT3 发现和进入流程 ..... 360 F.2.1 TBT3 无源电缆发现身份响应 ..... 362 F.2.2 TBT3 有源电缆发现身份响应 ..... 364 F.2.3 TBT3 设备发现身份响应 ..... 367 F.2.4 TBT3 发现 SVID 响应 ..... 368 F.2.5 TBT3 设备发现模式响应 ..... 369 F.2.6 TBT3 电缆发现模式响应 ..... 370 F.2.7 TBT3 电缆进入模式命令 ..... 371 F.2.8 TBT3 设备进入模式命令 ..... 372 F.2.9 TBT3 电缆功能差异摘要 373

数字

图 2-1 USB Type-C 插座接口（正面视图） ..... 30 图 2-2 USB 全功能 Type-C 插头接口（正面视图） ..... 31 图 3-1 USB Type-C 插座接口尺寸 ..... 42 图 3-2 参考设计 USB Type-C 插头外部 EMC 弹簧触点区域 ..... 45 图 3-3 USB 全功能 Type-C 插头接口尺寸 ..... 46 图 3-4 USB Type-C 垂直安装插座的参考封装（信息性） ..... 49 图 3-5 USB Type-C 双排 SMT 直角插座的参考封装（信息性） ..... 50 图 3-6 USB Type-C 混合直角插座的参考封装（信息性） ..... 51 图3-7 USB Type-C 中置双排 SMT 插座的参考封装（参考） 52

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-8 Reference Footprint for a USB Type-C Mid-Mount Hybrid Receptacle (Informative) 53
Figure 3-9 Reference Footprint for a USB 2.0 Type-C Through Hole Right Angle Receptacle (Informative) 54
Figure 3-10 Reference Footprint for a USB 2.0 Type-C Single Row Right Angle Receptacle (Informative) 55
Figure 3-11 *USB 2.0* Type-C Plug Interface Dimensions 57
Figure 3-12 USB Type-C Plug EMC Shielding Spring Tip Requirements 60
Figure 3-13 Reference Design of Receptacle Mid-Plate 61
Figure 3-14 Reference Design of the Retention Latch 62
Figure 3-15 Illustration of the Latch Soldered to the Paddle Card Ground 62
Figure 3-16 Reference Design of the USB Full-Featured Type-C Plug Internal EMC Spring 63
Figure 3-17 Reference Design of the *USB 2.0* Type-C Plug Internal EMC Spring 64
Figure 3-18 Reference Design of Internal EMC Pad 65
Figure 3-19 Reference Design of a USB Type-C Receptacle with External EMC Springs 66
Figure 3-20 Reference Design for a USB Full-Featured Type-C Plug Paddle Card 67
Figure 3-21 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example with VCONN 70
Figure 3-22 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example without VCONN 70
Figure 3-23 USB Full-Featured Type-C Standard Cable Assembly 74
Figure 3-24 USB Type-C to USB 3.1 Standard-A Cable Assembly 77
Figure 3-25 USB Type-C to *USB 2.0* Standard-A Cable Assembly 78
Figure 3-26 USB Type-C to *USB 3.1* Standard-B Cable Assembly 79
Figure 3-27 USB Type-C to *USB 2.0* Standard-B Cable Assembly 80
Figure 3-28 USB Type-C to *USB 2.0* Mini-B Cable Assembly 81
Figure 3-29 USB Type-C to *USB 3.1* Micro-B Cable Assembly 82
Figure 3-30 USB Type-C to *USB 2.0* Micro-B Cable Assembly 84
Figure 3-31 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly 85
Figure 3-32 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly 87
Figure 3-33 Illustration of Test Points for a Mated Cable Assembly 89
Figure 3-34 Recommended Differential Insertion Loss Requirement (USB 3.2 Gen2 and USB4 Gen2) 90
Figure 3-35 Recommended Differential Return Loss Requirement 91
Figure 3-36 Recommended Differential Crosstalk Requirement 91
Figure 3-37 Recommended Differential Near-End and Far-End Crosstalk Requirement between USB D+/D− Pair and TX/RX Pair 92
Figure 3-38 Recommended Differential Insertion Loss Requirement (USB4 Gen3) 92
Figure 3-39 Illustration of Insertion Loss Fit at Nyquist Frequency 94
Figure 3-40 Input Pulse Spectrum 95
Figure 3-41 IMR Limit as Function of ILfitatNq 95
Figure 3-42 IRL Limit as Function of ILfitatNq 97
Figure 3-43 Differential-to-Common-Mode Conversion Requirement 98
Figure 3-44 IMR Limit as Function of ILfit at 10 GHz (USB4 Gen3) 99
Figure 3-45 Definition of Port, Victim, and Aggressor 99
Figure 3-46 IXT_DP and IXT_USB Limit as Function of ILfit at 10 GHz (USB4 Gen3) 100
Figure 3-47 IRL Limit as Function of ILfitatNq (USB4 Gen3) 100
Figure 3-48 Differential-to-Commom-Mode Conversion Requirement (USB4 Gen3) 101
Figure 3-49 Cable Assembly in System 101
Figure 3-50 Requirement for Differential Coupling between CC and D+/D− 104
Figure 3-51 Requirement for Single-Ended Coupling between CC and D− in USB 2.0 Type-C Cables 104
Figure 3-52 Requirement for Single-Ended Coupling between CC and D− in USB Full-Featured Type-C Cables 105
Figure 3-53 Requirement for Differential Coupling between VBUS and D+/D− 105
Figure 3-54 Requirement for Single-Ended Coupling between SBU_A and SBU_B 106

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-8 USB Type-C 中部安装混合插座的参考封装（参考） ..... 53 图 3-9 USB 2.0 Type-C 通孔直角插座的参考封装（参考） ..... 54 图 3-10 USB 2.0 Type-C 单排直角插座的参考封装（参考） ..... 55 图 3-11 *USB 2.0* Type-C 插头接口尺寸 ..... 57 图 3-12 USB Type-C 插头 EMC 屏蔽弹簧头要求 ..... 60 图 3-13 插座中板的参考设计 ..... 61 图 3-14 固定闩锁的参考设计 ..... 62 图 3-15 闩锁焊接至切换卡接地的图示 ..... 62 图 3-16 USB 全功能 Type-C 插头内部 EMC 弹簧的参考设计 ..... 63 图 3-17 *USB 2.0* Type-C 插头内部 EMC 弹簧的参考设计 ..... 64 图 3-18 内部 EMC 焊盘的参考设计 ..... 65 图 3-19 带外部 EMC 弹簧的 USB Type-C 插座的参考设计 ..... 66 图 3-20 USB 全功能 Type-C 插头桨卡的参考设计 ..... 67 图 3-21 USB 全功能 Type-C 线缆横截面图，带 VCONN 的同轴线示例 ..... 70 图 3-22 USB 全功能 Type-C 线缆横截面图，不带 VCONN 的同轴线示例 ..... 70全功能 Type-C 标准线缆组件 ..... 74 图 3-24 USB Type-C 转 USB 3.1 标准 A 线缆组件 ..... 77 图 3-25 USB Type-C 转 *USB 2.0* 标准 A 线缆组件 ..... 78 图 3-26 USB Type-C 转 *USB 3.1* 标准 B 线缆组件 ..... 79 图 3-27 USB Type-C 转 *USB 2.0* 标准 B 线缆组件 ..... 80 图 3-28 USB Type-C 转 *USB 2.0* Mini-B 线缆组件 ..... 81 图 3-29 USB Type-C 转 *USB 3.1* Micro-B 线缆组件 ..... 82 图 3-30 USB Type-C 转 *USB 2.0* Micro-B 线缆组件 ..... 84 图 3-31 USB Type-C 转 *USB 3.1* 标准 A 插座适配器组件 ..... 85 图 3-32 USB Type-C 至 *USB 2.0* Micro-B 插座适配器组件 ..... 87 图 3-33 配对电缆组件的测试点插图 ..... 89 图 3-34 建议的差分插入损耗要求（USB 3.2 Gen2 和 USB4 Gen2） ..... 90 图 3-35 建议的差分回波损耗要求 ..... 91 图 3-36 建议的差分串扰要求 ..... 91 图 3-37 USB D+/D− 对和 TX/RX 对之间建议的差分近端和远端串扰要求 ..... 92 图 3-38 建议的差分插入损耗要求（USB4 Gen3） .....

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-55 Requirement for Single-Ended Coupling between SBU_A/SBU_B and CC 107
Figure 3-56 Requirement for Coupling between SBU_A and differential D+/D−, and SBU_B and differential D+/D− 107
Figure 3-57 Illustration of USB Type-C Mated Connector 108
Figure 3-58 Recommended Impedance Limits of a USB Type-C Mated Connector 109
Figure 3-59 Recommended Ground Void Dimensions for USB Type-C Receptacle 110
Figure 3-60 Recommended Differential Near-End and Far-End Crosstalk Limits between D+/D− Pair and TX/RX Pairs 112
Figure 3-61 Recommended Limits for Differential-to-Common-Mode Conversion 112
Figure 3-62 IMR Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly 116
Figure 3-63 IRL Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly 116
Figure 3-64 Cable Assembly Shielding Effectiveness Testing 120
Figure 3-65 Shielding Effectiveness Pass/Fail Criteria 121
Figure 3-66 LLCR Measurement Diagram 122
Figure 3-67 Temperature Measurement Point 124
Figure 3-68 Example Current Rating Test Fixture Trace Configuration 125
Figure 3-69 Example of 4-Axis Continuity Test Fixture 127
Figure 3-70 Example Wrenching Strength Test Fixture for Plugs without Overmold 129
Figure 3-71 Reference Wrenching Strength Continuity Test Fixture 130
Figure 3-72 Example of Wrenching Strength Test Mechanical Failure Point 130
Figure 3-73 Wrenching Strength Test with Cable in Fixture 131
Figure 3-74 USB Type-C Cable Receptacle Flange Example 133
Figure 3-75 EMC Guidelines for Side Latch and Mid-plate 134
Figure 3-76 EMC Finger Connections to Plug Shell 134
Figure 3-77 EMC Pad Connections to Receptacle Shell 135
Figure 3-78 Examples of Connector Apertures 135
Figure 3-79 Recommended Minimum Spacing between Connectors 136
Figure 3-80 Recommended Minimum Plug Overmold Clearance 136
Figure 3-81 Cable Plug Overmold and an Angled Surface 137
Figure 4-1 Cable IR Drop 140
Figure 4-2 Cable IR Drop for powered cables 140
Figure 4-3 Logical Model for Single-Lane Data Bus Routing across USB Type-C-based Ports 149
Figure 4-4 Logical Model for USB Type-C-based Ports for a Single-Lane Direct Connect Device 149
Figure 4-5 Pull-Up/Pull-Down CC Model 151
Figure 4-6 Current Source/Pull-Down CC Model 151
Figure 4-7 Source Functional Model for CC1 and CC2 154
Figure 4-8 Source Functional Model Supporting USB PD PR_Swap 155
Figure 4-9 Sink Functional Model for CC1 and CC2 156
Figure 4-10 Sink Functional Model Supporting USB PD PR_Swap and VCONN_Swap 157
Figure 4-11 DRP Functional Model for CC1 and CC2 157
Figure 4-12 Connection State Diagram: Source 162
Figure 4-13 Connection State Diagram: Sink 163
Figure 4-14 Connection State Diagram: Sink with Accessory Support 164
Figure 4-15 Connection State Diagram: DRP 165
Figure 4-16 Connection State Diagram: DRP with Accessory and Try.SRC Support 166
Figure 4-17 Connection State Diagram: DRP with Accessory and Try.SNK Support 167
Figure 4-18 Connection State Diagram: Charge-Through VPD 168
Figure 4-19 Sink Power Sub-States 192
Figure 4-20 Cable eMarker State Diagram 194
Figure 4-21 Source to Sink Functional Model 197
Figure 4-22 Source to DRP Functional Model 198
Figure 4-23 DRP to Sink Functional Model 199
Figure 4-24 DRP to DRP Functional Model – CASE 1 200
Figure 4-25 DRP to DRP Functional Model – CASE 2 & 3 201
Figure 4-26 Source to Source Functional Model 203

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-55 SBU_A/SBU_B 与 CC 之间的单端耦合要求 ..... 107 图 3-56 SBU_A 与差分 D+/D− 以及 SBU_B 与差分 D+/D− 之间的耦合要求 ..... 107 图 3-57 USB Type-C 配对连接器示意图 ..... 108 图 3-58 USB Type-C 配对连接器的建议阻抗限值 ..... 109 图 3-59 USB Type-C 插座的建议接地空隙尺寸 ..... 110 图 3-60 D+/D− 对与 TX/RX 对之间的建议差分近端和远端串扰限值 ..... 112 图 3-61 建议差模至共模转换的限制 ..... 112 图 3-62 USB Type-C 至传统电缆组件的 IMR 限值与 ILfitatNq 的关系 ..... 116 图 3-63 USB Type-C 至传统电缆组件的 IRL 限值与 ILfitatNq 的关系 ..... 116 图 3-64 电缆组件屏蔽效能测试 ..... 120 图 3-65 屏蔽效能通过/失败标准 ..... 121 图 3-66 LLCR 测量图 ..... 122 图 3-67 温度测量点 ..... 124 图 3-68 电流额定值测试夹具迹线配置示例 ..... 125 图 3-69 4 轴连续性测试夹具示例 ..... 127 图3-70 无包覆成型插头的扳手强度测试夹具示例 ..... 129 图 3-71 参考扳手强度连续性测试夹具 ..... 130 图 3-72 扳手强度测试机械故障点示例 ..... 130 图 3-73 夹具中有电缆时的扳手强度测试 ..... 131 图 3-74 USB Type-C 电缆插座法兰示例 ..... 133 图 3-75 侧锁扣和中板的 EMC 指南 ..... 134 图 3-76 EMC 手指与插头外壳的连接 ..... 134 图 3-77 EMC 垫与插座外壳的连接 ..... 135 图 3-78 连接器孔径示例 ..... 135 图 3-79 建议的最小连接器之间的间距 ..... 136 图 3-80 建议的最小插头包覆成型间隙 ..... 136 图 3-81 电缆插头包覆成型和倾斜表面 ..... 137 图 4-1 电缆 IR 压降 ..... 140 图 4-2 供电电缆的 IR 压降 ..... 140 图 4-3 跨 USB Type-C 端口的单通道数据总线布线逻辑模型 ..... 149 图 4-4 单通道直接连接设备的 USB Type-C 端口逻辑模型 ..... 149 图 4-5 上拉/下拉 CC 模型 ..... 151 图 4-6 电流源/下拉 CC 模型 ..... 151 CC2 ..... 154 图 4-8 源功能

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-27 Sink to Sink Functional Model 204
Figure 4-28 DRP to VPD Model 204
Figure 4-29 Example DRP to Charge-Through VCONN-Powered USB Device Model 205
Figure 4-30 Source to Legacy Device Port Functional Model 213
Figure 4-31 Legacy Host Port to Sink Functional Model 214
Figure 4-32 DRP to Legacy Device Port Functional Model 215
Figure 4-33 Legacy Host Port to DRP Functional Model 216
Figure 4-34 Sink Monitoring for Current in Pull-Up/Pull-Down CC Model 220
Figure 4-35 Sink Monitoring for Current in Current Source/Pull-Down CC Model 220
Figure 4-36 USB PD over CC Pins 221
Figure 4-37 USB PD BMC Signaling over CC 221
Figure 4-38 USB Type-C Cable's Output as a Function of Load for Non-PD-based USB Type-C Charging 226
Figure 4-39 0 – 3 A USB PD-based Charger USB Type-C Cable's Output as a Function of Load 226
Figure 4-40 3 – 5 A USB PD-based Charger USB Type-C Cable's Output as a Function of Load 227
Figure 4-41 Electronically Marked Cable with VCONN connected through the cable 231
Figure 4-42 Electronically Marked Cable with SOP' at both ends 232
Figure 4-43 Example Charge-Through VCONN-Power USB Device Use Case 235
Figure 4-44 DRP Timing 238
Figure 5-1 USB4 Discovery and Entry Flow Model 246
Figure 5-2 USB4 Hub with USB4 Host and Device Connection Flow Alignment 253
Figure 5-3 USB4 Hub with USB 3.2 Host and USB4 Device Host Connection Flow Model 254
Figure 5-4 USB4 Hub with USB4 Host and USB 3.2 Device Connection Flow Model 255
Figure 5-5 USB4 Hub with USB 3.2 Host and Device Connection Flow Model 256
Figure 5-6 USB4 Hub with USB4 Host and DP Alt Mode Device Connection Flow Model 257
Figure 5-7 USB4 Hub with USB 3.2 Host and DP Alt Mode Device Connection Flow Model 258
Figure 6-1 Electronically Marked Short Active Cable with SOP' Only 263
Figure 6-2 Electronically Marked Short Active Cable with SOP' and SOP" 263
Figure 6-3 Electronically Marked Optically Isolated Active Cable 264
Figure 6-4 OIAC USB PD Message Forwarding 270
Figure 6-5 OIAC Successful Data Role Swap 273
Figure 6-6 OIAC Rejected Data Role Swap 274
Figure 6-7 OIAC Wait Data Role Swap 274
Figure 6-8 OIAC Initiator Reject Data Role Swap 275
Figure 6-9 OIAC Initiator Wait Data Role Swap 276
Figure 6-10 OIAC Discovery – Phase 1 278
Figure 6-11 OIAC Reboot – Phase 2 279
Figure 6-12 OIAC Master Plug Configure as DFP – Phase 3 280
Figure 6-13 OIAC Master Plug Configure as UFP – Phase 3 281
Figure 6-14 OIAC Master Plug No Connection Possible Billboard – Phase 3 282
Figure 6-15 OIAC Master Plug State Diagram Part 1 (Phase 1 and 2) 283
Figure 6-16 OIAC Master Plug State Diagram Part 2 (Phase 3) 284
Figure 6-17 OIAC Slave Plug State Diagram 291
Figure 6-18 Active Cable Topologies 301
Figure 6-19 Illustrations of Usages for OIAC That Require an Adapter or Hub 304
Figure 6-20 SuperSpeed USB Electrical Test Points 305
Figure 6-21 SuperSpeed USB Compliance Test Setup 305
Figure A-1 Example Passive 3.5 mm to USB Type-C Adapter 312
Figure A-2 Example 3.5 mm to USB Type-C Adapter Supporting 500 mA Charge-Through 313
Figure B-1 USB Type-C Debug Accessory Layered Behavior 314
Figure B-2 DTS Plug Interface 315
Figure B-3 Connection State Diagram: DTS Source 316
Figure B-4 Connection State Diagram: DTS Sink 317
Figure B-5 Connection State Diagram: DTS DRP 318
Figure B-6 TS Sink Power Sub-States 323

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-27 吸电流到吸电流功能模型 ..... 204 图 4-28 DRP 到 VPD 模型 ..... 204 图 4-29 示例 DRP 到通过 VCONN 充电的 USB 设备模型 ..... 205 图 4-30 源电流到传统设备端口功能模型 ..... 213 图 4-31 传统主机端口到吸电流功能模型 ..... 214 图 4-32 DRP 到传统设备端口功能模型 ..... 215 图 4-33 传统主机端口到 DRP 功能模型 ..... 216 图 4-34 上拉/下拉 CC 模型中的吸电流监控 ..... 220 图 4-35 电流源电流/下拉 CC 模型中的吸电流监控 ..... 220 图 4-36 USB PD 通过 CC 引脚 ..... 221 图 4-37 USB PD BMC 通过 CC 信号传输 ..... 221 图 4-38 USB Type-C 线缆输出作为非 PD USB Type-C 充电负载的函数 ..... 226 图 4-39 0 – 3 A USB PD 充电器 USB Type-C 线缆输出作为负载的函数 ..... 226 图 4-40 3 – 5 A USB PD 充电器 USB Type-C 线缆输出作为负载的函数 ..... 227 图 4-41 通过线缆连接 VCONN 的电子标记线缆 ..... 231 图 4-42 两端带有 SOP ’ 的电子标记线缆 ..... 232 图 4-43 示例直通充电VCONN-Power USB 设备用例 ..... 235 图 4-44 DRP 时序 ..... 238 图 5-1 USB4 发现和进入流程模型 ..... 246 图 5-2 USB4 集线器与 USB4 主机和设备连接流程对齐 ..... 253 图 5-3 USB 4 集线器与 USB 3.2 主机和 USB4 设备主机连接流程模型 ..... 254 图 5-4 USB4 集线器与 USB4 主机和 USB 3.2 设备连接流程模型 ..... 255 图 5-5 USB4 集线器与 USB 3.2 主机和设备连接流程模型 ..... 256 图 5-6 USB4 集线器与 USB4 主机和 DP Alt 模式设备连接流程模型 ..... 257 图 5-7 USB4 集线器与 USB 3.2 主机和 DP Alt 模式设备连接流程模型 ..... 258 图 6-1仅带有 SOP ’ 的电子标记短有源线缆 ..... 263 图 6-2 带有 SOP ’ 和 SOP ” 的电子标记短有源线缆 ..... 263 图 6-3 电子标记光学隔离有源线缆 ..... 264 图 6-4 OIAC USB PD 消息转发 ..... 270 图 6-5 OIAC 成功数据角色交换 ..... 273 图 6-6 OIAC 拒绝数据角色交换 ..... 274 图 6-7 OIAC 等待数据角色交换 ..... 274 图 6-8 OIAC 发起方拒绝数据角色交换 ..... 275 图 6-9 OIAC 发起方等待数据角色交换 ..... 276 图 6-10 OIAC 发现 – 阶段1.....

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure D-1 Active Cable Model (Single Port, Top Mount Receptacle) 339
Figure D-2 Model Architecture 339
Figure D-3 Heat Sources and Heat Flow Paths 340
Figure D-4 Vertically Stacked Horizontal Connectors 3x1 Configuration (VERT) 342
Figure D-5 Horizontally Stacked Vertical Connectors 1x3 Configuration (HZ90) 342
Figure D-6 Horizontally Stacked Horizontal Connector 1x3 Configuration (HORZ) 342
Figure D-7 USB 3.2 Single-Lane 3A Active Cable in a 3-Port Configuration 343
Figure D-8 USB 3.2 Single-Lane 5A Active Cable in a 3-Port Configuration 344
Figure D-9 Impact of Over-mold Power P_O and Thermal Boundary Temperature T_{MB} at 3 A V_{BUS} in a Single Port Configuration 345
Figure D-10 Impact of Over-mold Power P_O and Thermal Boundary Temperature T_{MB} at 5 A V_{BUS} in a Single Port Configuration 346
Figure D-11 USB 3.2 Active Cable Dongle Design (One End Shown) 346
Figure D-12 USB 3.2 Dual-Lane 3A Active Cable in a 3-Port Configuration 347
Figure D-13 USB 3.2 Dual-Lane 5A Active Cable in a 3-Port Configuration 348
Figure D-14 Example: Additional Heat Spreader on Receptacle in Host or Device 349
Figure D-15 Example: Heat Sinking by Chassis of Host or Device 349
Figure E-1 Pins Available for Reconfiguration over the Full-Featured Cable 351
Figure E-2 Pins Available for Reconfiguration for Direct Connect Applications 351
Figure E-3 Alternate Mode Implementation using a USB Type-C to USB Type-C Cable 353
Figure E-4 Alternate Mode Implementation using a USB Type-C to Alternate Mode Cable or Device 354
Figure E-5 USB DisplayPort Dock Example 356
Figure F-1 TBT3 Discovery Flow 361

TABLES

Table 2-1 Summary of power supply options 36
Table 3-1 USB Type-C Standard Cable Assemblies 37
Table 3-2 USB Type-C Legacy Cable Assemblies 38
Table 3-3 USB Type-C Legacy Adapter Assemblies 38
Table 3-4 USB Type-C Receptacle Interface Pin Assignments 68
Table 3-5 USB Type-C Receptacle Interface Pin Assignments for USB 2.0-only Support 69
Table 3-6 USB Type-C Standard Cable Wire Assignments 71
Table 3-7 USB Type-C Cable Wire Assignments for Legacy Cables/Adapters 72
Table 3-8 Reference Wire Gauges for standard USB Type-C Cable Assemblies 73
Table 3-9 Reference Wire Gauges for USB Type-C to Legacy Cable Assemblies 73
Table 3-10 USB Full-Featured Type-C Standard Cable Assembly Wiring 75
Table 3-11 *USB 2.0* Type-C Standard Cable Assembly Wiring 76
Table 3-12 USB Type-C to *USB 3.1* Standard-A Cable Assembly Wiring 77
Table 3-13 USB Type-C to *USB 2.0* Standard-A Cable Assembly Wiring 78
Table 3-14 USB Type-C to *USB 3.1* Standard-B Cable Assembly Wiring 79
Table 3-15 USB Type-C to *USB 2.0* Standard-B Cable Assembly Wiring 80
Table 3-16 USB Type-C to *USB 2.0* Mini-B Cable Assembly Wiring 81
Table 3-17 USB Type-C to *USB 3.1* Micro-B Cable Assembly Wiring 83
Table 3-18 USB Type-C to *USB 2.0* Micro-B Cable Assembly Wiring 84
Table 3-19 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly Wiring 86
Table 3-20 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly Wiring 87
Table 3-21 Differential Insertion Loss Examples for TX/RX with Twisted Pair Construction 88
Table 3-22 Differential Insertion Loss Examples for USB TX/RX with Coaxial Construction 89
Table 3-23 Key Parameters in COM Configuration File 102
Table 3-24 Electrical Requirements for CC and SBU wires 103
Table 3-25 Coupling Matrix for Low Speed Signals 103
Table 3-26 Maximum Mutual Inductance (M) between V_{BUS} and Low Speed Signal Lines 106

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 D-1 有源电缆模型（单端口，顶部安装插座） ..... 339 图 D-2 模型架构 ..... 339 图 D-3 热源和热流路径 ..... 340 图 D-4 垂直堆叠水平连接器 3x1 配置 (VERT) ..... 342 图 D-5 水平堆叠垂直连接器 1x3 配置 (HZ90) ..... 342 图 D-6 水平堆叠水平连接器 1x3 配置 (HORZ) ..... 342 图 D-7 3 端口配置中的 USB 3.2 单通道 3A 有源电缆 ..... 343 图 D-8 3 端口配置中的 USB 3.2 单通道 5A 有源电缆 ..... 344 图 D-9 包覆成型功率 P_0 和热边界温度的影响单端口配置中 3 A VBUS 下的 T_{MB} ..... 345 图 D-10 单端口配置中 5 A VBUS 下的包覆成型功率 P_0 和热边界温度 T_{MB} 的影响 ..... 346 图 D-11 USB 3.2 有源线缆适配器设计（显示一端） ..... 346 图 D-12 3 端口配置中的 USB 3.2 双通道 3A 有源线缆 ..... 347 图 D-13 3 端口配置中的 USB 3.2 双通道 5A 有源线缆 ..... 348 图 D-14 示例：主机或设备插座上的附加散热器 ..... 349 图 D-15 示例：主机或设备底盘的散热 ..... 349 图 E-1通过全功能电缆进行重新配置 ..... 351 图 E-2 可用于直接连接应用重新配置的引脚 ..... 351 图 E-3 使用 USB Type-C 转 USB Type-C 电缆实现备用模式 ..... 353 图 E-4 使用 USB Type-C 转备用模式电缆或设备实现备用模式 354
图 E-5 USB DisplayPort 基座示例 ..... 356 图F-1 TBT3 发现流程 361

表格

表 2-1 电源选项摘要 ..... 36 表 3-1 USB Type-C 标准电缆组件 ..... 37 表 3-2 USB Type-C 传统电缆组件 ..... 38 表 3-3 USB Type-C 传统适配器组件 ..... 38 表 3-4 USB Type-C 插座接口引脚分配 ..... 68 表 3-5 仅支持 USB 2.0 的 USB Type-C 插座接口引脚分配 ..... 69 表 3-6 USB Type-C 标准电缆线分配 ..... 71 表 3-7 传统电缆/适配器的 USB Type-C 电缆线分配 ..... 72 表 3-8 标准 USB Type-C 电缆组件的参考线规 ..... 73 表3-9 USB Type-C 转传统电缆组件的参考线规 ..... 73 表 3-10 USB 全功能 Type-C 标准电缆组件接线 ..... 75 表 3-11 *USB 2.0* Type-C 标准电缆组件接线 ..... 76 表 3-12 USB Type-C 转 *USB 3.1* 标准 A 型电缆组件接线 ..... 77 表 3-13 USB Type-C 转 *USB 2.0* 标准 A 型电缆组件接线 ..... 78 表 3-14 USB Type-C 转 *USB 3.1* 标准 B 型电缆组件接线 ..... 79 表 3-15 USB Type-C 转 *USB 2.0* 标准 B 型电缆组件接线 ..... 80 表 3-16 USB Type-C 转 *USB 2.0* Mini-B 型电缆组件接线 ..... 81 表 3-17 USB Type-C 转*USB 3.1* Micro-B 电缆组件接线 ..... 83 表 3-18 USB Type-C 至 *USB 2.0* Micro-B 电缆组件接线 ..... 84 表 3-19 USB Type-C 至 *USB 3.1* 标准 A 型插座适配器组件接线 ..... 86 表 3-20 USB Type-C 至 *USB 2.0* Micro-B 插座适配器组件接线 ..... 87 表 3-21 采用双绞线结构的 TX/RX 差分插入损耗示例 ..... 88 表 3-22 采用同轴结构的 USB TX/RX 差分插入损耗示例 ..... 89 表 3-23 COM 配置文件中的关键参数 ..... 102 表 3-24 CC 和 SBU 线的电气要求 ..... 103 表 3-25 低速信号的耦合矩阵 ..... 103 表 3-26 VBUS 与低速信号线间最大互感（M） 106

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-27 USB D+/D− Signal Integrity Requirements for USB Type-C to USB Type-C Passive Cable Assemblies 108
Table 3-28 USB Type-C Mated Connector Recommended Signal Integrity Characteristics (Informative) 110
Table 3-29 USB Type-C Mated Connector Signal Integrity Characteristics for USB4 Gen3 (Normative) 113
Table 3-30 USB D+/D− Signal Integrity Requirements for USB Type-C to Legacy USB Cable Assemblies 114
Table 3-31 Design Targets for USB Type-C to *USB 3.1* Gen2 Legacy Cable Assemblies (Informative) 115
Table 3-32 USB Type-C to *USB 3.1* Gen2 Legacy Cable Assembly Signal Integrity Requirements (Normative) 115
Table 3-33 USB D+/D− Signal Integrity Requirements for USB Type-C to Legacy USB Adapter Assemblies (Normative) 117
Table 3-34 Design Targets for USB Type-C to *USB 3.1* Standard-A Adapter Assemblies (Informative) 118
Table 3-35 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly Signal Integrity Requirements (Normative) 119
Table 3-36 Current Rating Test PCB 124
Table 3-37 Maximum DC Resistance Requirement (Normative) 125
Table 3-38 Force and Moment Requirements 128
Table 3-39 Environmental Test Conditions 131
Table 3-40 Reference Materials 132
Table 4-1 USB Type-C List of Signals 138
Table 4-2 VBUS Source Characteristics 141
Table 4-3 VBUS Sink Characteristics 142
Table 4-4 USB Type-C Source Port's VCONN Requirements Summary 143
Table 4-5 VCONN Source Characteristics 144
Table 4-6 Cable VCONN Sink Characteristics 145
Table 4-7 VCONN-Powered Accessory (VPA) Sink Characteristics 146
Table 4-8 VCONN-Powered USB Device (VPD) Sink Characteristics 147
Table 4-9 USB Type-C-based Port Interoperability 150
Table 4-10 Source Perspective 152
Table 4-11 Source (Host) and Sink (Device) Behaviors by State 153
Table 4-12 USB PD Swapping Port Behavior Summary 159
Table 4-13 Power Role Behavioral Model Summary 160
Table 4-14 Source Port CC Pin State 169
Table 4-15 Sink Port CC Pin State 169
Table 4-16 Mandatory and Optional States 195
Table 4-17 Precedence of power source usage 217
Table 4-18 USB Type-C Current Advertisement and PDP Equivalent 219
Table 4-19 Precedence of power source usage 223
Table 4-20 Example Charge-Through VPD Sink Maximum Currents based on VBUS Impedance and GND Impedance 223
Table 4-21 SOP' and SOP" Timing 232
Table 4-22 Charge-Through VPD CC Impedance (RccCON) Requirements 234
Table 4-23 CTVPD Charge-Through Port VBUS Bypass Requirements 234
Table 4-24 Source CC Termination (Rp) Requirements 235
Table 4-25 Sink CC Termination (Rd) Requirements 236
Table 4-26 Powered Cable Termination Requirements 236
Table 4-27 CC Termination Requirements for Disabled state, ErrorRecovery state, and Unpowered Source 236
Table 4-28 SBU Termination Requirements 236
Table 4-29 VBUS and VCONN Timing Parameters 237
Table 4-30 DRP Timing Parameters 238

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-27 USB Type-C 至 USB Type-C 无源线缆组件的 USB D+/D− 信号完整性要求 ..... 108 表 3-28 USB Type-C 配对连接器推荐信号完整性特性（参考） ..... 110 表 3-29 USB Type-C 配对连接器 USB4 Gen3 信号完整性特性（规范性） ..... 113 表 3-30 USB Type-C 至传统 USB 线缆组件的 USB D+/D− 信号完整性要求 ..... 114 表 3-31 USB Type-C 至 *USB 3.1* Gen2 传统线缆组件的设计目标（参考） ..... 115 表 3-32 USB Type-C 至 *USB 3.1* Gen2 传统电缆组件信号完整性要求（规范性） ..... 115 表 3-33 USB Type-C 至传统 USB 适配器组件的 USB D+/D− 信号完整性要求（规范性） ..... 117 表 3-34 USB Type-C 至 *USB 3.1* 标准 A 适配器组件的设计目标（参考性） ..... 118 表 3-35 USB Type-C 至 *USB 3.1* 标准 A 插座适配器组件信号完整性要求（规范性） ..... 119 表 3-36 电流额定值测试 PCB ..... 124 表 3-37 最大直流电阻要求（规范性） ..... 125 表 3-38 力和力矩要求 ..... 128 表 3-39 环境测试条件 ..... 131 表 3-40 参考资料 ..... 132 表 4-1 USB Type-C 信号列表 ..... 138 表 4-2 VBUS 源特性 ..... 141 表 4-3 VBUS 接收器特性 ..... 142 表 4-4 USB Type-C 源端口的 VCONN 要求摘要 ..... 143 表 4-5 VCONN 源特性 ..... 144 表 4-6 电缆 VCONN 接收器特性 ..... 145 表 4-7 VCONN 供电配件 (VPA)接收器特性 ..... 146 表 4-8 VCONN 供电的 USB 设备 (VPD) 接收器特性 ..... 147 表 4-9 基于 USB Type-C 的端口互操作性 ..... 150 表 4-10 源视角 ..... 152 表 4-11 源（主机）和接收器（设备）按状态的行为 .....

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 4-31 CC Timing 239
Table 4-32 CC Voltages on Source Side – Default USB 240
Table 4-33 CC Voltages on Source Side – 1.5 A @ 5 V 240
Table 4-34 CC Voltages on Source Side – 3.0 A @ 5 V 241
Table 4-35 Voltage on Sink CC Pins (Default USB Type-C Current only) 241
Table 4-36 Voltage on Sink CC pins (Multiple Source Current Advertisements) 241
Table 5-1 Certified Cables Where USB4-compatible Operation is Expected 247
Table 5-2 Fallback Mapping USB4 Peripheral Functions to USB Device Class Types 259
Table 5-3 USB Billboard Device Class Availability Following USB4 Device Entry Failure 260
Table 6-1 Comparison of Active Cables 262
Table 6-2 Summary of Active Cable Features 262
Table 6-3 OIAC USB PD Message Behavior on Initial Connection 265
Table 6-4 OIAC USB PD Messages Which Do Not Traverse in Active State 267
Table 6-5 OIAC USB PD Messages Addressed to SOP Which Traverse the OIAC in the Active State . 269
Table 6-6 OIAC USB PD Message Timing 270
Table 6-7 OIAC SOP Messages Which Terminate at the Cable Plug 271
Table 6-8 Port and Plug Capabilities 277
Table 6-9 OIAC Sink_Capabilities PDO (SOP) on Initial Connection 296
Table 6-10 OIAC Sink_Capabilities_Extended PDO (SOP) on Initial Connection 296
Table 6-11 OIAC Sink RDO (SOP) on Initial Connection 297
Table 6-12 OIAC Active Sink RDO (SOP) 297
Table 6-13 OIAC Sink_Capabilities PDO (SOP) in Active 298
Table 6-14 Cable Temperature Requirements 299
Table 6-15 Summary of Active Cable Features 300
Table 6-16 Active Cable Power-on Requirements 302
Table 6-17 OIAC Maximum USB 3.2 U0 Delay 303
Table 6-18 Usages for OIAC That Require an Adapter or Hub 303
Table 6-19 USB 3.2 U-State Requirements 304
Table 6-20 Active Cable USB 3.2 Stressed Source Swing, TP1 306
Table 6-21 Active Cable USB 3.2 Stressed Source Jitter, TP1 306
Table 6-22 Active Cable USB 3.2 Input Swing at TP2 (Informative) 307
Table 6-23 Active Cable USB 3.2 Output Swing at TP3 (Informative) 307
Table A-1 USB Type-C Analog Audio Pin Assignments 310
Table A-2 USB Type-C Analog Audio Pin Electrical Parameter Ratings 311
Table B-1 DTS to TS Port Interoperability 315
Table B-2 Rp/Rp Charging Current Values for a DTS Source 323
Table B-3 Mandatory and Optional States 325
Table D-1 Heat Sources and Heat Dissipation Example (1.5 W cable and 5 A) 341
Table D-2 USB 3.2 Active Cable Design Single Port Case Study at 35 °C Ambient and 60 °C Thermal Boundary (Single Lane) 341
Table D-3 USB 3.2 Active Cable Design Single Port Case Study at 35 °C Ambient and 60 °C Thermal Boundary (Dual Lane) 345
Table E-1 USB Safe State Electrical Requirements 354
Table E-2 USB Billboard Device Class Availability Following Alternate Mode Entry Failure 355
Table E-3 Alternate Mode Signal Noise Ingression Requirements 355
Table F-1 TBT3 Passive Cable Discover Identity VDO Responses 362
Table F-2 TBT3 Passive Cable VDO for USB PD Revision 2.0, Version 1.3 363
Table F-3 TBT3 Passive Cable VDO for USB PD Revision 3.0, Version 1.2 363
Table F-4 TBT3 Active Cable Discover Identity VDO Responses 364
Table F-5 TBT3 Active Cable VDO for USB PD Revision 2.0, Version 1.3 365
Table F-6 TBT3 Active Cable VDO 1 for USB PD Revision 3.0, Version 1.2 365
Table F-7 TBT3 Active Cable VDO 2 for USB PD Revision 3.0, Version 1.2 366
Table F-8 TBT3 Device Discover Identity VDO Responses 367
Table F-9 TBT3 Discover SVID VDO Responses 368
Table F-10 TBT3 Device Discover Mode VDO Responses 369

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 4-31 CC 时序 ..... 239 表 4-32 源侧的 CC 电压 – 默认 USB ..... 240 表 4-33 源侧的 CC 电压 – 1.5 A @ 5 V ..... 240 表 4-34 源侧的 CC 电压 – 3.0 A @ 5 V ..... 241 表 4-35 接收器 CC 引脚上的电压（仅限默认 USB Type-C 电流） ..... 241 表 4-36 接收器 CC 引脚上的电压（多个源电流通告） ..... 241 表 5-1 预期兼容 USB4 操作的认证电缆 ..... 247 表 5-2 将 USB4 外设功能回退映射到 USB 设备类类型 ..... 259 表 5-3 USB4 设备进入后 USB 公告牌设备类可用性故障 ..... 260 表 6-1 有源电缆比较 ..... 262 表 6-2 有源电缆特性摘要 ..... 262 表 6-3 初始连接时的 OIAC USB PD 消息行为 ..... 265 表 6-4 在活动状态下不遍历的 OIAC USB PD 消息 ..... 267 表 6-5 在活动状态下遍历 OIAC 的、发送到 SOP 的 OIAC USB PD 消息。 269 表 6-6 OIAC USB PD 消息时序 ..... 270 表 6-7 终止于电缆插头的 OIAC SOP 消息 ..... 271 表 6-8 端口和插头功能 ..... 277 表 6-9 初始连接时的 OIAC Sink_Capabilities PDO（SOP） ..... 296 表 6-10 初始连接时的 OIAC Sink_Capabilities_Extended PDO（SOP） ..... 296 表 6-11 初始连接时的 OIAC Sink RDO（SOP） ..... 297 表 6-12 OIAC Active Sink RDO（SOP） ..... 297 表 6-13 处于 Active 状态的 OIAC Sink_Capabilities PDO（SOP） ..... 298 表 6-14 电缆温度要求 ..... 299 表 6-15 有源电缆功能摘要 ..... 300 表 6-16 有源电缆开机要求 ..... 302 表 6-17 OIAC 最大 USB 3.2 U0 延迟 ..... 303 表 6-18 需要适配器或集线器的 OIAC 用法 ..... 303 表 6-19 USB 3.2 U 状态要求 ..... 304 表 6-20 有源电缆 USB 3.2 压力源摆幅，TP1 ..... 306 表 6-21 有源电缆 USB 3.2 压力源抖动，TP1 ..... 306 表 6-22 有源电缆 USB 3.2 TP2 处的输入摆幅（参考信息） ..... 307 表 6-23 TP3 处有源电缆 USB 3.2 输出摆幅（参考信息） ..... 307 表 A-1 USB Type-C 模拟音频引脚分配 ..... 310 表 A-2 USB Type-C 模拟音频引脚电气参数额定值 ..... 311 表 B-1 DTS 至 TS 端口互操作性 .....

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table F-11 TBT3 Cable Discover Mode VDO Responses 370
Table F-12 TBT3 Cable Enter Mode Command 371
Table F-13 TBT3 Device Enter Mode Command 372
Table F-14 TBT3 Cable Functional Difference Summary 373

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 F-11 TBT3 电缆发现模式 VDO 响应 ..... 370 表 F-12 TBT3 电缆进入模式命令 ..... 371 表 F-13 TBT3 设备进入模式命令 ..... 372 表 F-14 TBT3 电缆功能差异摘要 373

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Specification Work Group Chairs / Specification Editors

Intel Corporation (USB Promoter company)	Yun Ling – Mechanical WG co-chair, Mechanical Chapter Co-editor Brad Saunders – Plenary/Functional WG chair, Specification Co-author
Renesas Electronics Corp. (USB Promoter company)	Bob Dunstan – Functional WG co-chair, Specification Co-author
Seagate	Alvin Cox, Mechanical WG co-chair, Mechanical Chapter Co-editor

Specification Work Group Contributors

Note: For historical reasons, the following list also includes individual contributors that were members of the work group and associated with their company affliations at the time of the original Release 1.0 and Release 2.0.

Advanced-Connectek, Inc. (ACON)	Victory Chen Glen Chandler Dennis Cheung Jeff Chien Lee (Dick Lee) Ching	Conrad Choy Vicky Chuang Jessica Feng Aven Kao Danny Liao	Alan Tsai Wayne Wang Stephen Yang Sunney Yang
Advanced Micro Devices	Steve Capezza Walter Fry Will Harris	Jason Hawken Tim Perley	Joseph Scanlon Peter Teng
Allion Labs, Inc.	Howard Chang Minoru Ohara	Brian Shih	Chester Tsai
Amphenol AssembleTech (Xiamen) Co., Ltd.	Louis Chan Jesse Jaramillo Terry Ke	Martin Li Lino Liu Shawn Wei	Alan Yang
Amphenol Corporation	Zhinenng Fan		
Agilent Technologies, Inc.	James Choate		
Analogix Semiconductor, Inc.	Mehran Badii Greg Stewart	Haijian Sui	Yueke Tang
Apple Inc. (USB Promoter company)	Colin Abraham Mahmoud Amini Sree Anantharaman Brian Baek Paul Baker Michael Bonham Carlos Calderon Jason Chung David Conroy Bill Cornelius Christophe Daniel William Ferry Brian Follis	Zheng Gao Derek Iwamoto Scott Jackson Girault Jones Keong Kam Kevin Keeler Min Kim Woopoung Kim Alexei Kosut Christine Krause Chris Ligtenberg Matthew Mora Nathan Ng	James Orr Keith Porthouse Breton Saunders Reese Schreiber Sascha Tietz Jennifer Tsai Colin Whitby-Strevens Jeff Wilcox Eric Wiles Dan Wilson Dennis Yarak
Bizlink Technology, Inc.	Alex Chou	Morphy Hsieh	

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

规范工作组主席/规范编辑

Intel Corporation (USB Promoter company)	Yun Ling – Mechanical WG co-chair, Mechanical Chapter Co-editor Brad Saunders – Plenary/Functional WG chair, Specification Co-author
Renesas Electronics Corp. (USB Promoter company)	Bob Dunstan – Functional WG co-chair, Specification Co-author
Seagate	Alvin Cox, Mechanical WG co-chair, Mechanical Chapter Co-editor

规范工作组贡献者

注意：由于历史原因，以下列表还包括在最初的 1.0 版和 2.0 版发布时属于工作组成员且与其公司有关联的个人贡献者。

Advanced-Connectek, Inc. (ACON)	Victory Chen Glen Chandler Dennis Cheung Jeff Chien Lee (Dick Lee) Ching	Conrad Choy Vicky Chuang Jessica Feng Aven Kao Danny Liao	Alan Tsai Wayne Wang Stephen Yang Sunney Yang
Advanced Micro Devices	Steve Capezza Walter Fry Will Harris	Jason Hawken Tim Perley	Joseph Scanlon Peter Teng
Allion Labs, Inc.	Howard Chang Minoru Ohara	Brian Shih	Chester Tsai
Amphenol AssembleTech (Xiamen) Co., Ltd.	Louis Chan Jesse Jaramillo Terry Ke	Martin Li Lino Liu Shawn Wei	Alan Yang
Amphenol Corporation	Zhinenng Fan		
Agilent Technologies, Inc.	James Choate		
Analogix Semiconductor, Inc.	Mehran Badii Greg Stewart	Haijian Sui	Yueke Tang
Apple Inc. (USB Promoter company)	Colin Abraham Mahmoud Amini Sree Anantharaman Brian Baek Paul Baker Michael Bonham Carlos Calderon Jason Chung David Conroy Bill Cornelius Christophe Daniel William Ferry Brian Follis	Zheng Gao Derek Iwamoto Scott Jackson Girault Jones Keong Kam Kevin Keeler Min Kim Woopoung Kim Alexei Kosut Christine Krause Chris Ligtenberg Matthew Mora Nathan Ng	James Orr Keith Porthouse Breton Saunders Reese Schreiber Sascha Tietz Jennifer Tsai Colin Whitby-Strevens Jeff Wilcox Eric Wiles Dan Wilson Dennis Yarak
Bizlink Technology, Inc.	Alex Chou	Morphy Hsieh	

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Cadence Design Systems, Inc.	Marcin Behrendt	Dariusz Kaczmarczyk	Neelabh Singh
	Huzaifa Dalal	Tomasz Klimek	Michal Staworko
	Pawel Eichler	Jie Min	Fred Stivers
	Sathish Kumar Ganesan	Asila Nahas	Mark Summers
		Uyen Nguyen	Claire Ying
Canova Tech	Piergiorgio Beruto	Michael Marioli	Paola Pilla
	Andrea Maniero	Antonio Orzelli	Nicola Scantamburlo
Cirrus Logic Inc.	Sean Davis	Darren Holding	Brad Lambert
Corning Optical Communication LLC	Wojciech Giziewicz	Ian McKay	Jamie Silva
Cosemi Technologies Inc.	Samir Desai	Devang Parekh	
Cypress Semiconductor	Mark Fu	Benjamin Kropf	Jagadeesan Raj
	Naman Jain	Venkat Mandagulathur	Sanjay Sancheti
	Rushil Kadakia	Anup Nayak	Subu Sankaran
Dell	Mohammed Hijazi	Ernesto Ramirez	Thomas Voor
	David Meyers	Siddhartha Reddy	Merle Wood
	Sean O'Neal		
Dialog Semiconductor (UK) Ltd.	Yimin Chen		
Diodes Incorporated	Kay Annamalai	Bob Lo	Qun Song
	Justin Lee	Jaya Shukla	Ada Yip
	Paul Li		
DisplayLink (UK) Ltd.	Pete Burgers		
DJI Technology Co., Ltd.	Steve Huang		
Electronics Testing Center, Taiwan	Sophia Liu		
Elka International Ltd.	Roy Ting		
Ellisys	Abel Astley	Mario Pasquali	Tim Wei
	Rick Bogart	Chuck Trefts	
Etron Technology, Inc.	Chien-Cheng Kuo		
Feature Integration Technologies Inc.	Jacky Chan	KungAn Lin	Paul Yang
	Chen Kris	Yuchi Tsao	Amanda Ying
	Yulin Lan		
Foxconn / Hon Hai	Patrick Casher	Bob Hall	Pei Tsao
	Asroc Chen	Chien-Ping Kao	AJ Yang
	Joe Chen	Ji Li	Yuan Zhang
	Allen Cheng	Ann Liu	Jessica Zheng
	Jason Chou	Terry Little	Jie Zheng
	Edmond Choy	Steve Sedio	Andy Yao
	Fred Fons	Christine Tran	
Foxlink/Cheng Uei Precision Industry Co., Ltd.	Robert Chen	Armando Lee	Steve Tsai
	Sunny Chou	Dennis Lee	Wen Yang
	Carrie Chuang	Justin Lin	Wiley Yang
	Wen-Chuan Hsu	Robert Lu	Junjie Yu
	Alex Hsue	Tse Wu Ting	
Fresco Logic Inc.	Bob McVay	Christopher Meyers	

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Cadence Design Systems, Inc.	Marcin Behrendt	Dariusz Kaczmarczyk	Neelabh Singh
	Huzaifa Dalal	Tomasz Klimek	Michal Staworko
	Pawel Eichler	Jie Min	Fred Stivers
	Sathish Kumar Ganesan	Asila Nahas	Mark Summers
		Uyen Nguyen	Claire Ying
Canova Tech	Piergiorgio Beruto	Michael Marioli	Paola Pilla
	Andrea Maniero	Antonio Orzelli	Nicola Scantamburlo
Cirrus Logic Inc.	Sean Davis	Darren Holding	Brad Lambert
Corning Optical Communication LLC	Wojciech Giziewicz	Ian McKay	Jamie Silva
Cosemi Technologies Inc.	Samir Desai	Devang Parekh	
Cypress Semiconductor	Mark Fu	Benjamin Kropf	Jagadeesan Raj
	Naman Jain	Venkat Mandagulathur	Sanjay Sancheti
	Rushil Kadakia	Anup Nayak	Subu Sankaran
Dell	Mohammed Hijazi	Ernesto Ramirez	Thomas Voor
	David Meyers	Siddhartha Reddy	Merle Wood
	Sean O'Neal		
Dialog Semiconductor (UK) Ltd.	Yimin Chen		
Diodes Incorporated	Kay Annamalai	Bob Lo	Qun Song
	Justin Lee	Jaya Shukla	Ada Yip
	Paul Li		
DisplayLink (UK) Ltd.	Pete Burgers		
DJI Technology Co., Ltd.	Steve Huang		
Electronics Testing Center, Taiwan	Sophia Liu		
Elka International Ltd.	Roy Ting		
Ellisys	Abel Astley	Mario Pasquali	Tim Wei
	Rick Bogart	Chuck Trefts	
Etron Technology, Inc.	Chien-Cheng Kuo		
Feature Integration Technologies Inc.	Jacky Chan	KungAn Lin	Paul Yang
	Chen Kris	Yuchi Tsao	Amanda Ying
	Yulin Lan		
Foxconn / Hon Hai	Patrick Casher	Bob Hall	Pei Tsao
	Asroc Chen	Chien-Ping Kao	AJ Yang
	Joe Chen	Ji Li	Yuan Zhang
	Allen Cheng	Ann Liu	Jessica Zheng
	Jason Chou	Terry Little	Jie Zheng
	Edmond Choy	Steve Sedio	Andy Yao
	Fred Fons	Christine Tran	
Foxlink/Cheng Uei Precision Industry Co., Ltd.	Robert Chen	Armando Lee	Steve Tsai
	Sunny Chou	Dennis Lee	Wen Yang
	Carrie Chuang	Justin Lin	Wiley Yang
	Wen-Chuan Hsu	Robert Lu	Junjie Yu
	Alex Hsue	Tse Wu Ting	
Fresco Logic Inc.	Bob McVay	Christopher Meyers	

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Google	Alec Berg	Nithya Jagannathan	Adam Rodriguez
	Joshua Boilard	Lawrence Lam	David Schneider
	Alec Berg	Adam Langley	Stephan Schooley
	Todd Broch	Ingrid Lin	Toshak Singhal
	Jim Guerin	Richard Palatin	Ken Wu
	Jeffrey Hayashida	Vincent Palatin	
	Mark Hayter	Dylan Reid	
Granite River Labs	Yung Han Ang	Alan Chuang	Krishna Murthy
	Sandy Chang	Mike Engbretson	Johnson Tan
	Allen Chen	Caspar Lin	Chin Hun Yaep
	Swee Guan Chua		
Hewlett Packard Inc. (USB Promoter company)	Lee Atkinson	Robin Castell	Jim Mann
	Srinath Balaraman	Steve Chen	Linden McClure
	Roger Benson	Michael Krause	Mike Pescetto
	Alan Berkema	Rahul Lakdawala	Asjad Shamim
Hirose Electric Co., Ltd.	Jeremy Buan	William MacKillop	Eungsoo Shin
	William Kysiak	Gourgen Oganessyan	Sid Tono
	Sang-Muk Lim		
Hosiden Corporation	Takahisa Otsuji	Fumitake Tamaki	
I-PEX (Dai-ichi Seiko)	Alan Kinningham	Ro Richard	Tetsuya Tagawa
Infineon Technologies	Tue Fatt David Wee		
Intel Corporation (USB Promoter company)	Dave Ackelson	Ziv Kabiry	Sridharan Ranganathan
	Mike Bell	Vijaykumar Kadgi	Rajaram Regupathy
	Brad Berlin	Luke Johnson	Brad Saunders
	Pierre Bossart	Jerzy Kolinski	Ehud Shoor
	Kuan-Yu Chen	Rolf Kuhnis	Amit Srivastava
	Hengju Cheng	Henrik Leegaard	Einat Surijan
	Jhuda Dayan	Edmond Lau	Ron Swartz
	Paul Durley	Xiang Li	David Thompson
	Saranya Gopal	Yun Ling	Karthi Vadivelu
	Howard Heck	Guobin Liu	Tsion Vidal
	Hao-Han Hsu	Steve McGowan	Stephanie Wallick
	Seppo Ingalsuo	Sankaran Menon	Rafal Wielicki
	Abdul (Rahman) Ismail	Chee Lim Nge	Devon Worrell
	James Jaussi	Sagar Pawar	Li Yuan
Japan Aviation Electronics Industry Ltd. (JAE)	Kenji Hagiwara	Tadashi Okubo	Masaaki Takaku
	Hiroaki Ikeda	Kazuhiro Saito	Jussi Takaneva
	Masaki Kimura	Kimiaki Saito	Tomohiko Tamada
	Toshio Masumoto	Yuichi Saito	Kentaro Toda
	Kenta Minejima	Mark Saubert	Kouhei Ueda
	Toshiyuki Moritake	Toshio Shimoyama	Takakazu Usami
	Joe Motojima	Tatsuya Shioda	Masahide Watanabe
	Ron Muir	Atsuo Tago	Youhei Yokoyama
JPC/Main Super Inc.	Sam Tseng	Ray Yang	
LeCroy Corporation	Daniel H. Jacobs	Tyler Joe	

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Google	Alec Berg Joshua Boilard Alec Berg Todd Broch Jim Guerin Jeffrey Hayashida Mark Hayter	Nithya Jagannathan Lawrence Lam Adam Langley Ingrid Lin Richard Palatin Vincent Palatin Dylan Reid	Adam Rodriguez David Schneider Stephan Schooley Toshak Singhal Ken Wu
Granite River Labs	Yung Han Ang Sandy Chang Allen Chen Swee Guan Chua	Alan Chuang Mike Engbretson Caspar Lin	Krishna Murthy Johnson Tan Chin Hun Yaep
Hewlett Packard Inc. (USB Promoter company)	Lee Atkinson Srinath Balaraman Roger Benson Alan Berkema	Robin Castell Steve Chen Michael Krause Rahul Lakdawala	Jim Mann Linden McClure Mike Pescetto Asjad Shamim
Hirose Electric Co., Ltd.	Jeremy Buan William Kysiak Sang-Muk Lim	William MacKillop Gourgen Oganessyan	Eungsoo Shin Sid Tono
Hosiden Corporation	Takahisa Otsuji	Fumitake Tamaki	
I-PEX (Dai-ichi Seiko)	Alan Kinningham	Ro Richard	Tetsuya Tagawa
Infineon Technologies	Tue Fatt David Wee		
Intel Corporation (USB Promoter company)	Dave Ackelson Mike Bell Brad Berlin Pierre Bossart Kuan-Yu Chen Hengju Cheng Jhuda Dayan Paul Durley Saranya Gopal Howard Heck Hao-Han Hsu Seppo Ingalsuo Abdul (Rahman) Ismail James Jaussi	Ziv Kabiry Vijaykumar Kadgi Luke Johnson Jerzy Kolinski Rolf Kuhnis Henrik Leegaard Edmond Lau Xiang Li Yun Ling Guobin Liu Steve McGowan Sankaran Menon Chee Lim Nge Sagar Pawar	Sridharan Ranganathan Rajaram Regupathy Brad Saunders Ehud Shoor Amit Srivastava Einat Surijan Ron Swartz David Thompson Karthi Vadivelu Tsion Vidal Stephanie Wallick Rafal Wielicki Devon Worrell Li Yuan
Japan Aviation Electronics Industry Ltd. (JAE)	Kenji Hagiwara Hiroaki Ikeda Masaki Kimura Toshio Masumoto Kenta Minejima Toshiyuki Moritake Joe Motojima Ron Muir	Tadashi Okubo Kazuhiro Saito Kimiaki Saito Yuichi Saito Mark Saubert Toshio Shimoyama Tatsuya Shioda Atsuo Tago	Masaaki Takaku Jussi Takaneva Tomohiko Tamada Kentaro Toda Kouhei Ueda Takakazu Usami Masahide Watanabe Youhei Yokoyama
JPC/Main Super Inc.	Sam Tseng	Ray Yang	
LeCroy Corporation	Daniel H. Jacobs	Tyler Joe	

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Lenovo	Rob Bowser Tomoki Harada	Jianye Li Wei Liu	Howard Locker
LG Electronics Inc.	Do Kyun Kim		
Lintes Technology Co., Ltd.	Tammy Huang Charles Kaun RD Lintes	Max Lo CT Pien	JinYi Tu Jason Yang
Lotes Co., Ltd.	Ariel Delos Reyes Ernest Han Mark Ho Regina Liu-Hwang	Charles Kaun Chi-Chang Lin Max Lo	John Lynch JinYi Tu Jason Yang
LSI Corporation	Dave Thompson		
Luxshare-ICT	Josue Castillo Daniel Chen Lisen Chen Sally Chiu CY Hsu	Alan Kinningham Gorden Lin John Lin Stone Lin Alan Liu	Sean O'Neal Scott Shuey James Stevens Pat Young
Maxim Integrated Products	Forrest Christo Ken Helfrich	Sang Kim Jeff Lo	Michael Miskho Jacob Scott
MCCI Corporation	Terry Moore		
MediaTek Inc.	Alex YC Lin		
MegaChips Corporation	Alan Kobayashi	Satoru Kumashiro	
Microchip (SMSC)	Josh Averyt Mark Bohm Shannon Cash Thomas Farkas Fernando Gonzalez	Matthew Kalibat Donald Perkins Richard Petrie Mohammed Rahman Andrew Rogers	John Sisto Anthony Tarascio Kiet Tran Christopher Twigg Prasanna Vengateshan
Microsoft Corporation (USB Promoter company)	Randy Aull Jim Belesiu Michelle Bergeron Fred Bhesania Anthony Chen Philip Froese Vivek Gupta David Hargrove Robbie Harris Robert Hollyer	Teemu Helenius Dan Iatco Kai Inha Jayson Kastens Andrea Keating Shoaib Khan Eric Lee Ivan McCracken Arvind Murching Gene Obie	Toby Nixon Rahul Ramadas Srivatsan Ravindran Nathan Sherman Bala Sivakumar Timo Toivola David Voth Andrew Yang Panu Ylihaavisto
Molex LLC	Adib Al Abaji	Alan MacDougall	
Monolithic Power Systems	Di Han	Chris Sporck	
MQP Electronics Ltd.	Sten Carlsen	Pat Crowe	
NEC Corporation	Kenji Oguma		
Newnex Technology Corp.	Sam Liu	Nimrod Peled	
Nokia Corporation	Daniel Gratiot Pekka Leinonen	Samuli Makinen Pekka Talmola	Timo Toivola Panu Ylihaavisto
NXP Semiconductors	Mahmoud EL Sabbagh Dennis Ha	Ken Jaramillo Vijendra Kuroodi	Guru Prasad Krishnan TN
Oculus VR LLC	Amish Babu	Marty Evans	Joaquin Fierro

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Lenovo	Rob Bowser Tomoki Harada	Jianye Li Wei Liu	Howard Locker
LG Electronics Inc.	Do Kyun Kim		
Lintes Technology Co., Ltd.	Tammy Huang Charles Kaun RD Lintes	Max Lo CT Pien	JinYi Tu Jason Yang
Lotes Co., Ltd.	Ariel Delos Reyes Ernest Han Mark Ho Regina Liu-Hwang	Charles Kaun Chi-Chang Lin Max Lo	John Lynch JinYi Tu Jason Yang
LSI Corporation	Dave Thompson		
Luxshare-ICT	Josue Castillo Daniel Chen Lisen Chen Sally Chiu CY Hsu	Alan Kinningham Gorden Lin John Lin Stone Lin Alan Liu	Sean O'Neal Scott Shuey James Stevens Pat Young
Maxim Integrated Products	Forrest Christo Ken Helfrich	Sang Kim Jeff Lo	Michael Miskho Jacob Scott
MCCI Corporation	Terry Moore		
MediaTek Inc.	Alex YC Lin		
MegaChips Corporation	Alan Kobayashi	Satoru Kumashiro	
Microchip (SMSC)	Josh Averyt Mark Bohm Shannon Cash Thomas Farkas Fernando Gonzalez	Matthew Kalibat Donald Perkins Richard Petrie Mohammed Rahman Andrew Rogers	John Sisto Anthony Tarascio Kiet Tran Christopher Twigg Prasanna Vengateshan
Microsoft Corporation (USB Promoter company)	Randy Aull Jim Belesiu Michelle Bergeron Fred Bhesania Anthony Chen Philip Froese Vivek Gupta David Hargrove Robbie Harris Robert Hollyer	Teemu Helenius Dan Iatco Kai Inha Jayson Kastens Andrea Keating Shoaib Khan Eric Lee Ivan McCracken Arvind Murching Gene Obie	Toby Nixon Rahul Ramadas Srivatsan Ravindran Nathan Sherman Bala Sivakumar Timo Toivola David Voth Andrew Yang Panu Ylihaavisto
Molex LLC	Adib Al Abaji	Alan MacDougall	
Monolithic Power Systems	Di Han	Chris Sporck	
MQP Electronics Ltd.	Sten Carlsen	Pat Crowe	
NEC Corporation	Kenji Oguma		
Newnex Technology Corp.	Sam Liu	Nimrod Peled	
Nokia Corporation	Daniel Gratiot Pekka Leinonen	Samuli Makinen Pekka Talmola	Timo Toivola Panu Ylihaavisto
NXP Semiconductors	Mahmoud EL Sabbagh Dennis Ha	Ken Jaramillo Vijendra Kuroodi	Guru Prasad Krishnan TN
Oculus VR LLC	Amish Babu	Marty Evans	Joaquin Fierro

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

ON Semiconductor	Eduardo De Reza Oscar Freitas	Christian Klein Amir Lahooti	Michael Smith
Parade Technologies, Inc.	Jian Chen Craig Wiley	Paul Xu	Alan Yuen
Power Integrations	Shruti Anand Rahul Joshi	Aditya Kulkarni Akshay Nayaknur	Amruta Patra
Qualcomm, Inc.	Lior Amarilio Aris Balatsos Tomer Ben Chen Richard Burrows Amit Gil James Goel Amit Gupta	Philip Hardy Will Kun Jonathan Luty Lalan Mishra George Paparrizos Vatsal Patel	Jack Pham Vamsi Samavedam Matthew Sienko Dmitrii Vasilchenko Joshua Warner Chris Wiesner
Realtek Semiconductor Corp.	Marco Chiu Tsung-Peng Chuang Charlie Hsu Fan-Hau Hsu	Ty Kingsmore Ray Lee Jay Lin Ryan Lin	Terry Lin Chuting Su Changhung Wu
Renesas Electronics Corp. (USB Promoter company)	Kai Bao Bob Dunstan Nobuo Furuya	Philip Leung Kiichi Muto Ziba Nami	Hajime Nozaki Yosuke Sasaki Toshifumi Yamaoka
Richtek Technology Corp.	Roger Lo		
Rohm Co., Ltd.	Mark Aaldering Kris Bahar Ruben Balbuena Nobutaka Itakura	Yusuke Kondo Arun Kumar Chris Lin Kazuomi Nagai	Yoshinori Ohwaki Takashi Sato Hiroshi Yoshimura
Samsung Electronics Co., Ltd.	Jaedeok Cha KangSeok Cho Wooin Choi Yeongbok Choi Cheolyoon Chung JaeRyong Han Jaehyeok Jang Wonseok Jang	Sangju Kim Soondo Kim Woonki Kim Jagoun Koo Termi Kwon Cheolho Lee Edward Lee	Jun Bum Lee Jinyoung Oh Chahoon Park Chulwoo Park Youngjin Park Jung Waneui Sunggeun Yoon
Seagate	Alvin Cox Emmanuel Lemay	Tony Priborsky Tom Skaar	Dan Smith
Shenzhen Deren Electronic Co., Ltd.	Smark (Zhudong) Huo Wen Fa Lei	Yang Lirong	Lucy Zhang
Silicon Line Gmbh	Ian Jackson		
SiliConch Systems Private Limited	Jaswanth Ammineni Pavitra Balasubramanian Kaustubh Kumar Aniket Mathad	Shubham Paliwal Jinisha Patel Vinay Patel Rakesh Polasa	Vishnu Pusuluri Abhishek Sardeshpande Satish Anand Verkila
Simula Technology Inc.	John Chang Voss Cheng Thomas Li	Jung Lin Jyunming Lin Doris Liu	CK Wang Alice Yu
Softnautics LLP	Bhavesh Desai Hetal Jariwala	Dipakkumar Modi Ishita Shah	Ujjwal Talati

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

ON Semiconductor	Eduardo De Reza Oscar Freitas	Christian Klein Amir Lahooti	Michael Smith
Parade Technologies, Inc.	Jian Chen Craig Wiley	Paul Xu	Alan Yuen
Power Integrations	Shruti Anand Rahul Joshi	Aditya Kulkarni Akshay Nayaknur	Amruta Patra
Qualcomm, Inc.	Lior Amarilio Aris Balatsos Tomer Ben Chen Richard Burrows Amit Gil James Goel Amit Gupta	Philip Hardy Will Kun Jonathan Luty Lalan Mishra George Paparrizos Vatsal Patel	Jack Pham Vamsi Samavedam Matthew Sienko Dmitrii Vasilchenko Joshua Warner Chris Wiesner
Realtek Semiconductor Corp.	Marco Chiu Tsung-Peng Chuang Charlie Hsu Fan-Hau Hsu	Ty Kingsmore Ray Lee Jay Lin Ryan Lin	Terry Lin Chuting Su Changhung Wu
Renesas Electronics Corp. (USB Promoter company)	Kai Bao Bob Dunstan Nobuo Furuya	Philip Leung Kiichi Muto Ziba Nami	Hajime Nozaki Yosuke Sasaki Toshifumi Yamaoka
Richtek Technology Corp.	Roger Lo		
Rohm Co., Ltd.	Mark Aaldering Kris Bahar Ruben Balbuena Nobutaka Itakura	Yusuke Kondo Arun Kumar Chris Lin Kazuomi Nagai	Yoshinori Ohwaki Takashi Sato Hiroshi Yoshimura
Samsung Electronics Co., Ltd.	Jaedeok Cha KangSeok Cho Wooin Choi Yeongbok Choi Cheolyoon Chung JaeRyong Han Jaehyeok Jang Wonseok Jang	Sangju Kim Soondo Kim Woonki Kim Jagoun Koo Termi Kwon Cheolho Lee Edward Lee	Jun Bum Lee Jinyoung Oh Chahoon Park Chulwoo Park Youngjin Park Jung Waneui Sunggeun Yoon
Seagate	Alvin Cox Emmanuel Lemay	Tony Priborsky Tom Skaar	Dan Smith
Shenzhen Deren Electronic Co., Ltd.	Smark (Zhudong) Huo Wen Fa Lei	Yang Lirong	Lucy Zhang
Silicon Line Gmbh	Ian Jackson		
SiliConch Systems Private Limited	Jaswanth Ammineni Pavitra Balasubramanian Kaustubh Kumar Aniket Mathad	Shubham Paliwal Jinisha Patel Vinay Patel Rakesh Polasa	Vishnu Pusuluri Abhishek Sardeshpande Satish Anand Verkila
Simula Technology Inc.	John Chang Voss Cheng Thomas Li	Jung Lin Jyunming Lin Doris Liu	CK Wang Alice Yu
Softnautics LLP	Bhavesh Desai Hetal Jariwala	Dipakkumar Modi Ishita Shah	Ujjwal Talati

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Sony Corporation	Shinichi Hirata	Shigenori Tagami	
Spectra7 Microsystems Corp.	Andrew Kim	James McGrath	John Mitchell
Specwerkz	Amanda Hosler	Diane Lenox	
STMicroelectronics (USB Promoter company)	Jerome Bach Nathalie Ballot Filippo Bonaccorso Christophe Cochard Nicolas Florenchie Cedric Force	Gregory Cosciniak Chekib Hammami Joel Huloux Christophe Lorin Patrizia Milazzo Federico Musarra	Pascal Legrand Richard O'Connor Massimo Panzica Legrand Pascal Nicolas Perrin
Sumitomo Electric Ind., Ltd.	Takeshi Inoue Yasuhiro Maeda	Wataru Sakurai Sainer Siagian	Masaki Suzuki Mitsuaki Tamura
Synaptics Inc.	Daniel Bogard	Jeff Lukanc	Prashant Shamarao
Synopsys, Inc.	Subramaniam Aravindhan	Morten Christiansen Nivin George	Satya Patnala
Tektronix, Inc.	Randy White		
Texas Instruments (USB Promoter company)	Jawaid Ahmad Mike Campbell Greg Collins Gary Cooper GP Gopalakrishnan Craig Greenberg Richard Hubbard Nate Johnson Michael Koltun IV Yoon Lee Grant Ley	Win Maung Shafiuddin Mohammed Lauren Moore Brian Parten Martin Patoka Jason Peck John Perry Louis Peryea Brian Quach	Sai Karthik Rajaraman Wes Ray Dafydd Roche Anwar Sadat Cory Stewart Sue Vining Bill Waters Deric Waters Gregory Watkins Roy Wojciechowski
Total Phase	Chris Yokum		
Tyco Electronics Corp. (TE Connectivity Ltd.)	Max Chao Robert E. Cid Calvin Feng Kengo Ijiro Eiji Ikematsu Joan Leu Clark Li	Mike Lockyer Jeff Mason Takeshi Nakashima Luis A. Navarro Masako Saito Yoshiaki Sakuma Gavin Shih	Hiroshi Shirai Hidenori Taguchi Nathan Tracy Bernard Vetten Ryan Yu Noah Zhang Sjoerd Zwartkruis
UL LLC	Michael Hu		
Varjo Technologies	Kai Inha		
Ventev Mobile	Brad Cox	Colin Vose	
VIA Technologies Inc.	Terrance Shih	Jay Tseng	Fong-Jim Wang
Weltrend Semiconductor	Hung Chiang Jeng Cheng	Wayne Lo Ho Wen Tsai	Eric Wu
Xiaomi Communications Co., Ltd.	Xiaoxing Yang	Juejia Zhou	

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Sony Corporation	Shinichi Hirata	Shigenori Tagami	
Spectra7 Microsystems Corp.	Andrew Kim	James McGrath	John Mitchell
Specwerkz	Amanda Hosler	Diane Lenox	
STMicroelectronics (USB Promoter company)	Jerome Bach Nathalie Ballot Filippo Bonaccorso Christophe Cochard Nicolas Florenchie Cedric Force	Gregory Cosciniak Chekib Hammami Joel Huloux Christophe Lorin Patrizia Milazzo Federico Musarra	Pascal Legrand Richard O'Connor Massimo Panzica Legrand Pascal Nicolas Perrin
Sumitomo Electric Ind., Ltd.	Takeshi Inoue Yasuhiro Maeda	Wataru Sakurai Sainer Siagian	Masaki Suzuki Mitsuaki Tamura
Synaptics Inc.	Daniel Bogard	Jeff Lukanc	Prashant Shamarao
Synopsys, Inc.	Subramaniam Aravindhan	Morten Christiansen Nivin George	Satya Patnala
Tektronix, Inc.	Randy White		
Texas Instruments (USB Promoter company)	Jawaid Ahmad Mike Campbell Greg Collins Gary Cooper GP Gopalakrishnan Craig Greenberg Richard Hubbard Nate Johnson Michael Koltun IV Yoon Lee Grant Ley	Win Maung Shafiuddin Mohammed Lauren Moore Brian Parten Martin Patoka Jason Peck John Perry Louis Peryea Brian Quach	Sai Karthik Rajaraman Wes Ray Dafydd Roche Anwar Sadat Cory Stewart Sue Vining Bill Waters Deric Waters Gregory Watkins Roy Wojciechowski
Total Phase	Chris Yokum		
Tyco Electronics Corp. (TE Connectivity Ltd.)	Max Chao Robert E. Cid Calvin Feng Kengo Ijiro Eiji Ikematsu Joan Leu Clark Li	Mike Lockyer Jeff Mason Takeshi Nakashima Luis A. Navarro Masako Saito Yoshiaki Sakuma Gavin Shih	Hiroshi Shirai Hidenori Taguchi Nathan Tracy Bernard Vetten Ryan Yu Noah Zhang Sjoerd Zwartkruis
UL LLC	Michael Hu		
Varjo Technologies	Kai Inha		
Ventev Mobile	Brad Cox	Colin Vose	
VIA Technologies Inc.	Terrance Shih	Jay Tseng	Fong-Jim Wang
Weltrend Semiconductor	Hung Chiang Jeng Cheng	Wayne Lo Ho Wen Tsai	Eric Wu
Xiaomi Communications Co., Ltd.	Xiaoxing Yang	Juejia Zhou	

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Pre-Release Draft Industry Reviewing Companies That Provided Feedback

Aces
Fairchild Semiconductor
Fujitsu Ltd.
Industrial Technology Research Institute (ITRI)
Joinsoon Electronics Mfg. Co. Ltd.
JST Mfg. Co., Ltd.
Korea Electric Terminal
Marvell Semiconductor
Motorola Mobility LLC
PalCONN/PalNova (Palpilot International Corp.)
Pericom
Semtech Corporation
Silicon Image
SMK Corporation
Toshiba Corporation

Revision History

Revision	Date	Description
1.0	August 11, 2014	Initial Release
1.1	April 3, 2015	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.2	March 25, 2016	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.3	July 14, 2017	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.4	March 29, 2019	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
2.0	August 2019	New release primarily for enabling USB4 over USB Type-C connectors and cables. Also includes incorporation of all approved ECNs as of the revision date plus editorial clean-up.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

发布前草案行业审查提供反馈的公司

Aces Fairchild Semiconductor 富士通有限公司 工业技术研究院 (ITRI) 锦顺电子制造有限公司

JST Mfg. Co., Ltd. 韩国电气终端 Marvell Semiconductor Motorola Mobility LLC PalCONN/PalNova (Palpilot International Corp.)

Pericom Semtech 公司

Silicon Image SMK 公司 东芝公司

修订历史

Revision	Date	Description
1.0	August 11, 2014	Initial Release
1.1	April 3, 2015	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.2	March 25, 2016	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.3	July 14, 2017	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.4	March 29, 2019	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
2.0	August 2019	New release primarily for enabling USB4 over USB Type-C connectors and cables. Also includes incorporation of all approved ECNs as of the revision date plus editorial clean-up.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

1 Introduction

With the continued success of the USB interface, there exists a need to adapt USB technology to serve newer computing platforms and devices as they trend toward smaller, thinner and lighter form-factors. Many of these newer platforms and devices are reaching a point where existing USB receptacles and plugs are inhibiting innovation, especially given the relatively large size and internal volume constraints of the Standard-A and Standard-B versions of USB connectors. Additionally, as platform usage models have evolved, usability and robustness requirements have advanced and the existing set of USB connectors were not originally designed for some of these newer requirements. This specification is to establish a new USB connector ecosystem that addresses the evolving needs of platforms and devices while retaining all of the functional benefits of USB that form the basis for this most popular of computing device interconnects.

1.1 Purpose

This specification defines the USB Type-C® receptacles, plug and cables.

The USB Type-C Cable and Connector Specification is guided by the following principles:

- Enable new and exciting host and device form-factors where size, industrial design and style are important parameters
- Work seamlessly with existing USB host and device silicon solutions
- Enhance ease of use for connecting USB devices with a focus on minimizing user confusion for plug and cable orientation

The USB Type-C Cable and Connector Specification defines a new receptacle, plug, cable and detection mechanisms that are compatible with existing USB interface electrical and functional specifications. This specification covers the following aspects that are needed to produce and use this new USB cable/connector solution in newer platforms and devices, and that interoperate with existing platforms and devices:

- USB Type-C receptacles, including electro-mechanical definition and performance requirements
- USB Type-C plugs and cable assemblies, including electro-mechanical definition and performance requirements
- USB Type-C to legacy cable assemblies and adapters
- USB Type-C-based device detection and interface configuration, including support for legacy connections
- USB Power Delivery optimized for the USB Type-C connector

The USB Type-C Cable and Connector Specification defines a standardized mechanism that supports Alternate Modes, such as repurposing the connector for docking-specific applications.

1.2 Scope

This specification is intended as a supplement to the existing *USB 2.0*, *USB 3.2*, *USB4™* and *USB Power Delivery* specifications. It addresses only the elements required to implement and support the USB Type-C receptacles, plugs and cables.

Normative information is provided to allow interoperability of components designed to this specification. Informative information, when provided, may illustrate possible design implementations.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

1 简介

随着 USB 接口的持续成功，需要调整 USB 技术以适应新的计算平台和设备，因为它们正朝着更小、更薄、更轻的外形发展。许多新的平台和设备已经达到现有 USB 插座和插头阻碍创新的程度，尤其是考虑到标准 A 和标准 B 版 USB 连接器的相对较大尺寸和内部容量限制。此外，随着平台使用模式的发展，可用性和稳健性要求也不断提高，而现有的 USB 连接器最初并不是为满足这些新要求而设计的。本规范旨在建立一个新的 USB 连接器生态系统，以满足平台和设备不断变化的需求，同时保留 USB 的所有功能优势，这些优势构成了这种最流行的计算设备互连的基础。

1.1 目的

该规范定义了 USB Type-C® 插座、插头和电缆。

USB Type-C 电缆和连接器规范遵循以下原则：

- 实现全新且令人兴奋的主机和设备外形尺寸，包括尺寸、工业设计和样式是重要参数
- 与现有 USB 主机和设备硅片解决方案无缝协作
- 增强连接 USB 设备的易用性，重点是尽量减少用户对插头和电缆方向的混淆

USB Type-C 电缆和连接器规范定义了与现有 USB 接口电气和功能规范兼容的新插座、插头、电缆和检测机制。此规范涵盖了在较新的平台和设备中生产和使用此新 USB 电缆/连接器解决方案所需的以下方面，以及与现有平台和设备的互操作性：

- USB Type-C 插座，包括机电定义和性能要求
- USB Type-C 插头和电缆组件，包括机电定义和性能要求
- USB Type-C 转传统电缆组件和适配器
- 基于 USB Type-C 的设备检测和接口配置，包括对传统连接的支持
- 针对 USB Type-C 连接器优化的 USB 供电

USB Type-C 电缆和连接器规范定义了一种支持备用模式的标准化机制，例如将连接器重新用于特定于对接的应用程序。

1.2 范围

本规范旨在补充现有的 *USB 2.0*、*USB 3.2*、*USB4™* 和 *USB Power Delivery* 规范。它仅涉及实施和支持 USB Type-C 插座、插头和电缆所需的元素。

提供规范性信息是为了实现按照本规范设计的组件之间的互操作性。提供的信息性信息可以说明可能的设计实现。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

1.3 Related Documents

USB 2.0 *Universal Serial Bus Revision 2.0 Specification*
This includes the entire document release package.

USB 3.2 *Universal Serial Bus Revision 3.2 Specification*
This includes the entire document release package.
USB 3.1 Legacy Cable and Connector Specification, Revision 1.0

USB4 *USB4™ Specification, Version 1.0, August 2019*
(including posted errata and ECNs)

TBT3 Chapter 13 of *USB4 Specification, Version 1.0, August 2019*

USB PD *USB Power Delivery Specification, Revision 2.0, Version 1.3, January 12, 2017*
USB Power Delivery Specification, Revision 3.0, Version 2.0, August 2019
(including posted errata and ECNs)

USB BB *USB Billboard Device Class Specification, Revision 1.21, September 8, 2016*

USB BC *Battery Charging Specification, Revision 1.2 (including errata and ECNs through March 15, 2012), March 15, 2012*

DP AM *DisplayPort™ Alt Mode on USB Type-C Standard, Version 1.0b, 03 November 2017*

All USB-specific documents are available for download at http://www.usb.org/documents. The DisplayPort Alt Mode specification is available from VESA (http://www.vesa.org).

1.4 Conventions

1.4.1 Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, and then text.

1.4.2 Keywords

The following keywords differentiate between the levels of requirements and options.

1.4.2.1 Informative

Informative is a keyword that describes information with this specification that intends to discuss and clarify requirements and features as opposed to mandating them.

1.4.2.2 May

May is a keyword that indicates a choice with no implied preference.

1.4.2.3 N/A

N/A is a keyword that indicates that a field or value is not applicable and has no defined value and shall not be checked or used by the recipient.

1.4.2.4 Normative

Normative is a keyword that describes features that are mandated by this specification.

1.4.2.5 Optional

Optional is a keyword that describes features not mandated by this specification. However, if an optional feature is implemented, the feature shall be implemented as defined by this specification (optional normative).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

1.3 相关文档

USB 2.0 *Universal Serial Bus Revision 2.0 Specification* 包括整个文档发布包。 USB 3.2 *Universal Serial Bus Revision 3.2 Specification* 包括整个文档发布包。
USB 3.1 Legacy Cable and Connector Specification, Revision 1.0 USB4
USB4™ Specification, Version 1.0, August 2019 (including posted errata and ECNs) TBT3 第 13 章 *USB4 Specification, Version 1.0, August 2019* USB PD
USB Power Delivery Specification, Revision 2.0, Version 1.3, January 12, 2017
USB Power Delivery Specification, Revision 3.0, Version 2.0, August 2019 (including posted errata and ECNs) USB BB
USB Billboard Device Class Specification, Revision 1.21, September 8, 2016 USB BC
Battery Charging Specification, Revision 1.2 (including errata and ECNs through March 15, 2012), March 15, 2012 DP AM
DisplayPort™ Alt Mode on USB Type-C Standard, Version 1.0b, 03 November 2017

所有 USB 特定文档均可从 http://www.usb.org/documents 下载。
DisplayPort Alt Mode 规范可从 VESA (http://www.vesa.org) 获得。

1.4 约定

1.4.1 优先级

若文、图、表三者有冲突，则以表格、图、文为优先。

1.4.2 关键字

以下关键字区分要求和选项的级别。

1.4.2.1 信息性

信息性是一个关键词，它描述此规范的信息，旨在讨论和澄清要求和特性，而不是强制要求它们。

1.4.2.2 五月

May 是一个表示选择但并不包含任何偏好的关键词。

1.4.2.3 不适用

N/A 是一个关键字，表示某个字段或值不适用且没有定义的值，不应被接收者检查或使用。

1.4.2.4 规范性

规范是关键 描述功能所要求的 是规范。

1.4.2.5 可选

Optional 是描述本规范未强制要求的功能的关键字。但是，如果实现了可选功能，则应按照本规范的定义实现该功能（可选规范）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

1.4.2.6 Reserved

Reserved is a keyword indicating reserved bits, bytes, words, fields, and code values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this specification and, unless otherwise stated, shall not be utilized or adapted by vendor implementation. A reserved bit, byte, word, or field shall be set to zero by the sender and shall be ignored by the receiver. Reserved field values shall not be sent by the sender and, if received, shall be ignored by the receiver.

1.4.2.7 Shall

Shall is a keyword indicating a mandatory (normative) requirement. Designers are mandated to implement all such requirements to ensure interoperability with other compliant Devices.

1.4.2.8 Should

Should is a keyword indicating flexibility of choice with a preferred alternative. Equivalent to the phrase "it is recommended that".

1.4.3 Numbering

Numbers that are immediately followed by a lowercase "b" (e.g., 01b) are binary values. Numbers that are immediately followed by an uppercase "B" are byte values. Numbers that are immediately followed by a lowercase "h" (e.g., 3Ah) are hexadecimal values. Numbers not immediately followed by either a "b", "B", or "h" are decimal values.

1.5 Terms and Abbreviations

Term	Description
Accessory Mode	A reconfiguration of the connector based on the presence of Rd/Rd or Ra/Ra on CC1/CC2, respectively.
Active cable	Active cables are USB Full-Featured Type-C Cables that incorporate repeaters in the *USB 3.2* data path. All active cables, regardless of length, are expected to comply with this specification, the *USB 3.2* Appendix E, and the *USB 3.2* active cable CTS. Active cables may incorporate repeaters in both ends of the cable, one end, or anywhere in the cable.
Alternate Mode	Operation defined by a vendor or standards organization that is associated with a SVID assigned by the USB-IF. Entry and exit into and from an Alternate Mode is controlled by the *USB PD* Structured VDM Enter Mode and Exit Mode commands.
Alternate Mode Adapter (AMA)	A *USB PD* Device which supports Alternate Modes and acts as a UFP.
Audio Adapter Accessory Mode	The Accessory Mode defined by the presence of Ra/Ra on CC1/CC2, respectively. See Appendix A.
BMC	Biphase Mark Coding used for *USB PD* communication over the CC wire.
Cable Port Partner	The USB Type-C DRP, Source, or Sink connected to the cable plug.
Captive cable	A cable that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

1.4.2.6 保留

保留是一个关键字，表示为将来标准化而预留的保留位、字节、字、字段和代码值。它们的使用和解释可能由本规范的未来扩展指定，除非另有说明，否则供应商实施不得使用或改编。发送方应将保留的位、字节、字或字段设置为零，接收方应忽略这些保留字段值。发送方不得发送保留字段值，如果接收方收到这些字段值，则应忽略这些字段值。

1.4.2.7 应当

“ Shall ” 是一个关键字，表示强制性（规范性）要求。设计人员必须实施所有此类要求，以确保与其他兼容设备的互操作性。

1.4.2.8 应

应该是一个关键词，表示选择的灵活性，并有首选的替代方案。相当于短语 “ 建议 ” 。

1.4.3 编号

后面紧跟着小写字母 “ b ” （例如 01b）的数字是二进制值。后面紧跟着大写字母 “ B ” 的数字是字节值。后面紧跟着小写字母 “ h ” （例如 3Ah）的数字是十六进制值。后面没有紧跟着 “ b ” 、 “ B ” 或 “ h ” 的数字是十进制值。

1.5 术语和缩写

Term	Description
Accessory Mode	A reconfiguration of the connector based on the presence of Rd/Rd or Ra/Ra on CC1/CC2, respectively.
Active cable	Active cables are USB Full-Featured Type-C Cables that incorporate repeaters in the *USB 3.2* data path. All active cables, regardless of length, are expected to comply with this specification, the *USB 3.2* Appendix E, and the *USB 3.2* active cable CTS. Active cables may incorporate repeaters in both ends of the cable, one end, or anywhere in the cable.
Alternate Mode	Operation defined by a vendor or standards organization that is associated with a SVID assigned by the USB-IF. Entry and exit into and from an Alternate Mode is controlled by the *USB PD* Structured VDM Enter Mode and Exit Mode commands.
Alternate Mode Adapter (AMA)	A *USB PD* Device which supports Alternate Modes and acts as a UFP.
Audio Adapter Accessory Mode	The Accessory Mode defined by the presence of Ra/Ra on CC1/CC2, respectively. See Appendix A.
BMC	Biphase Mark Coding used for *USB PD* communication over the CC wire.
Cable Port Partner	The USB Type-C DRP, Source, or Sink connected to the cable plug.
Captive cable	A cable that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Term	Description
CC	Configuration Channel (CC) used in the discovery, configuration and management of connections across a USB Type-C cable.
Charge-Through VPD (CTVPD)	A VCONN-Powered USB Device that has the mechanism to pass power and CC communication from one port to the other without any reregulation.
Configuration Lane	The USB 3.2 Configuration Lane is used to establish and manage dual-lane SuperSpeed USB operation. The Configuration Lane is specifically the SuperSpeed USB TX1/RX1 differential signal set in the cable/plug.
Debug Accessory Mode (DAM)	The Accessory Mode defined by the presence of Rd/Rd or Rp/Rp on CC1/CC2, respectively. See Appendix B.
Debug and Test System (DTS)	The combined hardware and software system that provides a system developer debug visibility and control when connected to a Target System in Debug Accessory Mode.
Default VBUS	VBUS voltage as defined by the *USB 2.0* and *USB 3.2* specifications. Note: where used, 5 V connotes the same meaning.
DFP	Downstream Facing Port, specifically associated with the flow of data in a USB connection. Typically the ports on a host or the ports on a hub to which devices are connected. In its initial state, the DFP sources VBUS and VCONN, and supports data. A charge-only DFP port only sources VBUS.
Direct connect device	A device with either a captive cable or just a USB Type-C plug (e.g., thumb drive).
DRD (Dual-Role-Data)	The acronym used in this specification to refer to a USB port that can operate as either a DFP (Host) or UFP (Device). The role that the port initially takes is determined by the port's power role at attach. A Source port takes on the data role of a DFP and a Sink port takes on the data role of a UFP. The port's data role may be changed dynamically using *USB PD* Data Role Swap.
DRP (Dual-Role-Power)	The acronym used in this specification to refer to a USB port that can operate as either a Source or a Sink. The role that the port offers may be fixed to either a Source or Sink or may alternate between the two port states. Initially when operating as a Source, the port will also take on the data role of a DFP and when operating as a Sink, the port will also take on the data role of a UFP. The port's power role may be changed dynamically using *USB PD* Power Role Swap.
DR_Swap	*USB PD* Data Role Swap.
Dual-lane (x2)	USB 3.2 dual-lane operation is defined as simultaneously signaling on both sets of SuperSpeed USB transmit and receive differential pairs (TX1/RX1 and TX2/RX2 in the cable/plug).
Electronically Marked Cable	A USB Type-C cable that uses *USB PD* to provide the cable's characteristics.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Term	Description
CC	Configuration Channel (CC) used in the discovery, configuration and management of connections across a USB Type-C cable.
Charge-Through VPD (CTVPD)	A VCONN-Powered USB Device that has the mechanism to pass power and CC communication from one port to the other without any reregulation.
Configuration Lane	The USB 3.2 Configuration Lane is used to establish and manage dual-lane SuperSpeed USB operation. The Configuration Lane is specifically the SuperSpeed USB TX1/RX1 differential signal set in the cable/plug.
Debug Accessory Mode (DAM)	The Accessory Mode defined by the presence of Rd/Rd or Rp/Rp on CC1/CC2, respectively. See Appendix B.
Debug and Test System (DTS)	The combined hardware and software system that provides a system developer debug visibility and control when connected to a Target System in Debug Accessory Mode.
Default VBUS	VBUS voltage as defined by the *USB 2.0* and *USB 3.2* specifications. Note: where used, 5 V connotes the same meaning.
DFP	Downstream Facing Port, specifically associated with the flow of data in a USB connection. Typically the ports on a host or the ports on a hub to which devices are connected. In its initial state, the DFP sources VBUS and VCONN, and supports data. A charge-only DFP port only sources VBUS.
Direct connect device	A device with either a captive cable or just a USB Type-C plug (e.g., thumb drive).
DRD (Dual-Role-Data)	The acronym used in this specification to refer to a USB port that can operate as either a DFP (Host) or UFP (Device). The role that the port initially takes is determined by the port's power role at attach. A Source port takes on the data role of a DFP and a Sink port takes on the data role of a UFP. The port's data role may be changed dynamically using *USB PD* Data Role Swap.
DRP (Dual-Role-Power)	The acronym used in this specification to refer to a USB port that can operate as either a Source or a Sink. The role that the port offers may be fixed to either a Source or Sink or may alternate between the two port states. Initially when operating as a Source, the port will also take on the data role of a DFP and when operating as a Sink, the port will also take on the data role of a UFP. The port's power role may be changed dynamically using *USB PD* Power Role Swap.
DR_Swap	*USB PD* Data Role Swap.
Dual-lane (x2)	USB 3.2 dual-lane operation is defined as simultaneously signaling on both sets of SuperSpeed USB transmit and receive differential pairs (TX1/RX1 and TX2/RX2 in the cable/plug).
Electronically Marked Cable	A USB Type-C cable that uses *USB PD* to provide the cable's characteristics.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Term	Description
eMarker	The element in an Electronically Marked Cable that returns information about the cable in response to a *USB PD* Discover Identity command.
Initiator	The port initiating a Vendor Defined Message. It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Initiator will be a host.
Internal Temperature	In reference to an active cable, the temperature measured inside a plug. It is not the skin temperature. There is a relationship between the plug's internal temperature and the skin temperature, but that relationship is design dependent.
Local Plug	The cable plug being referred to.
Optically Isolated Active Cable (OIAC)	A cable with a USB Type-C Plug on each end with one Cable Plug supporting SOP' and the other supporting SOP". This cable is electrically isolated between the two plugs.
Passive cable	A cable that does not incorporate any electronics to condition the data path signals. A passive cable may or may not be electronically marked.
Port Partner	Refers to the port (device or host) a port is attached to.
Power Bank	A device with a battery whose primary function is to charge or otherwise extend the runtime of other USB Type-C devices.
Power Sinking Devices (PSD)	Sink which draws power but has no other USB or Alternate Mode communication function, e.g. a USB-powered light.
Powered cable	A cable with electronics in the plug that requires VCONN indicated by the presence of Ra between the VCONN pin and ground.
PR_Swap	*USB PD* Power Role Swap.
Re-driver	Re-driver refers to an analog component that operates on the signal without re-timing it. This may include equalization, amplification, and transmitter. The re-driver does not include a clock-data recovery (CDR) circuit. Re-drivers are beyond the scope of this document.
Remote Plug	A remote cable plug in the context of OIAC plugs is the plug at the other end of the Optically Isolated Active Cable.
Repeater	Repeater refers to any active component that acts on a signal in order to increase the physical lengths and/or interconnect loss over which the signal can be transmitted successfully. The category of repeaters includes both re-timers and re-drivers.
Responder	The port responding to the Initiator of a Vendor Defined Message (VDM). It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Responder will be a device.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Term	Description
eMarker	The element in an Electronically Marked Cable that returns information about the cable in response to a *USB PD* Discover Identity command.
Initiator	The port initiating a Vendor Defined Message. It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Initiator will be a host.
Internal Temperature	In reference to an active cable, the temperature measured inside a plug. It is not the skin temperature. There is a relationship between the plug's internal temperature and the skin temperature, but that relationship is design dependent.
Local Plug	The cable plug being referred to.
Optically Isolated Active Cable (OIAC)	A cable with a USB Type-C Plug on each end with one Cable Plug supporting SOP' and the other supporting SOP". This cable is electrically isolated between the two plugs.
Passive cable	A cable that does not incorporate any electronics to condition the data path signals. A passive cable may or may not be electronically marked.
Port Partner	Refers to the port (device or host) a port is attached to.
Power Bank	A device with a battery whose primary function is to charge or otherwise extend the runtime of other USB Type-C devices.
Power Sinking Devices (PSD)	Sink which draws power but has no other USB or Alternate Mode communication function, e.g. a USB-powered light.
Powered cable	A cable with electronics in the plug that requires VCONN indicated by the presence of Ra between the VCONN pin and ground.
PR_Swap	*USB PD* Power Role Swap.
Re-driver	Re-driver refers to an analog component that operates on the signal without re-timing it. This may include equalization, amplification, and transmitter. The re-driver does not include a clock-data recovery (CDR) circuit. Re-drivers are beyond the scope of this document.
Remote Plug	A remote cable plug in the context of OIAC plugs is the plug at the other end of the Optically Isolated Active Cable.
Repeater	Repeater refers to any active component that acts on a signal in order to increase the physical lengths and/or interconnect loss over which the signal can be transmitted successfully. The category of repeaters includes both re-timers and re-drivers.
Responder	The port responding to the Initiator of a Vendor Defined Message (VDM). It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Responder will be a device.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Term	Description
Re-timer	Re-timer refers to a component that contains a clock-data recovery (CDR) circuit that "retimes" the signal. The re-timer latches the signal into a synchronous memory element before re-transmitting it. It is used to extend the physical length of the system without accumulating high frequency jitter by creating separate clock domains on either side of the re-timer. Re-timers are defined in *USB 3.2* Appendix E and *USB4*.
SBU	Sideband Use.
Short Active Cable (SAC)	A cable with a USB Type-C Plug on each end at least one of which is a Cable Plug supporting SOP'. Cable length up to 5 meters.
SID	A Standard ID (SID) is a unique 16-bit value assigned by the USB-IF to identify an industry standard.
Single-lane (x1)	USB 3.2 single-lane operation is defined as signaling on only one set of SuperSpeed USB transmit and receive differential pairs (TX1/RX1 in the cable/plug).
Sink	Port asserting Rd on CC and when attached is consuming power from VBUS; most commonly a Device.
Skin Temperature	In reference to an active cable, the temperature of a plug's over-mold.
Source	Port asserting Rp on CC and when attached is providing power over VBUS; most commonly a Host or Hub DFP.
SVID	General reference to either a SID or a VID. Used by *USB PD* Structured VDMs when requesting SIDs and VIDs from a device.
Target System (TS)	The system being debugged in Debug Accessory Mode.
Type-A	A general reference to all versions of USB "A" plugs and receptacles.
Type-B	A general reference to all versions of USB "B" plugs and receptacles.
Type-C Plug	A USB plug conforming to the mechanical and electrical requirements in this specification.
Type-C Port	The USB port associated to a USB Type-C receptacle. This includes the USB signaling, CC logic, multiplexers and other associated logic.
Type-C Receptacle	A USB receptacle conforming to the mechanical and electrical requirements of this specification.
UFP	Upstream Facing Port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks VBUS and supports data.
USB 2.0 Type-C Cable	A USB Type-C to Type-C cable that only supports *USB 2.0* data operation. This cable does not include *USB 3.2* or SBU wires.
USB 2.0 Type-C Plug	A USB Type-C plug specifically designed to implement the *USB 2.0* Type-C cable.
USB Full-Featured Type-C Cable	A USB Type-C to Type-C cable that supports *USB 2.0*, *USB 3.2* and *USB4* data operation. This cable includes SBU wires and is an Electronically Marked Cable.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Term	Description
Re-timer	Re-timer refers to a component that contains a clock-data recovery (CDR) circuit that "retimes" the signal. The re-timer latches the signal into a synchronous memory element before re-transmitting it. It is used to extend the physical length of the system without accumulating high frequency jitter by creating separate clock domains on either side of the re-timer. Re-timers are defined in *USB 3.2* Appendix E and *USB4*.
SBU	Sideband Use.
Short Active Cable (SAC)	A cable with a USB Type-C Plug on each end at least one of which is a Cable Plug supporting SOP'. Cable length up to 5 meters.
SID	A Standard ID (SID) is a unique 16-bit value assigned by the USB-IF to identify an industry standard.
Single-lane (x1)	USB 3.2 single-lane operation is defined as signaling on only one set of SuperSpeed USB transmit and receive differential pairs (TX1/RX1 in the cable/plug).
Sink	Port asserting Rd on CC and when attached is consuming power from VBUS; most commonly a Device.
Skin Temperature	In reference to an active cable, the temperature of a plug's over-mold.
Source	Port asserting Rp on CC and when attached is providing power over VBUS; most commonly a Host or Hub DFP.
SVID	General reference to either a SID or a VID. Used by *USB PD* Structured VDMs when requesting SIDs and VIDs from a device.
Target System (TS)	The system being debugged in Debug Accessory Mode.
Type-A	A general reference to all versions of USB "A" plugs and receptacles.
Type-B	A general reference to all versions of USB "B" plugs and receptacles.
Type-C Plug	A USB plug conforming to the mechanical and electrical requirements in this specification.
Type-C Port	The USB port associated to a USB Type-C receptacle. This includes the USB signaling, CC logic, multiplexers and other associated logic.
Type-C Receptacle	A USB receptacle conforming to the mechanical and electrical requirements of this specification.
UFP	Upstream Facing Port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks VBUS and supports data.
USB 2.0 Type-C Cable	A USB Type-C to Type-C cable that only supports *USB 2.0* data operation. This cable does not include *USB 3.2* or SBU wires.
USB 2.0 Type-C Plug	A USB Type-C plug specifically designed to implement the *USB 2.0* Type-C cable.
USB Full-Featured Type-C Cable	A USB Type-C to Type-C cable that supports *USB 2.0*, *USB 3.2* and *USB4* data operation. This cable includes SBU wires and is an Electronically Marked Cable.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Term	Description
USB Full-Featured Type-C Plug	A USB Type-C plug specifically designed to implement the USB Full-Featured Type-C cable.
USB4 Hub	A USB4 hub product is used for USB port expansion, includes only USB upstream and downstream ports, and does not include any additional capability that exposes other connector types or functions except as defined in Section 5.2.3 (Alternate Modes).
USB4-based Dock	A USB4-based dock product combines a USB4 hub (including at least one exposed USB Type-C downstream port) with additional capabilities that either exposes other connector types and/or includes other user-visible functions, e.g. storage, networking, etc. Examples of functions that are not considered user-visible include firmware update and device authentication.
USB Safe State	The USB Safe State as defined by the *USB PD* specification.
VCONN-Powered Accessory (VPA)	An accessory that is powered from VCONN to operate in an Alternate Mode. VPAs cannot implement the charge-through mechanism described for VPDs, and instead must intermediate by negotiating USB Power Delivery with both the connected host and source in order to enable similar functionality.
VCONN-Powered USB Device (VPD)	A USB direct-connect or captive-cable device that can be powered solely from either VCONN or VBUS. VPDs may optionally support the VPD charge-through capability.
VCONN_Swap	*USB PD* VCONN Swap.
VDM	Vendor Defined Message as defined by the *USB PD* specification.
VID	A Vendor ID (VID) is a unique 16-bit value assigned by the USB-IF to identify a vendor.
vSafe0V	VBUS "0 volts" as defined by the *USB PD* specification.
vSafe5V	VBUS "5 volts" as defined by the *USB PD* specification.
x1	See Single-lane.
x2	See Dual-lane.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Term	Description
USB Full-Featured Type-C Plug	A USB Type-C plug specifically designed to implement the USB Full-Featured Type-C cable.
USB4 Hub	A USB4 hub product is used for USB port expansion, includes only USB upstream and downstream ports, and does not include any additional capability that exposes other connector types or functions except as defined in Section 5.2.3 (Alternate Modes).
USB4-based Dock	A USB4-based dock product combines a USB4 hub (including at least one exposed USB Type-C downstream port) with additional capabilities that either exposes other connector types and/or includes other user-visible functions, e.g. storage, networking, etc. Examples of functions that are not considered user-visible include firmware update and device authentication.
USB Safe State	The USB Safe State as defined by the *USB PD* specification.
VCONN-Powered Accessory (VPA)	An accessory that is powered from VCONN to operate in an Alternate Mode. VPAs cannot implement the charge-through mechanism described for VPDs, and instead must intermediate by negotiating USB Power Delivery with both the connected host and source in order to enable similar functionality.
VCONN-Powered USB Device (VPD)	A USB direct-connect or captive-cable device that can be powered solely from either VCONN or VBUS. VPDs may optionally support the VPD charge-through capability.
VCONN_Swap	*USB PD* VCONN Swap.
VDM	Vendor Defined Message as defined by the *USB PD* specification.
VID	A Vendor ID (VID) is a unique 16-bit value assigned by the USB-IF to identify a vendor.
vSafe0V	VBUS "0 volts" as defined by the *USB PD* specification.
vSafe5V	VBUS "5 volts" as defined by the *USB PD* specification.
x1	See Single-lane.
x2	See Dual-lane.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

2 Overview

2.1 Introduction

The USB Type-C® receptacle, plug and cable provide a smaller, thinner and more robust alternative to legacy USB interconnect (Standard and Micro USB cables and connectors). This solution targets use in very thin platforms, ranging from ultra-thin notebook PCs down to smart phones where existing Standard-A and Micro-AB receptacles are deemed too large, difficult to use, or inadequately robust. Some key specific enhancements include:

- The USB Type-C receptacle may be used in very thin platforms as its total system height for the mounted receptacle is under 3 mm
- The USB Type-C plug enhances ease of use by being plug-able in either upside-up or upside-down directions
- The USB Type-C cable enhances ease of use by being plug-able in either direction between host and devices

While the USB Type-C interconnect no longer physically differentiates plugs on a cable by being an A-type or B-type, the USB interface still maintains such a host-to-device logical relationship. Determination of this host-to-device relationship is accomplished through a Configuration Channel (CC) that is connected through the cable. In addition, the Configuration Channel is used to set up and manage power and Alternate/Accessory Modes.

Using the Configuration Channel, the USB Type-C interconnect defines a simplified 5 volt VBUS-based power delivery and charging solution that supplements what is already defined in the *USB 3.2 Specification*. More advanced power delivery and battery charging features over the USB Type-C interconnect are based on the *USB Power Delivery Specification*. As a product implementation improvement, the USB Type-C interconnect shifts the *USB PD* communication protocol from being communicated over VBUS to being delivered across the USB Type-C Configuration Channel.

The USB Type-C receptacle, plug and cable designs are intended to support future USB functional extensions. As such, consideration was given to frequency scaling performance, pin-out arrangement and the configuration mechanisms when developing this solution. The definition of future USB functional extensions is not in the scope of this specification but rather will be provided in future releases of the base USB Specification, i.e., beyond the existing *USB4™ Specification*.

Figure 2-1 illustrates the comprehensive functional signal plan for the USB Full-Featured Type-C receptacle, not all signals shown are required in all platforms or devices. As shown, the receptacle signal list functionally delivers both *USB 2.0* (D+ and D−) and either *USB 3.2* or *USB4* (TX and RX pairs) data buses, USB power (VBUS) and ground (GND), Configuration Channel signals (CC1 and CC2), and two Sideband Use (SBU) signal pins. Multiple sets of USB data bus signal locations in this layout facilitate being able to functionally map the USB signals independent of plug orientation in the receptacle. For reference, the signal pins are labeled. For the *USB 2.0* Type-C receptacle, neither the *USB 3.2* nor *USB4* signals are implemented.

Figure 2-1 USB Type-C Receptacle Interface (Front View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

2 概述

2.1 简介

USB Type-C® 插座、插头和电缆为传统 USB 互连（标准和微型 USB 电缆和连接器）提供了更小、更薄、更坚固的替代方案。该解决方案适用于非常薄的平台，从超薄笔记本电脑到智能手机，现有的标准 A 和微型 AB 插座被认为太大、难以使用或不够坚固。一些关键的具体增强功能包括：

- USB Type-C 插座可用于非常薄的平台，因为其安装插座的总系统高度不到 3 毫米。
- USB Type-C 插头可上下插入，提高了易用性。

颠倒方向
- USB Type-C 电缆可在主机和设备之间任意方向插入，提高了易用性

虽然 USB Type-C 互连不再通过 A 型或 B 型来物理区分电缆上的插头，但 USB 接口仍然保持这种主机到设备的逻辑关系。这种主机到设备关系的确定是通过电缆连接的配置通道 (CC) 来完成的。此外，配置通道用于设置和管理电源和备用/附件模式

。

使用配置通道，USB Type-C 互连定义了一种简化的基于 5 伏 VBUS 的供电和充电解决方案，补充了 *USB 3.2 Specification* 中已定义的内容。USB Type-C 互连上更高级的供电和电池充电功能基于 *USB Power Delivery Specification*。作为产品实施的改进，USB Type-C 互连将 *USB PD* 通信协议从通过 VBUS 传输转变为通过 USB Type-C 配置通道传输。

USB Type-C 插座、插头和电缆设计旨在支持未来的 USB 功能扩展。因此，在开发此解决方案时，我们考虑了频率缩放性能、引脚排列和配置机制。未来 USB 功能扩展的定义不在本规范的范围内，而是将在基础 USB 规范的未来版本中提供，即现有 *USB4™ Specification* 之外的版本。

图 2-1 显示了 USB 全功能 Type-C 插座的综合功能信号规划，并非所有平台或设备都需要所示的所有信号。如图所示，插座信号列表在功能上提供 *USB 2.0*（D+ 和 D–）和 *USB 3.2* 或 *USB4*（TX 和 RX 对）数据总线、USB 电源 (VBUS) 和接地 (GND)、配置通道信号 (CC1 和 CC2) 以及两个边带使用 (SBU) 信号引脚。此布局中的多组 USB 数据总线信号位置有助于能够独立于插座中的插头方向在功能上映射 USB 信号。作为参考，信号引脚已标记。对于 *USB 2.0* Type-C 插座，未实现 *USB 3.2* 和 *USB4* 信号。

弗图 2-1 USB Type-C 插座接口（前 看法）

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1–	VBUS	CC1	D+	D–	SBU1	VBUS	RX2–	RX2+	GND
GND	RX1+	RX1–	VBUS	SBU2	D–	D+	CC2	VBUS	TX2–	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 2-2 illustrates the comprehensive functional signal plan for the USB Type-C plug. Only one CC pin is connected through the cable to establish signal orientation and the other CC pin is repurposed as VCONN for powering electronics in the USB Type-C plug. Also, only one set of *USB 2.0* D+/D− wires are implemented in a USB Type-C cable. For USB Type-C cables that only intend to support *USB 2.0* functionality, the TX/RX and SBU signals are not implemented. For the USB Type-C Power-Only plug (intended only for USB Type-C Sink applications), only nine contacts are implemented to support CC, VBUS, and GND.

Figure 2-2 USB Full-Featured Type-C Plug Interface (Front View)

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

2.2 USB Type-C Receptacles, Plugs and Cables

Cables and connectors, including USB Type-C to USB legacy cables and adapters, are explicitly defined within this specification. These are the only connectors and cables that are authorized by the licensing terms of this specification. All licensed cables and connectors are required to comply with the compliance and certification requirements that are developed and maintained by the USB-IF.

The following USB Type-C receptacles and plugs are defined.

- USB Full-Featured Type-C receptacle for *USB 2.0*, *USB 3.2*, *USB4* and full-featured platforms and devices
- *USB 2.0* Type-C receptacle for *USB 2.0* platforms and devices
- USB Full-Featured Type-C plug
- *USB 2.0* Type-C plug
- USB Type-C Power-Only plug

The following USB Type-C cables are defined.

- USB Full-Featured Type-C cable with a USB Full-Featured Type-C plug at both ends for *USB 3.2*, *USB4* and full-featured applications
- *USB 2.0* Type-C cable with a *USB 2.0* Type-C plug at both ends for *USB 2.0* applications
- Captive cable with either a USB Full-Featured Type-C plug or *USB 2.0* Type-C plug at one end
- Active cables as defined in Chapter 6

All of the defined USB Type-C receptacles, plugs and cables (except OIAC) support USB charging applications, including support for the optional USB Type-C-specific implementation of the *USB Power Delivery Specification* (See Section 4.6.2.4).

All USB Full-Featured Type-C cables are electronically marked. *USB 2.0* Type-C cables may be electronically marked. See Section 4.9 for the requirements of Electronically Marked Cables.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 2-2 说明了 USB Type-C 插头的综合功能信号规划。只有一个 CC 引脚通过电缆连接以建立信号方向，另一个 CC 引脚被重新用作 VCONN，为 USB Type-C 插头中的电子设备供电。此外，USB Type-C 电缆中只实现了一组 *USB 2.0* D+/D− 线。对于仅打算支持 *USB 2.0* 功能的 USB Type-C 电缆，未实现 TX/RX 和 SBU 信号。对于 USB Type-C 仅供电插头（仅适用于 USB Type-C 接收器应用），只实现了九个触点来支持 CC、VBUS 和 GND。

图 2-2 USB 全功能 Type-C 插头接口（正面图）

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

2.2 USB Type-C 插座、插头和电缆

本规范明确定义了电缆和连接器，包括 USB Type-C 转 USB 传统电缆和适配器。这些是本规范许可条款授权的唯一连接器和电缆。所有获得许可的电缆和连接器都必须符合 USB-IF 制定和维护的合规性和认证要求。

定义了以下 USB Type-C 插座和插头。

- USB 全功能 Type-C 插座，适用于 *USB 2.0*、*USB 3.2*、*USB4* 及全功能平台与设备 • *USB 2.0* Type-C 插座，适用于 *USB 2.0* 平台与设备 • USB 全功能 Type-C 插头 • *USB 2.0* Type-C 插头 • USB Type-C 仅供电插头

定义了以下 USB Type-C 电缆。

- USB 全功能 Type-C 线缆，两端均带有 USB 全功能 Type-C 插头，适用于 *USB 3.2*、*USB4* 和全功能应用 • *USB 2.0* Type-C 线缆，两端均带有 *USB 2.0* Type-C 插头，适用于 *USB 2.0* 应用 • 固定线缆，一端带有 USB 全功能 Type-C 插头或 *USB 2.0* Type-C 插头 • 有源线缆，定义见第 6 章

所有定义的 USB Type-C 插座、插头和电缆（OIAC 除外）均支持 USB 充电应用，包括支持 *USB Power Delivery Specification* 的可选 USB Type-C 特定实现（参见第 4.6.2.4 节）。

所有 USB 全功能 Type-C 线缆均采用电子标记。*USB 2.0* Type-C 线缆可以采用电子标记。有关电子标记线缆的要求，请参阅第 4.9 节。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The following USB Type-C to USB legacy cables and adapters are defined.

- USB 3.2 Type-C to Legacy Host cable with a USB Full-Featured Type-C plug at one end and a USB 3.1 Standard-A plug at the other end – *this cable supports use of a USB Type-C-based device with a legacy USB host*
- USB 2.0 Type-C to Legacy Host cable with a USB 2.0 Type-C plug at one end and a USB 2.0 Standard-A plug at the other end – *this cable supports use of a USB Type-C-based device with a legacy USB 2.0 host (primarily for mobile charging and sync applications)*
- USB 3.2 Type-C to Legacy Device cable with a USB Full-Featured Type-C plug at one end and a USB 3.1 Standard-B plug at the other end – *this cable supports use of legacy USB 3.1 hubs and devices with a USB Type-C-based host*
- USB 2.0 Type-C to Legacy Device cable with a USB 2.0 Type-C plug at one end and a USB 2.0 Standard-B plug at the other end – *this cable supports use of legacy USB 2.0 hubs and devices with a USB Type-C-based host*
- USB 2.0 Type-C to Legacy Mini Device cable with a USB 2.0 Type-C plug at one end and a USB 2.0 Mini-B plug at the other end – *this cable supports use of legacy devices with a USB 2.0 Type-C-based host*
- USB 3.2 Type-C to Legacy Micro Device cable with a USB Full-Featured Type-C plug at one end and a USB 3.1 Micro-B plug at the other end – *this cable supports use of legacy USB 3.1 hubs and devices with a USB Type-C-based host*
- USB 2.0 Type-C to Legacy Micro Device cable with a USB 2.0 Type-C plug at one end and a USB 2.0 Micro-B plug at the other end – *this cable supports use of legacy USB 2.0 hubs and devices with a USB Type-C-based host*
- USB 3.2 Type-C to Legacy Standard-A adapter with a USB Full-Featured Type-C plug at one end and a USB 3.1 Standard-A receptacle at the other end – *this adapter supports use of a legacy USB "thumb drive" style device or a legacy USB ThinCard device with a USB 3.2 Type-C-based host*
- USB 2.0 Type-C to Legacy Micro-B adapter with a USB 2.0 Type-C plug at one end and a USB 2.0 Micro-B receptacle at the other end – *this adapter supports charging a USB Type-C-based mobile device using a legacy USB Micro-B-based chargers, either captive cable-based or used in conjunction with a legacy USB 2.0 Standard-A to Micro-B cable*

USB Type-C receptacle to USB legacy adapters are explicitly not defined or allowed. Such adapters would allow many invalid and potentially unsafe cable connections to be constructed by users.

2.3 Configuration Process

The USB Type-C receptacle, plug and cable solution incorporates a configuration process to detect a downstream facing port to upstream facing port (Source-to-Sink) connection for VBUS management and host-to-device connected relationship determination.

The USB Type-C port configuration process is used for the following:

- Source-to-Sink attach/detach detection
- Plug orientation/cable twist detection
- Initial power (Source-to-Sink) detection and establishing the data (Host-to-Device) relationship
- Detect if cable requires VCONN
- USB Type-C VBUS current detection and usage

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

定义了以下 USB Type-C 至 USB 传统电缆和适配器。

• *USB 3.2* Type-C 转传统主机线缆，一端带有 USB 全功能 Type-C 插头，另一端带有 *USB 3.1* 标准 A 插头 *– this cable supports use of a USB Type-C-based device with a legacy USB host* • *USB 2.0* Type-C 转传统主机线缆，一端带有 *USB 2.0* Type-C 插头，另一端带有 *USB 2.0* 标准 A 插头 *– this cable supports use of a USB Type-C-based device with a legacy USB 2.0 host (primarily for mobile charging and sync applications)* • *USB 3.2* Type-C 转传统设备线缆，一端带有 USB 全功能 Type-C 插头，另一端带有 *USB 3.1* 标准 B 插头 *– this cable supports use of legacy USB 3.1 hubs and devices with a USB Type-C-based host* • *USB 2.0* Type-C 转传统设备线缆，一端带有 *USB 2.0* Type-C 插头，另一端带有 *USB 2.0* 标准 B 插头 *– this cable supports use of legacy USB 2.0 hubs and devices with a USB Type-C-based host* • *USB 2.0* Type-C 转传统迷你设备线缆，一端带有 *USB 2.0* Type-C 插头，另一端带有 *USB 2.0* Mini-B 插头 *– this cable supports use of legacy devices with a USB 2.0 Type-C-based host* • *USB 3.2* Type-C 转传统微型设备线缆，一端带有 USB 全功能 Type-C 插头，另一端带有 *USB 3.1* Micro-B 插头 *– this cable supports use of legacy USB 3.1 hubs and devices with a USB Type-C-based host* • *USB 2.0* Type-C 转传统微型设备线缆，一端带有 *USB 2.0* Type-C 插头，另一端带有 *USB 2.0* Micro-B 插头 *– this cable supports use of legacy USB 2.0 hubs and devices with a USB Type-C-based host* • *USB 3.2* Type-C 转传统标准 A 适配器，一端带有 USB 全功能 Type-C 插头，另一端带有 *USB 3.1* 标准 A 插座 *– this adapter supports use of a legacy USB "thumb drive" style device or a legacy USB ThinCard device with a USB 3.2 Type-C-based host* • *USB 2.0* Type-C 转传统 Micro-B 适配器，一端带有 *USB 2.0* Type-C 插头，另一端带有 *USB 2.0* Micro-B 插座 *– this adapter supports charging a USB Type-C-based mobile device using a legacy USB Micro-B-based chargers, either captive cable-based or used in conjunction with a legacy USB 2.0 Standard-A to Micro-B cable*

USB Type-C 插座与 USB 传统适配器之间的连接明确未定义或不允许。此类适配器将允许用户构建许多无效且可能不安全的电缆连接。

2.3 配置流程

USB Type-C 插座、插头和电缆解决方案包含一个配置过程，用于检测下游端口到上游端口（源到接收器）的连接，以进行 VBUS 管理和主机到设备的连接关系确定。

USB Type-C 端口配置流程用于：

• 源到接收器连接/断开检测 • 插头方向/电缆扭曲检测 • 初始电源（源到接收器）检测并建立数据（主机到设备）关系 • 检测电缆是否需要 VCONN • USB Type-C VBUS 电流检测和使用情况

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- *USB PD* communication
- Discovery and configuration of functional extensions

Two pins on the USB Type-C receptacle, CC1 and CC2, are used for this purpose. Within a standard USB Type-C cable, only a single CC pin position within each plug of the cable is connected through the cable.

2.3.1 Source-to-Sink Attach/Detach Detection

Initially, Source-to-Sink attach is detected by a host or hub port (Source) when one of the CC pins at its USB Type-C receptacle senses a specified resistance to GND. Subsequently, Source-to-Sink detach is detected when the CC pin that was terminated at its USB Type-C receptacle is no longer terminated to GND.

Power is not applied to the USB Type-C host or hub receptacle (V_{BUS} or V_{CONN}) until the Source detects the presence of an attached device (Sink) port. When a Source-to-Sink attach is detected, the Source is expected to enable power to the receptacle and proceed to normal USB operation with the attached device. When a Source-to-Sink detach is detected, the port sourcing V_{BUS} removes power.

2.3.2 Plug Orientation/Cable Twist Detection

The USB Type-C plug can be inserted into a receptacle in either one of two orientations, therefore the CC pins enable a method for detecting plug orientation in order to determine the lane ordering of the SuperSpeed USB data signal pairs functionally connected through the cable and identify the Configuration Lane for dual-lane operation when supported. This allows for signal routing, if needed, within a host or device to be established for a successful connection.

2.3.3 Initial Power (Source-to-Sink) Detection and Establishing the Data (Host-to-Device) Relationship

Unlike existing USB Type-A and USB Type-B receptacles and plugs, the mechanical characteristics of the USB Type-C receptacle and plug do not inherently establish the relationship of USB host and device ports. The CC pins on the receptacle also serve to establish an initial power (Source-to-Sink) and data (Host-to-Device) relationships prior to the normal USB enumeration process.

For the purpose of defining how the CC pins are used to establish the initial power relationship, the following port power behavior modes are defined.

1. Source-only – for this mode, the port exclusively behaves as a Source
2. Sink-only – for this mode, the port exclusively behaves as a Sink
3. Dual-Role-Power (DRP) – for this mode, the port can behave either as a Source or Sink

Additionally, when a port supports USB data operation, a port's data behavior modes are defined.

1. DFP-only – for this mode, the port exclusively behaves as a DFP
2. UFP-only – for this mode, the port exclusively behaves as a UFP
3. Dual-Role-Data (DRD) – for this mode, the port can behave either as a DFP or UFP

The DFP-only and UFP-only ports behaviorally map to traditional USB host ports and USB device ports, respectively but may not necessarily do USB data communication. When a host-only port is attached to a device-only port, the behavior from the user's perspective

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- *USB PD* 通信
- 功能扩展的发现和配置

USB Type-C 插座上的两个引脚 CC1 和 CC2 用于此目的。在标准 USB Type-C 电缆中，电缆的每个插头内只有一个 CC 引脚位置通过电缆连接。

2.3.1 源到接收器的连接/分离检测

最初，当 USB Type-C 插座上的 CC 引脚之一感应到指定 GND 电阻时，主机或集线器端口 (Source) 会检测到源到接收器的连接。随后，当 USB Type-C 插座上的 CC 引脚不再端接到 GND 时，会检测到源到接收器的断开。

在源端检测到连接的设备（接收器）端口存在之前，不会向 USB Type-C 主机或集线器插座（VBUS 或 VCONN）供电。当检测到源端到接收器的连接时，源端应为插座供电，并继续与连接的设备进行正常的 USB 操作。当检测到源端到接收器的断开时，端口供电 VBUS 将断开电源。

2.3.2 插头方向/电缆扭曲检测

USB Type-C 插头可以以两种方向插入插座，因此 CC 引脚可以实现一种检测插头方向的方法，以确定通过电缆功能连接的超高速 USB 数据信号对的通道顺序，并在支持双通道操作时识别配置通道。如果需要，这可以在主机或设备内建立信号路由，以成功连接。

2.3.3 初始电源（源到接收器）检测和建立数据（主机到设备）关系

与现有的 USB Type-A 和 USB Type-B 插座和插头不同，USB Type-C 插座和插头的机械特性本身并不建立 USB 主机和设备端口的关系。插座上的 CC 引脚还用于在正常 USB 枚举过程之前建立初始电源（源到接收器）和数据（主机到设备）关系。

为了定义如何使用 CC 引脚建立初始电源关系，定义了以下端口电源行为模式。

1. 仅源 — 在此模式下，端口仅充当源 2. 仅接收器 — 在此模式下，端口仅充当接收器 3. 双角色电源 (DRP) — 在此模式下，端口既可以充当源，也可以充当接收器

此外，当端口支持 USB 数据操作时，会定义端口的数据行为模式。

1. 仅 DFP – 在此模式下，端口仅充当 DFP 2. 仅 UFP – 在此模式下，端口仅充当 UFP 3. 双角色数据 (DRD) – 在此模式下，端口可以充当 DFP 或 UFP

DFP 专用端口和 UFP 专用端口在行为上分别映射到传统 USB 主机端口和 USB 设备端口，但不一定进行 USB 数据通信。当主机专用端口连接到设备专用端口时，从用户的角度来看，行为

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

follows the traditional USB host-to-device port model. However, the USB Type-C connector solution does not physically prevent host-to-host or device-to-device connections. In this case, the resulting host-to-host or device-to-device connection results in a safe but non-functional situation.

Once initially established, the Source supplies VBUS and behaves as a DFP, and the Sink consumes VBUS and behaves as a UFP. *USB PD*, when supported by both ports, may then be used to independently swap both the power and data roles of the ports.

A port that supports dual-role operation by being able to shift to the appropriate connected mode when attached to either a Source-only or Sink-only port is a DRP. In the special case of a DRP being attached to another DRP, an initialization protocol across the CC pins is used to establish the initial host-to-device relationship. Given no role-swapping intervention, the determination of which is DFP or UFP is random from the user's perspective.

Two independent set of mechanisms are defined to allow a USB Type-C DRP to functionally swap power and data roles. When *USB PD* is supported, power and data role swapping is performed as a subsequent step following the initial connection process. For non-PD implementations, power/data role swapping can optionally be dealt with as part of the initial connection process. To improve the user's experience when connecting devices that are of categorically different types, products may be implemented to strongly prefer being a DFP or a UFP, such that the DFP/UFP determination becomes predictable when connecting two DRPs of differing categories. See Section 4.5.1.4 for more on available swapping mechanisms.

As an alternative to role swapping, a USB Type-C DRP may provide useful functionality by when operating as a host, exposing a CDC/network (preferably TCP/IP) stack or when operating as a device, exposing a CDC/network interface.

USB hubs have two types of ports, a UFP that is connected to a DFP (host or another hub) that initially functions as a Sink, and one or more DFPs for connecting other devices that initially function as Sources.

2.3.4 USB Type-C VBUS Current Detection and Usage

With the USB Type-C connector solution, a Source (host or downstream hub port) may implement higher source current over VBUS to enable faster charging of mobile devices or higher-power devices. All USB host and hub ports advertise via the CC pins the level of current that is presently available. The USB device port is required to manage its load to stay within the current level offered by the host or hub, including dynamically scaling back the load if the host or hub port changes its advertisement to a lower level as indicated over the CC pins.

Three current level advertisements at 5V VBUS are defined by USB Type-C Current:

- Default is the as-configured for high-power operation current value as defined by a USB Specification (500 mA for USB 2.0 ports; 900 mA or 1,500 mA for USB 3.2 ports operating in single-lane or dual-lane, respectively)
- USB Type-C Current @ 1.5 A
- USB Type-C Current @ 3.0 A

There is a clear functional distinction between advertising Default versus the USB Type-C Current at either 1.5 A or 3.0 A.

- Default is intended for host operation in providing bus power to a connected device where the host manages the device's current consumption for the low-power, high-power and suspend states as defined in the USB base specifications.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

遵循传统的 USB 主机到设备端口模型。但是，USB Type-C 连接器解决方案不会在物理上阻止主机到主机或设备到设备的连接。在这种情况下，由此产生的主机到主机或设备到设备的连接会导致安全但无法正常工作的情况。

一旦最初建立，源端提供 VBUS 并充当 DFP，而接收器消耗 VBUS 并充当 UFP。当两个端口都支持时，*USB PD* 可用于独立交换端口的电源和数据角色。

DRP 端口支持双重角色操作，即在连接到仅源端口或仅接收器端口时能够切换到适当的连接模式。在 DRP 连接到另一个 DRP 的特殊情况下，使用跨 CC 引脚的初始化协议来建立初始主机到设备关系。如果没有角色交换干预，

从用户的角度来看，确定哪个是 DFP 还是 UFP 是随机的。

定义了两组独立的机制，允许 USB Type-C DRP 在功能上交换电源和数据角色。当支持 *USB PD* 时，电源和数据角色交换将作为初始连接过程之后的后续步骤执行。对于非 PD 实现，可以选择将电源/数据角色交换作为初始连接过程的一部分来处理。为了改善用户在连接不同类型设备时的体验，产品可以实现为强烈倾向于成为

DFP 或 UFP，这样当连接两个不同类别的 DRP 时，DFP/UFP 的确定就变得可预测。有关可用交换机制的更多信息，请参阅第 4.5.1.4 节。

作为角色交换的替代方案，USB Type-C DRP 可以在作为主机运行时提供有用的功能，从而公开 CDC/网络（最好是 TCP/IP）堆栈，或者在作为设备运行时提供有用的功能，从而公开 CDC/网络接口。

USB 集线器有两种类型的端口：一个 UFP，它连接到最初用作接收器 (Sink) 的 DFP（主机或另一个集线器）；以及一个或多个 DFP，用于连接最初用作源 (Source) 的其他设备。

2.3.4 USB Type-C VBUS 电流检测和使用

使用 USB Type-C 连接器解决方案，源（主机或下游集线器端口）可通过 VBUS 实现更高的源电流，从而更快地为移动设备或高功率设备充电。所有 USB 主机和集线器端口都通过 CC 引脚通告当前可用的电流水平。USB 设备端口需要管理其负载以保持在主机或集线器提供的电流水平内，包括在主机或集线器端口将其通告更改为较低水平（如 CC 引脚所示）时动态缩减负载。

USB Type-C 电流定义了 5V VBUS 下的三种电流水平广告：

- 默认值为 USB 规范定义的高功率工作电流值（USB 2.0 端口为 500 mA；USB 3.2 端口在单通道或双通道中分别为 900 mA 或 1,500 mA）• USB Type-C 电流 @ 1.5 A • USB Type-C 电流 @ 3.0 A

广告默认电流与 USB Type -C 电流（1.5 A 或 3.0 A）之间存在明显的功能区别。

- 默认值用于主机操作，为连接的设备提供总线电源，其中主机管理设备在低功耗、高功率和挂起状态下的电流消耗，如 USB 基本规范中所定义。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- USB Type-C Current at either 1.5 A or 3.0 A is primarily intended for charging applications. The Sink can vary its current draw up to the advertised limit. Offering USB Type-C Current at either 1.5 A or 3.0 A is allowed for a host providing bus power to a device. The host needs to assume that the device will continuously draw up to the offered limit.

The higher USB Type-C Current levels that can be advertised allows hosts and devices that do not implement *USB PD* to take advantage of higher charging current.

2.3.5 USB PD Communication

USB Power Delivery is a feature on products (hosts, hubs and devices). *USB PD* communications is used to:

- Establish power contracts that allow voltage and current beyond existing USB data bus specifications.
- Change the port sourcing VBUS.
- Change the port sourcing VCONN.
- Swap DFP and UFP roles.
- Communicate with cables.

The *USB PD* Bi-phase Mark Coded (BMC) communications are carried on the CC wire of the USB Type-C cable.

2.3.6 Functional Extensions

Functional extensions (see Chapter E) are enabled via a communications channel across CC using methods defined by the *USB Power Delivery Specification*.

2.4 VBUS

VBUS provides a path to deliver power between a host and a device, and between a USB power charger and a host/device. A simplified high-current supply capability is defined for hosts and chargers that optionally support current levels beyond the *USB 2.0*, *USB 3.2*, and *USB4* specifications. The *USB Power Delivery Specification* is supported.

Table 2-1 summarizes the power supply options available from the perspective of a device with the USB Type-C connector. Not all options will be available to the device from all host or hub ports – only the first two listed options are mandated by the base USB specifications and form the basis of USB Type-C Current at the Default USB Power level.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• 1.5 A 或 3.0 A 的 USB Type-C 电流主要用于充电应用。接收器可以改变其电流消耗，直至达到广告限制。对于为设备提供总线电源的主机，允许提供 1.5 A 或 3.0 A 的 USB Type-C 电流。主机需要假设设备将持续消耗到提供的限制。

可以宣传的更高的 USB Type-C 电流水平允许未实现 *USB PD* 的主机和设备利用更高的充电电流。

2.3.5 USB PD 通信

USB Power Delivery 是产品（主机、集线器和设备）的一项功能。*USB PD* 通信用于：

• 建立允许电压和电流超出现有 USB 数据总线规格的电源合同。• 更改端口源 VBUS。• 更改端口源 VCONN。• 交换 DFP 和 UFP 角色。• 与电缆通信。

*USB PD*双相标记编码 (BMC) 通信在 USB Type-C 电缆的 CC 线上进行。

2.3.6 功能扩展

功能扩展（参见第 E 章）是通过 CC 上的通信通道使用 *USB Power Delivery Specification* 定义的方法启用的。

2.4 总线电压

VBUS 为主机和设备之间以及 USB 电源充电器和主机/设备之间提供供电路径。针对主机和充电器定义了简化的高电流供电能力，可选择支持超出 *USB 2.0*、*USB 3.2* 和 *USB4* 规格的电流水平。支持 *USB Power Delivery Specification*。

表 2-1 总结了从配备 USB Type-C 连接器的设备的角度来看可用的电源选项。并非所有选项都适用于所有主机或集线器端口的设备 - 只有前两个列出的选项是基本 USB 规范所要求的，并构成了默认 USB 功率级别的 USB Type-C 电流的基础。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 2-1 Summary of power supply options

Mode of Operation	Voltage	Current	Notes
USB 2.0	5 V	See *USB 2.0*	
USB 3.2	5 V	See *USB 3.2*	
USB4	5 V	1.5 A	See Section 5.3.
USB BC 1.2	5 V	1.5 A[1]	Legacy charging
USB Type-C Current @ 1.5 A	5 V	1.5 A	Supports higher power devices
USB Type-C Current @ 3.0 A	5 V	3 A	Supports higher power devices
USB PD	Configurable up to 20 V	Configurable up to 5 A	Directional control and power level management

Notes:

1. Whereas *USB BC 1.2* specification permits a power provider to be designed to support a level of power between 0.5 A and 1.5 A, the USB Type-C specification requires that a Source port that supports *USB BC 1.2* be at a minimum capable of supplying 1.5 A and advertise USB Type-C Current @ 1.5 A in addition to supporting the *USB BC 1.2* power provider termination.

The USB Type-C receptacle is specified for current capability of 5 A whereas standard USB Type-C cable assemblies are rated for 3 A. The higher rating of the receptacle enables systems to deliver more power over directly attached docking solutions or using appropriately designed chargers with captive cables when implementing *USB PD*. Also, USB Type-C cable assemblies designed for *USB PD* and appropriately identified via electronic marking are allowed to support up to 5 A.

2.5 VCONN

Once the connection between host and device is established, the CC pin (CC1 or CC2) in the receptacle that is not connected via the CC wire through the standard cable is repurposed to source VCONN to power circuits in the plug needed to implement Electronically Marked Cables (see Section 4.9), VCONN-Powered Accessories and VCONN-Powered USB Devices. Initially, the source supplies VCONN and the source of VCONN may be swapped using *USB PD* VCONN_Swap.

Electronically marked cables may use VBUS instead of VCONN as VBUS is available across the cable. VCONN functionally differs from VBUS in that it is isolated from the other end of the cable. VCONN is independent of VBUS and, unlike VBUS which can use *USB PD* to support higher voltages, VCONN voltage stays within the range of 3.0 to 5.5 V (vVCONNValid).

2.6 Hubs

USB hubs implemented with USB Type-C receptacles are required to clearly identify the upstream facing port. This requirement is needed because a user can no longer know which port on a hub is the upstream facing port and which ports are the downstream facing ports by the type of receptacles that are exposed, i.e., USB Type-B is the upstream facing port and USB Type-A is a downstream facing port.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 2-1 电源选项摘要

Mode of Operation	Voltage	Current	Notes
USB 2.0	5 V	See *USB 2.0*	
USB 3.2	5 V	See *USB 3.2*	
USB4	5 V	1.5 A	See Section 5.3.
USB BC 1.2	5 V	1.5 A[1]	Legacy charging
USB Type-C Current @ 1.5 A	5 V	1.5 A	Supports higher power devices
USB Type-C Current @ 3.0 A	5 V	3 A	Supports higher power devices
USB PD	Configurable up to 20 V	Configurable up to 5 A	Directional control and power level management

注：1. 虽然 *USB BC 1.2* 规范允许电源设计为支持 0.5 A 至 1.5 A 之间的功率水平，但 USB Type-C 规范要求支持 *USB BC 1.2* 的源端口至少能够提供 1.5 A 的电流，并且除了宣传 USB Type-C 电流 @ 1.5 A 之外

支持*USB BC 1.2*电源供应商终止。

USB Type-C 插座的额定电流为 5 A，而标准 USB Type-C 电缆组件的额定电流为 3 A。插座的额定电流越高，系统就越能通过直接连接的对接解决方案或使用适当设计的带固定电缆的充电器（在实施 *USB PD* 时）提供更多电力。此外，为 *USB PD* 设计并通过电子标记适当标识的 USB Type-C 电缆组件最多可支持 5 A 的电流。

2.5 VCONN

一旦主机和设备之间的连接建立，插座中未通过标准电缆通过 CC 线连接的 CC 引脚（CC1 或 CC2）将重新用于为插头中的电源电路提供 VCONN，以实现电子标记电缆（参见第 4.9 节）、VCONN 供电配件和 VCONN 供电 USB 设备。最初，电源为 VCONN 供电，可~~以使用 *USB PD* VCONN~~_Swap ~~交换~~ VCONN 的电源。

电子标记电缆可能使用 VBUS 而不是 VCONN，因为 VBUS 可在整个电缆上使用。VCONN 在功能上与 VBUS 不同，因为它与电缆的另一端隔离。VCONN 独立于 VBUS，并且与可以使用 *USB PD* 支持更高电压的 VBUS 不同，VCONN 电压保持在 3.0 至 5.5 V 的~~范围内~~（vVCONNValid）。

2.6 集线器

采用 USB Type-C 插座实现的 USB 集线器需要明确标识面向上游的端口。之所以需要此要求，是因为用户无法再根据暴露的插座类型来判断集线器上的哪个端口是面向上游的端口，哪些端口是面向下游的端口（即 USB Type-B 是面向上游的端口，而 USB Type-A 是面向下游的端口）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3 Mechanical

3.1 Overview

This chapter defines the USB Type-C® connectors and wired cable assemblies. Cables which include active elements in the data path are defined in Chapter 6 (Active Cables).

3.1.1 Compliant Connectors

The USB Type-C specification defines the following standard connectors:

- USB Full-Featured Type-C receptacle
- *USB 2.0* Type-C receptacle
- USB Full-Featured Type-C plug
- *USB 2.0* Type-C plug
- USB Type-C Power-Only plug

3.1.2 Compliant Cable Assemblies

Table 3-1 summarizes the USB Type-C standard cable assemblies along with the primary differentiating characteristics. All USB Full-Featured Type-C cables shall support simultaneous, independent signal transmission on both *USB 3.2* and *USB4™* (TX and RX pairs) data buses. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements. All cables that are either full-featured and/or are rated at more than 3 A current are Electronically Marked Cables.

Table 3-1 USB Type-C Standard Cable Assemblies

Cable Ref	Plug 1	Plug 2	USB Version	Cable Length	Current Rating	USB Power Delivery	USB Type-C Electronically Marked
CC2-3	C	C	USB 2.0	≤ 4 m	3 A	Supported	Optional
CC2-5					5 A		Required
CC3G1-3	C	C	USB 3.2 Gen1 and USB4 Gen2	≤ 2 m	3 A	Supported	Required
CC3G1-5					5 A		
CC3G2-3	C	C	USB 3.2 Gen2 and USB4 Gen2	≤ 1 m	3 A	Supported	Required
CC3G2-5					5 A		
CC4G3-3	C	C	USB4 Gen3	≤ 0.8 m	3 A	Supported	Required
CC4G3-5					5 A		

USB Type-C products are also allowed to have a captive cable. See Section 3.4.3.

3.1.3 Compliant USB Type-C to Legacy Cable Assemblies

Table 3-2 summarizes the USB Type-C legacy cable assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements. *USB 3.2* Type-C legacy cables assemblies that only offer performance up to *USB 3.1* Gen1 are not allowed by this specification. All USB Type-C to legacy cable assemblies are only defined specific to *USB 2.0* and *USB 3.2* as there are no USB Type-C to legacy cables that are uniquely applicable to *USB4*.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3 机械

3.1 概述

本章定义了 USB Type-C® 连接器和有线电缆组件。第 6 章（有源电缆）定义了数据路径中包含有源元件的电缆。

3.1.1 兼容连接器

USB Type-C 规范定义了以下标准连接器：

- USB 全功能 Type-C 插座
- *USB 2.0* Type-C 插座
- USB 全功能 Type-C 插头
- *USB 2.0* Type-C 插头
- USB Type-C 仅供电插头

3.1.2 兼容电缆组件

表 3-1 总结了 USB Type-C 标准电缆组件以及主要的区别特性。所有 USB 全功能 Type-C 电缆都应支持 *USB 3.2* 和 *USB4™*（TX 和 RX 对）数据总线上的同步、独立信号传输。表中列出的电缆长度仅供参考，代表基于电缆性能要求的实际长度。所有功能齐全和/或额定电流超过 3 A 的电缆均为电子标记电缆。

表 3-1 USB Type-C 标准线缆组件

Cable Ref	Plug 1	Plug 2	USB Version	Cable Length	Current Rating	USB Power Delivery	USB Type-C Electronically Marked
CC2-3	C	C	USB 2.0	≤ 4 m	3 A	Supported	Optional
CC2-5					5 A		Required
CC3G1-3	C	C	USB 3.2 Gen1 and USB4 Gen2	≤ 2 m	3 A	Supported	Required
CC3G1-5					5 A		
CC3G2-3	C	C	USB 3.2 Gen2 and USB4 Gen2	≤ 1 m	3 A	Supported	Required
CC3G2-5					5 A		
CC4G3-3	C	C	USB4 Gen3	≤ 0.8 m	3 A	Supported	Required
CC4G3-5					5 A		

USB Type-C 产品也允许使用固定电缆。请参阅第 3.4.3 节。

3.1.3 符合 USB Type-C 标准的旧式电缆组件

表 3-2 总结了 USB Type-C 传统电缆组件及其主要区别特征。表中列出的电缆长度仅供参考，代表基于电缆性能要求的实际长度。本规范不允许仅提供最高可达 *USB 3.1* Gen1 性能的 *USB 3.2* Type-C 传统电缆组件。所有 USB Type-C 至传统电缆组件仅针对 *USB 2.0* 和 *USB 3.2* 进行定义，因为没有专门适用于 *USB4* 的 USB Type-C 至传统电缆。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

For USB Type-C legacy cable assemblies that incorporate Rp termination, the value of this termination is required to be specified to the Default setting of USB Type-C Current even though the cable assemblies are rated for 3 A. The Rp termination in these cables is intended to represent the maximum current of a compliant legacy USB host port, not the current rating of the cable itself. The cable current rating is intentionally set to a higher level given that there are numerous non-standard power chargers that offer more than the Default levels established by the *USB 2.0* and *USB 3.1* specifications.

Table 3-2 USB Type-C Legacy Cable Assemblies

Cable Ref	Plug 1[3]	Plug 2[3]	USB Version	Cable Length	Current Rating
AC2-3	USB 2.0 Standard-A	USB 2.0 Type-C[1]	USB 2.0	≤ 4 m	3 A
AC3G2-3	USB 3.1 Standard-A	USB Full-Featured Type-C[1]	USB 3.1 Gen2	≤ 1 m	3 A
CB2-3	USB 2.0 Type-C[2]	USB 2.0 Standard-B	USB 2.0	≤ 4 m	3 A
CB3G2-3	USB Full-Featured Type-C[2]	USB 3.1 Standard-B	USB 3.1 Gen2	≤ 1 m	3 A
CmB2	USB 2.0 Type-C[2]	USB 2.0 Mini-B	USB 2.0	≤ 4 m	500 mA
CμB2-3	USB 2.0 Type-C[2]	USB 2.0 Micro-B	USB 2.0	≤ 2 m	3 A
CμB3G2-3	USB Full-Featured Type-C[2]	USB 3.1 Micro-B	USB 3.1 Gen2	≤ 1 m	3 A

Notes:

1. USB Type-C plugs associated with the "B" end of a legacy adapter cable are required to have Rp (56 kΩ ± 5%) termination incorporated into the plug assembly – see Section 4.5.3.2.2.
2. USB Type-C plugs associated with the "A" end of a legacy adapter cable are required to have Rd (5.1 kΩ ± 20%) termination incorporated into the plug assembly – see Section 4.5.3.2.1.
3. Refer to Section 3.7.5.3 for the mated resistance and temperature rise required for the legacy plugs.

3.1.4 Compliant USB Type-C to Legacy Adapter Assemblies

Table 3-3 summarizes the USB Type-C legacy adapter assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements. All USB Type-C to legacy adapter assemblies are only defined specific to *USB 2.0* and *USB 3.2* as there are no USB Type-C to legacy adapters that are uniquely applicable to *USB4*.

Table 3-3 USB Type-C Legacy Adapter Assemblies

Adapter Ref	Plug	Receptacle[3]	USB Version	Cable Length	Current Rating
CμBR2-3	USB 2.0 Type-C[1]	USB 2.0 Micro-B	USB 2.0	≤ 0.15 m	3 A
CAR3G1-3	USB Full-Featured Type-C[2]	USB 3.1 Standard-A	USB 3.1 Gen1	≤ 0.15 m	3 A

Notes:

1. USB Type-C plugs associated with the "B" end of a legacy adapter are required to have Rp (56 kΩ ± 5%) termination incorporated into the plug assembly – see Section 4.5.3.2.2.
2. USB Type-C plugs associated with the "A" end of a legacy adapter are required to have Rd (5.1 kΩ ± 20%) termination incorporated into the plug assembly – see Section 4.5.3.2.1.
3. Refer to Section 3.7.6.3 for the mated resistance and temperature rise required for the legacy receptacles.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

对于包含 Rp 端接的 USB Type-C 旧式电缆组件，即使电缆组件的额定电流为 3 A，也需要将此端接值指定为 USB Type-C 电流的默认设置。这些电缆中的 Rp 端接旨~~在表示兼容旧式 USB~~ 主机端口的最大电流，而不是电缆本身的电流额定值。鉴于有~~许~~多非标准电源充电器提供的电流超过 *USB 2.0* 和 *USB 3.1* 规范规定的默认水平，因此有意将电缆电流额定值设置为更高的水平。

表 3-2 USB Type-C 传统电缆组件

Cable Ref	Plug 1[3]	Plug 2[3]	USB Version	Cable Length	Current Rating
AC2-3	USB 2.0 Standard-A	USB 2.0 Type-C[1]	USB 2.0	≤ 4 m	3 A
AC3G2-3	USB 3.1 Standard-A	USB Full-Featured Type-C[1]	USB 3.1 Gen2	≤ 1 m	3 A
CB2-3	USB 2.0 Type-C[2]	USB 2.0 Standard-B	USB 2.0	≤ 4 m	3 A
CB3G2-3	USB Full-Featured Type-C[2]	USB 3.1 Standard-B	USB 3.1 Gen2	≤ 1 m	3 A
CmB2	USB 2.0 Type-C[2]	USB 2.0 Mini-B	USB 2.0	≤ 4 m	500 mA
CμB2-3	USB 2.0 Type-C[2]	USB 2.0 Micro-B	USB 2.0	≤ 2 m	3 A
CμB3G2-3	USB Full-Featured Type-C[2]	USB 3.1 Micro-B	USB 3.1 Gen2	≤ 1 m	3 A

笔记：

1. 与传统适配器电缆 “ B ” 端相关的 USB Type-C 插头需要在插头组件中集成 Rp (56 kΩ ± 5%) 终端电阻 - 请参阅第 4.5.3.2.2 节。 2. 与传统适配器电缆 “ A ” 端相关的 USB Type-C 插头需要在插头组件中集成 Rd (5.1 kΩ ± 20%)

插头组件中包括端接 – 见第 4.5.3.2.1 节。3. 有关传统插头所需的配接电阻和温升，请参阅第 3.7.5.3 节。

3.1.4 兼容 USB Type-C 至传统适配器组件

表 3-3 总结了 USB Type-C 旧版适配器组件及其主要区别特征。表中列出的电缆长度仅供参考，代表基于电缆性能要求的实际长度。所有 USB Type-C 至旧版适配器组件仅针对 *USB 2.0* 和 *USB 3.2* 定义，因为没有专门适用于 *USB4* 的 USB Type-C 至旧版适配器。

表 3-3 USB Type-C 传统适配器组件

Adapter Ref	Plug	Receptacle[3]	USB Version	Cable Length	Current Rating
CμBR2-3	USB 2.0 Type-C[1]	USB 2.0 Micro-B	USB 2.0	≤ 0.15 m	3 A
CAR3G1-3	USB Full-Featured Type-C[2]	USB 3.1 Standard-A	USB 3.1 Gen1	≤ 0.15 m	3 A

笔记：

1. 与传统适配器 “ B ” 端相关的 USB Type-C 插头需要在插头组件中集成 Rp（56 kΩ ± 5%）终端 - 请参阅第 4.5.3.2.2 节。 2. 与传统适配器 “ A ” 端相关的 USB Type-C 插头需要在插头组件中集成 Rd（5.1 kΩ ± 20%）终端 - 请参阅第 4.5.3.2.1 节。 3. 有关传统插座所需的配对电阻和温升，请参阅第 3.7.6.3 节。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.2 USB Type-C Connector Mating Interfaces

This section defines the connector mating interfaces, including the connector interface drawings, pin assignments, and descriptions. All dimensions in figures are in millimeters

3.2.1 Interface Definition

Figure 3-1 and Figure 3-3 show, respectively, the USB Type-C receptacle and USB Full-Featured Type-C plug interface dimensions.

Figure 3-11 shows the *USB 2.0* Type-C plug interface dimensions. The dimensions that govern the mating interoperability are specified. All the REF dimensions are provided for reference only, not hard requirements.

Key features, configuration options, and design areas that need attention:

1. Figure 3-1 shows a vertical-mount receptacle. Other PCB mounting types such as right-angle mount and mid-mount are allowed.
2. A mid-plate is required between the top and bottom signals inside the receptacle tongue to manage crosstalk in full-featured applications. The mid-plate shall be connected to the PCB ground with at least two grounding points. A reference design of the mid-plate is provided in Section 3.2.2.1.
3. Retention of the cable assembly in the receptacle is achieved by the side-latches in the plug and features on the sides of the receptacle tongue. Side latches are required for all plugs except plugs used for docking with no cable attached. Side latches shall be connected to ground inside the plug. A reference design of the side latches is provided in Section 3.2.2.2 along with its grounding scheme. Docking applications may not have side latches, requiring special consideration regarding EMC (Electromagnetic Compatibility).
4. The EMC shielding springs are required inside the cable plug. The shielding spring shall be connected to the plug shell. No EMC shielding spring finger tip of the USB Full-Featured Type-C plug or *USB 2.0* Type-C plug shall be exposed in the plug housing opening of the unmated USB Type-C plug (see Figure 3-12). Section 3.2.2.3 shows reference designs of the EMC spring.
5. Shorting of any signal or power contact spring to the plug metal shell is not allowed. The spring in the deflected state should not touch the plug shell. An isolation layer (e.g., Kapton tape placed on the plug shell) is recommended to prevent accidental shorting due to plug shell deformation.
6. The USB Type-C receptacle shall provide an EMC ground return path through one of the following options:
   - a system of specific points of contact on the receptacle outer shell (e.g., spring fingers or spring fingers and formed solid bumps),
   - internal EMC pads, or
   - a combination of both points of contact on the receptacle outer shell and internal EMC pads.

   If points of contacts are used on the receptacle, then the receptacle points of contact shall make connection with the mated plug within the contact zones defined in Figure 3-2. A minimum of four separate points of contact are required. Additional points of contact are allowed. See Section 3.2.2.4 for a reference design of receptacle outer shell. The reference design includes four spring fingers as points of contact. Alternate configurations may include spring fingers on the A contact side or B contact side and formed solid bumps (e.g., dimples) on the B contact side or A contact side, respectively. Spring fingers are required on a minimum of one side to provide a pressure fit on

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.2 USB Type-C 连接器配接接口

本节定义连接器配合接口，包括连接器接口图、引脚分配和说明。图中所有尺寸以毫米为单位

3.2.1 接口定义

图 3-1 和图 3-3 分别显示了 USB Type-C 插座和 USB 全功能 Type-C 插头接口尺寸。

图 3-11 显示了 *USB 2.0* Type-C 插头接口尺寸。指定了控制配接互操作性的尺寸。所有 REF 尺寸仅供参考，并非硬性要求。

主要功能、配置选项以及需要注意的设计领域：

1. 图 3-1 显示了垂直安装插座。允许使用其他 PCB 安装类型，例如直角安装和中部安装。 2. 插座舌片内部的顶部和底部信号之间需要中间板来管理全功能应用中的串扰。中间板应通过至少两个接地点连接到 PCB 接地。第 3.2.2.1 节提供了中间板的参考设计。 3. 插座中的电缆组件通过插头中的侧闩锁和插座舌片侧面的功能实现。所有插头都需要侧闩锁，但用于对接且未连接电缆的插头除外。侧闩锁应连接到插头内的接地。第 3.2.2.2 节提供了侧闩锁的参考设计及其接地方案。对接应用可能没有侧闩锁，需要特别考虑 EMC（电磁兼容性）。 4. 电缆插头内需要有 EMC 屏蔽弹簧。屏蔽弹簧应连接到插头外壳。未配对的 USB Type-C 插头的插头外壳开口中不得露出 USB 全功能 Type-C 插头或 *USB 2.0* Type-C 插头的 EMC 屏蔽弹簧指尖（见图 3-12）。第 3.2.2.3 节显示了 EMC 弹簧的参考设计。

5.不允许将任何信号或电源接触弹簧短接至插头金属外壳。
弹簧在弯曲状态下不应接触插头外壳。建议使用隔离层（例如，在插头外壳上放置 Kapton 胶带），以防止插头外壳变形导致意外短路。

6. USB Type-C 插座应通过以下选项之一提供 EMC 接地返回路径：

- 插座外壳上的特定接触点系统（例如，弹簧指或弹簧指和形成的固体凸块），
- 内部 EMC 垫，或
- 插座外壳上的接触点和内部 EMC 垫的组合。

如果插座上使用接触点，则插座接触点应
在图 3-2 定义的接触区内与配对插头连接。至少需要四个单独的接触点。允许有额外的接触点。请参阅第 3.2.2.4 节了解插座外壳的参考设计。参考设计包括四个弹簧指作为接触点。替代配置可能分别包括 A 触点侧或 B 触点侧上的弹簧指以及 B 触点侧或 A 触点侧上的成型实心凸块（例如，凹坑）。

至少一侧需要弹簧夹来提供压力配合

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

opposing sides of the plug shell. Additional bumps may be used, but if bumps are on opposing sides of the receptacle shell, the minimum distance between the bumps shall be greater than the maximum plug shell defined dimension.

If internal EMC pads are present in the receptacle, then they shall comply with the requirements defined in Figure 3-1. The shielding pads shall be connected to the receptacle shell. If no receptacle shell is present, then the receptacle shall provide a means to connect the shielding pad to ground. See Section 3.2.2.3 for a reference design of the shielding pad and ground connection.

7. This specification defines the USB Type-C receptacle shell length of 6.20 mm as a reference dimension. The USB Type-C receptacle is designed to have shell length of 6.20 ± 0.20 mm to provide proper mechanical and electrical mating of the plug to the receptacle (e.g., full seating of the plug in the receptacle and protection of the receptacle tongue during insertion/withdrawal). The USB Type-C receptacle at the system level should be implemented such that the USB Type-C receptacle connector mounted in the associated system hardware has an effective shell length equal to 6.20 ± 0.20 mm.

8. The USB Type-C connector mating interface is defined so that the electrical connection may be established without the receptacle shell. To prevent excessive misalignment of the plug when it enters or exits the receptacle, the enclosure should have features to guide the plug for insertion and withdrawal when a modified receptacle shell is present. If the USB Type-C receptacle shell is modified from the specified dimension, then the recommended lead in from the receptacle tongue to the plug point of entry is 1.5 mm minimum when mounted in the system.

   This specification allows receptacle configurations with a conductive shell, a non-conductive shell, or no shell. The following requirements apply to the receptacle contact dimensions shown in SECTION A-A and ALTERNATE SECTION A-A shown in Figure 3-1:

   - If the receptacle shell is conductive, then the receptacle contact dimensions of SECTION A-A or ALTERNATE SECTION A-A shown in Figure 3-1 shall be used.
   - If the receptacle shell is non-conductive, then the receptacle contact dimensions of ALTERNATE SECTION A-A shown in Figure 3-1 shall be used. The contact dimensions of SECTION A-A are not allowed.
   - If there is no receptacle shell, then the receptacle contact dimensions of either SECTION A-A or ALTERNATE SECTION A-A shown in Figure 3-1 shall be used. If there is no receptacle shell and the receptacle is used in an implementation that does not effectively provide a conductive shell, then a receptacle with the contact dimensions of ALTERNATE SECTION A-A shown in Figure 3-1 should be used.

9. A paddle card (e.g., PCB) may be used in the USB Type-C plug to manage wire termination and electrical performance. Section 3.2.2.5 includes the guidelines and a design example for a paddle card.

10. This specification does not define standard footprints. Figure 3-4 shows an example SMT (surface mount) footprint for the vertical receptacle shown in Figure 3-1. Additional reference footprints and mounting configurations are shown in Figure 3-5, Figure 3-6, Figure 3-7, Figure 3-8, Figure 3-9 and Figure 3-10.

11. The receptacle shell shall be connected to the PCB ground plane.

12. All VBUS pins shall be connected together in the USB Type-C plug.

13. All Ground return pins shall be connected together in the USB Type-C plug.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

插头外壳的相对两侧。可以使用额外的凸块，但如果凸块位于插座外壳的相对两侧，凸块之间的最小距离应大于插头外壳定义的最大尺寸。

如果插座中有内部 EMC 垫，则它们应符合图 3-1 中定义的要求。屏蔽垫应连接到插座外壳。如果没有插座外壳，则插座应提供将屏蔽垫接地的方法。有关屏蔽垫和接地连接的参考设计，请参阅第 3.2.2.3 节。

7. 本规范将 USB Type-C 插座外壳长度 6.20 毫米定义为参考尺寸。USB Type-C 插座的外壳长度设计为 6.20 ± 0.20 毫米，以便插头与插座进行适当的机械和电气配合（例如，插头在插座中完全就位并在插入/拔出期间保护插座舌片）。系统级 USB Type-C 插座应这样实现，即安装在相关系统硬件中的 USB Type-C 插座连接器的有效外壳长度等于 6.20 ± 0.20 毫米。

8. USB Type-C 连接器配接接口的定义使得无需插座外壳即可建立电气连接。为防止插头在插入或拔出插座时过度错位，外壳应具有在插座外壳经过修改时引导插头插入和拔出的功能。如果 USB Type-C 插座外壳根据指定尺寸进行了修改，则在系统中安装时，从插座舌片到插头入口点的建议引入距离至少为 1.5 毫米。

本规范允许插座配置导电外壳、非导电外壳或无外壳。以下要求适用于图 3-1 中 A-A 部分和 A-A 替代部分所示的插座触点尺寸：

• 如果插座外壳导电，则应使用图 3-1 中所示的 A-A 截面或 A-A 替代截面的插座触点尺寸。• 如果插座外壳不导电，则应使用图 3-1 中所示的 A-A 替代截面的插座触点尺寸。不允许使用 A-A 截面的触点尺寸。• 如果没有插座外壳，则应使用图 3-1 中所示的 A-A 截面或 A-A 替代截面的插座触点尺寸。如果没有插座外壳，并且插座用于无法有效提供导电外壳的实现中，则应使用图 3-1 中所示的 A-A 替代截面的触点尺寸的插座。

9. USB Type-C 插头中可使用插卡（例如 PCB）来管理电线端接和电气性能。第 3.2.2.5 节包含插卡指南和设计示例。

10. 本规范未定义标准封装。图 3-4 显示了图 3-1 中垂直插座的 SMT（表面贴装）封装示例。其他参考封装和安装配置如图 3-5、图 3-6、图 3-7、图 3-8、图 3-9 和图 3-10 所示。

11. 插座外壳应连接至 PCB 接地平面。

12. 所有VBUS引脚应在USB Type-C插头中连接在一起。

13. USB Type-C 插头中的所有接地返回引脚都应连接在一起。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

14. All VBUS pins shall be connected together at the USB Type-C receptacle when it is in its mounted condition (e.g., all VBUS pins bussed together in the PCB).
15. All Ground return pins shall be connected together at the USB Type-C receptacle when it is in its mounted condition (e.g., all Ground return pins bussed together in the PCB).
16. The USB Type-C Power-Only plug is a depopulated version of the USB Full-Featured Type-C plug or the *USB 2.0* Type-C plug. The interface dimensions shall conform to Figure 3-3 or Figure 3-11. Contacts for CC, VBUS, and GND (i.e., A1, A4, A5, A9, A12, B1, B4, B9, and B12) shall be present. Physical presence of contacts in the other 15 contact locations is optional. The USB Type-C Power-Only plug shall only be used on a non-charger captive cable application. Implementation of Rd or CC communication on pin A5 is required in the application.

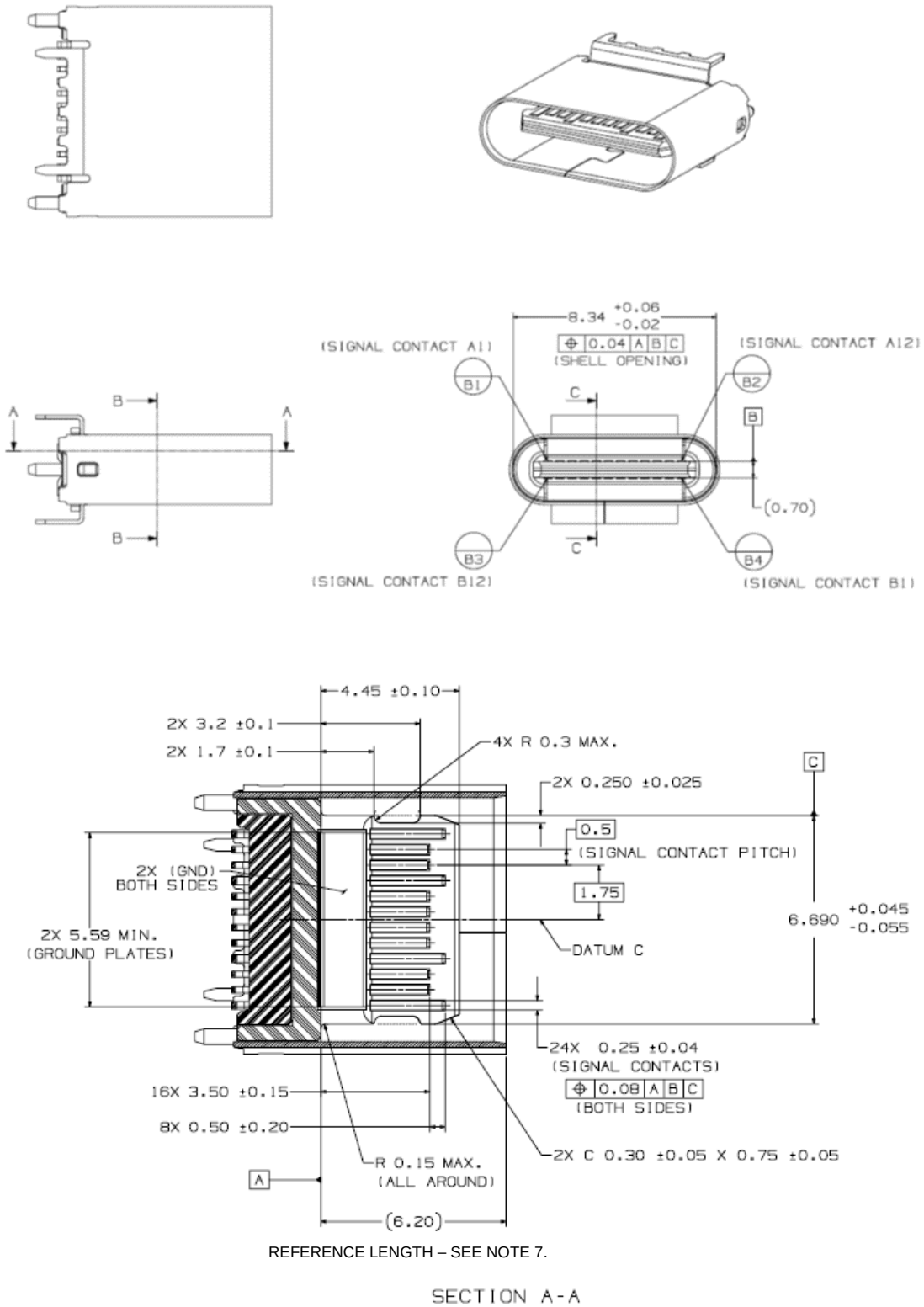
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

14. USB Type-C 插座处于安装状态时，所有 VBUS 引脚应连接在一起（例如，所有 VBUS 引脚在 PCB 中总线连接在一起）。15. USB Type-C 插座处于安装状态时，所有接地返回引脚应连接在一起（例如，所有接地返回引脚在 PCB 中总线连接在一起）。16. USB Type-C 仅供电插头是 USB 全功能 Type-C 插头或 *USB 2.0* Type-C 插头的简化版本。接口尺寸应符合图 3-3 或图 3-11 。应存在 CC、VBUS 和 GND 触点（即 A1、A4、A5、A9、A12、B1、B4、B9 和 B12）。其他 15 个触点位置的触点物理存在是可选的。USB Type-C 仅供电插头应仅用于

非充电器专用电缆应用。Rd 或 CC 通信的实现
应用程序中需要引脚A5。

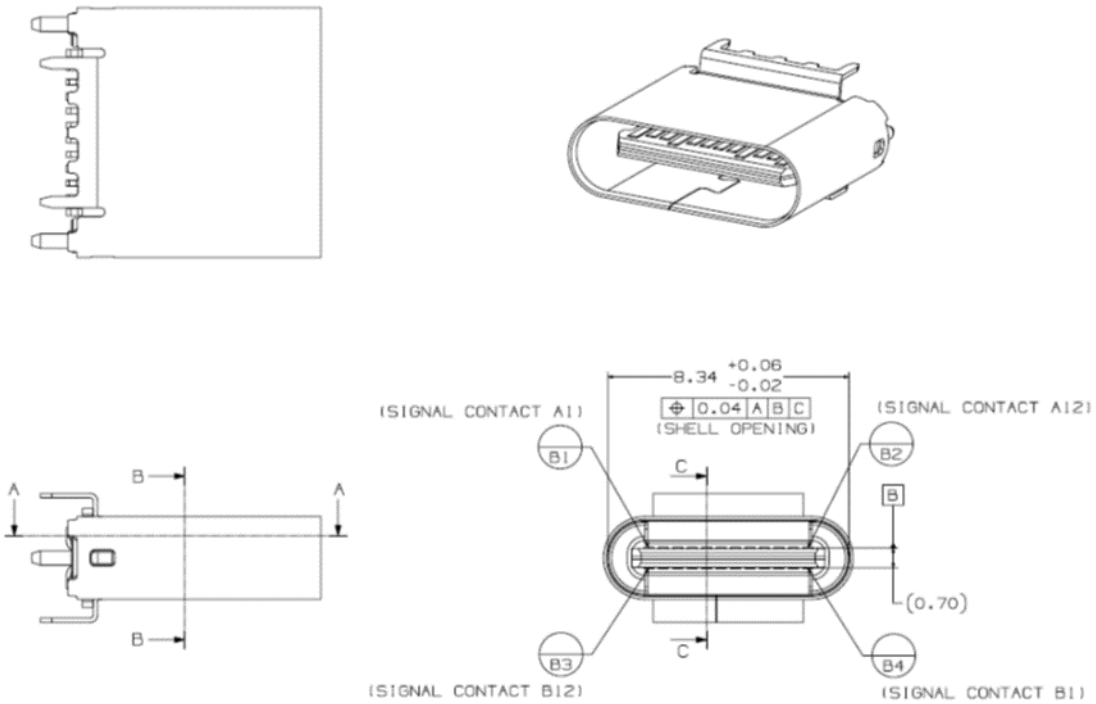
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

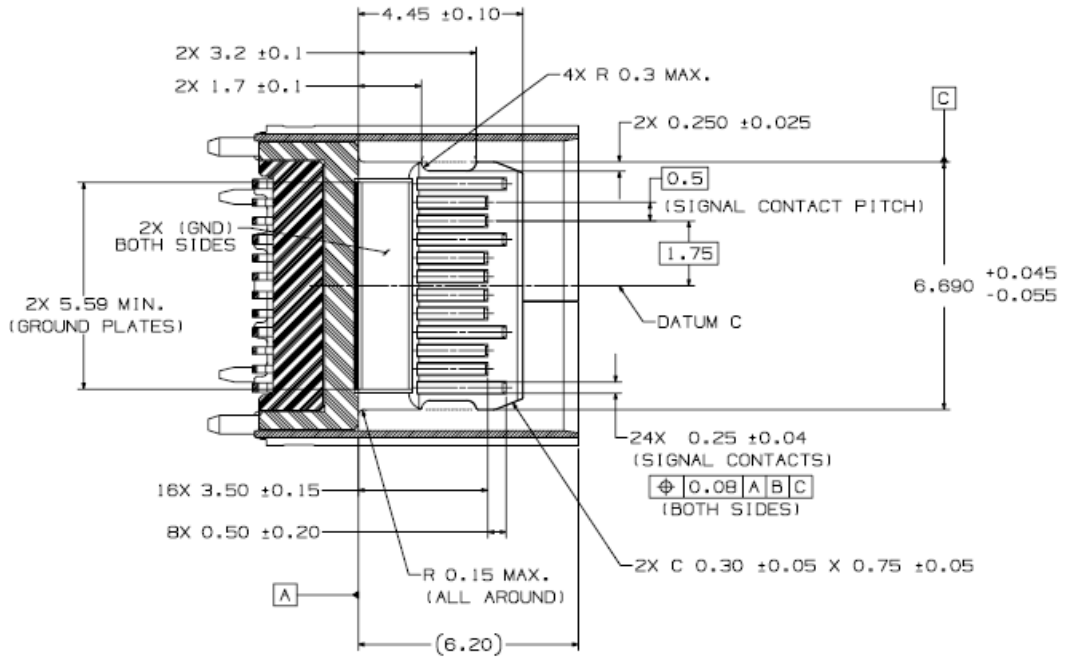
Figure 3-1 USB Type-C Receptacle Interface Dimensions



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-1 USB Type-C 插座接口尺寸



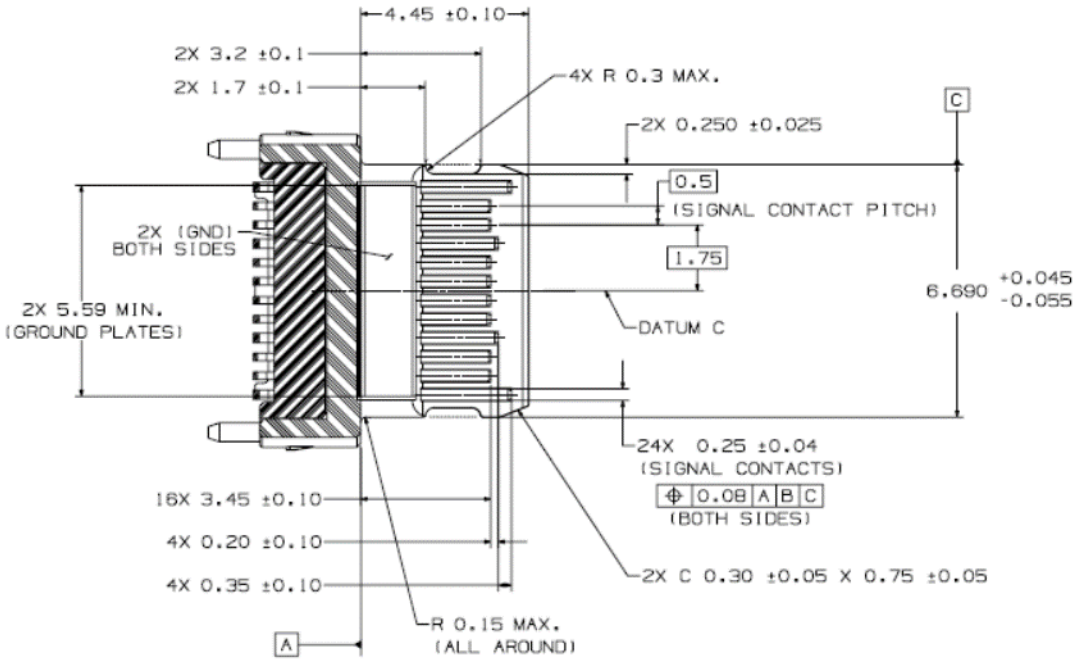


REFERENCE LENGTH – SEE NOTE 7.

SECTION A-A

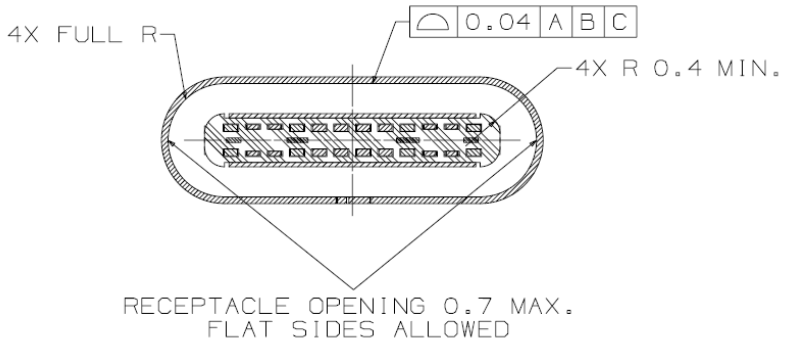
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-1 USB Type-C Receptacle Interface Dimensions, cont.



ALTERNATE SECTION A-A dimensions for use if the receptacle shell is non-conductive or there is no receptacle shell. This configuration is also allowed for receptacles with a conductive shell. See text for full requirements.

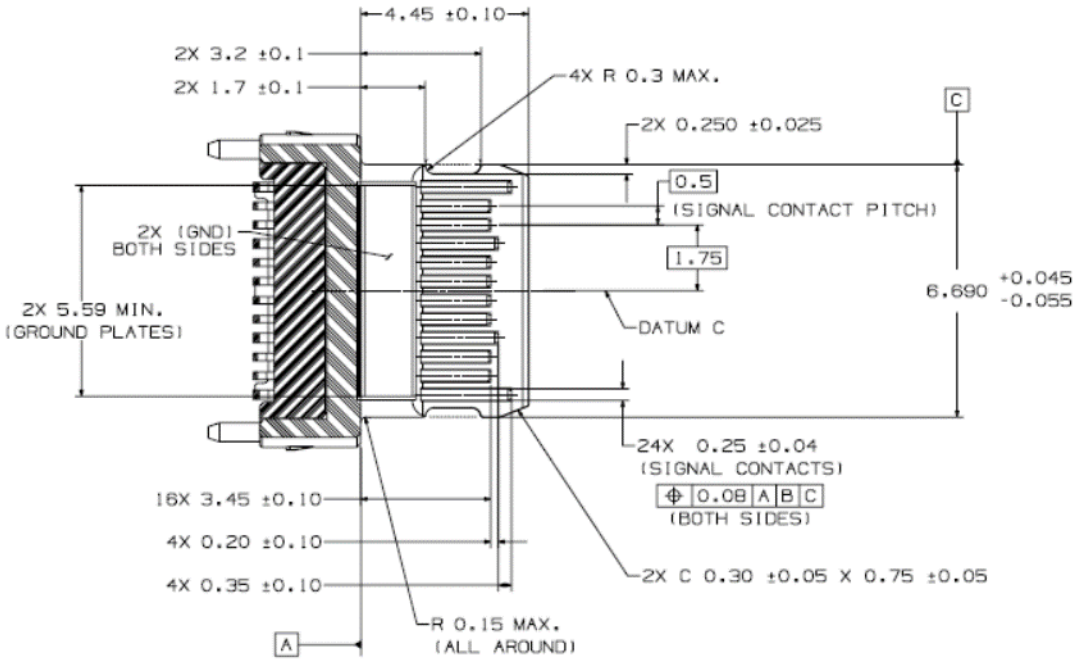
ALTERNATE SECTION A-A



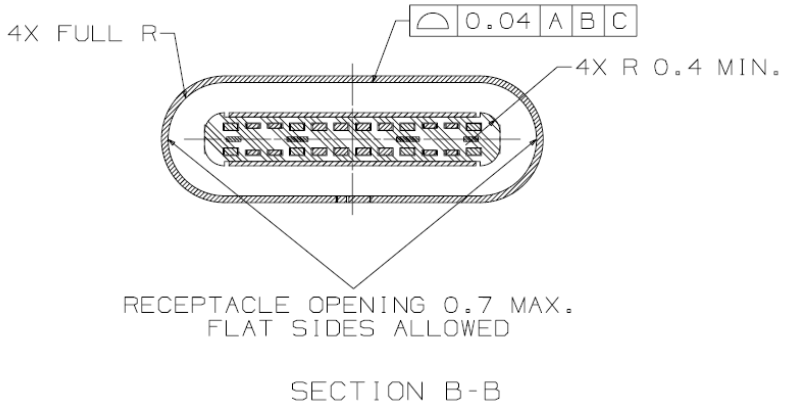
SECTION B-B

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-1 USB Type-C 插座接口尺寸（续）

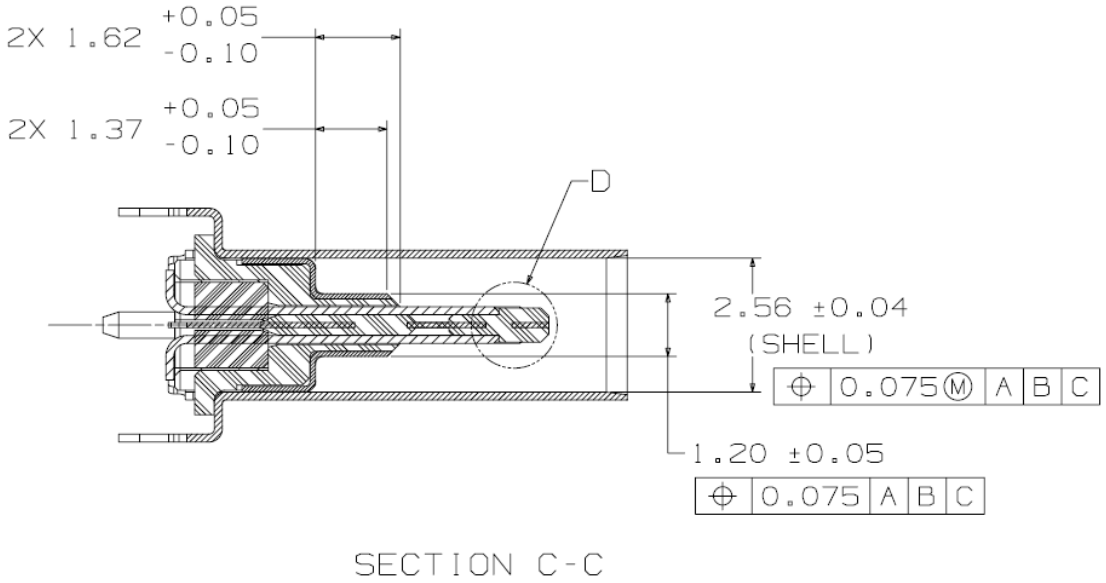


如果插座外壳不导电或没有插座外壳，则使用替代部分 A-A 尺寸。这种配置也适用于具有导电外壳的插座。请参阅文本了解完整要求。

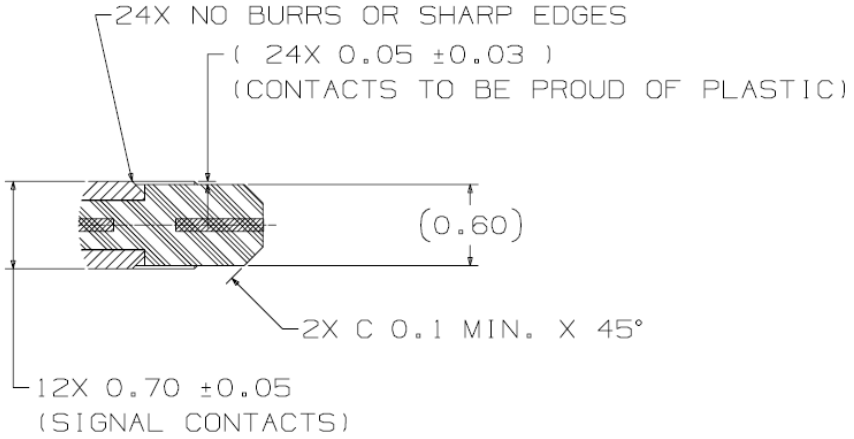


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-1 USB Type-C Receptacle Interface Dimensions, cont.



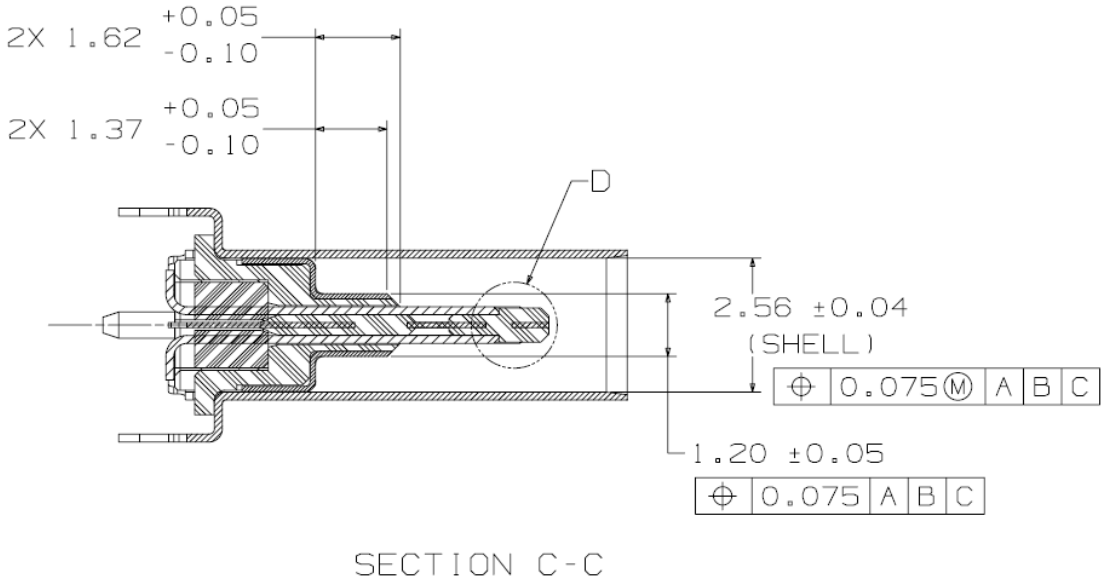
SECTION C-C

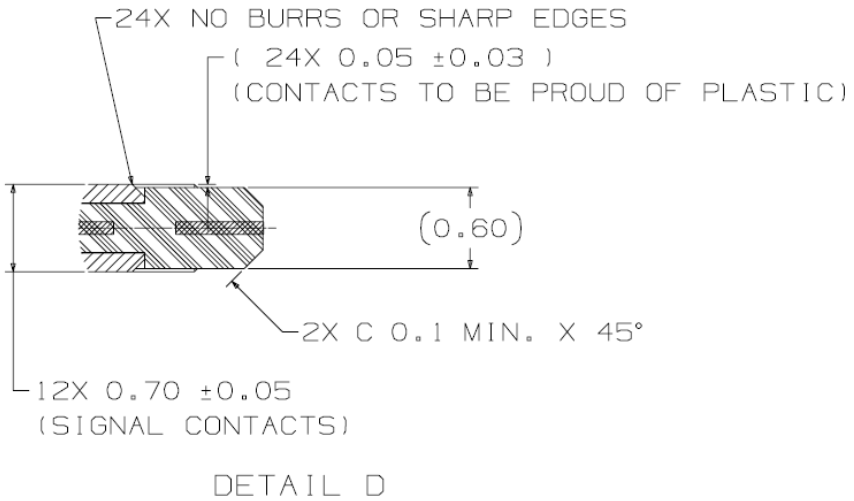


DETAIL D

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

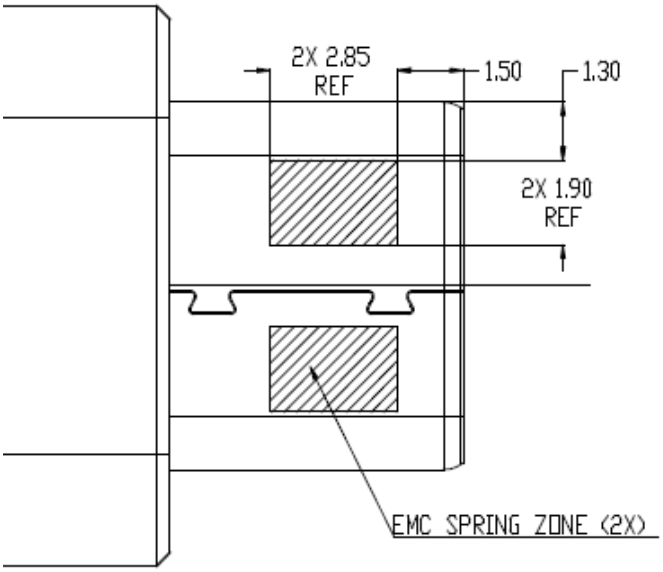
图 3-1 USB Type-C 插座接口尺寸（续）

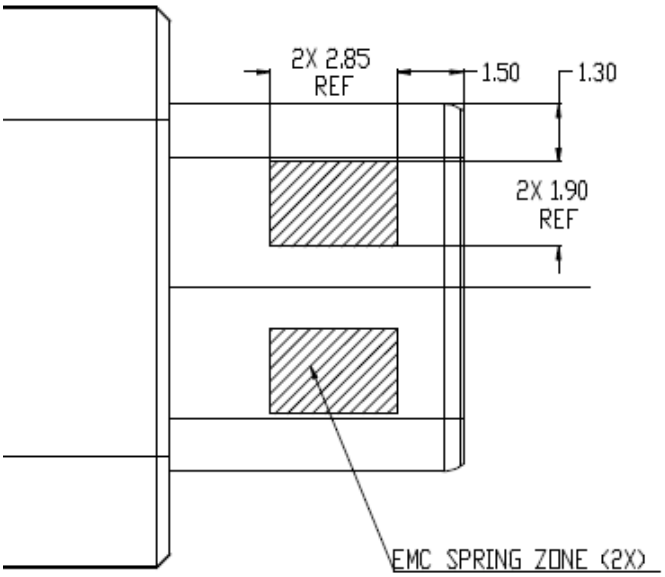




Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

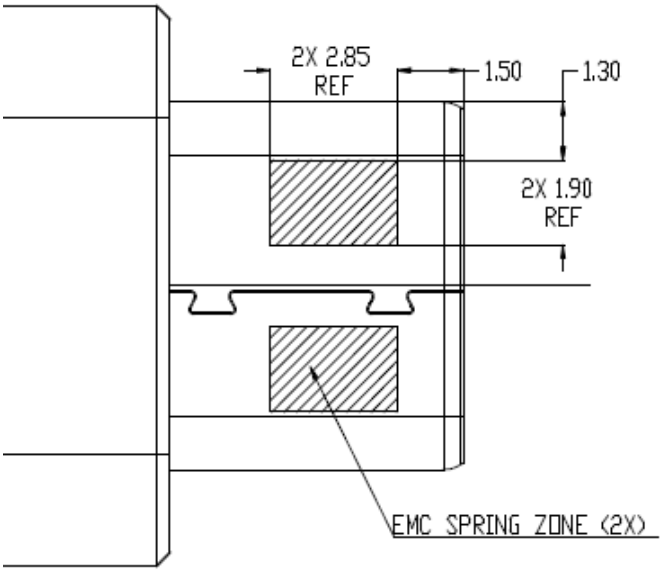
Figure 3-2 Reference Design USB Type-C Plug External EMC Spring Contact Zones

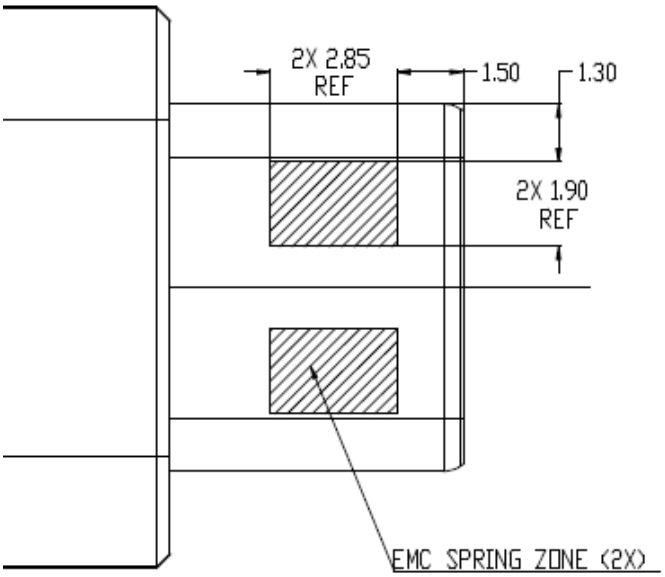




Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

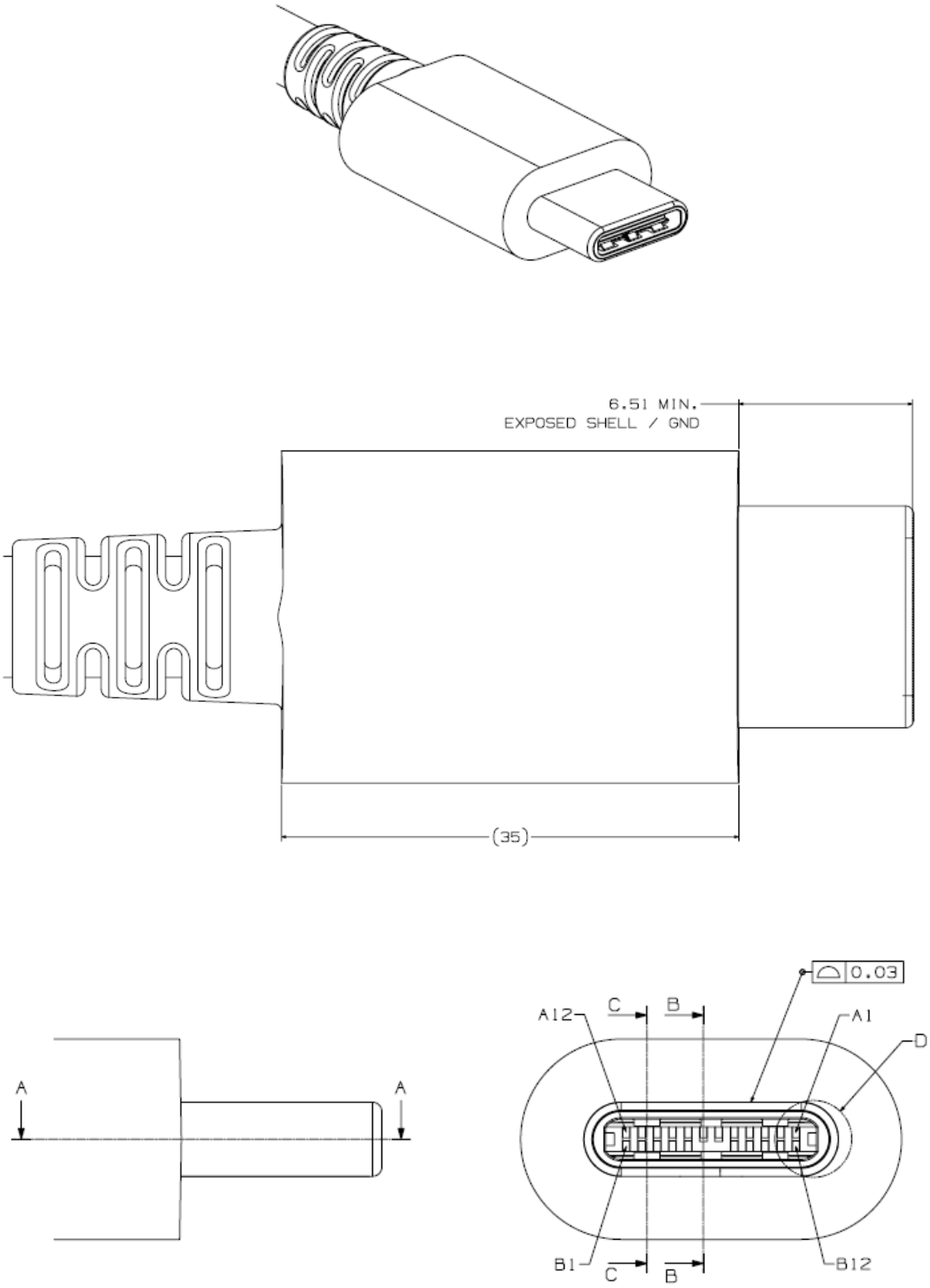
图 3-2 参考设计 USB Type-C 插头外部 EMC 弹簧接触区域





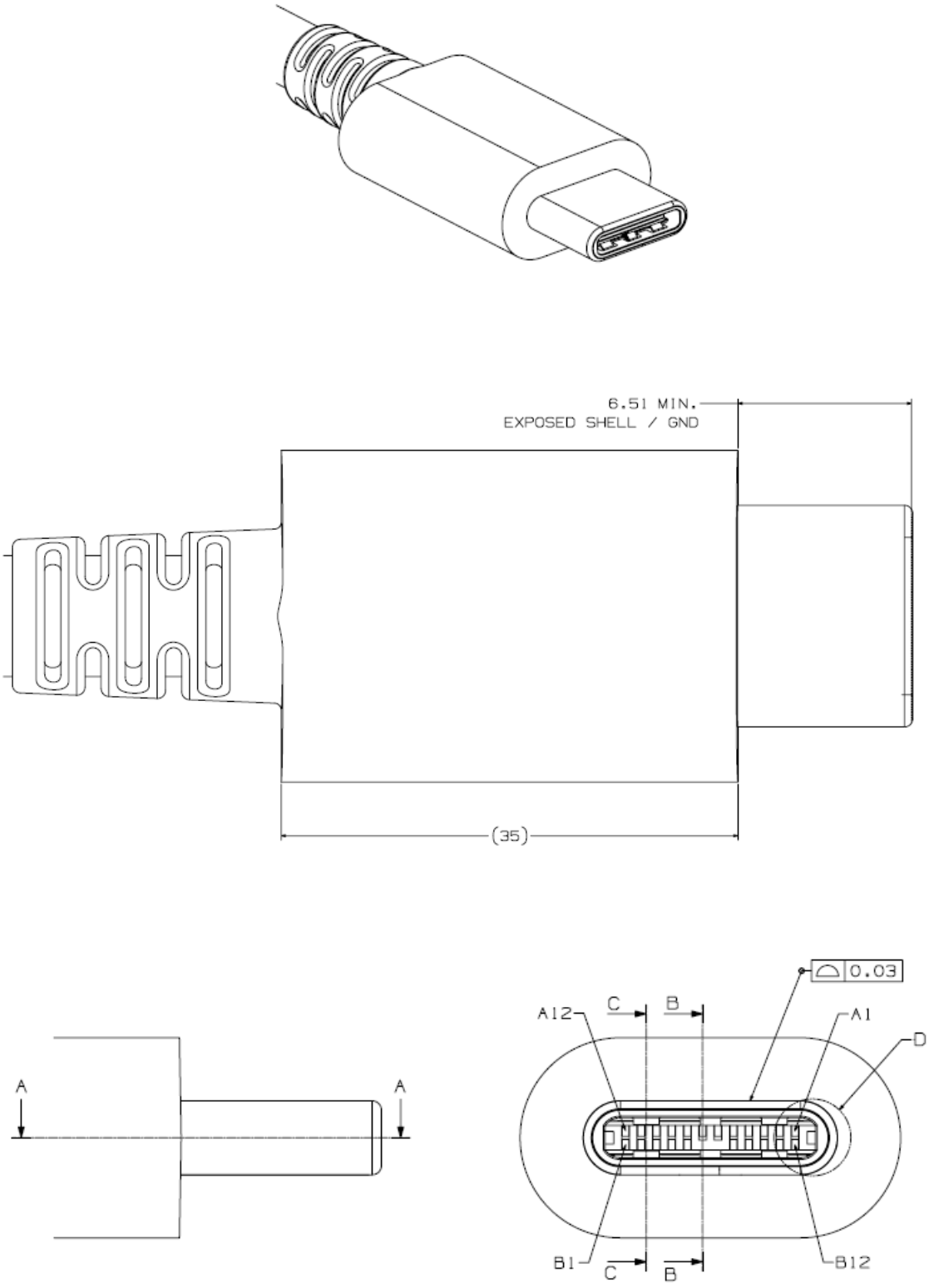
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions



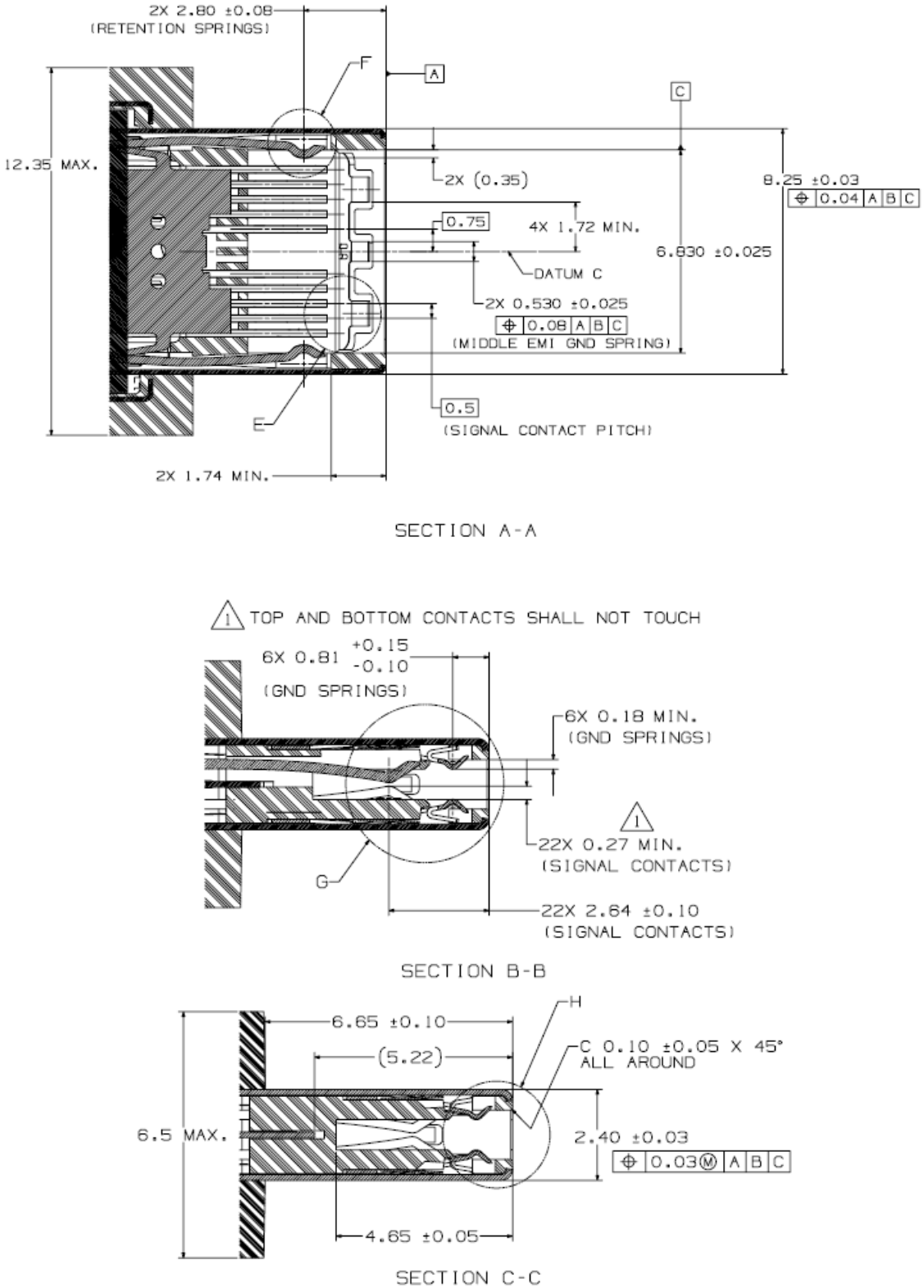
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-3 USB 全功能 Type-C 插头接口尺寸



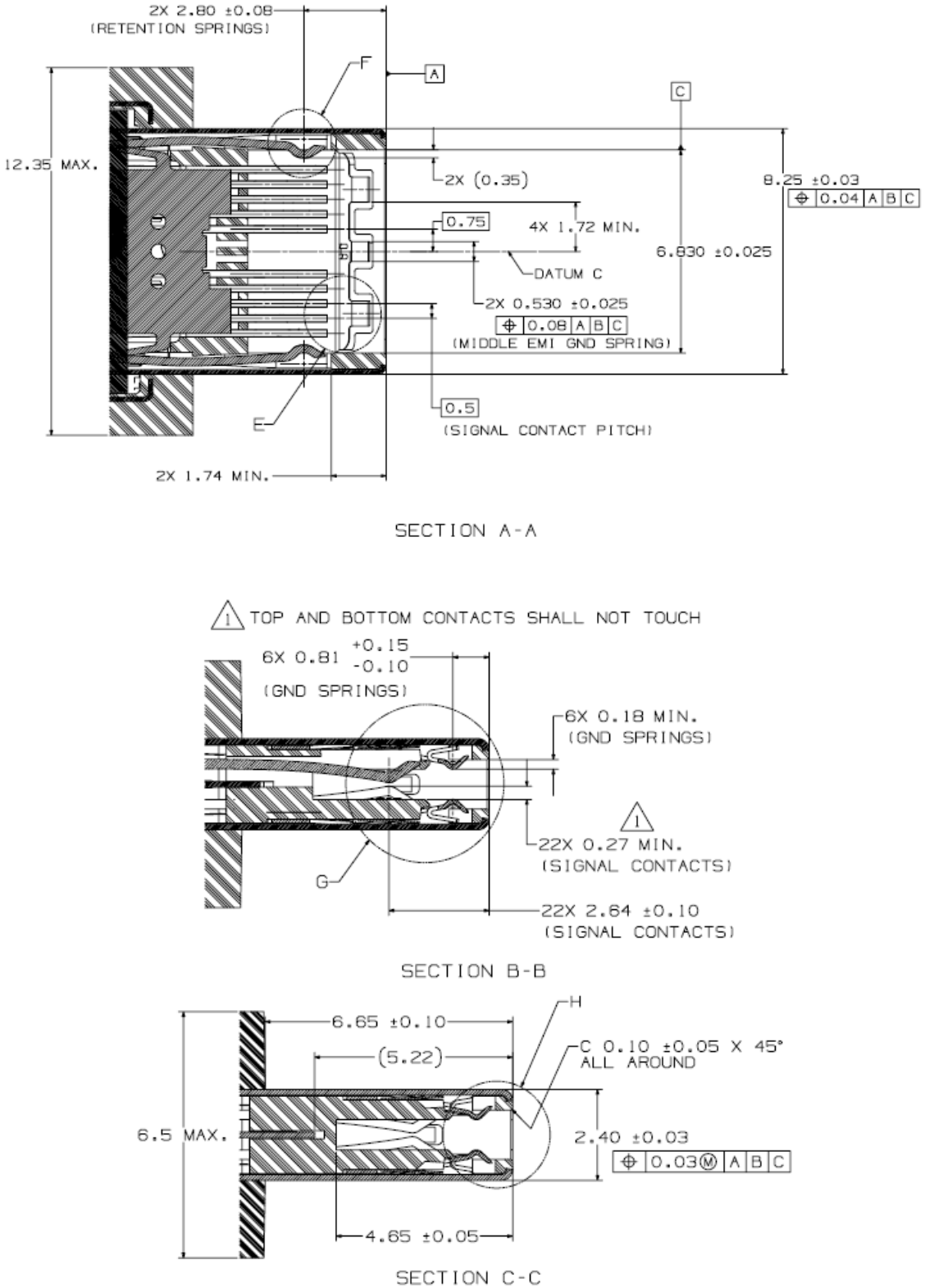
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions, cont.



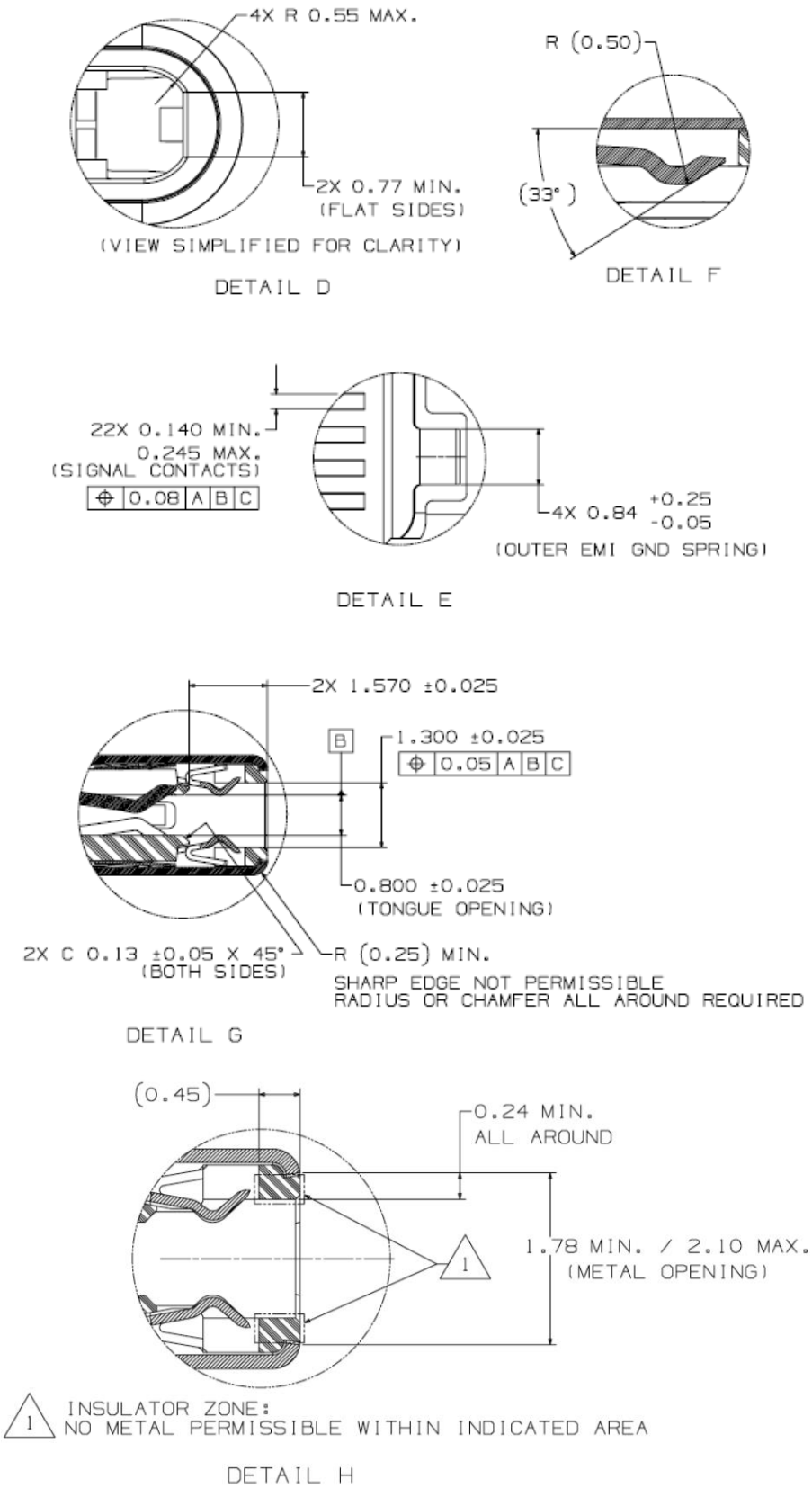
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-3 USB 全功能 Type-C 插头接口尺寸（续）



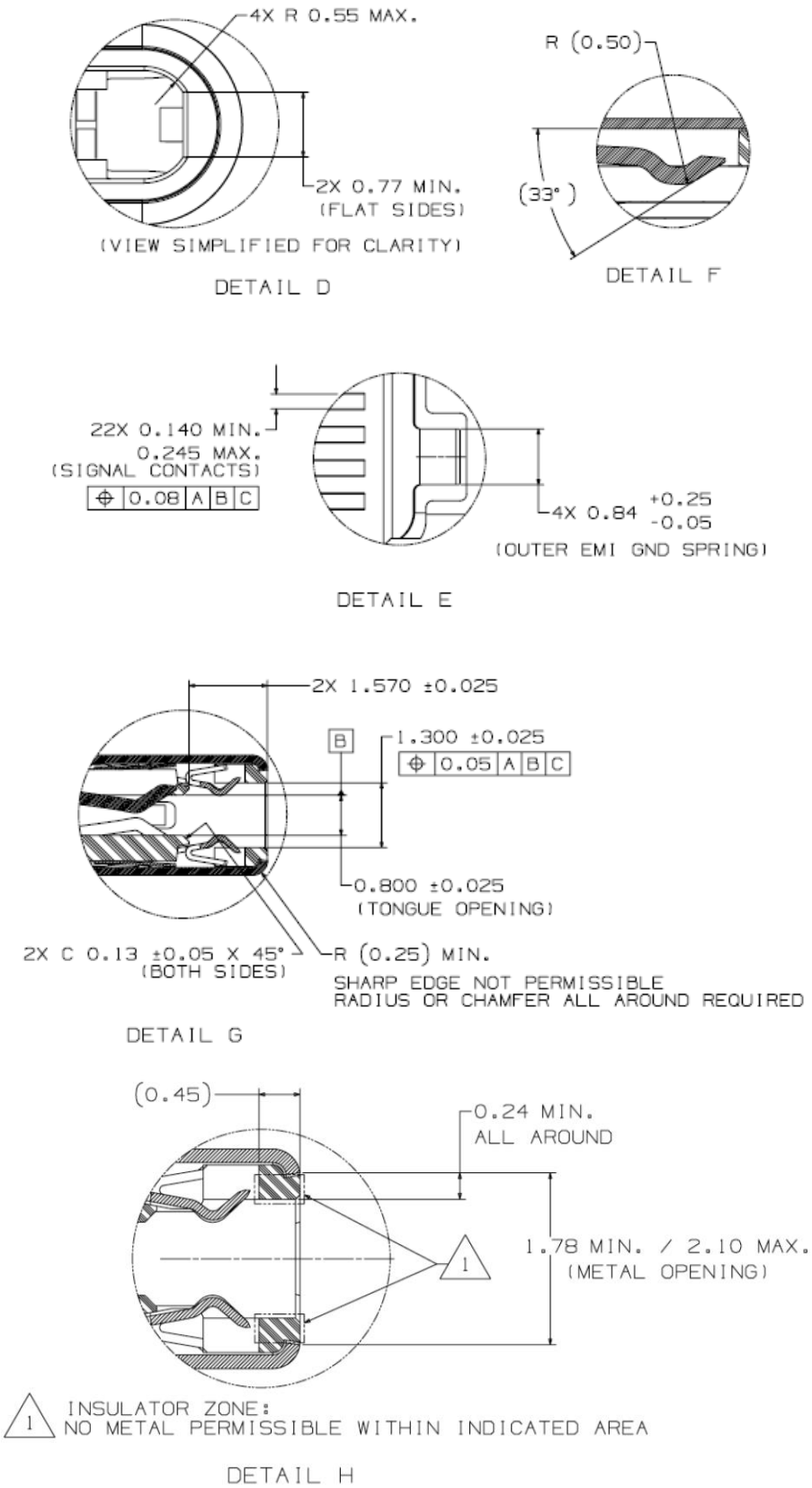
版权所有 © 2019 USB 3.0 Promoter Group。保留所有权利。

Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions, cont.



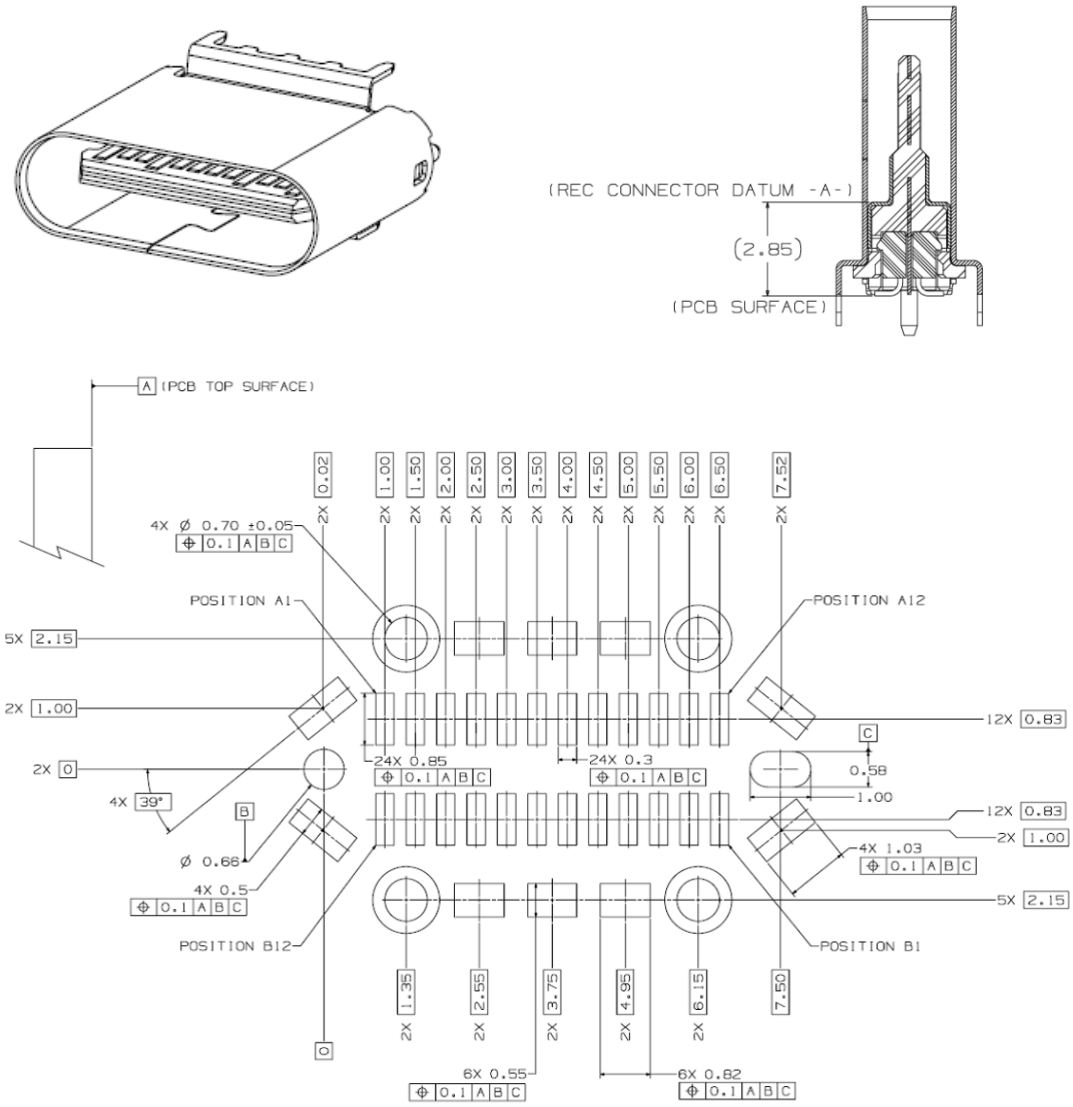
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-3 USB 全功能 Type-C 插头接口尺寸（续）



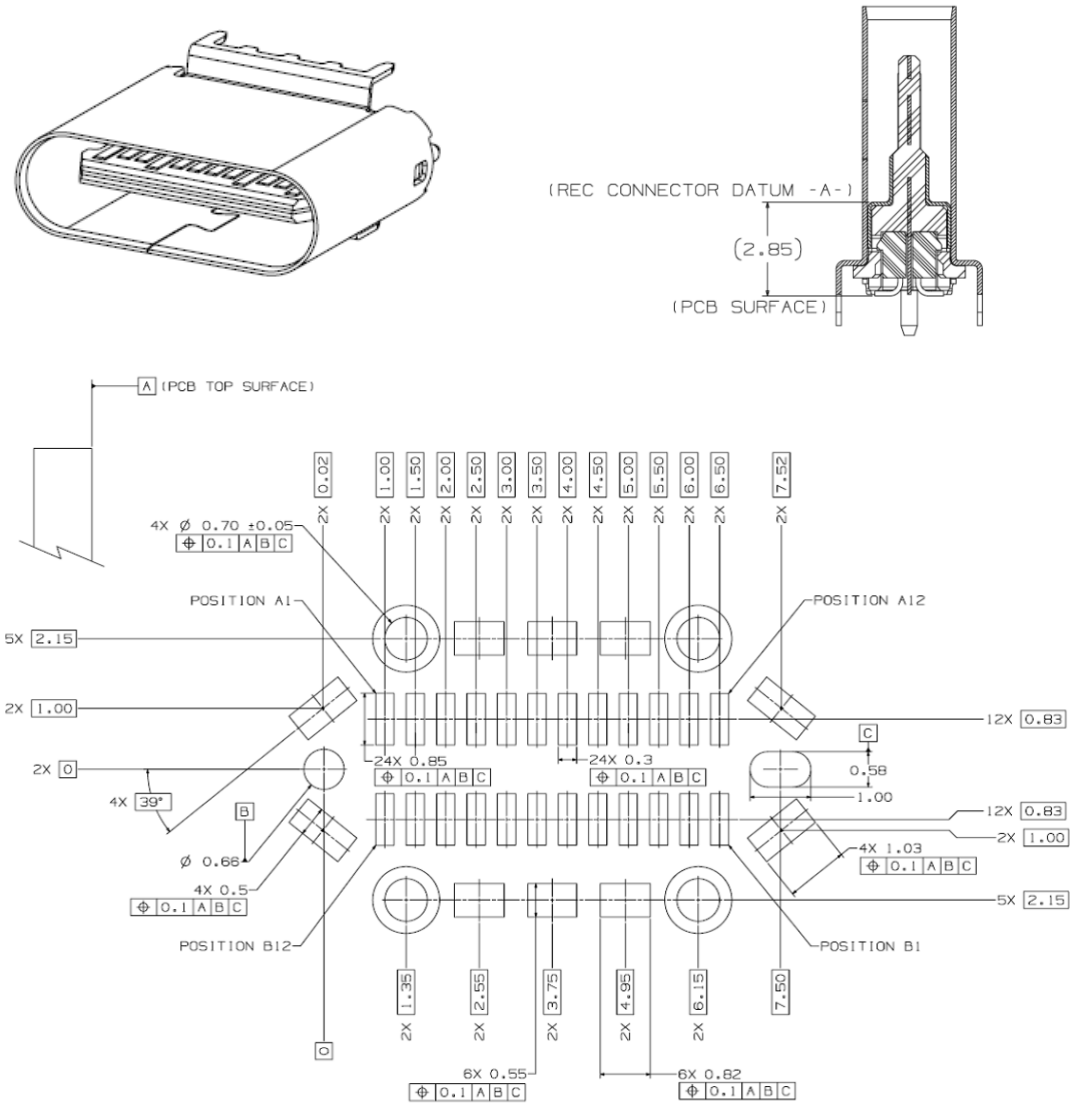
版权所有 © 2019 USB 3.0 Promoter Group。保留所有权利。

Figure 3-4 Reference Footprint for a USB Type-C Vertical Mount Receptacle (Informative)



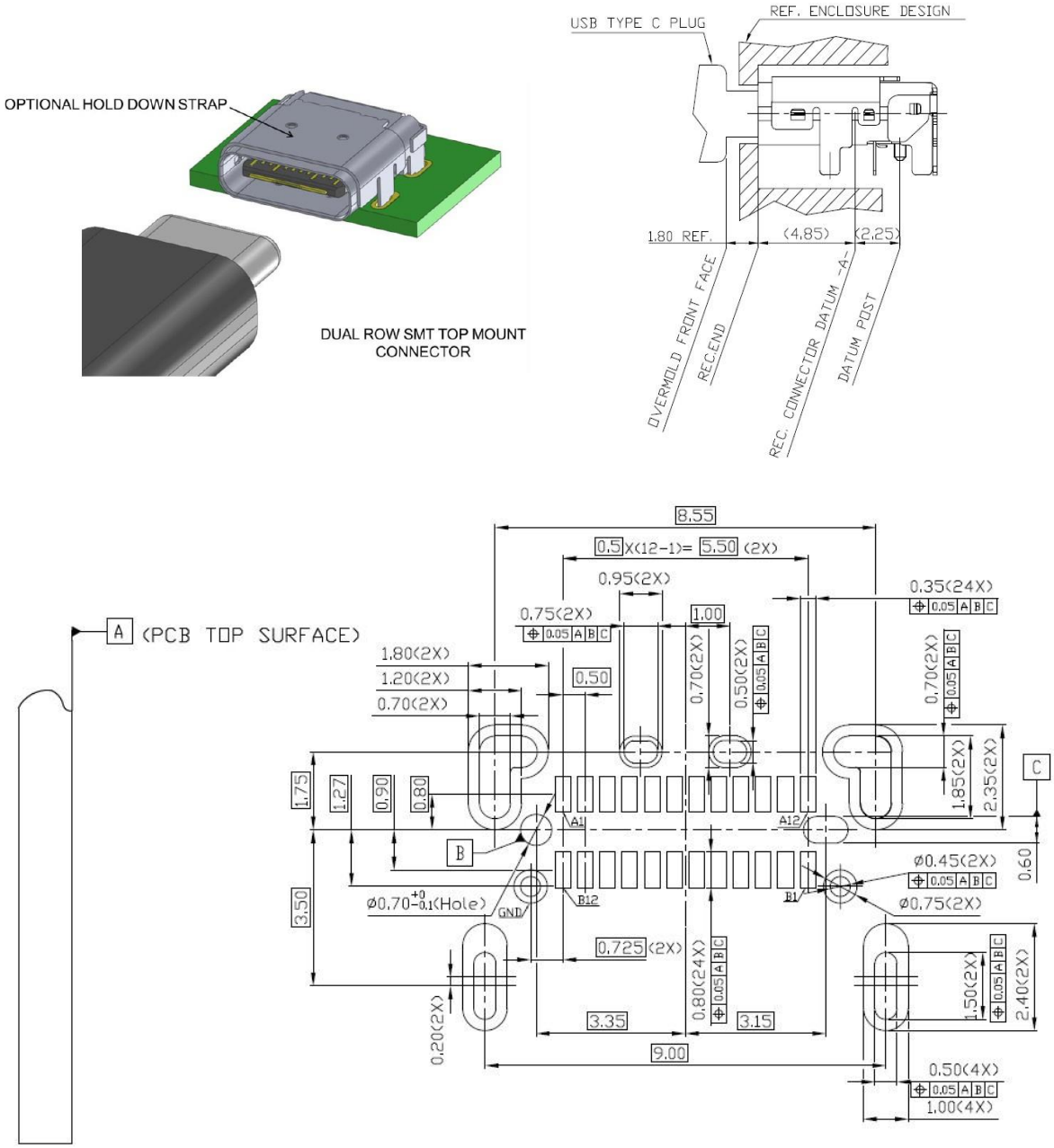
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-4 Reference Footprint for a USB Type-C Vertical Mount Receptacle (Informative)



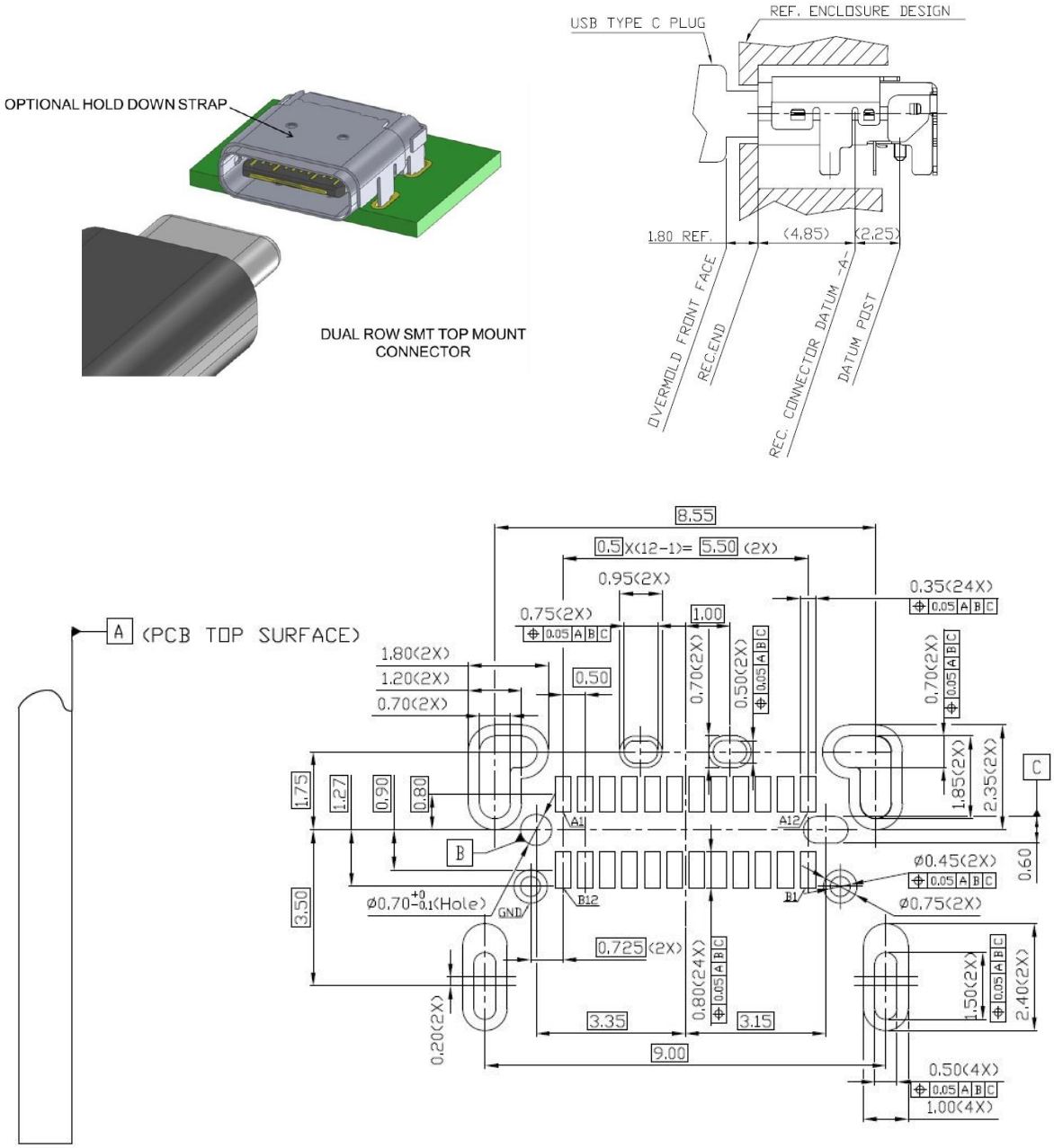
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-5 Reference Footprint for a USB Type-C Dual-Row SMT Right Angle Receptacle (Informative)



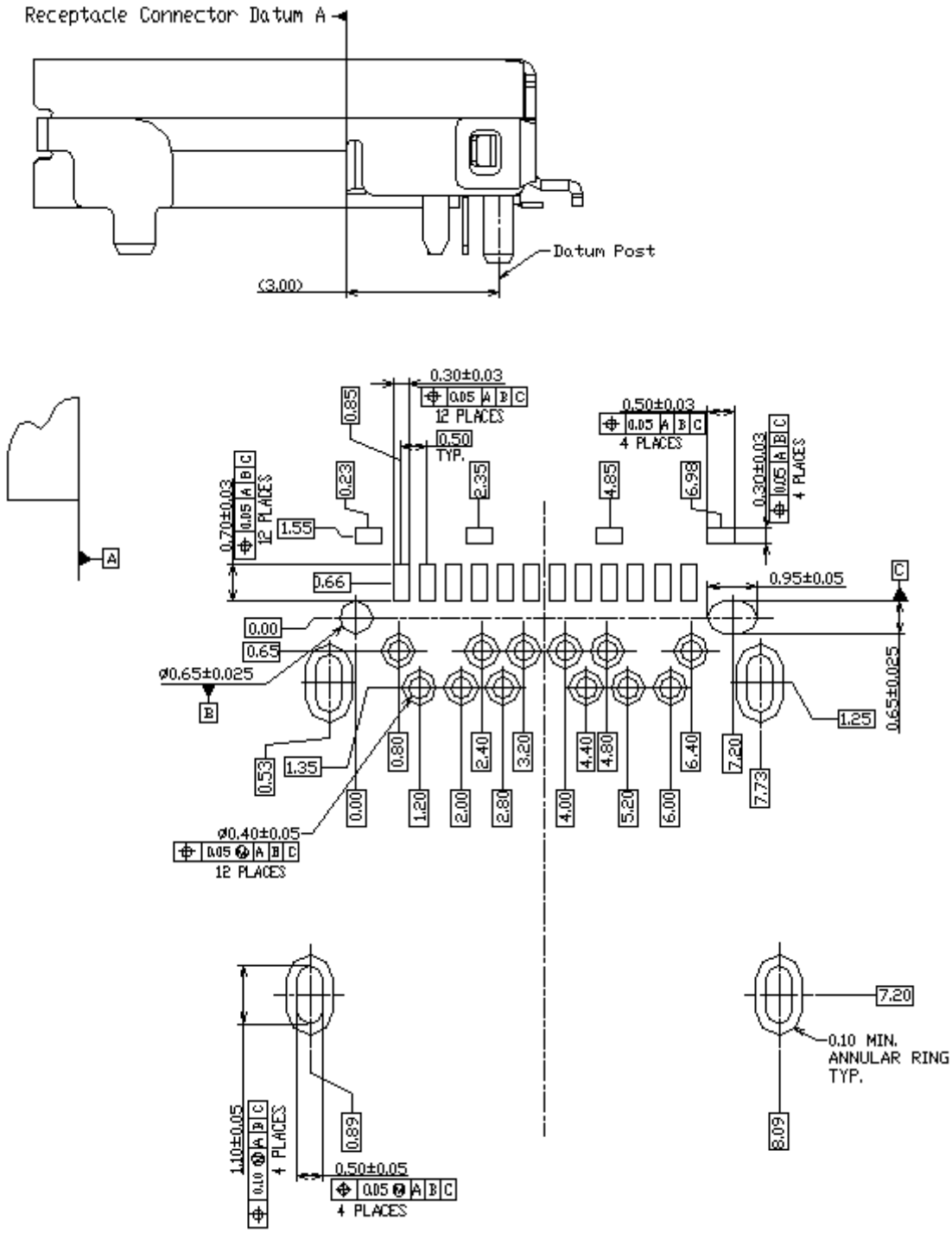
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-5 Reference Footprint for a USB Type-C Dual-Row SMT Right Angle Receptacle (Informative)



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

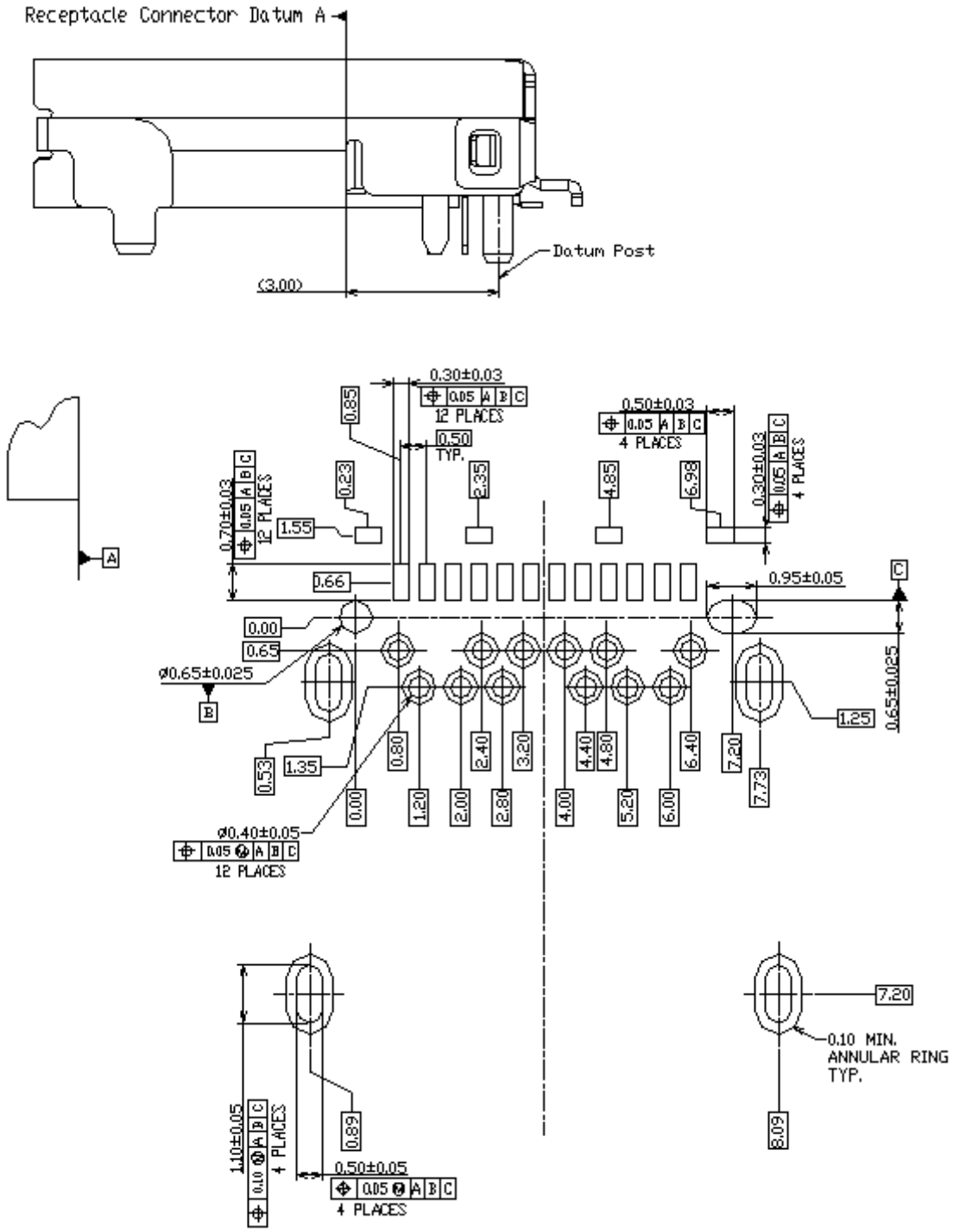
Figure 3-6 Reference Footprint for a USB Type-C Hybrid Right-Angle Receptacle (Informative)



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

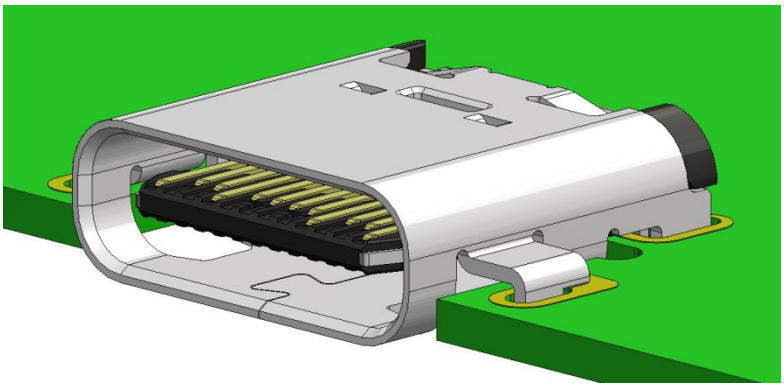
图 3-6 USB Type-C 混合直角插座的参考封装

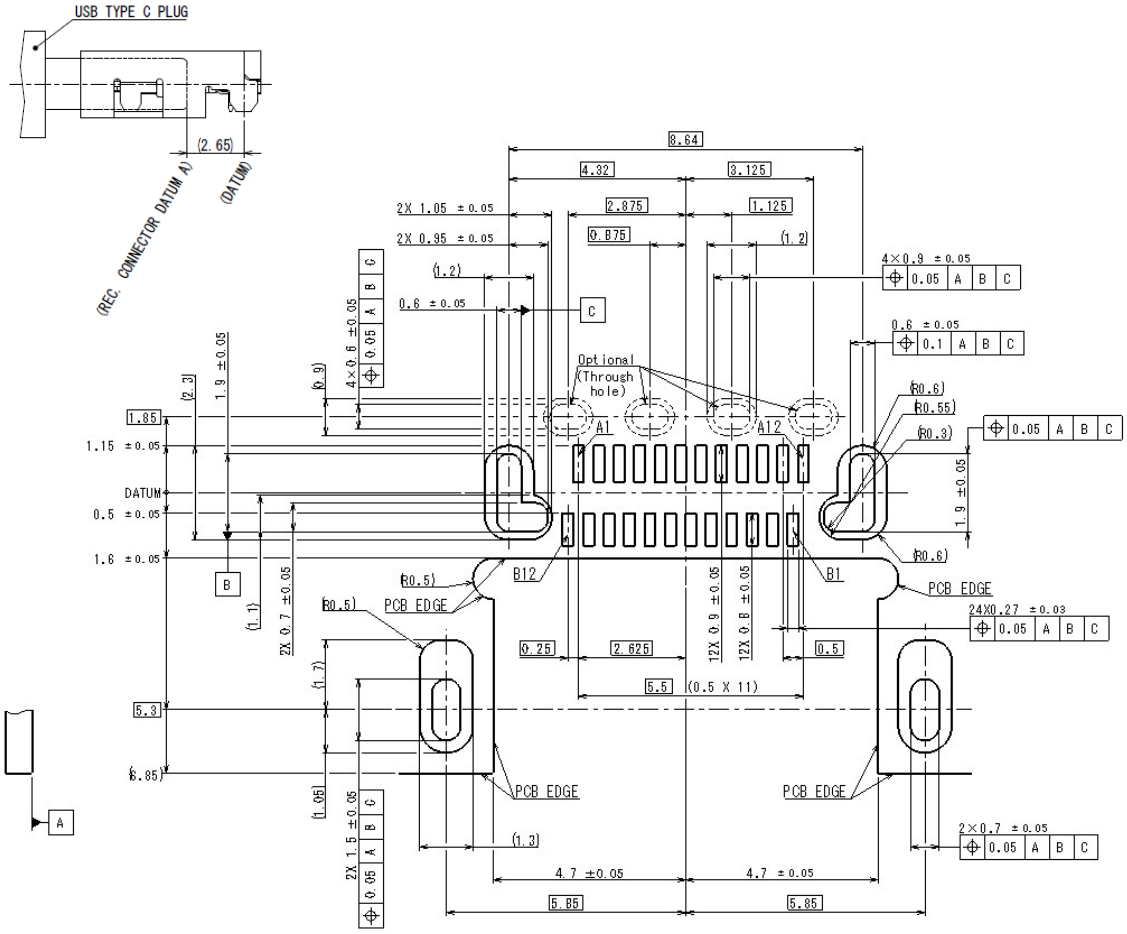
(Informative)



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

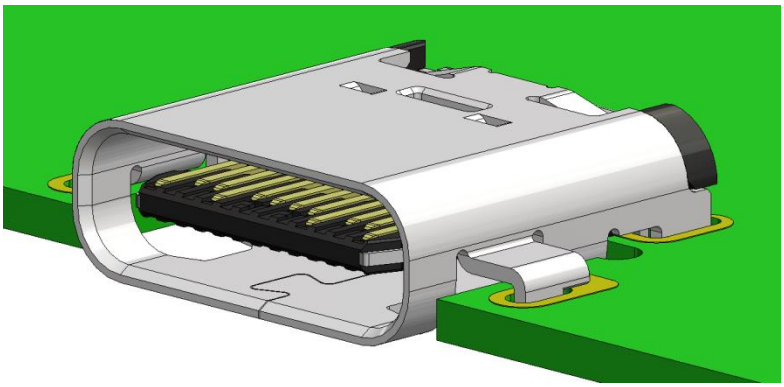
Figure 3-7 Reference Footprint for a USB Type-C Mid-Mount Dual-Row SMT Receptacle (Informative)

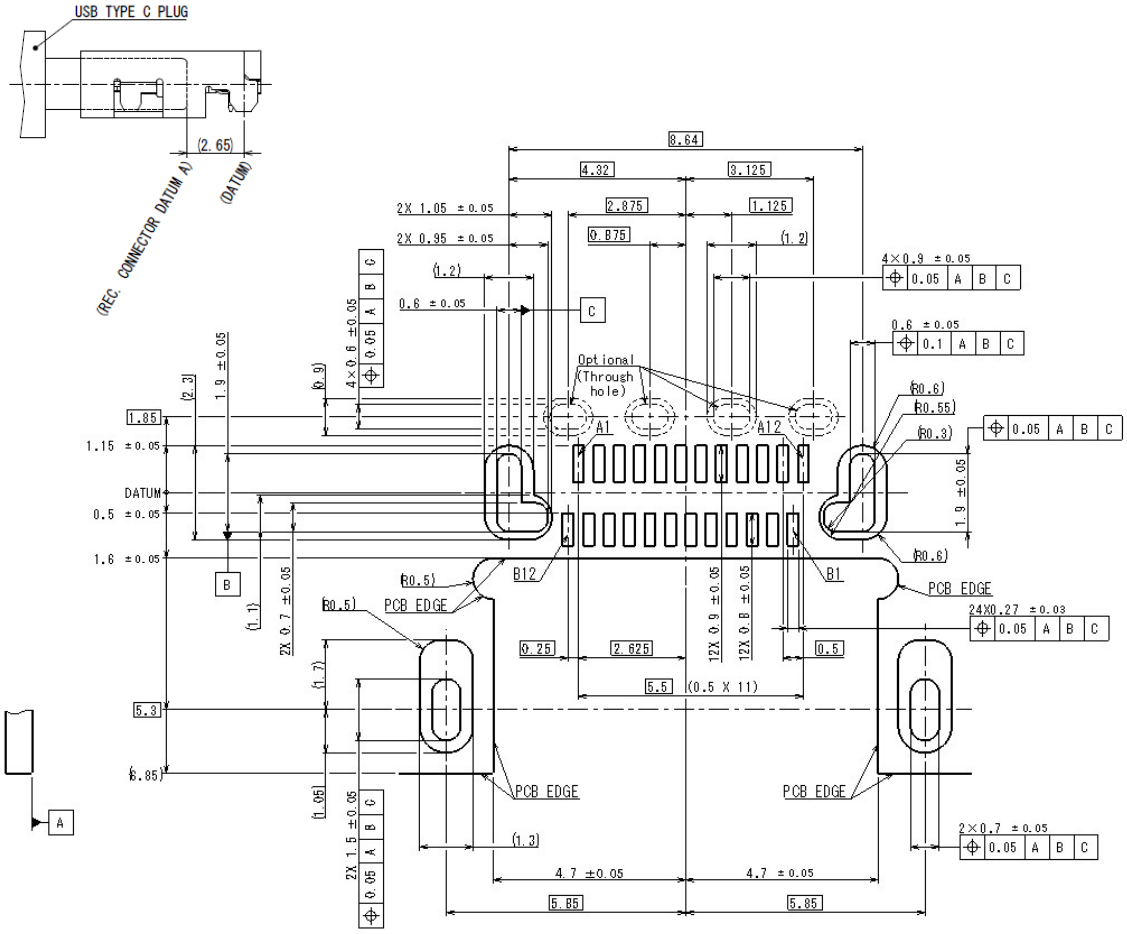




Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

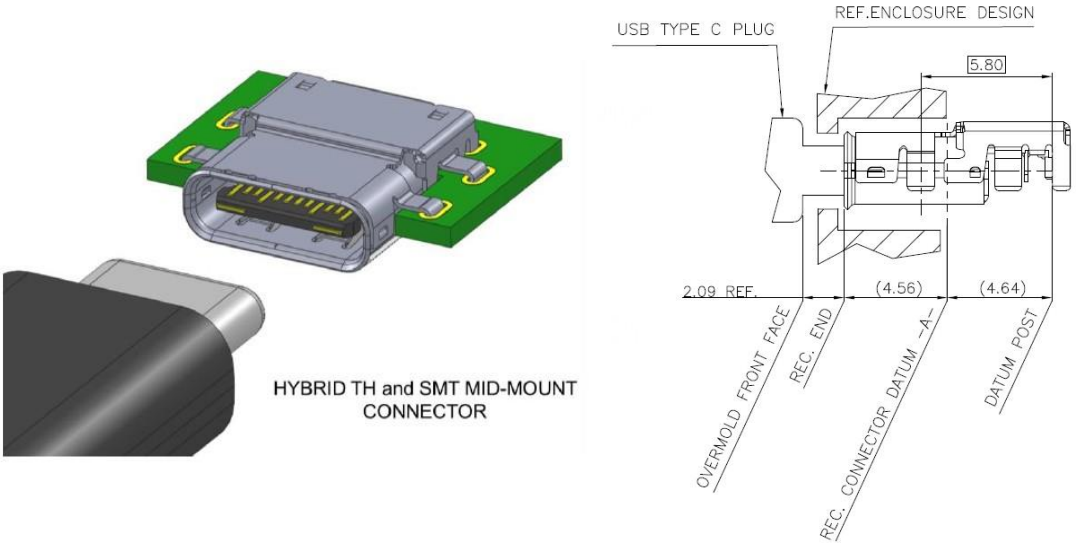
图 3-7 USB Type-C 中置双排 SMT 插座参考封装（参考）

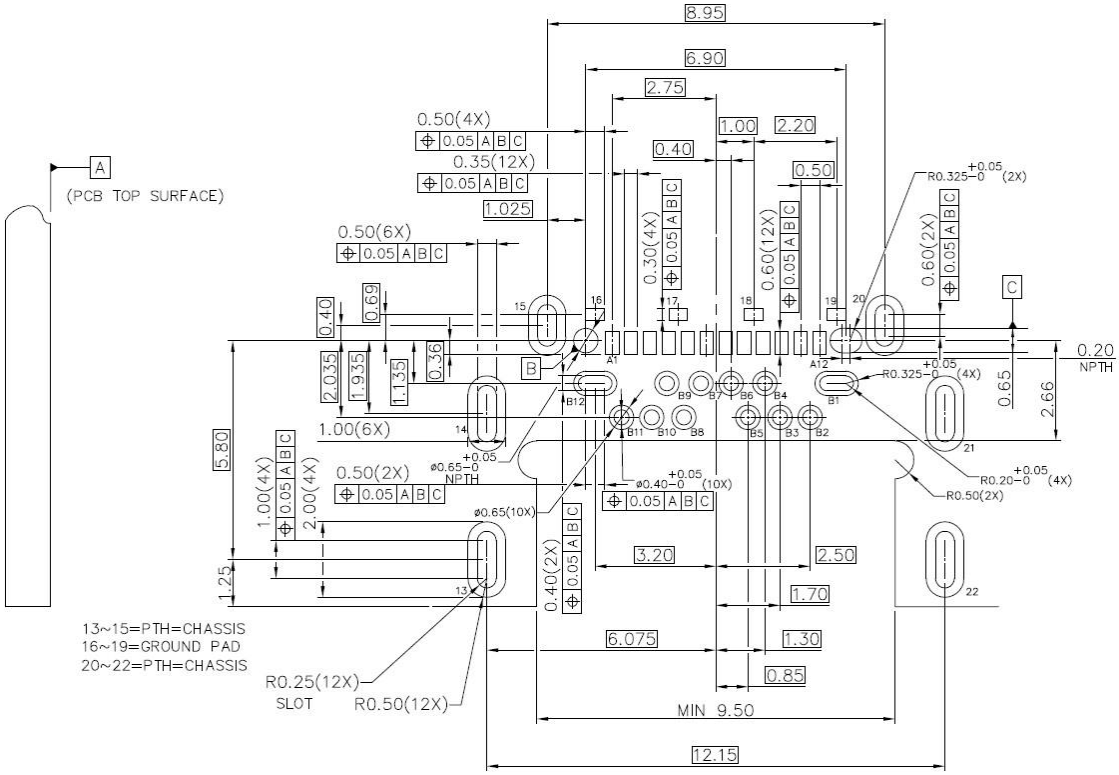




Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

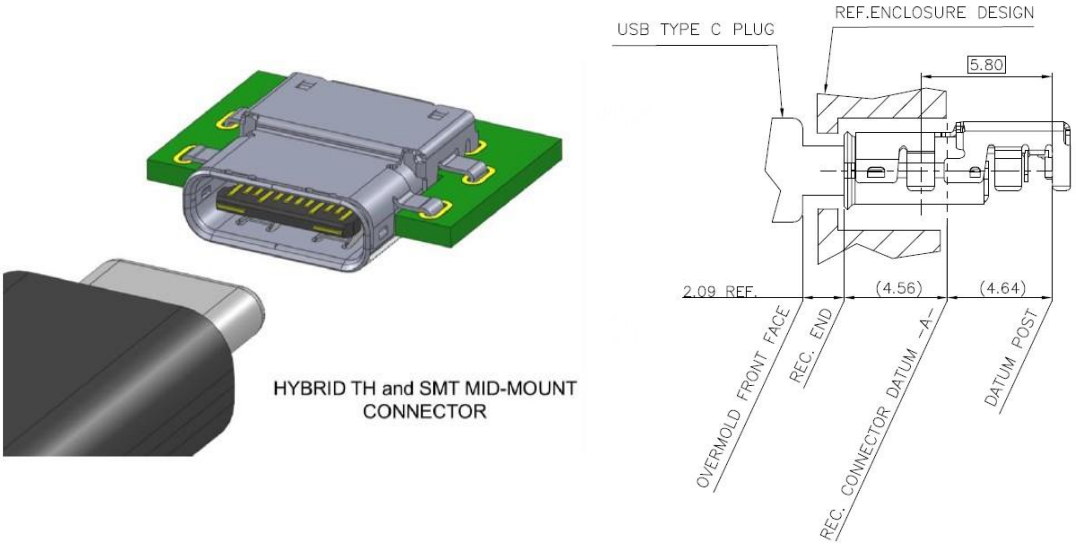
Figure 3-8 Reference Footprint for a USB Type-C Mid-Mount Hybrid Receptacle (Informative)

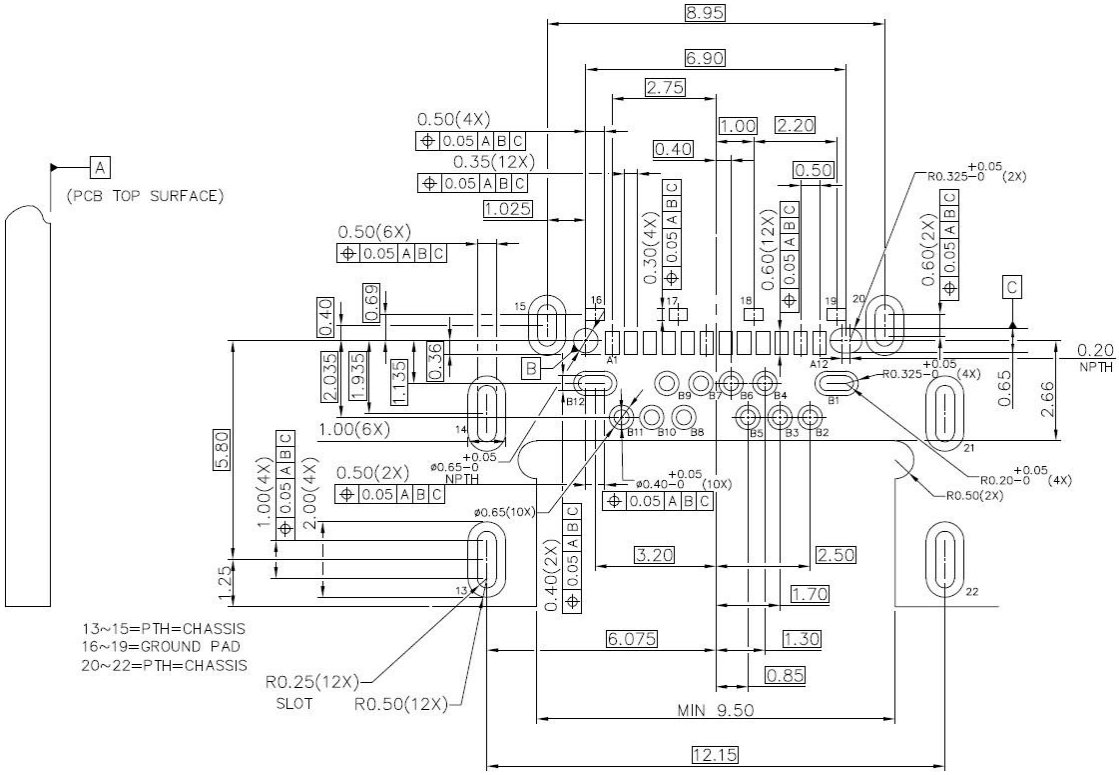




Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

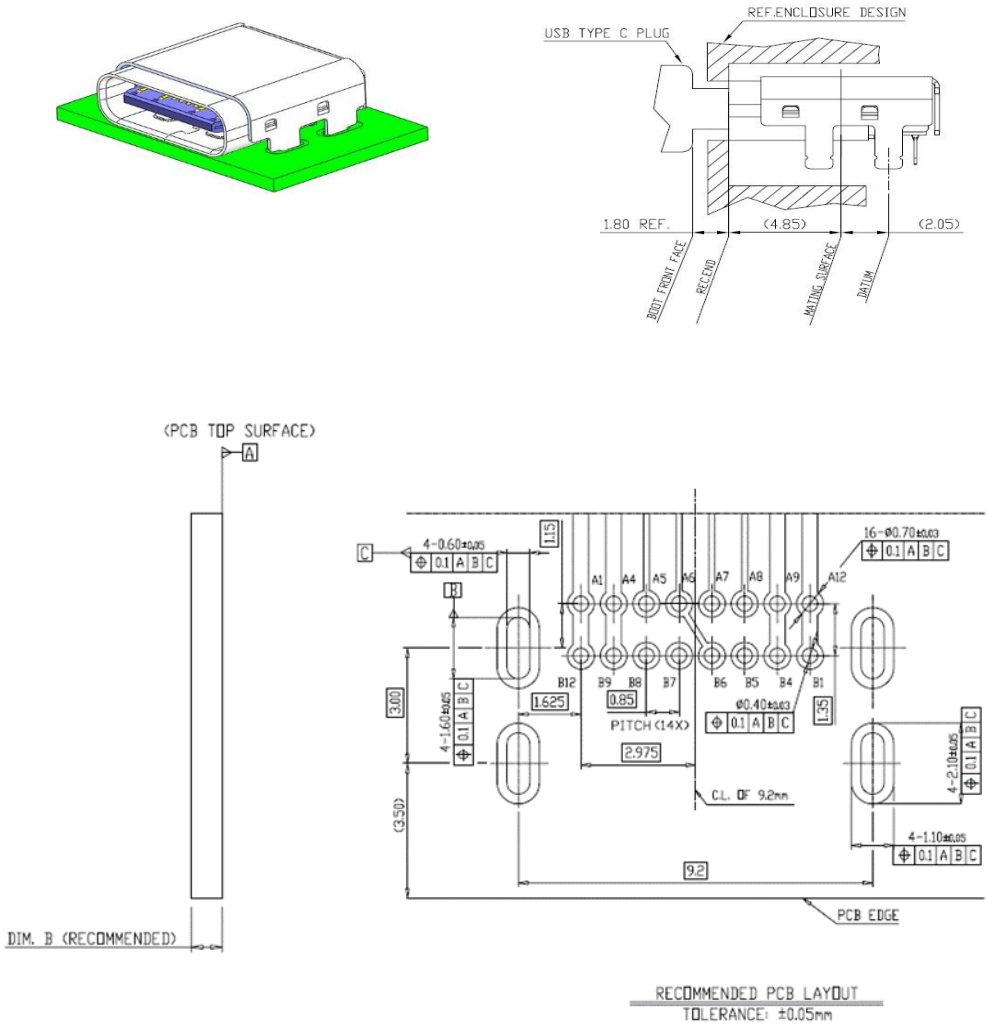
Figure 3-8 Reference Footprint for a USB Type-C Mid-Mount Hybrid Receptacle (Informative)





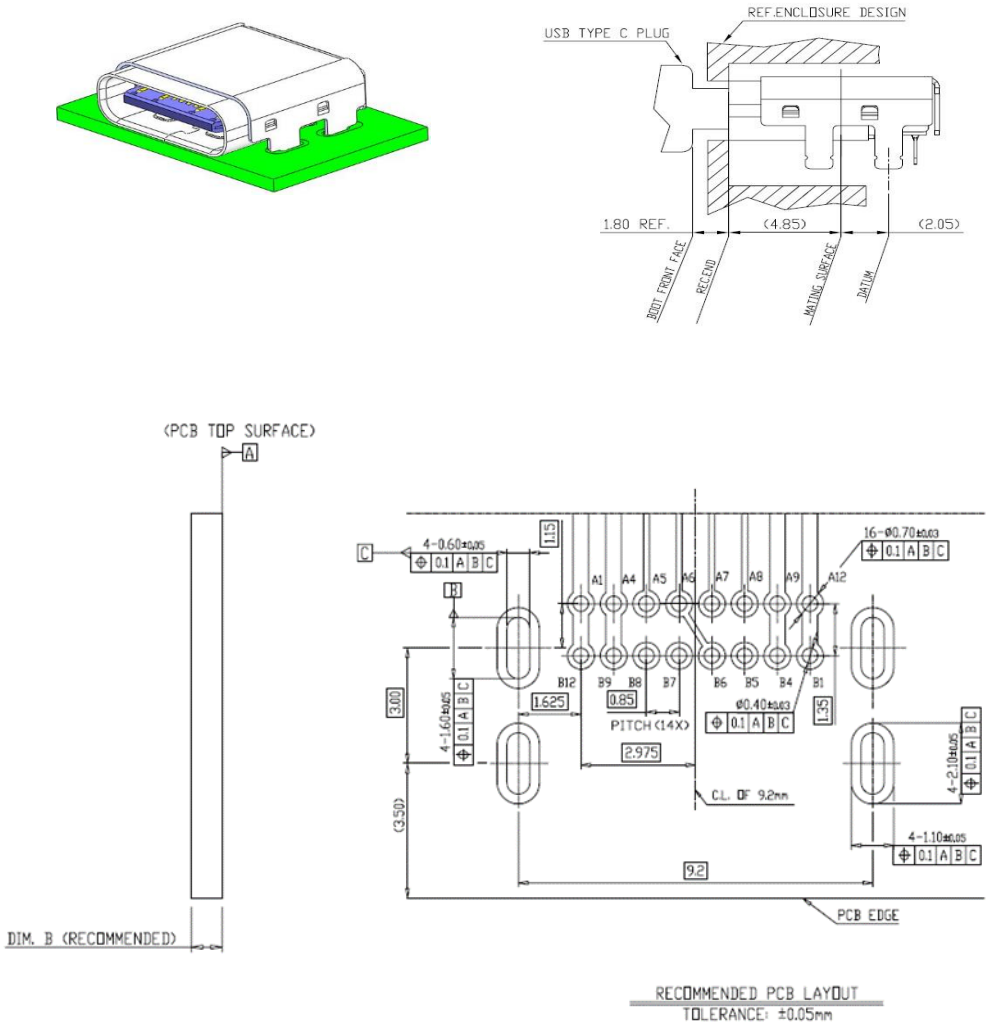
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-9 Reference Footprint for a USB 2.0 Type-C Through Hole Right Angle Receptacle (Informative)



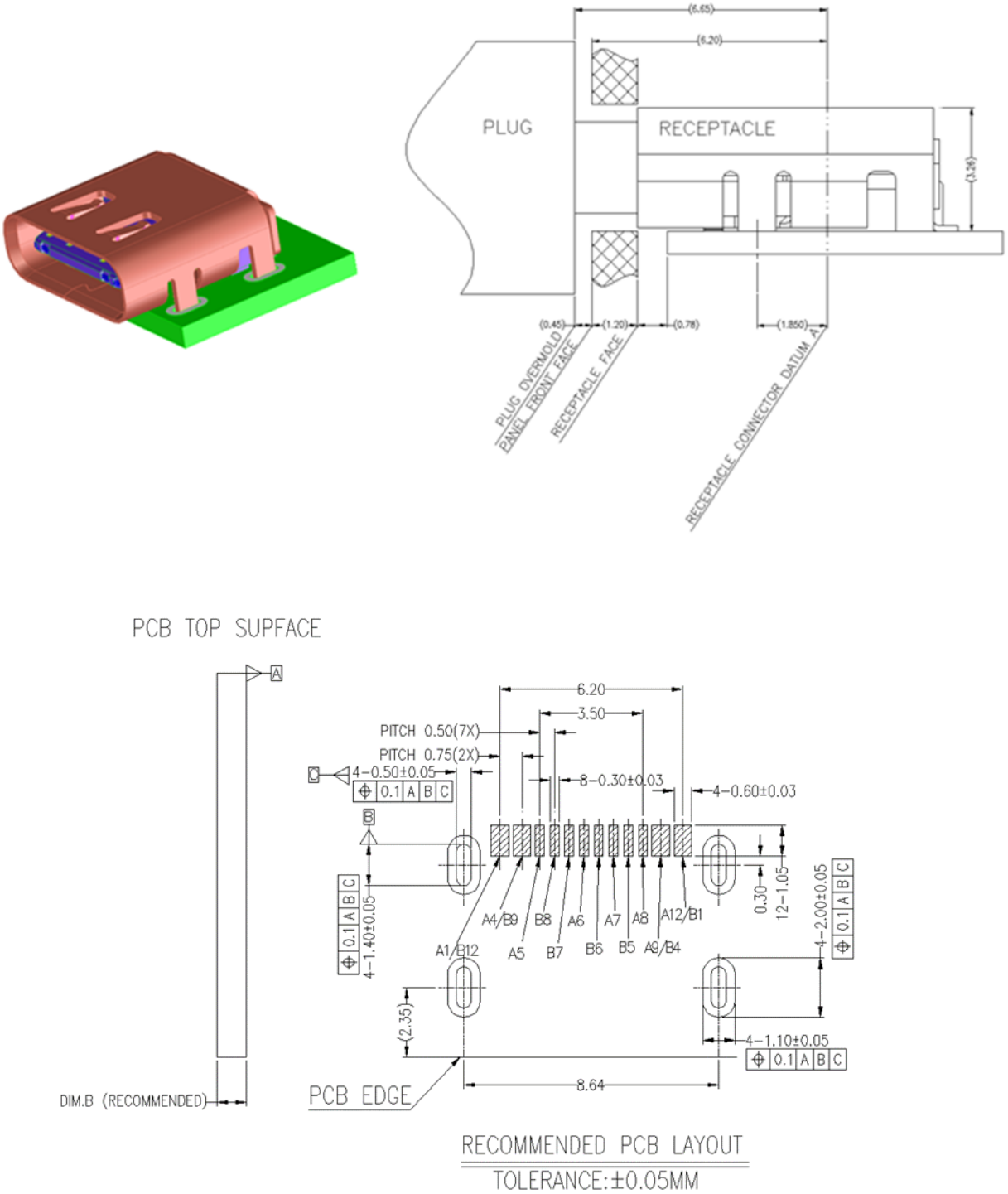
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-9 USB 2.0 Type-C 通孔直角插座的参考封装（参考）



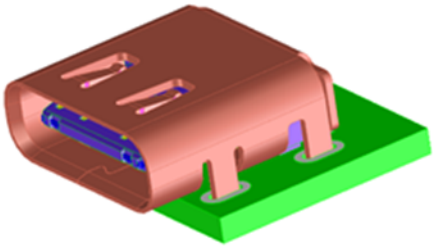
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

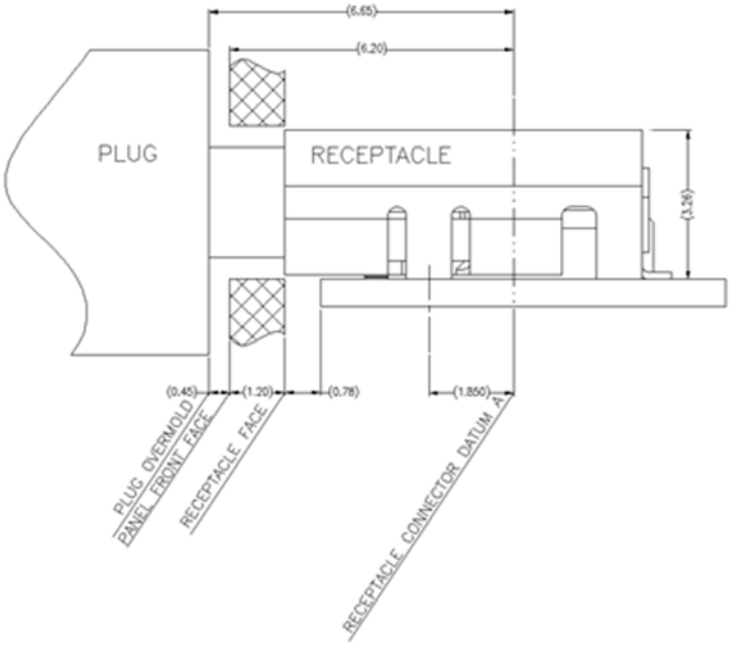
Figure 3-10 Reference Footprint for a USB 2.0 Type-C Single Row Right Angle Receptacle (Informative)

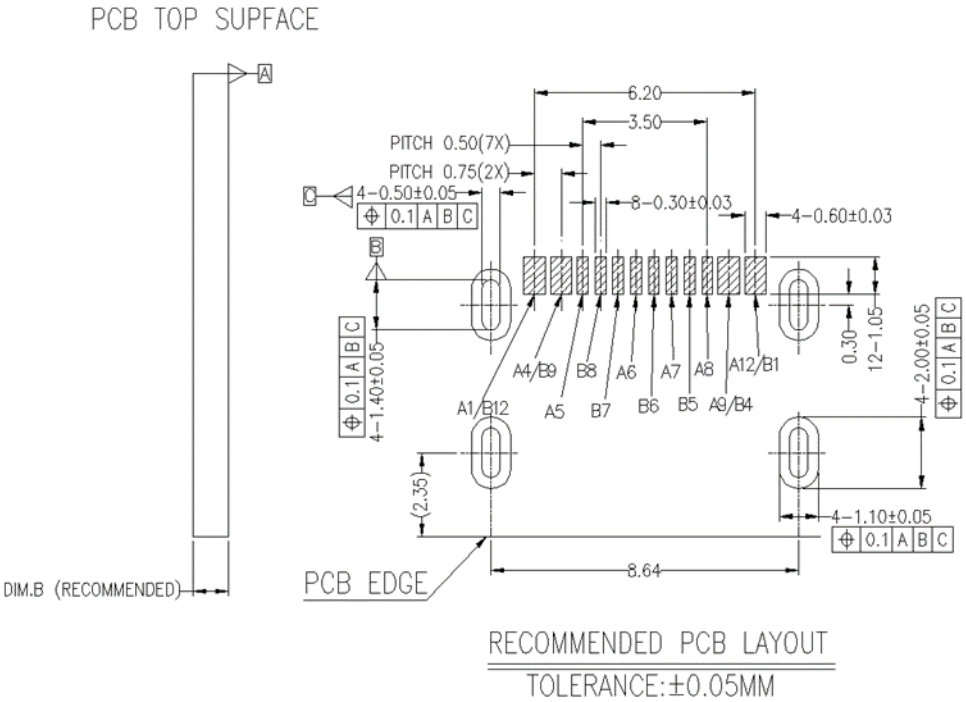


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-10 USB 2.0 Type-C 单排直角插座的参考封装（参考资料）







Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

This specification requires that all contacts be present in the mating interface of the USB Full-Featured Type-C receptacle connector and all contacts except the *USB 3.2* or *USB4* signals (i.e., A2, A3, A10, A11, B2, B3, B10 and B11) be present in the mating interface of the *USB 2.0* Type-C receptacle connector, but allows the plug to include only the contacts required for *USB PD* and *USB 2.0* functionality for applications that only support *USB 2.0*. The *USB 2.0* Type-C plug is shown in Figure 3-11. The following design simplifications may be made when only *USB 2.0* is supported:

- Only the contacts necessary to support *USB PD* and *USB 2.0* are required in the plug. All other pin locations may be unpopulated. See Table 3-5. All contacts are required to be present in the mating interface of the USB Type-C receptacle connector.
- Unlike the USB Full-Featured Type-C plug, the internal EMC springs may be formed from the same strip as the signal, power, and ground contacts. The internal EMC springs contact the inner surface of the plug shell and mate with the receptacle EMC pads when the plug is seated in the receptacle. Alternately, the *USB 2.0* Type-C plug may use the same EMC spring configuration as defined for the USB Full-Featured Type-C plug. The *USB 2.0* Type-C plug four EMC spring locations are defined in Figure 3-11. The alternate configuration using the six spring locations is defined in Figure 3-1. Also refer to the reference designs in 3.2.2.3 for further clarification.
- A paddle card inside the plug may not be necessary if wires are directly attached to the contact pins.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

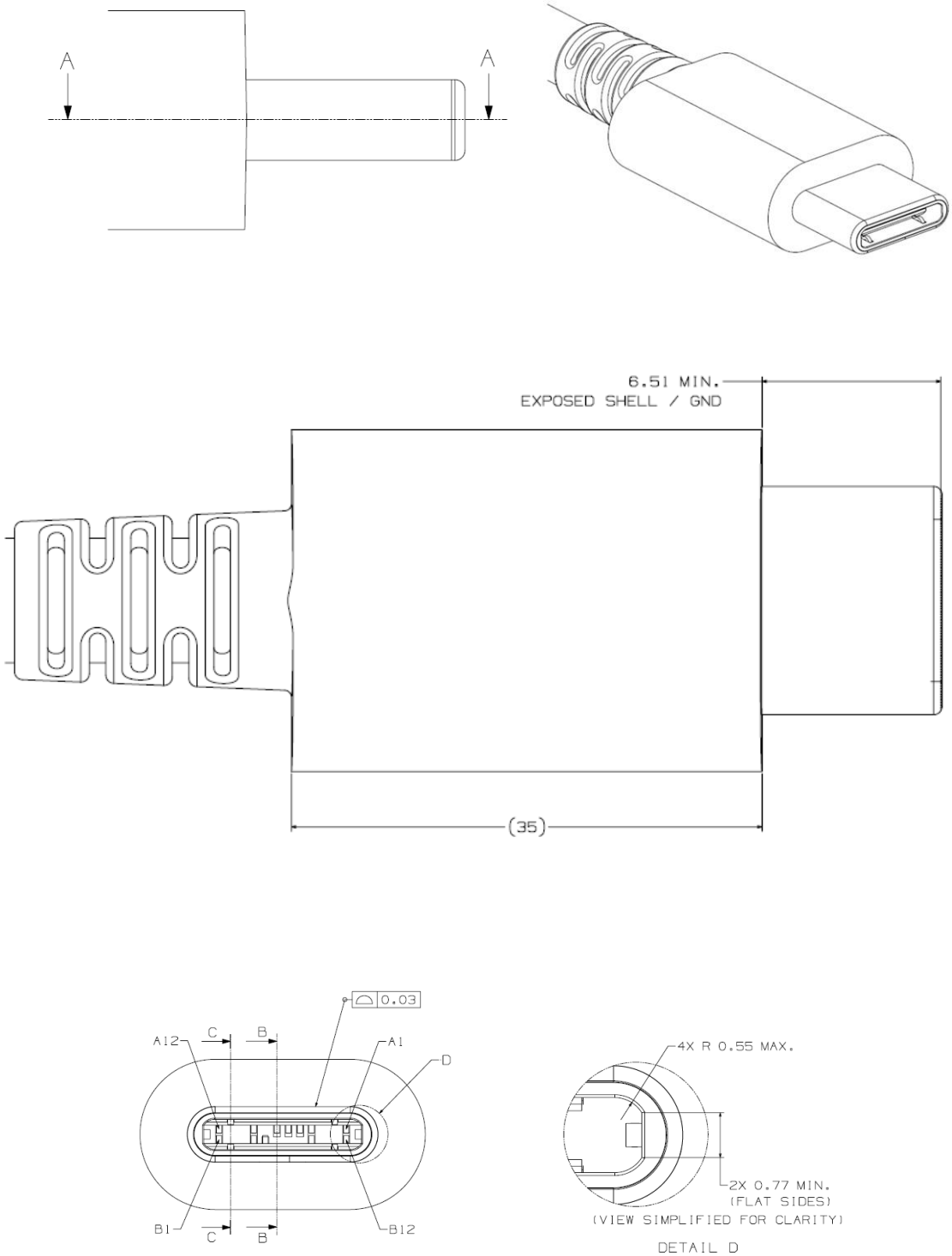
本规范要求所有触点均存在于 USB 全功能 Type-C 插座连接器的配接接口中，除 *USB 3.2* 或 *USB4* 信号（即 A2、A3、A10、A11、B2、B3、B10 和 B11）之外的所有触点均存在于 *USB 2.0* Type-C 插座连接器的配接接口中，但对于仅支持 *USB 2.0* 的应用，允许插头仅包含 *USB PD* 和 *USB 2.0* 功能所需的触点。*USB 2.0* Type-C 插头如图 3-11 所示。当仅支持 *USB 2.0* 时，可以进行以下设计简化：

- 插头中仅需要支持 *USB PD* 和 *USB 2.0* 所需的触点。所有其他引脚位置可以不填充。请参阅表 3-5。所有触点都是必需的

存在于 USB Type-C 插座连接器的配接接口中。• 与 USB 全功能 Type-C 插头不同，内部 EMC 弹簧可以由与信号、电源和接地触点相同的条带形成。当插头插入插座时，内部 EMC 弹簧接触插头外壳的内表面并与插座 EMC 垫配接。或者，*USB 2.0* Type-C 插头可以使用与 USB 全功能 Type-C 插头相同的 EMC 弹簧配置。*USB 2.0* Type-C 插头的四个 EMC 弹簧位置在图 3-11 中定义。使用六个弹簧位置的替代配置在图 3-1 中定义。另请参阅 3.2.2.3 中的参考设计以获得进一步的说明。• 如果电线直接连接到接触针，则插头内部的拨卡可能没有必要。

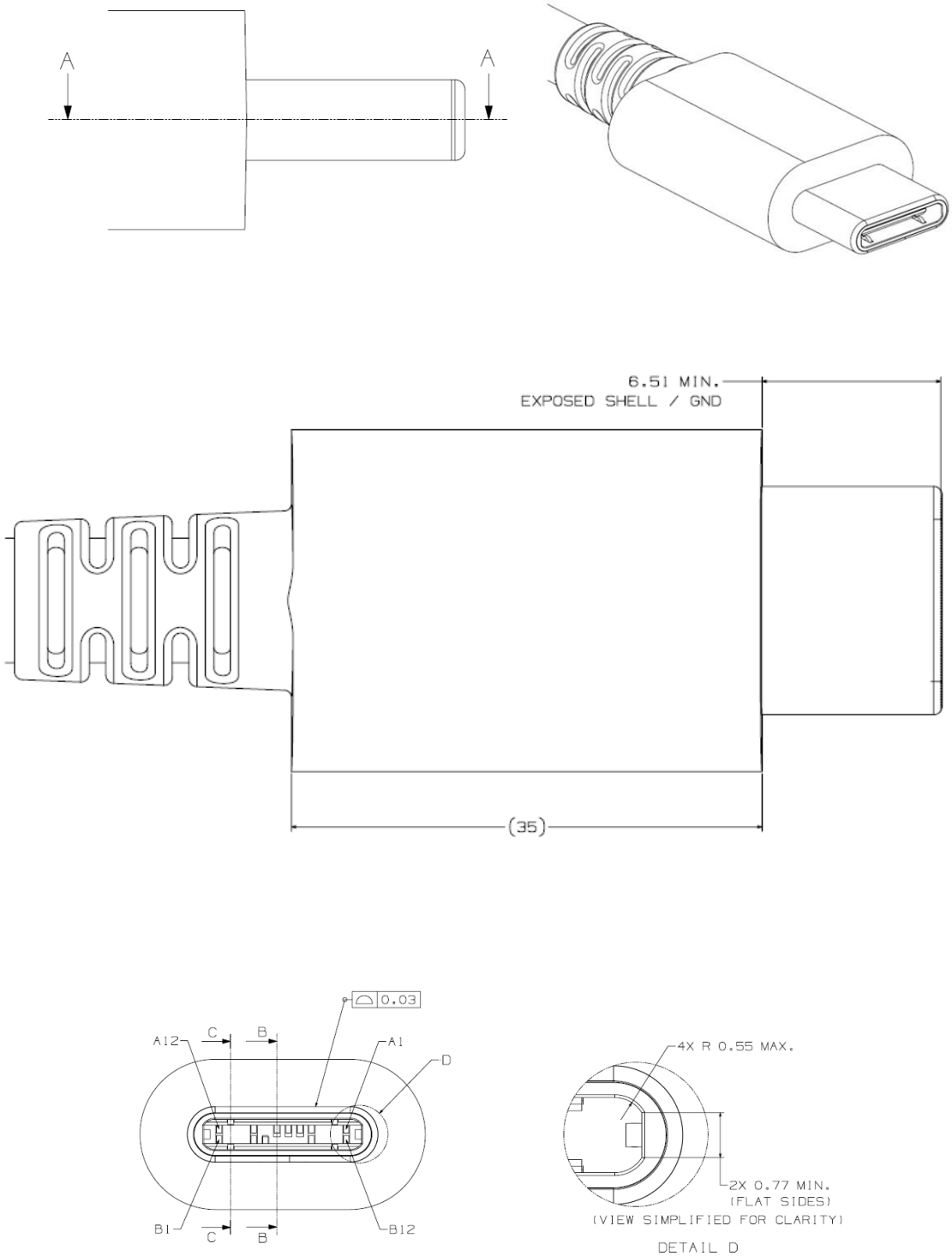
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-11 *USB 2.0* Type-C Plug Interface Dimensions



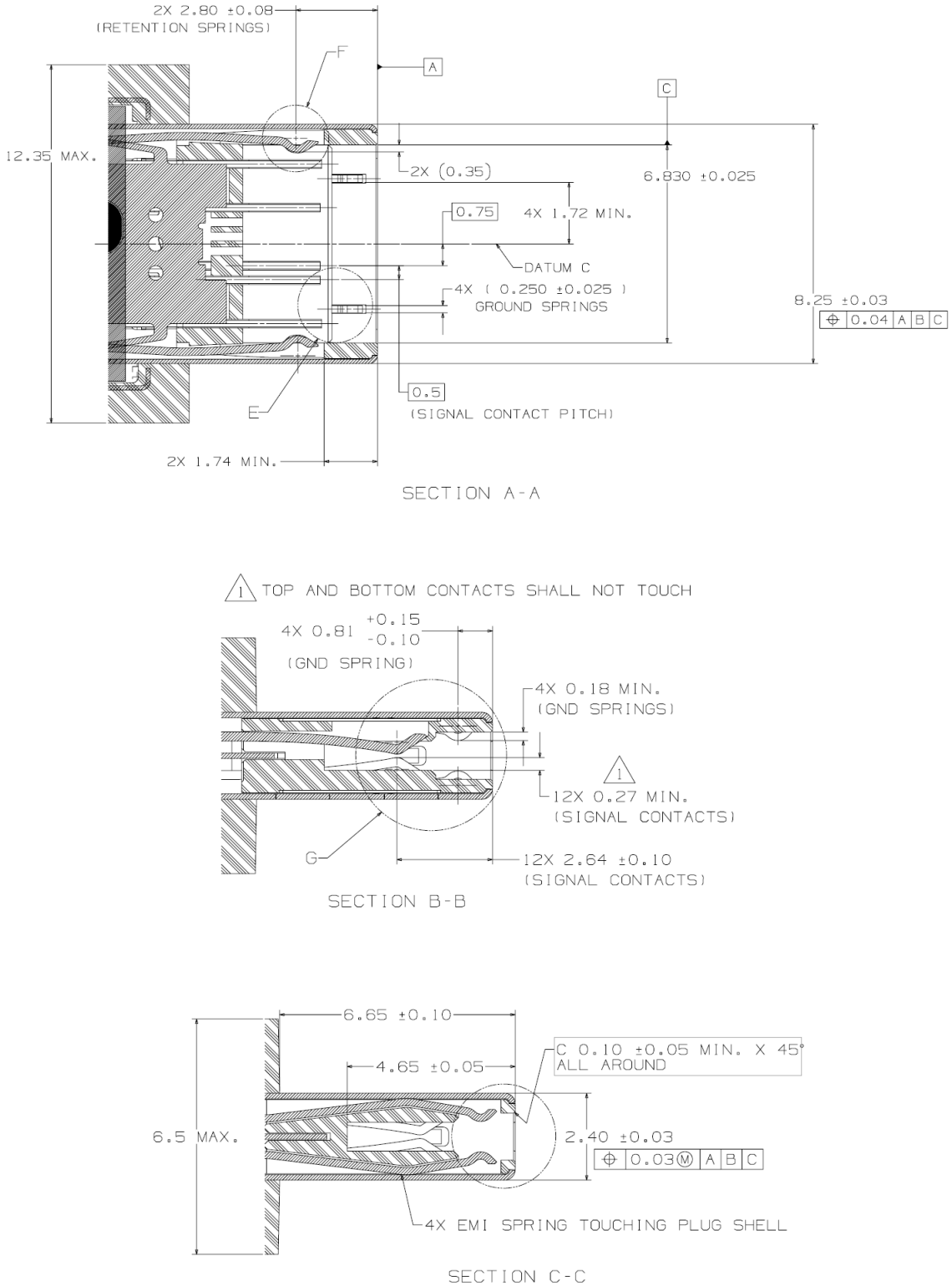
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-11 ***USB 2.0*** Type-C 插头接口尺寸



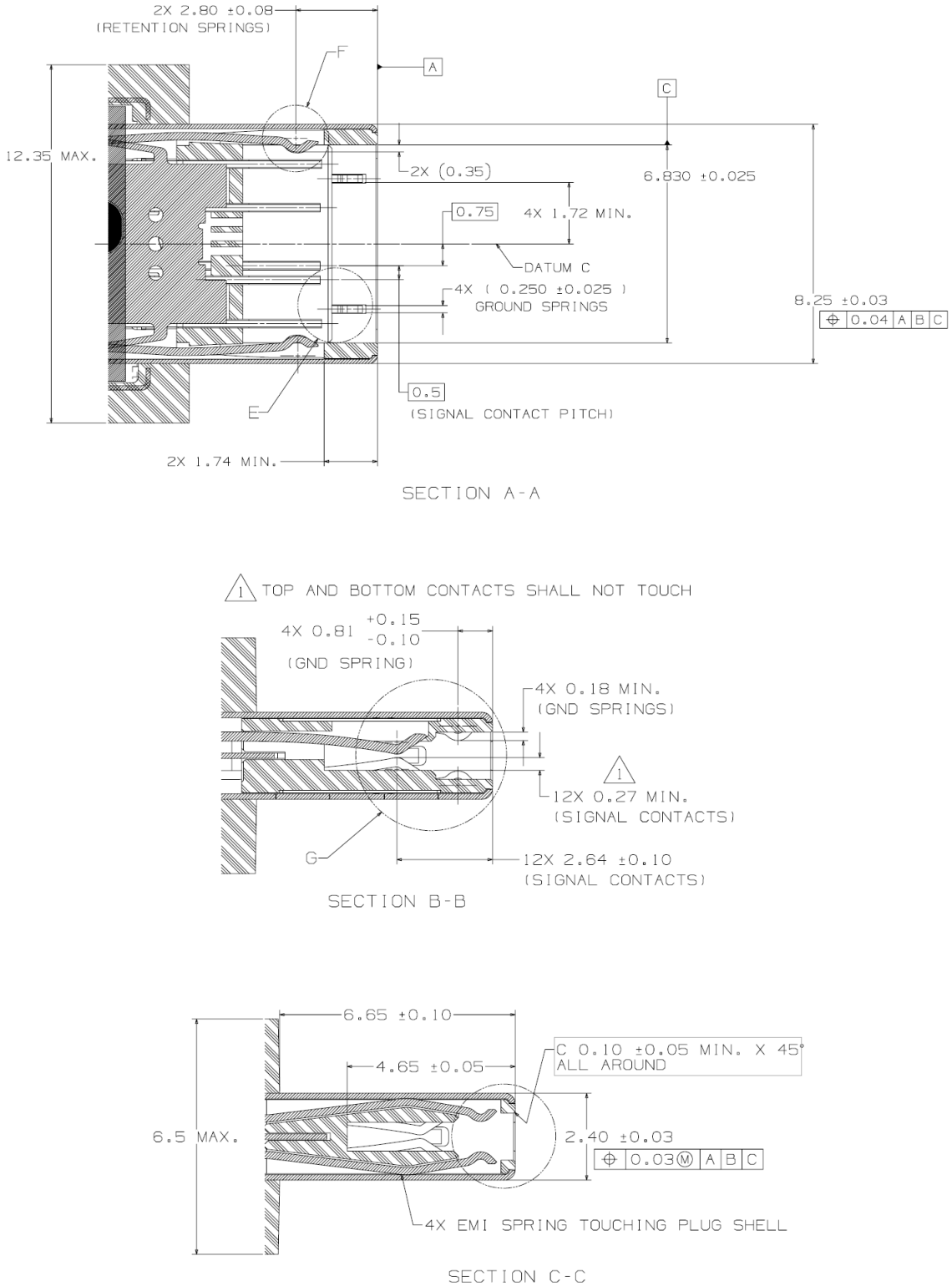
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-11 *USB 2.0* Type-C Plug Interface Dimensions, cont.



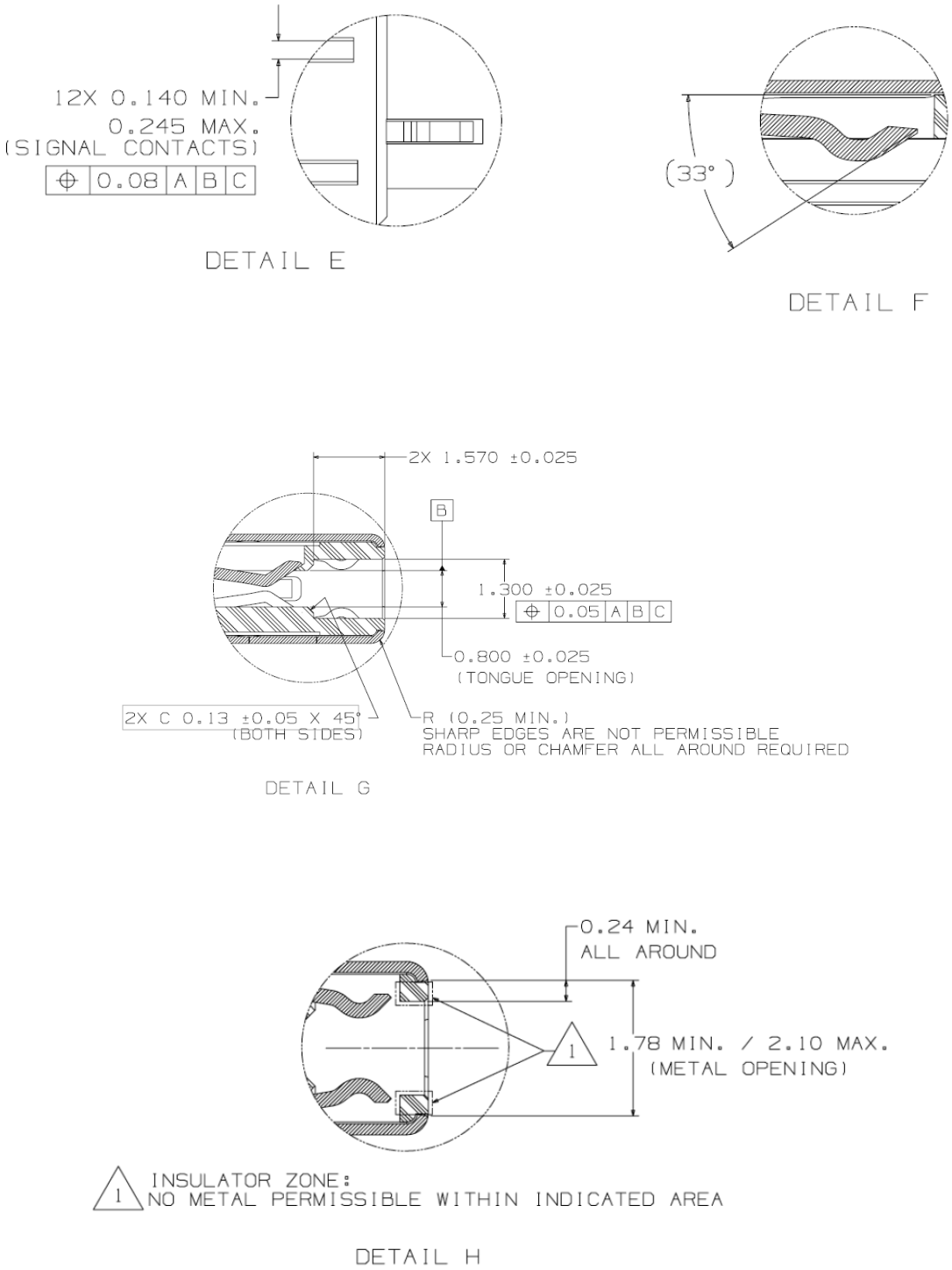
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-11 ***USB 2.0*** Type-C 插头接口尺寸（续）



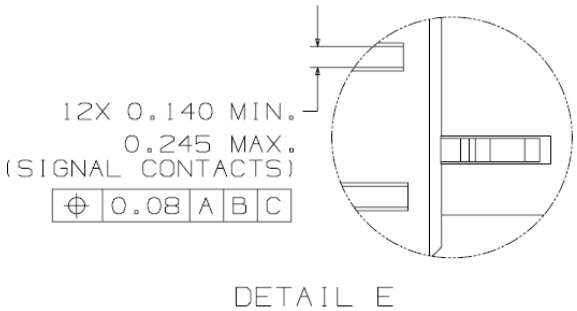
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

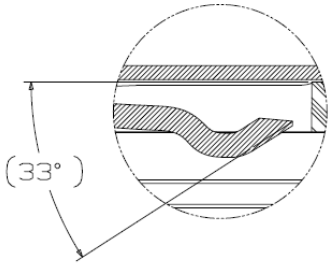
Figure 3-11 *USB 2.0* Type-C Plug Interface Dimensions, cont.

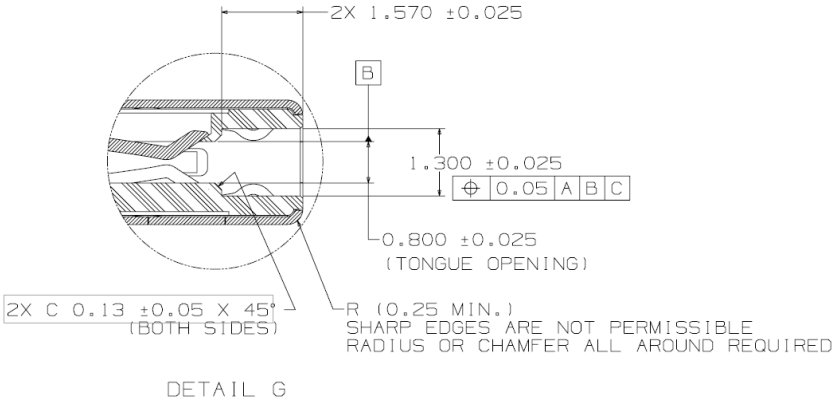


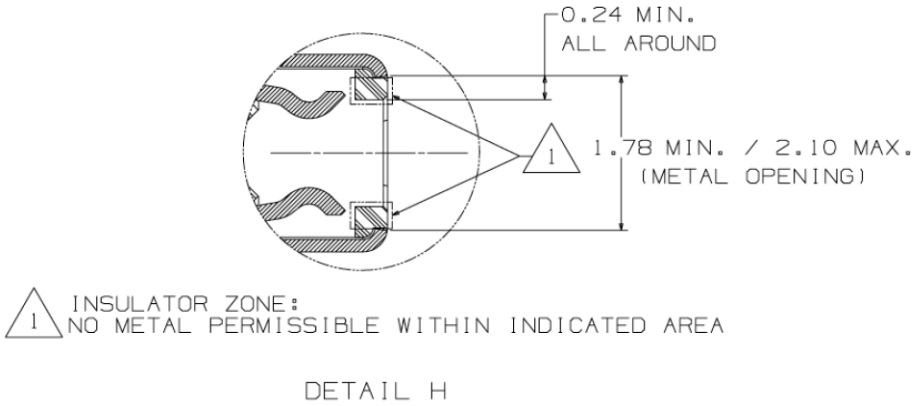
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-11 ***USB 2.0*** Type-C 插头接口尺寸（续）



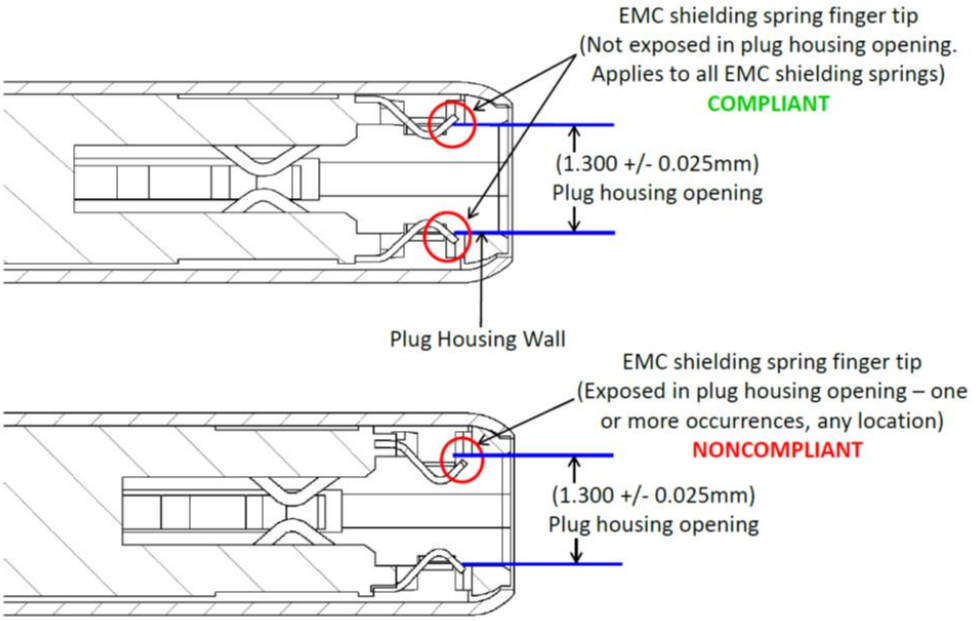






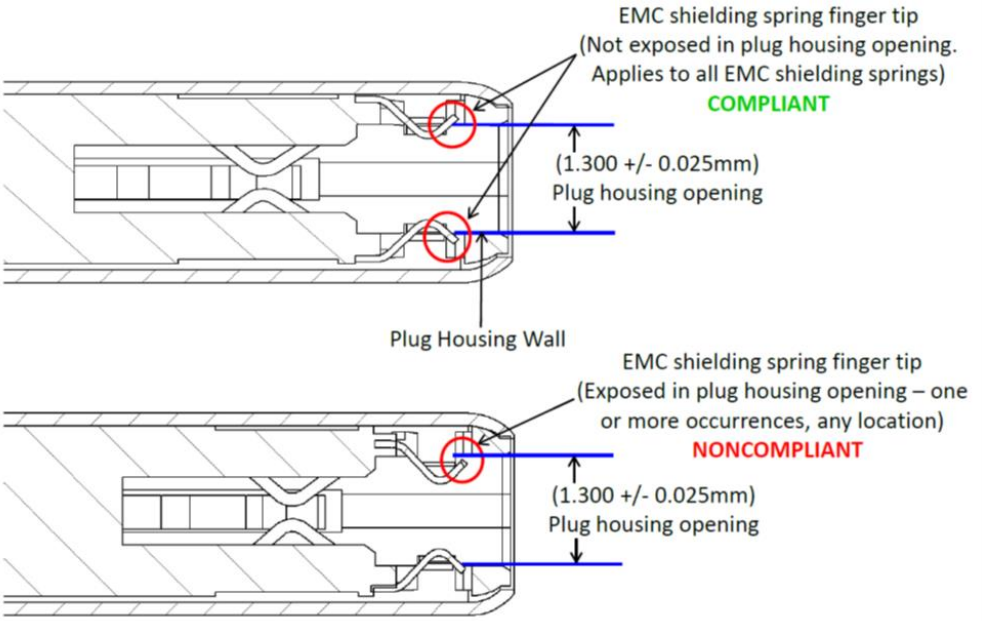
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-12 USB Type-C Plug EMC Shielding Spring Tip Requirements



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-12 USB Type-C 插头 EMC 屏蔽弹簧头要求



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.2.2 Reference Designs

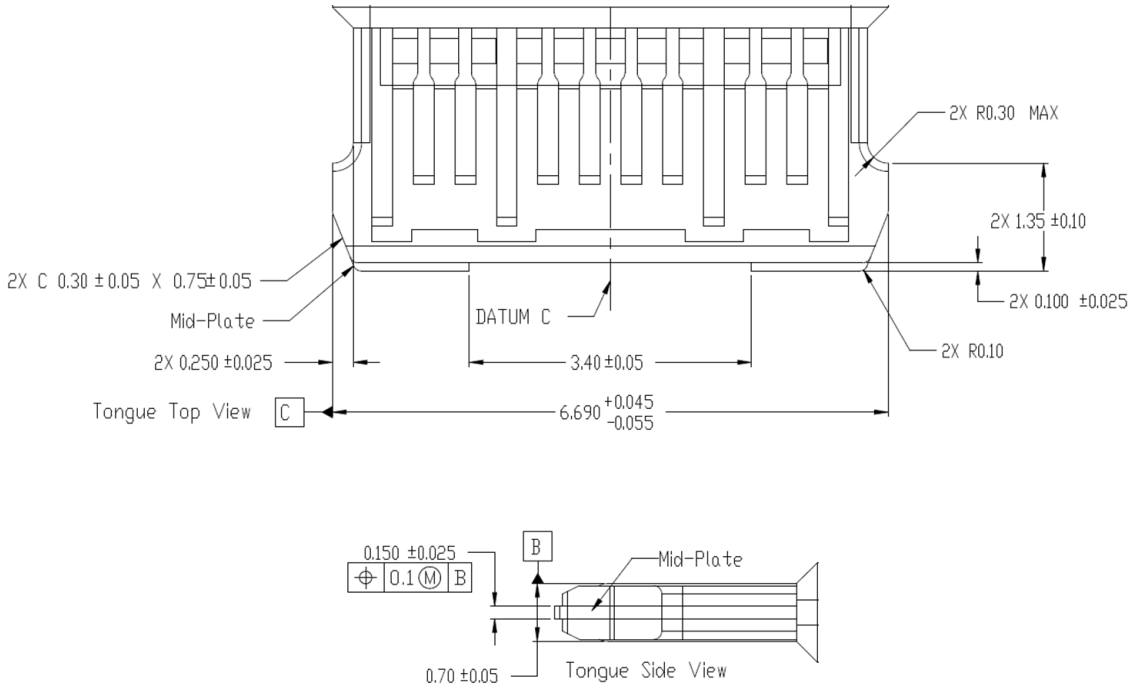
This section provides reference designs for a few key features of the USB Type-C connector. The reference designs are provided as acceptable design examples. They are not normative.

3.2.2.1 Receptacle Mid-Plate (Informative)

The signals between the top and bottom of the receptacle tongue are isolated by a mid-plate inside the tongue. Figure 3-13 shows a reference design of the mid-plate. It is important to pay attention to the following features of the middle plate:

- The distance between the signal contacts and the mid-plate should be accurately controlled since the variation of this distance may significantly impact impedance of the connector.
- The mid-plate in this particular design protrudes slightly beyond the front surface of the tongue. This is to protect the tongue front surface from damage caused by miss-insertion of small objects into the receptacle.
- The mid-plate is required to be directly connected to the PCB ground with at least two grounding points.
- The sides of the mid-plate mate with the plug side latches, making ground connections to reduce EMC. Proper surface finishes are necessary in the areas where the side latches and mid-plate connections occur.

Figure 3-13 Reference Design of Receptacle Mid-Plate



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.2.2 参考设计

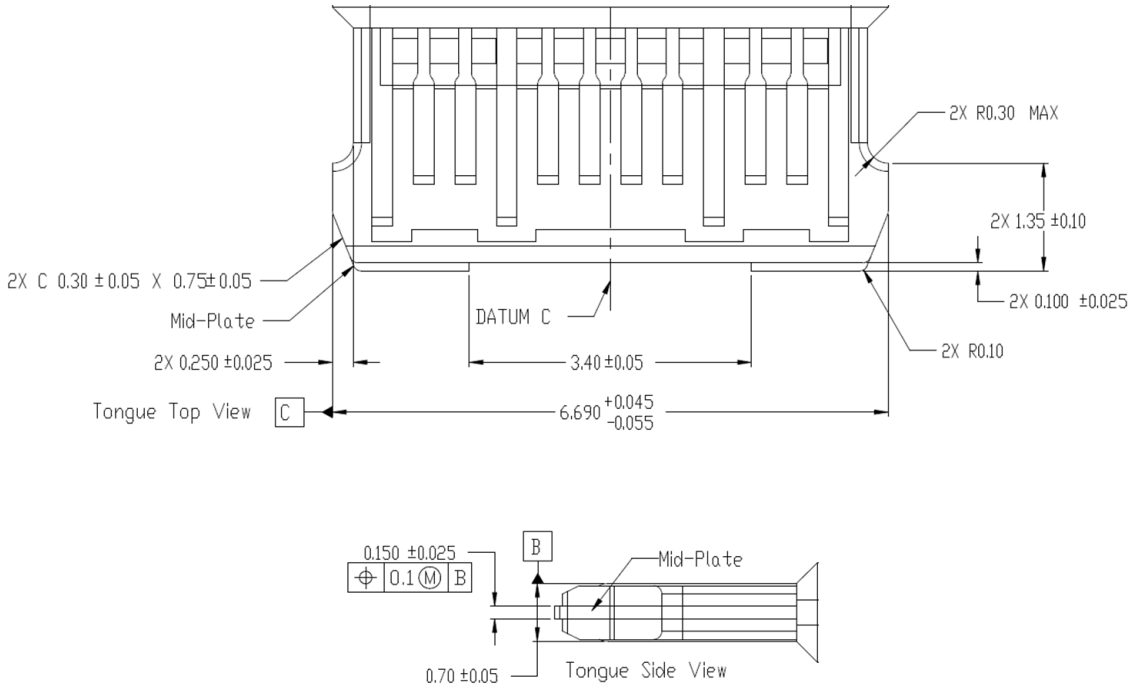
本节提供 USB Type-C 连接器几个关键功能的参考设计。参考设计作为可接受的设计示例提供。它们不是规范性的。

3.2.2.1 插座中板（参考资料）

插座舌片顶部和底部之间的信号通过舌片内部的中板隔离。图 3-13 显示了中板的参考设计。需要注意中板的以下特点：

- 应精确控制信号触点和中板之间的距离，因为此距离的变化可能会显著影响连接器的阻抗。
- 此特定设计中的中板略微突出于舌片的前表面。这是为了保护舌片前表面免受因小物体误插入插座而造成的损坏。
- 中板需要通过至少两个接地点直接连接到 PCB 接地。
- 中板的侧面与插头侧闩锁相配，形成接地连接以降低 EMC。在侧闩锁和中板连接的区域需要适当的表面处理。

图 3-13 插座中板参考设计



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.2.2.2 Side Latch (informative)

The side latches (retention latches) are located in the plug. Figure 3-14 shows a reference design of a blanked side latch. The plug side latches should contact the receptacle mid-plate to provide an additional ground return path.

Figure 3-14 Reference Design of the Retention Latch

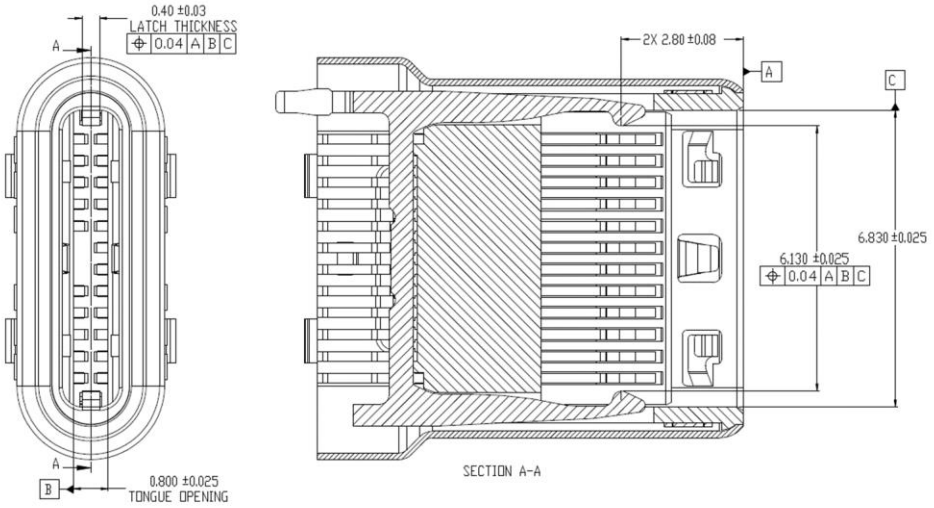
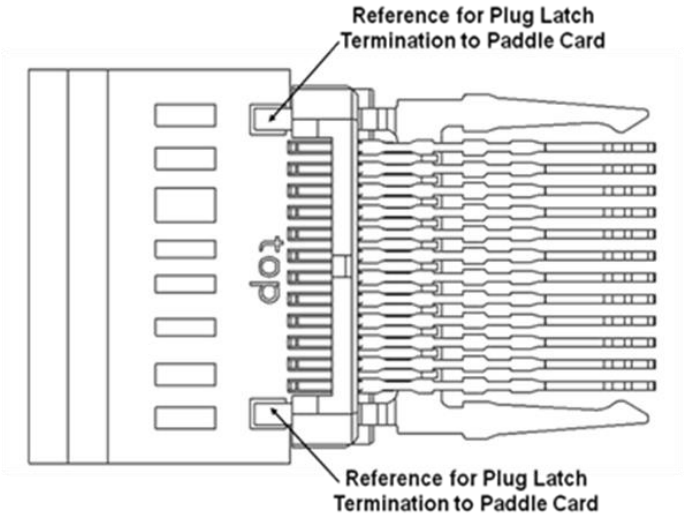


Figure 3-15 Illustration of the Latch Soldered to the Paddle Card Ground



3.2.2.3 Internal EMC Springs and Pads (Informative)

Figure 3-16 is a reference design of the internal EMC spring located inside the USB Full-Featured Type-C plug. Figure 3-17 is a reference design of the internal EMC spring located inside the *USB 2.0* Type-C plug.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.2.2.2 侧锁（参考资料）

侧闩锁（固定闩锁）位于插头中。图 3-14 显示了空白侧闩锁的参考设计。插头侧闩锁应接触插座中板，以提供额外的接地回路。

图 3-14 固定闩锁的参考设计

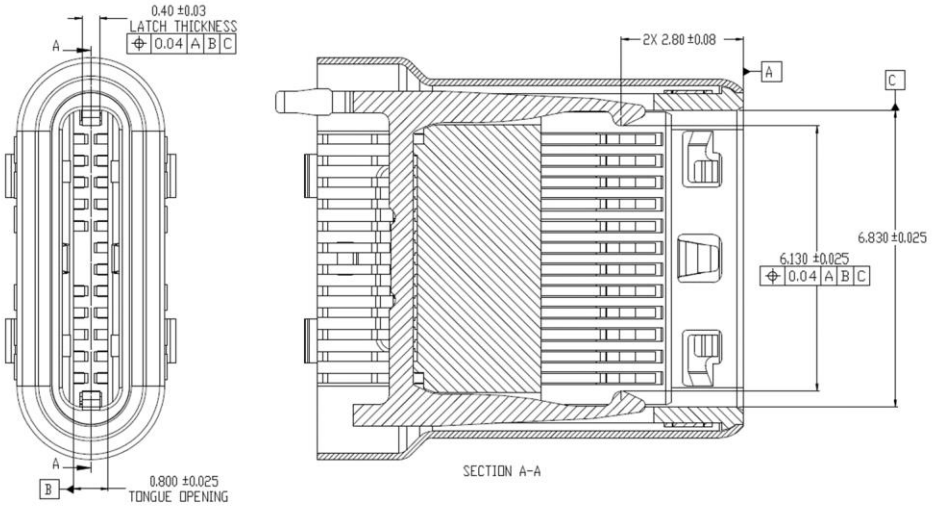
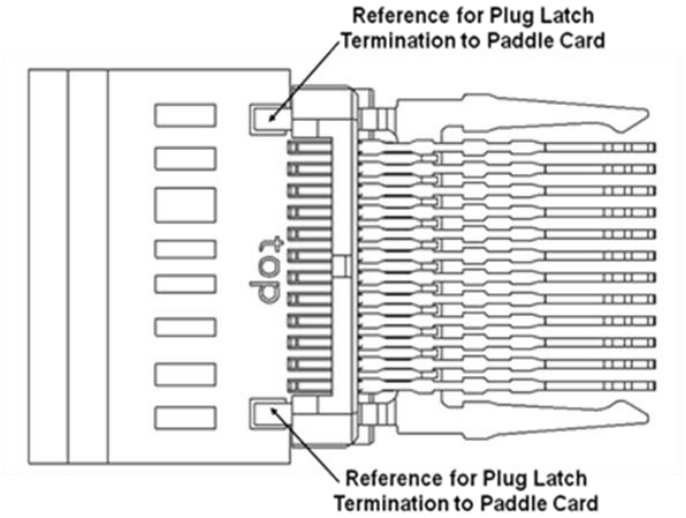


图 3-15 焊接至插卡接地的闩锁示意图

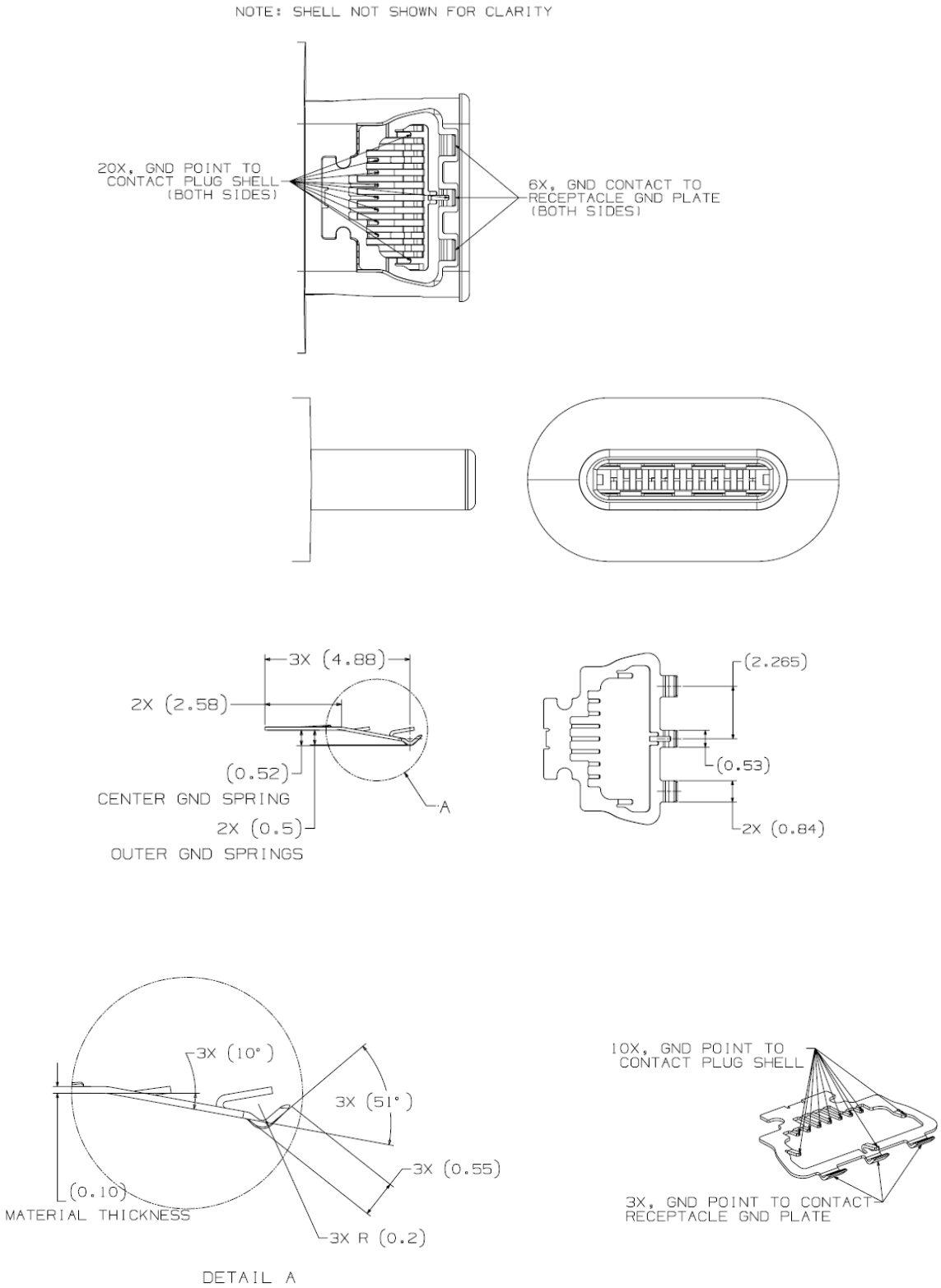


3.2.2.3 内部 EMC 弹簧和垫片（参考）

图 3-16 为 USB 全功能 Type-C 插头内部 EMC 弹簧的参考设计。图 3-17 为 *USB 2.0* Type-C 插头内部 EMC 弹簧的参考设计。

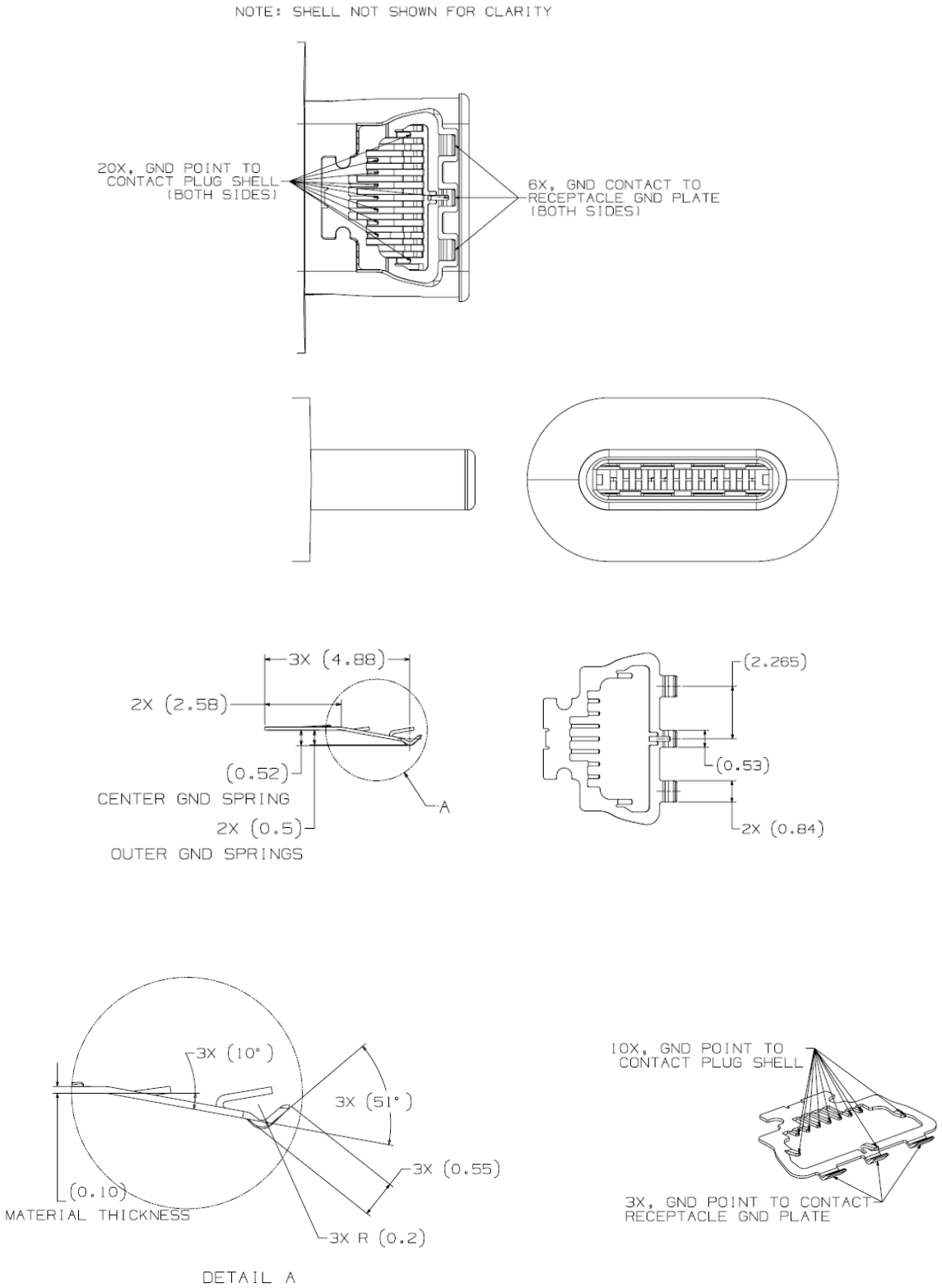
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-16 Reference Design of the USB Full-Featured Type-C Plug Internal EMC Spring



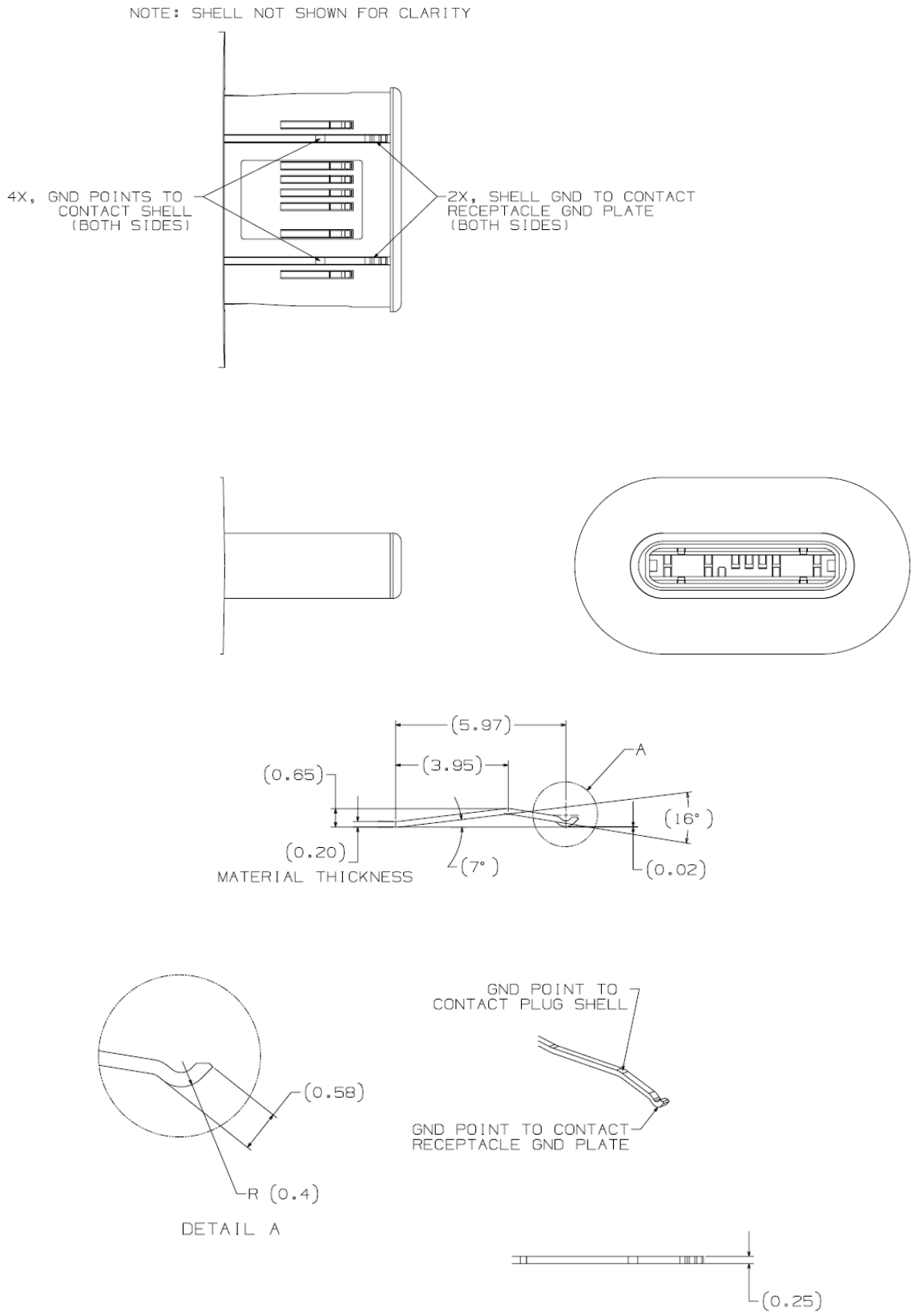
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-16 USB全功能Type-C插头内部EMC弹簧参考设计



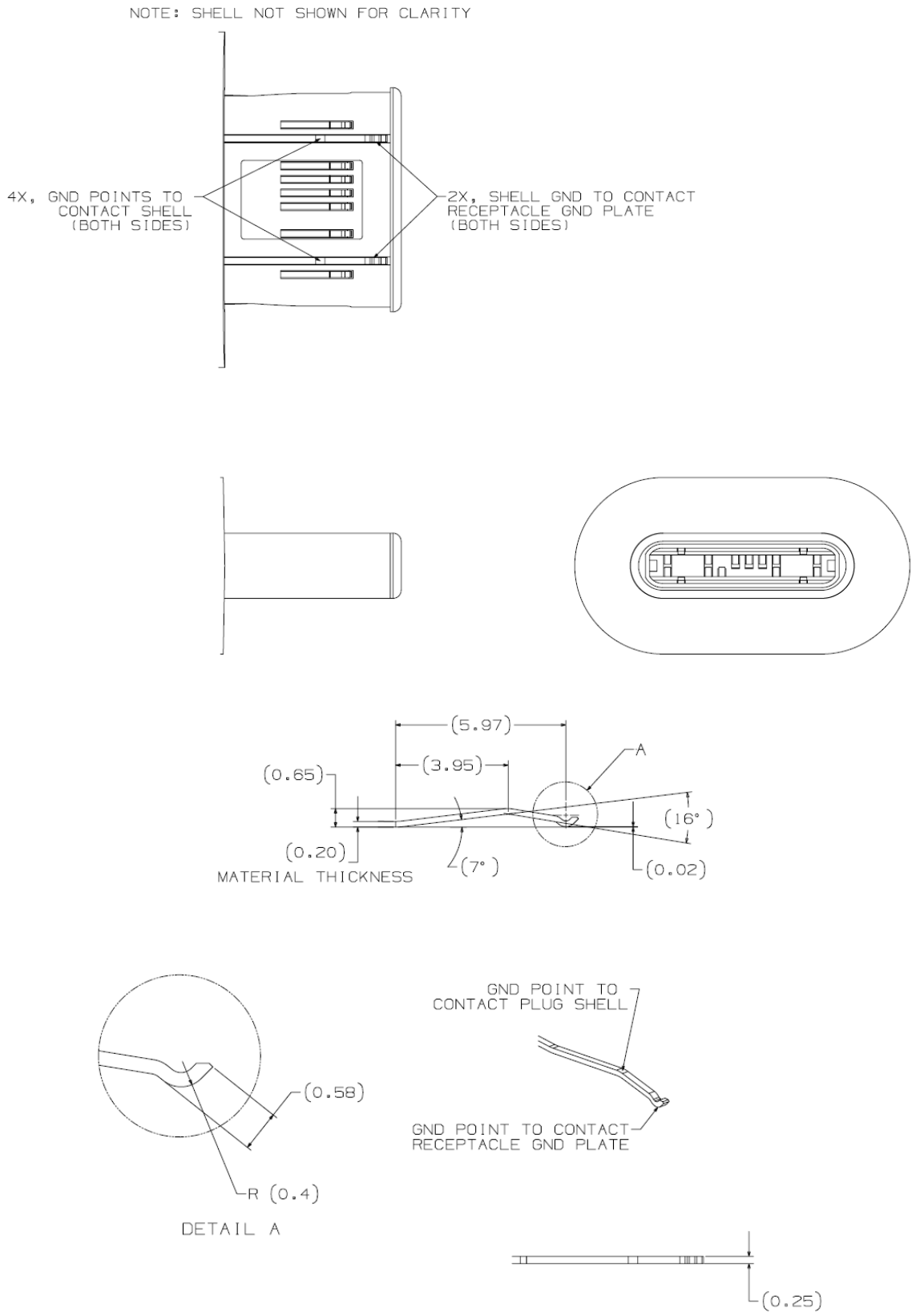
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-17 Reference Design of the *USB 2.0* Type-C Plug Internal EMC Spring



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-17 ***USB 2.0*** Type-C 插头内部 EMC 弹簧参考设计

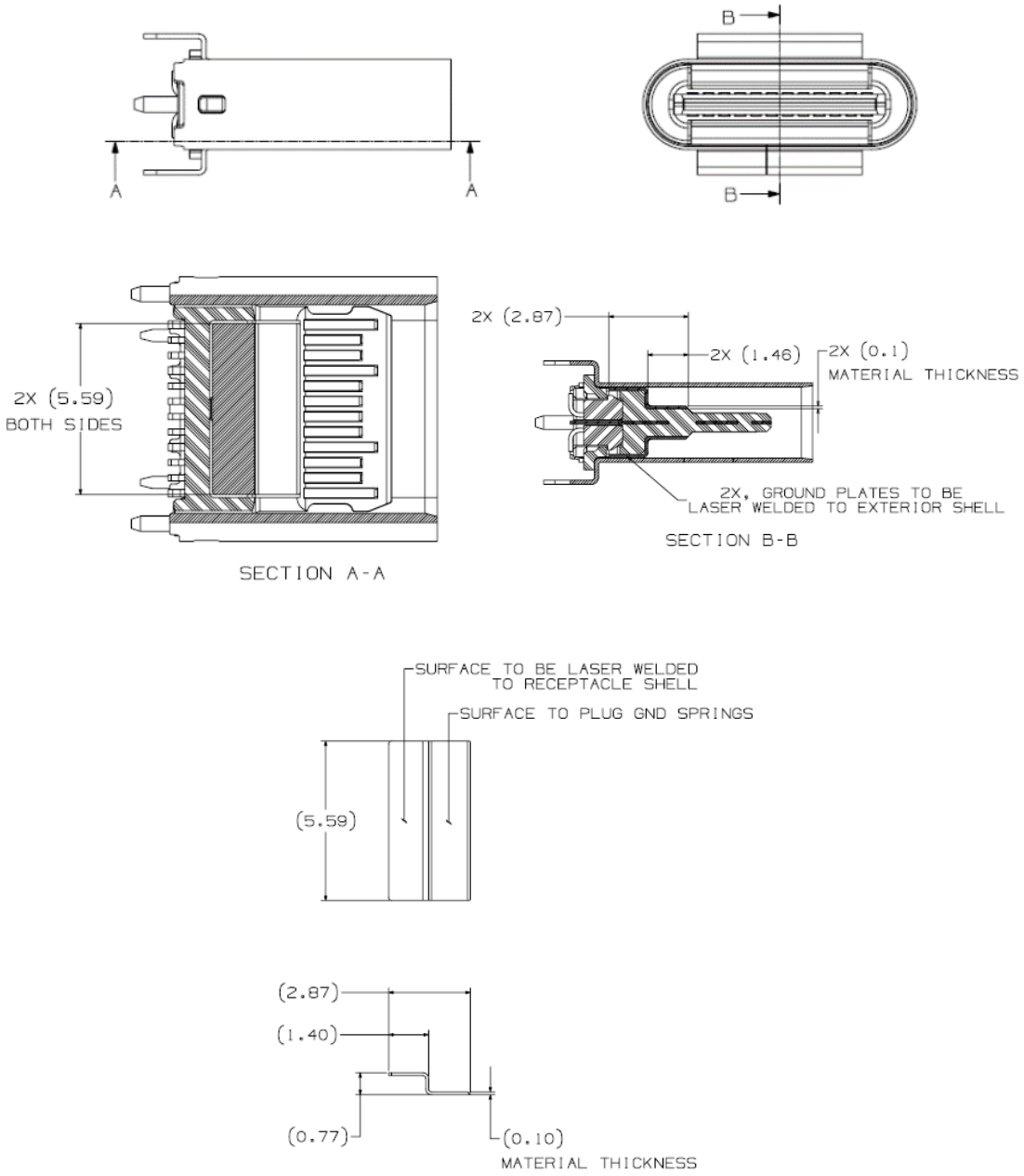


版权所有 © 2019 USB 3.0 Promoter Group。保留所有权利。

It is critical that the internal EMC spring contacts the plug shell as close to the EMC spring mating interface as possible to minimize the length of the return path.

The internal EMC pad (i.e., ground plate) shown in Figure 3-18 is inside the receptacle. It mates with the EMC spring in the plug. To provide an effective ground return, the EMC pads should have multiple connections with the receptacle shell.

Figure 3-18 Reference Design of Internal EMC Pad

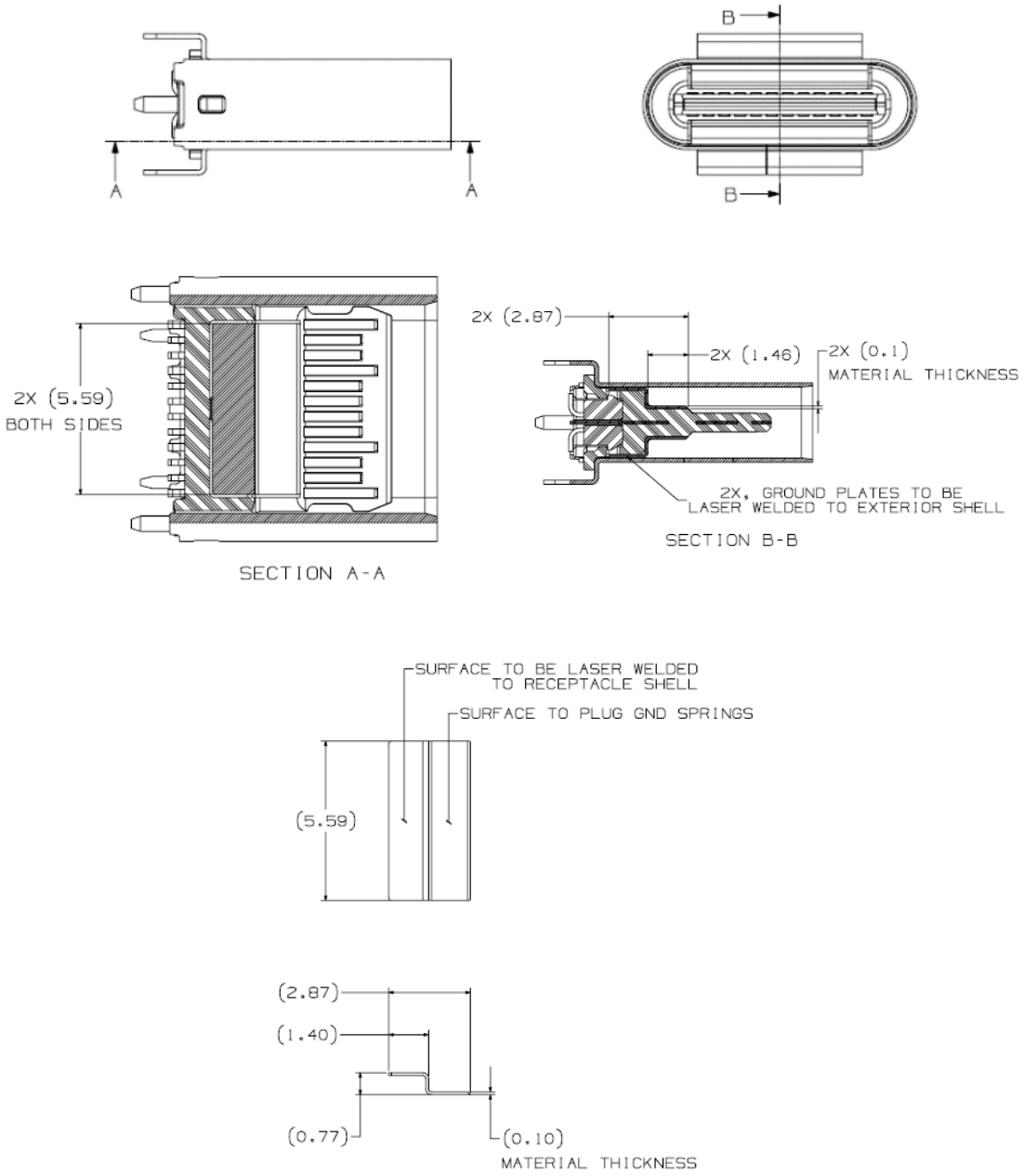


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

至关重要的是，内部 EMC 弹簧应尽可能靠近 EMC 弹簧配合接口接触插头外壳，以最大程度地缩短返回路径的长度。

图 3-18 所示的内部 EMC 垫（即接地板）位于插座内部。它与插头中的 EMC 弹簧配合。为了提供有效的接地回路，EMC 垫
应该与插座外壳有多个连接。

图 3-18 内置 EMC 垫参考设计

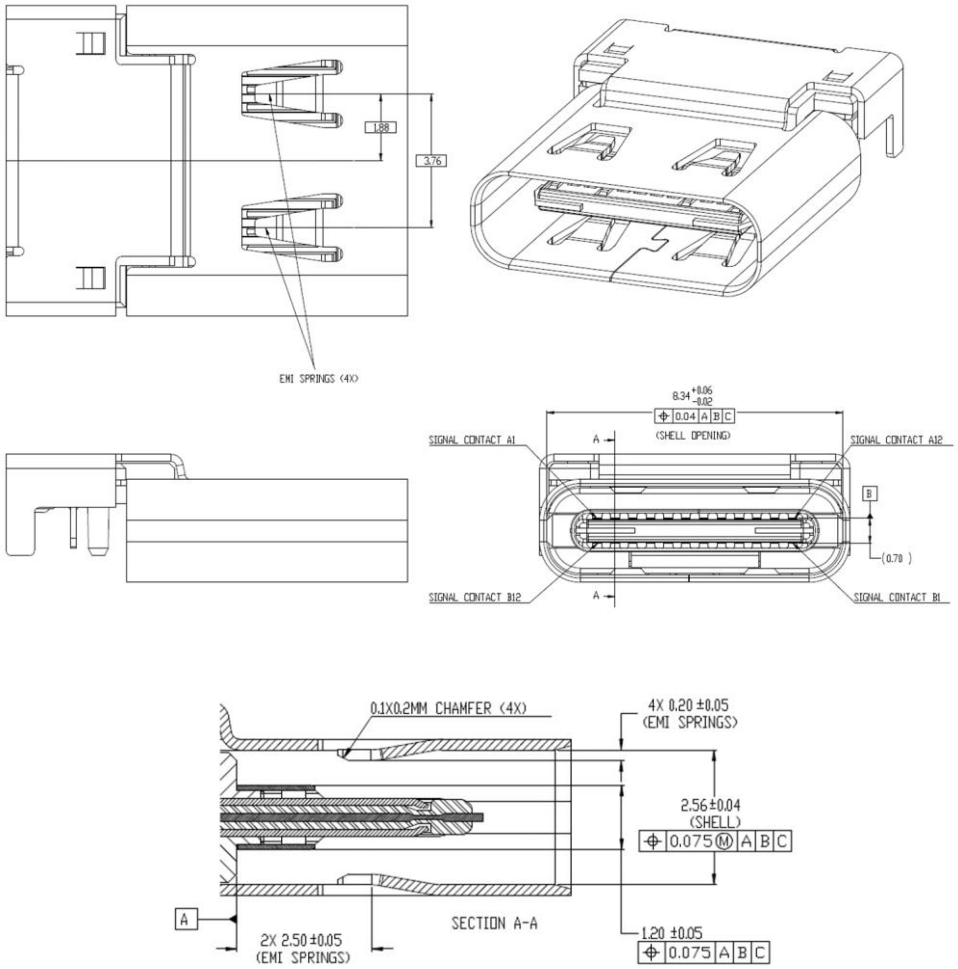


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.2.2.4 Optional External Receptacle EMC Springs (Informative)

Some applications may use receptacles with EMC springs that contact the outside of the plug shell. Figure 3-19 shows a reference receptacle design with external EMC springs. The EMC spring contact landing zones for the fully mated condition are normative and defined in Section 3.2.1.

Figure 3-19 Reference Design of a USB Type-C Receptacle with External EMC Springs

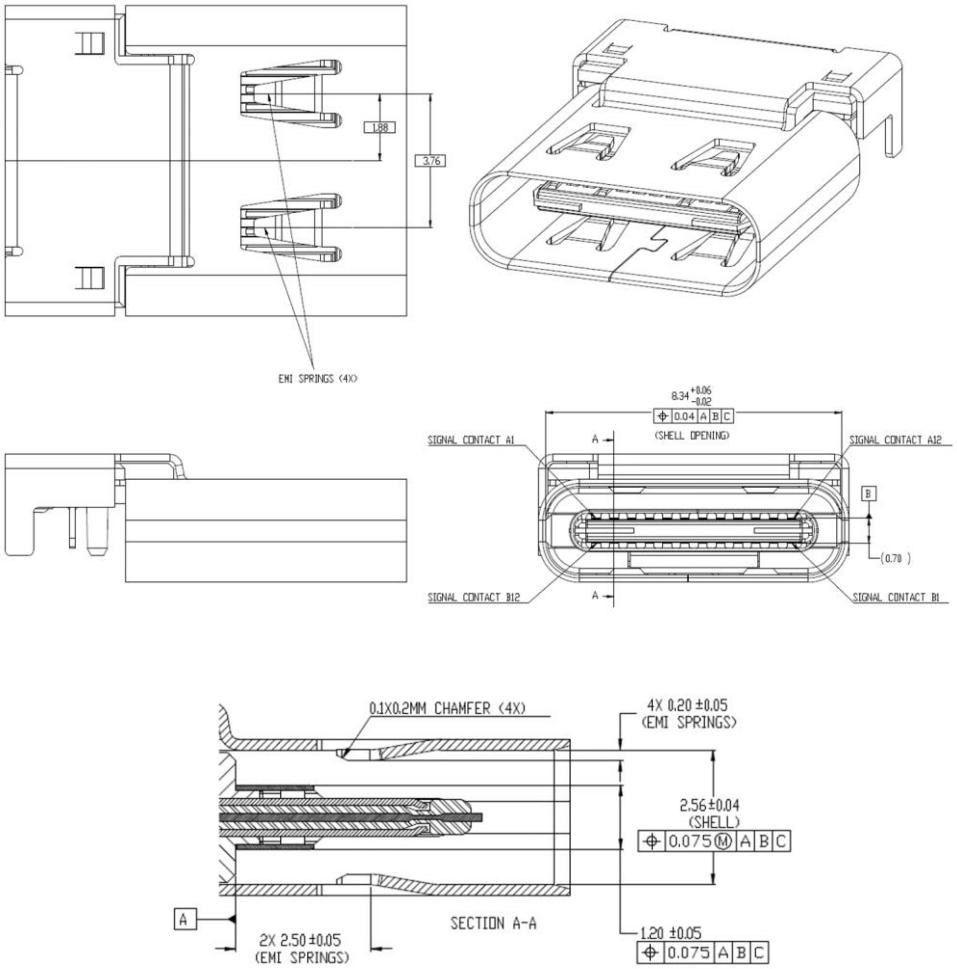


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.2.2.4 可选外部插座 EMC 弹簧（参考）

某些应用可能会使用带有 EMC 弹簧的插座，这些弹簧与插头外壳的外部接触。图 3-19 显示了带有外部 EMC 弹簧的参考插座设计。完全配合条件下的 EMC 弹簧接触着陆区是规范性的，在第 3.2.1 节中定义。

图 3-19 带外部 EMC 弹簧的 USB Type-C 插座参考设计



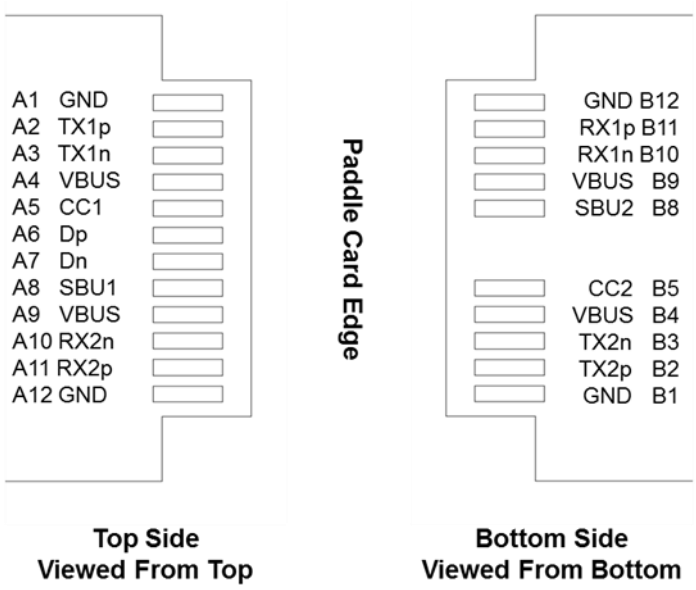
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.2.2.5 USB Full-Featured Type-C Plug Paddle Card (Informative)

The use of a paddle card is expected in the USB Full-Featured Type-C Plug. Figure 3-20 illustrates the paddle card pin assignment and contact spring connection location for a USB Full-Featured Type-C plug. The following guidelines are provided for the paddle card design:

- The paddle card should use high performance substrate material. The recommended paddle card thickness should have a tolerance less than or equal to ± 10%.
- The SuperSpeed USB traces should be as short as possible and have a nominal differential characteristic impedance of 85 Ω.
- The wire attach should have two high speed differential pairs on one side and two other high speed differential pairs on the other side, separated as far as practically allowed.
- It is recommended that a grounded coplanar waveguide (CPWG) system be selected as a transmission line method.
- Use of vias should be minimized.
- VBUS pins should be bussed together on the paddle card.
- GND pins should be bussed together on the paddle card.

Figure 3-20 Reference Design for a USB Full-Featured Type-C Plug Paddle Card



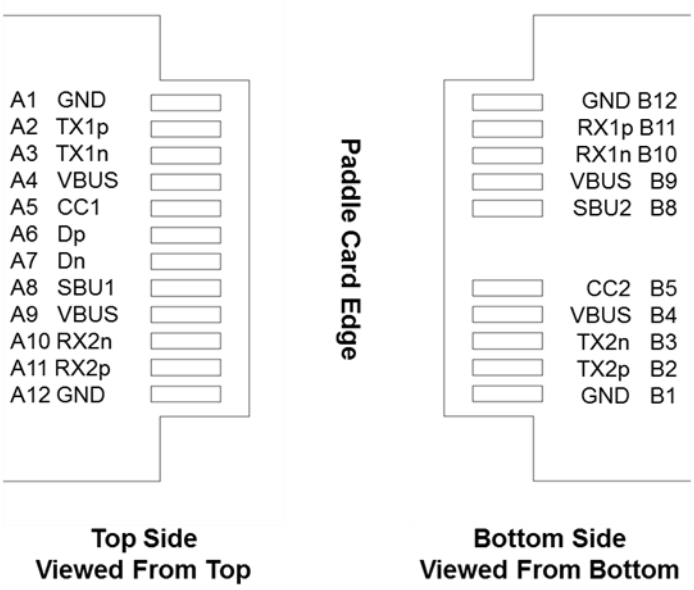
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.2.2.5 USB全功能Type-C插头插卡（参考资料）

USB 全功能 Type-C 插头中预计会使用插卡。图 3-20 显示了 USB 全功能 Type-C 插头的插卡引脚分配和接触弹簧连接位置。插卡设计遵循以下准则：

• 拨卡应采用高性能基板材料。建议
桨卡厚度的公差应小于或等于 ± 10%。• 超高速 USB 走线应尽可能短，并具有 85 Ω 的标称差分特性阻抗。• 线路连接应在一侧有两个高速差分对，在另一侧有两个其他高速差分对，并在实际允许的范围内尽可能分开。• 建议选择接地共面波导 (CPWG) 系统作为传输线方法。• 应尽量减少过孔的使用。• VBUS 引脚应在桨卡上通过总线连接在一起。• GND 引脚应在桨卡上通过总线连接在一起。

图 3-20 USB 全功能 Type-C 插头插卡参考设计



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.2.3 Pin Assignments and Descriptions

The usage and assignments of the 24 pins for the USB Type-C receptacle interface are defined in Table 3-4.

Table 3-4 USB Type-C Receptacle Interface Pin Assignments

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2	TXp1	Positive half of first TX differential pair	Second	B11	RXp1	Positive half of first RX differential pair	Second
A3	TXn1	Negative half of first TX differential pair	Second	B10	RXn1	Negative half of first RX differential pair	Second
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the *USB 2.0* differential pair – Position 1	Second	B7	Dn2	Negative half of the *USB 2.0* differential pair – Position 2	Second
A7	Dn1	Negative half of the *USB 2.0* differential pair – Position 1	Second	B6	Dp2	Positive half of the *USB 2.0* differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	VBUS	Bus Power	First	B4	VBUS	Bus Power	First
A10	RXn2	Negative half of second RX differential pair	Second	B3	TXn2	Negative half of second TX differential pair	Second
A11	RXp2	Positive half of second RX differential pair	Second	B2	TXp2	Positive half of second TX differential pair	Second
A12	GND	Ground return	First	B1	GND	Ground return	First

Notes:

1. Contacts B6 and B7 should not be present in the USB Type-C plug. The receptacle side shall support the *USB 2.0* differential pair present on Dp1/Dn1 or Dp2/Dn2. The plug orientation determines which pair is active. In one implementation, Dp1 and Dp2 may be shorted on the host/device as close to the receptacle as possible to minimize stub length; Dn1 and Dn2 may also be shorted. The maximum shorting trace length should not exceed 3.5 mm.
2. All VBUS pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all VBUS pins bussed together on the PCB).
3. All Ground return pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all ground return pins bussed together on the PCB).
4. If the contact dimensions shown in Figure 3-1 ALTERNATE SECTION A-A are used, then the VBUS contacts (A4, A9, B4 and B9) mate second, and signal contacts (A2, A3, A5, A6, A7, A8, A10, A11, B2, B3, B5, B6, B7, B8, B10 and B11) mate third.

The usage and assignments of the signals necessary for the support of only *USB 2.0* with the USB Type-C mating interface are defined in Table 3-5.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.2.3 引脚分配及说明

USB Type-C 插座接口的 24 个引脚的用途和分配定义在表 3-4 中。

表 3-4 USB Type-C 插座接口引脚分配

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2	TXp1	Positive half of first TX differential pair	Second	B11	RXp1	Positive half of first RX differential pair	Second
A3	TXn1	Negative half of first TX differential pair	Second	B10	RXn1	Negative half of first RX differential pair	Second
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the *USB 2.0* differential pair – Position 1	Second	B7	Dn2	Negative half of the *USB 2.0* differential pair – Position 2	Second
A7	Dn1	Negative half of the *USB 2.0* differential pair – Position 1	Second	B6	Dp2	Positive half of the *USB 2.0* differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	VBUS	Bus Power	First	B4	VBUS	Bus Power	First
A10	RXn2	Negative half of second RX differential pair	Second	B3	TXn2	Negative half of second TX differential pair	Second
A11	RXp2	Positive half of second RX differential pair	Second	B2	TXp2	Positive half of second TX differential pair	Second
A12	GND	Ground return	First	B1	GND	Ground return	First

否注意：1. 触点 B6 和 B7 不应存在于 USB Type-C 插头中。插座侧应支持 Dp1/Dn1 或 Dp2/Dn2 上存在的 *USB 2.0* 差分对。插头方向决定哪对有效。在一个实现中，Dp1 和 Dp2 可以在主机/设备上短路，因为靠近

到插座以最小化短截线长度；Dn1 和 Dn2 也可以短接。最大短接迹线长度不应超过 3.5 毫米。2. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起，并且应在插座处于安装状态时在 USB Type-C 插座连接器处连接在一起（例如，所有 VBUS 引脚在 PCB 上总线连接在一起）。3. 所有接地返回引脚应在 USB Type-C 插头内连接在一起，并且应在插座处于安装状态时在 USB Type-C 插座连接器处连接在一起（例如，所有接地返回引脚在 PCB 上总线连接在一起）。 4. 如果使用图 3-1 ALTERNATE SECTION A-A 中所示的触点尺寸，则 VBUS 触点（A4、A9、B4 和 B9）第二个匹配，信号触点（A2、A3、A5、A6、A7、A8、A10、A11、B2、B3、B5、B6、B7、B8、B10 和 B11）第三个匹配。

表 3-5 定义了仅支持 USB Type-C 配接接口的 *USB 2.0* 所需信号的使用和分配。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-5 USB Type-C Receptacle Interface Pin Assignments for USB 2.0-only Support

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2				B11			
A3				B10			
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the *USB 2.0* differential pair – Position 1	Second	B7	Dn2	Negative half of the *USB 2.0* differential pair – Position 2	Second
A7	Dn1	Negative half of the *USB 2.0* differential pair – Position 1	Second	B6	Dp2	Positive half of the *USB 2.0* differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	VBUS	Bus Power	First	B4	VBUS	Bus Power	First
A10				B3			
A11				B2			
A12	GND	Ground return	First	B1	GND	Ground return	First

Notes:

1. Unused contact locations shall be electrically isolated from power, ground or signaling (i.e., not connected).
2. Contacts B6 and B7 should not be present in the USB Type-C plug. The receptacle side shall support the *USB 2.0* differential pair present on Dp1/Dn1 or Dp2/Dn2. The plug orientation determines which pair is active. In one implementation, Dp1 and Dp2 may be shorted on the host/device as close to the receptacle as possible to minimize stub length; Dn1 and Dn2 may also be shorted. The maximum shorting trace length should not exceed 3.5 mm.
3. Contacts A8 and B8 (SBU1 and SBU2) shall be not connected unless required for a specified purpose (e.g., Audio Adapter Accessory Mode).
4. All VBUS pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all VBUS pins bussed together on the PCB).
5. All Ground return pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all ground return pins bussed together on the PCB).
6. If the contact dimensions shown in Figure 3-1 ALTERNATE SECTION A-A are used then the VBUS contacts (A4, A9, B4 and B9) mate second, and signal contacts (A5, A6, A7, A8, B5, B6, B7 and B8) mate third.

3.3 Cable Construction and Wire Assignments

This section discusses the USB Type-C cables, including cable construction, wire assignments, and wire gauges.

3.3.1 Cable Construction (Informative)

Figure 3-21 illustrates an example of USB Full-Featured Type-C cable cross-section, using micro-coaxial wires for TX/RX pairs. There are four groups of wires: USB D+/D− (typically unshielded twisted pairs (UTP)), TX/RX signal pairs (coaxial wires, twin-axial or shielded twisted pairs), sideband signal wires, and power and ground wires. In this example, the optional VCONN wire is shown whereas in Figure 3-22 the example is shown with the VCONN

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-5 仅支持 USB 2.0 的 USB Type-C 插座接口引脚分配

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2				B11			
A3				B10			
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the *USB 2.0* differential pair – Position 1	Second	B7	Dn2	Negative half of the *USB 2.0* differential pair – Position 2	Second
A7	Dn1	Negative half of the *USB 2.0* differential pair – Position 1	Second	B6	Dp2	Positive half of the *USB 2.0* differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	VBUS	Bus Power	First	B4	VBUS	Bus Power	First
A10				B3			
A11				B2			
A12	GND	Ground return	First	B1	GND	Ground return	First

否注意事项：1. 未使用的触点位置应与电源、接地或信号电隔离（即，不连接）。2. USB Type-C 插头中不应存在触点 B 6 和 B7。插座侧应支持 Dp1/Dn1 或 Dp2/Dn2 上的 *USB 2.0* 差分对。插头方向决定哪对处于活动状态。在一种实现中，Dp1 和 Dp2 可在尽可能靠近插座的主机/设备上短接以最小化短截线长度；Dn1 和 Dn2 也可以短接。最大短接迹线长度不应超过 3.5 毫米。3. 除非出于特定目的（例如，音频适配器附件模式）需要，否则触点 A8 和 B8（SBU1 和 SBU2）不得连接。 4. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起，并且应在 USB Type-C 插座连接器处连接在一起（当插座处于安装状态时，例如，所有 VBUS 引脚在 PCB 上总线连接在一起）。 5. 所有接地返回引脚应在 USB Type-C 插头内连接在一起，并且应在 USB Type-C 插座连接器处连接在一起（当插座处于安装状态时，例如，所有接地返回引脚在 PCB 上总线连接在一起）。 6. 如果使用图 3-1 ALTERNATE SECTION A-A 中所示的触点尺寸，则 VBUS 触点（A4、A9、B4 和 B9）第二个配对，信号触点（A5、A6、A7、A8、B5、B6、B7 和 B8）第三个配对。

3.3 电缆结构和电线分配

本节讨论 USB Type-C 电缆，包括电缆结构、电线分配和电线规格。

3.3.1 电缆结构（参考资料）

图 3-21 显示了 USB 全功能 Type-C 电缆横截面的示例，使用微同轴线作为 TX/RX 对。有四组电线：USB D+/D–（通常为非屏蔽双绞线 (UTP)）、TX/RX 信号对（同轴线、双轴或屏蔽双绞线）、边带信号线以及电源线和地线。在此示例中，显示了可选的 VCONN 电线，而图 3-22 中的示例显示了 VCONN

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

wire removed – the inclusion of VCONN or not relates to the implementation approach chosen for Electronically Marked Cables (See Section 4.9).

Figure 3-21 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example with VCONN

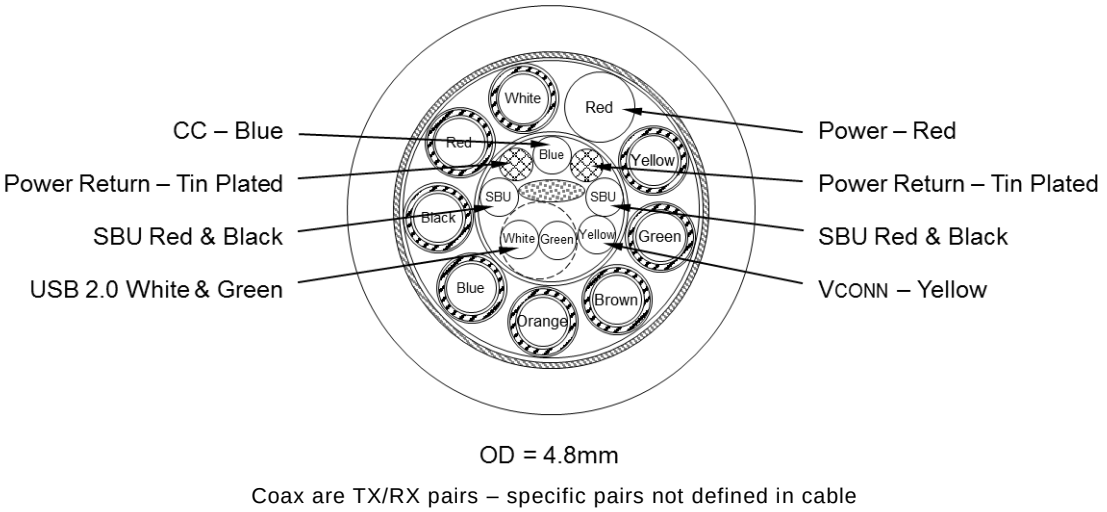
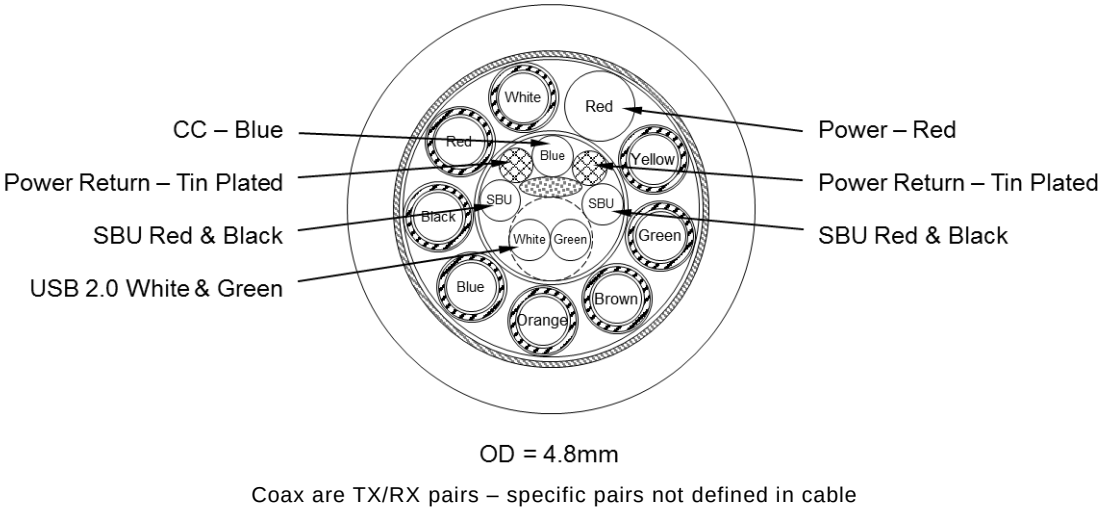


Figure 3-22 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example without VCONN

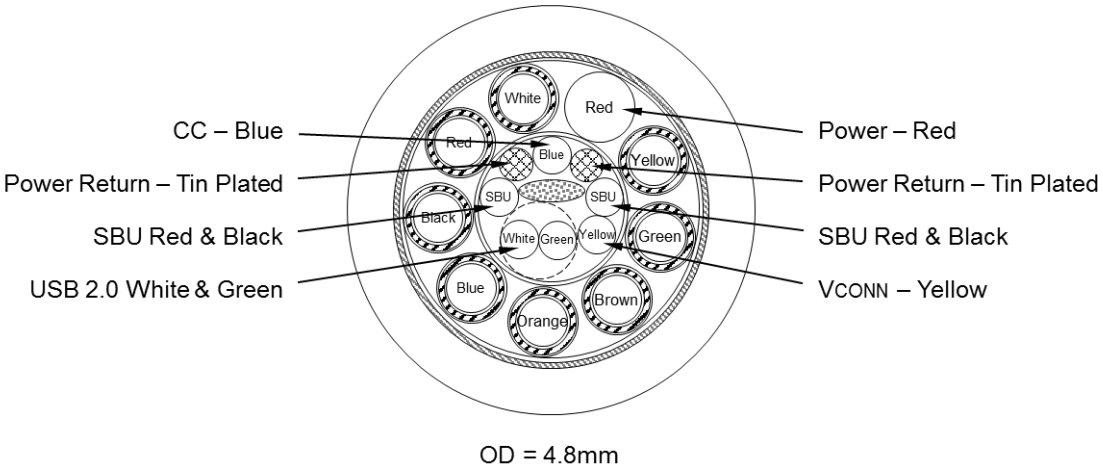


The USB D+/D− signal pair is intended to transmit the *USB 2.0* Low-Speed, Full-Speed and High-Speed signaling while the TX/RX signal pairs are used for either *USB 3.2* or *USB4* signaling. Shielding is needed for the TX/RX differential pairs for signal integrity and EMC performance.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

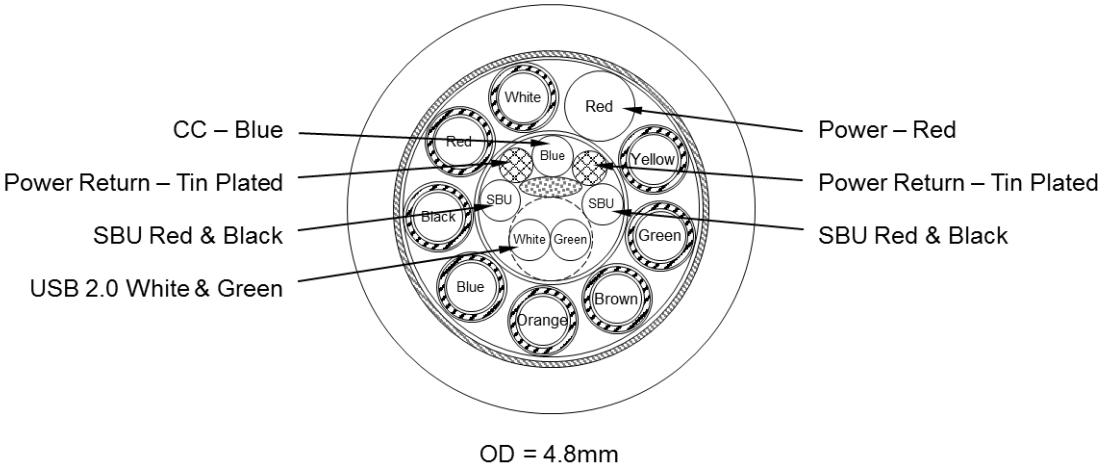
移除电线——是否包含 VCONN 与为电子标记电缆选择的实施方法有关（参见第 4.9 节）。

图 3-21 USB 全功能 Type-C 线缆横截面示意图，以 VCONN 为示例的同轴线



同轴电缆为 TX/RX 对 – 电缆中未定义具体对

图 3-22 USB 全功能 Type-C 线缆横截面图，不含 VCONN 的同轴线示例



同轴电缆为 TX/RX 对 – 电缆中未定义具体对

USB D+/D− 信号对用于传输 *USB 2.0* 低速、全速和高速信号，而 TX/RX 信号对则用于 *USB 3.2* 或 *USB4* 信号。TX/RX 差分对需要屏蔽，以确保信号完整性和 EMC 性能。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.3.2 Wire Assignments

Table 3-6 defines the full set of possible wires needed to produce all standard USB Type-C cables assemblies. For some cable assemblies, not all of these wires are used. For example, a USB Type-C cable that only provides *USB 2.0* functionality will not include wires 6–15.

Table 3-6 USB Type-C Standard Cable Wire Assignments

Wire Number	Signal Name	Description
1	GND_PWRrt1	Ground for power return
2	PWR_VBUS1	VBUS power
3	CC	Configuration Channel
4	UTP_Dp	Unshielded twist pair, positive
5	UTP_Dn	Unshielded twist pair, negative
6	SDPp1	Shielded differential pair #1, positive
7	SDPn1	Shielded differential pair #1, negative
8	SDPp2	Shielded differential pair #2, positive
9	SDPn2	Shielded differential pair #2, negative
10	SDPp3	Shielded differential pair #3, positive
11	SDPn3	Shielded differential pair #3, negative
12	SDPp4	Shielded differential pair #4, positive
13	SDPn4	Shielded differential pair #4, negative
14	SBU_A	Sideband Use
15	SBU_B	Sideband Use
16	GND_PWRrt2	Ground for power return (optional)
17	PWR_VBUS2	VBUS power (optional)
18	PWR_VCONN	VCONN power (optional, see Section 4.9)
Braid	Shield	Cable external braid

Note:

1. This table is based on the assumption that coaxial wire construction is used for all SDP's and there are no drain wires. The signal ground return is through the shields of the coaxial wires. If shielded twisted or twin-axial pairs are used, then drain wires are needed.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.3.2 线路分配

表 3-6 定义了生产所有标准 USB Type-C 电缆组件所需的全部可能电线。对于某些电缆组件，并非所有这些电线都会用到。例如，仅提供 *USB 2.0* 功能的 USB Type-C 电缆将不包含电线 6-15。

表 3-6 USB Type-C 标准电缆线分配

Wire Number	Signal Name	Description
1	GND_PWRrt1	Ground for power return
2	PWR_VBUS1	VBUS power
3	CC	Configuration Channel
4	UTP_Dp	Unshielded twist pair, positive
5	UTP_Dn	Unshielded twist pair, negative
6	SDPp1	Shielded differential pair #1, positive
7	SDPn1	Shielded differential pair #1, negative
8	SDPp2	Shielded differential pair #2, positive
9	SDPn2	Shielded differential pair #2, negative
10	SDPp3	Shielded differential pair #3, positive
11	SDPn3	Shielded differential pair #3, negative
12	SDPp4	Shielded differential pair #4, positive
13	SDPn4	Shielded differential pair #4, negative
14	SBU_A	Sideband Use
15	SBU_B	Sideband Use
16	GND_PWRrt2	Ground for power return (optional)
17	PWR_VBUS2	VBUS power (optional)
18	PWR_VCONN	VCONN power (optional, see Section 4.9)
Braid	Shield	Cable external braid

否注：1. 本表基于以下假设：所有 SDP 均采用同轴电缆结构，且无排扰线。信号接地回路通过同轴电缆的屏蔽层。如果使用屏蔽双绞线或双轴对，则需要排扰线。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-7 defines the full set of possible wires needed to produce USB Type-C to legacy cable assemblies. For some cable assemblies, not all of these wires are needed. For example, a USB Type-C to *USB 2.0* Standard-B cable will not include wires 5–10.

Table 3-7 USB Type-C Cable Wire Assignments for Legacy Cables/Adapters

Wire Number	Signal Name	Description
1	GND_PWRrt1	Ground for power return
2	PWR_VBUS1	VBUS power
3	UTP_Dp	Unshielded twist pair, positive
4	UTP_Dn	Unshielded twist pair, negative
5	SDPp1	Shielded differential pair #1, positive
6	SDPn1	Shielded differential pair #1, negative
7	SDP1_Drain	Drain wire for SDPp1 and SDPn1
8	SDPp2	Shielded differential pair #2, positive
9	SDPn2	Shielded differential pair #2, negative
10	SDP2_Drain	Drain wire for SDPp2 and SDPn2
Braid	Shield	Cable external braid

Note:

a. This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are needed and the signal ground return is through the shields of the coaxial wires.

3.3.3 Wire Gauges and Cable Diameters (Informative)

This specification does not specify wire gauge. Table 3-8 and Table 3-9 list typical wire gauges for reference purposes only. A large gauge wire incurs less loss, but at the cost of cable diameter and flexibility. Multiple wires may be used for a single wire such as for VBUS or Ground. It is recommended to use the smallest possible wire gauges that meet the cable assembly electrical and mechanical requirements.

To maximize cable flexibility, all wires should be stranded and the cable outer diameter should be minimized as much as possible. A typical USB Full-Featured Type-C cable outer diameter may range from 4 mm to 6 mm while a typical *USB 2.0* Type-C cable outer diameter may range from 2 mm to 4 mm. A typical USB Type-C to *USB 3.1* legacy cable outer diameter may range from 3 mm to 5 mm.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-7 定义了生产 USB Type-C 转传统电缆组件所需的全部电线。对于某些电缆组件，并不需要所有这些电线。例如，USB Type-C 转 *USB 2.0* 标准 B 电缆将不包含电线 5-10。

表 3-7 USB Type-C 电缆线分配（适用于传统电缆/适配器）

Wire Number	Signal Name	Description
1	GND_PWRrt1	Ground for power return
2	PWR_VBUS1	VBUS power
3	UTP_Dp	Unshielded twist pair, positive
4	UTP_Dn	Unshielded twist pair, negative
5	SDPp1	Shielded differential pair #1, positive
6	SDPn1	Shielded differential pair #1, negative
7	SDP1_Drain	Drain wire for SDPp1 and SDPn1
8	SDPp2	Shielded differential pair #2, positive
9	SDPn2	Shielded differential pair #2, negative
10	SDP2_Drain	Drain wire for SDPp2 and SDPn2
Braid	Shield	Cable external braid

注意：a. 本表基于以下假设：所有 SDP 均使用屏蔽双绞线，且有排扰线。如果使用同轴电缆结构，则无需排扰线，信号接地回路通过同轴电缆的屏蔽层。

3.3.3 线规和电缆直径（参考 ）

本规范未指定线规。表 3-8 和表 3-9 列出了典型的线规，仅供参考。线规较大的线损耗较小，但会牺牲电缆直径和柔韧性。多根线可以用作单根线，例如 V BUS 或接地线。建议使用尽可能小的线规，以满足电缆组件的电气和机械要求。

为了最大限度地提高电缆的灵活性，所有电线都应绞合在一起，并且应尽可能减小电缆外径。典型的 USB 全功能 Type-C 电缆外径范围为 4 毫米至 6 毫米，而典型的 *USB 2.0* Type-C 电缆外径范围为 2 毫米至 4 毫米。典型的 USB Type-C 至 *USB 3.1* 传统电缆外径范围为 3 毫米至 5 毫米。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-8 Reference Wire Gauges for standard USB Type-C Cable Assemblies

Wire Number	Signal Name	Wire Gauge (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	CC	32-34
4	UTP_Dp	28-34
5	UTP_Dn	28-34
6	SDPp1	26-34
7	SDPn1	26-34
8	SDPp2	26-34
9	SDPn2	26-34
10	SDPp3	26-34
11	SDPn3	26-34
12	SDPp4	26-34
13	SDPn4	26-34
14	SBU_A	32-34
15	SBU_B	32-34
16	GND_PWRrt2	20-28
17	PWR_VBUS2	20-28
18	PWR_VCONN	32-34

Table 3-9 Reference Wire Gauges for USB Type-C to Legacy Cable Assemblies

Wire Number	Signal Name	Wire Gauge (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	UTP_Dp	28-34
4	UTP_Dn	28-34
5	SDPp1	26-34
6	SDPn1	26-34
7	SDP1_Drain	28-34
8	SDPp2	26-34
9	SDPn2	26-34
10	SDP2_Drain	28-34

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-8 标准 USB Type-C 电缆组件的参考线规

Wire Number	Signal Name	Wire Gauge (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	CC	32-34
4	UTP_Dp	28-34
5	UTP_Dn	28-34
6	SDPp1	26-34
7	SDPn1	26-34
8	SDPp2	26-34
9	SDPn2	26-34
10	SDPp3	26-34
11	SDPn3	26-34
12	SDPp4	26-34
13	SDPn4	26-34
14	SBU_A	32-34
15	SBU_B	32-34
16	GND_PWRrt2	20-28
17	PWR_VBUS2	20-28
18	PWR_VCONN	32-34

表 3-9 USB Type-C 转传统线缆组件的参考线规

Wire Number	Signal Name	Wire Gauge (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	UTP_Dp	28-34
4	UTP_Dn	28-34
5	SDPp1	26-34
6	SDPn1	26-34
7	SDP1_Drain	28-34
8	SDPp2	26-34
9	SDPn2	26-34
10	SDP2_Drain	28-34

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.4 Standard USB Type-C Cable Assemblies

Two standard USB Type-C cable assemblies are defined and allowed by this specification. In addition, captive cables are allowed (see Section 3.4.3). Shielding (braid) is required to enclose all the wires in the USB Type-C cable. The shield shall be terminated to the plug metal shells. The shield should be physically connected to the plug metal shell as close to 360° as possible, to control EMC.

Note: Up until Release 1.4 of this specification, the TX and RX signals used in this specification were named SSTX and SSRX. With the introduction of USB4, these signals were renamed such that they generically can apply to both SuperSpeed USB and USB4 signaling. It is intended that the TX and RX signal names are synonymous with the original SSTX and SSRX names for implementations prior to Release 2.0 of this specification.

3.4.1 USB Full-Featured Type-C Cable Assembly

Figure 3-23 shows a USB Full-Featured Type-C standard cable assembly.

Figure 3-23 USB Full-Featured Type-C Standard Cable Assembly

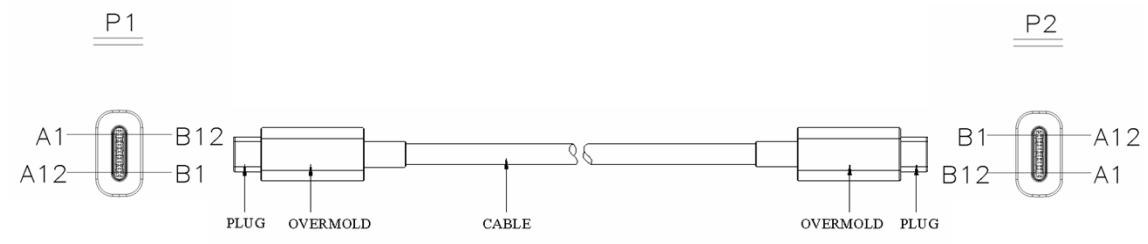


Table 3-10 defines the wire connections for the USB Full-Featured Type-C standard cable assembly.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.4 标准 USB Type-C 电缆组件

本规范定义并允许使用两种标准 USB Type-C 电缆组件。此外，还允许使用固定电缆（见第 3.4.3 节）。需要使用屏蔽层（编织层）包裹 USB Type-C 电缆中的所有电线。屏蔽层应端接到插头金属外壳。屏蔽层应尽可能 360° 地物理连接到插头金属外壳，以控制 EMC。

注意：在本规范的 1.4 版之前，本规范中使用的 TX 和 RX 信号被命名为 SSTX 和 SSRX。随着 USB4 的推出，这些信号被重新命名，以便它们可以同时适用于超高速 USB 和 USB4 信号。TX 和 RX 信号名称旨在与本规范 2.0 版之前的实现中的原始 SSTX 和 SSRX 名称同义。

3.4.1 USB 全功能 Type-C 线缆组件

图 3-23 显示了 USB 全功能 Type-C 标准电缆组件。

图 3-23 USB 全功能 Type-C 标准线缆组件

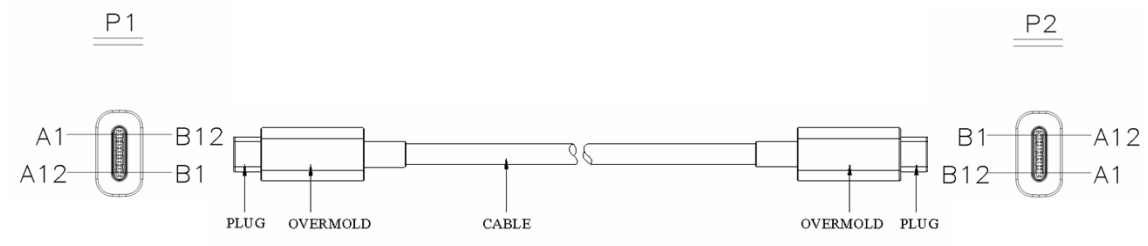


表 3-10 定义了 USB 全功能 Type-C 标准电缆组件的电线连接。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-10 USB Full-Featured Type-C Standard Cable Assembly Wiring

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1 [16]	GND_PWRrt1 [GND_PWRrt2]	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2 [17]	PWR_VBUS1 [PWR_VBUS2]	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See Section 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
A2	TXp1	6	SDPp1	B11	RXp1
A3	TXn1	7	SDPn1	B10	RXn1
B11	RXp1	8	SDPp2	A2	TXp1
B10	RXn1	9	SDPn2	A3	TXn1
B2	TXp2	10	SDPp3	A11	RXp2
B3	TXn2	11	SDPn3	A10	RXn2
A11	RXp2	12	SDPp4	B2	TXp2
A10	RXn2	13	SDPn4	B3	TXn2
A8	SBU1	14	SBU_A	B8	SBU2
B8	SBU2	15	SBU_B	A8	SBU1
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. This table is based on the assumption that coaxial wire construction is used for all SDP's and there are no drain wires. The shields of the coaxial wires are connected to the ground pins. If shielded twisted pair is used, then drain wires are needed and shall be connected to the GND pins.
2. Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A 10 nF bypass capacitor (minimum voltage rating of 30 V) is required for the VBUS pin in the full-featured cable at each end of the cable. The bypass capacitor should be placed as close as possible to the power supply pad.
5. All GND pins shall be connected together within the USB Type-C plug
6. Shield and GND shall be connected within the USB Type-C plug on both ends of the cable assembly.

3.4.2 USB 2.0 Type-C Cable Assembly

A *USB 2.0* Type-C standard cable assembly has the same form factor shown in Figure 3-23.

Table 3-11 defines the wire connections for the *USB 2.0* Type-C standard cable assembly.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-10 USB 全功能 Type-C 标准电缆组件接线

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1 [16]	GND_PWRrt1 [GND_PWRrt2]	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2 [17]	PWR_VBUS1 [PWR_VBUS2]	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See Section 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
A2	TXp1	6	SDPp1	B11	RXp1
A3	TXn1	7	SDPn1	B10	RXn1
B11	RXp1	8	SDPp2	A2	TXp1
B10	RXn1	9	SDPn2	A3	TXn1
B2	TXp2	10	SDPp3	A11	RXp2
B3	TXn2	11	SDPn3	A10	RXn2
A11	RXp2	12	SDPp4	B2	TXp2
A10	RXn2	13	SDPn4	B3	TXn2
A8	SBU1	14	SBU_A	B8	SBU2
B8	SBU2	15	SBU_B	A8	SBU1
Shell	Shield	Outer shield	Shield	Shell	Shield

否注释：1. 本表基于以下假设：所有 SDP 均采用同轴电缆结构，且无排扰线。同轴电缆的屏蔽层连接至接地引脚。如果使用屏蔽双绞线，则需要排扰线，并应连接至 GND 引脚。2. 此电缆的电子标记版本应使用 USB Type-C 插头的引脚 B5 (VCONN)。

请参阅第 4.9 节。 3. USB Type-C 插头中不应存在触点 B6 和 B7。 4. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起。全功能电缆两端的 VBUS 引脚需要一个 10 nF 旁路电容（最低电压额定值为 30 V）。旁路电容应尽可能靠近电源焊盘。 5. 所有 GND 引脚应在 USB Type-C 插头内连接在一起 6. 屏蔽层和 GND 应在电缆组件两端的 USB Type-C 插头内连接在一起。

3.4.2 USB 2.0 Type-C 电缆组件

USB 2.0 Type-C 标准电缆组件具有与图 3-23 所示的相同的外形尺寸。

表 3-11 定义了 *USB 2.0* Type-C 标准电缆组件的线路连接。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-11 *USB 2.0* Type-C Standard Cable Assembly Wiring

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See Section 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is not required for the VBUS pin in the *USB 2.0* Type-C cable.
4. All GND pins shall be connected together within the USB Type-C plug.
5. All USB Type-C plug pins that are not listed in this table shall be open (not connected).
6. Shield and GND grounds shall be connected within the USB Type-C plug on both ends of the cable assembly.

3.4.3 USB Type-C Captive Cable Assemblies

A captive cable assembly is a cable assembly that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end. The cable assembly that is hardwired is not detachable from the device.

The assembly wiring for captive USB Type-C cables follow the same wiring assignments as the standard cable assemblies (see Table 3-10 and Table 3-11) with the exception that the hardwired attachment on the device side substitutes for the USB Type-C Plug #2 end.

The CC wire in a captive cable shall be terminated and behave as appropriate to the function of the product to which it is captive (e.g. host or device).

This specification does not define how the hardwired attachment is physically done on the device side.

3.5 Legacy Cable Assemblies

To enable interoperability between USB Type-C-based products and legacy USB products, the following standard legacy cable assemblies are defined. Only the cables defined within this specification are allowed.

Legacy cable assemblies that source power to a USB Type-C connector (e.g. a USB Type-C to USB Standard-A plug cable assembly and a USB Type-C plug to USB Micro-B receptacle adapter assembly) are required to use the Default USB Type-C Current Rp resistor (56 kΩ). The value of Rp is used to inform the Sink how much current the Source can provide. Since the legacy cable assembly does not comprehend the capability of the Source it is connected to, it is only allowed to advertise Default USB Type-C Current as defined by the *USB 2.0*, *USB*

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-11 ***USB 2.0*** Type-C 标准电缆组件接线

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See Section 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
Shell	Shield	Outer shield	Shield	Shell	Shield

注意：1. 该电缆的电子标记版本应使用 USB Type-C 插头的引脚 B5 (VCONN)。

请参阅第 4.9 节。2. USB Type-C 插头中不应存在触点 B6 和 B7。3. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起。*USB 2.0* Type-C 电缆中的 VBUS 引脚无需旁路电容。4. 所有 GND 引脚应在 USB Type-C 插头内连接在一起。5. 本表未列出的所有 USB Type-C 插头引脚应开路（未连接）。6. 屏蔽和 GND 接地应在电缆组件两端的 USB Type-C 插头内连接。

3.4.3 USB Type-C 固定电缆组件

固定电缆组件是一种一端带有 USB Type-C 插头、另一端具有供应商特定连接方式（硬接线或定制可拆卸）的电缆组件。硬接线的电缆组件不能从设备上拆卸。

固定式 USB Type-C 电缆的组装接线遵循与标准电缆组件相同的接线分配（参见表 3-10 和表 3-11），不同之处在于设备端的硬连线附件替代了 USB Type-C 插头 #2 端。

固定电缆中的 CC 线应端接并按照功能要求运行
它所依赖的产品（例如主机或设备）。

该规范没有定义硬连线附件在设备端的物理完成方式。

3.5 传统电缆组件

为了实现基于 USB Type-C 的产品与传统 USB 产品之间的互操作性，定义了以下标准传统电缆组件。仅允许使用此规范中定义的电缆。

为 USB Type-C 连接器供电的传统电缆组件（例如 USB Type-C 转 USB 标准 A 插头电缆组件和 USB Type-C 插头转 USB Micro-B 插座适配器组件）需要使用默认 USB Type-C 电流 Rp 电阻（56 kΩ）。Rp 的值用于告知接收器源可以提供多少电流。由于传统电缆组件不理解所连接的源的能力，因此仅允许通告 *USB 2.0*、*USB* 定义的默认 USB Type-C 电流

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.1 and USB BC 1.2 specifications. No other Rp values are permitted because these may cause a USB Type-C Sink to overload a legacy power supply.

3.5.1 USB Type-C to USB 3.1 Standard-A Cable Assembly

Figure 3-24 shows a USB Type-C to USB 3.1 Standard-A cable assembly.

Figure 3-24 USB Type-C to USB 3.1 Standard-A Cable Assembly

Table 3-12 defines the wire connections for the USB Type-C to USB 3.1 Standard-A cable assembly.

Table 3-12 USB Type-C to USB 3.1 Standard-A Cable Assembly Wiring

USB Type-C Plug		Wire		USB 3.1 Standard-A plug	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 2			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
A2	TXp1	5	SDPp1	6	StdA_SSRX+
A3	TXn1	6	SDPn1	5	StdA_SSRX–
B11	RXp1	8	SDPp2	9	StdA_SSTX+
B10	RXn1	9	SDPn2	8	StdA_SSTX–
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present and the shields of the coaxial wires are connected to the ground pins.
2. Pin A5 (CC) of the USB Type-C plug shall be connected to VBUS through a resistor Rp (56 kΩ ± 5%). See Section 4.5.3.2.2 and Table 4-24 for the functional description and value of Rp.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor shall be 10nF ± 20% in cables which incorporate a USB Standard-A plug. The bypass capacitor shall be placed as close as possible to the power supply pad.
5. All Ground return pins shall be connected together within the USB Type-C plug.
6. Shield and GND grounds shall be connected within the USB Type-C and USB 3.1 Standard-A plugs on both ends of the cable assembly.
7. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.1 和 *USB BC 1.2* 规范。不允许使用其他 Rp 值，因为这些值可能会导致 USB Type-C Sink 使传统电源过载。

3.5.1 USB Type-C 转 ***USB 3.1*** 标准 A 型电缆组件

图 3-24 显示了 USB Type-C 至 *USB 3.1* 标准 A 电缆组件。

图 3-24 USB Type-C 转 USB 3.1 标准 A 型线缆组件

表 3-12 定义了 USB Type-C 至 *USB 3.1* 标准 A 电缆组件的线路连接。

表 3-12 USB Type-C 转 ***USB 3.1*** 标准 A 型电缆组件接线

USB Type-C Plug		Wire		USB 3.1 Standard-A plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 2			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
A2	TXp1	5	SDPp1	6	StdA_SSRX+
A3	TXn1	6	SDPn1	5	StdA_SSRX–
B11	RXp1	8	SDPp2	9	StdA_SSTX+
B10	RXn1	9	SDPn2	8	StdA_SSTX–
Shell	Shield	Outer shield	Shield	Shell	Shield

否注意事项：1. 此表基于以下假设：所有 SDP 均使用屏蔽双绞线，且有排扰线。如果使用同轴线结构，则不存在排扰线，且同轴线的屏蔽层连接到接地引脚。2. USB Type-C 插头的引脚 A5 (CC) 应通过电阻 Rp (56 kΩ ± 5%) 连接到 VBUS。有关 Rp 的功能描述和值，请参见第 4.5.3.2.2 节和表 4-24。3. USB Type-C 插头中不应存在触点 B6 和 B7。4. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起。电缆的 USB Type-C 插头侧的 VBUS 和接地引脚之间需要一个旁路电容。对于包含 USB 标准 A 型插头的电缆，旁路电容应为 10nF ± 20%。旁路电容应尽可能靠近电源焊盘放置。5. 所有接地返回引脚应在 USB Type-C 插头内连接在一起。6. 屏蔽和 GND 接地应在电缆组件两端的 USB Type-C 和 *USB 3.1* 标准 A 插头内连接。7. 本表未列出的所有 USB Type-C 插头引脚应处于开路状态（未连接）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.5.2 USB Type-C to *USB 2.0* Standard-A Cable Assembly

Figure 3-25 shows a USB Type-C to *USB 2.0* Standard-A cable assembly.

Figure 3-25 USB Type-C to *USB 2.0* Standard-A Cable Assembly

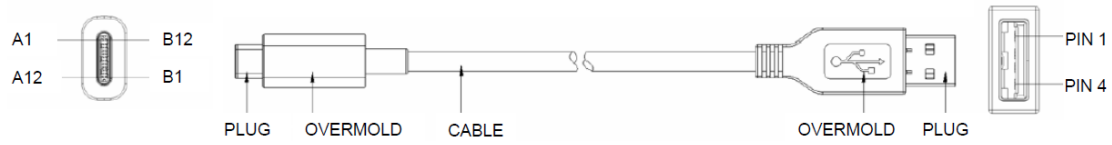


Table 3-13 defines the wire connections for the USB Type-C to *USB 2.0* Standard-A cable assembly.

Table 3-13 USB Type-C to *USB 2.0* Standard-A Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Standard-A plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to VBUS through a resistor Rp (56 kΩ ± 5%). See Section 4.5.3.2.2 and Table 4-24 for the functional description and value of Rp.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. Shield and GND grounds shall be connected within the USB Type-C and *USB 2.0* Standard-A plugs on both ends of the cable assembly.
6. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.5.2 USB Type-C 转 ***USB 2.0*** 标准 A 型电缆组件

图 3-25 显示了 USB Type-C 至 *USB 2.0* 标准 A 电缆组件。

图 3-25 USB Type-C 转 ***USB 2.0*** Standard-A 线缆组件

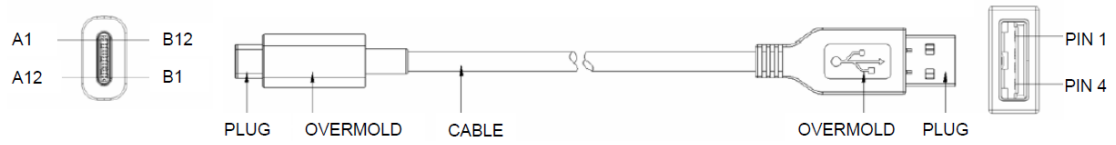


表 3-13 定义了 USB Type-C 至 *USB 2.0* 标准 A 电缆组件的线路连接。

表 3-13 USB Type-C 转 ***USB 2.0*** 标准 A 型电缆组件接线

USB Type-C Plug		Wire		USB 2.0 Standard-A plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
Shell	Shield	Outer shield	Shield	Shell	Shield

否注意事项：1. USB Type-C 插头的引脚 A5 (CC) 应通过电阻器 Rp (56 kΩ ± 5%) 连接到 VBUS。有关 Rp 的功能描述和值，请参阅第 4.5.3.2.2 节和表 4-24。2. USB Type-C 插头中不应存在触点 B6 和 B7。3. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起。此电缆中的 VBUS 引脚不需要旁路电容。4. 所有接地返回引脚应在 USB Type-C 插头内连接在一起。5. 屏蔽和 GND 接地应在电缆组件的两端的 USB Type-C 和 *USB 2.0* 标准 A 插头内连接。6. 本表未列出的所有 USB Type-C 插头引脚应处于开路（未连接）状态。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.5.3 USB Type-C to *USB 3.1* Standard-B Cable Assembly

Figure 3-26 shows a USB Type-C to *USB 3.1* Standard-B cable assembly.

Figure 3-26 USB Type-C to *USB 3.1* Standard-B Cable Assembly

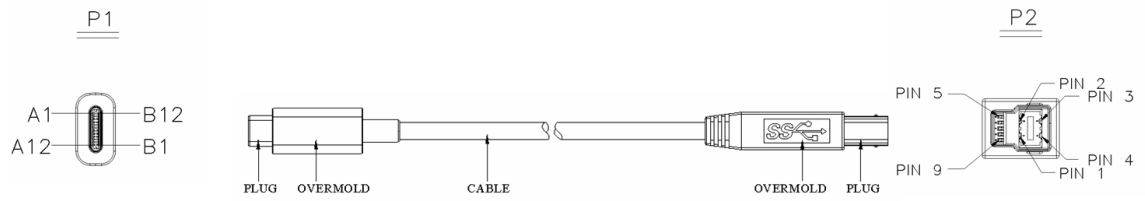


Table 3-14 defines the wire connections for the USB Type-C to *USB 3.1* Standard-B cable assembly.

Table 3-14 USB Type-C to *USB 3.1* Standard-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 3.1 Standard-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
A2	TXp1	5	SDPp1	9	StdB_SSRX+
A3	TXn1	6	SDPn1	8	StdB_SSRX–
B11	RXp1	8	SDPp2	6	StdB_SSTX+
B10	RXn1	9	SDPn2	5	StdB_SSTX–
Shell	Shield	Outer Shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-25 for the functional description and value of Rd.
2. This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present and the shields of the coaxial wires are connected to the ground pins.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor shall be 10nF ± 20% in cables which incorporate a USB Standard-B plug. The bypass capacitor shall be placed as close as possible to the power supply pad.
5. All Ground return pins shall be connected together within the USB Type-C plug.
6. Shield and GND grounds shall be connected within the USB Type-C and *USB 3.1* Standard-B plugs on both ends of the cable assembly.
7. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.5.3 USB Type-C 转 ***USB 3.1*** 标准 B 型电缆组件

图 3-26 显示了 USB Type-C 至 *USB 3.1* 标准 B 电缆组件。

图 3-26 USB Type-C 转 ***USB 3.1*** 标准 B 型线缆组件

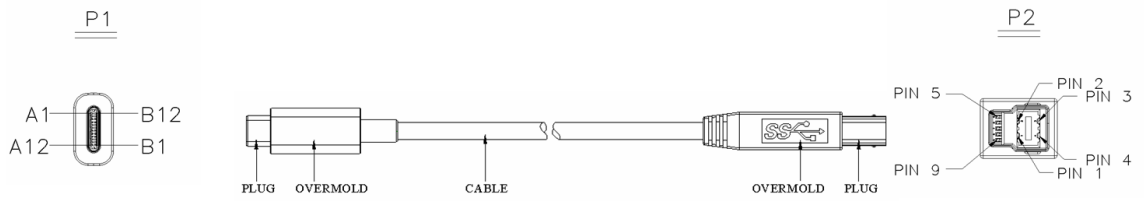


表 3-14 定义了 USB Type-C 至 *USB 3.1* 标准 B 电缆组件的线路连接。

表 3-14 USB Type-C 转 ***USB 3.1*** 标准 B 型电缆组件接线

USB Type-C Plug		Wire		USB 3.1 Standard-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
A2	TXp1	5	SDPp1	9	StdB_SSRX+
A3	TXn1	6	SDPn1	8	StdB_SSRX−
B11	RXp1	8	SDPp2	6	StdB_SSTX+
B10	RXn1	9	SDPn2	5	StdB_SSTX−
Shell	Shield	Outer Shield	Shield	Shell	Shield

注：1. USB Type-C 插头的引脚 A5 (CC) 应通过电阻器 Rd (5.1 kΩ ± 20%) 连接到 GND。有关 Rd 的功能描述和值，请参见第 4.5.3.2.1 节和表 4-25。2. 该表基于以下假设：所有 SDP 都使用屏蔽双绞线，并且存在排扰线。如果使用同轴线结构，则不存在排扰线，并且同轴线的屏蔽层连接到接地引脚。3. USB Type-C 插头中不应存在触点 B6 和 B7。4. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起。电缆的 USB Type-C 插头侧的 VBUS 和接地引脚之间需要一个旁路电容。在包含 USB 标准 B 插头的电缆中，旁路电容应为 10nF ± 20%。旁路电容应尽可能靠近电源焊盘放置。5. 所有接地返回引脚应在 USB Type-C 插头内连接在一起。6. 屏蔽和 GND 接地应在电缆组件两端的 USB Type-C 和 *USB 3.1* 标准 B 插头内连接。7. 本表未列出的所有 USB Type-C 插头引脚应处于开路状态（未连接）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.5.4 USB Type-C to *USB 2.0* Standard-B Cable Assembly

Figure 3-27 shows a USB Type-C to *USB 2.0* Standard-B cable assembly.

Figure 3-27 USB Type-C to *USB 2.0* Standard-B Cable Assembly

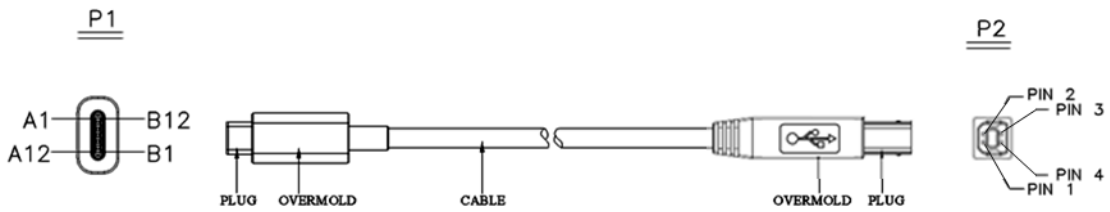


Table 3-15 defines the wire connections for the USB Type-C to *USB 2.0* Standard-B cable assembly.

Table 3-15 USB Type-C to *USB 2.0* Standard-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Standard-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-25 for the functional description and value of Rd.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. Shield and GND grounds shall be connected within the USB Type-C and *USB 2.0* Standard-B plugs on both ends of the cable assembly.
6. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.5.4 USB Type-C 转 ***USB 2.0*** 标准 B 型电缆组件

图 3-27 显示了 USB Type-C 至 *USB 2.0* 标准 B 电缆组件。

图 3-27 USB Type-C 转 ***USB 2.0*** 标准 B 型线缆组件

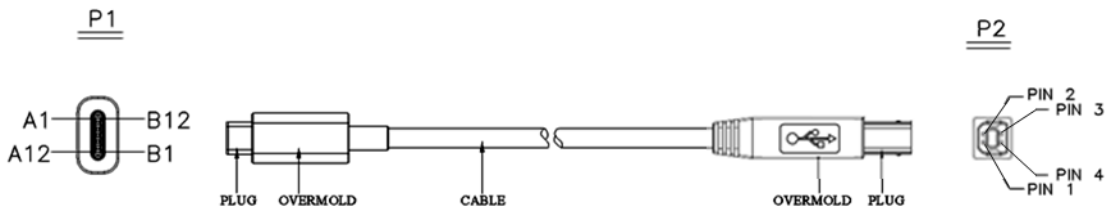


表 3-15 定义了 USB Type-C 至 *USB 2.0* 标准 B 电缆组件的线路连接。

表 3-15 USB Type-C 转 ***USB 2.0*** 标准 B 型电缆组件接线

USB Type-C Plug		Wire		USB 2.0 Standard-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
Shell	Shield	Outer shield	Shield	Shell	Shield

不 测试： 1. USB Type-C 插头的引脚 A5（CC）应通过电阻 Rd（5.1 kΩ ± 20%）连接到 GND。

有关 Rd 的功能描述和值，请参见第 4.5.3.2.1 节和表 4-25。2. USB Type-C 插头中不应存在触点 B6 和 B7。3. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起。此电缆中的 VBUS 引脚不需要旁路电容。4. 所有接地返回引脚应在 USB Type-C 插头内连接在一起。5. 屏蔽和 GND 接地应在电缆组件两端的 USB Type-C 和 *USB 2.0* 标准 B 插头内连接。6. 本表未列出的所有 USB Type-C 插头引脚都应开路（未连接）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.5.5 USB Type-C to *USB 2.0* Mini-B Cable Assembly

Figure 3-28 shows a USB Type-C to *USB 2.0* Mini-B cable assembly.

Figure 3-28 USB Type-C to *USB 2.0* Mini-B Cable Assembly

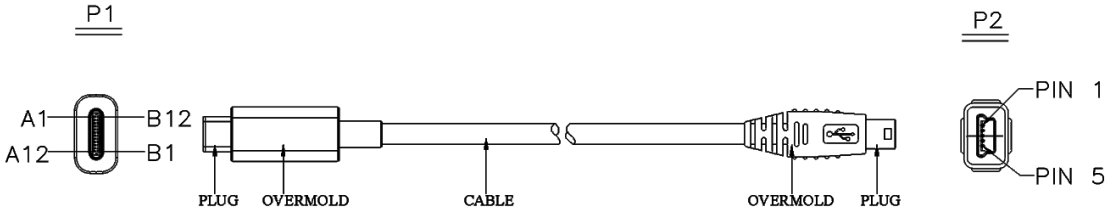


Table 3-16 defines the wire connections for the USB Type-C to *USB 2.0* Mini-B cable assembly.

Table 3-16 USB Type-C to *USB 2.0* Mini-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Mini-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-25 for the functional description and value of Rd.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. Pin 4 (ID) of the *USB 2.0* Mini-B plug shall be terminated as defined in the applicable specification for the cable type.
6. Shield and GND grounds shall be connected within the USB Type-C and *USB 2.0* Mini-B plugs on both ends of the cable assembly.
7. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.5.5 USB Type-C 转 *USB 2.0* Mini-B 线缆组件

图 3-28 显示了 USB Type-C 至 *USB 2.0* Mini-B 电缆组件。

图 3-28 USB Type-C 转 ***USB 2.0*** Mini-B 线缆组件

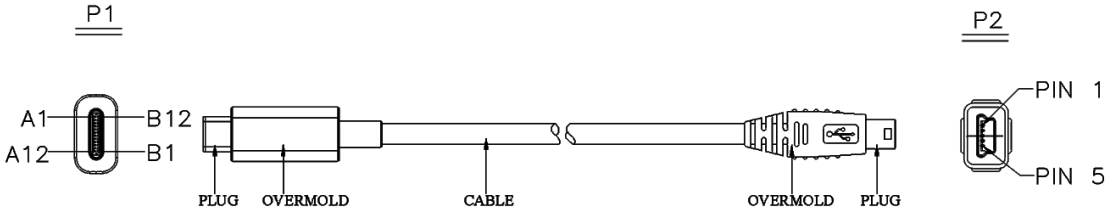


表 3-16 定义了 USB Type-C 至 *USB 2.0* Mini-B 电缆组件的线路连接。

表 3-16 USB Type-C 至 ***USB 2.0*** Mini-B 电缆组件接线

USB Type-C Plug		Wire		USB 2.0 Mini-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

注释：1. USB Type-C 插头的引脚 A5 应通过电阻器 Rd（5.1 kΩ ± 20%）连接到 GND。有关 Rd 的功能描述和值，请参见第 4.5.3.2.1 节和表 4-25。2. USB Type-C 插头中不应存在触点 B6 和 B7。3. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起。此电缆中的 VBUS 引脚不需要旁路电容。4. 所有接地返回引脚应在 USB Type-C 插头内连接在一起。5. *USB 2.0* Mini-B 插头的引脚 4（ID）应按照适用于该电缆类型的规范中的定义进行端接。6. 屏蔽层和 GND 接地应在电缆组件的两端的 USB Type-C 和 *USB 2.0* Mini-B 插头内连接。 7. 所有未在此表中列出的 USB Type-C 插头引脚均应处于开路状态（不连接）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.5.6 USB Type-C to *USB 3.1* Micro-B Cable Assembly

Figure 3-29 shows a USB Type-C to *USB 3.1* Micro-B cable assembly.

Figure 3-29 USB Type-C to *USB 3.1* Micro-B Cable Assembly

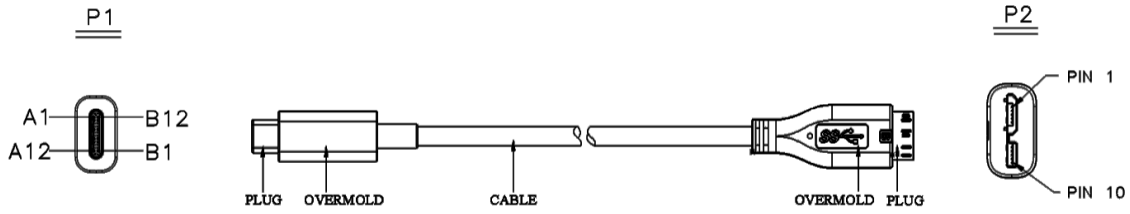


Table 3-17 defines the wire connections for the USB Type-C to *USB 3.1* Micro-B cable assembly.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.5.6 USB Type-C 转 ***USB 3.1*** Micro-B 电缆组件

图 3-29 展示了 USB Type-C 至 *USB 3.1* Micro-B 电缆组件。

图 3-29 USB Type-C 转 ***USB 3.1*** Micro-B 线缆组件

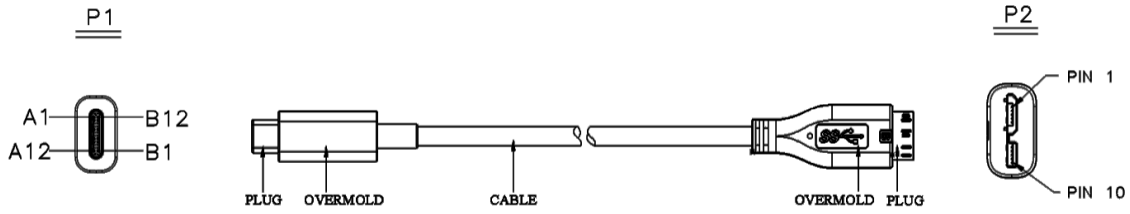


表 3-17 定义了 USB Type-C 至 *USB 3.1* Micro-B 电缆组件的线路连接。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-17 USB Type-C to *USB 3.1* Micro-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 3.1 Micro-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	5 8	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
A2	TXp1	5	SDPp1	10	MicB_SSRX+
A3	TXn1	6	SDPn1	9	MicB_SSRX−
B11	RXp1	8	SDPp2	7	MicB_SSTX+
B10	RXn1	9	SDPn2	6	MicB_SSTX−
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-25 for the functional description and value of Rd.
2. This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present and the shields of the coaxial wires are connected to the ground pins.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor shall be 10nF ± 20% in cables which incorporate a USB Micro-B plug. The bypass capacitor should be placed as close as possible to the power supply pad.
5. All Ground return pins shall be connected together within the USB Type-C plug.
6. Pin 4 (ID) of the *USB 3.1* Micro-B plug shall be terminated as defined in the applicable specification for the cable type.
7. Shield and GND grounds shall be connected within the USB Type-C and *USB 3.1* Micro-B plugs on both ends of the cable assembly.
8. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-17 USB Type-C 至 ***USB 3.1*** Micro-B 电缆组件接线

USB Type-C Plug		Wire		USB 3.1 Micro-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	5 8	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
A2	TXp1	5	SDPp1	10	MicB_SSRX+
A3	TXn1	6	SDPn1	9	MicB_SSRX−
B11	RXp1	8	SDPp2	7	MicB_SSTX+
B10	RXn1	9	SDPn2	6	MicB_SSTX−
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

不 测试： 1. USB Type-C 插头的引脚 A5（CC）应通过电阻 Rd（5.1 kΩ ± 20%）连接到 GND。

有关 Rd 的功能描述和值，请参见第 4.5.3.2.1 节和表 4-25。2. 此表基于以下假设：所有 SDP 都使用屏蔽双绞线，并且有排扰线。如果使用同轴线结构，则不存在排扰线，并且同轴线的屏蔽层连接到接地引脚。3. USB Type-C 插头中不应存在触点 B6 和 B7。4. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起。电缆的 USB Type-C 插头侧的 VBUS 和接地引脚之间需要一个旁路电容。在包含 USB Micro-B 插头的电缆中，旁路电容应为 10nF ± 20%。旁路电容应尽可能靠近电源焊盘。5. 所有接地返回引脚应在 USB Type-C 插头内连接在一起。 6. *USB 3.1* Micro-B 插头的引脚 4 (ID) 应按照电缆类型适用规范中的定义进行端接。 7. 屏蔽层和 GND 接地应在电缆组件两端的 USB Type-C 和 *USB 3.1* Micro-B 插头内连接。 8. 本表未列出的所有 USB Type-C 插头引脚均应处于开路状态（未连接）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.5.7 USB Type-C to *USB 2.0* Micro-B Cable Assembly

Figure 3-30 shows a USB Type-C to *USB 2.0* Micro-B cable assembly.

Figure 3-30 USB Type-C to *USB 2.0* Micro-B Cable Assembly

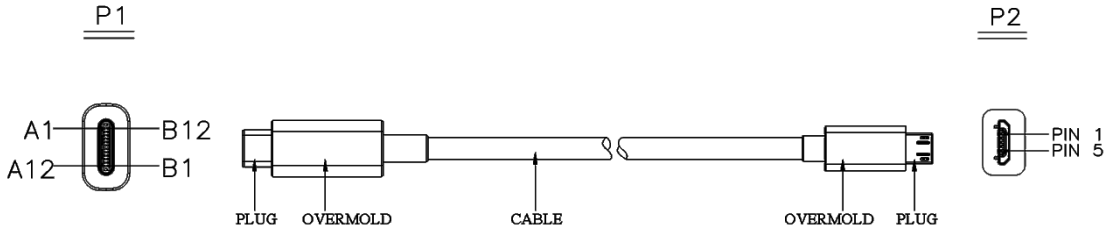


Table 3-18 defines the wire connections for the USB Type-C to *USB 2.0* Micro-B cable assembly.

Table 3-18 USB Type-C to *USB 2.0* Micro-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Micro-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-25 for the functional description and value of Rd.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. Pin 4 (ID) of the *USB 2.0* Micro-B plug shall be terminated as defined in the applicable specification for the cable type.
6. Shield and GND grounds shall be connected within the USB Type-C and *USB 2.0* Micro-B plugs on both ends of the cable assembly.
7. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.5.7 USB Type-C 转 *USB 2.0* Micro-B 线缆组件

图 3-30 展示了 USB Type-C 至 *USB 2.0* Micro-B 电缆组件。

图 3-30 USB Type-C 转 ***USB 2.0*** Micro-B 线缆组件

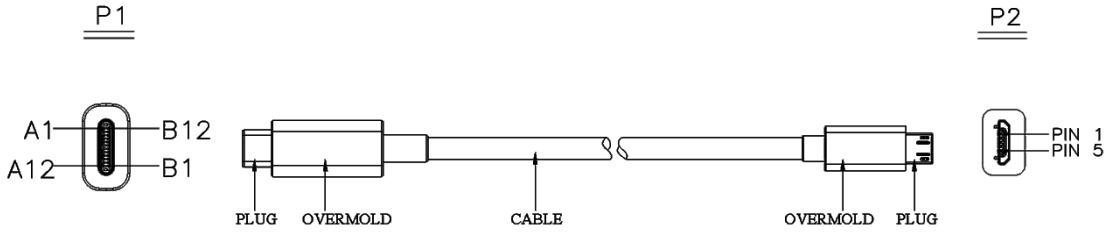


表 3-18 定义了 USB Type-C 至 *USB 2.0* Micro-B 电缆组件的线路连接。

表 3-18 USB Type-C 至 ***USB 2.0*** Micro-B 电缆组件接线

USB Type-C Plug		Wire		USB 2.0 Micro-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

否注意： 1. USB Type-C 插头的引脚 A5（CC）应通过电阻器 Rd（5.1 kΩ ± 20%）连接到 GND。

有关 Rd 的功能描述和值，请参见第 4.5.3.2.1 节和表 4-25。2. USB Type-C 插头中不应存在触点 B6 和 B7。3. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起。此电缆中的 VBUS 引脚不需要旁路电容。4. 所有接地返回引脚应在 USB Type-C 插头内连接在一起。5. *USB 2.0* Micro-B 插头的引脚 4（ID）应按照电缆类型的适用规范中的定义进行端接。6. 屏蔽和 GND 接地应在电缆组件的两端的 USB Type-C 和 *USB 2.0* Micro-B 插头内连接。7. 本表未列出的所有 USB Type-C 插头引脚应处于开路（未连接）状态。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.6 Legacy Adapter Assemblies

To enable interoperability between USB Type-C-based products and legacy USB products, the following standard legacy adapter assemblies are defined. Only the adapter assemblies defined in this specification are allowed.

3.6.1 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly

Figure 3-31 shows a USB Type-C to *USB 3.1* Standard-A receptacle adapter assembly. This cable assembly is defined for direct connect to a USB device (e.g., a thumb drive). System functionality of using this adaptor assembly together with another USB cable assembly is not guaranteed.

Figure 3-31 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly

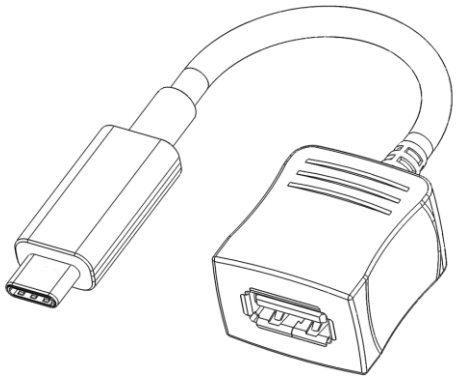


Table 3-19 defines the wire connections for the USB Type-C to *USB 3.1* Standard-A receptacle adapter assembly.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.6 旧式适配器组件

为了实现基于 USB Type-C 的产品与传统 USB 产品之间的互操作性，定义了以下标准传统适配器组件。仅允许使用本规范中定义的适配器组件。

3.6.1 USB Type-C 至 ***USB 3.1*** 标准 A 型插座适配器组件

图 3-31 显示了 USB Type-C 转 *USB 3.1* 标准 A 插座适配器组件。此电缆组件用于直接连接到 USB 设备（例如拇指驱动器）。无法保证将此适配器组件与另一个 USB 电缆组件一起使用时的系统功能。

图 3-31 USB Type-C 转 ***USB 3.1*** 标准 A 型插座适配器组件

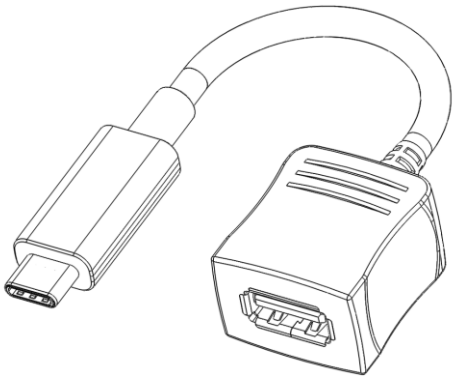


表 3-19 定义了 USB Type-C 至 *USB 3.1* 标准 A 插座适配器组件的线路连接。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-19 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly Wiring

USB Type-C Plug		USB 3.1 Standard-A receptacle	
Pin	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	1	VBUS
A5	CC	See Note 1	
B5	VCONN		
A6	Dp1	3	D+
A7	Dn1	2	D–
A2	TXp1	9	StdA_SSTX+
A3	TXn1	8	StdA_SSTX–
B11	RXp1	6	StdA_SSRX+
B10	RXn1	5	StdA_SSRX–
Shell	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-25 for the functional description and value of Rd.
2. This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present and the shields of the coaxial wires are connected to the ground pins.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A 10 nF bypass capacitor is required for the VBUS pin in the USB Type-C plug end of the cable. The bypass capacitor should be placed as close as possible to the power supply pad. A bypass capacitor is not required for the VBUS pin in the Standard-A receptacle.
5. All Ground return pins shall be connected together within the USB Type-C plug.
6. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-19 USB Type-C 至 ***USB 3.1*** 标准 A 型插座适配器组件接线

USB Type-C Plug		USB 3.1 Standard-A receptacle	
Pin	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	1	VBUS
A5	CC	See Note 1	
B5	VCONN		
A6	Dp1	3	D+
A7	Dn1	2	D−
A2	TXp1	9	StdA_SSTX+
A3	TXn1	8	StdA_SSTX−
B11	RXp1	6	StdA_SSRX+
B10	RXn1	5	StdA_SSRX−
Shell	Shield	Shell	Shield

笔记：

1. USB Type-C 插头的引脚 A5 (CC) 应通过电阻 Rd (5.1 kΩ ± 20%) 连接到 GND。有关 Rd 的功能描述和值，请参阅第 4.5.3.2.1 节和表 4-25。 2. 此表基于以下假设：所有 SDP 均使用屏蔽双绞线，并且有排扰线。如果使用同轴线结构，则不存在排扰线，同轴线的屏蔽层连接到接地引脚。 3. USB Type-C 插头中不应存在触点 B6 和 B7。 4. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起。电缆的 USB Type-C 插头端的 VBUS 引脚需要 10 nF 旁路电容。旁路电容应尽可能靠近电源焊盘放置。标准 A 插座中的 VBUS 引脚不需要旁路电容。 5. 所有接地返回引脚均应在 USB Type-C 插头内连接在一起。 6. 本表未列出的所有 USB Type-C 插头引脚均应开路（不连接）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.6.2 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly

Figure 3-31 shows a USB Type-C to *USB 2.0* Micro-B receptacle adapter assembly.

Figure 3-32 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly

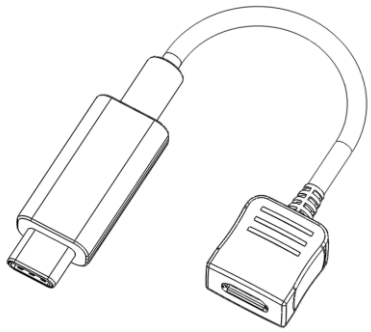


Table 3-19 defines the wire connections for the USB Type-C to *USB 2.0* Micro-B receptacle adapter assembly.

Table 3-20 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly Wiring

USB Type-C Plug		USB 2.0 Micro-B receptacle	
Pin	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	5	GND
A4, B4, A9, B9	VBUS	1	VBUS
A5	CC	See Note 1	
A6	Dp1	3	D+
A7	Dn1	2	D–
		4	ID
Shell	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to VBUS through a resistor Rp (56 kΩ ± 5%). See Section 4.5.3.2.2 and Table 4-24 for the functional description and value of Rp.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins at the Micro-B receptacle end of this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.6.2 USB Type-C 至 ***USB 2.0*** Micro-B 插座适配器组件

图 3-31 展示了 USB Type-C 至 *USB 2.0* Micro-B 插座适配器组件。

图 3-32 USB Type-C 转 ***USB 2.0*** Micro-B 插座适配器组件

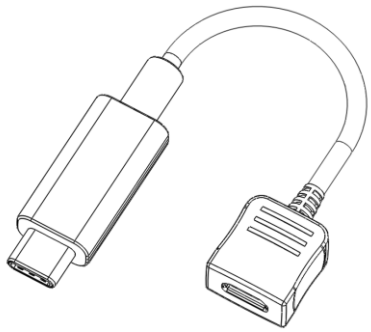


表 3-19 定义了 USB Type-C 至 *USB 2.0* Micro-B 插座适配器组件的线路连接。

表 3-20 USB Type-C 至 ***USB 2.0*** Micro-B 插座适配器组件接线

USB Type-C Plug		USB 2.0 Micro-B receptacle	
Pin	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	5	GND
A4, B4, A9, B9	VBUS	1	VBUS
A5	CC	See Note 1	
A6	Dp1	3	D+
A7	Dn1	2	D−
		4	ID
Shell	Shield	Shell	Shield

笔记：

1. USB Type-C 插头的 A5 引脚 (CC) 应通过电阻 Rp (56 kΩ ± 5%) 连接到 VBUS。有关 Rp 的功能描述和值，请参阅第 4.5.3.2.2 节和表 4-24。2. USB Type-C 插头中不应存在触点 B6 和 B7。3. 所有 VBUS 引脚应在 USB Type-C 插头内连接在一起。此电缆的 Micro-B 插座端的 VBUS 引脚无需旁路电容器。4. 所有 Gr

圆形返回引脚应在 USB 类型内连接在一起 -C 插头。 5. 本表未列出的所有 USB Type-C 插头引脚均应开路（不连接）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.7 Electrical Characteristics

This section defines the USB Type-C raw cable, connector, and cable assembly electrical requirements, including signal integrity, shielding effectiveness, and DC requirements. Chapter 4 defines additional requirements regarding functional signal definition, host/device discovery and configuration, and power delivery.

Unless otherwise specified, all measurements are made at a temperature of 15° to 35° C, a relative humidity of 25% to 85%, and an atmospheric pressure of 86 to 106 kPa and all S-parameters are normalized with an 85 Ω differential impedance.

3.7.1 Raw Cable (Informative)

Informative raw cable electrical performance targets are provided to help cable assembly manufacturers manage the procurement of raw cable. These targets are not part of the USB Type-C compliance requirements. The normative requirement is that the cable assembly meets the performance characteristics specified in Sections 3.7.2 and 3.7.5.3.

The differential characteristic impedance for shielded differential pairs is recommended to be 90 Ω ± 5 Ω. The single-ended characteristic impedance of coaxial wires is recommended to be 45 Ω ± 3 Ω. The impedance should be evaluated using a 200 ps (10%-90%) rise time; a faster rise time is not necessary for raw cable since it will make cable test fixture discontinuities more prominent.

3.7.1.1 Intra-Pair Skew (Informative)

The intra-pair skew for a differential pair is recommended to be less than 10 ps/m. It should be measured with a Time Domain Transmission (TDT) in a differential mode using a 200 ps (10%-90%) rise time with a crossing at 50% of the input voltage.

3.7.1.2 Differential Insertion Loss (Informative)

Cable loss depends on wire gauges, plating and dielectric materials. Table 3-21 and Table 3-22 show examples of differential insertion losses.

Table 3-21 Differential Insertion Loss Examples for TX/RX with Twisted Pair Construction

Frequency	34AWG	32AWG	30AWG	28AWG
0.625 GHz	−1.8 dB/m	−1.4 dB/m	−1.2 dB/m	−1.0 dB/m
1.25 GHz	−2.5 dB/m	−2.0 dB/m	−1.7 dB/m	−1.4 dB/m
2.50 GHz	−3.7 dB/m	−2.9 dB/m	−2.5 dB/m	−2.1 dB/m
5.00 GHz	−5.5 dB/m	−4.5 dB/m	−3.9 dB/m	−3.1 dB/m
7.50 GHz	−7.0 dB/m	−5.9 dB/m	−5.0 dB/m	−4.1 dB/m
10.00 GHz	−8.4 dB/m	−7.2 dB/m	−6.1 dB/m	−4.8 dB/m
12.50 GHz	−9.5 dB/m	−8.2 dB/m	−7.3 dB/m	−5.5 dB/m
15.00 GHz	−11.0 dB/m	−9.5 dB/m	−8.7 dB/m	−6.5 dB/m

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.7 电气特性

本节定义了 USB Type-C 原始电缆、连接器和电缆组件的电气要求，包括信号完整性、屏蔽效能和直流要求。第 4 章定义了有关功能信号定义、主机/设备发现和配置以及电力输送的其他要求。

除非另有说明，所有测量均在温度为 15° 至 35° C、相对湿度为 25% 至 85% 以及大气压力为 86 至 106 kPa 的条件下进行，并且所有 S 参数均采用 85 Ω 差分阻抗进行标准化。

3.7.1 原始电缆（参考资料）

提供信息丰富的原始电缆电气性能目标，以帮助电缆组件制造商管理原始电缆的采购。这些目标不属于 USB Type-C 合规性要求。规范要求是电缆组件满足第 3.7.2 节和第 3.7.5.3 节中规定的性能特性。

建议屏蔽差分对的差分特性阻抗为 90 Ω ± 5 Ω。建议同轴电缆的单端特性阻抗为 45 Ω ± 3 Ω。应使用 200 ps (10%-90%) 上升时间评估阻抗；对于原始电缆，不需要更快的上升时间，因为这会使电缆测试夹具的不连续性更加突出。

3.7.1.1 对内偏差（信息性）

建议差分对的对内偏移小于 10 ps/m。应使用差分模式下的时间域传输 (TDT) 测量，使用 200 ps (10%-90%) 上升时间，交叉点为输入电压的 50%。

3.7.1.2 差分插入损耗（参考资料）

电缆损耗取决于线规、镀层和介电材料。表 3-21 和表 3-22 显示了差分插入损耗的示例。

表 3-21 采用双绞线结构的 TX/RX 差分插入损耗示例

Frequency	34AWG	32AWG	30AWG	28AWG
0.625 GHz	−1.8 dB/m	−1.4 dB/m	−1.2 dB/m	−1.0 dB/m
1.25 GHz	−2.5 dB/m	−2.0 dB/m	−1.7 dB/m	−1.4 dB/m
2.50 GHz	−3.7 dB/m	−2.9 dB/m	−2.5 dB/m	−2.1 dB/m
5.00 GHz	−5.5 dB/m	−4.5 dB/m	−3.9 dB/m	−3.1 dB/m
7.50 GHz	−7.0 dB/m	−5.9 dB/m	−5.0 dB/m	−4.1 dB/m
10.00 GHz	−8.4 dB/m	−7.2 dB/m	−6.1 dB/m	−4.8 dB/m
12.50 GHz	−9.5 dB/m	−8.2 dB/m	−7.3 dB/m	−5.5 dB/m
15.00 GHz	−11.0 dB/m	−9.5 dB/m	−8.7 dB/m	−6.5 dB/m

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-22 Differential Insertion Loss Examples for USB TX/RX with Coaxial Construction

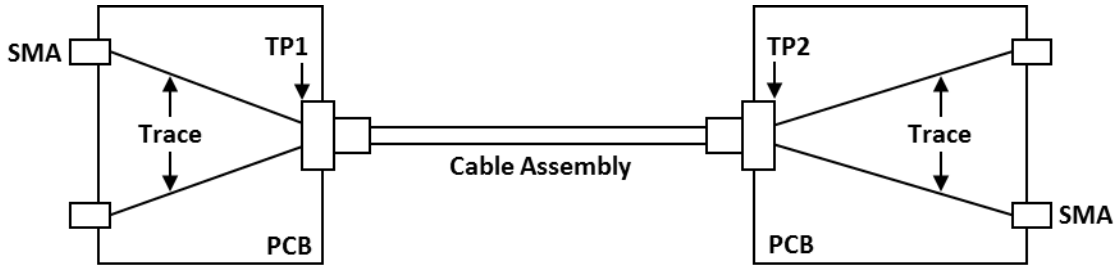
Frequency	34AWG	32AWG	30AWG	28AWG
0.625 GHz	−1.8 dB/m	−1.5 dB/m	−1.2 dB/m	−1.0 dB/m
1.25 GHz	−2.8 dB/m	−2.2 dB/m	−1.8 dB/m	−1.3 dB/m
2.50 GHz	−4.2 dB/m	−3.4 dB/m	−2.7 dB/m	−1.9 dB/m
5.00 GHz	−6.1 dB/m	−4.9 dB/m	−4.0 dB/m	−3.1 dB/m
7.50 GHz	−7.6 dB/m	−6.5 dB/m	−5.2 dB/m	−4.2 dB/m
10.0 GHz	−8.8 dB/m	−7.6 dB/m	−6.1 dB/m	−4.9 dB/m
12.5 GHz	−9.9 dB/m	−8.6 dB/m	−7.1 dB/m	−5.7 dB/m
15.0 GHz	−12.1 dB/m	−10.9 dB/m	−9.0 dB/m	−6.5 dB/m

3.7.2 USB Type-C to Type-C Passive Cable Assemblies (Normative)

A USB Type-C to Type-C cable assembly shall be tested using a test fixture with the receptacle tongue fabricated in the test fixture. This is illustrated in Figure 3-33. The USB Type-C receptacles are not present in the test fixture. Hosts and devices should account for the additional signal degradation the receptacle introduces.

The requirements are for the entire signal path of the cable assembly mated with the fixture PCB tongues, not including lead-in PCB traces. As illustrated in Figure 3-33, the measurement is between TP1 (test point 1) and TP2 (test point 2). Refer to documentation located at Cables and Connectors page on the USB-IF website for a detailed description of a standardized test fixture.

Figure 3-33 Illustration of Test Points for a Mated Cable Assembly



The cable assembly requirements are divided into informative and normative requirements. The informative requirements are provided as design targets for cable assembly manufacturers. The normative requirements are the pass/failure criteria for cable assembly compliance.

3.7.2.1 Recommended TX/RX Passive Cable Assembly Characteristics (USB 3.2 Gen2 and USB4 Gen2)

The recommended electrical characteristics defined in this section are informative design guidelines. Cable assemblies that do not meet these recommended electrical characteristics may still pass USB certification testing. Similarly, cable assemblies that meet these recommended electrical characteristics may or may not pass USB certification testing.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-22 同轴结构 USB TX/RX 差分插入损耗示例

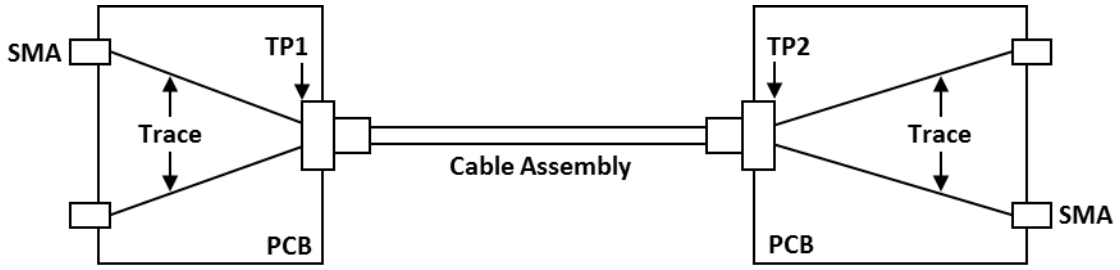
Frequency	34AWG	32AWG	30AWG	28AWG
0.625 GHz	−1.8 dB/m	−1.5 dB/m	−1.2 dB/m	−1.0 dB/m
1.25 GHz	−2.8 dB/m	−2.2 dB/m	−1.8 dB/m	−1.3 dB/m
2.50 GHz	−4.2 dB/m	−3.4 dB/m	−2.7 dB/m	−1.9 dB/m
5.00 GHz	−6.1 dB/m	−4.9 dB/m	−4.0 dB/m	−3.1 dB/m
7.50 GHz	−7.6 dB/m	−6.5 dB/m	−5.2 dB/m	−4.2 dB/m
10.0 GHz	−8.8 dB/m	−7.6 dB/m	−6.1 dB/m	−4.9 dB/m
12.5 GHz	−9.9 dB/m	−8.6 dB/m	−7.1 dB/m	−5.7 dB/m
15.0 GHz	−12.1 dB/m	−10.9 dB/m	−9.0 dB/m	−6.5 dB/m

3.7.2 USB Type-C 至 Type-C 无源电缆组件（规范）

USB Type-C 转 Type-C 电缆组件应使用测试夹具进行测试，测试夹具中装有插座舌片。如图 3-33 所示。测试夹具中没有 USB Type-C 插座。主机和设备应考虑插座带来的额外信号衰减。

这些要求适用于与夹具 PCB 舌片配合的电缆组件的整个信号路径，不包括引入 PCB 走线。如图 3-33 所示，测量位于 TP1（测试点 1）和 TP2（测试点 2）之间。有关标准化测试夹具的详细说明，请参阅 USB-IF 网站上的电缆和连接器页面中的文档。

图 3-33 已配接电缆组件的测试点图示



电缆组件要求分为信息性要求和规范性要求。信息性要求是作为电缆组件制造商的设计目标提供的。规范性要求是电缆组件合规性的通过/失败标准。

3.7.2.1 建议的 TX/RX 无源电缆组件特性（USB 3.2 Gen2 和 USB4 Gen2）

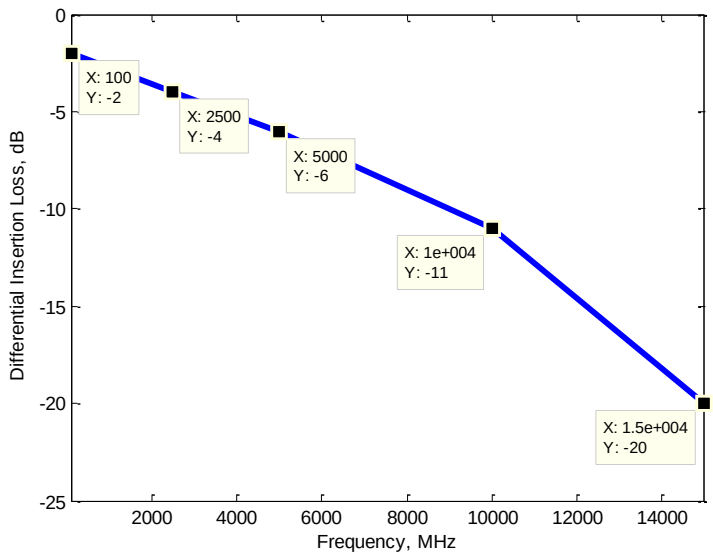
本节中定义的推荐电气特性仅供参考。不符合这些推荐电气特性的电缆组件仍可能通过 USB 认证测试。同样，符合这些推荐电气特性的电缆组件也可能通过或无法通过 USB 认证测试。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.7.2.1.1 Differential Insertion Loss (Informative – USB 3.2 Gen2 and USB4 Gen2)

Figure 3-34 shows the differential insertion loss limit for a *USB 3.2* Gen2 or a *USB4* Gen2 Type-C cable assembly, which is defined by the following vertices: (100 MHz, −2 dB), (2.5 GHz, −4 dB), (5.0 GHz, −6 dB), (10 GHz, −11 dB) and (15 GHz, −20 dB).

Figure 3-34 Recommended Differential Insertion Loss Requirement (USB 3.2 Gen2 and USB4 Gen2)



3.7.2.1.2 Differential Return Loss (Informative – USB 3.2 Gen2 and USB4 Gen2)

Figure 3-35 shows the differential return loss limit, which is defined by the following equation:

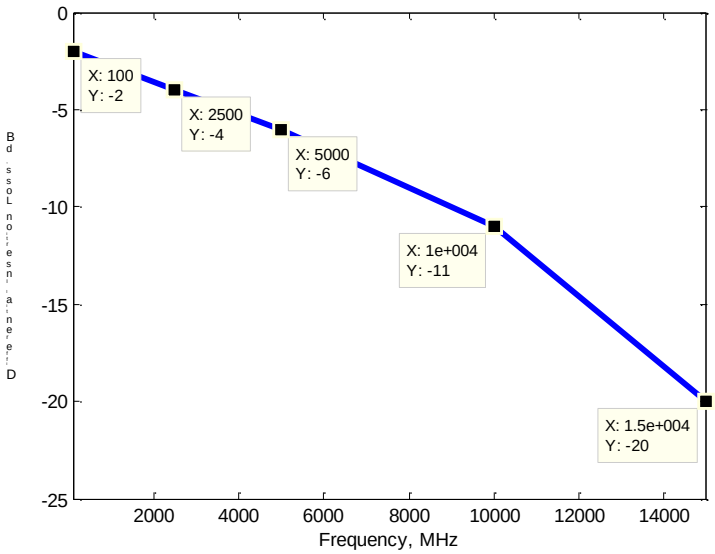
$$RL\ mask = \begin{cases} -18\ dB,\ f < 5\ Ghz \\ -18 + 45.43 \times \log_{10}\left(\frac{f}{5}\right)\ dB\ ,\ 5\ Ghz < f\ \leq 7.5\ Ghz \\ -15 + \frac{2}{3} \times f\ dB,\ 7.5\ Ghz < f \leq 15\ Ghz \end{cases}$$

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

差分插入损耗（信息 - USB 3.2 Gen2 和 USB4 Gen2）

图 3-34 显示了 *USB 3.2* Gen2 或 *USB4* Gen2 Type-C 电缆组件的差分插入损耗限值，由以下顶点定义：(100 MHz, −2 dB)、(2.5 GHz, −4 dB)、(5.0 GHz, −6 dB)、(10 GHz, −11 dB) 和 (15 GHz, −20 dB)。

图 3-34 建议差分插入损耗要求（USB 3.2 Gen2 和 USB4 Gen2）



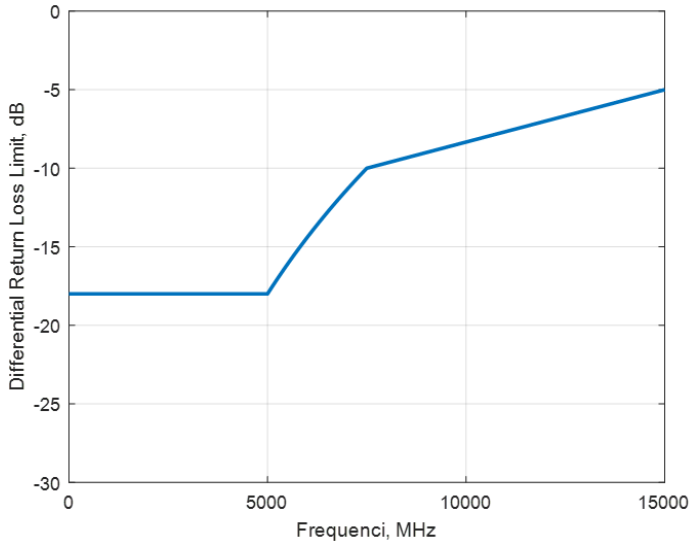
3.7.2.1.2 差分回波损耗（参考 - USB 3.2 Gen2 和 USB4 Gen2）

图 3-35 显示了差分回波损耗限值，该限值由以下公式定义：

$$RL\ mask = \begin{cases} -18\ dB,\ f < 5\ Ghz \\ -18 + 45.43 \times \log_{10}\left(\frac{f}{5}\right)\ dB\ ,\ 5\ Ghz < f\ \leq 7.5\ Ghz \\ -15 + \frac{2}{3} \times f\ dB,\ 7.5\ Ghz < f \leq 15\ Ghz \end{cases}$$

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

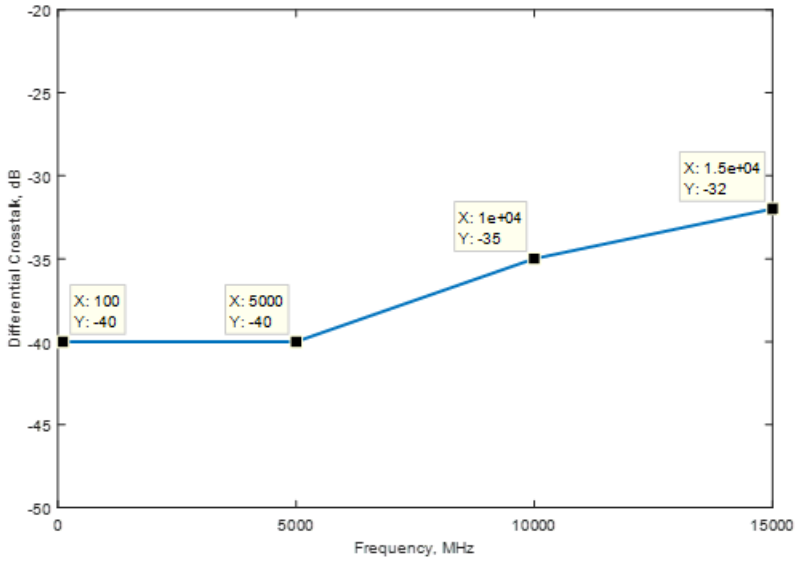
Figure 3-35 Recommended Differential Return Loss Requirement



3.7.2.1.3 Differential Near-End and Far-End Crosstalk between TX/RX Pairs (Informative – USB 3.2 Gen2 and USB4 Gen2)

Both the near-end crosstalk (DDNEXT) and far-end crosstalk (DDFEXT) are specified, as shown in Figure 3-36. The DDNEXT/DDFEXT limits are defined by the following vertices: (100 MHz, −40 dB), (5 GHz, −40 dB), (10 GHz, −35 dB), and (15 GHz, −32 dB).

Figure 3-36 Recommended Differential Crosstalk Requirement

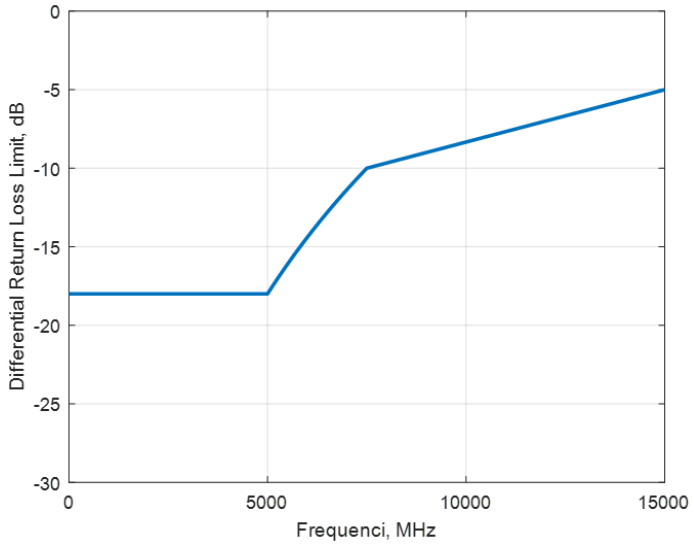


3.7.2.1.4 Differential Crosstalk between USB D+/D− and TX/RX Pairs (Informative – USB 3.2 Gen2 and USB4 Gen2)

The differential near-end and far-end crosstalk between the USB D+/D− pair and the TX/RX pairs should be managed not to exceed the limits shown in Figure 3-37. The USB D+/D− pair and the TX/RX pairs should be considered in the context of both an aggressor and a victim. It should also be considered that the D+/D− pair maximum frequency for similar tests is

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

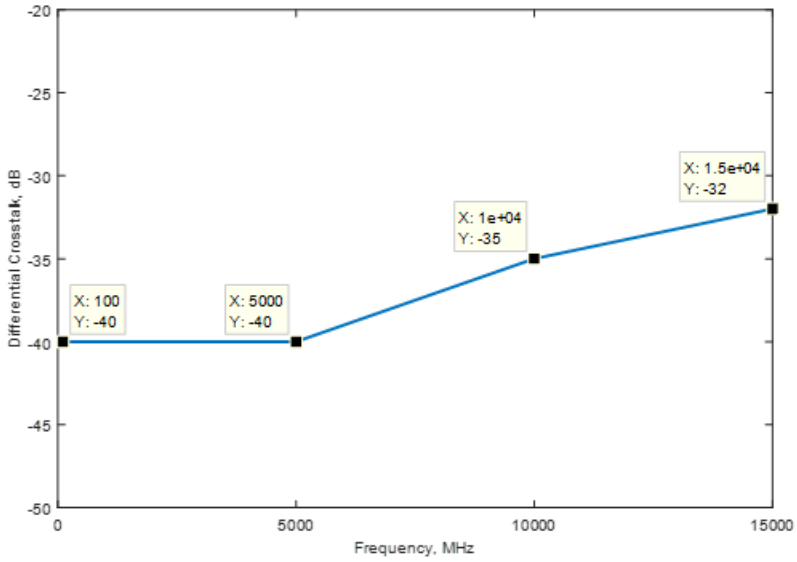
图 3-35 建议差分回波损耗要求



3.7.2.1.3 TX/RX 对之间的差分近端和远端串扰（信息 - USB 3.2 Gen2 和 USB4 Gen2）

近端串扰 (DDNEXT) 和远端串扰 (DDFEXT) 均有规定，如图 3-36 所示。DDNEXT/DDFEXT 限值由以下顶点定义：(100 MHz，−40 dB)、(5 GHz，−40 dB)、(10 GHz，−35 dB) 和 (15 GHz，−32 dB)。

数字　3-36 推荐差分串扰要求　　关管理



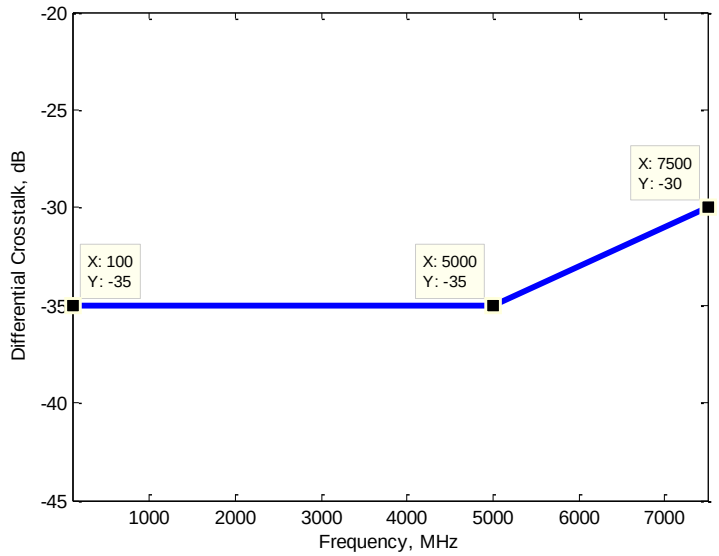
3.7.2.1.4 USB D+/D− 和 TX/RX 对之间的差分串扰（信息 - USB 3.2 Gen2 和 USB4 Gen2）

USB D+/D− 对和 TX/RX 对之间的差分近端和远端串扰应控制在不超过图 3-37 所示的限值。USB D+/D− 对和 TX/RX 对应在攻击者和受害者的背景下考虑。还应考虑 D+/D− 对进行类似测试的最大频率为

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

1.2 GHz (see Table 3-31), but in this case the crosstalk on the D+/D− pair is extended to 7.5 GHz. The limits are defined by the following points: (100 MHz, −35 dB), (5 GHz, −35 dB), and (7.5 GHz, −30 dB).

Figure 3-37 Recommended Differential Near-End and Far-End Crosstalk Requirement between USB D+/D− Pair and TX/RX Pair

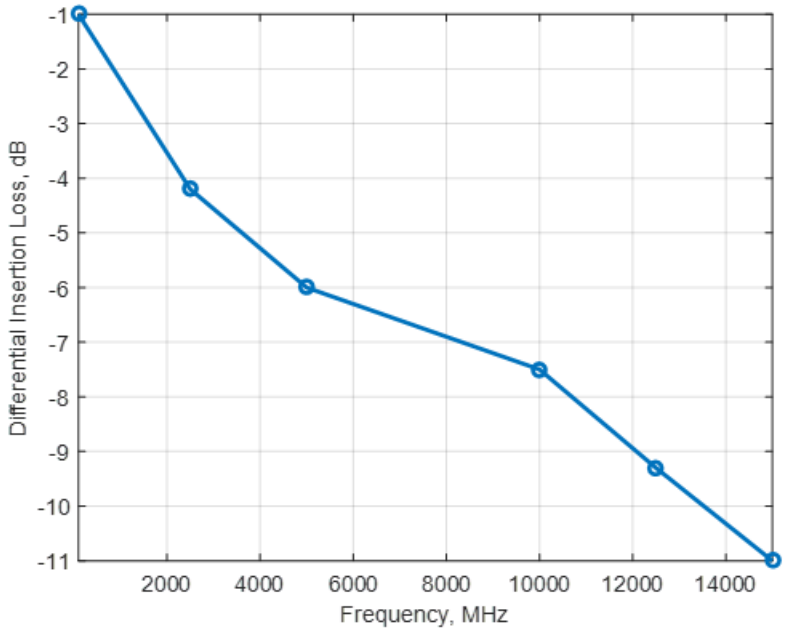


3.7.2.2 Recommended TX/RX Passive Cable Assembly Characteristics (USB4 Gen3)

3.7.2.2.1 Differential Insertion Loss (Informative – USB4 Gen3)

Figure 3-38 shows the recommended differential insertion loss limit for a *USB4* Gen3 Type-C cable assembly, which is defined by the following vertices: (100 MHz, −1 dB), (2.5 GHz, −4.2 dB), (5.0 GHz, −6 dB), (10 GHz, −7.5 dB), (12 GHz, −9.3 dB), and (15 GHz, −11 dB).

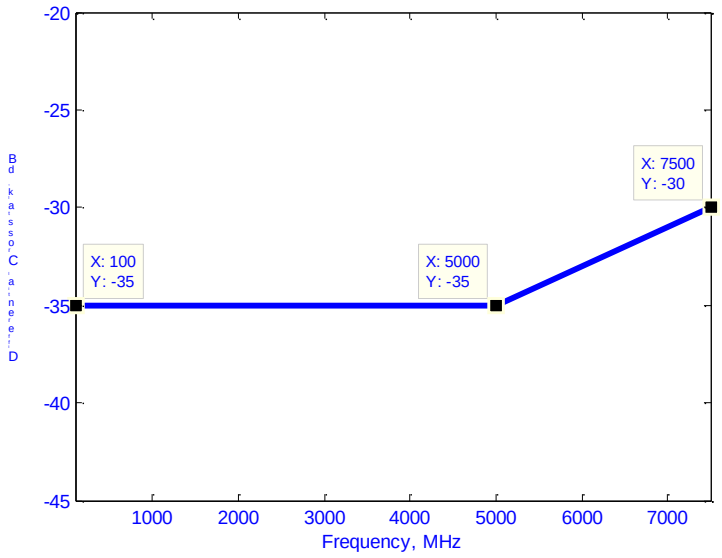
Figure 3-38 Recommended Differential Insertion Loss Requirement (USB4 Gen3)



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

1.2 GHz（见表 3-31），但在这种情况下，D+/D− 对上的串扰扩展到 7.5 GHz。限制由以下点定义：（100 MHz，−35 dB）、（5 GHz，−35 dB）和（7.5 GHz，−30 dB）。

图 3-37 USB D+/D− 对和 TX/RX 对之间的差分近端和远端串扰建议要求

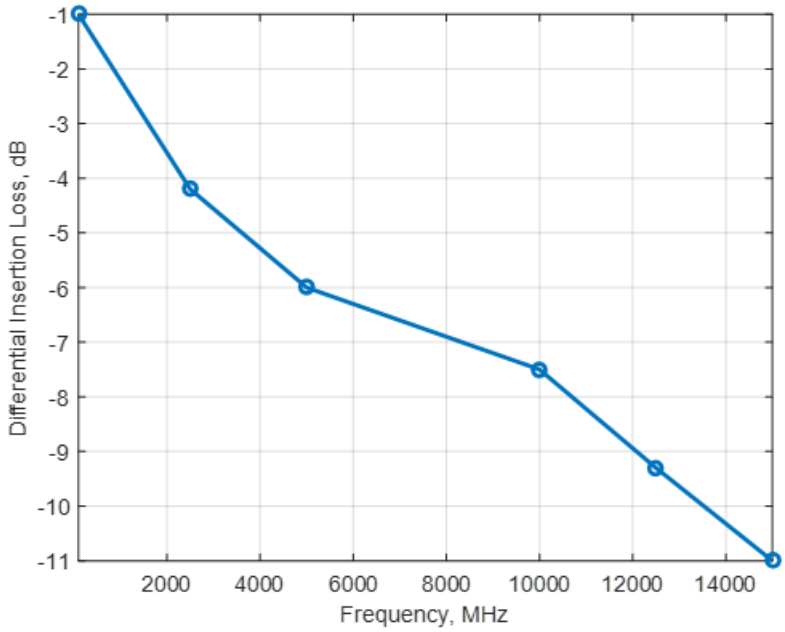


3

.7.2.2 建议的 TX/RX 无源电缆组件特性（USB4 Gen3） 3.7.2.2.1 差分插入损耗（信息 - USB4 Gen3）

图 3-38 显示了 *USB4* Gen3 Type-C 电缆组件的推荐差分插入损耗限值，该限值由以下顶点定义：(100 MHz，－1 dB)、(2.5 GHz，−4.2 dB)、(5.0 GHz，−6 dB)、(10 GHz，−7.5 dB)、(12 GHz，−9.3 dB) 和 (15 GHz，−11 dB)。

图 3-38 建议差分插入损耗要求（USB4 Gen3）



版权所有 © 2019 USB 3.0 Promoter Group。保留所有权利。

3.7.2.2.2 Differential Return Loss (Informative – USB4 Gen3)

The informative differential return loss mask is identical in Section 3.7.2.1.2.

3.7.2.2.3 Differential Near-End and Far-End Crosstalk between TX/RX Pairs (Informative – USB4 Gen3)

The recommended near-end crosstalk (DDNEXT) and far-end crosstalk (DDFEXT) are defined in Section 3.7.2.1.3. To minimize crosstalk, it is important to optimize the paddle card and wire termination designs inside the cable plug.

3.7.2.2.4 Differential Crosstalk between USB D+/D− and TX/RX Pairs (Informative – USB4 Gen3)

The informative near-end and far-end crosstalk between the USB D+/D− pair and the TX/RX pairs are the same as in Section 3.7.2.1.4.

3.7.2.3 Normative TX/RX Passive Cable Assembly Requirements (USB 3.2 Gen2 and USB4 Gen2)

The integrated parameters are used for cable assembly compliance (except for insertion loss and differential-to-common-mode conversion) to avoid potential rejection of a functioning cable assembly that may fail the traditional S-parameters spec at a few frequencies.

3.7.2.3.1 Insertion Loss Fit at Nyquist Frequencies (Normative – USB 3.2 Gen2 and USB4 Gen2)

The insertion loss fit at Nyquist frequency measures the attenuation of the cable assembly. To obtain the insertion loss fit at Nyquist frequency, the measured cable assembly differential insertion loss is fitted with a smooth function. A standard fitting algorithm and tool shall be used to extract the insertion loss fit at Nyquist frequencies. The fitting equation is defined by the following equation:

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3}$$

where f is the frequency and a, b, c, and d are the fitting coefficients.

Figure 3-39 illustrates an example of a measured cable assembly insertion loss fitted with a smooth function; the insertion loss fit at the Nyquist frequency of SuperSpeed USB Gen2 (5.0 GHz) is −5.8 dB.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.7.2.2.2 差分回波损耗（参考 - USB4 Gen3）

信息差分回波损耗掩模与第 3.7.2.1.2 节中的相同。

3.7.2.2.3 TX/RX 对之间的差分近端和远端串扰（信息 - USB4 Gen3）

建议的近端串扰 (DDNEXT) 和远端串扰 (DDFEXT) 在第 3.7.2.1.3 节中定义。为了最大限度地减少串扰，优化电缆插头内的插卡和电线端接设计非常重要。

3.7.2.2.4 USB D+/D− 和 TX/RX 对之间的差分串扰（信息 - USB4 Gen3）

USB D+/D− 对和 TX/RX 对之间的近端和远端串扰信息与第 3.7.2.1.4 节中的相同。

3.7.2.3 规范性 TX/RX 无源电缆组件要求（USB 3.2 Gen2 和 USB4 Gen2）

综合参数用于电缆组件合规性（插入损耗和差分到共模转换除外），以避免功能正常的电缆组件在某些频率下可能不符合传统 S 参数规格而被拒绝。

3.7.2.3.1 奈奎斯特频率下的插入损耗拟合（标准 - USB 3.2 Gen2 和 USB4 第二代）

奈奎斯特频率下的插入损耗拟合测量的是电缆组件的衰减。为了获得奈奎斯特频率下的插入损耗拟合，测量的电缆组件差分插入损耗用平滑函数拟合。标准拟合算法和

工具应用于提取奈奎斯特频率下的插入损耗拟合。拟合方程由以下公式定义：

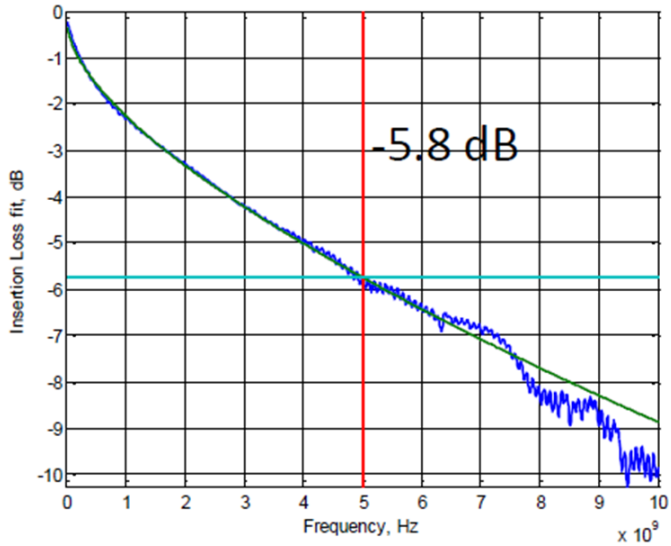
$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3}$$

其中，f 是频率，a、b、c 和 d 是拟合系数。

图 3-39 示出了用平滑函数拟合的测量电缆组件插入损耗的示例；在 SuperSpeed USB Gen2（5.0 GHz）的奈奎斯特频率下拟合的插入损耗为 −5.8 dB。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-39 Illustration of Insertion Loss Fit at Nyquist Frequency



The insertion loss fit at Nyquist frequency (ILfitatNq) shall meet the following requirements:

- ≥ −4 dB at 2.5 GHz,
- ≥ −6 dB at 5 GHz, and
- ≥ −11 dB at 10 GHz.

2.5 GHz, 5.0 GHz and 10 GHz are the Nyquist frequencies for SuperSpeed USB Gen1, SuperSpeed USB Gen2, and USB4 Gen3 data rate, respectively.

The SuperSpeed USB Gen1-only Type-C to Type-C cable assembly is allowed by this specification and shall comply with the following insertion loss fit at Nyquist frequency requirements:

- ≥ −7.0 dB at 2.5 GHz, and
- > −12 dB at 5 GHz.

This insertion fit at Nyquist frequency allows the SuperSpeed USB Gen1-only Type-C to Type-C cable assembly to achieve an overall length of approximately 2 meters.

3.7.2.3.2 Integrated Multi-reflection (Normative – USB 3.2 Gen2 and USB4 Gen2)

The insertion loss deviation, ILD, is defined as

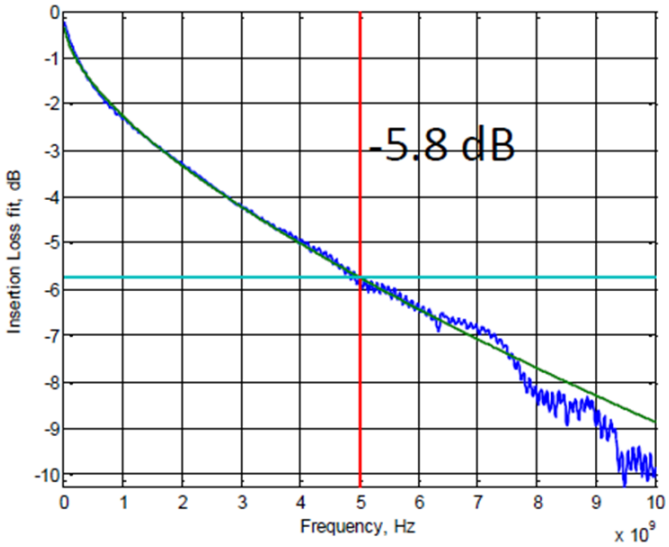
$$ILD(f) = IL(f) - ILfit(f)$$

It measures the ripple of the insertion loss, caused by multiple reflections inside the cable assembly (mated with the fixture). The integration of *ILD(f)* is called the integrated multi-reflection (IMR):

$$IMR = dB\left(\sqrt{\frac{\int_0^{f_{max}} |ILD(f)|^2 |Vin(f)|^2 df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-39 奈奎斯特频率下的插入损耗拟合图



插入损耗适合 t奈奎斯特频率（ILfitatNq）应满足以下条件 g 要求：

- ≥ −在 2.5 GHz 时为 4 dB
- ，• ≥ −在 5 GHz 时为 6 dB
- ，并且 • ≥ −在 10 GHz 时为 11 dB。

2.5 GHz、5.0 GHz 和 10 GHz 分别是 SuperSpeed USB Gen1、SuperSpeed USB Gen2 和 USB 4 Gen3 数据速率的奈奎斯特频率。

本规范允许使用仅适用于 SuperSpeed USB Gen1 的 Type-C 到 Type-C 电缆组件，并且应符合奈奎斯特频率要求下的以下插入损耗拟合：

- 2.5 GHz 时 • ≥ −为 7.0 dB，5 G Hz 时 • > −为 12 dB。

这种在奈奎斯特频率下的插入配合可使 SuperSpeed USB Gen1 专用 Type-C 到 Type-C 电缆组件实现约 2 米的总长度。

3.7.2.3.2 集成多重反射（规范 - USB 3.2 Gen2 和 USB4 Gen2）

插入损耗偏差ILD定义为

$$ILD(f) = IL(f) - ILfit(f)$$

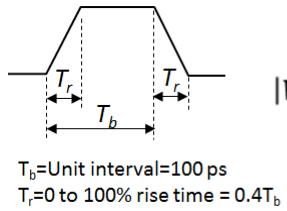
它测量插入损耗的纹波，由电缆组件（与夹具配合）内部的多次反射引起。*ILD(f)* 的积分称为积分多重反射 (IMR)：

$$IMR = dB\left(\sqrt{\frac{\int_0^{f_{max}} |ILD(f)|^2 |Vin(f)|^2 df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

where *fmax* = 12.5 GHz and *Vin(f)* is the input trapezoidal pulse spectrum, defined in Figure 3-40.

Figure 3-40 Input Pulse Spectrum



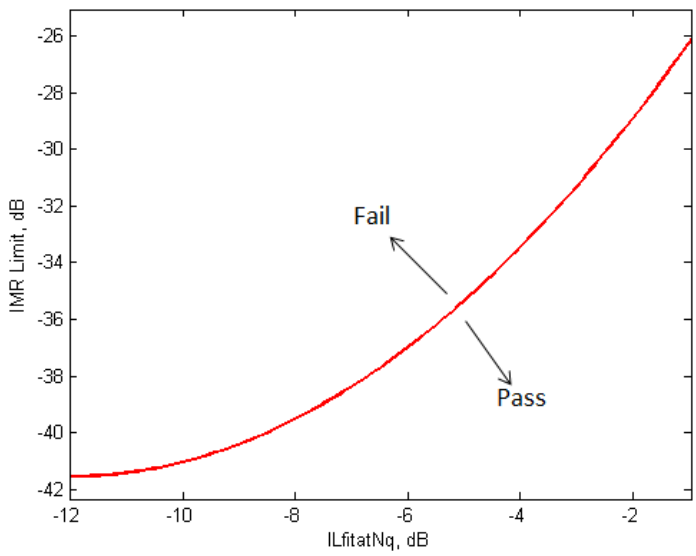
$$|V_{in}(f)| = \left|\frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b}\right|$$

IMR has dependency on ILfitatNq. More IMR may be tolerated when ILfitatNq decreases. The IMR limit is specified as a function of ILfitatNq:

$$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 23.392.$$

This is plotted in Figure 3-41.

Figure 3-41 IMR Limit as Function of ILfitatNq



3.7.2.3.3 Integrated Crosstalk between TX/RX Pairs (Normative – USB 3.2 Gen2 and USB4 Gen2)

The integrated crosstalk between all TX/RX pairs is calculated with the following equations:

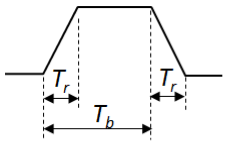
$$INEXT = dB\left(\sqrt{\frac{\int_0^{f_{max}}(|Vin(f)|^2(|NEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\,|NEXTd(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

$$IFEXT = dB\left(\sqrt{\frac{\int_0^{f_{max}}(|Vin(f)|^2(|FEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\,|FEXTd(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

其中 $fmax$ = 12.5 GHz，$Vin(f)$ 是输入梯形脉冲频谱，如图 3-40 所示。

图 3-40 输入脉冲频谱



$$|V_{in}(f)| = \left|\frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b}\right|$$

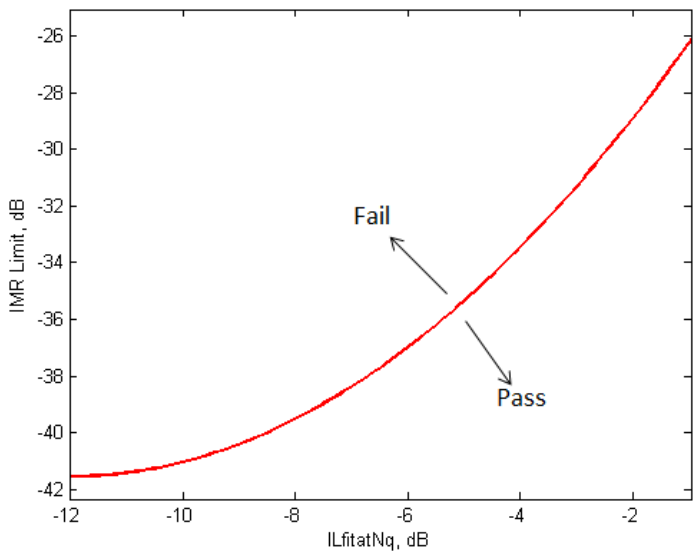
T_b=Unit interval=100 ps
T_r=0 to 100% rise time = 0.4T_b

IMR 依赖于 ILfitatNq。当 ILfitatNq 降低时，可能会容忍更多的 IMR。
IMR 限制被指定为 ILfitatNq 的函数：

$$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 23.392.$$

如图 3-41 所示。

图 3-41 IMR 限值作为 ILfitatNq 的函数



3.7.2.3.3 TX/RX 对之间的综合串扰（规范 - USB 3.2 Gen2 和 USB4 Gen2）

所有 TX/RX 对之间的综合串扰通过以下公式计算：

$$INEXT = dB\left(\sqrt{\frac{\int_0^{f_{max}}(|Vin(f)|^2(|NEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\,|NEXTd(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

$$IFEXT = dB\left(\sqrt{\frac{\int_0^{f_{max}}(|Vin(f)|^2(|FEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\,|FEXTd(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

版权所有 © 2019 USB 3.0 Promoter Group。保留所有权利。

where *NEXT(f)*, *FEXT(f)*, and *C2D(f)* are the measured near-end and far-end crosstalk between TX/RX pairs, and the common-mode-to-differential conversion, respectively. The factor of 0.125^2 accounts for the assumption that the common mode amplitude is 12.5% of the differential amplitude. *NEXTd(f)* and *FEXTd(f)* are, respectively, the near-end and far-end crosstalk from the D+/D− pair to TX/RX pairs. *Vdd(f)* is the input pulse spectrum evaluated using the equation in Figure 3-40 with Tb=2.08 ns.

The integration shall be done for each NEXT and FEXT between all differential pairs. The largest values of INEXT and IFEXT shall meet the following requirements:

- INEXT ≤ −40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2,
- IFEXT ≤ −40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2.

The port-to-port crosstalk (TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2) is specified to support the usages in which all the four SuperSpeed pairs transmit or receive signals simultaneously, for example in SuperSpeed USB dual-lane operation.

3.7.2.3.4 Integrated Crosstalk between TX/RX Pairs to USB 2.0 D+/D− (Normative – USB 3.2 Gen2 and USB4 Gen2)

Crosstalk from the TX/RX pairs to USB 2.0 D+/D− shall be controlled to ensure the robustness of the USB 2.0 link. Since USB Type-C to Type-C Full-Featured cable assemblies may support the usage of *USB 3.2*, *USB4* or an Alternate Mode (e.g., DisplayPort™), the crosstalk from the four high speed differential pairs to D+/D− may be from near-end crosstalk, far-end crosstalk, or a combination of the two. The integrated crosstalk to D+/D− is calculated with the following equations:

$$\text{IDDXT_1NEXT} + \text{FEXT} = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2 (|NEXT1(f)|^2 + |FEXT(f)|^2) df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

where:

NEXT = Near-end crosstalk from TX pair to D+/D−

FEXT = Far-end crosstalk from RX pair to D+/D−

fmax = 1.2 GHz

$$\text{IDDXT_2NEXT} = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2 (|NEXT1(f)|^2 + |NEXT2(f)|^2) df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

where:

NEXT1 = Near-end crosstalk from TX pair to D+/D−

NEXT2 = Near-end crosstalk from RX (the RX functioning in TX mode) pair to D+/D−

fmax = 1.2 GHz

The integration shall be done for NEXT + FEXT and 2NEXT on D+/D− from the two differential pairs located at A2, A3, B10 and B11 (see Figure 2-2) and for NEXT + FEXT and 2NEXT on D+/D− from the two differential pairs located at B2, B3 A10 and A11 (see Figure 2-2). Measurements are made in two sets to minimize the number of ports required for each measurement. The integrated differential crosstalk on D+/D− shall meet the following requirements:

- IDDXT_1NEXT + FEXT ≤ −34.5 dB,

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

其中 $NEXT(f)$、$FEXT(f)$ 和 $C2D(f)$ 分别是 TX/RX 对之间测量到的近端和远端串扰以及共模到差分转换。因子 0.125^2 表示共模幅度为差分幅度的 12.5% 的假设。$NEXTd(f)$ 和 $FEXTd(f)$ 分别是 D+/D− 对到 TX/RX 对的近端和远端串扰。$Vdd(f)$ 是使用图 3-40 中的公式计算的输入脉冲频谱，Tb = 为 2.08 ns。

应对所有差分对之间的每个 NEXT 和 FEXT 进行积分。INEXT 和 IFEXT 的最大值应满足以下要求：

- INEXT ≤ −40 dB 至 12.5GHz，适用于 TX1 至 RX1、TX2 至 RX2、TX1 至 RX2、TX2 至 RX1，TX1 到 TX2，以及 RX1 到 RX2，
- IFEXT ≤ −40 dB 到 12.5GHz，对于 TX1 到 RX1，TX2 到 RX2，TX1 到 RX2，TX2 到 RX1，TX1 到 TX2，以及 RX1 到 RX2。

端口到端口串扰 (TX1 到 RX2、TX2 到 RX1、TX1 到 TX2 和 RX1 到 RX2) 被指定用于支持所有四个 SuperSpeed 对同时发送或接收信号的用途，例如在 SuperSpeed USB 双通道操作中。

3.7.2.3.4 TX/RX 对与 USB 2.0 D+/D− 之间的集成串扰（规范 - USB 3.2 Gen2 和 USB4 Gen2）

应控制 TX/RX 对与 USB 2.0 D+/D− 之间的串扰，以确保 USB 2.0 链路的稳健性。由于 USB Type-C 到 Type-C 全功能电缆组件可能支持使用 *USB 3.2*、*USB4* 或备用模式（例如 DisplayPort™），因此四个高速差分对与 D+/D− ~~之间的串扰可~~能来自~~近端串扰、远端~~串扰或两者的组合。与 D+/D− 之间的综合串扰

通过以下公式计算：

$$\text{IDDXT_1NEXT} + \text{FEXT} = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2 (|NEXT1(f)|^2 + |FEXT(f)|^2) df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

在哪里：

$NEXT$ = TX 对到 D+/D− 的近端串扰

$FEXT$ = 从 RX 对到 D+/D− 的远端串扰

$fmax$ = 1.2 GHz

$$\text{IDDXT_2NEXT} = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2 (|NEXT1(f)|^2 + |NEXT2(f)|^2) df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

在哪里：

$NEXT1$ = TX 对到 D+/D− 的近端串扰

$NEXT2$ = RX（TX 模式下的 RX）对与 D+/D− 之间的近端串扰

$fmax$ = 1.2 GHz

应针对位于 A2、A3、B10 和 B11 的两个差分对的 D+/D− 上的 NEXT + FEXT 和 2NEXT 进行积分（见图 2-2），并针对位于 B2、B3 A10 和 A11 的两个差分对的 D+/D− 上的 NEXT + FEXT 和 2NEXT 进行积分（见图 2-2）。测量分为两组进行，以尽量减少每次测量所需的端口数。D+/D− 上的积分差分串扰应满足以下要求：

- IDDXT_1NEXT + FEXT ≤ −34.5 dB,

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- IDDXT_2NEXT ≤ −33 dB.

3.7.2.3.5 Integrated Return Loss (Normative – USB 3.2 Gen2 and USB4 Gen2)

The integrated return loss (IRL) manages the reflection between the cable assembly and the rest of the system (host and device). It is defined as:

$$IRL = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2 |SDD21(f)|^2 (|SDD11(f)|^2 + |SDD22(f)|^2) df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

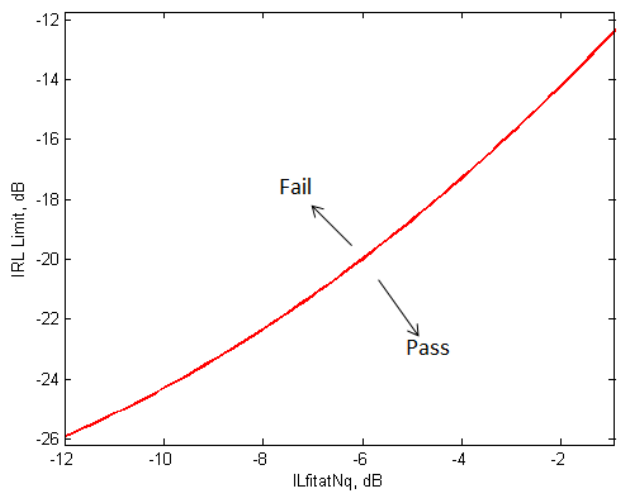
where *SDD21(f)* is the measured cable assembly differential insertion loss, *SDD11(f)* and *SDD22(f)* are the measured cable assembly return losses on the left and right sides, respectively, of a differential pair.

The IRL also has a strong dependency on ILfitatNq, and its limit is specified as a function of ILfitatNq:

$IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 10.784.$

It is shown in Figure 3-42.

Figure 3-42 IRL Limit as Function of ILfitatNq



3.7.2.3.6 Differential-to-Common-Mode Conversion (Normative – USB 3.2 Gen2 and USB4 Gen2)

The differential-to-common-mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Figure 3-43 illustrates the differential-to-common mode conversion (SCD12/SCD21) requirement. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to −20 dB from 100 MHz to 10 GHz.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- IDDXT_2NEXT ≤ −33 分贝。

3.7.2.3.5 综合回波损耗（规范 - USB 3.2 Gen2 和 USB4 Gen2）

综合回波损耗 (IRL) 管理电缆组件与系统其余部分（主机和设备）之间的反射。其定义为：

$$IRL = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2|SDD21(f)|^2(|SDD11(f)|^2+|SDD22(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2df}}\right)$$

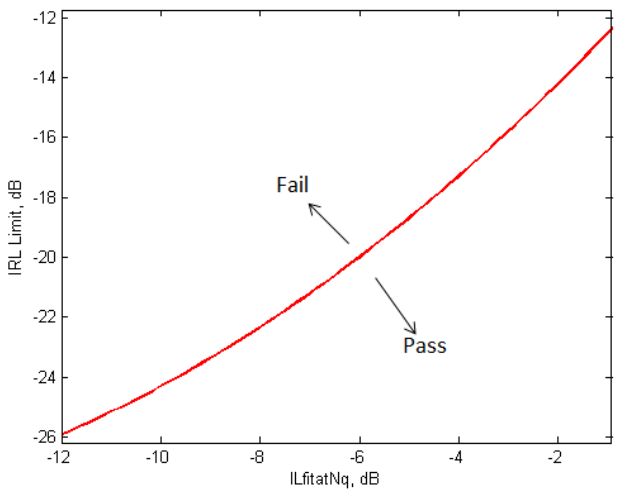
其中 $SDD21(f)$ 是测得的电缆组件差分插入损耗，$SDD11(f)$ 和 $SDD22(f)$ 分别是测得的差分对左侧和右侧的电缆组件回波损耗。

IRL 也对 ILfitatNq 具有很强的依赖性，并且其极限被指定为 ILfitatNq 的函数：

$$IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 10.784.$$

如图3-42所示。

图 3-42 IRL 限值作为 ILfitatNq 的函数

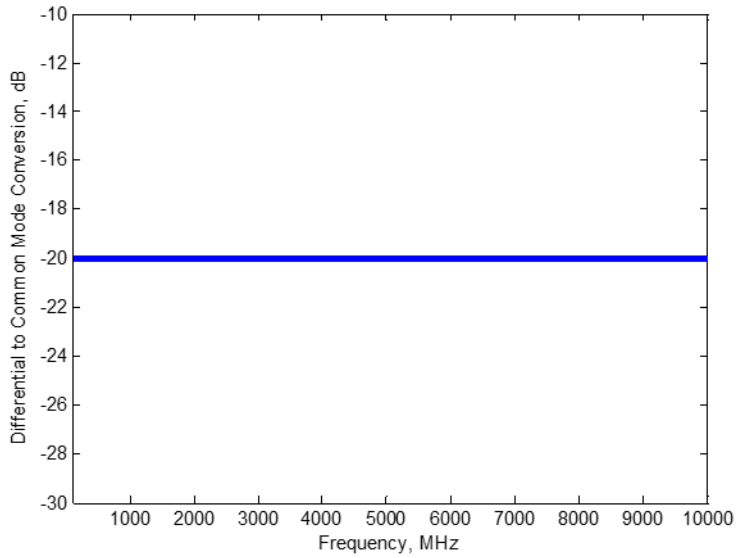


3.7.2.3.6 差模转共模转换（标准 - USB 3.2 Gen2 和 USB4 Gen2）

差模到共模转换用于控制电缆组件向主机或设备注入的共模噪声。图 3-43 说明了差模到共模转换 (SCD12/SCD21) 要求。如果 SCD12/SCD21 在 100 MHz 至 10 GHz 范围内小于或等于 −20 dB，则匹配的电缆组件通过测试。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-43 Differential-to-Common-Mode Conversion Requirement



3.7.2.4 Normative TX/RX Passive Cable Assembly Requirements (USB4 Gen3)

The integrated S-parameter requirements for *USB4* Gen3 follow the same methodology as defined in Section 3.7.2.3. There are parameter adjustments made to suit the *USB4* Gen3 data rate. Unless otherwise specified, the following parameters shall be used to calculate insertion loss fit and integrated parameters:

- T_b, the unit interval, is set to 50 ps, reflecting the *USB4* Gen3 data rate.
- T_r, the rise time, remains at 0.4 * T_b.
- f_{max}, the maximum frequency over which the integration or fitting is performed is increased to 20 GHz.
- An f-square term is added to the insertion loss fit equation to improve fitting quality:

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3} + e * \sqrt{f^4}$$

USB4 Gen3 introduces a system-level COM (Channel Operating Margin) specification for the cable assembly. The details are defined in Section 3.7.2.4.7.

3.7.2.4.1 Insertion Loss Fit at Nyquist Frequencies (Normative – USB4 Gen3)

The insertion loss fit at Nyquist frequency (ILfitatNq) shall meet the following requirements:

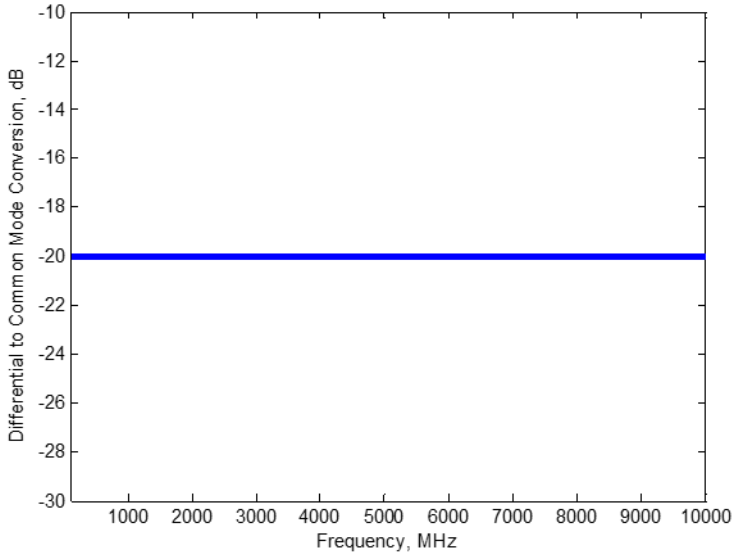
- ≥ −1 dB at 100 MHz,
- ≥ −4.2 dB at 2.5 GHz,
- ≥ −6 dB at 5 GHz,
- ≥ −7.5 dB at 10 GHz,
- ≥ −9.3 dB at 12.5 GHz, and
- ≥ −11 dB at 15 GHz.

3.7.2.4.2 Integrated Multi-Reflection (Informative – USB4 Gen3)

The IMR limit is plotted in Figure 3-44.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-43 差模转共模转换要求



3.7.2.4 规范

tive TX / RX无源电缆组件要求（USB 4 第三代）

USB4 Gen3 的综合 S 参数要求遵循第 3.7.2.3 节中定义的相同方法。进行了参数调整以适应 *USB4* Gen3 数据速率。除非另有规定，否则应使用以下参数来计算插入损耗拟合和综合参数：

• T_b，单位间隔，设置为 50 ps，反映 *USB4* Gen3 数据速率。• T_r，上升时间，保持在 0.4 * T_b。• f_{max}，执行积分或拟合的最大频率增加到 20 GHz。• 在插入损耗拟合方程中添加 f 平方项以提高拟合质量：

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3} + e * \sqrt{f^4}$$

USB4 Gen3 为电缆组件引入了系统级 COM（通道操作裕度）规范。详细信息在第 3.7.2.4.7 节中定义。

3.7.2.4.1 在 奈奎斯特频率下的损耗拟合（规范 - 美国 B4 第三代）

奈奎斯特频率下的插入损耗拟合（ILfitatNq）应满足以下要求：

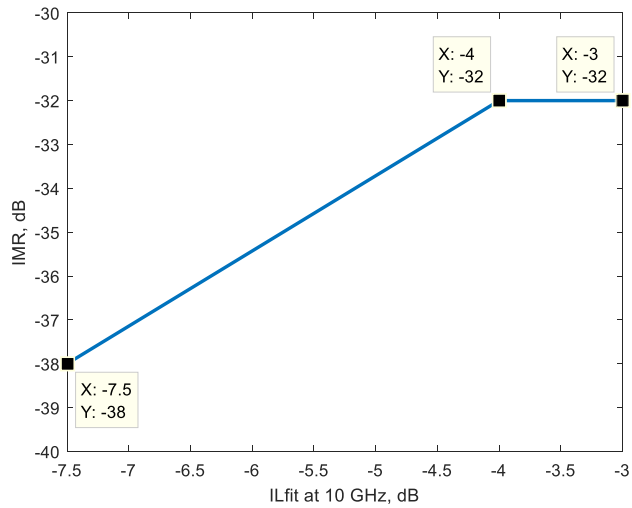
• ≥ −在 100 MHz 时为 1 dB，• ≥ −在 2.5 GHz 时为 4.2 dB，• ≥ −在 5 GHz 时为 6 dB，• ≥ −在 10 GHz 时为 7.5 dB，• ≥ −在 12.5 GHz 时为 9.3 dB，以及 • ≥ −在 15 GHz 时为 11 dB。

3.7.2.4.2 集成多重反射（参考 - USB4 Gen3）

IMR 限制如图 3-44 所示。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-44 IMR Limit as Function of ILfit at 10 GHz (USB4 Gen3)



3.7.2.4.3 Integrated Crosstalk between TX/RX Pairs (Normative – USB4 Gen3)

The integrated crosstalk within a port for TX1 to RX1 and TX2 to RX2 is recommended to meet the following informative requirements:

- INEXT ≤ −43 dB and
- IFEXT ≤ −43 dB.

The recommended informative requirement for the integrated port-to-port crosstalk for TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2) are defined as:

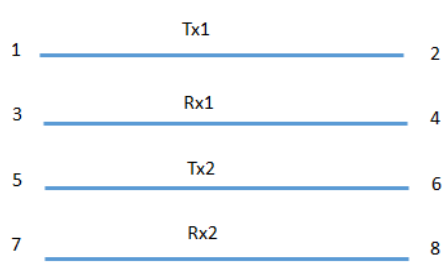
- INEXT_p2p ≤ −50 dB and
- IFEXT_p2p ≤ −50 dB.

The total crosstalk is defined for both the DP Alternate Mode and *USB4* operation. In DP Alternate Mode, all crosstalk is FEXT, while in *USB4* operation both FEXT and NEXT exist. The total crosstalk is defined in the equation below:

$$\text{IXTi_DP or IXTi_USB} = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2\sum_j|SDDij|^2df}{\int_0^{f_{max}}|Vin(f)|^2df}}\right)$$

where the victims i = 1 to 8 and the aggressors j are defined in Figure 3-45.

Figure 3-45 Definition of Port, Victim, and Aggressor



IXT_DP

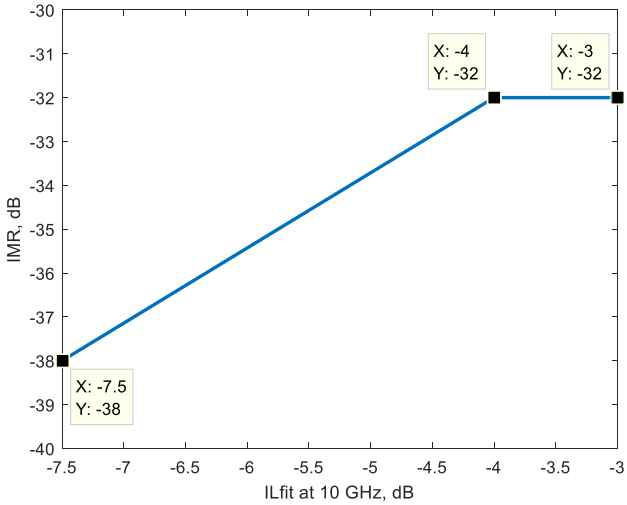
i	j		
1	4	6	8
2	3	5	7
3	2	6	8
4	1	5	7
5	2	4	8
6	1	3	7
7	2	4	6
8	1	3	5

IXT_USB

i	j		
1	3	7	6
2	4	8	5
3	1	5	8
4	2	6	7
5	3	7	2
6	4	8	1
7	1	5	4
8	2	6	3

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-44 10 GHz 时 IMR 限值与 ILfit 的关系（USB4 Gen3）



3.7.2.4.3 TX/RX 对之间的综合串扰（规范 - USB4 Gen3）

建议TX1到RX1和TX2到RX2端口内的综合串扰满足以下信息要求：

- INEXT ≤ −43 dB 和 • IFE
  XT ≤ −43 dB。

综合端口间串扰的建议信息要求
TX1 到 RX2、TX2 到 RX1、TX1 到 TX2 和 RX1 到 RX2) 定义为：

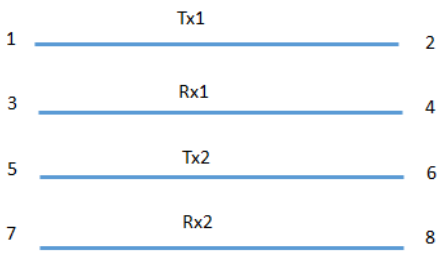
- INEXT_p2p ≤ −50 dB 和 • IFE
  XT_p2p ≤ −50 dB。

总串扰是针对 DP 交替模式和 *USB4* 操作定义的。在 DP 交替模式下，所有串扰都是 FEXT，而在 *USB4* 操作中，FEXT 和 NEXT 都存在。
总串扰定义如下：

$$\text{IXTi_DP or IXTi_USB} = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2\sum_j|SDDij|^2df}{\int_0^{f_{max}}|Vin(f)|^2df}}\right)$$

受害者在哪里 时间 i = 1 至 8 和侵略者 j 定义在 Figu 重新3-45。

图 3-45 端口、受害者、侵略者的定义



IXT_DP

i	j		
1	4	6	8
2	3	5	7
3	2	6	8
4	1	5	7
5	2	4	8
6	1	3	7
7	2	4	6
8	1	3	5

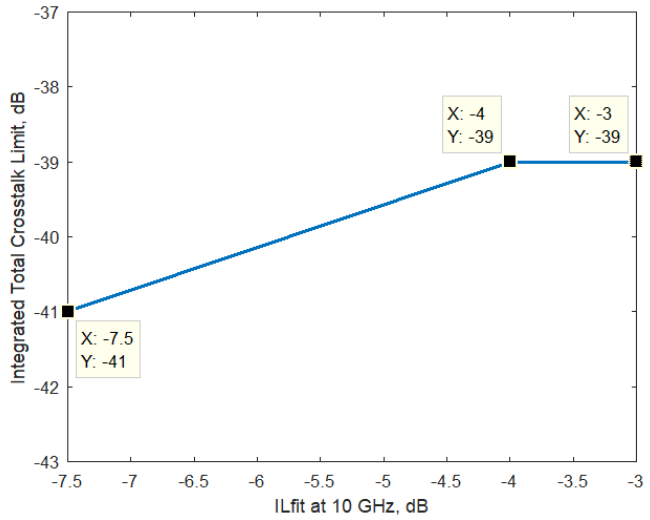
IXT_USB

i	j		
1	3	7	6
2	4	8	5
3	1	5	8
4	2	6	7
5	3	7	2
6	4	8	1
7	1	5	4
8	2	6	3

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The total crosstalk for the DP Alternate Mode and *USB4* operation shall be controlled. Its normative limit is defined in Figure 3-46.

Figure 3-46 IXT_DP and IXT_USB Limit as Function of ILfit at 10 GHz (USB4 Gen3)



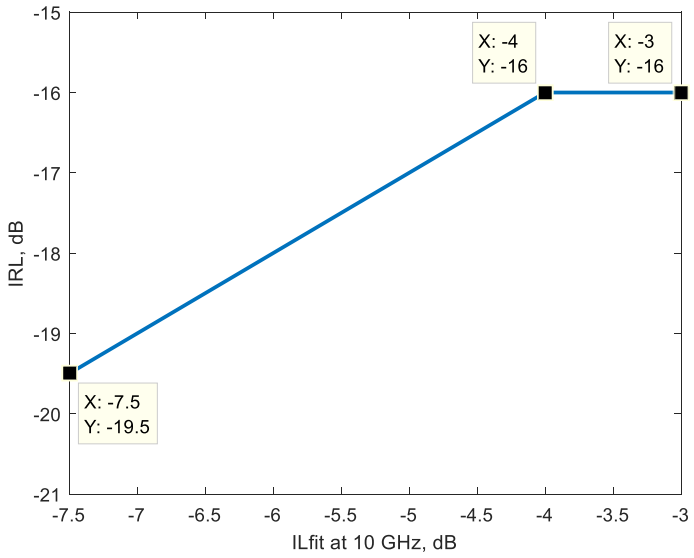
3.7.2.4.4 Integrated Crosstalk from TX/RX Pairs to USB 2.0 D+/D– (Normative – USB4 Gen3)

The requirements for the integrated crosstalk from the TX/RX pairs to USB 2.0 D+/D– are defined in Section 3.7.2.3.4.

3.7.2.4.5 Integrated Return Loss (Normative – USB4 Gen3)

The IRL limit is shown in Figure 3-47.

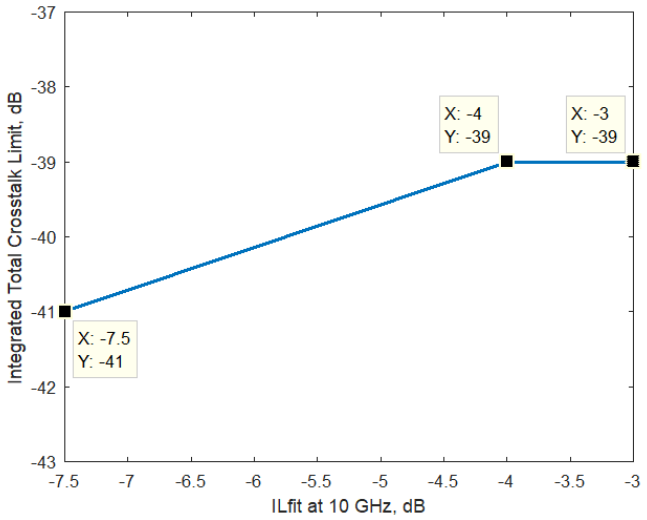
Figure 3-47 IRL Limit as Function of ILfitatNq (USB4 Gen3)



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

应控制 DP 交替模式和 *USB4* 操作的总串扰。其标准限值定义在图 3-46 中。

图 3-46 IXT_DP 和 IXT_USB 限值作为 10 GHz ILfit 的函数（USB4 Gen3）



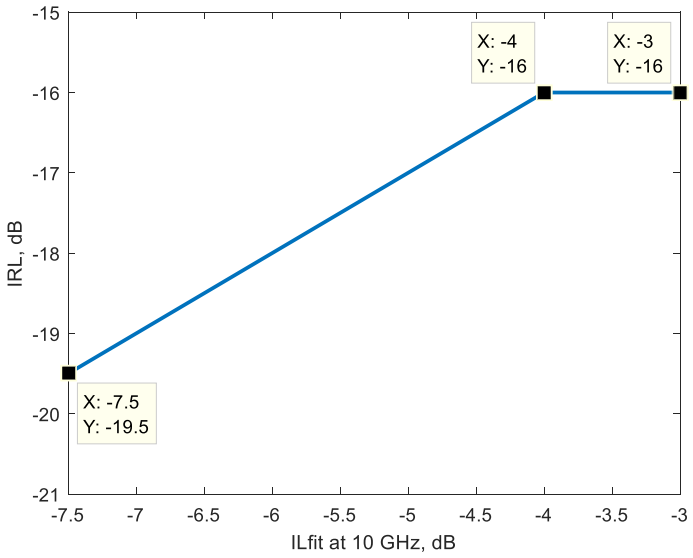
3.7.2.4.4 积分 TX/RX 对与 USB 2.0 D+/D− 之间的串扰（Nor mative − USB4 Gen3)

从 TX/RX 对到 USB 2.0 D+ /D− 的综合串扰要求在第 3.7.2.3.4 节中定义。

3.7.2.4.5 综合回波损耗（规范 - USB4 Gen3）

IRL 限制如图 3-47 所示。

如图 3-47 IRL限制作为ILfitatNq的函数（USB4 第三代）

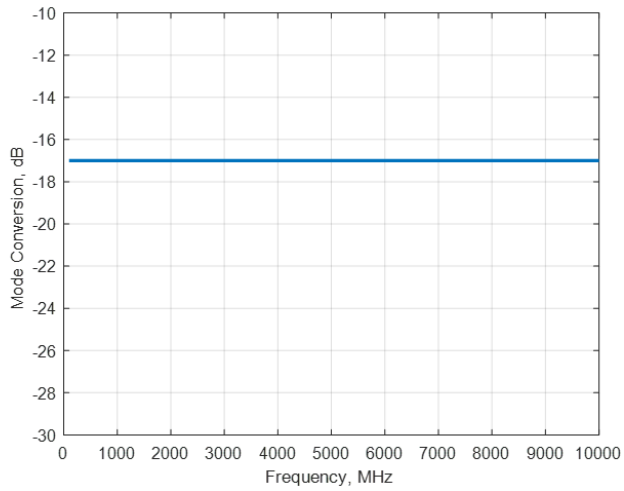


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.7.2.4.6 Differential-to-Common-Mode Conversion (Normative – USB4 Gen3)

Figure 3-48 illustrates the differential-to-common mode conversion (SCD12/SCD21) requirement. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to −17 dB from 100 MHz to 10 GHz. Note that −17 dB is the worst-case limit; no *USB4* Gen3 Type-C cable is allowed to exceed it.

Figure 3-48 Differential-to-Commom-Mode Conversion Requirement (USB4 Gen3)



3.7.2.4.7 COM Requirement (Normative – USB4 Gen3)

Channel Operating Margin (COM) is a figure of merit to measure the channel electrical quality. The technical detail of COM may be found in IEEE Std 802.3bj™-2014 Clause 93a.

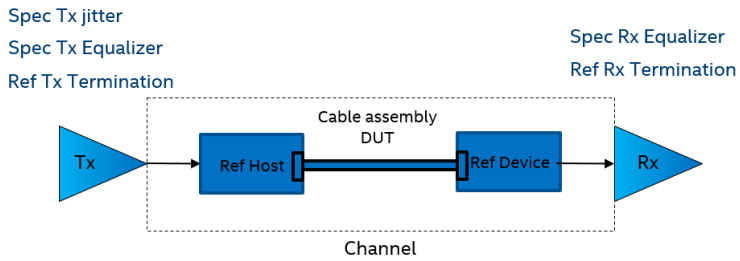
COM is essentially the channel signal-to-noise ratio:

$$COM = 20log10(\frac{A}{N})$$

where A is the signal amplitude and N is the combined noise at BER (bit-error-ratio), which includes the noise sources from ISI (inter-symbol-interference), crosstalk, transmitter jitter, etc.

To calculate COM, reference hosts/devices, which represent the worst-case hosts/devices, shall be defined and the reference TX and RX shall be used. As illustrated in Figure 3-49, the measured cable assembly S-parameters are cascaded with the reference host and reference device models to form the complete channel; the TX and RX die-loading and equalizers are then applied to the channel to calculate COM.

Figure 3-49 Cable Assembly in System

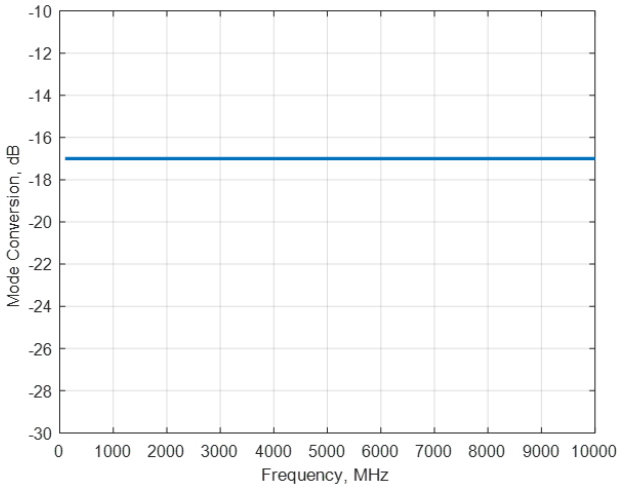


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

.7.2.4.6 差模转共模转换（标准 - USB4 Gen3）

图 3-48 说明了差模到共模转换 (SCD12/SCD21) 的要求。如果 SCD12/SCD21 在 100 MHz 至 10 GHz 范围内小于或等于 −17 dB，则配对的电缆组件通过测试。请注意，−17 dB 是最坏情况限制；任何 *USB4* Gen3 Type-C 电缆都不允许超过该限制。

图 3-48 差分到共模转换要求（USB4 Gen3）



3.7.2.4.7 COM 要求（规范 - USB4 Gen3）

通道操作裕度 (COM) 是衡量通道电气质量的指标。COM 的技术细节可在 IEEE Std 802.3bj™ -2014 Clause 93a 中找到。

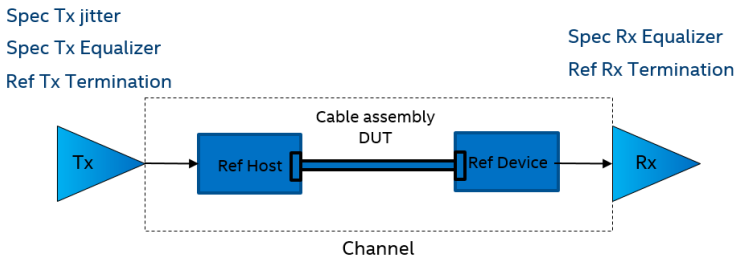
COM 本质上是通道信噪比：

$$COM = 20log10(\frac{A}{N})$$

其中 A 是信号幅度，N 是 BER（比特错误率）的组合噪声，其中包括来自 ISI（符号间干扰）、串扰、发射机抖动等的噪声源。

为了计算 COM，应定义代表最坏情况主机/设备的参考主机/设备，并使用参考 TX 和 RX。如图 3-49 所示，测量的电缆组件 S 参数与参考主机和参考设备模型级联以形成完整的通道；然后将 TX 和 RX 芯片负载和均衡器应用于通道以计算 COM。

图 3-49 系统中的电缆组件



版权所有 © 2019 USB 3.0 Promoter Group。保留所有权利。

Table defines the key parameters in the COM configuration file. It uses the standard COM notations. Note that all the TX and RX equalization settings follow the *USB4* specification.

Table 3-23 Key Parameters in COM Configuration File

Parameter	Setting	Unit	Information
f_b	20	GBd	USB4 Gen 3 data rate
C_d	[0 0]	nF	TX and RX capacitive loading. It is set to zeros as the die-loading is treated as part of the channel
R_d	[42.5 42.5]	Ohm	TX and RX termination resistance
ffe_preset	Table 3-4 of *USB4* Specification		TX equalization presets
g_DC	[-9:1:0]	dB	CTLE DC gain
f_p1	5	GHz	CTLE pole 1
f_p2	10	GHz	CTLE pole 2
f_z	3.55	GHz	CTLE zero
A_v	0.4	V	Signal swing
A_fe	0.4	V	FEXT aggressor swing
A_ne	0.6	V	NEXT aggressor swing
N_b	1		Number of DFE tap
b_max(1)	0.7		DFE bound, ratio to cursor
Sigma_RJ	0.01	UI	TX ramdom jitter, rms.
A_DD	0.085	UI	TX deterministic jitter, mean-to-peak
DER_0	1e-12		Target raw bit-error-rate
eta_0	3.3e-8	V^2/GHz	One sided noise spectral density
SNR_TX	40	dB	TX signal to noise ratio
COM Threshold	3	dB	Pass/fail criterion

To support the calculation of the cable assembly COM, the following collaterals is provided and may be obtained from USB-IF website:

- Reference host/device S-parameter models
- Reference TX and RX die-loading S-parameter models
- COM configuration file
- Tool to compute COM

3.7.2.5 Low-Speed Signal Requirements (Normative)

This section specifies the electrical requirements for CC and SBU wires and the coupling among CC, USB D+/D−, VBUS and SBU.

The CC and SBU wires may be unshielded or shielded, and shall have the properties specified in Table 3-24.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表格定义了 COM 配置文件中的关键参数。它使用标准 COM 符号。请注意，所有 TX 和 RX 均衡设置均遵循 *USB4* 规范。

表 3-23 COM 配置文件中的关键参数

Parameter	Setting	Unit	Information
f_b	20	GBd	USB4 Gen 3 data rate
C_d	[0 0]	nF	TX and RX capacitive loading. It is set to zeros as the die-loading is treated as part of the channel
R_d	[42.5 42.5]	Ohm	TX and RX termination resistance
ffe_preset	Table 3-4 of *USB4* Specification		TX equalization presets
g_DC	[-9:1:0]	dB	CTLE DC gain
f_p1	5	GHz	CTLE pole 1
f_p2	10	GHz	CTLE pole 2
f_z	3.55	GHz	CTLE zero
A_v	0.4	V	Signal swing
A_fe	0.4	V	FEXT aggressor swing
A_ne	0.6	V	NEXT aggressor swing
N_b	1		Number of DFE tap
b_max(1)	0.7		DFE bound, ratio to cursor
Sigma_RJ	0.01	UI	TX ramdom jitter, rms.
A_DD	0.085	UI	TX deterministic jitter, mean-to-peak
DER_0	1e-12		Target raw bit-error-rate
eta_0	3.3e-8	V^2/GHz	One sided noise spectral density
SNR_TX	40	dB	TX signal to noise ratio
COM Threshold	3	dB	Pass/fail criterion

为了支持电缆组件 COM 的计算，提供了以下资料，可从 USB-IF 网站获取：

- 参考主机/设备 S 参数模型
- 参考 TX 和 RX 芯片负载 S 参数模型
- COM 配置文件
- 计算 COM 的工具

3.7.2.5 低速信号要求（规范）

本节规定了 CC 和 SBU 线的电气要求以及 CC、USB D+/D−、VBUS 和 SBU 之间的耦合。

CC 和 SBU 线可以是非屏蔽的，也可以是屏蔽的，且应具有表 3-24 所规定的特性。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-24 Electrical Requirements for CC and SBU wires

Name	Description	Min	Max	Units
zCable_CC	Cable characteristic impedance on the CC wire	32	93	Ω
rCable_CC	Cable DC resistance on the CC wire		15	Ω
tCableDelay_CC	Cable propagation delay on the CC wire		26	ns
cCablePlug_CC	Capacitance for each cable plug on the CC wire		25	pF
zCable_SBU	Cable characteristic impedance on the SBU wires	32	53	Ω
tCableDelay_SBU	Cable propagation delay on the SBU wires		26	ns
rCable_SBU	DC resistance of SBU wires in the cable		5	Ω
SBU SE Insertion Loss	Cable SBU single-ended insertion loss		2.0 @ 0.5 MHz 4.0 @ 1 MHz 9.0 @ 10 MHz 10.7 @ 25 MHz 11.9 @ 50 MHz 13.0 @ 100 MHz	dB

Coupling or crosstalk, both near-end and far-end, among the low speed signals shall be controlled. Table 3-25 shows the matrix of couplings specified.

Table 3-25 Coupling Matrix for Low Speed Signals

Coupling Matrix	D− (SE)	D+/D− (DF)	VBUS	SBU_B/SBU_A (SE)
CC	FF, CT	FF, CT	FF, CT, CTVPD	FF
D+/D− (DF)	N/A	N/A	FF, CT	FF
SBU_A/SBU_B	N/A	FF	FF	FF

DF: Differential; FF: Full-featured cable; CT: Charge-through cable (including USB 2.0 function); CTVPD: Charge-Through VCONN-Powered USB Device.

3.7.2.5.1 CC to USB D+/D− (Normative)

The differential coupling between the CC and D+/D− shall be below the limit shown in Figure 3-50. The limit is defined with the vertices of (0.3 MHz, -60.5 dB), (1 MHz, −50 dB), (10 MHz, −30 dB), (16 MHz, −26 dB) and (100 MHz, −26 dB).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-24 CC 和 SBU 线的电气要求

Name	Description	Min	Max	Units
zCable_CC	Cable characteristic impedance on the CC wire	32	93	Ω
rCable_CC	Cable DC resistance on the CC wire		15	Ω
tCableDelay_CC	Cable propagation delay on the CC wire		26	ns
cCablePlug_CC	Capacitance for each cable plug on the CC wire		25	pF
zCable_SBU	Cable characteristic impedance on the SBU wires	32	53	Ω
tCableDelay_SBU	Cable propagation delay on the SBU wires		26	ns
rCable_SBU	DC resistance of SBU wires in the cable		5	Ω
SBU SE Insertion Loss	Cable SBU single-ended insertion loss		2.0 @ 0.5 MHz 4.0 @ 1 MHz 9.0 @ 10 MHz 10.7 @ 25 MHz 11.9 @ 50 MHz 13.0 @ 100 MHz	dB

低速信号间的近端和远端耦合或串扰应受到控制。表3-25显示了规定的耦合矩阵。

表 3-25 低速信号耦合矩阵

Coupling Matrix	D− (SE)	D+/D− (DF)	VBUS	SBU_B/SBU_A (SE)
CC	FF, CT	FF, CT	FF, CT, CTVPD	FF
D+/D− (DF)	N/A	N/A	FF, CT	FF
SBU_A/SBU_B	N/A	FF	FF	FF

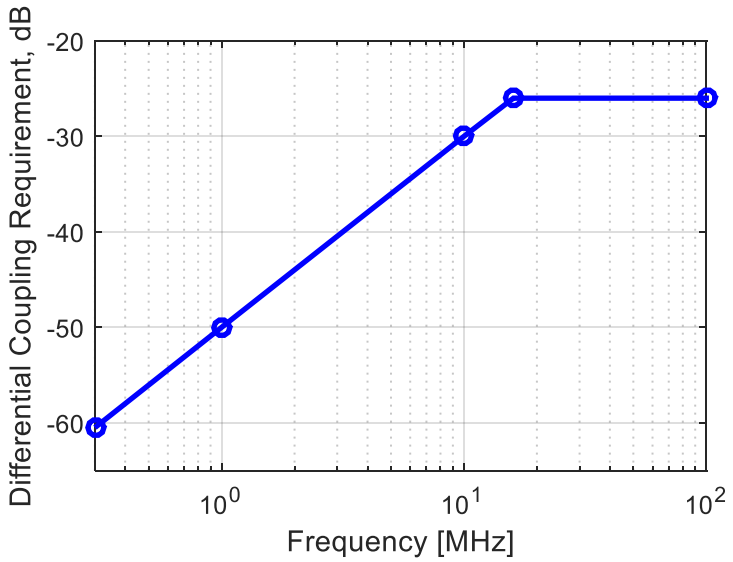
DF：差分；FF：全功能电缆；CT：充电电缆（包括 USB 2.0 功能）；CTVPD：充电 VCONN 供电 USB 设备。

3.7.2.5.1 CC 至 USB D+/D−（规范）

CC 和 D+/D− 之间的差分耦合应低于图 3-50 所示的限值。该限值定义为 (0.3 MHz, -60.5 dB)、(1 MHz, −50 dB)、(10 MHz, −30 dB)、(16 MHz, −26 dB) 和 (100 MHz, −26 dB) 的顶点。

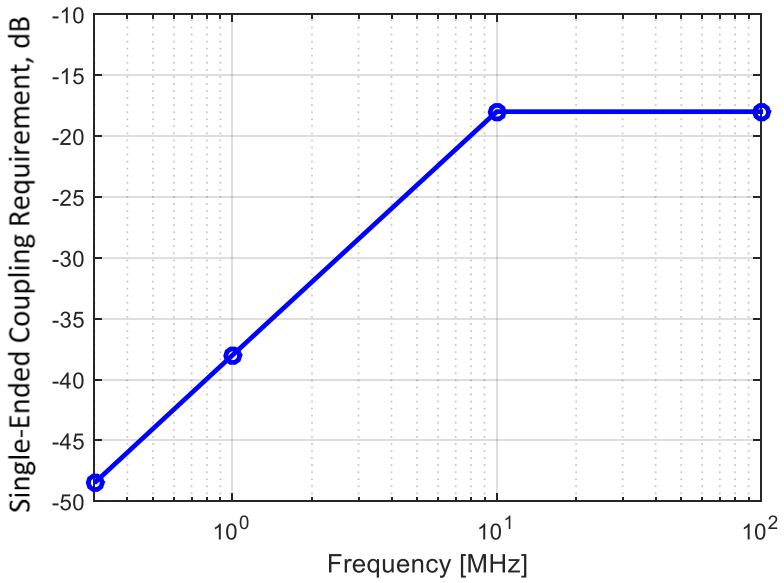
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-50 Requirement for Differential Coupling between CC and D+/D−



For USB 2.0 Type-C cables, the singled-ended coupling between the CC and D− shall be below the limit shown in Figure 3-51. The limit is defined with the vertices of (0.3 MHz, −48.5 dB), (1 MHz, −38 dB), (10 MHz, −18 dB) and (100 MHz, −18 dB).

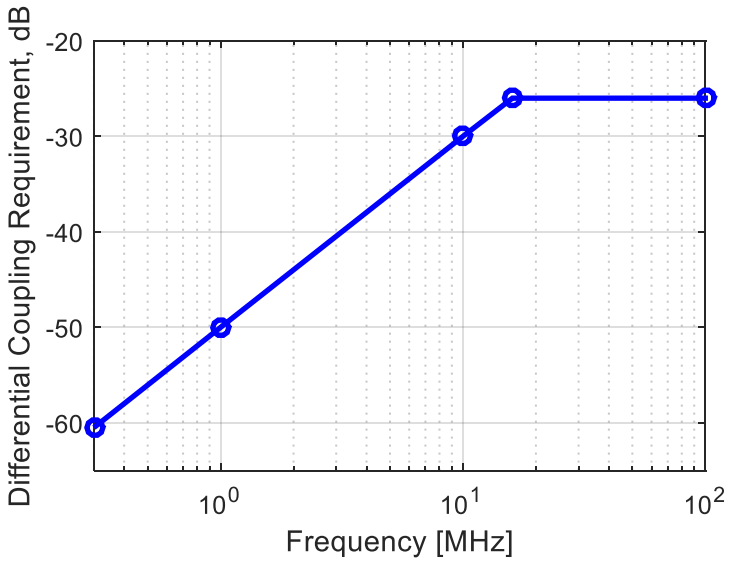
Figure 3-51 Requirement for Single-Ended Coupling between CC and D− in USB 2.0 Type-C Cables



For USB Full-Featured Type-C cables, the singled-ended coupling between the CC and D− shall be below the limit shown in Figure 3-52. The limit is defined with the vertices of (0.3 MHz, −8 dB), (10 MHz, −27.5 dB), (11.8 MHz, −26 dB) and (100 MHz, −26 dB).

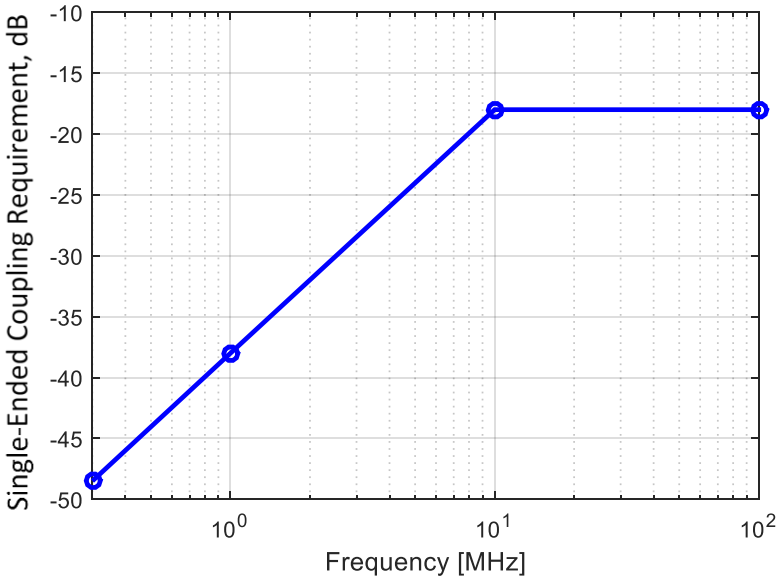
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-50 CC 与 D+/D – 之间的差分耦合要求



对于 USB 2.0 Type-C 电缆，CC 和 D– 之间的单端耦合应低于图 3-51 所示的限值。该限值定义为 (0.3 MHz, −48.5 dB)、(1 MHz, −38 dB)、(10 MHz, −18 dB) 和 (100 MHz, −18 dB) 的顶点。

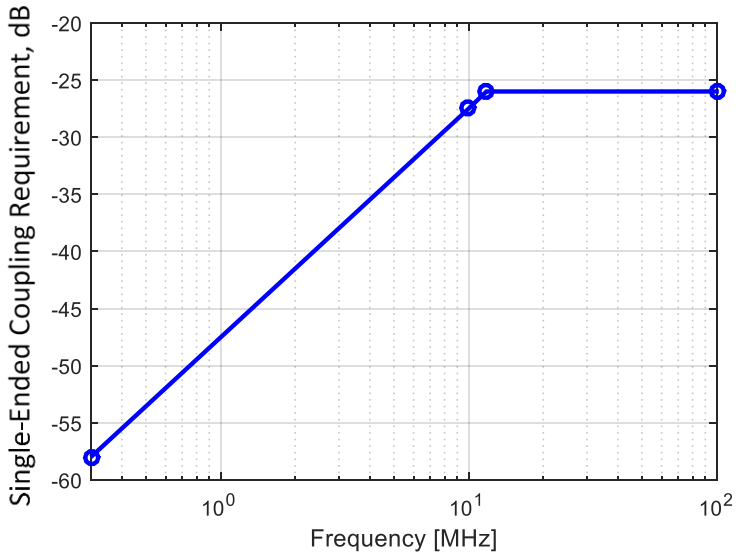
图 3-51 USB 2.0 Type-C 线缆中 CC 和 D– 之间的单端耦合要求



对于 USB 全功能 Type-C 电缆，CC 和 D– 之间的单端耦合应低于图 3-52 所示的限值。该限值定义为 (0.3 MHz，−8 dB)、(10 MHz，−27.5 dB)、(11.8 MHz，−26 dB) 和 (100 MHz，−26 dB) 的顶点。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

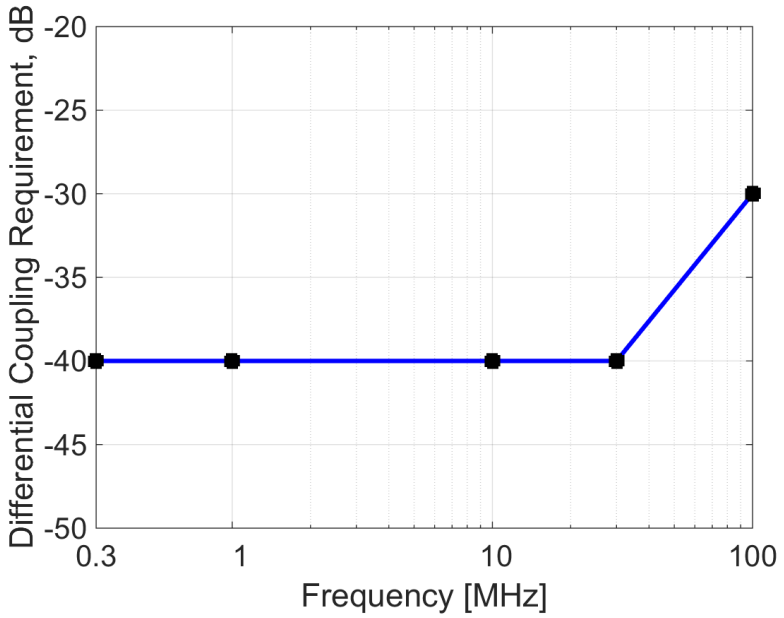
Figure 3-52 Requirement for Single-Ended Coupling between CC and D− in USB Full-Featured Type-C Cables



3.7.2.5.2 VBUS Coupling to SBU_A/SBU_B, CC, and USB D+/D− (Normative)

The differential coupling between VBUS and USB D+/D− shall be less than the limit shown in Figure 3-53. The limit is defined by the following vertices: (0.3 MHz, −40 dB), (1 MHz, −40 dB), (30 MHz, −40 dB), and (100 MHz, −30 dB).

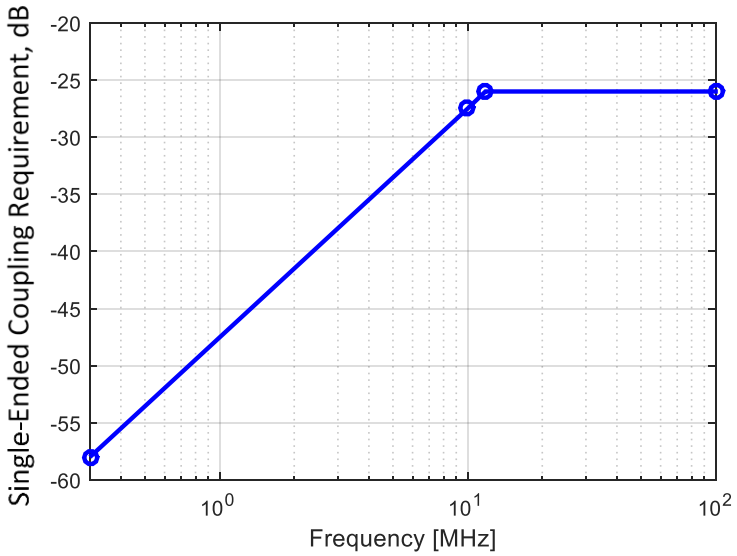
Figure 3-53 Requirement for Differential Coupling between VBUS and D+/D−



The maximum VBUS loop inductance shall be 900 nH and the maximum mutual inductance (M) between VBUS and low speed signal lines (CC, SBU_A, SBU_B, D+, D−) shall be as specified in Table 3-26 to limit VBUS inductive noise coupling on low speed signal lines. For full-

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

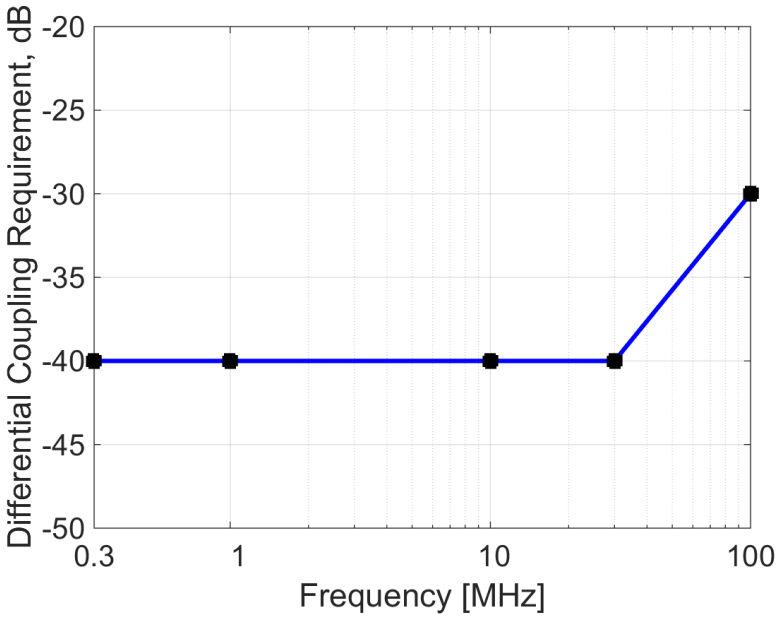
图 3-52 USB 全功能 Type-C 线缆中 CC 和 D− 之间的单端耦合要求



3.7.2.5.2 VBUS 耦合至 SBU_A/SBU_B、CC 和 USB D+/D−（规范）

VBUS 与 USB D+/D− 之间的差分耦合应小于图 3-53 所示的限值。该限值由以下顶点定义：(0.3 MHz, −40 dB)、(1 MHz, −40 dB)、(30 MHz, −40 dB) 和 (100 MHz, −30 dB)。

图 3-53 VBUS 与 D+/D− 之间的差分耦合要求



最大 VBUS 环路电感应为 900 nH，VBUS 与低速信号线（CC、SBU_A、SBU_B、D+、D−）之间的最大互感（M）应符合表 3-26 中的规定，以限制低速信号线上的 VBUS 感应噪声耦合。对于全

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

featured cables, the range of VBUS bypass capacitance shall be 8nF up to 500nF as any of the values in the range is equally effective for high-speed return-path bypassing.

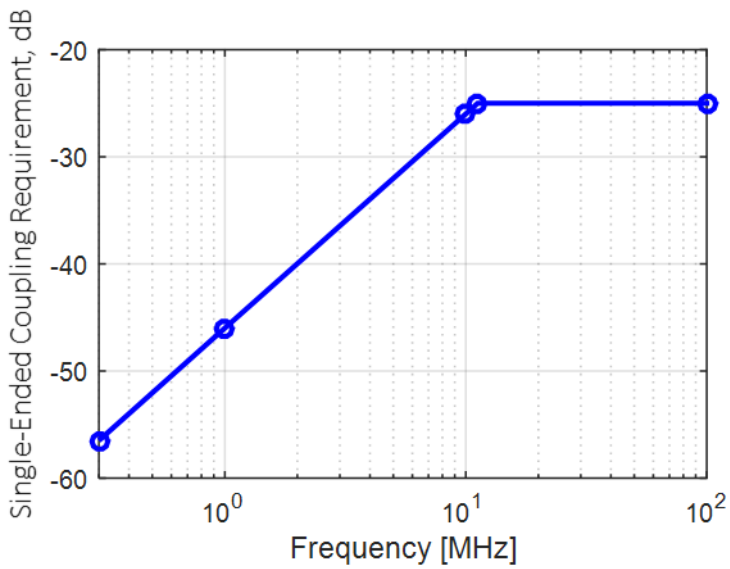
Table 3-26 Maximum Mutual Inductance (M) between VBUS and Low Speed Signal Lines

Low Speed Wire	Max Mutual Inductance (nH)
CC	350
SBU_A, SBU_B	330
D+, D−	330

3.7.2.5.3 Coupling between SBU_A and SBU_B (Normative)

The single-ended coupling between SBU_A and SBU_B shall be less than the limit shown in Figure 3-54. The limit is defined with the vertices of (0.3 MHz, −56.5 dB), (1 MHz, −46 dB), (10 MHz, −26 dB), (11.2 MHz, −25 dB), and (100 MHz, −25 dB).

Figure 3-54 Requirement for Single-Ended Coupling between SBU_A and SBU_B



3.7.2.5.4 Coupling between SBU_A/SBU_B and CC (Normative)

The single-ended coupling between SBU_A and CC, and between SBU_B and CC shall be less than the limit shown in Figure 3-55. The limit is defined with the vertices of (0.3 MHz, −65 dB), (1 MHz, −55 dB), (18 MHz, −30 dB), and (100 MHz, −30 dB).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

特色电缆，VBUS 旁路电容的范围应为 8nF 至 500nF，因为该范围内的任何值对于高速返回路径旁路都同样有效。

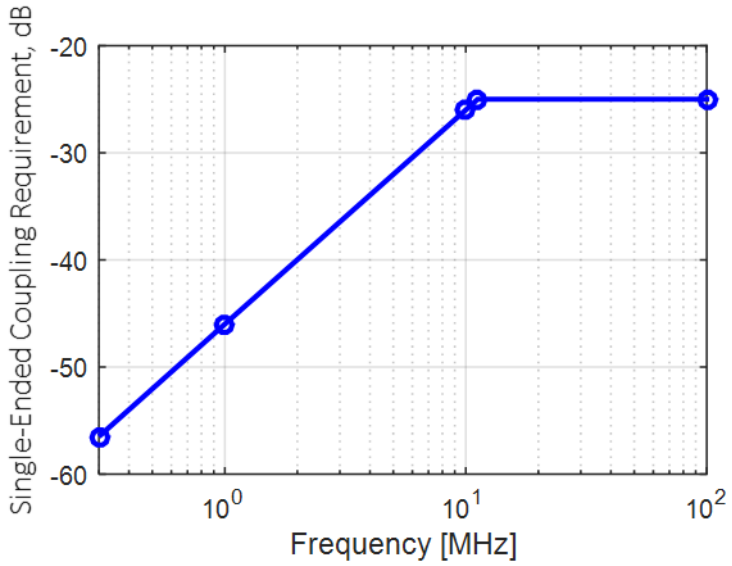
表 3-26 VBUS 与低速信号线之间的最大互感（M）

Low Speed Wire	Max Mutual Inductance (nH)
CC	350
SBU_A, SBU_B	330
D+, D−	330

3.7.2.5.3 SBU_A和SBU_B之间的耦合（规范）

SBU_A 和 SBU_B 之间的单端耦合应小于图 3-54 所示的限值。该限值定义为 (0.3 MHz, −56.5 dB)、(1 MHz, −46 dB)、(10 MHz, −26 dB)、(11.2 MHz, −25 dB) 和 (100 MHz, −25 dB) 的顶点。

图 3-54 SBU_A 和 SBU_B 之间的单端耦合要求

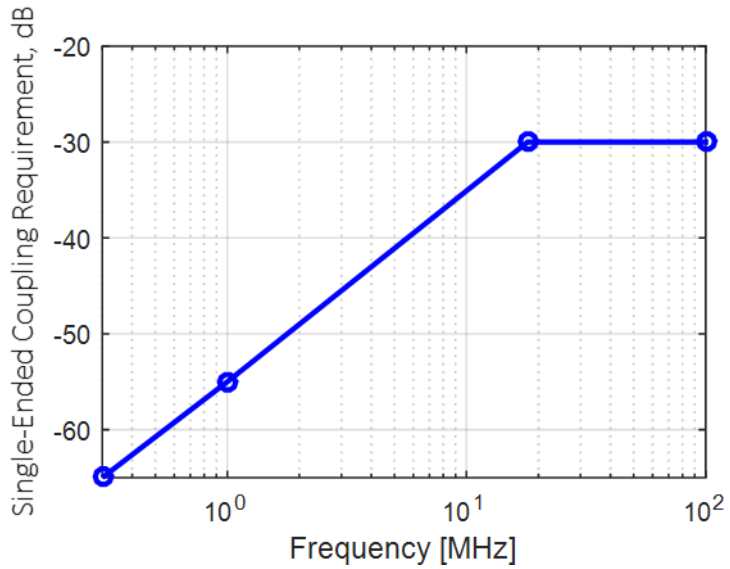


3.7.2.5.4 SBU_A/SBU_B与CC之间的耦合（规范）

SBU_A 和 CC 之间以及 SBU_B 和 CC 之间的单端耦合应小于图 3-55 所示的限值。该限值定义为 (0.3 MHz, −65 dB)、(1 MHz, −55 dB)、(18 MHz, −30 dB) 和 (100 MHz, −30 dB) 的顶点。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

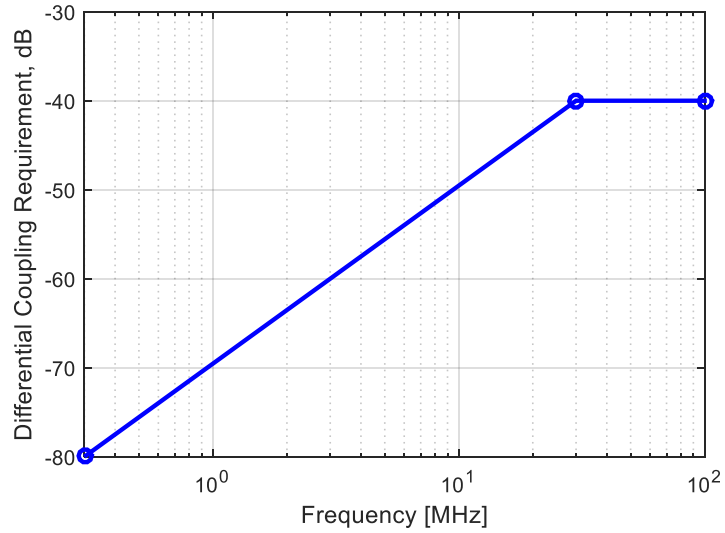
Figure 3-55 Requirement for Single-Ended Coupling between SBU_A/SBU_B and CC



3.7.2.5.5 Coupling between SBU_A/SBU_B and USB D+/D− (Normative)

The coupling between SBU_A and differential D+/D−, and between SBU_B and differential D+/D− shall be less than the limit shown in Figure 3-56. The limit is defined with the vertices of (0.3 MHz, −80 dB), (30 MHz, −40 dB), and (100 MHz, −40 dB).

Figure 3-56 Requirement for Coupling between SBU_A and differential D+/D−, and SBU_B and differential D+/D−

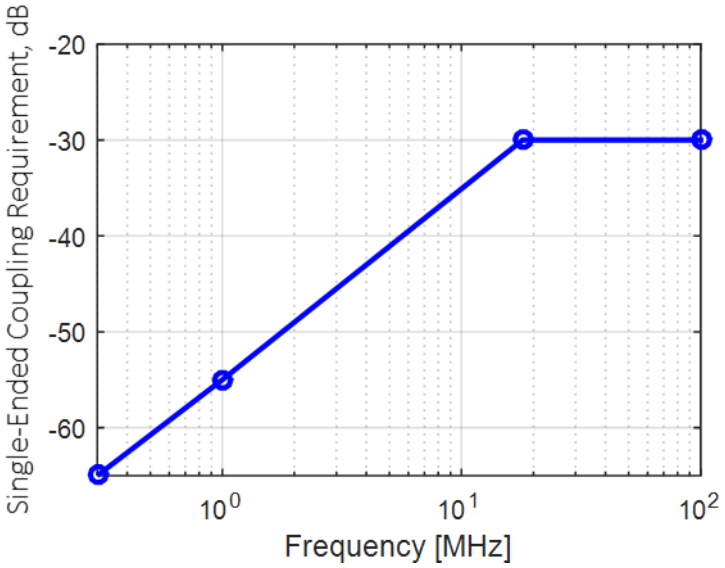


3.7.2.6 USB D+/D− Signal Requirements (Normative)

The USB D+/D− lines of the USB Type-C to USB Type-C passive cable assembly shall meet the requirements defined in Table 3-27.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

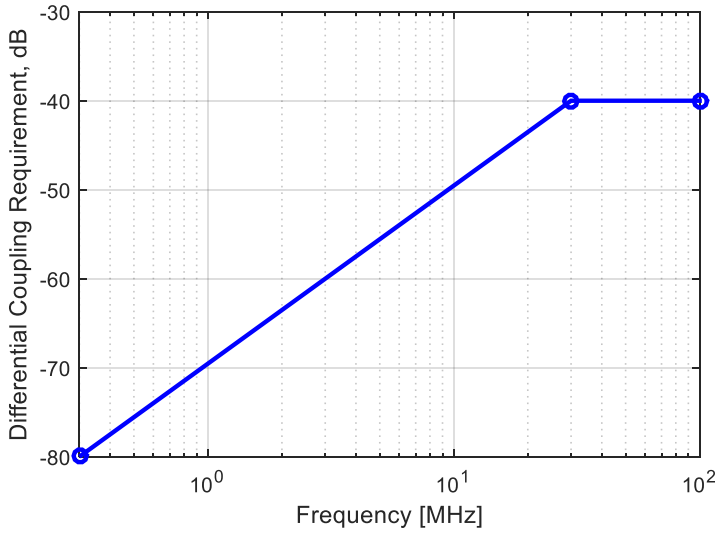
图 3-55 SBU_A/SBU_B 与 CC 之间的单端耦合要求



3.7.2.5.5 SBU_A/SBU_B 与 USB D+/D− 之间的耦合（标准 原生的)

SBU_A 与差分 D+/D− 之间的耦合，以及 SBU_B 与差分 D+/D− 之间的耦合应小于图 3-56 所示的限值。该限值定义为 (0.3 MHz, −80 dB)、(30 MHz, −40 dB) 和 (100 MHz, −40 dB) 的顶点。

图 3-56 SBU_A 与差分 D+/D− 以及 SBU_B 与差分 D+/D− 之间的耦合要求



3.7.2.6 USB D+/D− 信号要求（规范）

USB Type-C 至 USB Type-C 无源电缆组件的 USB D+/D− 线应满足表 3-27 定义的要求。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-27 USB D+/D− Signal Integrity Requirements for USB Type-C to USB Type-C Passive Cable Assemblies

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the cable assembly have the proper impedance. For the entire cable assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Propagation Delay	EIA 364-103 The purpose of the test is to verify the end-to-end propagation of the D+/D− lines of the cable assembly.	26 ns max. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of cable assembly arrive at the receiver at the same time.	100 ps max. 400 ps rise time (20%-80%).
D+/D− Pair Attenuation	EIA 364 – 101 This test ensures the D+/D− pair of a cable assembly is able to provide adequate signal strength to the receiver in order to maintain a low error rate.	≥ −1.02 dB @ 50 MHz ≥ −1.43 dB @ 100 MHz ≥ −2.40 dB @ 200 MHz ≥ −4.35 dB @ 400 MHz
D+ or D− DC Resistance	This test ensures the D+/D− has the proper DC resistance range in order to predict the EOP level and set the *USB 2.0* disconnect level.	3.5 ohms max.

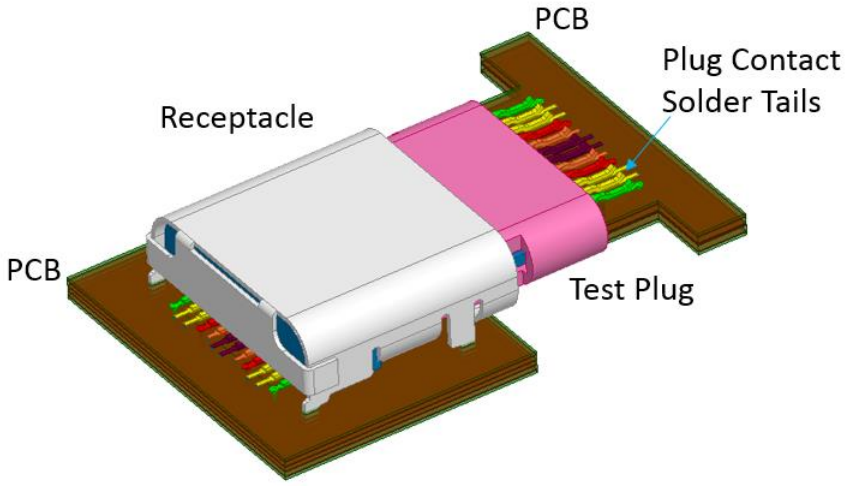
3.7.2.7 VBUS DC Voltage Tolerance (Normative)

A USB Type-C to USB Type-C cable assembly shall tolerate a VBUS voltage of 21 V DC at the cable rated current (i.e. 3 A or 5 A) applied for one hour as a pre-condition of the testing of the electrical aspects of the cable assembly.

3.7.3 Mated Connector (Informative – USB 3.2 Gen2 and USB4 Gen2)

The mated connector as defined in this specification for USB Type-C consists of a receptacle mounted on a PCB, representing how the receptacle is used in a product, and a test plug also mounted on a PCB (paddle card) without cable. This is illustrated in Figure 3-57. Note that the test plug is used in host/device TX/RX testing also.

Figure 3-57 Illustration of USB Type-C Mated Connector



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-27 USB Type-C 至 USB Type-C 无源电缆组件的 USB D+/D− 信号完整性要求

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the cable assembly have the proper impedance. For the entire cable assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Propagation Delay	EIA 364-103 The purpose of the test is to verify the end-to-end propagation of the D+/D− lines of the cable assembly.	26 ns max. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of cable assembly arrive at the receiver at the same time.	100 ps max. 400 ps rise time (20%-80%).
D+/D− Pair Attenuation	EIA 364 – 101 This test ensures the D+/D− pair of a cable assembly is able to provide adequate signal strength to the receiver in order to maintain a low error rate.	≥ −1.02 dB @ 50 MHz ≥ −1.43 dB @ 100 MHz ≥ −2.40 dB @ 200 MHz ≥ −4.35 dB @ 400 MHz
D+ or D− DC Resistance	This test ensures the D+/D− has the proper DC resistance range in order to predict the EOP level and set the *USB 2.0* disconnect level.	3.5 ohms max.

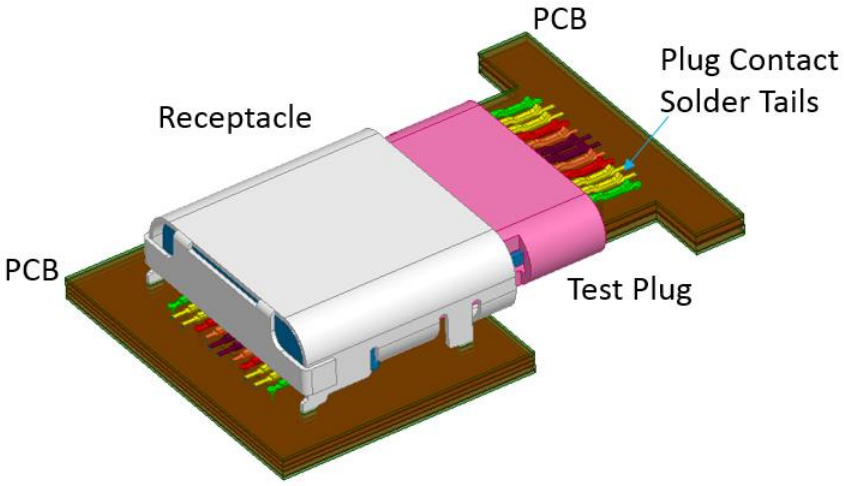
3.7.2.7 VBUS 直流电压容差（规范）

作为对电缆组件电气方面进行测试的先决条件，USB Type-C 至 USB Type-C 电缆组件应能够承受 21 V DC 的 VBUS 电压，电缆额定电流（即 3 A 或 5 A）持续一小时。

3.7.3 配对连接器（信息 - USB 3.2 Gen2 和 USB4 Gen2）

本规范中为 USB Type-C 定义的配对连接器由安装在 PCB 上的插座（表示插座在产品中的使用方式）和同样安装在 PCB（插卡）上的测试插头（不带电缆）组成。如图 3-57 所示。请注意，测试插头也用于主机/设备 TX/RX 测试。

图 3-57 USB Type-C 连接器配接示意图

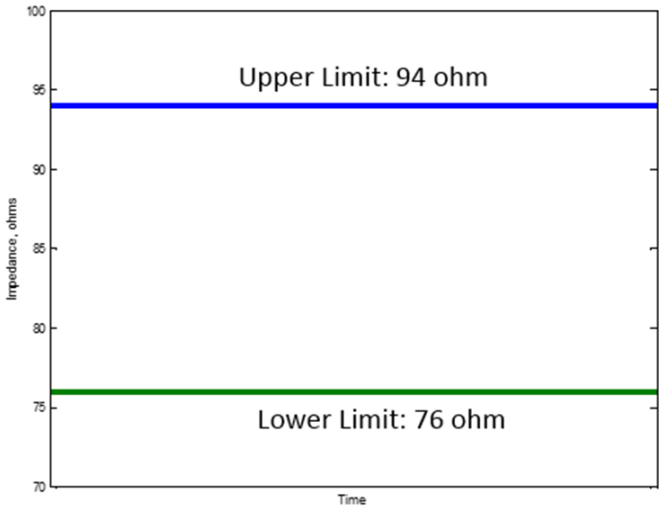


版权所有 © 2019 USB 3.0 Promoter Group。保留所有权利。

3.7.3.1 Differential Impedance (Informative)

The mated connector impedance target is specified to minimize reflection from the connector. The differential impedance of a mated connector should be within 85 Ω ± 9 Ω, as seen from a 40 ps (20% – 80%) rise time. The impedance profile of a mated connector should fall within the limits shown in Figure 3-58.

Figure 3-58 Recommended Impedance Limits of a USB Type-C Mated Connector



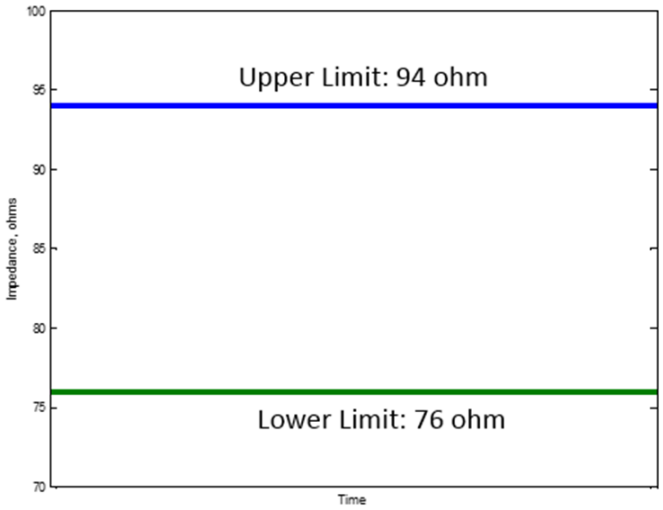
The PCB stack up, lead geometry, and solder pad geometry should be modeled in 3D field-solver to optimize electrical performance. Example ground voids under signal pads are shown in Figure 3-59 based on pad geometry, mounting type, and PCB stack-up shown.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.7.3.1 差分阻抗（参考）

指定匹配连接器阻抗目标是为了尽量减少连接器的反射。匹配连接器的差分阻抗应在 85 Ω ± 9 Ω 以内，从 40 ps (20% – 80%) 上升时间来看。匹配连接器的阻抗曲线应在图 3-58 所示的限值范围内。

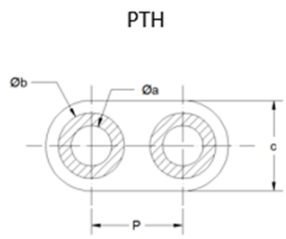
图 3-58 USB Type-C 连接器的推荐阻抗限值



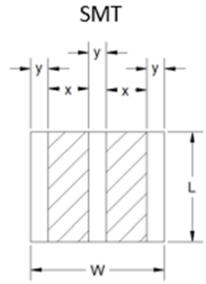
应在 3D 场解算器中对 PCB 堆叠、引线几何形状和焊盘几何形状进行建模，以优化电气性能。图 3-59 显示了信号焊盘下方的接地空隙示例，该示例基于焊盘几何形状、安装类型和所示的 PCB 堆叠。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-59 Recommended Ground Void Dimensions for USB Type-C Receptacle

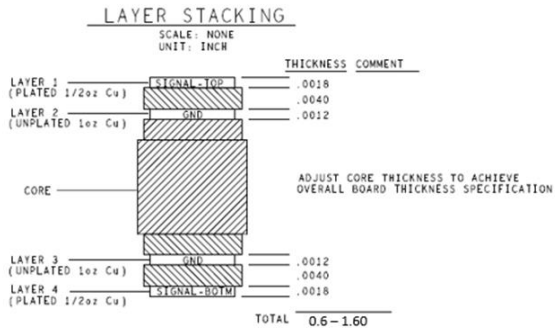


a	Finish hole diameter	0.40
b	Annular ring diameter	0.65
c	Antipad diameter	1.00
P	Antipad center to center distance	0.80



x	SMT pad width	0.35
y	Gap to SMT pad edge	0.15
L	Ground void length	0.7~0.95
W	Ground void width	1.15

Unit: mm



3.7.3.2 Mated Connector Recommended Differential S-Parameter and Signal Integrity Characteristics (Informative)

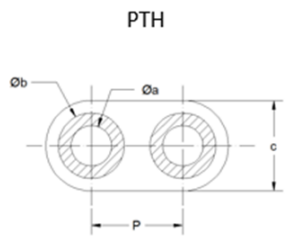
The recommended signal integrity characteristics of USB Type-C mated connector pair are listed in Table 3-28.

Table 3-28 USB Type-C Mated Connector Recommended Signal Integrity Characteristics (Informative)

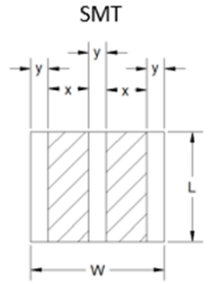
Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at the TX/RX Gen1, Gen2 and Gen3 generation Nyquist frequencies.	≥ −0.6 dB @ 2.5 GHz ≥ −0.8 dB @ 5.0 GHz ≥ −1.0 dB @ 10 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −40 dB

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-59 USB Type-C 插座的推荐接地空隙尺寸

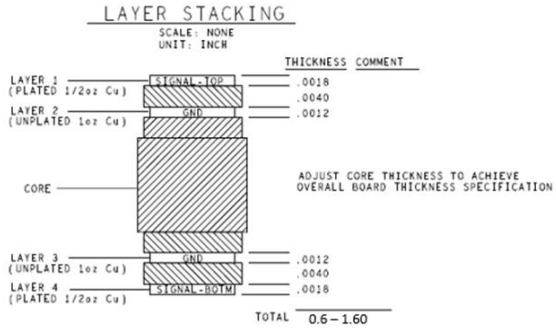


a	Finish hole diameter	0.40
b	Annular ring diameter	0.65
c	Antipad diameter	1.00
P	Antipad center to center distance	0.80



x	SMT pad width	0.35
y	Gap to SMT pad edge	0.15
L	Ground void length	0.7~0.95
W	Ground void width	1.15

Unit: mm



3.7.3.2 配对连接器推荐差分 S 参数和信号完整性特性（参考）

表 3-28 列出了 USB Type-C 连接器对的推荐信号完整性特性。

表 3-28 USB Type-C 连接器推荐信号完整性特性（参考）

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at the TX/RX Gen1, Gen2 and Gen3 generation Nyquist frequencies.	≥ −0.6 dB @ 2.5 GHz ≥ −0.8 dB @ 5.0 GHz ≥ −1.0 dB @ 10 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −40 dB

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Items	Descriptions and Procedures	Requirements
Integrated Differential Near-end Crosstalk on TX/RX (INEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + 0.125^2 \cdot \lvert C2D(f)\rvert^2)df + \int_0^{fmax}\lvert Vdd(f)\rvert^2\ \lvert NEXTd(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: $NEXT$ = NEXT between TX/RX pairs $NEXTd$ = NEXT between D+/D− and TX/RX pairs	≤ −44 dB
Integrated Differential Far-end Crosstalk on TX/RX (IFEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2 + 0.125^2 \cdot \lvert C2D(f)\rvert^2)df + \int_0^{fmax}\lvert Vdd(f)\rvert^2\ \lvert FEXTd(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: $FEXT$ = FEXT between TX/RX pairs $FEXTd$ = FEXT between D+/D− and TX/RX pairs	≤ −44 dB
Differential Crosstalk of TX/RX on D+/D−	The differential near-end and far-end crosstalk of the TX/RX pairs on the D+/D− pair in mated connectors.	See Figure 3-60
Differential Crosstalk of D+/D− on TX/RX	The differential near-end and far-end crosstalk of the D+/D− pair on the TX/RX pairs in mated connectors.	See Figure 3-60
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2 + \lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −18 dB
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	See Figure 3-61

Note: *fmax* = 12.5 GHz (unless otherwise specified);

Vin(f) is defined in Figure 3-40 with Tb (UI) = 100 ps;

Vdd(f) is also defined in Figure 3-40 with Tb (UI) = 2.08 ns.

C2D(f) =measured near-end and far-end crosstalk between TX/RX pairs, and the common-mode-to-differential conversion, respectively. The factor of 0.125^2 accounts for the assumption that the common mode amplitude is 12.5% of the differential amplitude.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Items	Descriptions and Procedures	Requirements
Integrated Differential Near-end Crosstalk on TX/RX (INEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + 0.125^2 \cdot \lvert C2D(f)\rvert^2)df + \int_0^{fmax}\lvert Vdd(f)\rvert^2\ \lvert NEXTd(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: $NEXT$ = NEXT between TX/RX pairs $NEXTd$ = NEXT between D+/D− and TX/RX pairs	≤ −44 dB
Integrated Differential Far-end Crosstalk on TX/RX (IFEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2 + 0.125^2 \cdot \lvert C2D(f)\rvert^2)df + \int_0^{fmax}\lvert Vdd(f)\rvert^2\ \lvert FEXTd(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: $FEXT$ = FEXT between TX/RX pairs $FEXTd$ = FEXT between D+/D− and TX/RX pairs	≤ −44 dB
Differential Crosstalk of TX/RX on D+/D−	The differential near-end and far-end crosstalk of the TX/RX pairs on the D+/D− pair in mated connectors.	See Figure 3-60
Differential Crosstalk of D+/D− on TX/RX	The differential near-end and far-end crosstalk of the D+/D− pair on the TX/RX pairs in mated connectors.	See Figure 3-60
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2 + \lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −18 dB
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	See Figure 3-61

注意：$fmax$ = 12.5 GHz（除非另有说明）；$Vin(f)$ 在图 3-40 中定义为 Tb (UI) = 100 ps；$Vdd(f)$ 也在图 3-40 中定义为 Tb (UI) = 2.08 ns。 $C2D(f)$ = 分别测量 TX/RX 对之间的近端和远端串扰以及共模到差分转换。0.125^2 的系数考虑了共模幅度为差分幅度的 12.5% 的假设。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-60 Recommended Differential Near-End and Far-End Crosstalk Limits between D+/D– Pair and TX/RX Pairs

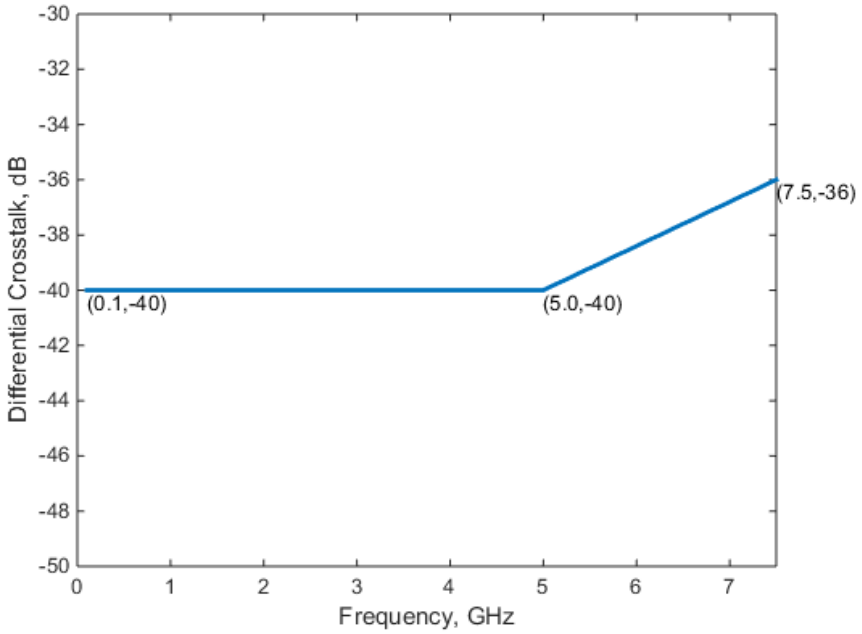
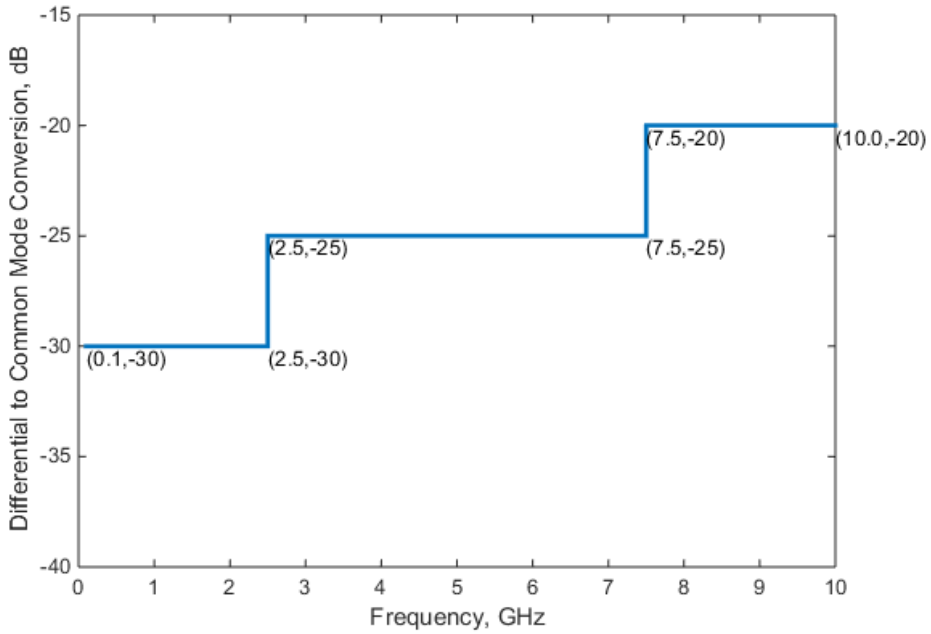


Figure 3-61 Recommended Limits for Differential-to-Common-Mode Conversion



3.7.4 Mated Connector (Normative – USB4 Gen3)

The mated connector requirements for *USB4* Gen3 is normative and listed in Table 3-29. Unless otherwise specified, the items to be specified are identical to what defined in Section 3.7.3 and the parameters used to calculate the integrated parameters are the same as defined in Section 3.7.2.4 for the *USB4* Gen3 cable assembly.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-60 D+/D− 对和 TX/RX 对之间的差分近端和远端串扰限值建议

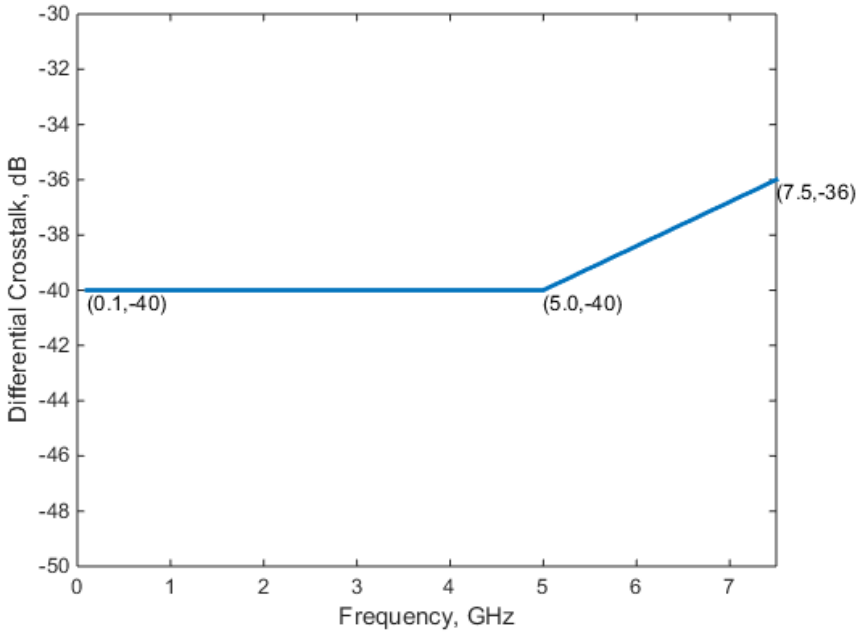
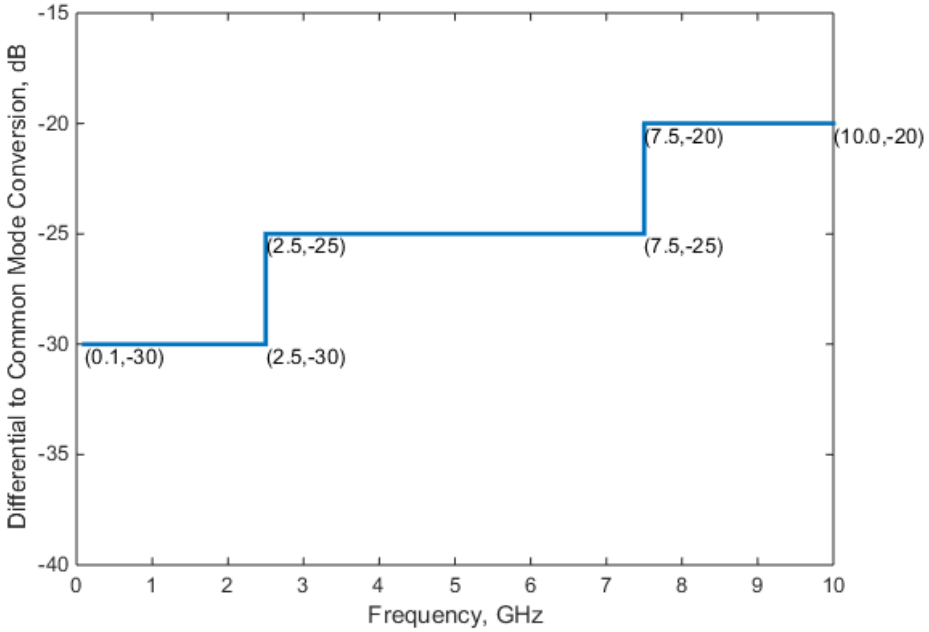


图 3-61 差模转共模的推荐限值



3.7.4 配对连接器（标准 - USB4 Gen3）

USB4 Gen3 的配接连接器要求是规范性的，列于表 3-29 中。除非另有规定，否则要指定的项目与第 3.7.3 节中定义的项目相同，用于计算综合参数的参数与第 3.7.2.4 节中针对 *USB4* Gen3 电缆组件定义的参数相同。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-29 USB Type-C Mated Connector Signal Integrity Characteristics for USB4 Gen3 (Normative)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at a few different frequencies.	≥ −0.6 dB @ 2.5 GHz ≥ −0.8 dB @ 5.0 GHz ≥ −1.0 dB @ 10 GHz ≥ −1.25 dB @ 12.5 GHz ≥ −1.5 dB @ 15 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −39 dB
Integrated Differential Near-end Crosstalk on TX/RX (INEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXT* = NEXT between TX1and RX1, and TX2 and RX2.	≤ −43 dB
Integrated Differential Far-end Crosstalk on TX/RX (IFEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *FEXT* = FEXT between TX1 and RX1, and TX2 and RX2.	≤ −43 dB
Differential Crosstalk of TX/RX on D+/D− Differential Crosstalk of D+/D− on TX/RX	The differential near-end and far-end crosstalk of the TX/RX pairs on the D+/D− pair in mated connectors, and the differential near-end and far-end crosstalk of the D+/D− pair on the TX/RX pairs in mated connectors. $dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2+\lvert NEXT(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *FEXT* = Far-end crosstalk between TX/RX and D+/D− pairs *NEXT* = Near-end crosstalk between TX/RX and D+/D− pairs *fmax* = 1.2 GHz	≤ −50 dB
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −15 dB
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	≤ −20 dB

Note: *fmax* = 20 GHz (unless otherwise specified);
Vin(f) is defined with Tb (UI) = 50 ps.

3.7.5 USB Type-C to Legacy Cable Assemblies (Normative)

The USB Type-C to legacy cable assemblies may support *USB 2.0* only or *USB 3.2* Gen2; *USB 3.2* Gen1-only Type-C to legacy cable assemblies are not allowed.

3.7.5.1 USB 2.0-only Cable Assemblies (Normative)

The *USB 2.0*-only Type-C to legacy USB cable assemblies include:

- USB Type-C plug to *USB 2.0* Standard-A plug

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-29 USB Type-C 连接器信号完整性特性（USB4 Gen3）（规范）

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at a few different frequencies.	≥ −0.6 dB @ 2.5 GHz ≥ −0.8 dB @ 5.0 GHz ≥ −1.0 dB @ 10 GHz ≥ −1.25 dB @ 12.5 GHz ≥ −1.5 dB @ 15 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −39 dB
Integrated Differential Near-end Crosstalk on TX/RX (INEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: $NEXT$ = NEXT between TX1and RX1, and TX2 and RX2.	≤ −43 dB
Integrated Differential Far-end Crosstalk on TX/RX (IFEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: $FEXT$ = FEXT between TX1 and RX1, and TX2 and RX2.	≤ −43 dB
Differential Crosstalk of TX/RX on D+/D− Differential Crosstalk of D+/D− on TX/RX	The differential near-end and far-end crosstalk of the TX/RX pairs on the D+/D− pair in mated connectors, and the differential near-end and far-end crosstalk of the D+/D− pair on the TX/RX pairs in mated connectors. $dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2+\lvert NEXT(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: $FEXT$ = Far-end crosstalk between TX/RX and D+/D− pairs $NEXT$ = Near-end crosstalk between TX/RX and D+/D− pairs $fmax$ = 1.2 GHz	≤ −50 dB
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −15 dB
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	≤ −20 dB

注意：$fmax$ = 20 GHz（除非另有规定）；
$Vin(f)$ 定义为 Tb (UI) = 50 ps。

3.7.5 USB Type-C 至传统电缆组件（规范）

USB Type-C 至传统电缆组件可能仅支持 *USB 2.0* 或 *USB 3.2* Gen2；不允许仅支持 *USB 3.2* Gen1 的 Type-C 至传统电缆组件。

3.7.5.1 仅限 USB 2.0 的电缆组件（规范）

仅限 *USB 2.0* 的 Type-C 转传统 USB 电缆组件包括：

- USB Type-C 插头转 *USB 2.0* 标准 A 插头

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- USB Type-C plug to *USB 2.0* Standard-B plug
- USB Type-C plug to *USB 2.0* Micro-B plug
- USB Type-C plug to *USB 2.0* Mini-B plug

The USB D+/D− signal integrity requirements are specified in Table 3-30.

Table 3-30 USB D+/D− Signal Integrity Requirements for USB Type-C to Legacy USB Cable Assemblies

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the cable assembly have the proper impedance. For the entire cable assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Propagation Delay	EIA 364-103 The purpose of the test is to verify the end-to-end propagation of the D+/D− lines of the cable assembly.	10 ns max for USB Type-C to Micro-B cable assembly; 20 ns max for all other USB Type-C to legacy USB cable assemblies. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of cable assembly arrive at the receiver at the same time.	100 ps max. 400 ps rise time (20%-80%).
D+/D− Pair Attenuation	EIA 364 – 101 This test ensures the D+/D− pair of a cable assembly is able to provide adequate signal strength to the receiver in order to maintain a low error rate.	≥ −1.02 dB @ 50 MHz ≥ −1.43 dB @ 100 MHz ≥ −2.40 dB @ 200 MHz ≥ −4.35 dB @ 400 MHz
D+ or D− DC Resistance	This test ensures the D+/D− has the proper DC resistance range in order to predict the EOP level and set the *USB 2.0* disconnect level.	3.5 ohms max.

3.7.5.2 *USB 3.1* Gen2 Cable Assemblies (Normative)

The USB Type-C to *USB 3.1* Gen2 legacy cable assemblies include:

- USB Type-C plug to *USB 3.1* Standard-A plug
- USB Type-C plug to *USB 3.1* Standard-B plug
- USB Type-C plug to *USB 3.1* Micro-B plug

The informative design targets for these cables are provided in Table 3-31.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• USB Type-C 插头转至 *USB 2.0* Standard-B 插头 • USB Type-C 插头转至 *USB 2.0* Micro-B 插头 • USB Type-C 插头转至 *USB 2.0* Mini-B 插头

USB D+/D−信号完整性要求如表 3-30 所示。

表 3-30 USB Type-C 转传统 USB 电缆组件的 USB D+/D− 信号完整性要求

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the cable assembly have the proper impedance. For the entire cable assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Propagation Delay	EIA 364-103 The purpose of the test is to verify the end-to-end propagation of the D+/D− lines of the cable assembly.	10 ns max for USB Type-C to Micro-B cable assembly; 20 ns max for all other USB Type-C to legacy USB cable assemblies. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of cable assembly arrive at the receiver at the same time.	100 ps max. 400 ps rise time (20%-80%).
D+/D− Pair Attenuation	EIA 364 – 101 This test ensures the D+/D− pair of a cable assembly is able to provide adequate signal strength to the receiver in order to maintain a low error rate.	≥ −1.02 dB @ 50 MHz ≥ −1.43 dB @ 100 MHz ≥ −2.40 dB @ 200 MHz ≥ −4.35 dB @ 400 MHz
D+ or D− DC Resistance	This test ensures the D+/D− has the proper DC resistance range in order to predict the EOP level and set the *USB 2.0* disconnect level.	3.5 ohms max.

3.7.5.2 ***USB 3.1*** Gen2 电缆组件（规范）

USB Type-C 至 *USB 3.1* Gen2 传统电缆组件包括：

• USB Type-C 插头转 *USB 3.1* 标准 A 插头 • USB Type-C 插头转 *USB 3.1* 标准 B 插头 • USB Type-C 插头转 *USB 3.1* Micro-B 插头

表 3-31 提供了这些电缆的信息设计目标。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-31 Design Targets for USB Type-C to *USB 3.1* Gen2 Legacy Cable Assemblies (Informative)

Items	Design Targets
Differential Impedance	76 ohms min and 96 ohms max. 40 ps rise time (20%-80%).
Differential Insertion Loss	≥ −2 dB @ 100 MHz ≥ −4 dB @ 2.5 GHz, except for the USB Type-C plug to USB 3.1 Standard-A plug cable assembly which is ≥−3.5 dB @ 2.5 GHz −6.0 dB max @ 5.0 GHz
Differential NEXT between SuperSpeed Pairs	≤ −34 dB to 5 GHz
Differential NEXT and FEXT between D+/D- and SuperSpeed Pairs	≤ −30 dB to 5 GHz

The normative requirements include the USB D+/D− signaling as specified in Table 3-30, and the SuperSpeed USB parameters specified in Table 3-32.

Table 3-32 USB Type-C to *USB 3.1* Gen2 Legacy Cable Assembly Signal Integrity Requirements (Normative)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at both the SuperSpeed Gen1 and Gen2 Nyquist frequencies.	≥ −4 dB @ 2.5 GHz, except for the USB Type-C plug to USB 3.1 Standard-A plug cable assembly which is ≥ −3.5 dB @ 2.5 GHz ≥ −6.0 dB at 5.0 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	$\leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 21.392$ See Figure 3-62.
Integrated Differential Crosstalk on SuperSpeed (ISSXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}(\lvert Vin(f)\rvert^2\lvert NEXTs(f)\rvert^2 + \lvert Vdd(f)\rvert^2\lvert NEXTd(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXTs* = NEXT between SuperSpeed pairs *NEXTd* = NEXT between D+/D− and SuperSpeed pairs *Vdd(f)* = Input pulse spectrum on D+/D− pair, evaluated using equation shown in Figure 3-40 with Tb (UI) = 2.08 ns.	≤ −38 dB
Integrated Differential Crosstalk on D+/D- (IDDXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + \lvert FEXT(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXT* = Near-end crosstalk from SuperSpeed to D+/D− *FEXT* = Far-end crosstalk from SuperSpeed to D+/D− *fmax* = 1.2 GHz	≤ −28.5 dB

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-31 USB Type-C 至 ***USB 3.1*** Gen2 传统电缆组件的设计目标（参考）

Items	Design Targets
Differential Impedance	76 ohms min and 96 ohms max. 40 ps rise time (20%-80%).
Differential Insertion Loss	≥ −2 dB @ 100 MHz ≥ −4 dB @ 2.5 GHz, except for the USB Type-C plug to USB 3.1 Standard-A plug cable assembly which is ≥−3.5 dB @ 2.5 GHz −6.0 dB max @ 5.0 GHz
Differential NEXT between SuperSpeed Pairs	≤ −34 dB to 5 GHz
Differential NEXT and FEXT between D+/D- and SuperSpeed Pairs	≤ −30 dB to 5 GHz

规范要求包括表 3-30 中规定的 USB D+/D− 信号，以及表 3-32 中规定的超高速 USB 参数。

表 3-32 USB Type-C 至 ***USB 3.1*** Gen2 传统电缆组件信号完整性要求（规范）

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at both the SuperSpeed Gen1 and Gen2 Nyquist frequencies.	≥ −4 dB @ 2.5 GHz, except for the USB Type-C plug to USB 3.1 Standard-A plug cable assembly which is ≥ −3.5 dB @ 2.5 GHz ≥ −6.0 dB at 5.0 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	$\leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 21.392$ See Figure 3-62.
Integrated Differential Crosstalk on SuperSpeed (ISSXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}(\lvert Vin(f)\rvert^2\lvert NEXTs(f)\rvert^2 + \lvert Vdd(f)\rvert^2\lvert NEXTd(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: $NEXTs$ = NEXT between SuperSpeed pairs $NEXTd$ = NEXT between D+/D− and SuperSpeed pairs $Vdd(f)$ = Input pulse spectrum on D+/D− pair, evaluated using equation shown in Figure 3-40 with Tb (UI) = 2.08 ns.	≤ −38 dB
Integrated Differential Crosstalk on D+/D- (IDDXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + \lvert FEXT(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: $NEXT$ = Near-end crosstalk from SuperSpeed to D+/D− $FEXT$ = Far-end crosstalk from SuperSpeed to D+/D− $fmax$ = 1.2 GHz	≤ −28.5 dB

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Items	Descriptions and Procedures	Requirements
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	$\leq 0.046\cdot ILfitatNq^2 + 1.812\cdot ILfitatNq - 9.784$ See Figure 3-63.
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	≤ −20 dB

Note: *fmax* = 10 GHz (unless otherwise specified); *Vin(f)* is defined in Figure 3-40 with Tb (UI) = 100 ps; and *Vdd(f)* is also defined in Figure 3-40 with Tb (UI) = 2.08 ns.

Figure 3-62 IMR Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly

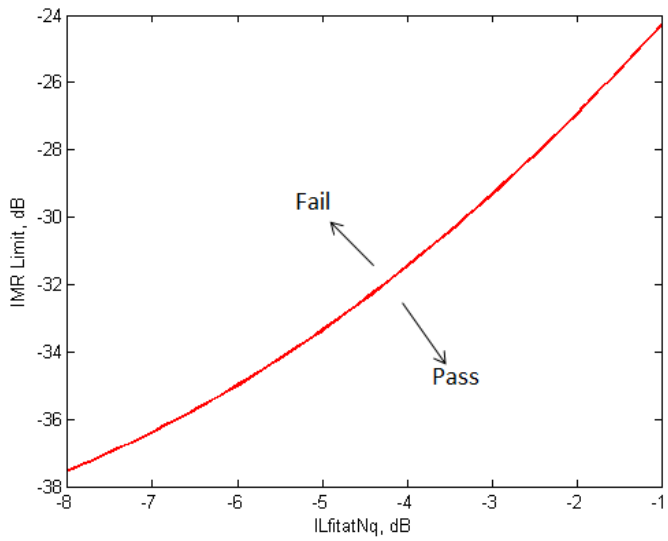
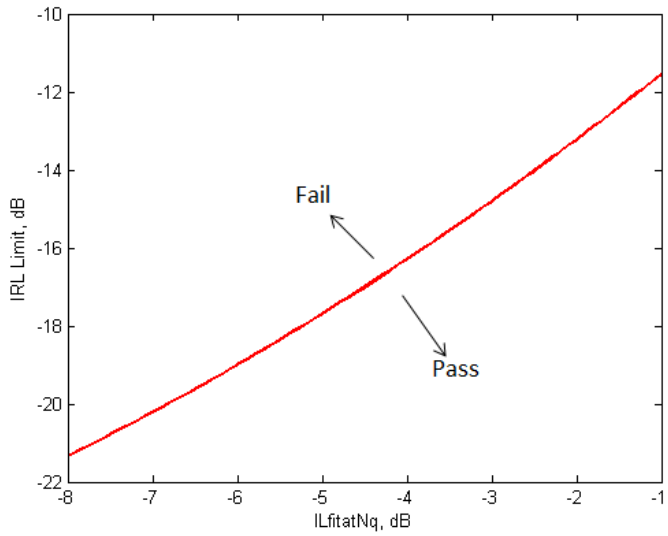


Figure 3-63 IRL Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Items	Descriptions and Procedures	Requirements
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	$\leq 0.046\cdot ILfitatNq^2 + 1.812\cdot ILfitatNq - 9.784$ See Figure 3-63.
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	≤ −20 dB

注意：$fmax$ = 10 GHz（除非另有说明）；$Vin(f)$ 在图 3-40 中定义为 Tb (UI) = 100 ps；$Vdd(f)$ 也在图 3-40 中定义为 Tb (UI) = 2.08 ns。

图 3-62 USB Type-C 转传统线缆组件的 IMR 限值与 ILfitatNq 的关系

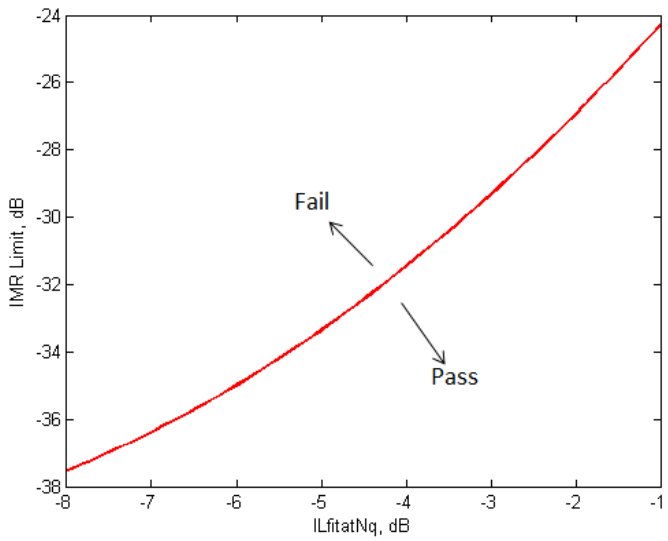
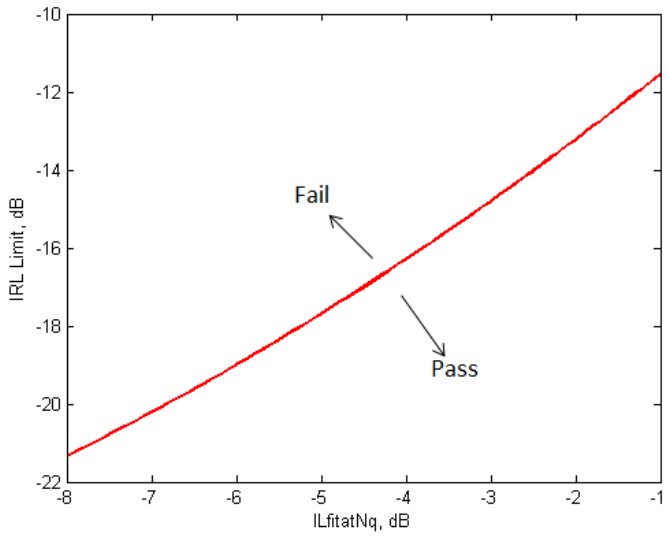


图 3-63 USB Type-C 转传统线缆组件的 IRL 限值与 ILfitatNq 的关系



版权所有 © 2019 USB 3.0 Promoter Group。保留所有权利。

3.7.5.3 Compliant USB Legacy Plugs used in USB Type-C to Legacy Cable Assemblies

The following requirements are incremental to the existing requirements for legacy connectors when used in compliant USB Type-C to legacy cable assemblies.

3.7.5.3.1 Contact Material Requirements for USB Type-C to USB Micro-B Assemblies

For USB Type-C to USB Micro-B assemblies, change the contact material in the USB Micro-B connector to achieve the following Low Level Contact Resistance (EIA 364-23B):

- 20 milliohms (Max) initial for VBUS and GND contacts,
- Maximum change (delta) of +10 milliohms after environmental stresses.

3.7.5.3.2 Contact Current Ratings for USB Standard-A, USB Standard-B and USB Micro-B Connector Mated Pairs (EIA 364-70, Method 2)

When a current of 3 A is applied to the VBUS pin and its corresponding GND pin (i.e., pins 1 and 4 in a USB Standard-A or USB Standard-B connector or pins 1 and 5 in a USB Micro-B connector), the delta temperature shall not exceed +30° C at any point on the connectors under test, when measured at an ambient temperature of 25° C.

3.7.6 USB Type-C to USB Legacy Adapter Assemblies (Normative)

Only the following standard legacy adapter assemblies are defined:

- *USB 2.0* Type-C plug to *USB 2.0* Micro-B receptacle
- USB Full-Featured Type-C plug to *USB 3.1* Standard-A receptacle

3.7.6.1 USB 2.0 Type-C Plug to *USB 2.0* Micro-B Receptacle Adapter Assembly (Normative)

This adapter assembly supports only the *USB 2.0* signaling. It shall not exceed 150 mm total length, measured from end to end. Table 3-33 defines the electrical requirements.

Table 3-33 USB D+/D− Signal Integrity Requirements for USB Type-C to Legacy USB Adapter Assemblies (Normative)

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the adapter assembly have the proper impedance. For the entire adaptor assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of adapter assembly arrive at the receiver at the same time.	20 ps max. 400 ps rise time (20%-80%).
Differential Insertion Loss	EIA 364 – 101 This test ensures the D+/D− pair of an adapter assembly can provide adequate signal strength to the receiver.	−0.7 dB max @ 400 MHz
D+ or D− DC Resistance	This test ensures the D+/D− has the proper DC resistance range in order to predict the EOP level and set the *USB 2.0* disconnect level.	2.5 ohms max.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.7.5.3 USB Type-C 转传统电缆组件中使用的兼容 USB 传统插头

当用于符合 USB Type-C 标准的传统电缆组件时，以下要求是对传统连接器现有要求的增量。

3.7.5.3.1 USB Type-C 至 USB Micro-B 组件的触点材料要求

对于 USB Type-C 至 USB Micro-B 组件，更改 USB Micro-B 连接器中的触点材料以实现以下低水平接触电阻 (EIA 364 -23B)：

对于 VBUS 和 GND 触点，• 初始值为 20 毫欧姆 (最大值)，环境压力之后，• 最大变化 (增量) 为 +10 毫欧姆。

3.7.5.3.2 USB 标准 A、USB 标准 B 和 USB Micro-B 连接器配对的接触电流额定值（EIA 364-70，方法 2）

当向 VBUS 引脚及其对应的 GND 引脚（即 USB 标准-A 或 USB 标准-B 连接器中的引脚 1 和 4，或 USB Micro-B 连接器中的引脚 1 和 5）施加 3 A 电流时，在 25°C 的环境温度下测量，被测连接器上任何一点的温差不得超过 +30°C。

3.7.6 USB Type-C 至 USB 传统适配器组件（规范）

仅定义了以下标准旧式适配器组件：

• *USB 2.0* Type-C 插头转 *USB 2.0* Micro-B 插座 • USB 全功能 Type-C 插头转 *USB 3.1* 标准 A 插座

3.7.6.1 USB 2.0 Type-C 插头至 ***USB 2.0*** Micro-B 插座适配器组件（规范）

此适配器组件仅支持 *USB 2.0* 信号。总长不得超过 150 毫米长度，从一端到另一端测量。表 3-33 定义了电气要求。

表 3-33 USB Type-C 至传统 USB 适配器组件的 USB D+/D− 信号完整性要求（规范）

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the adapter assembly have the proper impedance. For the entire adaptor assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of adapter assembly arrive at the receiver at the same time.	20 ps max. 400 ps rise time (20%-80%).
Differential Insertion Loss	EIA 364 – 101 This test ensures the D+/D− pair of an adapter assembly can provide adequate signal strength to the receiver.	−0.7 dB max @ 400 MHz
D+ or D− DC Resistance	This test ensures the D+/D− has the proper DC resistance range in order to predict the EOP level and set the *USB 2.0* disconnect level.	2.5 ohms max.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.7.6.2 USB Full-Featured Type-C Plug to *USB 3.1* Standard-A Receptacle Adapter Assembly (Normative)

The USB Full-Featured Type-C plug to *USB 3.1* Standard–A receptacle adapter assembly is intended to be used with a direct-attach device (e.g., USB thumb drive). A system is not guaranteed to function when using an adapter assembly together with a Standard USB cable assembly.

To minimize the impact of the adapter assembly to system signal integrity, the adapter assembly should meet the informative design targets in Table 3-34.

Table 3-34 Design Targets for USB Type-C to *USB 3.1* Standard-A Adapter Assemblies (Informative)

Items	Design Targets
Differential Return Loss	≤ −15 dB to 5 GHz Normalized with 85 ohms.
Differential Insertion Loss	≥ −2.4 dB to 2.5 GHz, ≥ −3.5 dB to 5 GHz
Differential NEXT between SuperSpeed Pairs	≤ −40 dB to 2.5 GHz ≤ −34 dB at 5 GHz
Differential NEXT and FEXT between D+/D− and SuperSpeed Pairs	≤ −30 dB to 2.5 GHz

The normative requirements for the adapter assembly are defined in Table 3-33 and Table 3-35. The adapter assembly total length is limited to 150 mm max.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.7.6.2 USB 全功能 Type-C 插头至 ***USB 3.1*** 标准 A 插座适配器组件（规范）

USB 全功能 Type-C 插头至 *USB 3.1* 标准 – A 插座适配器组件旨在与直接连接设备（例如 USB 拇指驱动器）一起使用。当将适配器组件与标准 USB 电缆组件一起使用时，不能保证系统正常运行。

为了尽量减少适配器组件对系统信号完整性的影响，适配器组件应满足表3-34中的设计目标
。

表 3-34 USB Type-C 至 ***USB 3.1*** 标准 A 适配器组件的设计目标（参考）

Items	Design Targets
Differential Return Loss	≤ −15 dB to 5 GHz Normalized with 85 ohms.
Differential Insertion Loss	≥ −2.4 dB to 2.5 GHz, ≥ −3.5 dB to 5 GHz
Differential NEXT between SuperSpeed Pairs	≤ −40 dB to 2.5 GHz ≤ −34 dB at 5 GHz
Differential NEXT and FEXT between D+/D− and SuperSpeed Pairs	≤ −30 dB to 2.5 GHz

适配器组件的规范要求定义在表 3-33 和表 3-35 中。适配器组件总长度最大限制为 150 mm。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 3-35 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly Signal Integrity Requirements (Normative)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequency (ILfitatNq)	ILfitatNq is evaluated at the SuperSpeed Gen1 Nyquist frequency.	≥ −2.4 dB at 2.5 GHz ≥ −3.5 dB at 5 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −38 dB, Tb = 200 ps ≤ −27 dB, Tb = 100 ps
Integrated Differential Crosstalk on SuperSpeed (ISSXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}(\lvert Vin(f)\rvert^2\lvert NEXTs(f)\rvert^2 + \lvert Vdd(f)\rvert^2\lvert NEXTd(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: $NEXTs$ = NEXT between SuperSpeed pairs $NEXTd$ = NEXT between D+/D− and SuperSpeed pairs $Vdd(f)$ = Input pulse spectrum on D+/D− pair, evaluated using equation shown in Figure 3-40 with Tb (UI) = 2.08 ns.	≤ −37 dB
Integrated Differential Crosstalk on D+/D- (IDDXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + \lvert FEXT(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: $NEXT$ = Near-end crosstalk from SuperSpeed to D+/D− $FEXT$ = Far-end crosstalk from SuperSpeed to D+/D− f_{max} = 1.2 GHz	≤ −30 dB
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −14.5 dB, Tb = 200 ps ≤ −12.0 dB, Tb = 100 ps
Diff to Comm mode	Differential to Common Mode conversion (SCD12, SCD21)	≤ −15 dB

Note: *fmax* = 7.5 GHz; *Vin(f)* is defined in Figure 3-40 with Tb (UI) = 200 ps; and *Vdd(f)* is also specified in Figure 3-40 with Tb (UI) = 2.08 ns.

3.7.6.3 Compliant USB Legacy Receptacles used in USB Type-C to Legacy Adapter Assemblies

3.7.6.3.1 Contact Material Requirements

Refer to Section 3.7.5.3.1 for contact material requirements as these apply to legacy USB Standard-A and USB Micro-B receptacles used in USB Type-C to Legacy Adapter Assemblies.

3.7.6.3.2 Contact Current Ratings

Refer to Section 3.7.5.3.2 for contact current rating requirements as these apply to legacy USB Standard-A and USB Micro-B receptacles used in USB Type-C to Legacy Adapter Assemblies.

3.7.7 Shielding Effectiveness Requirements (Normative)

The cable assembly shielding effectiveness (SE) test measures the EMI and RFI levels from the cable assembly. To perform the measurement, the cable assembly shall be installed in the cable SE test fixture as shown in Figure 3-64. The coupling factors from the cable to the fixture are characterized with a VNA.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 3-35 USB Type-C 至 ***USB 3.1*** 标准 A 插座适配器组件信号完整性要求（规范性）

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequency (ILfitatNq)	ILfitatNq is evaluated at the SuperSpeed Gen1 Nyquist frequency.	≥ −2.4 dB at 2.5 GHz ≥ −3.5 dB at 5 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −38 dB, Tb = 200 ps ≤ −27 dB, Tb = 100 ps
Integrated Differential Crosstalk on SuperSpeed (ISSXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}(\lvert Vin(f)\rvert^2\lvert NEXTs(f)\rvert^2 + \lvert Vdd(f)\rvert^2\lvert NEXTd(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: $NEXTs$ = NEXT between SuperSpeed pairs $NEXTd$ = NEXT between D+/D− and SuperSpeed pairs $Vdd(f)$ = Input pulse spectrum on D+/D− pair, evaluated using equation shown in Figure 3-40 with Tb (UI) = 2.08 ns.	≤ −37 dB
Integrated Differential Crosstalk on D+/D- (IDDXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + \lvert FEXT(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: $NEXT$ = Near-end crosstalk from SuperSpeed to D+/D− $FEXT$ = Far-end crosstalk from SuperSpeed to D+/D− f_{max} = 1.2 GHz	≤ −30 dB
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −14.5 dB, Tb = 200 ps ≤ −12.0 dB, Tb = 100 ps
Diff to Comm mode	Differential to Common Mode conversion (SCD12, SCD21)	≤ −15 dB

注意：$fmax$ = 7.5 GHz；$Vin(f)$ 在图 3-40 中定义为 Tb (UI) = 200 ps；$Vdd(f)$ 也在图 3-40 中指定，其 Tb (UI) = 2.08 ns。

3.7.6.3 USB Type-C 转传统适配器组件中使用的兼容 USB 传统插座

3.7.6.3.1 接触件材料要求

请参阅第 3.7.5.3.1 节了解接触材料要求，因为这些要求适用于 USB Type-C 至传统适配器组件中使用的传统 USB 标准 A 和 USB Micro-B 插座。

3.7.6.3.2 触点电流额定值

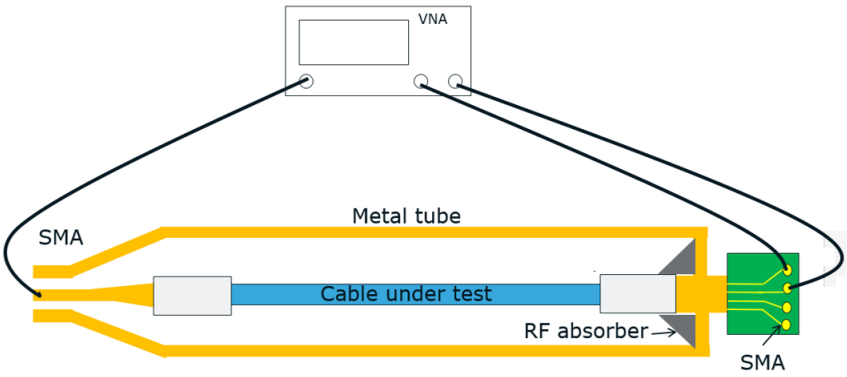
请参阅第 3.7.5.3.2 节了解接触电流额定值要求，因为这些要求适用于 USB Type-C 至传统适配器组件中使用的传统 USB 标准 A 和 USB Micro-B 插座。

3.7.7 屏蔽效能要求（规范）

电缆组件屏蔽效果 (SE) 测试测量电缆组件的 EMI 和 RFI 水平。要进行测量，应将电缆组件安装在电缆 SE 测试夹具中，如图 3-64 所示。从电缆到夹具的耦合系数用 VNA 来表征。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

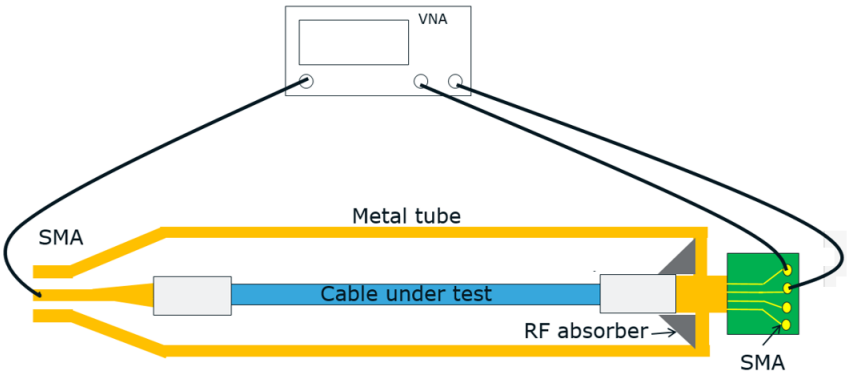
Figure 3-64 Cable Assembly Shielding Effectiveness Testing



All USB Type-C cable assemblies shall pass the shielding effectiveness test for compliance. Figure 3-65 shows the pass/fail criteria for (a) USB Type-C to USB Type-C cable assemblies, (b) USB Type-C to legacy USB cable assemblies, and (c) the USB Type-C to *USB 3.1* Standard-A Receptacle Adapter assembly. Note that the shielding effectiveness for the frequency band from 4 GHz to 5 GHz is not specified since there is no antenna operating in this frequency range.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-64 电缆组件屏蔽效能测试

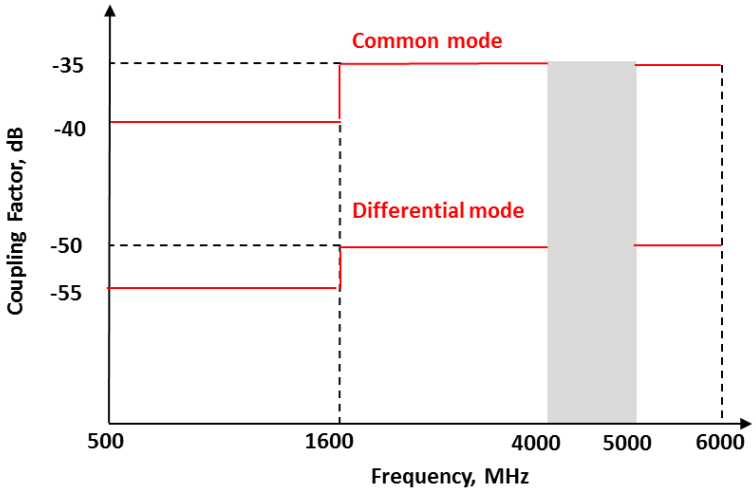


所有 USB Type-C 电缆组件均应通过屏蔽效能测试，以确保合规。图 3-65 显示了 (a) USB Type-C 至 USB Type-C 电缆组件、(b) USB Type-C 至传统 USB 电缆组件和 (c) USB Type-C 至 *USB 3.1* 标准 A 插座适配器组件的通过/失败标准。请注意，频段的屏蔽效能

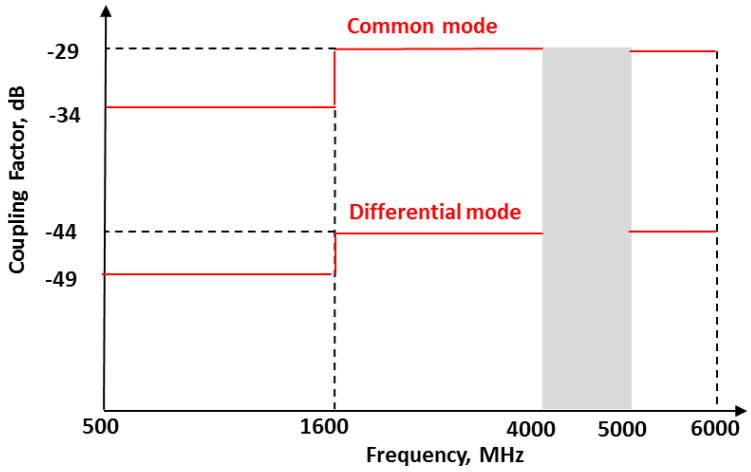
没有指定 4 GHz 至 5 GHz，因为在此频率范围内没有工作的天线。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

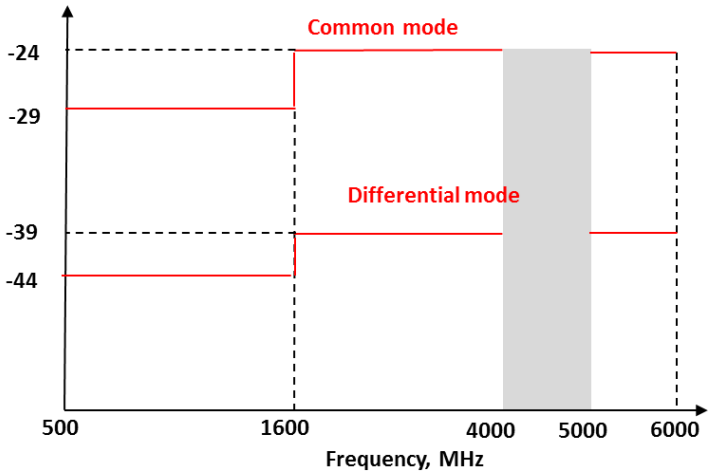
Figure 3-65 Shielding Effectiveness Pass/Fail Criteria



(a) For USB Type-C to USB Type-C Cable Assemblies



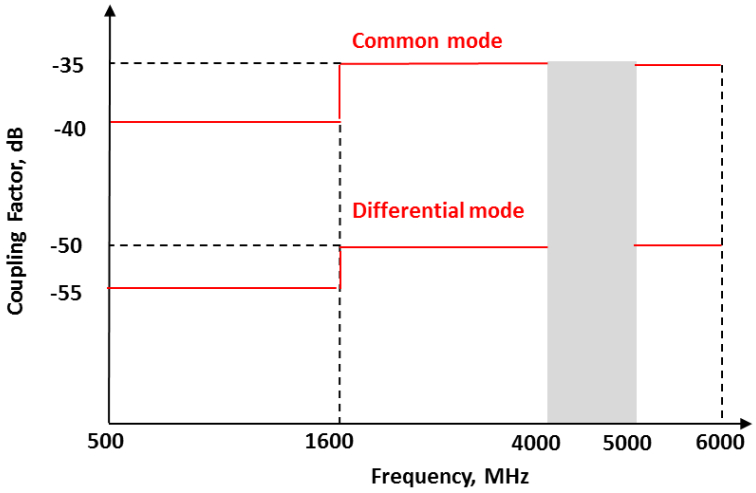
(b) For USB Type-C to legacy USB Cable Assemblies



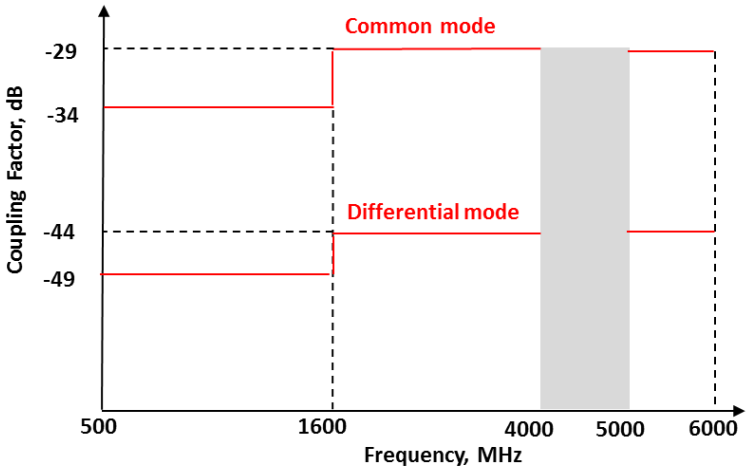
(c) For USB Type-C to USB3.1 Standard-A Receptacle Adapter Assembly

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

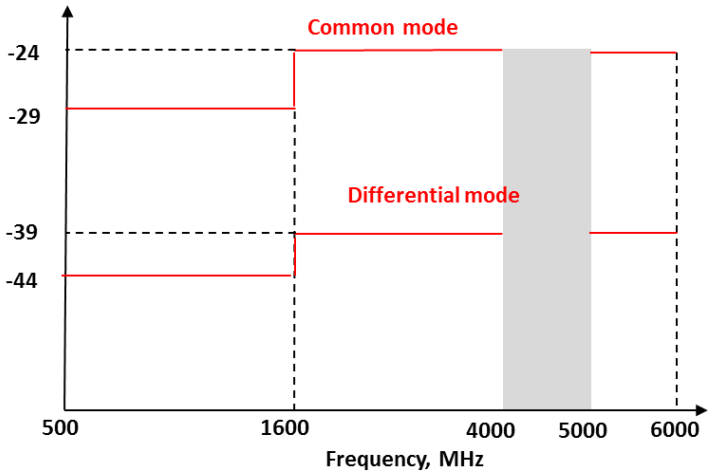
图 3-65 屏蔽效能通过/失败标准



(a) For USB Type-C to USB Type-C Cable Assemblies



(b) For USB Type-C to legacy USB Cable Assemblies



(c) For USB Type-C to USB3.1 Standard-A Receptacle Adapter Assembly

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.7.8 DC Electrical Requirements (Normative)

Unless otherwise stated, the tests in this section are performed on mated connector pairs.

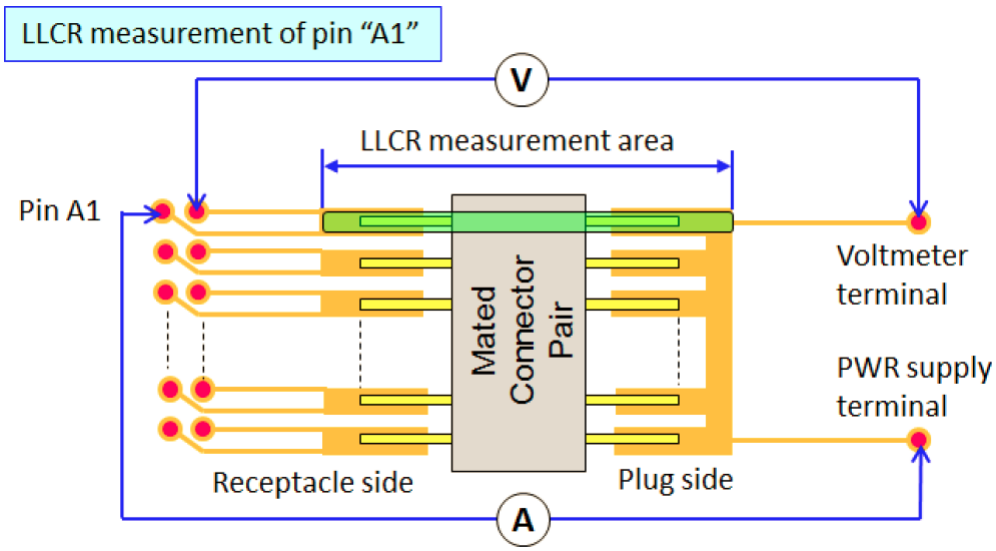
3.7.8.1 Low Level Contact Resistance (EIA 364-23B)

The low level contact resistance (LLCR) measurement is made across the plug and receptacle mated contacts and does not include any internal paddle cards or substrates of the plug or receptacle. See Figure 3-66. The following apply to the power and signal contacts:

- 40 mΩ (Max) initial for VBUS, GND and all other contacts.
- 50 mΩ (Max) after environmental stresses.
- Measure at 20 mV (Max) open circuit at 100 mA.

Refer to Section 3.8 for environmental requirements and test sequences.

Figure 3-66 LLCR Measurement Diagram



3.7.8.2 Dielectric Strength (EIA 364-20)

No breakdown shall occur when 100 Volts AC (RMS) is applied between adjacent contacts of unmated and mated connectors.

3.7.8.3 Insulation Resistance (EIA 364-21)

A minimum of 100 MΩ insulation resistance is required between adjacent contacts of unmated and mated connectors.

3.7.8.4 Contact Current Rating

The current rating testing for the USB Type-C connector (plug and receptacle) shall be conducted per the following set up and procedures:

- A current of 5 A shall be applied collectively to VBUS pins (i.e., pins A4, A9, B4, and B9) and 1.25 A shall be applied to the VCONN pin (i.e., B5) as applicable, terminated through the corresponding GND pins (i.e., pins A1, A12, B1, and B12). A minimum current of 0.25 A shall also be applied individually to all the other contacts, as applicable. When current is applied to the contacts, the temperature of the connector pair shall be allowed to stabilize. The temperature rise of the outside

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.7.8 直流电气要求（规范）

除非另有说明，本节中的测试均在配对的连接器上进行。

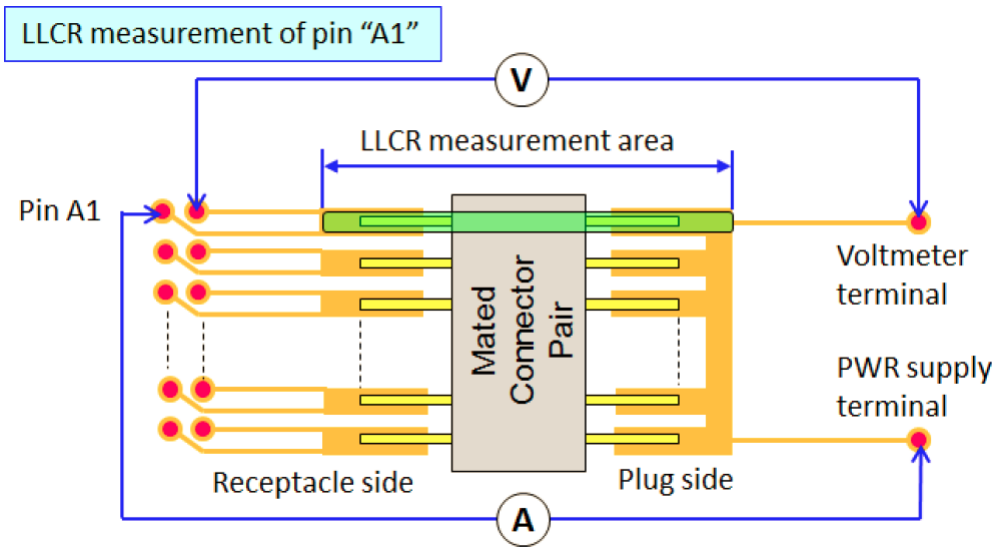
3.7.8.1 低水平接触电阻（EIA 364-23B）

低电平接触电阻 (LLCR) 测量是在插头和插座配对触点之间进行的，不包括插头或插座的任何内部插卡或基板。参见图 3-66。以下内容适用于电源和信号触点：

- VBUS、GND 和所有其他触点的初始值为 40 mΩ（最大值）。
- 环境压力后为 50 mΩ（最大值）。• 在 100 mA 下测量 20 mV（最大值）开路。

参见 3.8 环境要求及测试顺序 条件。

图 3-66 LLCR 测量图



3.7.8.2 介电强度（EIA 364-20）

在未配对和配对连接器的相邻触点之间施加 100 伏交流电 (RMS) 时，不得发生击穿。

3.7.8.3 绝缘电阻（EIA 364-21）

未配对和配对连接器的相邻触点之间至少需要 100 MΩ 的绝缘电阻。

3.7.8.4 触点电流额定值

USB Type-C 连接器（插头和插座）的额定电流测试应按照以下设置和程序进行：

- 应将 5 A 电流集体施加到 VBUS 引脚（即引脚 A4、A9、B4 和 B9），并将 1.25 A 电流施加到 VCONN 引脚（即 B5）（如适用），通过相应的 GND 引脚（即引脚 A1、A12、B1 和 B12）终止。还应将最小 0.25 A 电流单独施加到所有其他触点（如适用）。当电流施加到触点时，应允许连接器对的温度稳定下来。外部温度升高

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

shell surface of the mated pair above the VBUS and GND contacts shall not exceed 30 °C above the ambient temperature. Figure 3-67 provides an illustration of the measurement location.

- The measurement shall be done in still air.
- The connectors shall be oriented such that the accessible outer shell surface is on top and horizontal to the ground.
- The plug and receptacle may require modification to access solder tails or cable attachment points.
- Either thermocouple or thermo-imaging (preferred) method may be used for temperature measurement
- For certification, the connector manufacturer shall provide the receptacle and plug samples under test mounted on a current rating test PCB with no copper planes. A cable plug may use short wires to attach the cable attachment points together rather than using a current rating test PCB.
    - The current rating test PCBs shall be of a 2-layer construction. If 2-layer construction is not possible due to the solder tail configuration, VBUS and ground traces shall be located on the outer layers with the inner layers reserved for signal traces, as required; VCONN traces may be routed either on internal or external layers. Table 3-36 defines the requirements for the test PCB thickness and traces. The trace length applies to each PCB (receptacle PCB and plug PCB) and is from the contact terminal to the current source tie point. Figure 3-68 provides an informative partial trace illustration of the current rating test PCB.
    - If short wires are used instead of a current rating test PCB, the wire length shall not exceed 70 mm, measured from the plug contact solder point to the other end of the wire. There shall be no paddle card or overmold included in the test set-up. Each plug solder tail shall be attached with a wire with the wire gauge of AWG 36 for signals, AWG 32 for power (VBUS and VCONN), and AWG 30 for ground.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

VBUS 和 GND 触点上方的配对外壳表面温度不得超过环境温度 30 °C。图 3-67 提供了测量位置的图示。

- 测量应在静止的空气中进行。
- 连接器的放置位置应使得可触及的外壳表面位于顶部并与地面水平。
- 插头和插座可能需要修改才能接触到焊尾或电缆连接点。
- 可以使用热电偶或热成像（首选）方法进行温度测量
- 为了获得认证，连接器制造商应提供安装在无铜平面的额定电流测试 PCB 上的受测插座和插头样品。电缆插头可以使用短线将电缆连接点连接在一起，而不是使用额定电流测试 PCB。

  o 额定电流测试 PCB 应为 2 层结构。如果由于焊尾配置而无法采用 2 层结构，则 V BUS 和接地线迹应位于外层，内层保留用于信号线迹（根据需要）；VCONN 线迹可以布线在内层或外层。表 3-36 定义了测试 PCB 厚度和线迹的要求。线迹长度适用于每个 PCB（插座 PCB 和插头 PCB），从接触端子到电流源连接点。图 3-68 提供了额定电流测试 PCB 的有用部分线迹图示。

  o 如果使用短线代替额定电流测试 PCB，则线长不得超过 70 毫米（从插头接触焊点到线的另一端测量）。测试装置中不得包含插卡或包覆成型件。每个插头焊尾都应连接一根线，线规为 AWG 36（用于信号）、AWG 32（用于电源（VBUS 和 VCONN））和 AWG 30（用于接地）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-67 Temperature Measurement Point

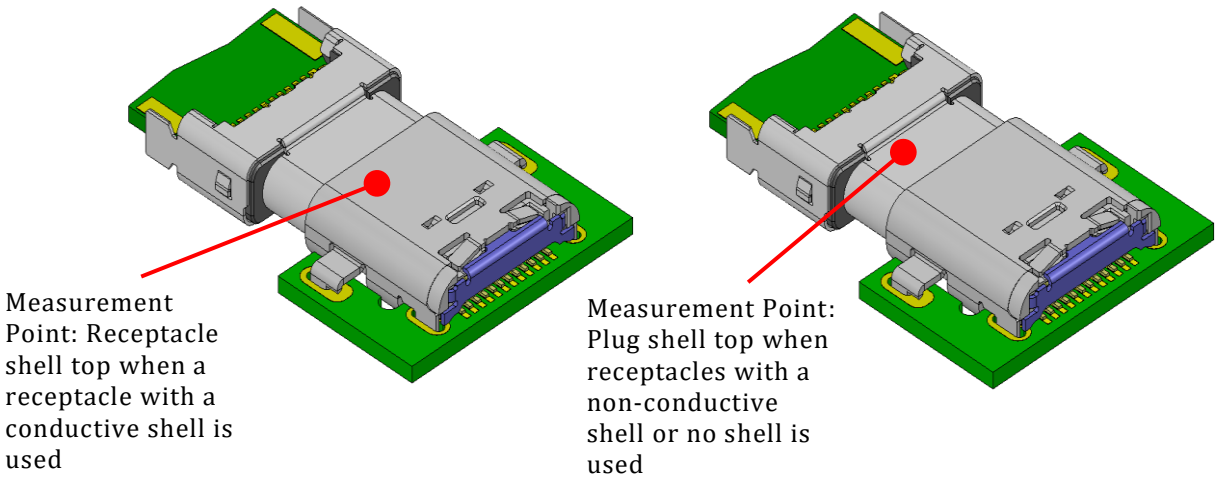


Table 3-36 Current Rating Test PCB

Item	Trace width (mm)	Trace length (mm) on each PCB	Thickness
Signal trace	0.25 max.	13 max.	35 µm (1 oz. copper)
Ground trace	1.57 max.	38 max.	35 µm (1 oz. copper)
VBUS and VCONN	1.25 max.	30 max.	35 µm (1 oz. copper)
PCB	N/A	N/A	0.80 – 1.20 mm

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-67 温度测量点

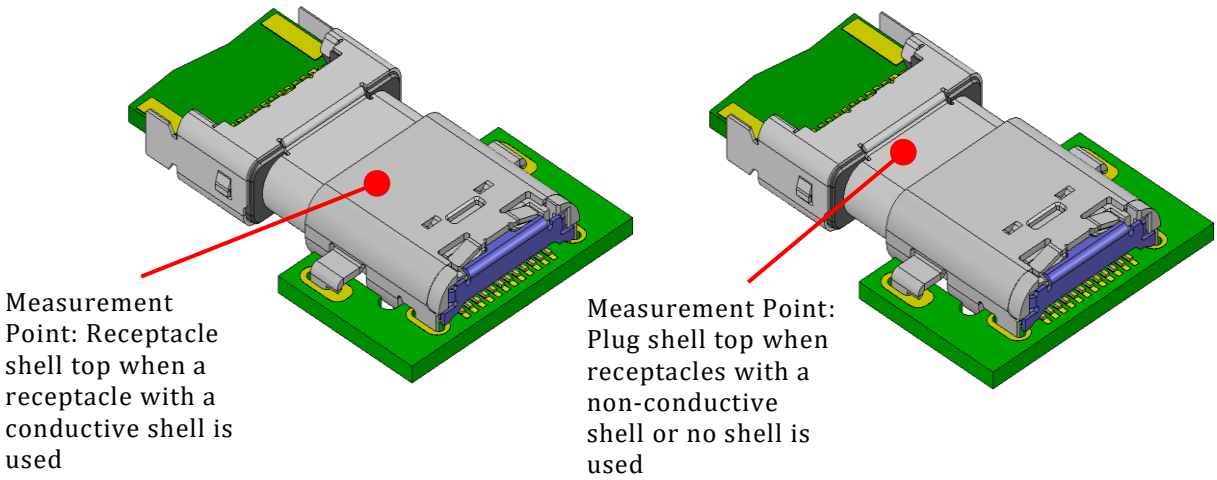
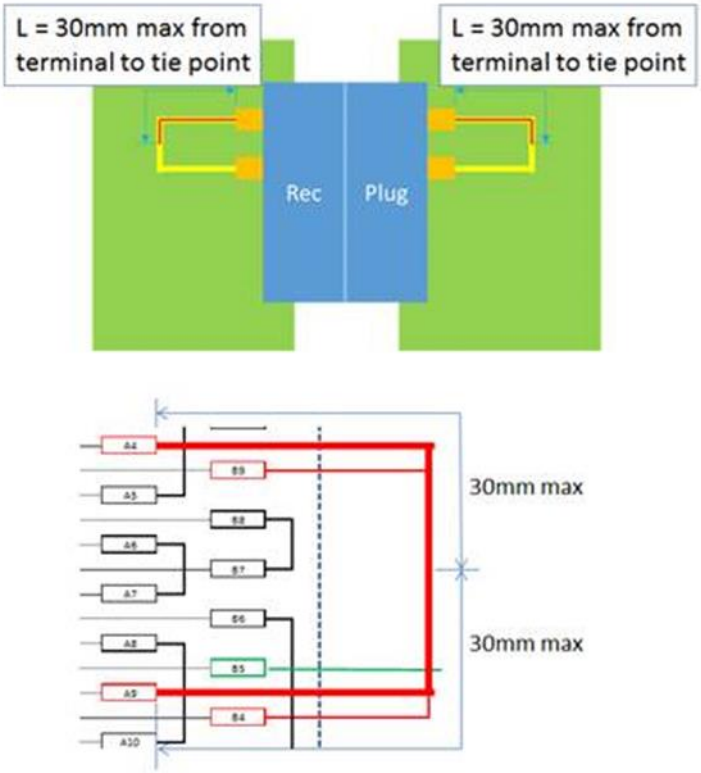


表 3-36 电流额定值测试 PCB

Item	Trace width (mm)	Trace length (mm) on each PCB	Thickness
Signal trace	0.25 max.	13 max.	35 µm (1 oz. copper)
Ground trace	1.57 max.	38 max.	35 µm (1 oz. copper)
VBUS and VCONN	1.25 max.	30 max.	35 µm (1 oz. copper)
PCB	N/A	N/A	0.80 – 1.20 mm

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-68 Example Current Rating Test Fixture Trace Configuration



3.7.8.5 DC Resistance of D+ and D−

The DC Resistance of the D+ and D− in *USB 2.0* High-Speed capable USB Type-C devices and *USB 2.0* High-Speed capable USB Type-C Captive devices shall be equal or less than the maximum value specified in Table 3-37. The D+ and D− DC Resistance is the series combination of any resistance in switches, multiplexers, and the USB PHY.

Table 3-37 Maximum DC Resistance Requirement (Normative)

	Maximum DC Resistance
USB Type-C Device (USB 2.0 High-speed capable)	19 Ω
USB Type-C Captive Device (USB 2.0 High-speed capable)	25 Ω

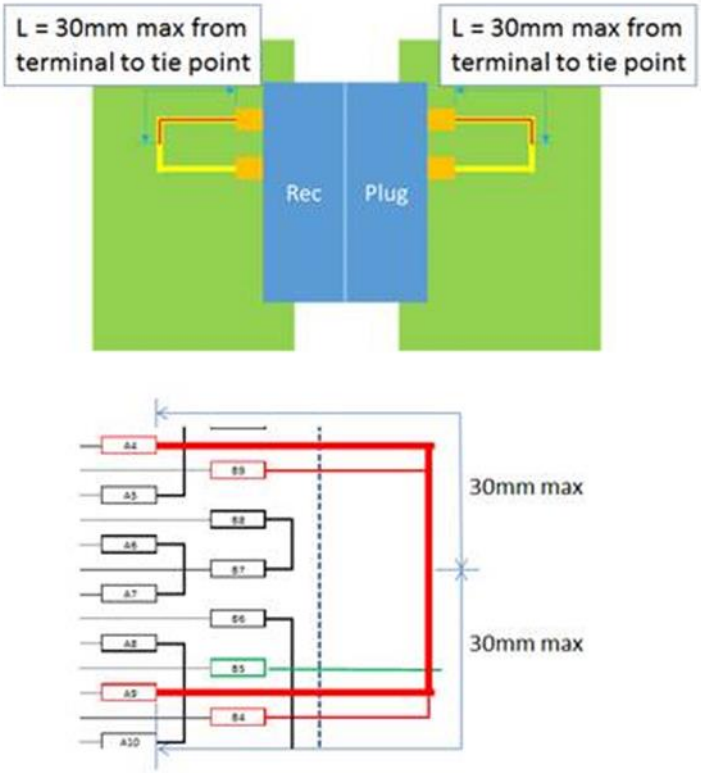
A USB Type-C Host operating in *USB 2.0* High-Speed mode shall implement a disconnect threshold voltage (V_{HSDSC}) level as defined in the *USB 2.0* DCR ECN.

3.8 Mechanical and Environmental Requirements (Normative)

The requirements in this section apply to all USB Type-C connectors and/or cable assemblies unless otherwise specified. For USB Type-C plug connectors and cable assemblies, the test methods are based on an assumption that the cable exits the overmold in line with mating direction to a USB Type-C receptacle (i.e., straight out the back of the overmold). For USB Type-C plug connectors and cable assemblies with the cable exiting the overmold in a different direction than straight out the back (e.g., right angle to the mating direction), test fixtures and procedures shall be modified as required to accomplish the measurement.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-68 电流额定值测试夹具走线配置示例



3.7.8.5 D+ 和 D– 的直流电阻

具有 *USB 2.0* 高速能力的 USB Type-C 设备和具有 *USB 2.0* 高速能力的 USB Type-C 固定设备中的 D+ 和 D– 的直流电阻应等于或小于表 3-37 中规定的最大值。D+ 和 D– 直流电阻是开关、多路复用器和 USB PHY 中任意电阻的串联组合。

表 3-37 最大直流电阻要求（标准）

	Maximum DC Resistance
USB Type-C Device (USB 2.0 High-speed capable)	19 Ω
USB Type-C Captive Device (USB 2.0 High-speed capable)	25 Ω

在 *USB 2.0* 高速模式下运行的 USB Type-C 主机应实现 *USB 2.0* DCR ECN 中定义的断开阈值电压 (V_{HSDSC}) 水平。

3.8 机械和环境要求（规范）

除非另有规定，本节中的要求适用于所有 USB Type-C 连接器和/或电缆组件。对于 USB Type-C 插头连接器和电缆组件，测试方法基于以下假设：电缆从包覆成型件中出来时的方向与 USB Type-C 插座的插接方向一致（即，直接从包覆成型件的背面出来）。对于电缆从包覆成型件中出来时的方向与直接从背面出来时不同（例如，与插接方向成直角）的 USB Type-C 插头连接器和电缆组件，应根据需要修改测试夹具和程序以完成测量。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.8.1 Mechanical Requirements

3.8.1.1 Insertion Force (EIA 364-13)

The initial connector insertion force shall be within the range from 5 N to 20 N at a maximum rate of 12.5 mm (0.492") per minute. This requirement does not apply when the connectors are used in a docking application.

It is recommended to use a non-silicone based lubricant on the latching mechanism to reduce wear. The effects of lubricants should be restricted to insertion and extraction characteristics and should not increase the resistance of the mated connection.

3.8.1.2 Extraction Force (EIA 364-13)

The initial connector extraction force shall be within the range of 8 N to 20 N, measured after a preconditioning of five insertion/extraction cycles (i.e., the sixth extraction). After an additional twenty-five insertion/extraction cycles, the extraction force shall be measured again (i.e., the thirty-second extraction) and the extraction force shall be:

a. within 33% of the initial reading, and
b. within the range of 8 N to 20 N.

The extraction force shall be within the range of 6 N to 20 N after 10,000 insertion/ extraction cycles. The extraction force measurement shall be performed at a maximum speed of 12.5 mm (0.492”) per minute. The extraction force requirement does not apply when the connectors are used in a mechanical docking application.

It is recommended to use a non-silicone based lubricant on the latching mechanism to reduce wear. The effects of lubricants should be restricted to insertion and extraction characteristics and should not increase the resistance of the mated connection.

3.8.1.3 Durability or Insertion/Extraction Cycles (EIA 364-09)

The durability rating shall be 10,000 cycles minimum for the USB Type-C connector family. The durability test shall be done at a rate of 500 ± 50 cycles per hour and no physical damage to any part of the connector and cable assembly shall occur.

3.8.1.4 Cable Flexing (EIA 364-41, Condition 1)

No physical damage or discontinuity over 1ms during flexing shall occur to the cable assembly with Dimension X = 3.7 times the cable diameter and 100 cycles in each of two planes.

3.8.1.5 Cable Pull-Out (EIA 364-38, Method A)

No physical damage to the cable assembly shall occur when it is subjected to a 40 N axial load for a minimum of 1 minute while clamping one end of the cable plug.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.8.1 机械要求

3.8.1.1 插入力（EIA 364-13）

连接器的初始插入力应在 5 N 至 20 N 范围内，最大插入速率为每分钟 12.5 毫米 (0.492")。当连接器用于对接应用时，此要求不适用。

建议在锁扣机构上使用非硅基润滑剂以减少磨损。润滑剂的影响应仅限于插入和拔出特性，不应增加配合连接的阻力。

3.8.1.2 拔出力（EIA 364-13）

连接器的初始拔出力应在 8 N 至 20 N 范围内，在预处理五次插入/拔出循环（即第六次拔出）后进行测量。在额外的二十五次插入/拔出循环之后，应再次测量拔出力（即第三十二次拔出），拔出力应为：

a. 在初始读数的 33% 以内，并且 b. 在 8 N 至
20 N 的范围内。

经过 10,000 次插入/拔出循环后，拔出力应在 6 N 至 20 N 范围内。拔出力测量应以每分钟 12.5 毫米 (0.492 ”) 的最大速度进行。当连接器用于机械对接应用时，拔出力要求不适用。

建议在锁扣机构上使用非硅基润滑剂以减少磨损。润滑剂的影响应仅限于插入和拔出特性，不应增加配合连接的阻力。

3.8.1.3 耐久性或插入/拔出循环（EIA 364 -09）

USB Type-C 连接器系列的耐久性等级至少应为 10,000 次循环。
耐久性试验应以每小时 500 次（50 个循环）的速度进行，并且连接器和电缆组件的任何部分都不得发生物理损坏。

3.8.1.4 电缆弯曲（EIA 364-41，条件 1）

电缆组件尺寸 X = 为电缆直径的 3.7 倍，在两个平面上各弯曲 100 次，在弯曲过程中不得发生超过 1 毫秒的物理损坏或不连续现象。

3.8.1.5 电缆拉出（EIA 364-38，方法 A）

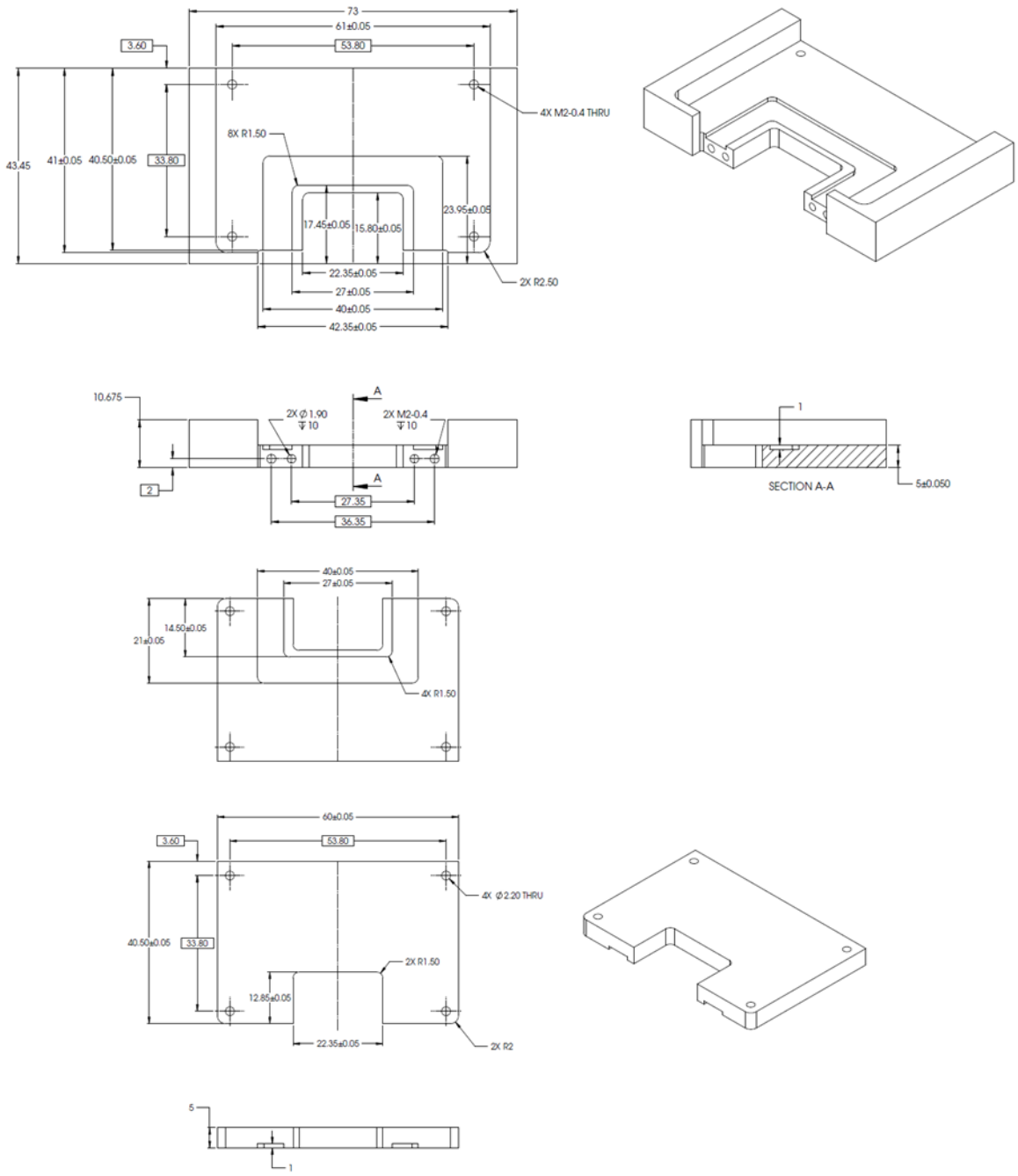
当 夹紧 电缆 插头 的 一端 并 使其 承受 40N 轴向 负载 至少 1 分钟 时 , 电缆 组件 不得 发生 物理 损坏 .

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.8.1.6 4-Axis Continuity Test

The USB Type-C connector family shall be tested for continuity under stress using a test fixture shown in Figure 3-69 or equivalent.

Figure 3-69 Example of 4-Axis Continuity Test Fixture

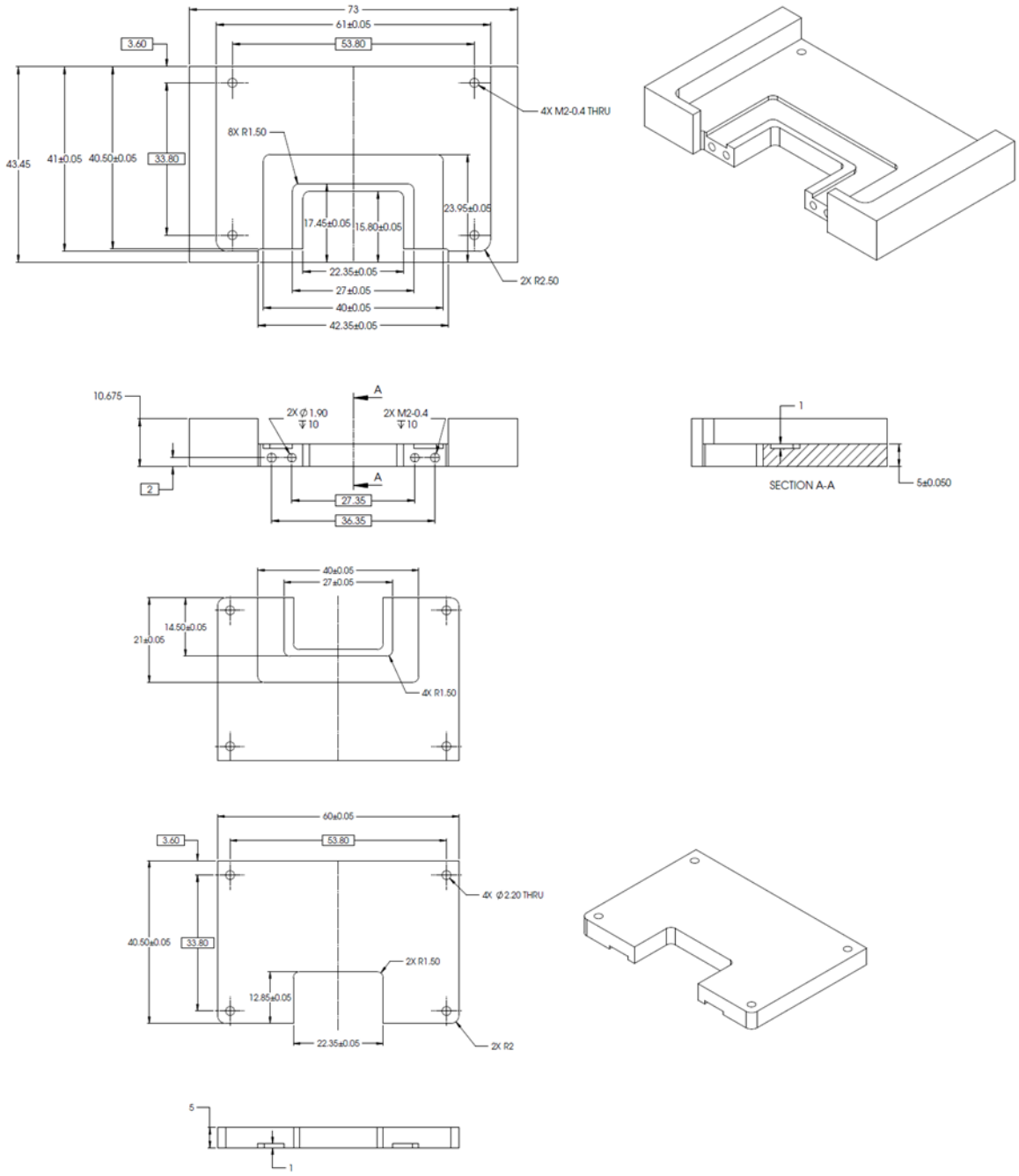


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.8.1.6 4 轴连续性测试

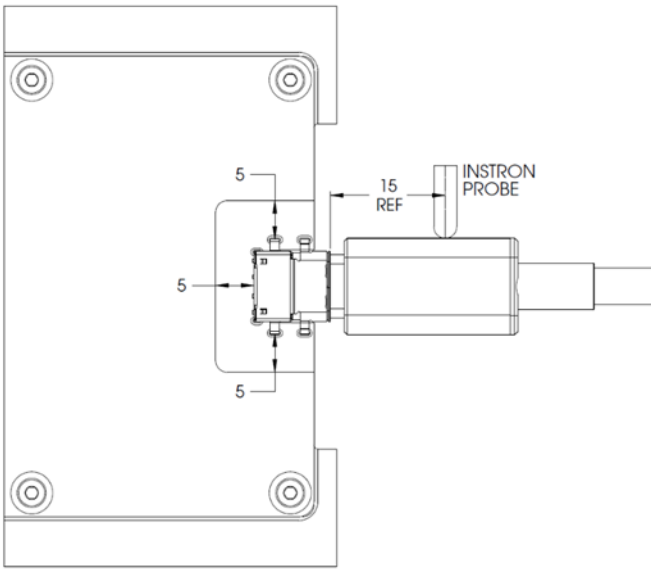
USB Type-C 连接器系列应使用图 3-69 所示的测试夹具或等效装置进行压力下的连续性测试。

图 3-69 4 轴连续性测试夹具示例



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-60 Example of 4-Axis Continuity Test Fixture, cont.



Plugs shall be supplied with a representative overmold or mounted on a 2 layer printed circuit board (PCB) between 0.8 mm and 1.0 mm thickness as applicable. A USB Type-C receptacle shall be mounted on a 2 layer PCB between 0.8 mm and 1.0 mm thickness. The PCB shall be clamped on three sides of the receptacle no further than 5 mm away from the receptacle outline. The receptacle PCB shall initially be placed in a horizontal plane, and a perpendicular moment shall be applied to the plug with a 5 mm ball tipped probe for a period of at least 10 seconds at a distance of 15 mm from the mating edge of the receptacle shell in a downward direction, perpendicular to the axis of insertion. See Table 3-38 for the force and moment to be applied. Any configuration of non-conductive shell receptacles shall be tested at the values specified for the vertical receptacle configuration.

Table 3-38 Force and Moment Requirements

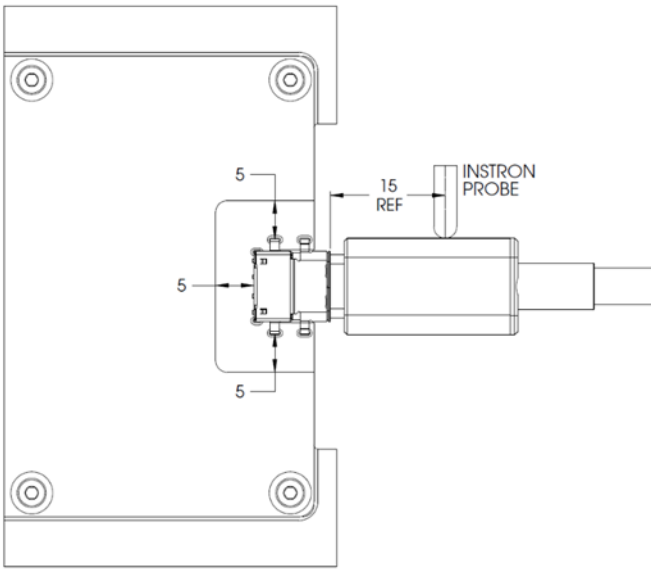
Receptacle configuration with respect to mounting surface	Force at 15 mm from receptacle shell mating edge (N)	Moment with respect to receptacle shell mating edge (Nm)
Right angle	20	0.30
Vertical[1]	8	0.12

Notes:
1. Any configuration of non-conductive shell receptacles shall be tested at the values specified for the vertical receptacle configuration.

The continuity across each contact shall be measured throughout the application of the tensile force. Each non-ground contact shall also be tested to confirm that it does not short to the shell during the stresses. The PCB shall then be rotated 90 degrees such that the cable is still inserted horizontally and the tensile force in Table 3-38 shall be applied again in the downward direction and continuity measured as before. This test is repeated for 180 degree and 270 degree rotations. Passing parts shall not exhibit any discontinuities or shorting to the shell greater than 1 µs duration in any of the four orientations.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-60 4 轴连续性测试夹具示例（续）



插头应配备代表性的包覆成型件或安装在厚度在 0.8 mm 至 1.0 mm 之间的 2 层印刷电路板 (PCB) 上（视情况而定）。USB Type-C 插座应安装在厚度在 0.8 mm 至 1.0 mm 之间的 2 层 PCB 上。PCB 应夹在插座的三侧，距离插座轮廓不超过 5 mm。插座 PCB 应首先放置在水平面上，使用 5 mm 球头探针在距离插座外壳配合边缘 15 mm 处向下垂直于插入轴施加垂直力矩至少 10 秒。有关要施加的力和力矩，请参见表 3-38。任何非导电外壳插座配置都应按照垂直插座配置规定的值进行测试。

表 3-38 力和力矩要求

Receptacle configuration with respect to mounting surface	Force at 15 mm from receptacle shell mating edge (N)	Moment with respect to receptacle shell mating edge (Nm)
Right angle	20	0.30
Vertical[1]	8	0.12
Notes: 1. Any configuration of non-conductive shell receptacles shall be tested at the values specified for the vertical receptacle configuration.		

在施加拉力的整个过程中，应测量每个触点的连续性。还应测试每个非接地触点，以确认其在应力作用期间不会与外壳短路。然后应将 PCB 旋转 90 度，使电缆仍然水平插入，并再次向下施加表 3-38 中的拉力，并像以前一样测量连续性。重复此测试 180 度和 270 度旋转。通过测试的部件在四个方向中的任何一个方向上都不应出现任何不连续或与外壳短路超过 1 μs 的持续时间。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

One method for measuring the continuity through the contacts is to short all the wires at the end of the cable pigtail and apply a voltage through a pull-up to each of VBUS, USB D+, USB D−, SBU, CC, and TX/RX pins, with the GND pins connected to ground.

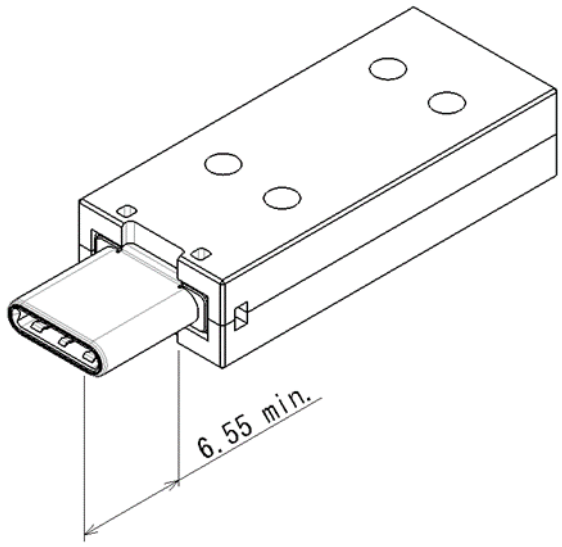
Alternate methods are allowed to verify continuity through all pins.

3.8.1.7 Wrenching Strength

USB Type-C plugs on cable assemblies and fixture plugs without overmold (including PCB-mount USB Type-C plugs) shall be tested using the mechanical wrenching test fixture defined in the Universal Serial Bus Type-C Connectors and Cable Assemblies Compliance Document. For plug without overmold, the supplier shall provide a plug test fixture that conforms to the specified plug overmold dimensions for the USB Type-C plug (see Figure 3-70). The fixture may be metal or other suitable material. Perpendicular moments are applied to the plug with a 5 mm ball tipped probe for a period of at least 10 seconds when inserted in the test fixture to achieve the defined moments in four directions of up or down (i.e., perpendicular to the long axis of the plug opening) and left or right (i.e., in the plane of the plug opening). Compliant connectors shall meet the following force thresholds:

- A moment of 0-0.75 Nm (e.g., 50 N at 15 mm from the edge of the receptacle) is applied to a plug inserted in the test fixture in each of the four directions. A single plug shall be used for this test. Some mechanical deformation may occur. The plug shall be mated with the continuity test fixture after the test forces have been applied to verify no damage has occurred that causes discontinuity or shorting. The continuity test fixture shall provide a planar surface on the mating side located 6.20 ± 0.20 mm from the receptacle Datum A, perpendicular to the direction of insertion. No moment forces are applied to the plug during this continuity test. Figure 3-71 illustrates an example continuity test fixture to perform the continuity test. The Dielectric Withstanding Voltage test shall be conducted after the continuity test to verify plug compliance.

Figure 3-70 Example Wrenching Strength Test Fixture for Plugs without Overmold



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

测量通过触点连续性的一种方法是短接电缆尾纤末端的所有电线，并通过上拉电阻向 VBUS、USB D+、USB D−、SBU、CC 和 TX/RX 每个引脚施加电压，并将 GND 引脚接地。

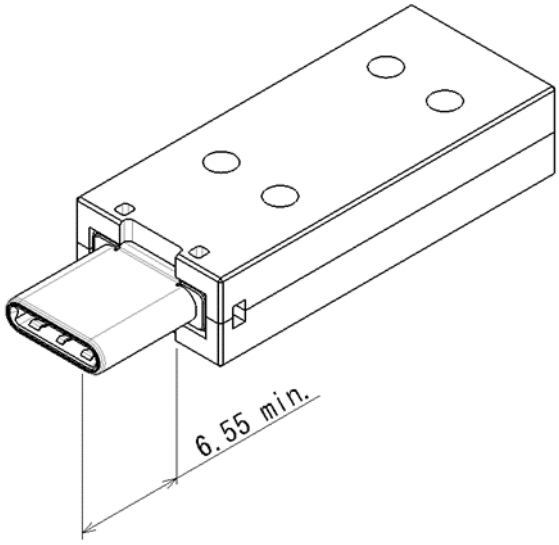
允许使用其他方法来验证所有引脚的连续性。

3.8.1.7 扭转强度

电缆组件上的 USB Type-C 插头和无包覆成型的固定装置插头（包括 PCB 安装的 USB Type-C 插头）应使用通用串行总线 Type-C 连接器和电缆组件合规性文件中定义的机械扳手测试夹具进行测试。对于无包覆成型的插头，供应商应提供符合 USB Type-C 插头规定的插头包覆成型尺寸的插头测试夹具（见图 3-70）。夹具可以是金属或其他合适的材料。将插头插入测试夹具后，用 5 毫米球头探针对插头施加垂直力矩至少 10 秒，以在上下（即垂直于插头开口的长轴）和左右（即在插头开口的平面）四个方向上实现定义的力矩。符合要求的连接器应满足以下力阈值：

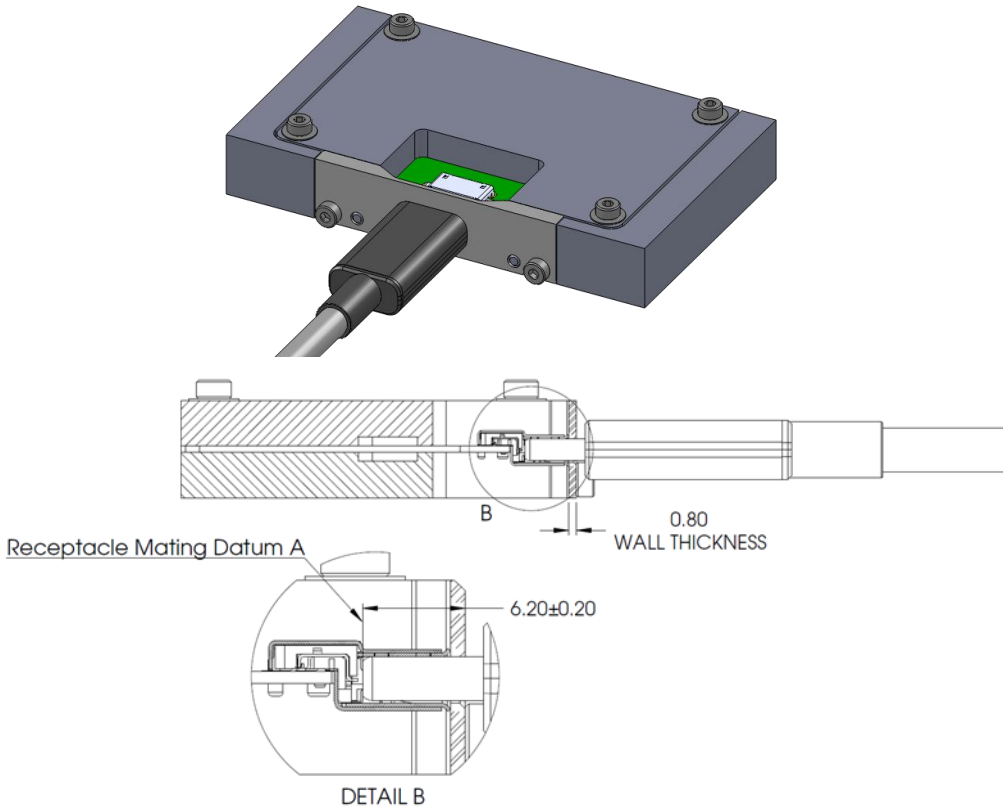
- 对插入测试夹具的插头在四个方向上分别施加 0-0.75 Nm（例如，在距插座边缘 15 毫米处施加 50 N）的力矩。该测试应使用单个插头。可能会发生一些机械变形。施加测试力后，应将插头与连续性测试夹具配合，以验证未发生导致不连续或短路的损坏。连续性测试夹具应在距离插座基准 A 6.20 ± 0.20 毫米的配合侧提供一个平面，垂直于插入方向。在此连续性测试期间，不会对插头施加任何力矩。图 3-71 显示了用于执行连续性测试的连续性测试夹具示例。连续性测试之后应进行介电耐压测试，以验证插头是否符合要求。

图 3-70 示例 插头扭力试验机 吨:次成型



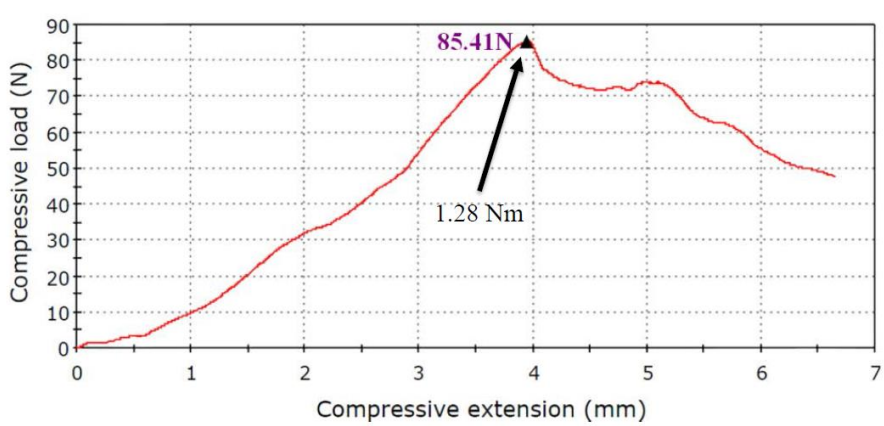
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-71 Reference Wrenching Strength Continuity Test Fixture



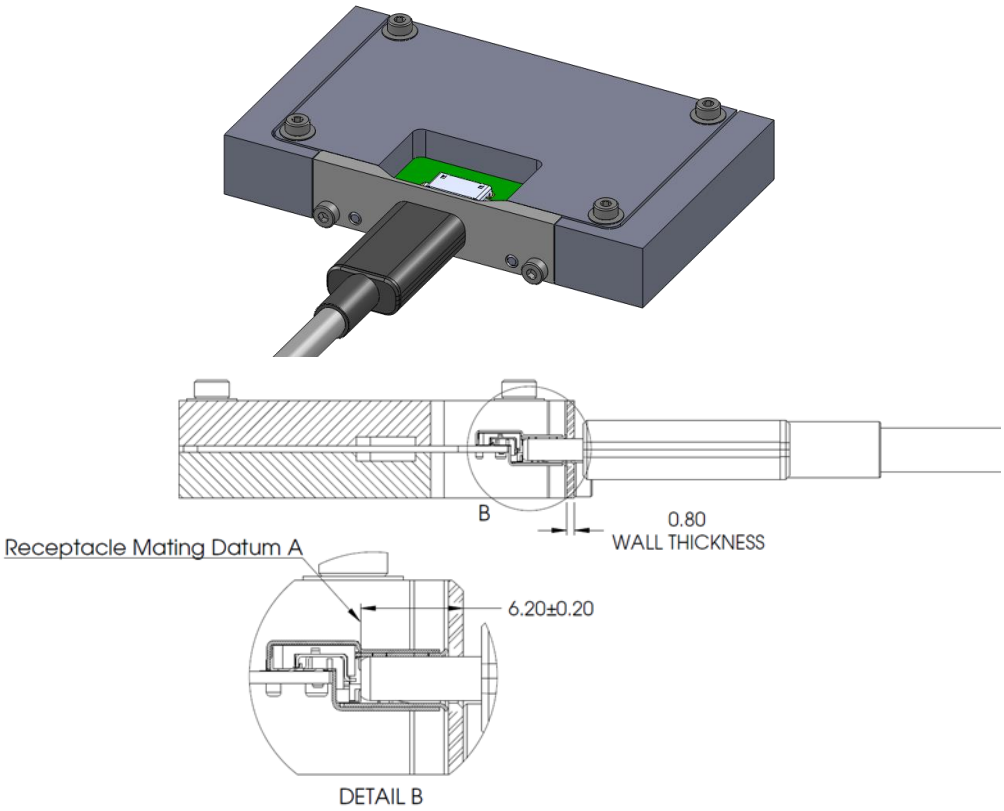
- The plug shall disengage from the test fixture or demonstrate mechanical failure (i.e., the force applied during the test procedure peaks and drops off) when a moment of 2.0 Nm is applied to the plug in the up and down directions and a moment 3.5 Nm is applied to the plug in the left and right directions. A new plug is required for each of the four test directions. An example of the mechanical failure point and an illustration of the wrenching test fixture are shown in Figure 3-72 and Figure 3-73, respectively.

Figure 3-72 Example of Wrenching Strength Test Mechanical Failure Point



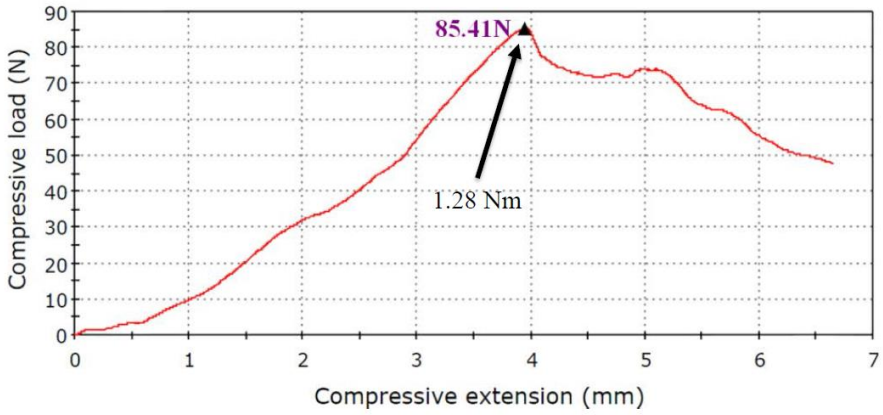
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-71 参考扳手强度连续性测试夹具



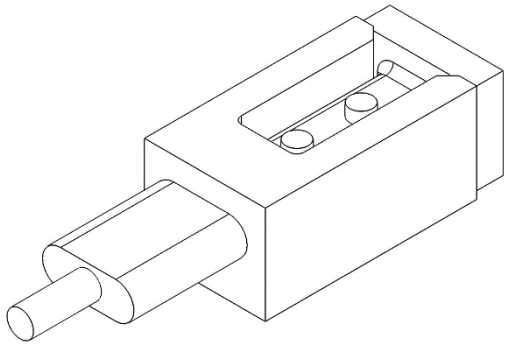
• 当在上下方向对插头施加 2.0 Nm 的力矩并在左右方向对插头施加 3.5 Nm 的力矩时，插头应脱离测试装置或出现机械故障（即，测试过程中施加的力达到峰值并下降）。四个测试方向中的每一个都需要一个新的插头。图 3-72 和图 3-73 分别显示了机械故障点的示例和扳手测试装置的图示。

图 3-72 扭力强度试验机械破坏点示例



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-73 Wrenching Strength Test with Cable in Fixture



3.8.1.8 Restriction of Hazardous Substances

It is recommended that components be RoHS compliant.

3.8.2 Environmental Requirements

The connector interface environmental tests shall follow EIA 364-1000.01, Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications.

Since the connector defined has more than 0.127 mm wipe length, Test Group 6 in EIA 364-1000.01 is not required. The temperature life test duration and the mixed flowing gas test duration values are derived from EIA 364-1000.01 based on the field temperature per the following.

Table 3-39 Environmental Test Conditions

Temperature Life test temperature and duration	105 °C for 120 hours
Temperature Life test temperature and duration for preconditioning	105 °C for 72 hours
Mixed flowing gas test duration	7 days

The pass/fail criterion for the low level contact resistance (LLCR) is as defined in Section 3.7.8.1. The durability ratings are defined in Section 3.8.1.3.

3.8.2.1 Reference Materials (Informative)

This specification does not specify materials for connectors and cables. Connector and cable manufacturers should select appropriate materials based on performance requirements. The information below is provided for reference only.

Note: Connector and cable manufacturers should comply with contact plating requirements per the following options:

Option I

Receptacle

Contact area: (Min) 0.05 µm Au + (Min) 0.75 µm Ni-Pd on top of (Min) 2.0 µm Ni

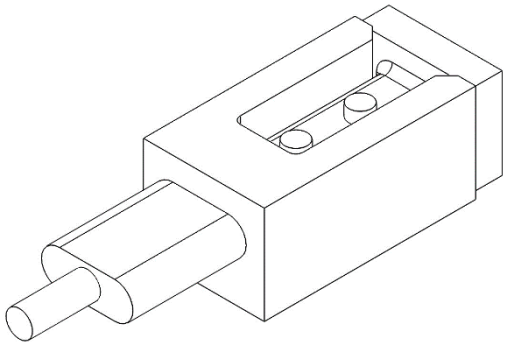
Plug

Contact area: (Min) 0.05 µm Au + (Min) 0.75 µm Ni-Pd on top of (Min) 2.0 µm Ni

Option II

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-73 夹具中带有电缆的扳手强度测试



3.8.1.8 有害物质限制

建议组件符合RoHS 标准。

3.8.2 环境要求

连接器接口环境测试应遵循 E IA 364-1000.01《评估商业办公应用中使用的电连接器和插座性能的环境测试方法》。

由于定义的连接器具有超过 0.127 毫米的擦拭长度，因此不需要 EIA 364-1000.01 中的测试组 6。温度寿命测试持续时间和混合流动气体测试持续时间值是根据以下现场温度从 EIA 364-1000.01 得出的。

表 3-39 环境测试条件

Temperature Life test temperature and duration	105 °C for 120 hours
Temperature Life test temperature and duration for preconditioning	105 °C for 72 hours
Mixed flowing gas test duration	7 days

低水平接触电阻 (LLCR) 的通过/失败标准如第 3.7.8.1 节中定义。耐久性等级定义在第 3.8.1.3 节中。

3.8.2.1 参考资料（资料性）

本规范不规定连接器和电缆的材料。连接器和电缆制造商应根据性能要求选择合适的材料。以下信息仅供参考。

注意：连接器和电缆制造商应按照以下选项遵守触点电镀要求：

选项一

容器

接触面积：（最小）0.05 µm Au +（最小）0.75 µm Ni-Pd 位于（最小）2.0 µm Ni 之上

插头

接触面积：（最小）0.05 µm Au +（最小）0.75 µm Ni-Pd 位于（最小）2.0 µm Ni 之上

方案二

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Receptacle

Contact area: (Min) 0.75 µm Au on top of (Min) 2.0 µm Ni

Plug

Contact area: (Min) 0.75 µm Au on top of (Min) 2.0 µm Ni

Other reference materials that connector and cable manufacturers select based on performance parameters listed in Table 3-40 are for reference only.

Table 3-40 Reference Materials

Component	Materials
Cable	Conductor: copper with tin or silver plating
	SDP Shield: AL foil or AL/mylar foil
	Coaxial shield: copper strand
	Braid: Tin plated copper or aluminum
	Jacket: PVC or halogen free substitute material
Cable Overmold	Thermoset or thermoplastic
Connector Shells	Stainless steel or phosphor bronze
Plug Side Latches	Stainless steel
Receptacle Mid-Plate	Stainless steel
Plug Internal EMC Spring	Stainless steel or high yield strength copper alloy
Receptacle EMC Pad	Stainless steel or phosphor bronze
Receptacle Shell	Stainless steel or phosphor bronze
Receptacle Tongue	Glass-filled nylon
Housing	Thermoplastics capable of withstanding lead-free soldering temperature

Note: Halogen-free materials should be considered for all plastics

3.9 Docking Applications (Informative)

In this specification, docking refers to plugging a device directly into a dock without using a cable assembly. The USB Type-C connector is defined to support such applications.

The connector is only part of a docking solution. A complete docking solution at the system level may also include retention or locking mechanisms, alignment mechanisms, docking plug mounting solutions, and protocols supported through the connector. This specification does not attempt to standardize system docking solutions, therefore there is no interoperability requirement for docking solutions.

The following list includes the requirements and guidelines when using the USB Type-C connector for docking:

1. The USB Type-C plug used for docking shall work with compliant USB Type-C receptacle. It shall comply with all dimensional, electrical and mechanical requirements.
2. If the plug on the dock does not include the side latches, then the dock should provide a retention or locking mechanism to secure the device to the plug. The retention latches also serve as one of the ground return paths for EMC. The docking

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

容器

接触面积：（最小）0.75 µm Au 位于（最小）2.0 µm Ni 之上

插头

接触面积：（最小）0.75 µm Au 位于（最小）2.0 µm Ni 之上

连接器及电缆生产厂家根据表3-40所列性能参数选择的其他参考资料仅供参考。

表 3-40 参考资料

Component	Materials
Cable	Conductor: copper with tin or silver plating
	SDP Shield: AL foil or AL/mylar foil
	Coaxial shield: copper strand
	Braid: Tin plated copper or aluminum
	Jacket: PVC or halogen free substitute material
Cable Overmold	Thermoset or thermoplastic
Connector Shells	Stainless steel or phosphor bronze
Plug Side Latches	Stainless steel
Receptacle Mid-Plate	Stainless steel
Plug Internal EMC Spring	Stainless steel or high yield strength copper alloy
Receptacle EMC Pad	Stainless steel or phosphor bronze
Receptacle Shell	Stainless steel or phosphor bronze
Receptacle Tongue	Glass-filled nylon
Housing	Thermoplastics capable of withstanding lead-free soldering temperature

注：所有塑料都应考虑采用无卤材料

3.9 对接应用（参考资料）

在本规范中，对接是指将设备直接插入底座，而无需使用电缆组件。USB Type-C 连接器被定义为支持此类应用。

连接器只是对接解决方案的一部分。系统级的完整对接解决方案还可能包括保持或锁定机制、对准机制、对接插头安装解决方案以及通过连接器支持的协议。本规范不试图标准化系统对接解决方案，因此对接解决方案没有互操作性要求。

以下列表包括使用 USB Type-C 连接器进行对接时的要求和指南：

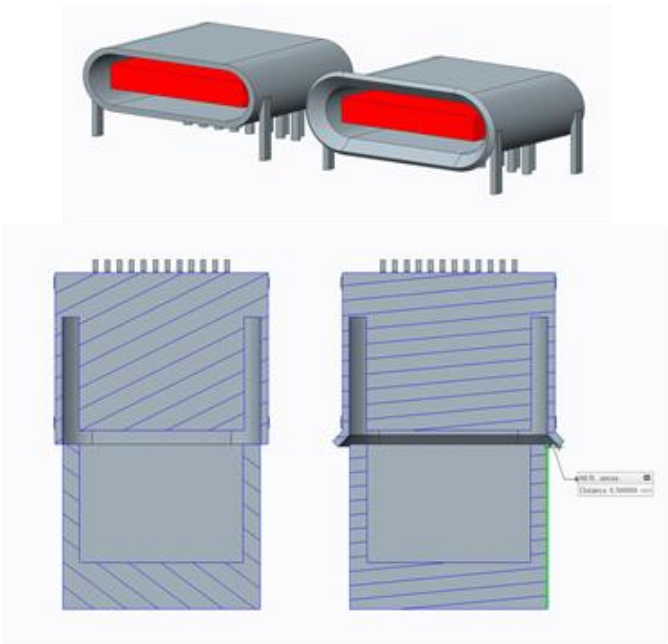
1. 用于对接的 USB Type-C 插头应与兼容的 USB Type-C 插座配合使用。它应符合所有尺寸、电气和机械要求。2. 如果底座上的插头不包含侧闩锁，则底座应提供固定或锁定机制，以将设备固定到插头上。固定闩锁还可用作 EMC 的接地回路之一。对接

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

design should ensure adequate EMC performance without the side latches if they are not present.

3. The internal EMC fingers are not required for the docking plug as long as the receptacle and plug shells have adequate electrical connection.
4. Alignment is critical for docking. Depending on system design, standard USB Type-C connectors alone may not provide adequate alignment for mating. System level alignment is highly recommended. Alignment solutions are implementation-specific.
5. Fine alignment is provided by the connector. The receptacle front face may have lead-in features for fine alignment. Figure 3-74 shows an example of a USB Type-C receptacle with a lead-in flange compared to a receptacle without the flange.

Figure 3-74 USB Type-C Cable Receptacle Flange Example



3.10 Implementation Notes and Design Guides

This section discusses a few implementation notes and design guides to help users design and use the USB Type-C connectors and cables.

3.10.1 EMC Management (Informative)

Connector and cable assembly designers, as well as system implementers should pay attention to receptacle and cable assembly shielding to ensure a low-impedance grounding path. The following are guidelines for EMC management:

- The quality of raw cables should be ensured. The intra-pair skew or the differential to common mode conversion of the TX/RX pairs has a significant impact on cable EMC and should be controlled within the limits of this specification.
- The cable external braid should be physically connected to the plug metal shell as close to 360° as possible to control EMC. Without appropriate shielding termination, even a perfect cable with zero intra-pair skew may not meet EMC requirements. Copper tape may be needed to shield off the braid termination area.
- The wire termination contributes to common-mode noise. The breakout distance for the wire termination should be kept as small as possible to optimize EMC and signal

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

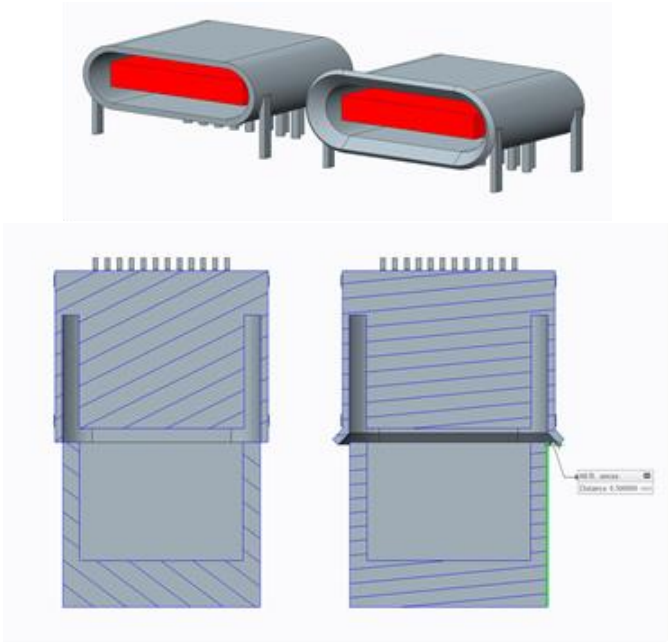
如果没有侧闩锁，设计也应能保证足够的 EMC 性能。

3. 只要插座和插头外壳具有足够的电气连接，对接插头就不需要内部 EMC 手指。

4. 对齐对于对接至关重要。根据系统设计，标准 USB Type-C 连接器本身可能无法提供足够的对齐以进行配接。强烈建议使用系统级对齐。对齐解决方案是特定于实施的。

5. 连接器提供精细对准。插座正面可能具有用于精细对准的引入功能。图 3-74 显示了带有引入凸缘的 USB Type-C 插座与不带凸缘的插座的比较示例。

图 3-74 USB Type-C 线缆插座法兰示例



3.10 实施说明和设计指南

本节讨论了一些实施说明和设计指南，以帮助用户设计和使用 USB Type-C 连接器和电缆。

3.10.1 EMC 管理（资料性）

连接器和电缆组件设计人员以及系统实施人员应注意插座和电缆组件屏蔽，以确保低阻抗接地路径。以下是 EMC 管理指南：

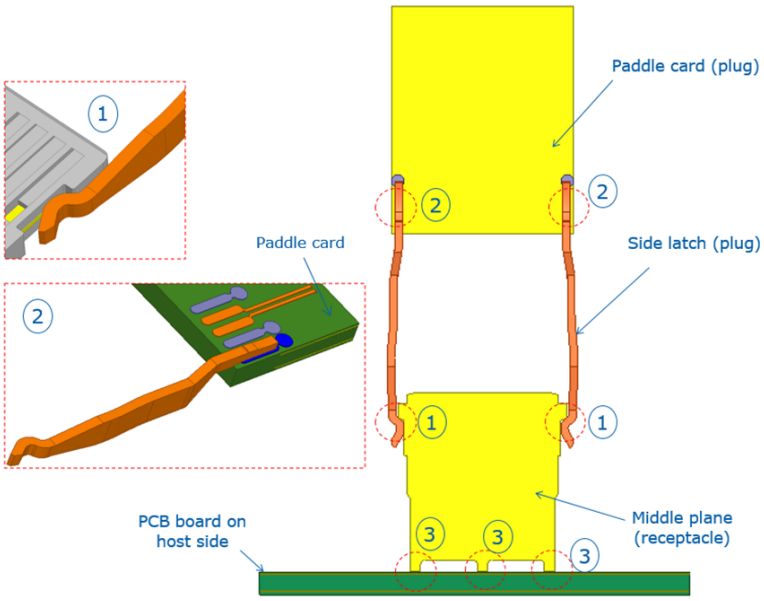
• 应确保原始电缆的质量。TX/RX 对的对内偏移或差分到共模转换对电缆 EMC 有重大影响，应控制在本规范的限制范围内。• 电缆外部编织层应尽可能 360° 物理连接到插头金属外壳以控制 EMC。如果没有适当的屏蔽端接，即使是对内偏移为零的完美电缆也可能无法满足 EMC 要求。可能需要铜带来屏蔽编织层端接区域。• 电线端接会产生共模噪声。电线端接的分支距离应尽可能小，以优化 EMC 和信号

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

integrity performance. If possible, symmetry should be maintained for the two lines within a differential pair.

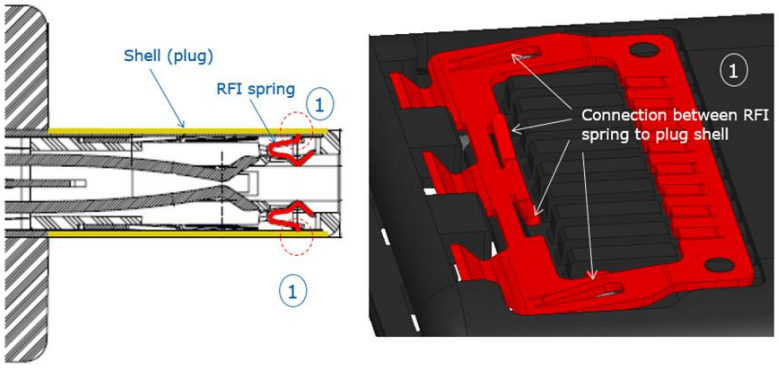
- Besides the mechanical function, the side latches on the plug and the mid-plate in the receptacle also play a role for EMC. This is illustrated in Figure 3-75:
    1. The side latch should have electrical connection to the receptacle mid-plate (a docking plug may not have side latches).
    2. The side latches should be terminated to the paddle card GND plane inside the plug.
    3. The mid-plate should be directly connected to system PCB GND plane with three or more solder leads/tails.

Figure 3-75 EMC Guidelines for Side Latch and Mid-plate



- The internal RFI finger inside the plug should have adequate connection points to the inner surface of the plug shell. Four or more connection points are recommended as illustrated in Figure 3-76.

Figure 3-76 EMC Finger Connections to Plug Shell



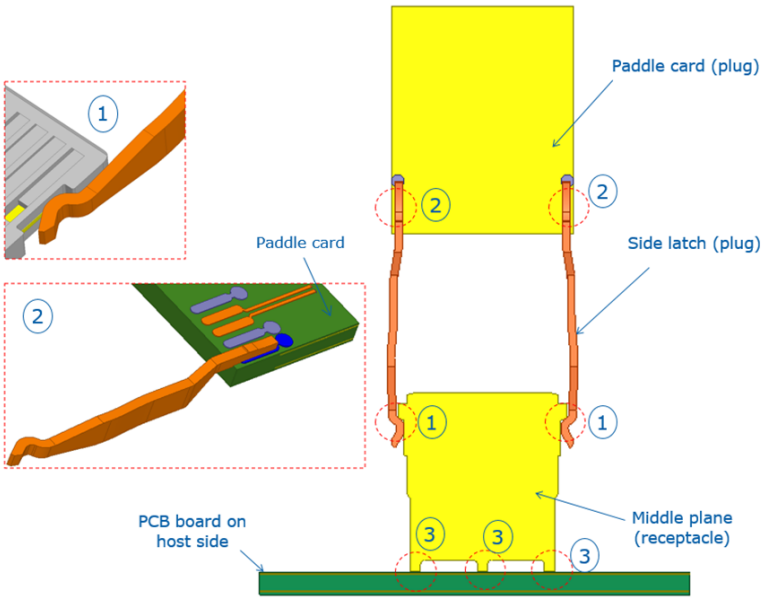
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

完整性性能。如果可能的话，差分对中的两条线应该保持对称。

•除了机械功能外，插头上的侧闩和插座中的中板也对 EMC 起着作用。如图 3-75 所示：

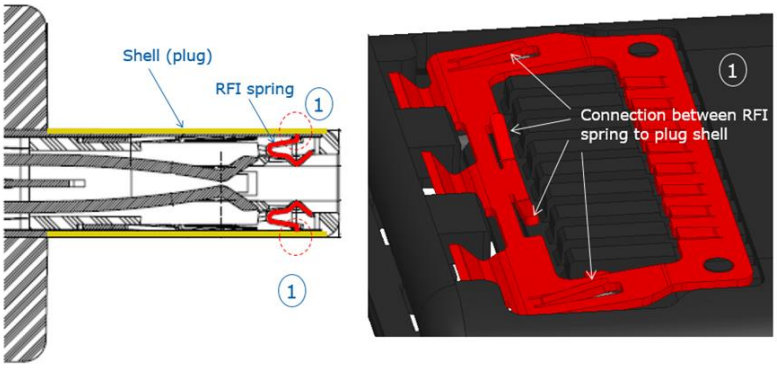
1. 侧闩应与插座中板有电气连接
（对接插头可能没有侧闩锁）。2. 侧闩锁应端接至插头内的插卡 GND 平面。3. 中板应通过三根或更多根焊线/焊尾直接连接至系统 PCB GND 平面。

图 3-75 侧锁和中板的 EMC 指南



• 插头内部的 RFI 指状物应具有足够的与插头外壳内表面的连接点。建议有四个或更多的连接点，如图 3-76 所示。

图 3-76 EMC 手指连接至插头外壳

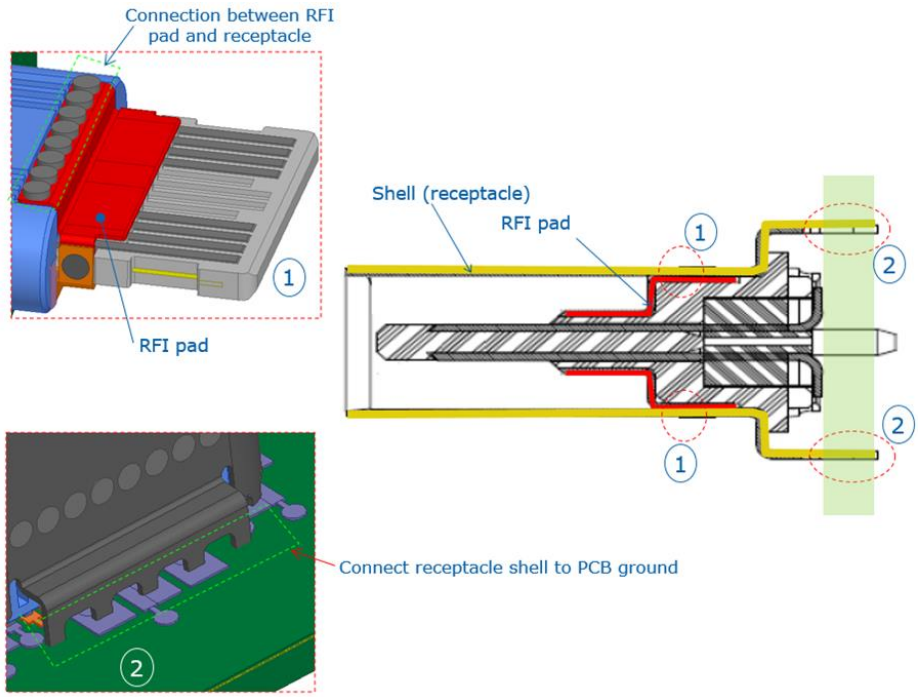


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- The EMC fingers inside the plug mates with the EMC pad in the receptacle. It is important for the EMC pad to have adequate connections to the receptacle shell. As illustrated in Figure 3-77, there are multiple laser welding points between the EMC pads and the receptacle shell, top and bottom.

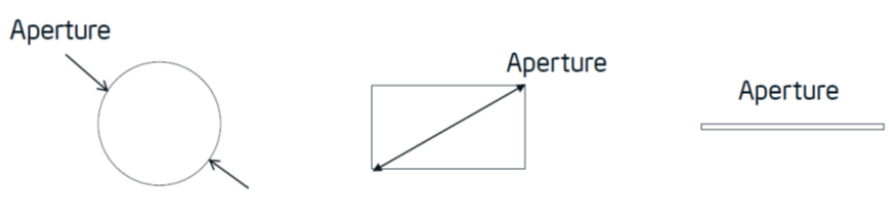
- The receptacle shell should have sufficient connection points to the system PCB GND plane with apertures as small as possible. Figure 3-77 illustrates an example with multiple solder tails to connect the receptacle shell to system PCB GND.

Figure 3-77 EMC Pad Connections to Receptacle Shell



- Apertures in the receptacle and plug shells should be minimized. If apertures are unavoidable, a maximum aperture size of 1.5 mm is recommended. See Figure 3-78 for aperture illustrations. Copper tape may be applied to seal the apertures inside the cable plug.

Figure 3-78 Examples of Connector Apertures



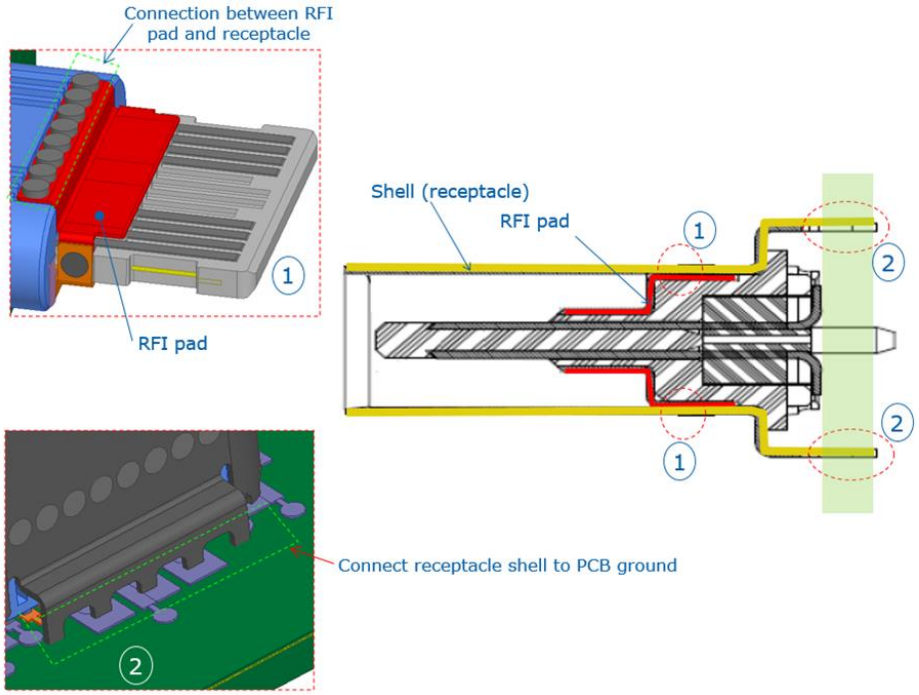
- The receptacle connectors should be connected to metal chassis or enclosures through grounding fingers, screws, or any other way to manage EMC.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• 插头内的 EMC 指状物与插座内的 EMC 焊盘相配。EMC 焊盘与插座外壳的充分连接非常重要。如图 3-77 所示，EMC 焊盘与插座外壳顶部和底部之间有多个激光焊接点。

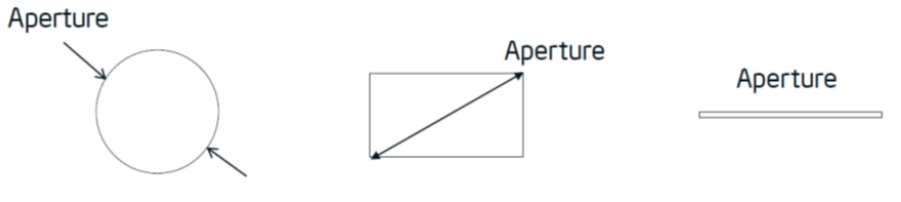
• 插座外壳应具有足够的连接点到系统 PCB GND 平面，且孔径应尽可能小。图 3-77 显示了使用多个焊尾将插座外壳连接到系统 PCB GND 的示例。

图 3-77 EMC 垫与插座外壳的连接



• 插座和插头外壳上的孔径应尽量减小。如果无法避免，建议最大孔径为 1.5 毫米。请参阅图 3-78 中的孔径图示。可使用铜带密封电缆插头内的孔径。

图 3-78 连接器孔径示例



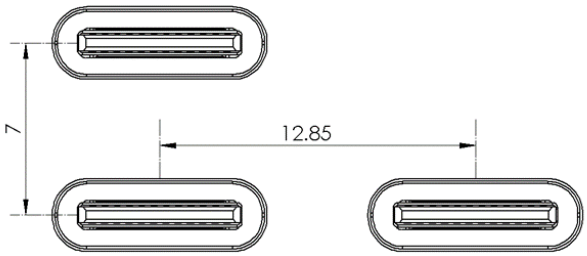
• 插座连接器应通过接地手指、螺钉或任何其他方式连接到金属底盘或外壳，以管理 EMC。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.10.2 Stacked and Side-by-Side Connector Physical Spacing (Informative)

Stacked and side-by-side USB connectors are commonly used in PC systems. Figure 3-79 illustrates the recommended spacing between connectors for stacked and side-by-side configurations.

Figure 3-79 Recommended Minimum Spacing between Connectors



3.10.3 Cable Mating Considerations (Informative)

The receptacle mounting location, exterior product surfaces, cable overmold, and plug mating length need to be considered to ensure the USB Type-C plug is allowed to fully engage the USB Type-C receptacle. Figure 3-80 illustrates the recommended minimum plug overmold clearance to allow the cable plug to fully seat in the product receptacle.

Figure 3-80 Recommended Minimum Plug Overmold Clearance

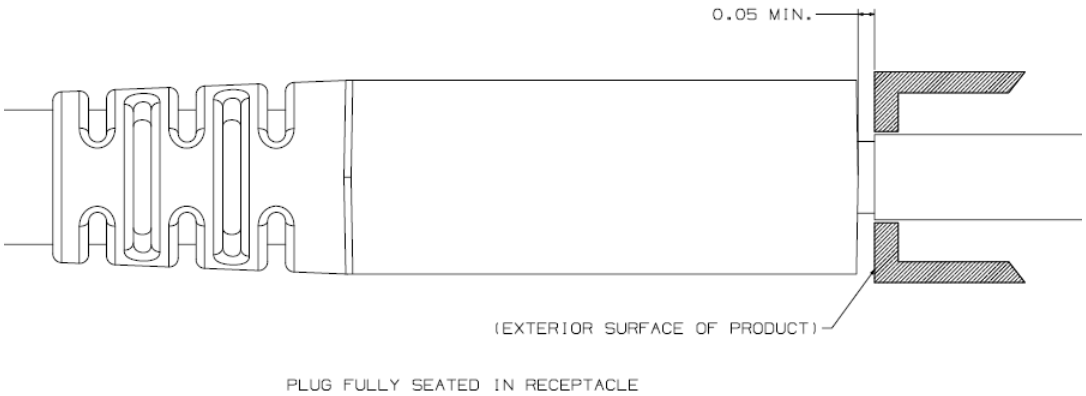


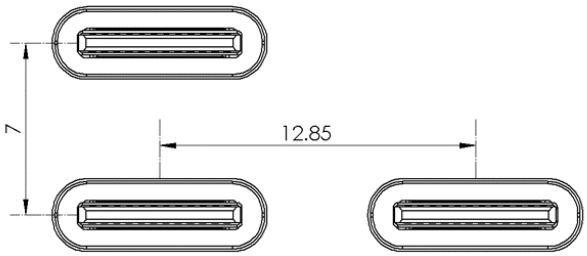
Figure 3-81 illustrates special considerations required when external walls are angled. For such applications, the USB Type-C receptacle shell may not provide as much mechanical alignment protection to the receptacle tongue as in the full shell design. Design options to allow the receptacle to pass mechanical test requirements include relief in the exterior wall surface to allow use of a full shell receptacle or use of a receptacle specifically designed for the application.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.10.2 堆叠和并排连接器物理间距（参考）

堆叠式和并排式 USB 连接器在 PC 系统中很常见。图 3-79 显示了堆叠式和并排式配置中连接器之间的建议间距。

图 3-79 连接器之间的建议最小间距



3.10.3 电缆配接注意事项（参考）

需要考虑插座安装位置、外部产品表面、电缆包覆成型和插头配接长度，以确保 USB Type-C 插头能够完全接合 USB Type-C 插座。图 3-80 显示了建议的最小插头包覆成型间隙，以允许电缆插头完全固定在产品插座中。

图 3-80 建议的最小插头包覆成型间隙

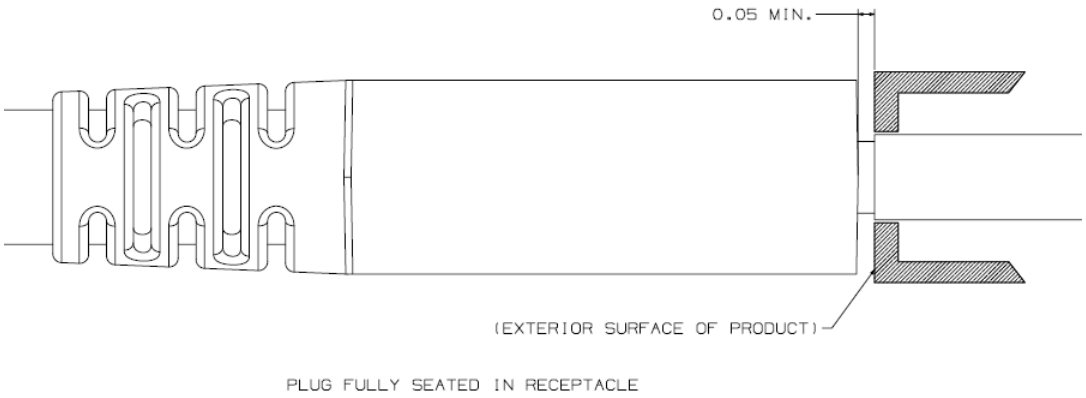
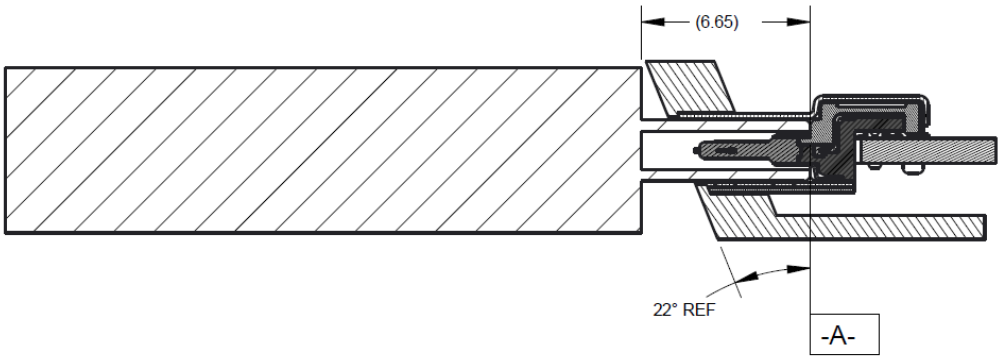


图 3-81 说明了当外壁倾斜时需要特别注意的事项。对于此类应用，USB Type-C 插座外壳可能无法像全壳设计那样为插座舌片提供足够的机械对准保护。为使插座能够通过机械测试要求，设计选项包括外壁表面的浮雕，以允许使用全壳插座或使用专为该应用设计的插座。

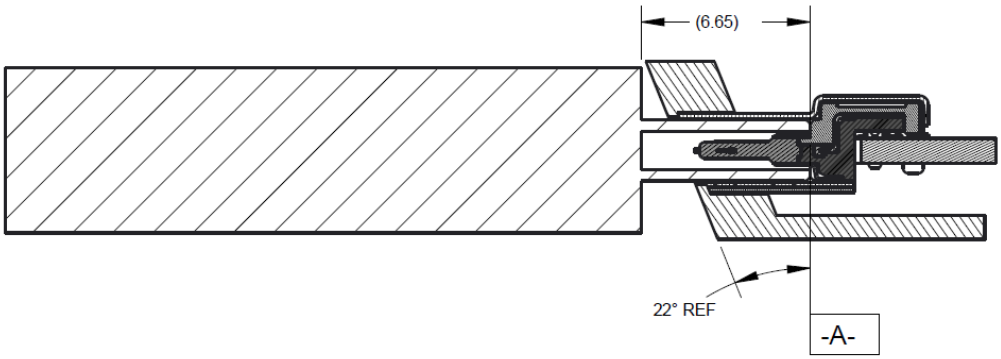
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 3-81 Cable Plug Overmold and an Angled Surface



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 3-81 电缆插头包覆成型件和倾斜表面



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4 Functional

This chapter covers the functional requirements for the signaling across the USB Type-C® cables and connectors. This includes functional signal definition, discovery and configuration processes, and power delivery.

4.1 Signal Summary

Table 4-1 summarizes the list of signals used on the USB Type-C connectors.

Table 4-1 USB Type-C List of Signals

Signal Group	Signal	Description
USB 3.2 / *USB4™*	**TXp1, TXn1** **RXp1, RXn1** **TXp2, TXn2** **RXp2, RXn2**	Both the *USB 3.2* SuperSpeed USB and *USB4* serial data interfaces defines 1 differential transmit pair and 1 differential receive pair per lane. On a USB Type-C receptacle, two sets of signal pins are defined to support dual-lane operation and enable plug flipping feature.
USB 2.0	**Dp1, Dn1** **Dp2, Dn2**	*USB 2.0* serial data interface defines a differential pair. On a USB Type-C receptacle, two set of *USB 2.0* signal pins are defined to enable plug flipping feature.
Configuration	**CC1, CC2** (receptacle) **CC** (plug)	CC channel in the plug used for connection detect, interface configuration and VCONN.
Auxiliary signals	**SBU1, SBU2**	Sideband Use. For *USB4*, these signals are used for SBTX and SBRX.
Power	**VBUS**	USB cable bus power
	VCONN (plug)	USB plug power
	GND	USB cable return current path

4.2 Signal Pin Descriptions

4.2.1 SuperSpeed USB Pins

TXp1, TXn1
TXp2, TXn2

These pins are required to implement the system's transmit path of either a *USB 3.2* SuperSpeed or *USB4* TX/RX interface. The transmitter differential pair in a port are routed to the receiver differential pair in the port at the opposite end of the path. Depending on the established connection, the *USB 3.2 Specification* or *USB4 Specification* defines all electrical characteristics, enumeration, protocol, and management features for this interface.

Two pairs of pins are defined to enable dual-lane operation – see Section 4.5.1.1 for further definition.

RXp1, RXn1
RXp2, RXn2

These pins are required to implement the system's receive path of a *USB 3.2* SuperSpeed or *USB4* TX/RX interface. The receiver differential pair in a port are routed to the transmitter differential pair in the port at the opposite end of the path. Depending on the established connection, the *USB 3.2 Specification* or *USB4 Specification* defines all electrical characteristics, enumeration, protocol, and management features for this interface.

Two pairs of pins are defined to enable dual-lane operation – see Section 4.5.1.1 for further definition.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4 功能

本章介绍 USB Type-C® 电缆和连接器信号传输的功能要求。其中包括功能信号定义、发现和配置过程以及电力传输。

4.1 信号摘要

表 4-1 总结　　列出 USB Type-C 连接器上使用的信号列表　　导演。

表 4-1 USB Type-C 信号列表

Signal Group	Signal	Description
USB 3.2 / *USB4™*	**TXp1, TXn1** **RXp1, RXn1** **TXp2, TXn2** **RXp2, RXn2**	Both the *USB 3.2* SuperSpeed USB and *USB4* serial data interfaces defines 1 differential transmit pair and 1 differential receive pair per lane. On a USB Type-C receptacle, two sets of signal pins are defined to support dual-lane operation and enable plug flipping feature.
USB 2.0	**Dp1, Dn1** **Dp2, Dn2**	*USB 2.0* serial data interface defines a differential pair. On a USB Type-C receptacle, two set of *USB 2.0* signal pins are defined to enable plug flipping feature.
Configuration	**CC1, CC2** (receptacle) **CC** (plug)	CC channel in the plug used for connection detect, interface configuration and VCONN.
Auxiliary signals	**SBU1, SBU2**	Sideband Use. For *USB4*, these signals are used for SBTX and SBRX.
Power	**VBUS**	USB cable bus power
	VCONN (plug)	USB plug power
	GND	USB cable return current path

4.2 信号引脚说明

4.2.1 超高速 USB 引脚

TXp1、TXn1
TXp2、TXn2

这些引脚是实现 *USB 3.2* SuperSpeed 或 *USB4* TX/RX 接口的系统传输路径所必需的。端口中的发射器差分对被路由到路径另一端端口中的接收器差分对。根据建立的连接，*USB 3.2 Specification* 或 *USB4 Specification* 定义此接口的所有电气特性、枚举、协议和管理功能。

定义了两对引脚以实现双通道操作 - 有关进一步的定义，请参阅第 4.5.1.1 节。

RXp1、RXn1
RXp2、RXn2

这些引脚是实现 *USB 3.2* SuperSpeed 或 *USB4* TX/RX 接口的系统接收路径所必需的。端口中的接收器差分对被路由到路径另一端端口中的发射器差分对。根据建立的连接，*USB 3.2 Specification* 或 *USB4 Specification* 定义所有电气

此接口的特性、枚举、协议和管理功能。

定义了两对引脚以实现双通道操作 - 有关进一步的定义，请参阅第 4.5.1.1 节。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.2.2 USB 2.0 Pins

Dp1, Dn1 (Dp2, Dn2)

These pins are required to implement *USB 2.0* functionality. *USB 2.0* in all three modes (LS, FS, and HS) is supported. The *USB 2.0 Specification* defines all electrical characteristics, enumeration, and bus protocol and bus management features for this interface.

Two pairs of pins are defined to enable the plug flipping feature – see Section 4.5.1.1 for further definition.

4.2.3 Auxiliary Signal Pins

SBU1, SBU2

These pins are assigned to sideband use. For *USB4*, these signals are used for SBTX and SBRX. Refer to Section 4.3 for the functional requirements.

4.2.4 Power and Ground Pins

VBUS

These pins are for USB cable bus power as defined by the USB specifications. VBUS is only present when a Source-to-Sink connection across the CC channel is present – see Section 4.5.1.2.1. Refer to Section 4.4.2 for the functional requirements for VBUS.

VCONN

VCONN is applied to the unused CC pin to supply power to the local plug. Refer to Section 4.4.3 for the functional requirements for VCONN.

GND

Return current path.

4.2.5 Configuration Pins

CC1, CC2, CC

These pins are used to detect connections and configure the interface across the USB Type-C cables and connectors. Refer to Section 4.5 for the functional definition. Once a connection is established, CC1 or CC2 will be reassigned for providing power over the VCONN pin of the plug – see Section 4.5.1.2.1.

4.3 Sideband Use (SBU)

The Sideband Use pins (SBU1 and SBU2) are limited to the uses as defined by this specification and additional functionality defined in the *USB4 Specification*. See Appendix E and Appendix A for use of the SBU pins in Alternate Modes and Audio Adapter Accessory Mode.

The SBU pins on a port shall either be open circuit or have a weak pull-down to ground no stronger than zSBUTermination.

These pins are pre-wired in the standard USB Full-Featured Type-C cable as individual single-ended wires (SBU_A and SBU_B). Note that SBU1 and SBU2 are cross-connected in the cable.

When operating in *USB4*, these pins are used as the *USB4* Sideband Channel with SBU1 mapping to SBTX and SBU2 mapping to SBRX. SBTX and SBRX functional requirements are as defined in the *USB4 Specification*. When a port determines that the locally-inserted plug is flipped (i.e. CC1 is open, CC2 is terminated), the *USB4 Specification* (reference Sideband Channel Lane Reversal) dictates that the port flip the SBTX and SBRX mappings to SBU1 and SBU2 in order to assure proper sideband transmit-to-receive end-to-end operation.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.2.2 USB 2.0 Pins

Dp1, Dn1 (Dp2, Dn2)	These pins are required to implement *USB 2.0* functionality. *USB 2.0* in all three modes (LS, FS, and HS) is supported. The *USB 2.0 Specification* defines all electrical characteristics, enumeration, and bus protocol and bus management features for this interface. Two pairs of pins are defined to enable the plug flipping feature – see Section 4.5.1.1 for further definition.

4.2.3 Auxiliary Signal Pins

SBU1, SBU2	These pins are assigned to sideband use. For *USB4*, these signals are used for SBTX and SBRX. Refer to Section 4.3 for the functional requirements.

4.2.4 Power and Ground Pins

VBUS	These pins are for USB cable bus power as defined by the USB specifications. VBUS is only present when a Source-to-Sink connection across the CC channel is present – see Section 4.5.1.2.1. Refer to Section 4.4.2 for the functional requirements for VBUS.
VCONN	VCONN is applied to the unused CC pin to supply power to the local plug. Refer to Section 4.4.3 for the functional requirements for VCONN.
GND	Return current path.

4.2.5 Configuration Pins

CC1, CC2, CC	These pins are used to detect connections and configure the interface across the USB Type-C cables and connectors. Refer to Section 4.5 for the functional definition. Once a connection is established, CC1 or CC2 will be reassigned for providing power over the VCONN pin of the plug – see Section 4.5.1.2.1.

4.3 边带使用（SBU）

边带使用引脚（SBU1 和 SBU2）仅限于本规范定义的用途以及 *USB4 Specification* 中定义的附加功能。有关备用模式和音频适配器附件模式下 SBU 引脚的使用，请参阅附录 E 和附录 A。

端口上的 SBU 引脚应为开路，或具有不强于 zSBUTermination 的弱下拉接地。

这些引脚在标准 USB 全功能 Type-C 电缆中预接线为单独的单端线（SBU_A 和 SBU_B）。请注意，SBU1 和 SBU2 在电缆中交叉连接。

在 *USB4* 中操作时，这些引脚用作 *USB4* 边带通道，其中 SBU1 映射到 SBTX，SBU2 映射到 SBRX。SBTX 和 SBRX 功能要求如 *USB4 Specification* 中定义。当端口确定本地插入的插头被翻转（即 CC1 处于打开状态，CC2 终止）时，*USB4 Specification*（参考边带通道通道反转）指示端口将 SBTX 和 SBRX 映射翻转为 SBU1 和 SBU2，以确保正确的边带发送到接收端到端操作。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.4 Power and Ground

4.4.1 IR Drop

The maximum allowable cable IR drop for ground (including ground on a captive cable) shall be 250 mV and for VBUS shall be 500 mV through the cable to the cable's maximum rated VBUS current capacity. When VCONN is being sourced, the IR drop for the ground shall still be met considering any additional VCONN return current.

Figure 4-1 illustrates what parameters contribute to the IR drop and where it shall be measured. The IR drop includes the contact resistance of the mated plug and receptacles at each end.

Figure 4-1 Cable IR Drop

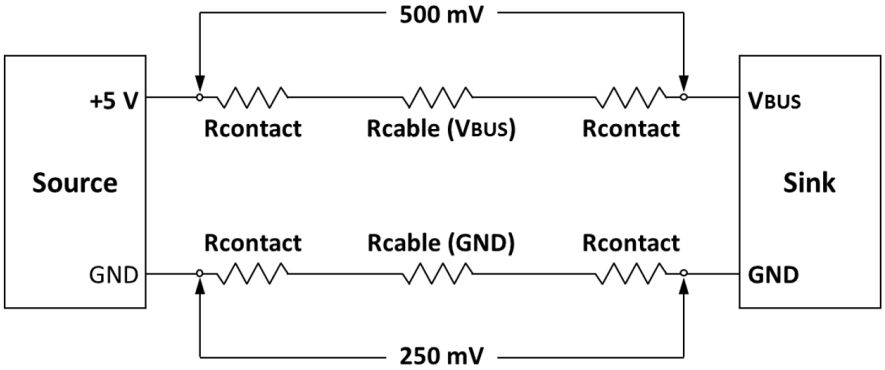
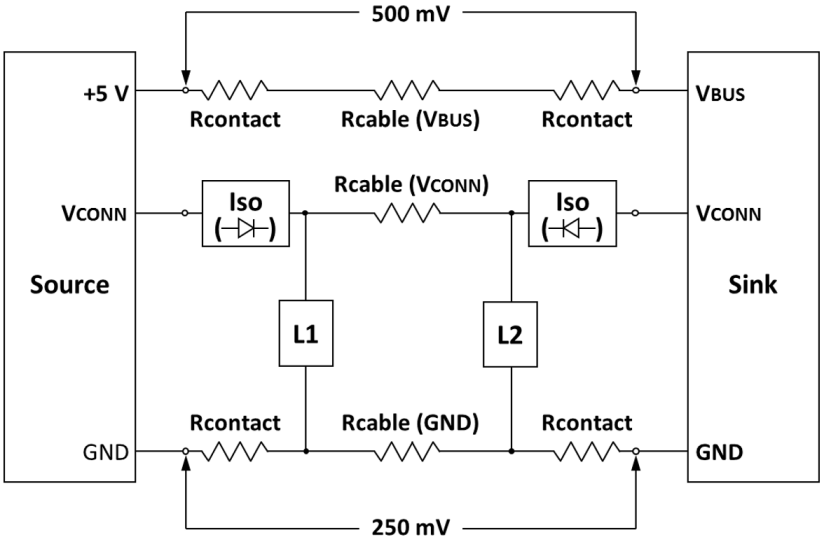


Figure 4-2 illustrates what parameters contribute to the IR drop for a powered cable and where it shall be measured. Note that the powered cable includes isolation elements (Iso) and loads (L1 and L2) for the functions in the powered cable such as *USB PD* controllers. The IR drop shall remain below 250 mV in all cases.

Figure 4-2 Cable IR Drop for powered cables



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.4 电源和接地

4.4.1 电压降

电缆接地（包括固定电缆上的接地）的最大允许 IR 压降应为 250 mV，VBUS 的最大允许 IR 压降应为 500 mV（通过电缆达到电缆的最大额定 VBUS 电流容量）。当 VCONN 为源极时，考虑到任何额外的 VCONN 返回电流，接地的 IR 压降仍应满足要求。

图 4-1 说明了哪些参数会影响 IR 压降以及应在何处进行测量。IR 压降包括两端的插头和插座的接触电阻。

图 4-1 电缆压降

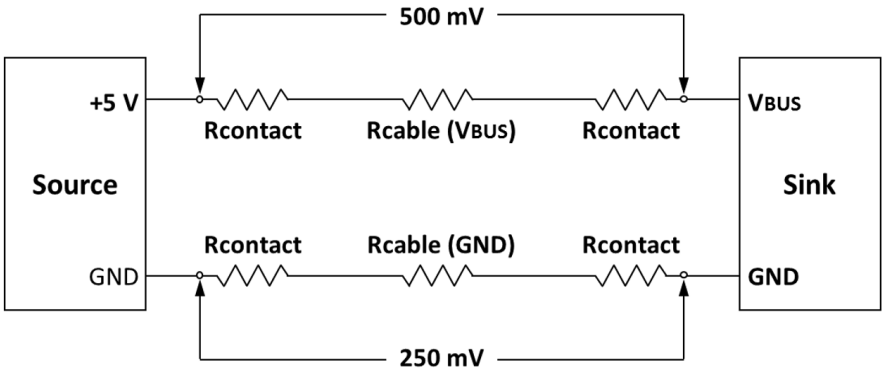
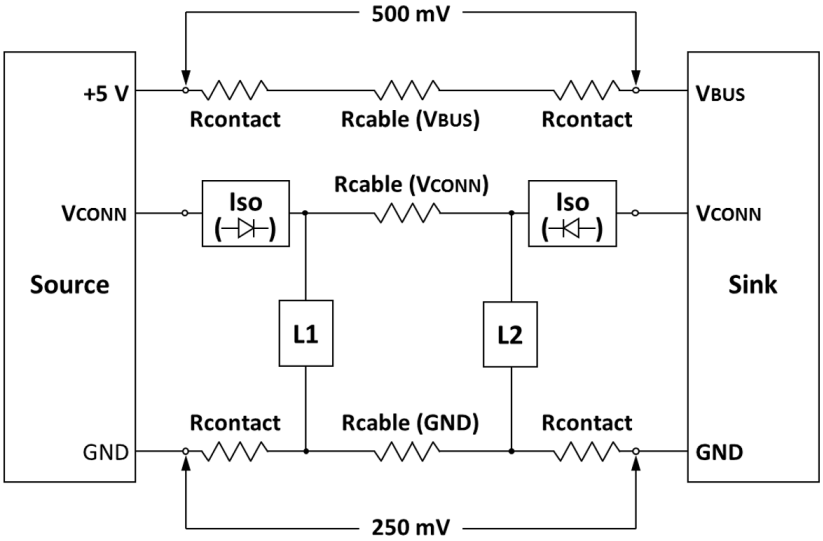


图 4-2 说明了哪些参数会影响供电电缆的 IR 压降以及应在何处进行测量。请注意，供电电缆包括隔离元件 (Iso) 和负载 (L1 和 L2)，用于供电电缆中的功能，例如 *USB PD* 控制器。在所有情况下，IR 压降都应保持在 250 mV 以下。

图 4-2 供电电缆的 IR 压降



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.4.2 VBUS

The allowable default range for VBUS as measured at the Source receptacle shall be as defined by the *USB 2.0 Specification* and *USB 3.2 Specification*. For *USB4*, the *USB 3.2 Specification* is used for this requirement. NOTE that due to higher currents allowed, legacy devices may experience a higher voltage (up to 5.5V maximum) at light loads.

The Source's USB Type-C receptacle VBUS pin shall remain unpowered and shall limit the capacitance between VBUS and GND as specified in Table 4-2 until a Sink is attached. The VBUS pin shall return to the unpowered state when the Sink is detached. See Table 4-29 for VBUS timing values. Legacy hosts/chargers that by default source VBUS when connected using any legacy USB connector (Standard-A, Micro-B, etc.) to USB Type-C cable or adapter are exempted from these two requirements.

A DRP or Source (or device with Accessory Support) implementing an Rp pull-up as its method of connection detection shall provide an impedance between VBUS and GND on its receptacle pins as specified in Table 4-2 when not sourcing power on VBUS (i.e., when in states Unattached.SRC or Unattached.Accessory).

Table 4-2 VBUS Source Characteristics

	Minimum	Maximum	Notes
VBUS Leakage Impedance	72.4 kΩ		Leakage between VBUS pins and GND pins on receptacle when VBUS is not being sourced.
VBUS Capacitance		3000 µF	Capacitance for source-only ports between VBUS and GND pins on receptacle when VBUS is not being sourced.
		10 µF	Capacitance for DRP ports between VBUS and GND pins on receptacle when VBUS is not being sourced.

Table 4-3 specifies VBUS Sink characteristics with regard to disconnect behavior based on monitoring VBUS. Sinks may monitor the CC pin for the removal of Rp by the Source as an additional indication of disconnect.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.4.2 总线电压

在源插座处测量的 VBUS 的允许默认范围应由 *USB 2.0 Specification* 和 *USB 3.2 Specification* 定义。对于 *USB4*, ~~*USB 3.2 Specification* 用于满足此要求。请注意，由于允许的电流较大，旧设备在轻负载下可~~能会经历更高的电压（最高可达 5.5V）。

源端的 USB Type-C 插座 VBUS 引脚应保持无电状态，并应限制 VBUS 和 GND 之间的电容（如表 4-2 所示），直到连接接收器。断开接收器后，VBUS 引脚应返回无电状态。有关 VBUS 时序值，请参阅表 4-29。使用任何传统 USB 连接器（标准 A、Micro-B 等）连接到 USB Type-C 电缆或适配器时，默认为源端提供 VBUS 的传统主机/充电器不受这两项要求的约束。

当未通过 VBUS 供电时（即处于 Unattached.SRC 或 Unattached.Accessory 状态时），实施 Rp 上拉作为连接检测方法的 DRP 或源（或具有附件支持的设备）应在其插座引脚上的 V BUS 和 GN D 之间提供如表 4-2 所示的阻抗。

表 4-2 VBUS 源特性

	Minimum	Maximum	Notes
VBUS Leakage Impedance	72.4 kΩ		Leakage between VBUS pins and GND pins on receptacle when VBUS is not being sourced.
VBUS Capacitance		3000 µF	Capacitance for source-only ports between VBUS and GND pins on receptacle when VBUS is not being sourced.
		10 µF	Capacitance for DRP ports between VBUS and GND pins on receptacle when VBUS is not being sourced.

表 4-3 指定了基于监控 VBUS 的 VBUS 接收器特性，包括断开连接行为。接收器可以监控 CC 引脚，以查看源是否移除 Rp，作为断开连接的额外指示。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 4-3 VBUS Sink Characteristics

	Minimum	Maximum	Notes
tSinkDisconnect		40 ms	Time limit for transition from Attached.SNK to Unattached.SNK
vSinkDisconnect[1]	0.8V	3.67V	Threshold used for transition from Attached.SNK to Unattached.SNK when VBUS is 5 V. This also applies for *USB PD* contracts at 5 V. For *USB PD* contracts at 5 V, the Sink shall take IR drop and margin into account when selecting this threshold.
		PPS_APDO_ Min_Voltage * 0.95	Threshold used for transition from Attached.SNK to Unattached.SNK. This applies for *USB PD* PPS contracts for RDO Output Voltage less than or equal to 5 V. This also applies for *USB PD* PPS contracts operating in the Current Limit mode. The Sink shall take IR drop and margin into account when selecting this threshold.
vSinkPD_min[1]		vNew – 750 mV + vValid	Minimum valid VBUS voltage seen by sink when negotiated through *USB PD*. vNew = vSrcNew (min) or vPpsNew (min) as defined in *USB PD*. 750 mV= 500 mV + 250 mV (maximum IR drop) vValid = vSrcValid (min) or vPpsValid (min) as defined in *USB PD*.
vSinkDisconnectPD[1]	90% of vSinkPD_min	vSinkPD_min	VBUS disconnect threshold when VBUS voltage was negotiated through *USB PD* to a value above 5 V. This applies for *USB PD* PPS contracts for RDO Output Voltage above 5 V. This also applies for *USB PD* PPS contracts operating in the Constant Voltage mode.
VBUS Capacitance		10 µF	Capacitance between VBUS and GND pins on receptacle when not in Attached.SNK.

Note 1: See Section 4.5.2.2.5.2 with regard to applicability of this requirement.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 4-3 VBUS 接收特性

	Minimum	Maximum	Notes
tSinkDisconnect		40 ms	Time limit for transition from Attached.SNK to Unattached.SNK
vSinkDisconnect[1]	0.8V	3.67V	Threshold used for transition from Attached.SNK to Unattached.SNK when VBUS is 5 V. This also applies for *USB PD* contracts at 5 V. For *USB PD* contracts at 5 V, the Sink shall take IR drop and margin into account when selecting this threshold.
		PPS_APDO_ Min_Voltage * 0.95	Threshold used for transition from Attached.SNK to Unattached.SNK. This applies for *USB PD* PPS contracts for RDO Output Voltage less than or equal to 5 V. This also applies for *USB PD* PPS contracts operating in the Current Limit mode. The Sink shall take IR drop and margin into account when selecting this threshold.
vSinkPD_min[1]		vNew – 750 mV + vValid	Minimum valid VBUS voltage seen by sink when negotiated through *USB PD*. vNew = vSrcNew (min) or vPpsNew (min) as defined in *USB PD*. 750 mV= 500 mV + 250 mV (maximum IR drop) vValid = vSrcValid (min) or vPpsValid (min) as defined in *USB PD*.
vSinkDisconnectPD[1]	90% of vSinkPD_min	vSinkPD_min	VBUS disconnect threshold when VBUS voltage was negotiated through *USB PD* to a value above 5 V. This applies for *USB PD* PPS contracts for RDO Output Voltage above 5 V. This also applies for *USB PD* PPS contracts operating in the Constant Voltage mode.
VBUS Capacitance		10 µF	Capacitance between VBUS and GND pins on receptacle when not in Attached.SNK.

注 1：参见第 1 节关于本要求的适用性，请参见 4.5.2.2.5.2 導致。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.4.3 VCONN

VCONN is provided by the Source to power cables with electronics in the plug. VCONN is provided over the CC pin that is determined not to be connected to the CC wire of the cable.

Initially, VCONN shall be sourced on all Source USB Type-C receptacles that utilize the TX and RX pins during specific connection states as described in Section 4.5.2.2. Subsequently, if VCONN is not explicitly required by the cable or device as indicated in its eMarker, VCONN may be removed as described in Table 4-4. VCONN may also be sourced by USB Type-C receptacles that do not utilize the TX and RX pins as described in Section 4.5.2.2. *USB PD* VCONN_Swap command also provides the Source a means to request that the attached Sink source VCONN.

Table 4-4 USB Type-C Source Port's VCONN Requirements Summary

D+/D–	TX/RX, VPD	> 3 A	VCONN Requirements
No	No	No	Not required to source VCONN
Yes	No	No	Not required to source VCONN
Yes	Yes	No	Required to source 1 W for x1 implementations and 1.5 W for x2 implementations. If not otherwise required, VCONN power may be removed after the source has read the cable's eMarker and has determined that it is not an active cable nor a VPD.
No	No	Yes	Required to source 100 mW. If not otherwise required, VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity.
Yes	No	Yes	Required to source 100 mW. If not otherwise required, VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity.
Yes	Yes	Yes	Required to source 1 W for x1 implementations and 1.5 W for x2 implementations. If not otherwise required, VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity and that it is not an active cable nor a VPD.

Table 4-5 provides the voltage and power requirements that shall be met for VCONN. See Section 4.9 for more details about Electronically Marked Cables. See Appendix E regarding optional support for an increased VCONN power range in Alternate Modes.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.4.3 VCONN

VCONN 由电源提供，用于为插头中带有电子设备的电缆供电。VCONN 通过 CC 引脚提供，该引脚确定不连接到电缆的 CC 线。

最初，VCONN 应在特定连接状态下使用 TX 和 RX 引脚的所有源 USB Type-C 插座上提供，如第 4.5.2.2 节所述。随后，如果电缆或设备未明确要求 VCONN（如其 eMarker 所示），则可以移除 VCONN，如表 4-4 所述。VCONN 也可以由不使用 TX 和 RX 引脚的 USB Type-C 插座提供，如第 4.5.2.2 节所述。*USB PD* VCONN_Swap 命令还为源提供了一种请求连接的接收器提供 VCONN 的方法。

表 4-4 USB Type-C 源端口 VCONN 要求汇总

D+/D−	TX/RX, VPD	> 3 A	VCONN Requirements
No	No	No	Not required to source VCONN
Yes	No	No	Not required to source VCONN
Yes	Yes	No	Required to source 1 W for x1 implementations and 1.5 W for x2 implementations. If not otherwise required, VCONN power may be removed after the source has read the cable's eMarker and has determined that it is not an active cable nor a VPD.
No	No	Yes	Required to source 100 mW. If not otherwise required, VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity.
Yes	No	Yes	Required to source 100 mW. If not otherwise required, VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity.
Yes	Yes	Yes	Required to source 1 W for x1 implementations and 1.5 W for x2 implementations. If not otherwise required, VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity and that it is not an active cable nor a VPD.

表 4-5 提供了 V CONN 应满足的电压和功率要求。有关电子标记电缆的更多详细信息，请参阅第 4.9 节。有关在替代模式下对增加 VCONN 功率范围的可选支持，请参阅附录 E。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 4-5 VCONN Source Characteristics

	Minimum	Maximum	Notes
vVCONNValid	3.0 V	5.5 V	The voltage range over which VCONN is considered valid.
Power for Sources with TX/RX Signals	x1 1 W		Source may latch-off VCONN if excessive power is drawn beyond the specified inrush and mode wattage. Source may disable VCONN per Table 4-4. Alternate modes may require higher power.
	x2 1.5 W		
Power for Sources with VPD support	1 W		Source may latch-off VCONN if excessive power is drawn beyond the specified inrush and mode wattage.
Power for Sources in USB Suspend or without TX/RX Signals	100 mW		Minimum power Source must provide in USB Suspend or without TX/RX signals. Source may disable VCONN per Table 4-4.
Rdch	30 Ω	6120 Ω	Discharge resistance applied in UnattachedWait.SRC between the CC pin being discharged and GND.

To aid in reducing the power associated with supplying VCONN, a Source is allowed to either not source VCONN or turn off VCONN under any of the following conditions:

- Ra is not detected on the CC pin after tCCDebounce when the other CC pin is in the SRC.Rd state, or
- if there is no GoodCRC response to *USB PD* Discover Identity messages sent to SOP'.

If the power source used to supply VCONN power is a shared power source for other USB VCONN and VBUS outputs, it must be bypassed with capacitance identical to the VBUS capacitance requirements of *USB 3.2* Section 11.4.4 – Dynamic Attach and Detach. Any VCONN power source bypass capacitance must be isolated from the CC pins when VCONN is not being provided.

Table 4-6 provides the requirements that shall be met for cables that consume VCONN power.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 4-5 VCONN 源特性

	Minimum	Maximum	Notes
vVCONNValid	3.0 V	5.5 V	The voltage range over which VCONN is considered valid.
Power for Sources with TX/RX Signals	x1 1 W		Source may latch-off VCONN if excessive power is drawn beyond the specified inrush and mode wattage. Source may disable VCONN per Table 4-4. Alternate modes may require higher power.
	x2 1.5 W		
Power for Sources with VPD support	1 W		Source may latch-off VCONN if excessive power is drawn beyond the specified inrush and mode wattage.
Power for Sources in USB Suspend or without TX/RX Signals	100 mW		Minimum power Source must provide in USB Suspend or without TX/RX signals. Source may disable VCONN per Table 4-4.
Rdch	30 Ω	6120 Ω	Discharge resistance applied in UnattachedWait.SRC between the CC pin being discharged and GND.

为了帮助降低与供应 VCONN 相关的功耗，在以下任一情况下，源都可以不供应 VCONN 或关闭 VCONN：

当另一个 CC 引脚处于 SRC.Rd 状态时，tCCDebounce 之后未在 CC 引脚上检测到 • Ra，或者

如果对发送到 SOP ’ 的 *USB PD* 发现身份消息没有 GoodCRC 响应，则 •。

如果用于为 VCONN 供电的电源是其他 USB VCONN 和 VBUS 输出的共享电源，则必须使用与 *USB 3.2* 节 11.4.4 – 动态连接和分离的 VBUS 电容要求相同的电容对其进行旁路。当未提供 VCONN 时，任何 VCONN 电源旁路电容都必须与 CC 引脚隔离。

表 4-6 提供了消耗 V CONN 电源的电缆应满足的要求。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 4-6 Cable VCONN Sink Characteristics

	Minimum	Maximum	Notes
Voltage	3.0	5.5V	Voltage range (vVCONNValid) over which this table applies
Inrush Capacitance		10 µF	A cable shall not present more than the equivalent inrush capacitance to the VCONN source. The active cable is responsible for discharging its capacitance.
Power for Electronically Marked Passive Cables		20mW	See Section 4.9. Measured with no USB PD traffic at least 500ms after VCONN applied Note: 75mW max allowed for the first 500ms after VCONN applied.
USB 3.2 Power for Active Cables in U-states		See Table 6-19	U0, U1, U2, U3, Rx.Detect, and eSS.Disabled.
tVCONNDischarge		230ms	Time from cable disconnect to vVCONNDischarge met.
vVCONNDischarge		800mV	VCONN voltage after tVCONNDischarge
vRaReconnect	800mV		Voltage at which the cable shall reapply Ra on the falling edge of VCONN.

The cable shall remove or weaken Ra when VCONN is in the valid voltage range (vVCONNValid). The cable shall reapply Ra when VCONN falls below vRaReconnect as defined in Table 4-6. The cable shall discharge VCONN to below vVCONNDischarge on a cable disconnect. The cable shall take into account the VCONN capacitance present in the cable when discharging VCONN.

Implementation Note: Increasing Ra to 20KΩ will meet both the power dissipation for electronically marked passive cables and discharge 10µF to less than vVCONNDischarge in tVCONNDischarge.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 4-6 电缆 VCONN 接收器特性

	Minimum	Maximum	Notes
Voltage	3.0	5.5V	Voltage range (vVCONNValid) over which this table applies
Inrush Capacitance		10 µF	A cable shall not present more than the equivalent inrush capacitance to the VCONN source. The active cable is responsible for discharging its capacitance.
Power for Electronically Marked Passive Cables		20mW	See Section 4.9. Measured with no USB PD traffic at least 500ms after VCONN applied Note: 75mW max allowed for the first 500ms after VCONN applied.
USB 3.2 Power for Active Cables in U-states		See Table 6-19	U0, U1, U2, U3, Rx.Detect, and eSS.Disabled.
tVCONNDischarge		230ms	Time from cable disconnect to vVCONNDischarge met.
vVCONNDischarge		800mV	VCONN voltage after tVCONNDischarge
vRaReconnect	800mV		Voltage at which the cable shall reapply Ra on the falling edge of VCONN.

当 VCONN 处于有效电压范围 (vVCONNValid) 内时，电缆应移除或减弱 Ra。当 VCONN 低于表 4-6 中定义的 vRaReconnect 时，电缆应重新施加 Ra。电缆断开时，电缆应将 VCONN 放电至低于 vVCONNDischarge。电缆在放电 VCONN 时应考虑电缆中存在的 VCONN 电容。

实施注意事项：将 Ra 增加到 20KΩ 将满足电子标记无源电缆的功率耗散和将 10µF 放电至 tVCONNDischarge 中的 vVCONNDischarge 以下。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 4-7 VCONN-Powered Accessory (VPA) Sink Characteristics

	Minimum	Maximum	Notes
Voltage	3.0 V	5.5 V	Voltage range (vVCONNValid) over which this table applies
Inrush Capacitance		10 µF	An accessory shall not present more than the equivalent inrush capacitance to the VCONN source. The accessory is responsible for discharging its capacitance when detached from a port.
Power before Alternate Mode Entry		35 mW	Maximum power in USB suspend Note: Power shall be reduced 5 seconds after VCONN is applied if no Alternate Mode Entry has occurred. A VCONN power cycle may be required to re-enable USB-PD communication.
tVCONNDischarge		230 ms	Time from VPA disconnect to vVCONNDischarge met.
vVCONNDischarge		800 mV	VCONN voltage after tVCONNDischarge
vRaReconnect	800 mV		Voltage at which the VPA shall reapply Ra on the falling edge of VCONN.
vVCONNDisconnect	800 mV	2.4 V	Threshold used to detect VCONN disconnect.

The VCONN powered accessory shall remove or weaken Ra when VCONN is in the valid voltage range (vVCONNValid). The VCONN powered accessory shall reapply Ra when VCONN falls below vRaReconnect as defined in Table 4-7. The VCONN powered accessory shall take into account the VCONN capacitance present in the accessory when discharging VCONN.

The maximum power consumption while in an Alternate Mode is defined by the specification specific to the Alternate Mode being used.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 4-7 VCONN 供电配件 (VPA) 接收器特性

	Minimum	Maximum	Notes
Voltage	3.0 V	5.5 V	Voltage range (vVCONNValid) over which this table applies
Inrush Capacitance		10 µF	An accessory shall not present more than the equivalent inrush capacitance to the VCONN source. The accessory is responsible for discharging its capacitance when detached from a port.
Power before Alternate Mode Entry		35 mW	Maximum power in USB suspend Note: Power shall be reduced 5 seconds after VCONN is applied if no Alternate Mode Entry has occurred. A VCONN power cycle may be required to re-enable USB-PD communication.
tVCONNDischarge		230 ms	Time from VPA disconnect to vVCONNDischarge met.
vVCONNDischarge		800 mV	VCONN voltage after tVCONNDischarge
vRaReconnect	800 mV		Voltage at which the VPA shall reapply Ra on the falling edge of VCONN.
vVCONNDisconnect	800 mV	2.4 V	Threshold used to detect VCONN disconnect.

当 VCONN 处于有效电压范围 (vVCONNValid) 时，VCONN 供电配件应移除或减弱 Ra。当 VCONN 低于表 4-7 中定义的 vRaReconnect 时，VCONN 供电配件应重新应用 Ra。当放电 VCONN 时，VCONN 供电配件应考虑配件中存在的 VCONN 电容。

备用模式下的最大功耗由所使用的备用模式特定规范定义。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 4-8 VCONN-Powered USB Device (VPD) Sink Characteristics

	Minimum	Maximum	Notes
Voltage	3.0 V	5.5 V	Voltage range (vVCONNValid) over which this table applies
Inrush Capacitance		10 µF	A VPD shall not present more than the equivalent inrush capacitance to the VCONN source. The VPD is responsible for discharging its capacitance when detached from a port.
Power before USB enumeration		35 mW	Maximum power in USB suspend
Power when active		500 mW (*USB 2.0*) 750 mW (*USB 3.2*)	A VPD shall only expose a low-power interface over USB.
tVCONNDischarge		230 ms	Time from VPD disconnect to vVCONNDischarge met.
vVCONNDischarge		800 mV	VCONN voltage after tVCONNDischarge
vRaReconnect	800 mV		Voltage at which the VPD shall reapply Ra on the falling edge of VCONN.
vVCONNDisconnect	800 mV	2.4 V	Threshold used to detect VCONN disconnect.

The VPD shall remove or weaken Ra when VCONN is in the valid voltage range (vVCONNValid).

The VPD shall reapply Ra when VCONN falls below vRaReconnect as defined in Table 4-8. The VPD shall take into account the VCONN capacitance present in the device when discharging VCONN.

4.5 Configuration Channel (CC)

4.5.1 Architectural Overview

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.

- Detect attach of USB ports, e.g. a Source to a Sink
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish data roles between two attached ports
- Discover and configure VBUS: USB Type-C Current modes or *USB Power Delivery*

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 4-8 VCONN 供电的 USB 设备 (VPD) 接收特性

	Minimum	Maximum	Notes
Voltage	3.0 V	5.5 V	Voltage range (vVCONNValid) over which this table applies
Inrush Capacitance		10 µF	A VPD shall not present more than the equivalent inrush capacitance to the VCONN source. The VPD is responsible for discharging its capacitance when detached from a port.
Power before USB enumeration		35 mW	Maximum power in USB suspend
Power when active		500 mW (*USB 2.0*) 750 mW (*USB 3.2*)	A VPD shall only expose a low-power interface over USB.
tVCONNDischarge		230 ms	Time from VPD disconnect to vVCONNDischarge met.
vVCONNDischarge		800 mV	VCONN voltage after tVCONNDischarge
vRaReconnect	800 mV		Voltage at which the VPD shall reapply Ra on the falling edge of VCONN.
vVCONNDisconnect	800 mV	2.4 V	Threshold used to detect VCONN disconnect.

当 VCONN 处于有效电压范围（vVCONNValid）内时，VPD 应移除或削弱 Ra。

当 VCONN 低于表 4-8 中定义的 vRaReconnect 时，VPD 应重新应用 Ra。VPD 在放电 VCONN 时应考虑设备中存在的 VCONN 电容。

4.5 配置通道（CC）

4.5.1 架构概述

对于 USB Type-C 解决方案，连接器上的两个引脚 CC1 和 CC2 用于建立和管理源到接收器的连接。当设备通过集线器连接时，集线器上的接收器 (UFP) 与源 (主机端口) 之间的连接以及接收器 (设备端口) 与源 (集线器上的 DFP) 之间的连接被视为单独的连接。从功能上讲，配置通道用于实现以下目的。

- 检测 USB 端口的连接，例如，源到接收器 • 解析电缆方向并扭转连接以建立 USB 数据总线路由 • 在两个连接端口之间建立数据角色 • 发现和配置 VBUS：USB Type-C 电流模式或 *USB Power Delivery*

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- Configure VCONN
- Discover and configure optional Alternate and Accessory modes

4.5.1.1 USB Data Bus Interface and USB Type-C Plug Flip-ability

Since the USB Type-C plug can be inserted in either right-side-up or upside-down position, the hosts and devices that support USB data bus functionality must operate on the signal pins that are actually connected end-to-end. In the case of *USB 2.0*, this is done by shorting together the two D+ signal pins and the two D− signal pins in the host and device receptacles. In the case of *USB 3.2* SuperSpeed USB or *USB4* TX/RX signals in a single-lane implementation, it requires the functional equivalent of a switch in both the host and device to appropriately route the TX and RX signal pairs to the connected path through the cable. For a *USB 3.2* SuperSpeed USB or *USB4* dual-lane implementation, the host and/or device resolves the lane ordering.

Figure 4-3 illustrates the logical data bus model for a USB Type-C-based Host connected to a USB Type-C-based Device that is only capable of SuperSpeed USB single-lane operation. The USB cable that sits between a host and device can be in one of four possible connected states when viewed by the host:

- Un-flipped straight through – Position ① ⇔ Position ①
- Un-flipped twisted through – Position ① ⇔ Position ②
- Flipped straight through – Position ② ⇔ Position ②
- Flipped twisted through – Position ② ⇔ Position ①

To establish the proper routing of the active USB data bus from host to device, the standard USB Type-C cable is wired such that a single CC wire is position aligned with the first TX/RX signal pairs (TXp1/TXn1 and RXp1/RXn1) – in this way, the CC wire and TX/RX data bus wires that are used for single-lane operational signaling within the cable track with regard to the orientation and twist of the cable. By being able to detect which of the CC pins (CC1 or CC2) at the receptacle is terminated by the device, the host is able to determine which TX/RX signals are to be used for the single-lane connection and the host can use this to control the functional switch for routing the TX/RX signal pairs. Similarly in the device, detecting which of the CC pins at the receptacle is terminated by the host allows the device to control the functional switch that routes its TX/RX signal pairs.

For a dual-lane implementation, the TX/RX signal pairs in the cable/plug aligned with the CC wire/pin is Lane 0 and in reference to *USB 3.2*, shall be identified as the Configuration Lane. The second TX/RX signal pairs (TXp2/TXn2 and RXp2/RXn2) in the cable/plug is Lane 1 of a dual-lane configuration.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• 配置 VCONN • 发现并配置可选的替代和附件模式

4.5.1.1 USB 数据总线接口和 USB Type-C 插头翻转功能

由于 USB Type-C 插头既可以正面插入，也可以反面插入，因此支持 USB 数据总线功能的主机和设备必须在实际端到端连接的信号引脚上进行操作。对于 *USB 2.0*，这是通过将主机和设备插座中的两个 D+ 信号引脚和两个 D– 信号引脚短接在一起来实现的。对于单通道实现中的 *USB 3.2* SuperSpeed USB 或 *USB4* TX/RX 信号，主机和设备中都需要具有相当于开关的功能，以便通过电缆将 TX 和 RX 信号对适当地路由到连接的路径。对于 *USB 3.2* SuperSpeed USB 或 *USB4* 双通道实现，主机和/或设备会解决通道排序问题。

图 4-3 说明了 USB Type-C 型主机连接到仅支持超高速 USB 单通道操作的 USB Type-C 型设备的逻辑数据总线模型。从主机的角度来看，主机和设备之间的 USB 电缆可能处于以下四种连接状态之一：

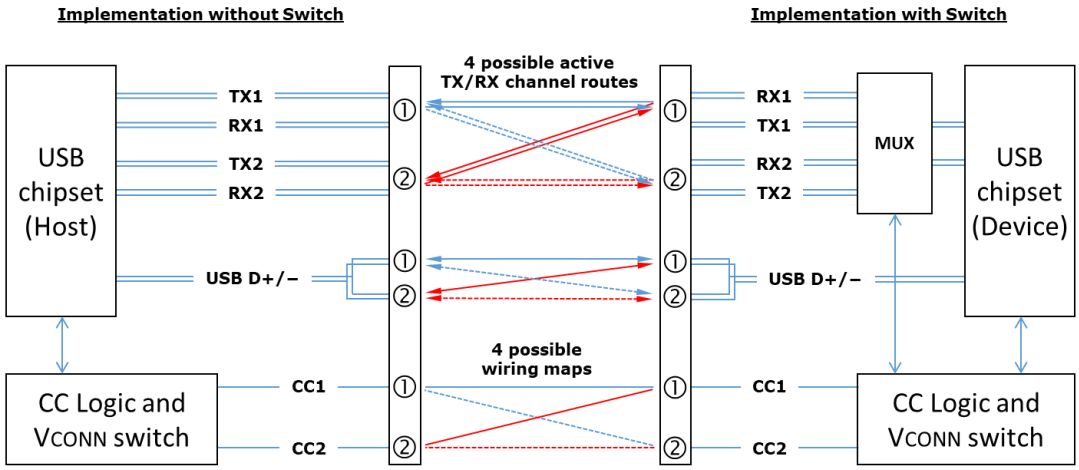
- 未翻转直接通过 – 位置 Position
- Un-flipped twisted through – Position Position
- Flipped straight through – Position Position
- Flipped twisted through – Position Position

为了正确布线从主机到设备的有源 USB 数据总线，标准 USB Type-C 电缆的布线方式是，单条 CC 线与第一个 TX/RX 信号对 (TXp1/TXn1 和 RXp1/RXn1) 的位置对齐 - 这样，用于在电缆轨道内进行单通道操作信号的 CC 线和 TX/RX 数据总线线就与电缆的方向和扭曲度有关。通过检测插座上的哪个 CC 引脚 (CC1 或 CC2) 由设备终止，主机能够确定哪些 TX/RX 信号将用于单通道连接，并且主机可以使用它来控制用于路由 TX/RX 信号对的功能开关。同样，在设备中，检测插座上的哪个 CC 引脚由主机终止允许设备控制路由其 TX/RX 信号对的功能开关。

对于双通道实施，与 CC 线/引脚对齐的电缆/插头中的 TX/RX 信号对为通道 0，并且参考 *USB 3.2*，应标识为配置通道。电缆/插头中的第二个 TX/RX 信号对（TXp2/TXn2 和 RXp2/RXn2）为双通道配置的通道 1。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

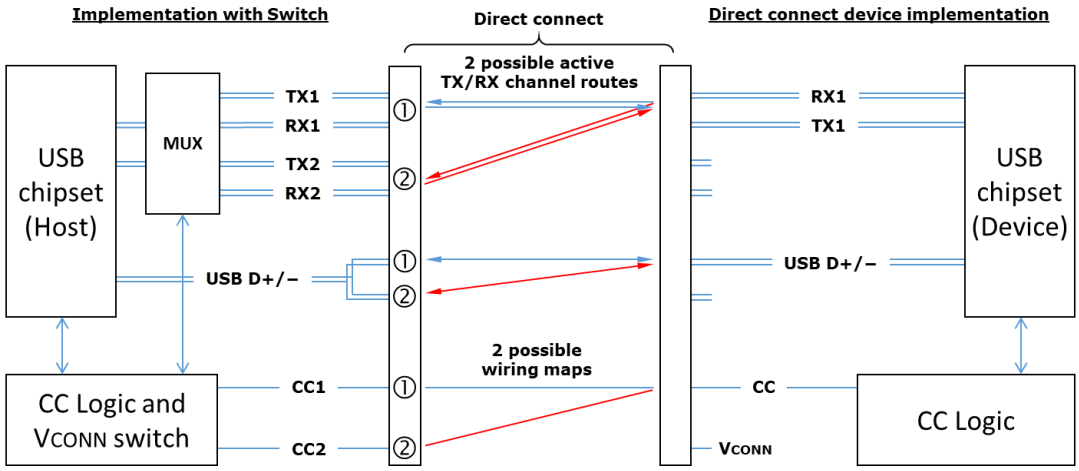
Figure 4-3 Logical Model for Single-Lane Data Bus Routing across USB Type-C-based Ports



While Figure 4-3 illustrates the functional model as a host connected to a device, this model equally applies to a USB hub's downstream ports as well.

Figure 4-4 illustrates the logical data bus model for a single-lane USB Type-C-based Device (implemented with a USB Type-C plug either physically incorporated into the device or permanently attached as a captive cable) connected directly to a USB Type-C-based Host. For the device, the location of the TX/RX data bus, *USB 2.0* data bus, CC and VCONN pins are fixed by design. Given that the device pin locations are fixed, only two possible connected states exist when viewed by the host.

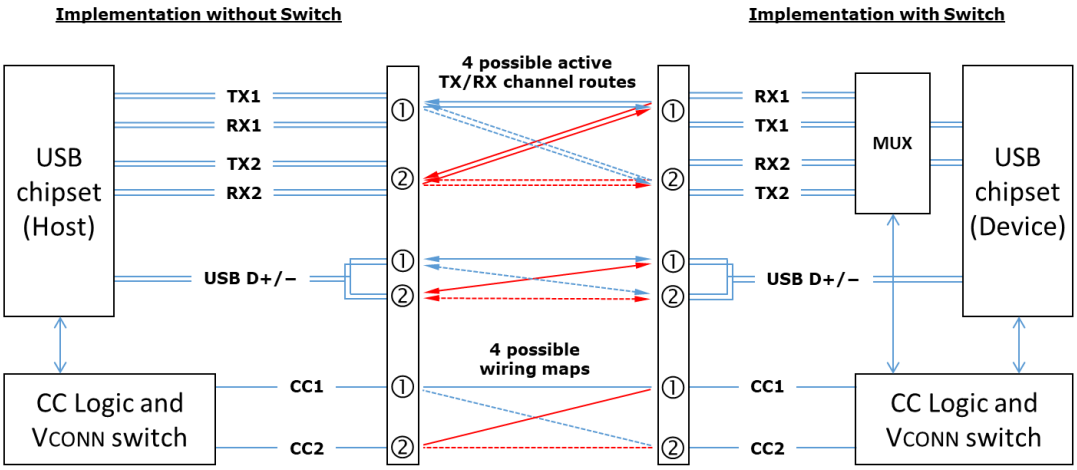
Figure 4-4 Logical Model for USB Type-C-based Ports for a Single-Lane Direct Connect Device



The functional requirements for implementing TX/RX data bus routing for the USB Type-C receptacle are not included in the scope of this specification. There are multiple host, device and hub architectures that can be used to accomplish this which could include either discrete or integrated switching, and could include merging this functionality with other *USB 3.2* or *USB4* design elements, e.g. a bus repeater.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

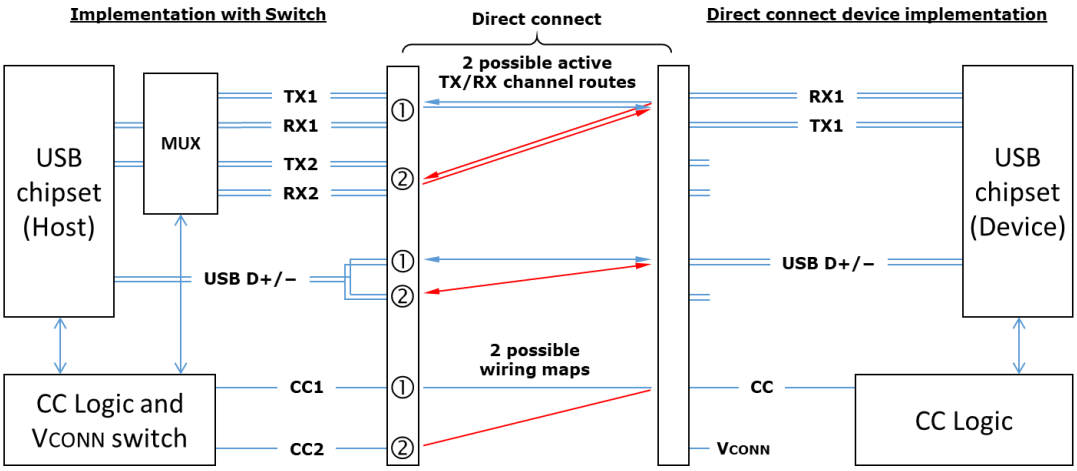
图 4-3 单通道数据总线布线逻辑模型
基于 USB Type-C 的端口



虽然图 4-3 说明了主机连接到设备的功能模型，但该模型同样适用于 USB 集线器的下游端口。

图 4-4 显示了单通道 USB Type-C 设备（使用 USB Type-C 插头实现，该插头可以物理地并入设备中或作为固定电缆永久连接）直接连接到 USB Type-C 主机的逻辑数据总线模型。对于该设备，TX/RX 数据总线、*USB 2.0* 数据总线、CC 和 VCONN 引脚的位置在设计上是固定的。鉴于设备引脚位置是固定的，从主机的角度来看，只有两种可能的连接状态。

图 4-4 USB Type-C 端口逻辑模型
单通道直接连接设备



本规范的范围不包括实现 USB Type-C 插座的 TX/RX 数据总线路由的功能要求。有多种主机、设备和集线器架构可用于实现此目的，这些架构可能包括分立或集成开关，也可能包括将此功能与其他 *USB 3.2* 或 *USB4* 设计元素（例如总线中继器）合并。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The functional requirements for addressing SBU1 and SBU2 routing is not included in the scope of this specification. For *USB4*, where SBTX and SBRX are mapped to SBU1 and SBU2, the adjustment to the mapping of these signals based on the connection state (flipped and/or twisted) of the cable is defined by the *USB4 Specification* (reference Sideband Channel Lane Reversal).

4.5.1.2 Connecting Sources and Sinks

Given that the USB Type-C receptacle and plug no longer differentiate host and device roles based on connector shape, e.g., as was the case with USB Type-A and Type-B connectors, any two ports that have USB Type-C receptacles can be connected together with a standard USB Type-C cable. Table 4-9 summarizes the expected results when interconnecting Source, Sink and DRP ports.

Table 4-9 USB Type-C-based Port Interoperability

	Source-only	**Sink-only**	**DRP (Dual-Role-Power)**
Source-only	Non-functional	Functional	Functional
Sink-only	Functional	Non-functional	Functional
DRP (Dual-Role-Power)	Functional	Functional	Functional*

* Resolution of roles may be automatic or manually driven

In the cases where no function results, neither port shall be harmed by this connection. The user has to independently realize the invalid combination and take appropriate action to resolve. While these two invalid combinations mimic traditional USB where host-to-host and device-to-device connections are not intended to work, the non-keyed USB Type-C solution does not prevent the user from attempting such interconnects. VBUS and VCONN shall not be applied by a Source (host) in these cases.

The typical flow for the configuration of the interface in the general USB case of a Source (Host) to a Sink (Device) is as follows:

1. Detect a valid connection between the ports (including determining cable orientation, Source/Sink and DFP/UFP relationship)
2. Optionally discover the cable's capabilities
3. Optionally establish alternatives to traditional USB power (See Section 4.6.2)
    a. *USB PD* communication over CC for advanced power delivery negotiation
    b. USB Type-C Current modes
    c. *USB BC 1.2*
4. USB Device Enumeration

For cases of Dual-Role-Power (DRP) ports connecting to either Source-only, Sink-only or another DRP, the process is essentially the same except that during the detecting a valid connection step, the DRP alternates between operating as a Source for detecting an attached Sink and presenting as a Sink to be detected by an attached Source. Ultimately this results in a Source-to-Sink connection.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

解决 SBU1 和 SBU2 路由的功能要求不在本规范的范围内。对于 *USB4*，其中 SBTX 和 SBRX 映射到 SBU1 和 SBU2，基于电缆的连~~接状态~~（翻转和/或扭曲）对这些信号映射的调整由 *USB4 Specification*（参考边带通道通道反转）定义。

4.5.1.2 连接源和接收器

由于 USB Type-C 插座和插头不再根据连接器形状区分主机和设备角色（例如 USB Type-A 和 Type-B 连接器的情况），因此任何两个具有 USB Type-C 插座的端口都可以通过标准 USB Type-C 电缆连接在一起。表 4-9 总结了互连源、接收器和 DRP 端口时的预期结果。

表 4-9 USB Type-C 端口互操作性

	Source-only	**Sink-only**	**DRP (Dual-Role-Power)**
Source-only	Non-functional	Functional	Functional
Sink-only	Functional	Non-functional	Functional
DRP (Dual-Role-Power)	Functional	Functional	Functional*

* 角色解析可以自动或手动进行

如果无法正常工作，则此连接不会损害任何端口。用户必须自行识别无效组合并采取适当措施来解决。虽然这两种无效组合模仿传统 USB，其中主机到主机和设备到设备的连接无法工作，但非键控 USB Type-C 解决方案不会阻止用户尝试此类互连。在这些情况下，源（主机）不得应用 VBUS 和 VCONN。

在一般 USB 情况下，源 (Host) 到接收器 (Device) 的接口配置典型流程如下：

1. 检测端口之间的有效连接（包括确定电缆方向、源/接收器和 DFP/UFP 关系） 2. 可选择发现电缆的功能 3. 可选择建立传统 USB 电源的替代方案（参见第 4.6.2 节） a. 通过 CC 进行 *USB PD* 通信以实现高级电力传输协商

b. USB Type-C 电流模式 c. *USB BC 1.2*

4.USB 设备枚举

对于双角色电源 (DRP) 端口连接到仅源、仅接收器或另一个 DRP 的情况，过程基本相同，只是在检测有效连接步骤期间，DRP 交替作为源来检测连接的接收器，并作为接收器呈现给连接的源进行检测。最终，这会产生源到接收器的连接。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.1.2.1 Detecting a Valid Source-to-Sink Connection

The general concept for setting up a valid connection between a Source and Sink is based on being able to detect terminations residing in the product being attached.

To aid in defining the functional behavior of CC, a pull-up (Rp) and pull-down (Rd) termination model is used – actual implementation in hosts and devices may vary, for example, the pull-up termination could be replaced by a current source. Figure 4-5 and Figure 4-6 illustrates two models, the first based on a pull-up resistor in the Source and the second replacing this with a current source.

Figure 4-5 Pull-Up/Pull-Down CC Model

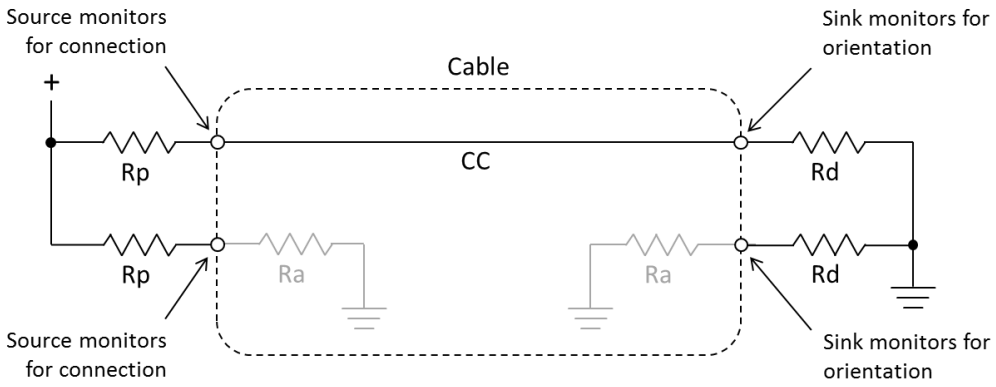
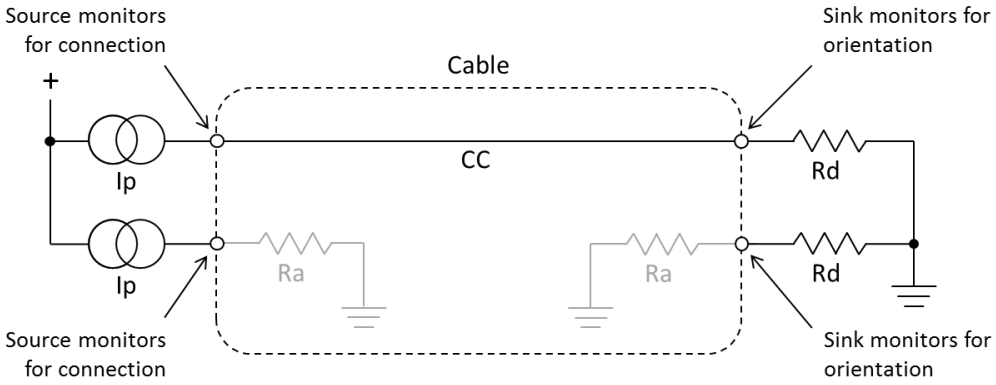


Figure 4-6 Current Source/Pull-Down CC Model



Initially, a Source exposes independent Rp terminations on its CC1 and CC2 pins, and a Sink exposes independent Rd terminations on its CC1 and CC2 pins, the Source-to-Sink combination of this circuit configuration represents a valid connection. To detect this, the Source monitors CC1 and CC2 for a voltage lower than its unterminated voltage – the choice of Rp is a function of the pull-up termination voltage and the Source's detection circuit. This indicates that either a Sink, a powered cable, or a Sink connected via a powered cable has been attached.

Prior to application of VCONN, a powered cable exposes Ra on its VCONN pin. Ra represents the load on VCONN plus any resistive elements to ground. In some cable plugs it might be a pure resistance and in others it may be simply the load.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.1.2.1 检测有效的源到接收器连接

在源和接收器之间建立有效连接的一般概念是基于能够检测所连接产品中的终端。

为了帮助定义 CC 的功能行为，使用了上拉 (Rp) 和下拉 (Rd) 终端模型 - 主机和设备中的实际实现可能有所不同，例如，上拉终端可以用电流源代替。图 4-5 和图 4-6 说明了两种模型，第一种基于源中的上拉电阻，第二种用电流源代替它。

图 4-5 上拉/下拉 CC 模型

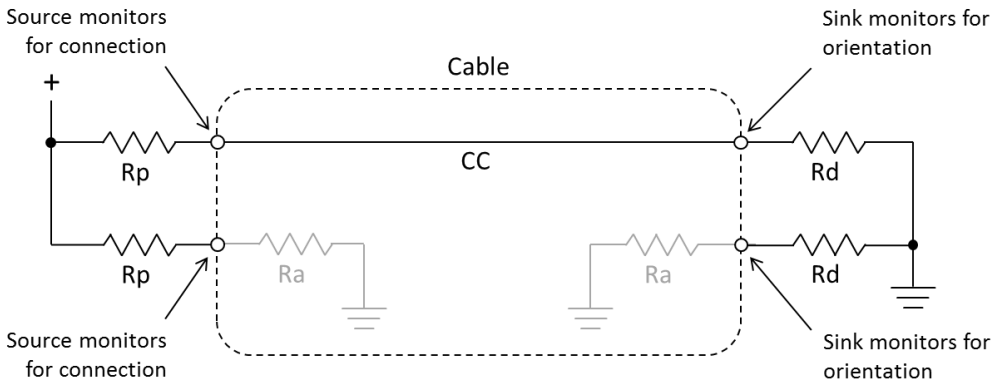
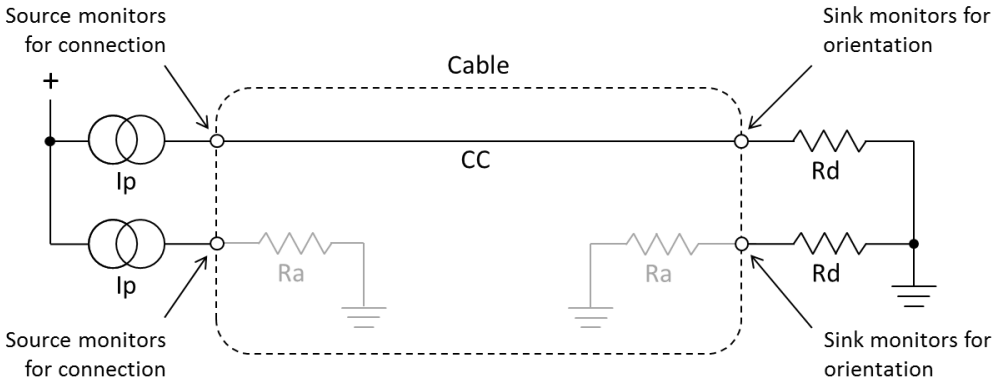


图 4-6 电流源/下拉 CC 模型



最初，源端在其 CC1 和 CC2 引脚上暴露独立的 Rp 端接，而接收器在其 CC1 和 CC2 引脚上暴露独立的 Rd 端接，这种电路配置的源端到接收器组合代表有效连接。为了检测这一点，源端监控 CC1 和 CC2 的电压是否低于其未端接电压 - Rp 的选择取决于上拉端接电压和源端的检测电路。这

表示已连接 Sink、供电电缆、或者通过供电电缆连接的 Sink。

在应用 VCONN 之前，带电电缆的 VCONN 引脚上会暴露 Ra。Ra 表示 VCONN 上的负载加上接地电阻元件。在某些电缆插头中，它可能是纯电阻，而在其他电缆插头中，它可能只是负载。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The Source has to be able to differentiate between the presence of Rd and Ra to know whether there is a Sink attached and where to apply VCONN. The Source is not required to source VCONN unless Ra is detected.

Two special termination combinations on the CC pins as seen by a Source are defined for directly attached Accessory Modes: Ra/Ra for Audio Adapter Accessory Mode (Appendix A) and Rd/Rd for Debug Accessory Mode (Appendix B).

The Source uses de-bounce timers to reliably detect states on the CC pins to de-bounce the connection (tCCDebounce), and hide *USB PD* BMC communications (tPDDebounce).

Table 4-10 summarizes the port state from the Source's perspective.

Table 4-10 Source Perspective

CC1	CC2	State	Position
Open	**Open**	Nothing attached	N/A
Rd	**Open**	Sink attached	①
Open	**Rd**		②
Open	**Ra**	Powered cable without Sink attached	①
Ra	**Open**		②
Rd	**Ra**	Powered cable with Sink, VCONN-Powered Accessory (VPA), or VCONN-Powered USB Device (VPD) attached	①
Ra	**Rd**		②
Rd	**Rd**	Debug Accessory Mode attached (Appendix B)	N/A
Ra	**Ra**	Audio Adapter Accessory Mode attached (Appendix A)	N/A

Once the Sink is powered, the Sink monitors CC1 and CC2 for a voltage greater than its local ground. The CC pin that is at a higher voltage (i.e. pulled up by Rp in the Source) indicates the orientation of the plug.

Table 4-11 summarizes the typical behaviors for simple Sources (Hosts) and Sinks (Devices) for each state in Table 4-10.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Source 必须能够区分 Rd 和 Ra 的存在，以便知道是否连接了 Sink 以及在何处应用 VCONN。除非检测到 Ra，否则 Source 不需要为 VCONN 提供源。

对于直接连接的附件模式，定义了源所见的 CC 引脚上的两种特殊终端组合：音频适配器附件模式为 Ra/Ra（附录 A），调试附件模式为 Rd/Rd（附录 B）。

源使用去抖动定时器来可靠地检测 CC 引脚上的状态以消除连接抖动 (tCCDebounce)，并隐藏 *USB PD* BMC 通信 (tPDDebounce)。

表 4-10 从源的角度总结了端口状态。

表 4-10 源视角

CC1	CC2	State	Position
Open	**Open**	Nothing attached	N/A
Rd	**Open**	Sink attached	①
Open	**Rd**		②
Open	**Ra**	Powered cable without Sink attached	①
Ra	**Open**		②
Rd	**Ra**	Powered cable with Sink, VCONN-Powered Accessory (VPA), or VCONN-Powered USB Device (VPD) attached	①
Ra	**Rd**		②
Rd	**Rd**	Debug Accessory Mode attached (Appendix B)	N/A
Ra	**Ra**	Audio Adapter Accessory Mode attached (Appendix A)	N/A

一旦 Sink 通电，Sink 就会监控 CC1 和 CC2 的电压是否高于其本地接地。电压较高的 CC 引脚（即被 Source 中的 Rp 上拉）指示插头的方向。

表 4-11 总结了表 4-10 中每种状态下简单源（主机）和接收器（设备）的典型行为。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 4-11 Source (Host) and Sink (Device) Behaviors by State

State	Source Behavior	Sink Behavior
Nothing attached	• Sense CC pins for attach • Do not apply VBUS or VCONN	• Sense VBUS for attach
Sink attached	• Sense CC for orientation • Sense CC for detach • Apply VBUS and VCONN	• Sense CC pins for orientation • Sense loss of VBUS for detach
Powered cable without Sink attached	• Sense CC pins for attach • Do not apply VBUS or VCONN	• Sense VBUS for attach
Powered cable with Sink, VCONN-Powered Accessory, or VCONN-Powered USB Device attached	• Sense CC for orientation • Sense CC for detach • Apply VBUS and VCONN • Detect VPD and remove VBUS	• If accessories or VPDs are supported, see Source Behavior with exception that VBUS is not applied., otherwise, N/A.
Debug Accessory Mode attached	• Sense CC pins for detach • Reconfigure for debug	• Sense VBUS for detach • Reconfigure for debug
Audio Adapter Accessory Mode attached	• Sense CC pins for detach • Reconfigure for analog audio	• If accessories are supported, see Source Behavior, otherwise, N/A

Figure 4-3 shows how the inserted plug orientation is detected at the Source's receptacle by noting on which of the two CC pins in the receptacle an Rd termination is sensed. Now that the Source (Host) has recognized that a Sink (Device) is attached and the plug orientation is determined, it configures the TX/RX data bus routing to the receptacle.

The Source (Host) then turns on VBUS. For the CC pin that does not connect Source-to-Sink through the cable, the Source supplies VCONN and may remove the termination. With the Sink (Device) now powered, it configures the USB data path. This completes the Host-to-Device connection.

The Source monitors the CC wire for the loss of pull-down termination to detect detach. If the Sink is removed, the Source port removes any voltage applied to VBUS and VCONN, resets its interface configuration and resumes looking for a new Sink attach.

Once a valid Source-to-Sink connection is established, alternatives to traditional USB power (VBUS as defined by either *USB 2.0* or *USB 3.2* specifications) may be available depending on the capabilities of the host and device. These include USB Type-C Current, USB Power Delivery, and *USB Battery Charging 1.2*.

In the case where *USB PD* PR_Swap is used to swap the Source and Sink of VBUS, the supplier of VCONN remains unchanged during and after the VBUS power swap. The new Source monitors the CC wire and the new Sink monitors VBUS to detect detach. When a detach event is detected, any voltages applied to VBUS and VCONN are removed, each port resets its interface configuration and resumes looking for an attach event.

In the case where *USB PD* DR_Swap is used to swap the data roles (DFP and UFP), the source of VBUS and VCONN do not change after the data role swap.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 4-11 源 (主机) 和接收器 (设备) 状态行为

State	Source Behavior	Sink Behavior
Nothing attached	• Sense CC pins for attach • Do not apply VBUS or VCONN	• Sense VBUS for attach
Sink attached	• Sense CC for orientation • Sense CC for detach • Apply VBUS and VCONN	• Sense CC pins for orientation • Sense loss of VBUS for detach
Powered cable without Sink attached	• Sense CC pins for attach • Do not apply VBUS or VCONN	• Sense VBUS for attach
Powered cable with Sink, VCONN-Powered Accessory, or VCONN-Powered USB Device attached	• Sense CC for orientation • Sense CC for detach • Apply VBUS and VCONN • Detect VPD and remove VBUS	• If accessories or VPDs are supported, see Source Behavior with exception that VBUS is not applied., otherwise, N/A.
Debug Accessory Mode attached	• Sense CC pins for detach • Reconfigure for debug	• Sense VBUS for detach • Reconfigure for debug
Audio Adapter Accessory Mode attached	• Sense CC pins for detach • Reconfigure for analog audio	• If accessories are supported, see Source Behavior, otherwise, N/A

图 4-3 显示了如何通过注意插座中两个 CC 引脚中的哪一个检测到 Rd 终端来检测源插座的插入插头方向。现在，源（主机）已识别出已连接接收器（设备），并且已确定插头方向，它会配置到插座的 TX/RX 数据总线路由。

然后，源 (主机) 打开 VBUS。对于未通过电缆连接源到接收器的 CC 引脚，源提供 VCONN 并可能移除终端。现在接收器 (设备) 已通电，它会配置 USB 数据路径。这样就完成了主机到设备的连接。

源端监控 CC 线是否丢失下拉终端以检测断开连接。如果 Sink 被移除，源端端口将移除施加到 VBUS 和 VCONN 的任何电压，重置其接口配置并继续寻找新的 Sink 连接。

一旦建立了有效的源到接收器连接，根据主机和设备的功能，可以使用传统 USB 电源（由 *USB 2.0* 或 *USB 3.2* 规范定义的 VBUS）的替代方案。这些替代方案包括 USB Type-C Current、USB Power Delivery 和 *USB Battery Charging 1.2*。

在使用 *USB PD* PR_Swap 交换 VBUS 的源和接收器的情况下，VCONN 的供应方在 VBUS 电源交换期间和之后保持不变。新的源监控 CC 线，新的接收器监控 VBUS 以检测分离。当检测到分离事件时，施加到 VBUS 和 VCONN 的任何电压都会被移除，每个端口都会重置其接口配置并继续寻找连接事件。

在使用 *USB PD* DR_Swap 交换数据角色（DFP 和 UFP）的情况下，数据角色交换后 VBUS 和 VCONN 的来源不会改变。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

In the case where *USB PD* VCONN_Swap is used to swap the VCONN source, the VBUS Source/Sink and DFP/UFP roles are maintained during and after the VCONN swap.

The last step in the normal USB Type-C connect process is for the USB device to be attached and enumerated per standard *USB 2.0* and *USB 3.2* processes.

4.5.1.3 Configuration Channel Functional Models

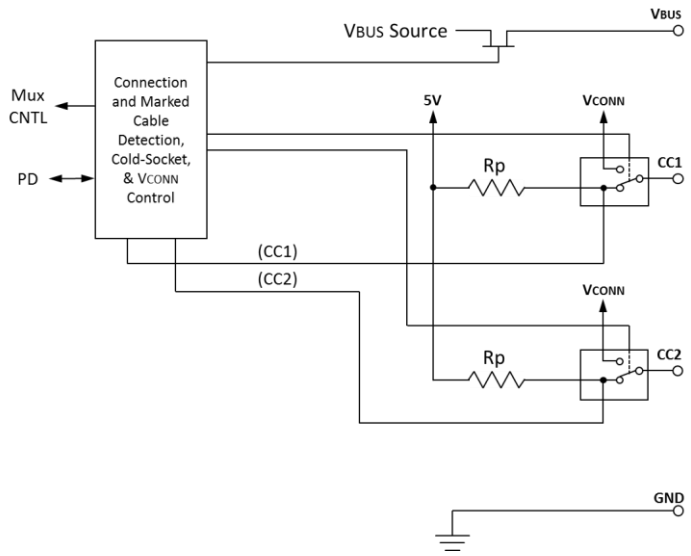
The functional models for the configuration channel behavior based on the CC1 and CC2 pins are described in this section for each port type: Source, Sink and Dual-Role-Power (DRP).

The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete. In these figures, VBUS and VCONN may or may not actually be available.

4.5.1.3.1 Source Configuration Channel Functional Model

Figure 4-7 illustrates the functional model for CC1 and CC2 for a Source port prior to attach. This illustration includes consideration for *USB PD*.

Figure 4-7 Source Functional Model for CC1 and CC2



Referring to Figure 4-7, a port that behaves as a Source has the following functional characteristics:

1. The Source uses a FET to enable/disable power delivery across VBUS and initially the Source has VBUS disabled.
2. The Source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a Sink. The presence of an Rd pull-down resistor on either pin indicates that a Sink is being attached. The value of Rp indicates the initial USB Type-C Current level supported by the host.
3. The Source uses the CC pin pull-down characteristic to detect and establish the correct routing for the SuperSpeed USB data path and determine which CC pin is intended for supplying VCONN.
4. Once a Sink is detected, the Source enables VBUS and VCONN.
5. The Source can dynamically adjust the value of Rp to indicate a change in available USB Type-C Current to a Sink.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

在使用 *USB PD* VCONN_Swap 交换 VCONN 源的情况下，在 V CONN 交换期间和之后，VBUS Source/Sink 和 DFP/UFP 角色将保持不变。

正常 USB Type-C 连接过程的最后一步是按照标准 *USB 2.0* 和 *USB 3.2* 流程连接和枚举 USB 设备。

4.5.1.3 配置通道功能模型

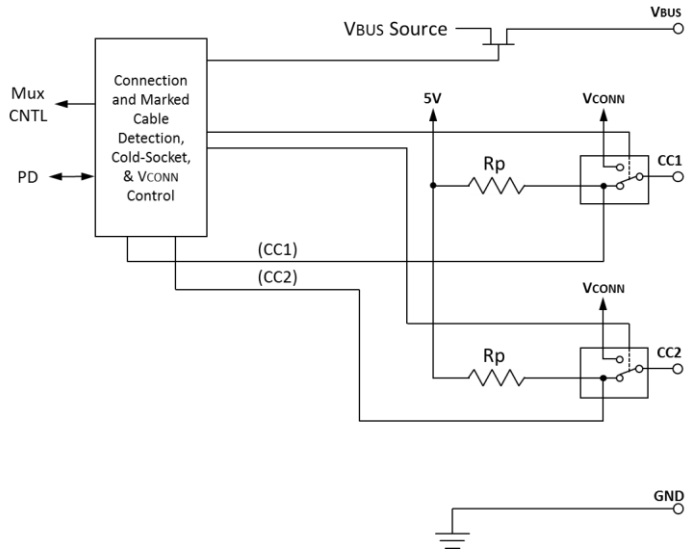
本节针对每个端口类型描述了基于 CC1 和 CC2 引脚的配置通道行为的功能模型：源端口、接收器端口和双角色电源 (DRP)。

以下部分中的图片说明了 CC 检测过程完成后的 CC1 和 CC2 路由。在这些图中，VBUS 和 VCONN 实际上可能可用，也可能不可用。

4.5.1.3.1 源配置通道功能模型

图 4-7 说明了连接之前源端口的 CC1 和 CC2 的功能模型。
此图包括对*USB PD*的考虑。

图 4-7 CC1 和 CC2 的源功能模型



参考图 4-7，作为源的端口具有以下功能特征：

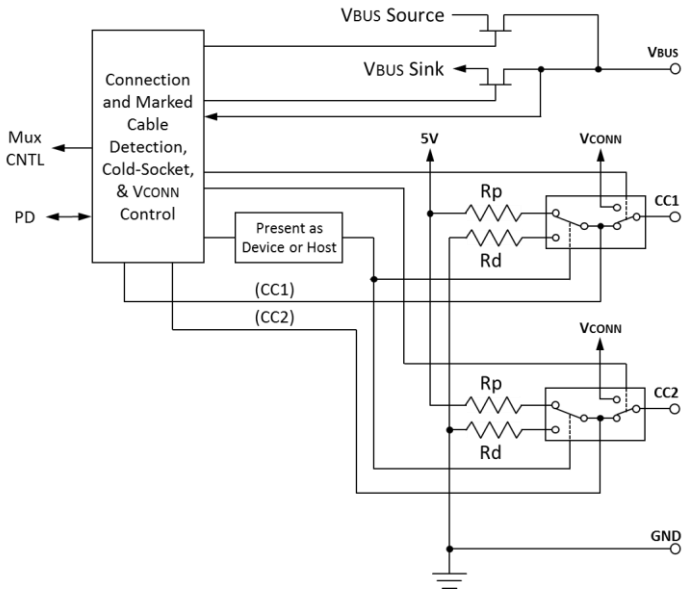
1. 源端使用 FET 来启用/禁用 VBUS 上的供电，并且源端最初禁用 VBUS。2. 源端在 CC1 和 CC2 上提供上拉电阻 (Rp)，并监控两者以检测接收器。任一引脚上存在 Rd 下拉电阻表示正在连接 Sink。Rp 的值表示主机支持的初始 USB Type-C 电流水平。3. Source 使用 CC 引脚下拉特性来检测和建立超高速 USB 数据路径的正确路由，并确定哪个 CC 引脚用于提供 VCONN。4. 一旦检测到 Sink，Source 就会启用 VBUS 和 VCONN。5. Source 可以动态调整 Rp 的值以指示可用于 Sink 的 USB Type-C 电流的变化。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6. The Source monitors the continued presence of Rd to detect Sink detach. When a detach event is detected, the Source removes, if supplied, VBUS and VCONN, and returns to step 2.
7. If the Source supports advanced functions (*USB Power Delivery* and/or Alternate Modes), *USB PD* communication is required.

Figure 4-8 illustrates the functional model for CC1 and CC2 for a Source that supports *USB PD* PR_Swap.

Figure 4-8 Source Functional Model Supporting USB PD PR_Swap



4.5.1.3.2 Sink Configuration Channel Functional Model

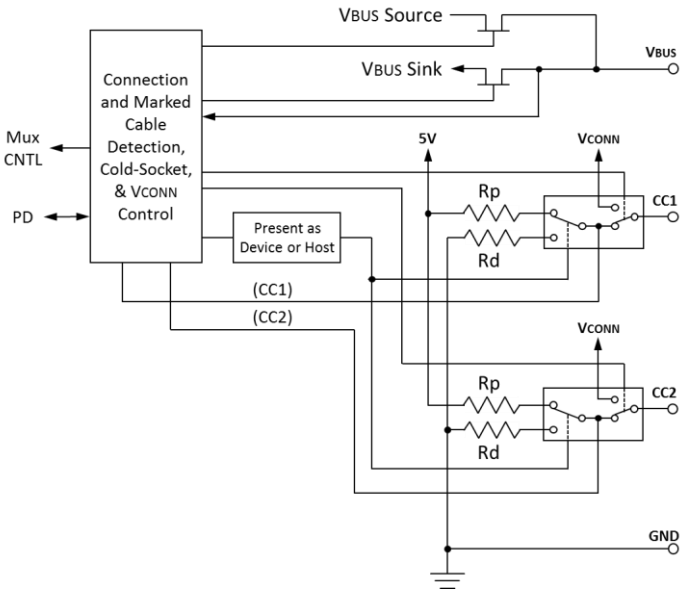
Figure 4-9 illustrates the functional model for CC1 and CC2 for a Sink. This illustration includes consideration for both USB Type-C Current and *USB PD*.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6. 源端监控 Rd 是否持续存在，以检测接收器是否断开连接。检测到断开连接事件时，源端将移除 VBUS 和 VCONN（如果已提供），并返回步骤 2。7. 如果源端支持高级功能 (*USB Power Delivery* 和/或备用模式），则需要 *USB PD* 通信。

图 4-8 说明了支持 *USB PD* PR_Swap 的源的 CC1 和 CC2 的功能模型。

图 4-8 支持 USB PD PR_Swap 的源功能模型

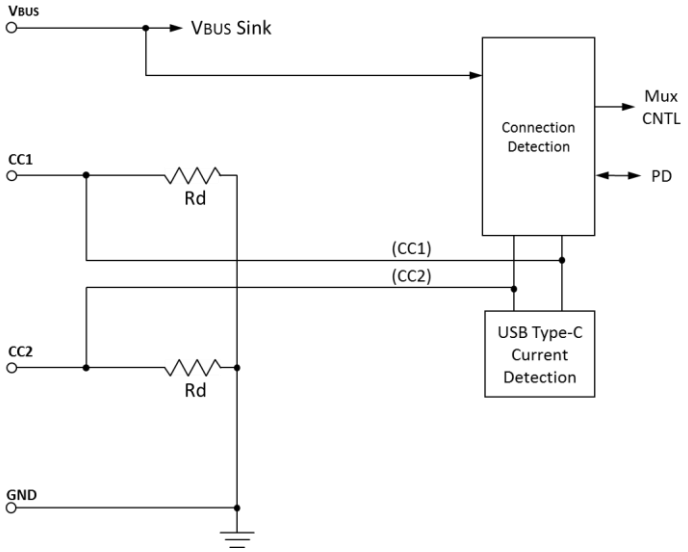


4.5.1.3.2 接收器配置通道功能模型

图 4-9 显示了接收器的 CC1 和 CC2 功能模型。此图同时考虑了 USB Type-C Current 和 *USB PD*。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-9 Sink Functional Model for CC1 and CC2



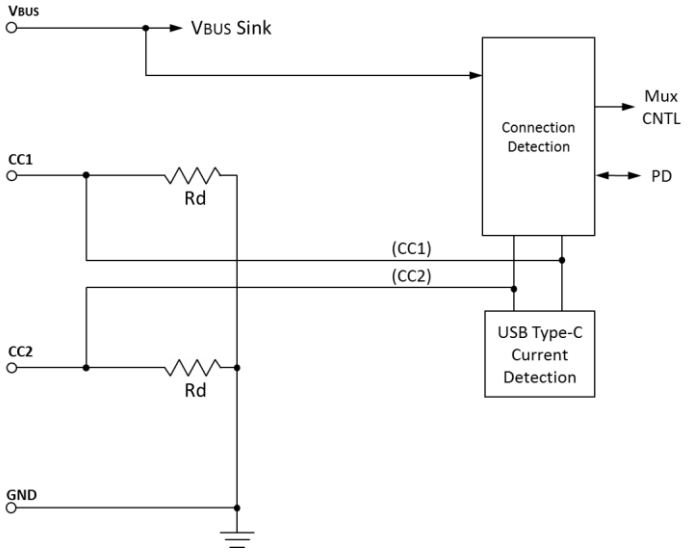
Referring to Figure 4-9, a port that behaves as a Sink has the following functional characteristics:

1. The Sink terminates both CC1 and CC2 to GND using pull-down resistors.
2. The Sink determines that a Source is attached by the presence of power on VBUS.
3. The Sink uses the CC pin pull-up characteristic to detect and establish the correct routing for the SuperSpeed USB data path.
4. The Sink can optionally monitor CC to detect an available higher USB Type-C Current from the Source. The Sink shall manage its load to stay within the detected Source current limit.
5. If the Sink supports advanced functions (*USB Power Delivery* and/or Alternate Modes), *USB PD* communication is required.

Figure 4-10 illustrates the functional model for CC1 and CC2 for a Sink that supports *USB PD* PR_Swap and supports *USB PD* VCONN_Swap prior to attach.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-9 CC1 和 CC2 的接收器功能模型



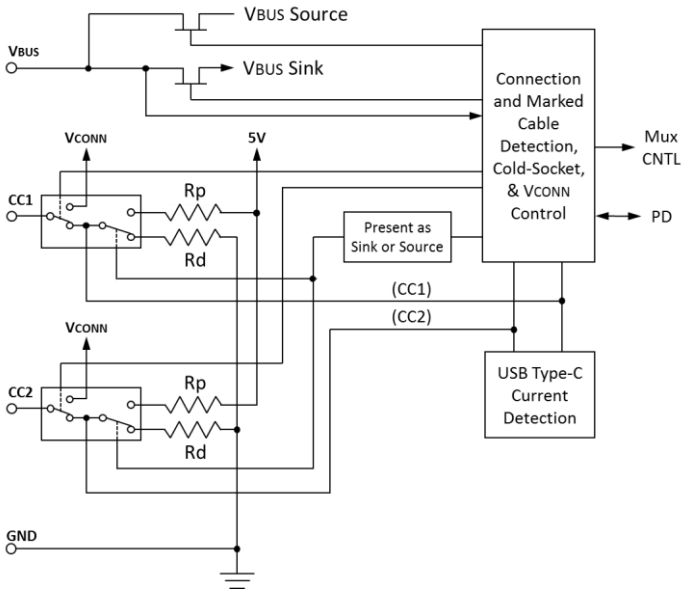
参考图4-9，作为Sink的端口有以下功能特征：

1. Sink 使用下拉电阻将 CC1 和 CC2 端接至 GND。2. Sink 通过 VBUS 上的电源确定源已连接。3. Sink 使用 CC 引脚上拉特性来检测并建立超高速 USB 数据路径的正确路由。4. Sink 可以选择性地监控 CC，以检测源是否有可用的更高 USB Type-C 电流。Sink 应管理其负载以保持在检测到的源电流限制范围内。5. 如果 Sink 支持高级功能 (*USB Power Delivery* 和/或替代模式)，则需要 *USB PD* 通信。

图 4-10 说明了支持 *USB PD* PR_Swap 并在连接之前支持 *USB PD* VCONN_Swap 的 Sink 的 CC1 和 CC2 的功能模型。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

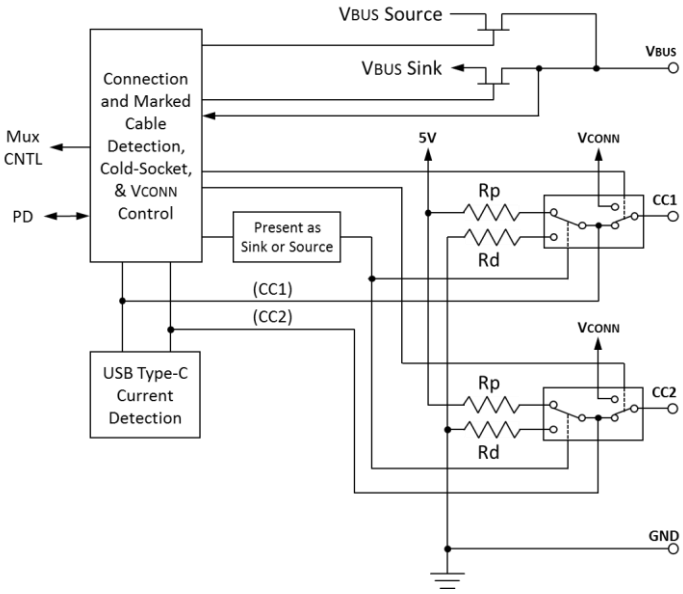
Figure 4-10 Sink Functional Model Supporting USB PD PR_Swap and VCONN_Swap



4.5.1.3.3 Dual-Role-Power (DRP) Configuration Channel Functional Model

Figure 4-11 illustrates the functional model for CC1 and CC2 for a DRP presenting as a Source prior to attach. This illustration includes consideration for both the USB Type-C Current and the *USB PD* features.

Figure 4-11 DRP Functional Model for CC1 and CC2

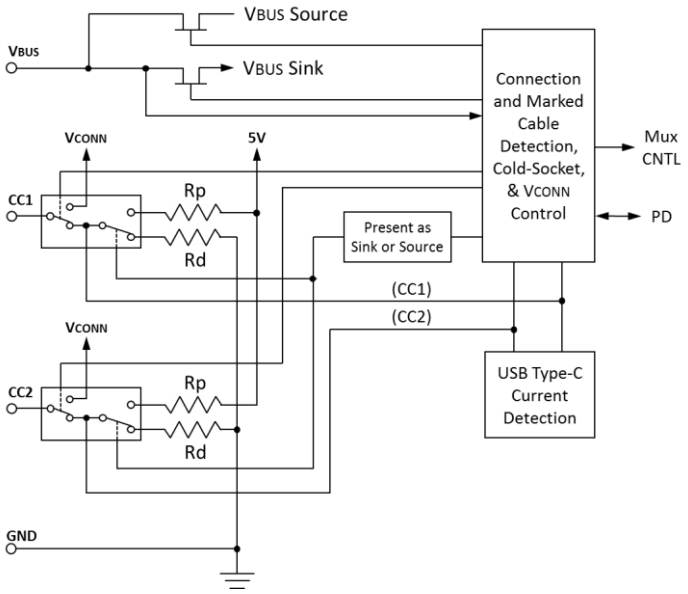


Referring to Figure 4-11, a port that can alternate between DFP and UFP behaviors has the following functional characteristics:

1. The DRP uses a FET to enable/disable power delivery across VBUS and initially when in Source mode has VBUS disabled.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

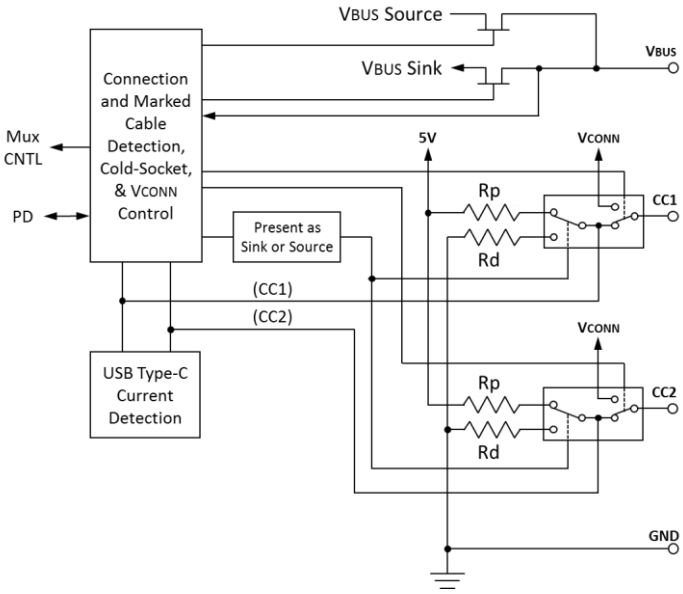
图 4-10 支持 USB PD PR_Swap 和 VCONN_Swap 的 Sink 功能模型



4
.5.1.3.3 双角色电源 (DRP) 配置通道功能模型

图 4-11 说明了 DRP 在连接前作为源呈现时的 CC1 和 CC2 功能模型。此图考虑了 USB Type-C Current 和 *USB PD* 功能。

图 4-11 CC1 和 CC2 的 DRP 功能模型



参考图4-11，可以在DFP和UFP行为之间交替的端口具有以下功能特征：

1. DRP 使用 FET 来启用/禁用 VBUS 上的供电，最初
   在源模式下，VBUS 已禁用。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

2. The DRP uses switches for presenting as a Source or Sink.
3. The DRP has logic used during initial attach to toggle between Source and Sink operation:
    a. Until a specific stable state is established, the DRP alternates between exposing itself as a Source and Sink. The timing of this process is dictated by a period (tDRP), percentage of time that a DRP exposes Rp (dcSRC.DRP) and role transition time (tDRPTransition).
    b. When the DRP is presenting as a Source, it follows Source operation to detect an attached Sink – if a Sink is detected, it applies VBUS, VCONN, and continues to operate as a Source (e.g., cease alternating).
    c. When the DRP is presenting as a Sink, it monitors VBUS to detect that it is attached to a Source – if a Source is detected, it continues to operate as a Sink (cease alternating).
4. If the DRP supports advanced functions (*USB Power Delivery* and/or Alternate Modes), *USB PD* communication is required.

4.5.1.4 USB Type-C Port Power Roles and Role Swapping Mechanisms

USB Type-C ports on products (USB hosts, USB devices, USB chargers, etc.) can be generally characterized as implementing one of seven power role behavioral models:

- Source-only
- Source (Default) – strong preference toward being a Source but subsequently capable of becoming a Sink using USB PD swap mechanisms.
- Sink-only
- Sink (Default) – strong preference toward being a Sink but subsequently capable of becoming a Source using USB PD swap mechanisms.
- DRP: Toggling (Source/Sink)
- DRP: Sourcing Device
- DRP: Sinking Host

Two independent sets of swapping mechanisms are defined for USB Type-C port implementations, one based on role swapping within the initial state machine connection process and the other based on subsequent use of *USB PD*-based swapping mechanisms.

4.5.1.4.1 USB Type-C State-Machine-Based Role Swapping

During the initial USB Type-C state machine connection process, the products being connected end up in one of the two following roles associated with the termination of its port:

- Rp → VBUS and VCONN source and behaving as a downstream facing port (USB Host)
- Rd → VBUS sink and behaving as an upstream facing port (USB Device)

A USB Type-C DRP-based product may incorporate either or both the Try.SRC and Try.SNK swap mechanisms to affect the resulting role. Try.SRC allows a DRP that has a policy-based preference to be a Source when connecting to another DRP to effect a transition from a destined Sink role to the Source role. Alternately, Try.SNK allows a DRP that has a policy-based preference to be a Sink when connecting to another DRP to effect a transition from a destined Source role to the Sink role. Connection timing and other factors are involved in this process as defined in the USB Type-C state machine operation (see Section 4.5.2). It is

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

2. DRP 使用交换机来呈现为源 (Source) 或接收器 (Sink)。

3. DRP 具有在初始连接期间用于在源和接收器操作之间切换的逻辑：

a. 在建立特定的稳定状态之前，DRP 会交替显示自己为源和接收器。此过程的时间由周期 (tDRP)、DRP 暴露 Rp 的时间百分比 (dcSRC.DRP) 和角色转换时间 (tDRPTransition) 决定。b. 当 DRP 显示为源时，它会遵循源操作来检测连接的接收器 - 如果检测到接收器，它会应用 VBUS、VCONN 并继续作为源运行（例如，停止交替）。c. 当 DRP 显示为接收器时，它会监控 VBUS 以检测它是否连接到源 - 如果检测到源，它会继续作为接收器运行（停止交替）。

4. 如果 DRP 支持高级功能（*USB Power Delivery* 和/或备用模式），则需要 *USB PD* 通信。

4.5.1.4 USB Type-C 端口电源角色和角色交换机制

产品（USB 主机、USB 设备、USB 充电器等）上的 USB Type-C 端口通常可描述为实现七种电源角色行为模型之一：

• 仅源 • 源（默认）——强烈倾向于成为源，但随后能够使用 USB PD 交换机制成为接收器。
• 仅接收器 • 接收器（默认）——强烈倾向于成为接收器，但随后能够使用 USB PD 交换机制成为源。• DRP：切换（源/接收器）• DRP：源设备 • DRP：接收器主机

为 USB Type-C 端口实现定义了两组独立的交换机制，一组基于初始状态机连接过程中的角色交换，另一组基于后续使用基于 *USB PD* 的交换机制。

4.5.1.4.1 基于 USB Type-C 状态机的角色交换

在初始 USB Type-C 状态机连接过程中，所连接的产品最终会处于与其端口终止相关的以下两种角色之一：

• Rp → VBUS 和 VCONN 源并充当下游端口（USB 主机）
• Rd → VBUS 接收器并充当上游端口（USB 设备）

基于 USB Type-C DRP 的产品可以结合 Try.SRC 和 Try.SNK 交换机制中的一种或两种来影响最终角色。Try.SRC 允许具有基于策略的 DRP 连接到另一个 DRP 时，优先选择作为源，以实现从目标接收器角色到源角色的转换。或者，Try.SNK 允许具有基于策略的偏好的 DRP 在连接到另一个 DRP 时作为接收器，以实现从目标源角色到接收器角色的转换。此过程涉及连接时序和其他因素，如 USB Type-C 状态机操作中所定义（参见第 4.5.2 节）。它是

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

important to note that these mechanisms, Try.SRC and Try.SNK, can only be used once as part of the initial connection process.

Try.SRC and Try.SNK are intended to ensure more predictable power roles when initially connecting two DRPs, especially if the port partner does not support *USB PD*. For example, a small mobile device may want to implement Try.SNK, so that when attaching to a DRP laptop, the mobile device will always initially be the power sink. Similarly, a laptop or Power Bank may wish to implement Try.SRC to ensure it always sources power to attached DRPs. Self-powered devices such as AMAs or those whose primary function is a data UFP may also consider implementing Try.SNK to ensure they can properly expose their functionality. If both sides support *USB PD*, the appropriate roles may then be further refined or swapped as per the *USB PD* specification.

4.5.1.4.2 USB PD-based Power Role, Data Role and VCONN Swapping

Following the completion of the initial USB Type-C state machine connection process, products may use *USB PD*-based swapping mechanisms to command a change power roles, data roles and which end of the cable will supply VCONN. These mechanisms are:

- *USB PD* PR_Swap : swaps Source (Rp) and Sink (Rd)
- *USB PD* DR_Swap : swaps DFP (host data) and UFP (device data) roles
- *USB PD* VCONN_Swap : swaps which port supplies VCONN

Table 4-12 summarizes the behaviors of a port in response to the three *USB PD* swap commands.

Table 4-12 USB PD Swapping Port Behavior Summary

	DFP/UFP Data Roles	Rp/Rd	VBUS Source/Sink	VCONN Source
PR_Swap	Unchanged	Swapped	Swapped	Unchanged
DR_Swap	Swapped	Unchanged	Unchanged	Unchanged
VCONN_Swap	Unchanged	Unchanged	Unchanged	Swapped*

* Swapping of VCONN source port

4.5.1.4.3 Power Role Behavioral Model Summary

Table 4-13 provides a summary of the defining characteristics of the seven fundamental power roles.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

需要注意的是，这些机制 Try.SRC 和 Try.SNK 只能作为初始连接过程的一部分使用一次。

Try.SRC 和 Try.SNK 旨在确保在最初连接两个 DRP 时更可预测的电源角色，尤其是在端口伙伴不支持 *USB PD* 的情况下。例如，小型移动设备可能希望实现 Try.SNK，以便在连接到 DRP 笔记本电脑时，移动设备最初始终是电源接收器。同样，笔记本电脑或移动电源可能希望实现 Try.SRC，以确保它始终为连接的 DRP 供电。自供电设备（例如 AMA）或主要功能是数据 UFP 的设备也可以考虑实现 Try.SNK，以确保它们能够正确展示其功能。如果双方都支持 *USB PD*，则可以根据 *USB PD* 规范进一步细化或交换适当的角色。

4.5.1.4.2 基于 USB PD 的电源角色、数据角色和 VCONN 交换

完成初始 USB Type-C 状态机连接过程后，产品可以使用基于 *USB PD* 的交换机制来命令更改电源角色、数据角色以及电缆的哪一端将为 VCONN 供电。这些机制包括：

- *USB PD* PR_Swap : 交换 Source (Rp) 和 Sink (Rd) • *USB PD* DR_Swap : 交换 DFP (主机数据) 和 UFP (设备数据) 角色 • *USB PD* VCONN_Swap : 交换哪个端口提供 VCONN

表 4-12 总结了端口响应三个 *USB PD* swap 命令的行为。

表 4-12 USB PD 交换端口行为摘要

	DFP/UFP Data Roles	Rp/Rd	VBUS Source/Sink	VCONN Source
PR_Swap	Unchanged	Swapped	Swapped	Unchanged
DR_Swap	Swapped	Unchanged	Unchanged	Unchanged
VCONN_Swap	Unchanged	Unchanged	Unchanged	Swapped*

* 交换 VCONN 源端口

4.5.1.4.3 权力角色行为模型总结

表 4-13 总结了七个基本权力角色的定义特征。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 4-13 Power Role Behavioral Model Summary

Power Role		Toggles	PR_Swap	USB Host	USB Device	DFP	UFP	DR_Swap	Try.SRC/ Try.SNK	Connects with
Source-Only		No	NA	Opt.	Opt.[1]	Req.	Opt.	Opt.	NA	Sink/ DRP
Source (Default)		No	Req.	Opt.	Opt.[1]	Req.	Opt.	Opt.	NA	Sink/ DRP
Sink-Only		No	NA	Opt.[1]	Opt.	Opt.	Req.	Opt.	NA	Source/ DRP
Sink (Default)		No	Req.	Opt.[1]	Opt.	Opt.	Req.	Opt.	NA	Source/ DRP
DRP	**Toggling (Source/Sink)**	Req.	Req.	Opt.	Opt.	Req.	Req.	Req.	Opt.	Source/ Sink/ DRP
	Sourcing Device	Req.	Req.	NA	Req.	Req.	Req.	Req.	Opt.	
	Sinking Host	Req.	Req.	Req.	NA	Req.	Req.	Req.	Opt.	

Note: 1. Requires use of DR_Swap

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 4-13 权力角色行为模型摘要

Connection Where	Source/Sink PRD	Source/Sink PRD	Source/Source PRD	Source/Source PRD	Source/Sink PRD		
Source/Sink Transition	AN	AN	AN	AN	Stop	Stop	Stop
PWR_Role	Stop	Stop	Stop	Stop	Request	Request	Request
PFU	Stop	Stop	Request	Request	Request	Request	Request
PFD	Request	Request	Stop	Stop	Request	Request	Request
BSU Received	1 Stop	1 Stop	Stop	Stop	Stop	Request	AN
BSU Sent	Stop	Stop	1 Stop	1 Stop	Stop	AN	Request
PWR_Role	AN	Request	AN	Request	Request	Request	Request
Signal Sent	on	on	on	on	Request	Request	Request
Port Power Role	**Source Source**	**Source Source (Delayed)**	**Source Source**	**Source Sink (Delayed)**	**Sink Source (Source/Sink)**	**Sink Source Received**	**Sink Sink Held**
					PRD		

Note 1 Requires PRS_Wait

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2 CC Functional and Behavioral Requirements

This section provides the functional and behavioral requirements for implementing CC. The first sub-section provides connection state diagrams that are the basis for the remaining sub-sections.

The terms Source (SRC) and Sink (SNK) used in this section refer to the port's power role while the terms DFP and UFP refer to the port's data role. A DRP (Dual-Role-Power) port is capable of acting as either a Source or Sink. Typically Sources are found on hosts and supply VBUS while a Sink is found on a device and consumes power from VBUS. When a connection is initially made, the port's initial power state and data role are established. *USB PD* introduces three swap commands that may alter a port's power or data role:

- The PR_Swap command changes the port's power state as reflected in the following state machines. PR_Swap does not change the port sourcing VCONN.
- The DR_Swap command has no effect on the following state machines or VCONN as it only changes the port's data role.
- VCONN_Swap command changes the port sourcing VCONN. The PR_Swap command and DR_Swap command have no effect on the port sourcing VCONN.

Note: A VCONN-Powered USB Device that supports the optional Charge-Through capability, once detected via *USB PD* messaging, will also change the Host-side port's power state without changing the port sourcing VCONN.

Note: *USB PD* defines another optional swapping mechanism (FR_Swap) that is used in a special case where a user interaction could inadvertently trigger a need to change the source of VBUS. A variant of PR_Swap, FR_Swap similarly swaps Source (Rp) and Sink (Rd) between two connected ports. For purposes of this specification, only PR_Swap is explicitly considered in the behavior requirements and implementations that support FR_Swap should, where applicable, apply PR_Swap-related behaviors to FR_Swap. See the *USB PD* specification for further details regarding FR_Swap.

The connection state diagrams and CC behavior descriptions in this section describe the behavior of receptacle-based ports. The plug on a direct connect device or a device with a captive cable shall behave as a plug on a cable that is attached at its other end in normal orientation to a receptacle, These devices shall apply and sense CC voltage levels on pin A5 only and pin B5 shall have an impedance above zOPEN, unless it is a VCONN-Powered Accessory, in which case B5 shall have an impedance Ra.

4.5.2.1 Connection State Diagrams

This section provides reference connection state diagrams for CC-based behaviors.

Refer to Section 4.5.2.2 for the specific state transition requirements related to each state shown in the diagrams.

Refer to Section 4.5.2.4 for a description of which states are mandatory for each port type, and a list of states where *USB PD* communication is permitted.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2 CC 功能和行为要求

本节提供实现 CC 的功能和行为要求。第一小节提供连接状态图，这是其余小节的基础。

本节中使用的术语“ 源 (SRC) ”和“ 接收器 (SNK) ”是指端口的电源角色，而术语“ DFP ”和“ UFP ”是指端口的数据角色。DRP（双角色电源）端口可以充当源或接收器。通常，源位于主机上并提供 VBUS，而接收器位于设备上并从 VBUS 消耗电力。最初建立连接时，将建立端口的初始电源状态和数据角色。*USB PD* 引入了三个可能改变端口电源或数据角色的交换命令：

- PR_Swap 命令会更改端口的电源状态，如以下状态机所示。PR_Swap 不会更改端口源 VCONN。• DR_Swap 命令对以下状态机或 VCONN 没有影响，因为它只会更改端口的数据角色。• VCONN_Swap 命令会更改端口源 VCONN。PR_Swap 命令和 DR_Swap 命令对端口源 VCONN 没有影响。

注意：支持可选 Charge-Through 功能的 VCONN 供电 USB 设备一旦通过 *USB PD* 消息传递检测到，也将更改主机端端口的电源状态，而不会更改端口源 VCONN。

注意：*USB PD* 定义了另一种可选交换机制 (FR_Swap)，用于特殊情况，即用户交互可能会无意中触发更改 VBUS 源的需要。FR_Swap 是 PR_Swap 的变体，类似地在两个连接的端口之间交换源 (Rp) 和接收器 (Rd)。出于本规范的目的，在行为要求中仅明确考虑 PR_Swap，支持 FR_Swap 的实现应在适用的情况下将与 PR_Swap 相关的行为应用于 FR_Swap。有关 FR_Swap 的更多详细信息，请参阅 *USB PD* 规范。

本节中的连接状态图和 CC 行为描述描述了基于插座的端口的行为。直接连接设备或带有固定电缆的设备上插头的行为应与电缆上的插头相同，电缆另一端以正常方向连接到插座，这些设备应仅在引脚 A5 上应用和感应 CC 电压电平，引脚 B5 的阻抗应高于 zOPEN，除非它是 VCONN 供电的配件，在这种情况下 B5 的阻抗应为 Ra。

4.5.2.1 连接状态图

本节提供基于 CC 的行为的参考连接状态图。

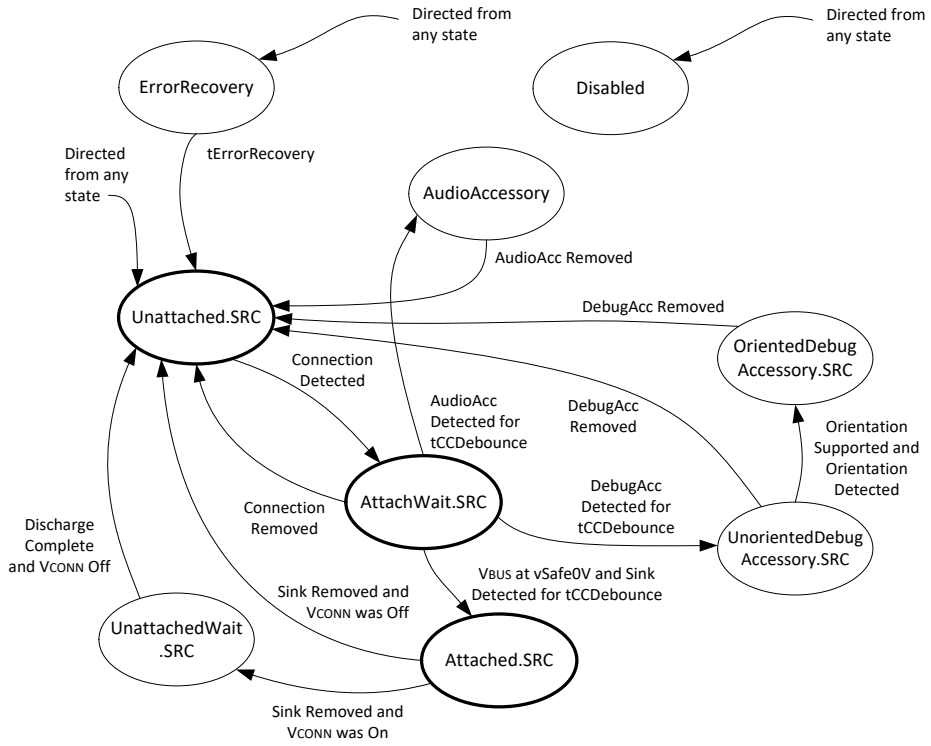
有关图中所示每个状态的具体状态转换要求，请参阅第 4.5.2.2 节。

请参阅第 4.5.2.4 节，了解每种端口类型强制执行的状态描述，以及允许 *USB PD* 通信的状态列表。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-12 illustrates a connection state diagram for a Source (Host/Hub DFP).

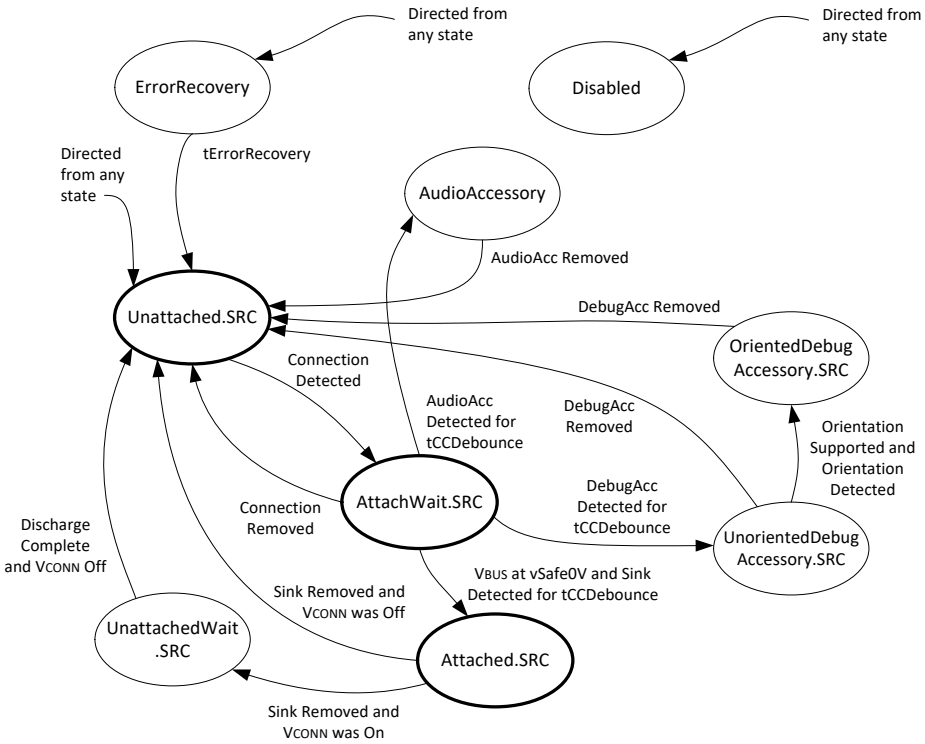
Figure 4-12 Connection State Diagram: Source



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-12 说明了源（主机/集线器 DFP）的连接状态图。

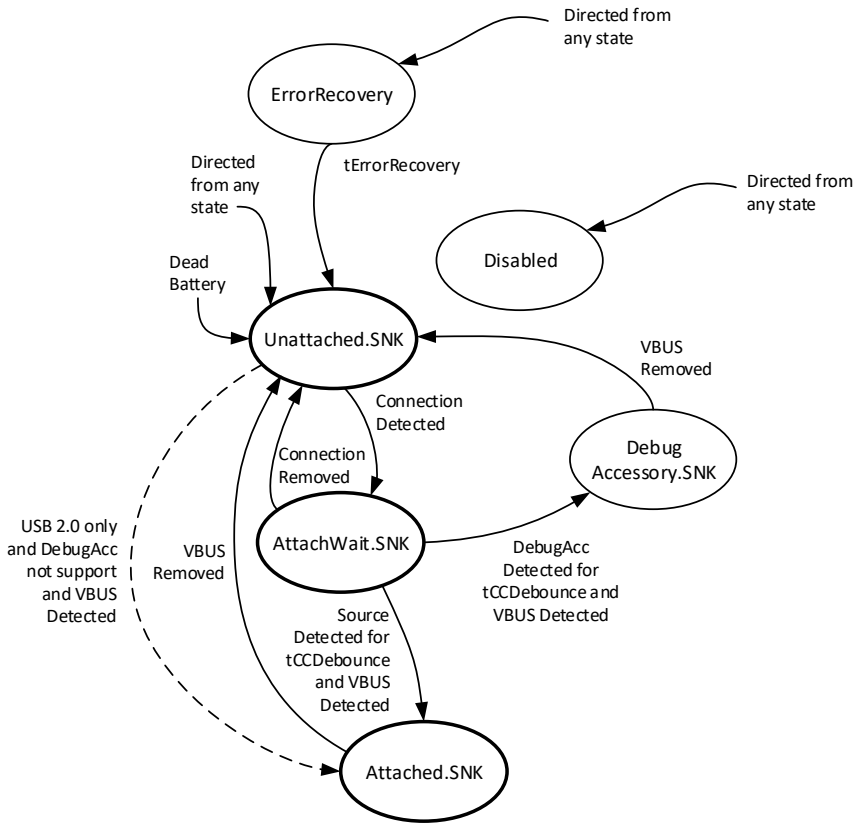
图 4-12 连接状态图：源



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-13 illustrates a connection state diagram for a simple Sink (Device/Hub UFP).

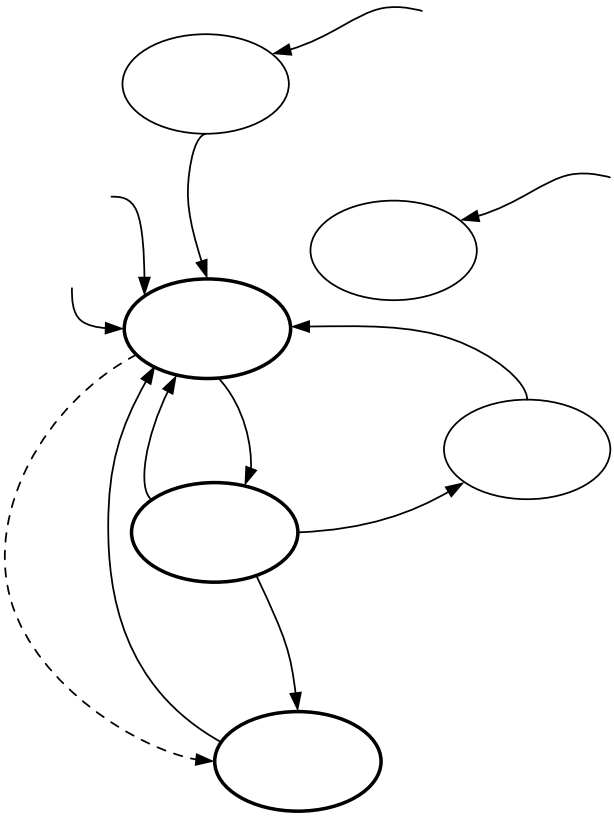
Figure 4-13 Connection State Diagram: Sink



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-13 说明了简单接收器（设备/集线器 UFP）的连接状态图。

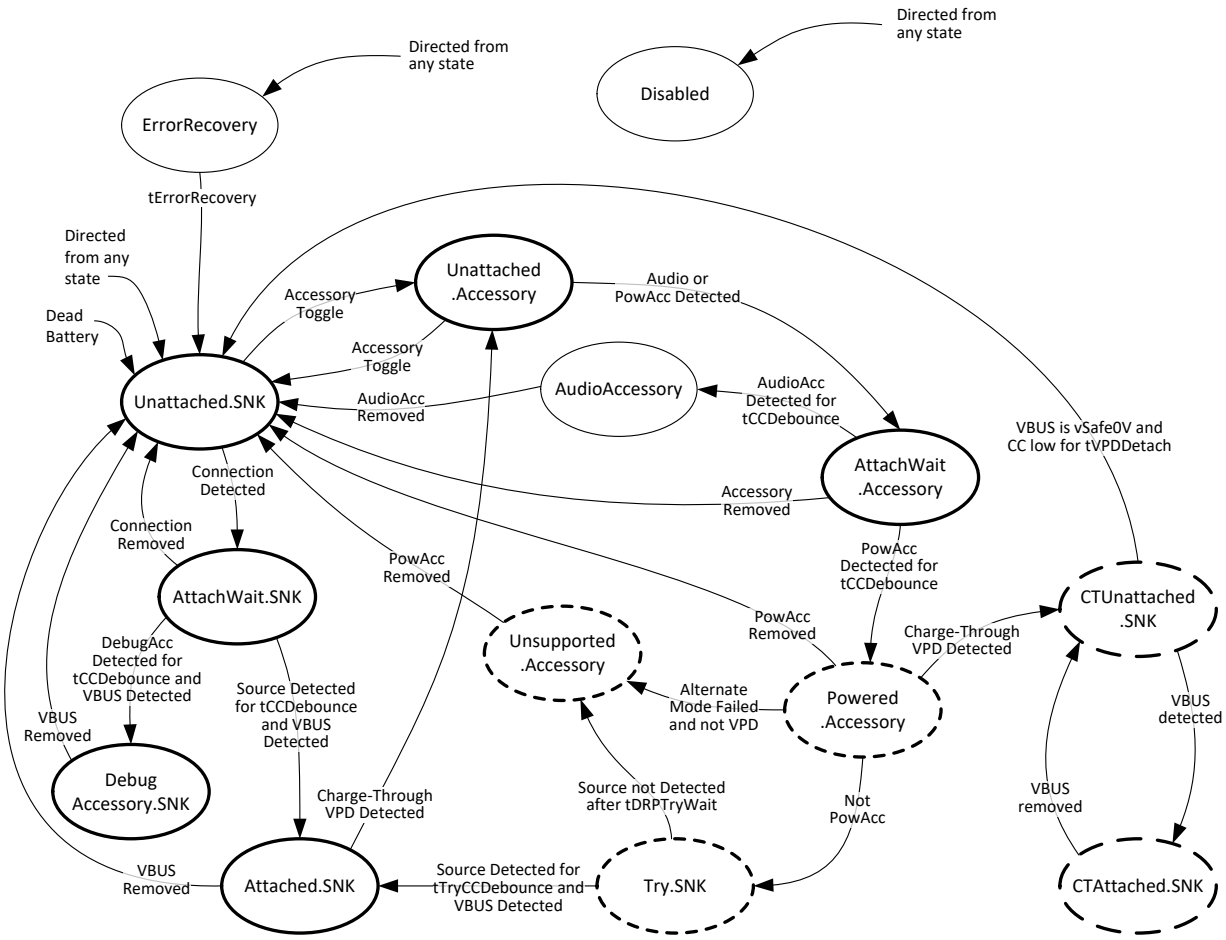
图 4-13 连接状态图：Sink



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-14 illustrates a connection state diagram for a Sink that supports Accessory Modes.

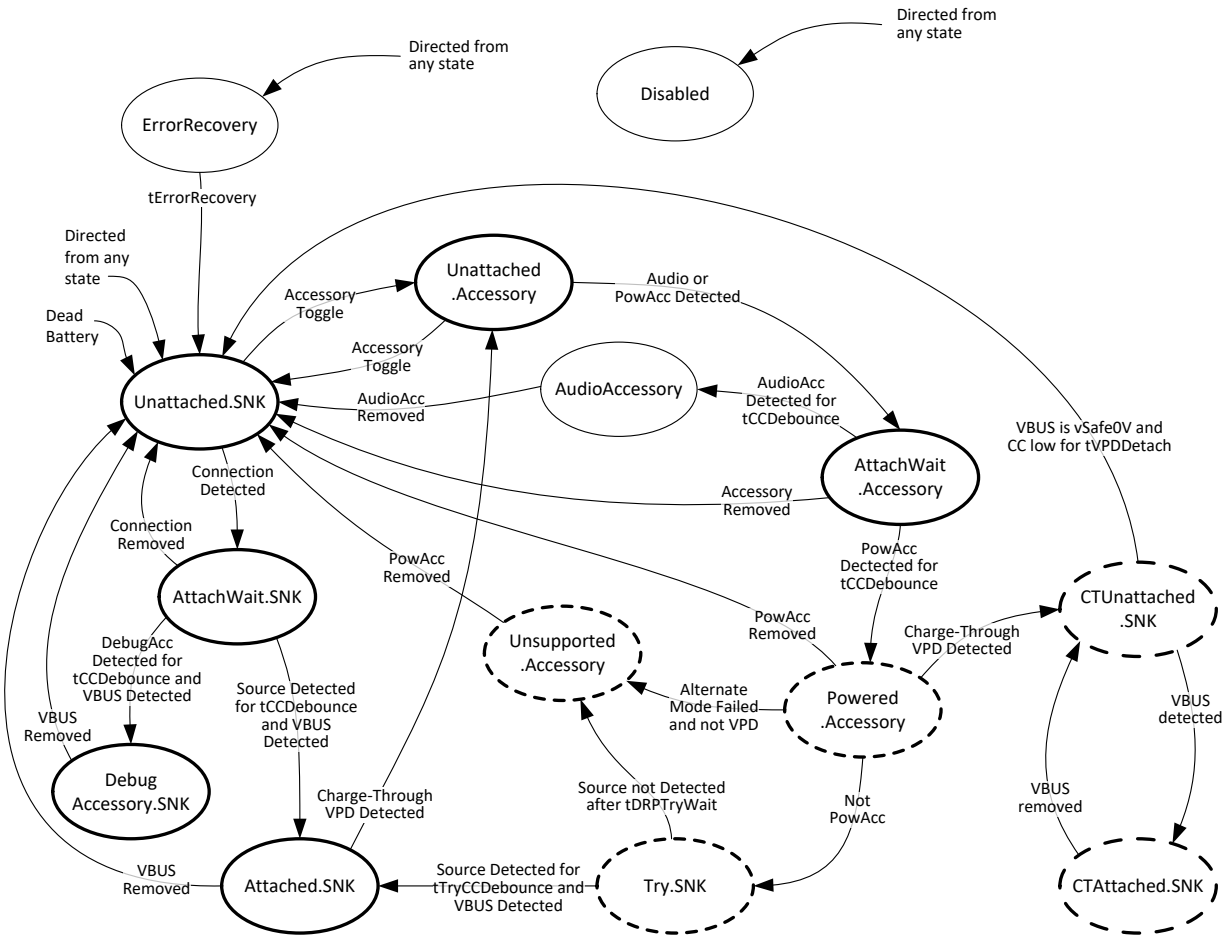
Figure 4-14 Connection State Diagram: Sink with Accessory Support



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图4-14说明了支持配件模式的接收器的连接状态图。

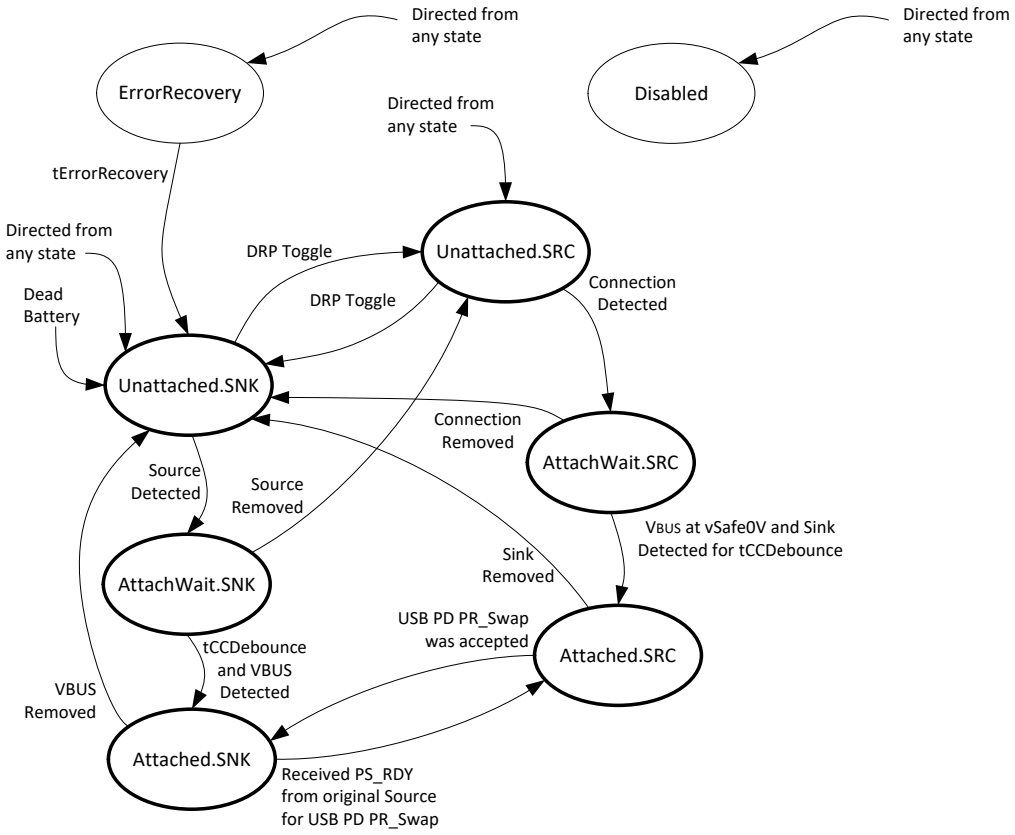
图 4-14 连接状态图：接收器与附件 支持



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-15 illustrates a connection state diagram for a simple DRP (Dual-Role-Power) port.

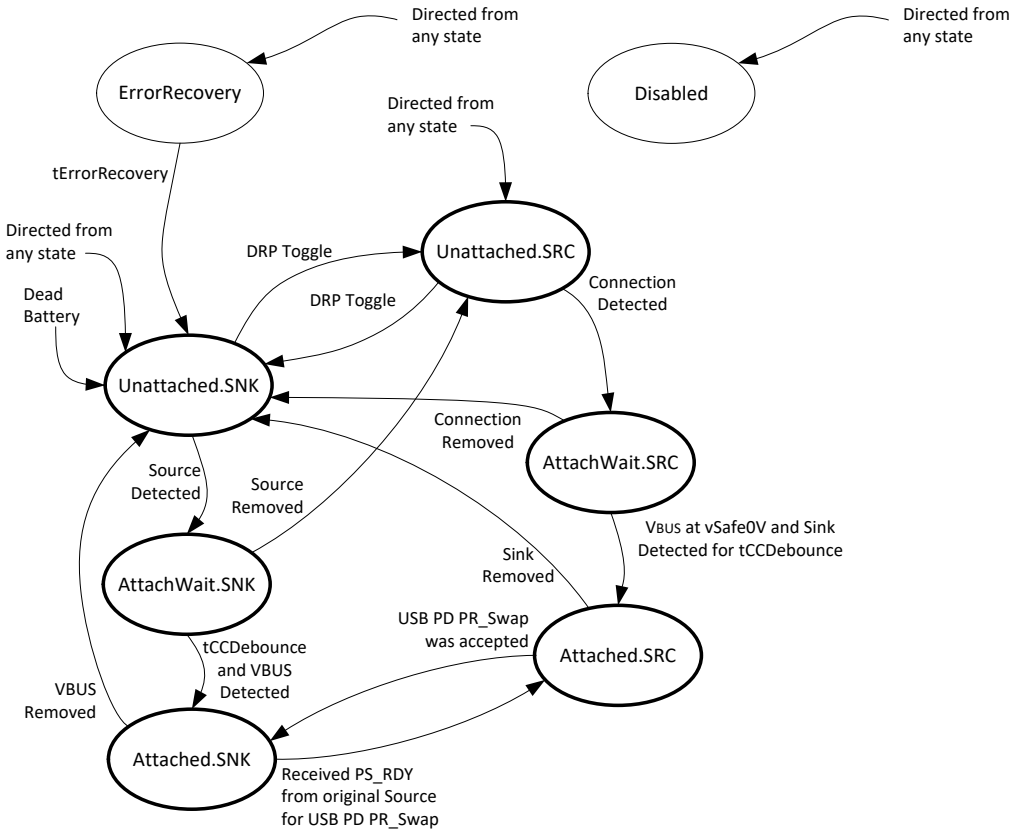
Figure 4-15 Connection State Diagram: DRP



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-15 说明了简单 DRP（双角色电源）端口的连接状态图。

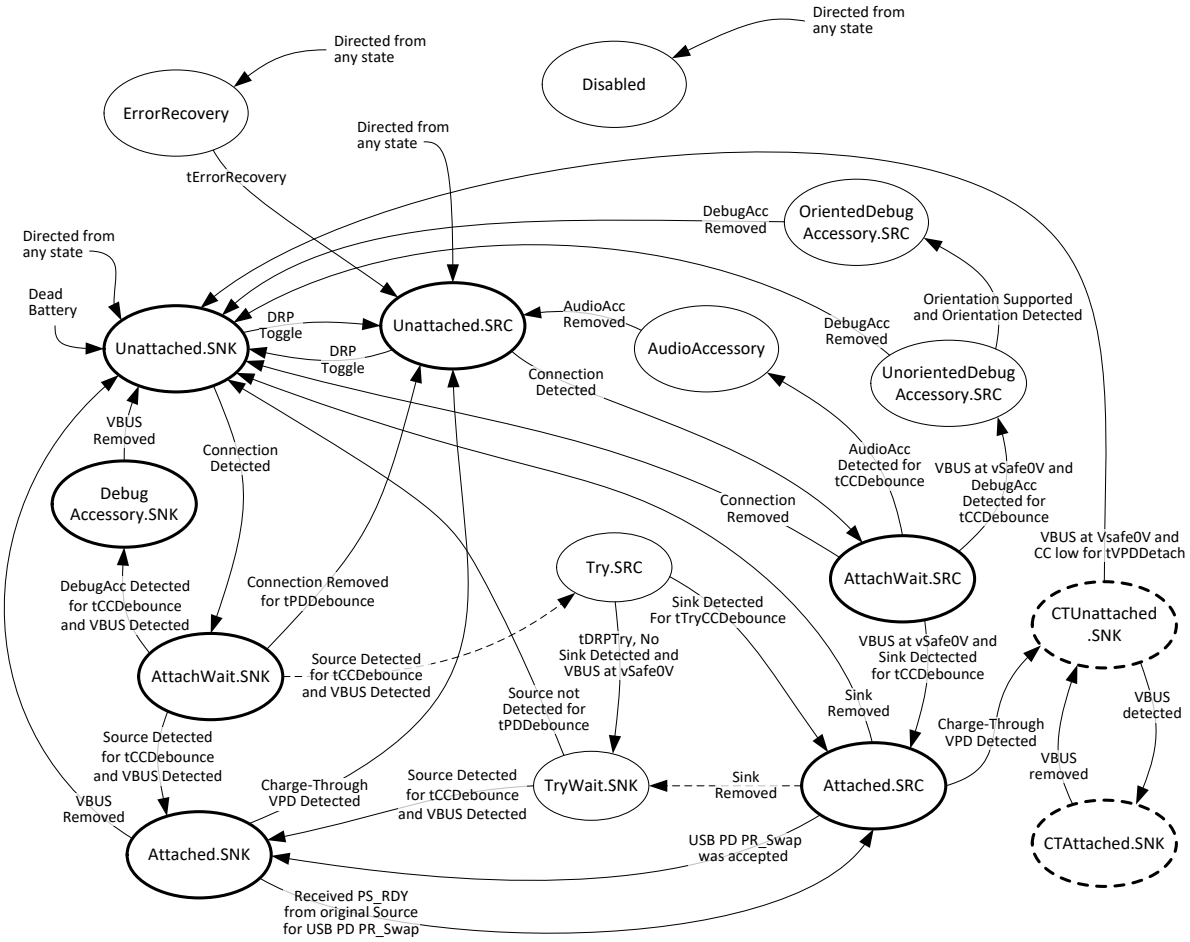
图 4-15 连接状态图：DRP



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-16 illustrates a connection state diagram for a DRP that supports Try.SRC and Accessory Modes.

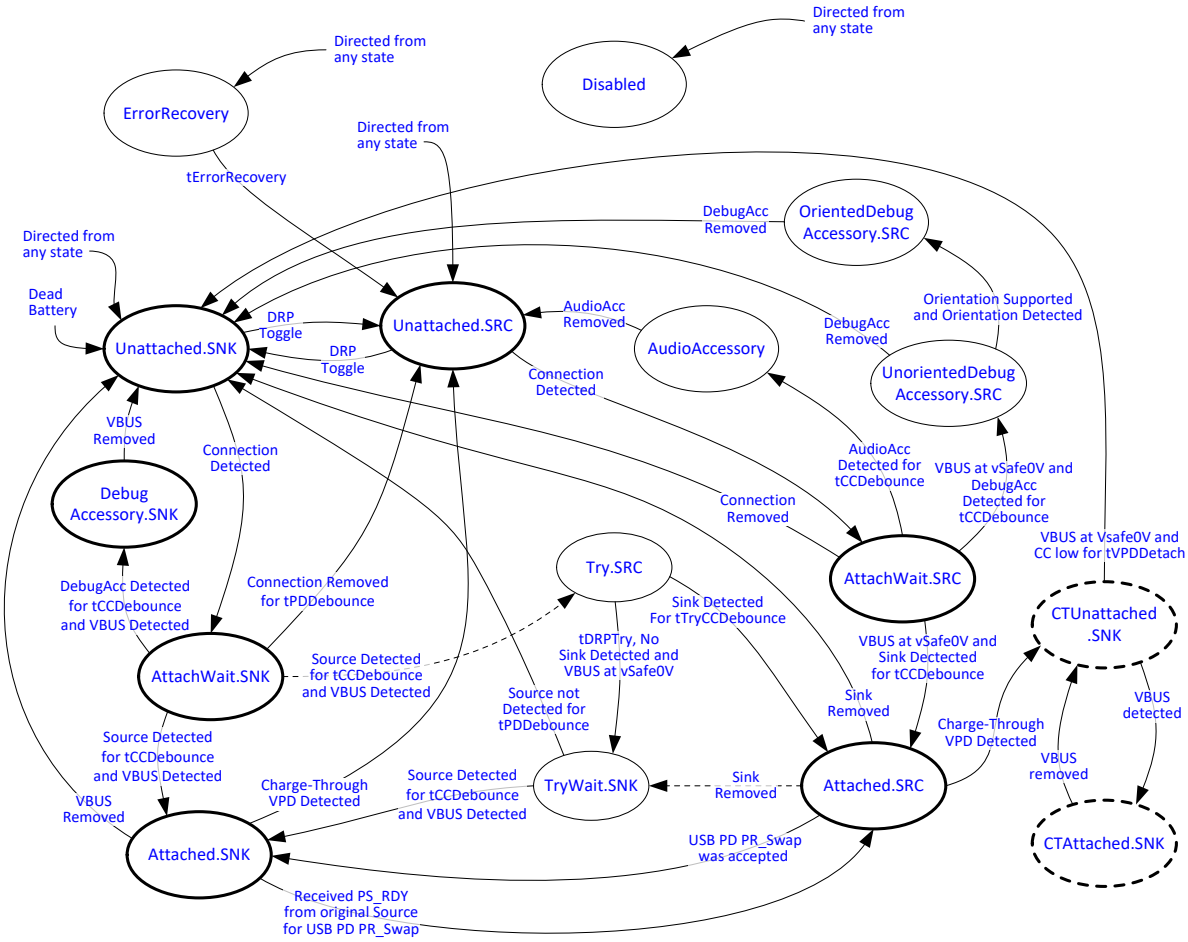
Figure 4-16 Connection State Diagram: DRP with Accessory and Try.SRC Support



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-16 说明了支持 Try.SRC 和附件模式的 DRP 的连接状态图。

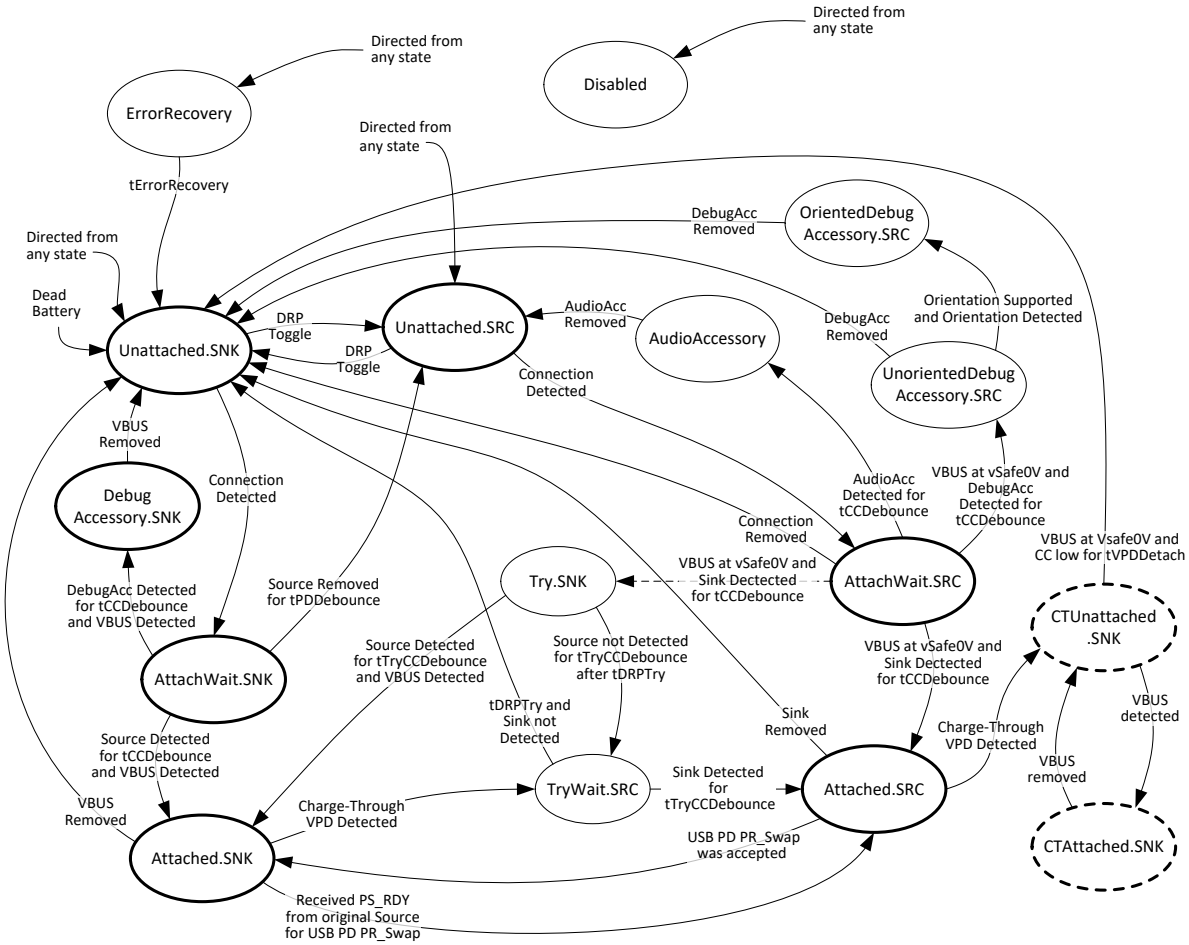
图 4-16 连接状态图：带附件和 Try.SRC 支持的 DRP



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-17 illustrates a connection state diagram for a DRP that supports Try.SNK and Accessory Modes.

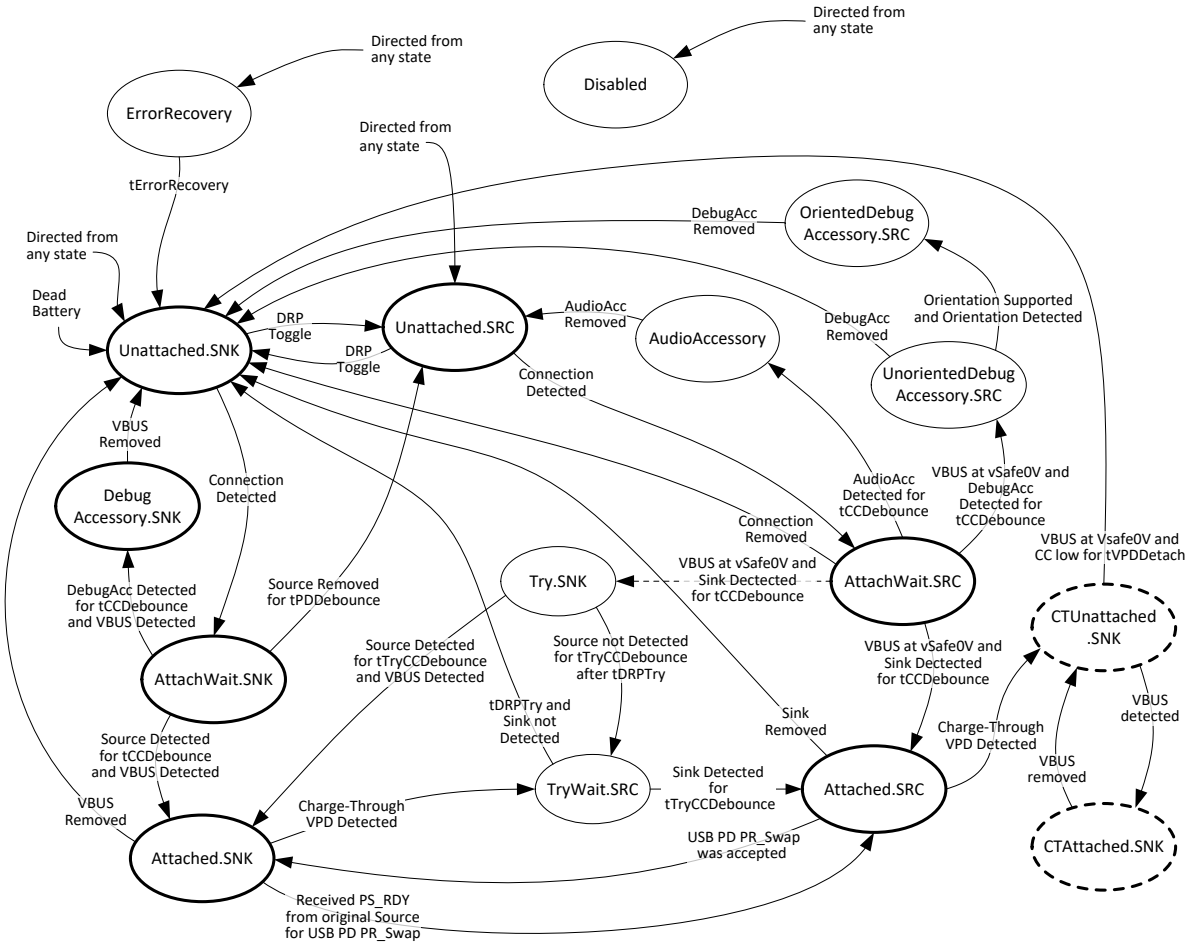
Figure 4-17 Connection State Diagram: DRP with Accessory and Try.SNK Support



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-17 说明了支持 Try.SNK 和配件模式的 DRP 的连接状态图。

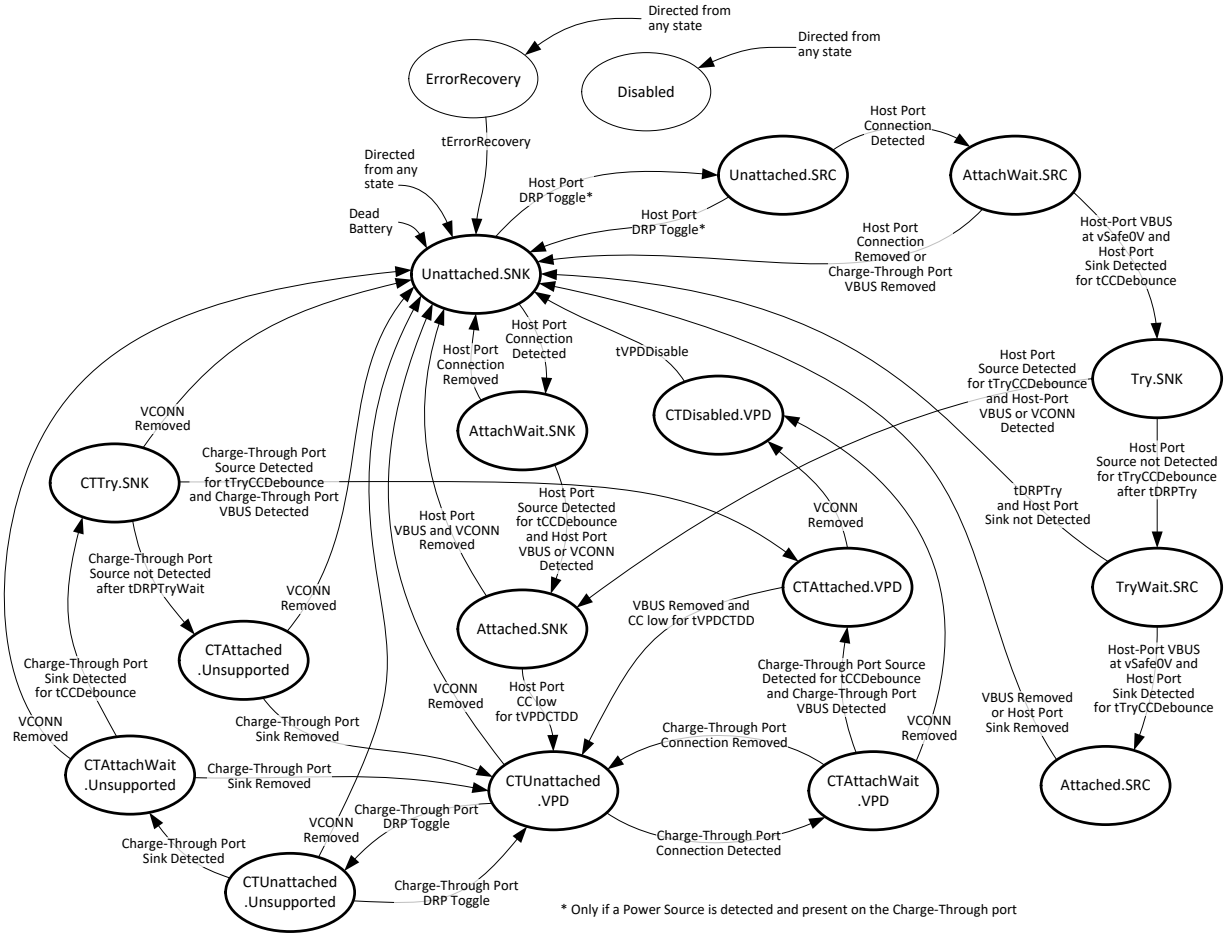
图 4-17 连接状态图：带附件和 Try.SNK 支持的 DRP



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-18 illustrates a connection state diagram for a Charge-Through VCONN-Powered USB Device.

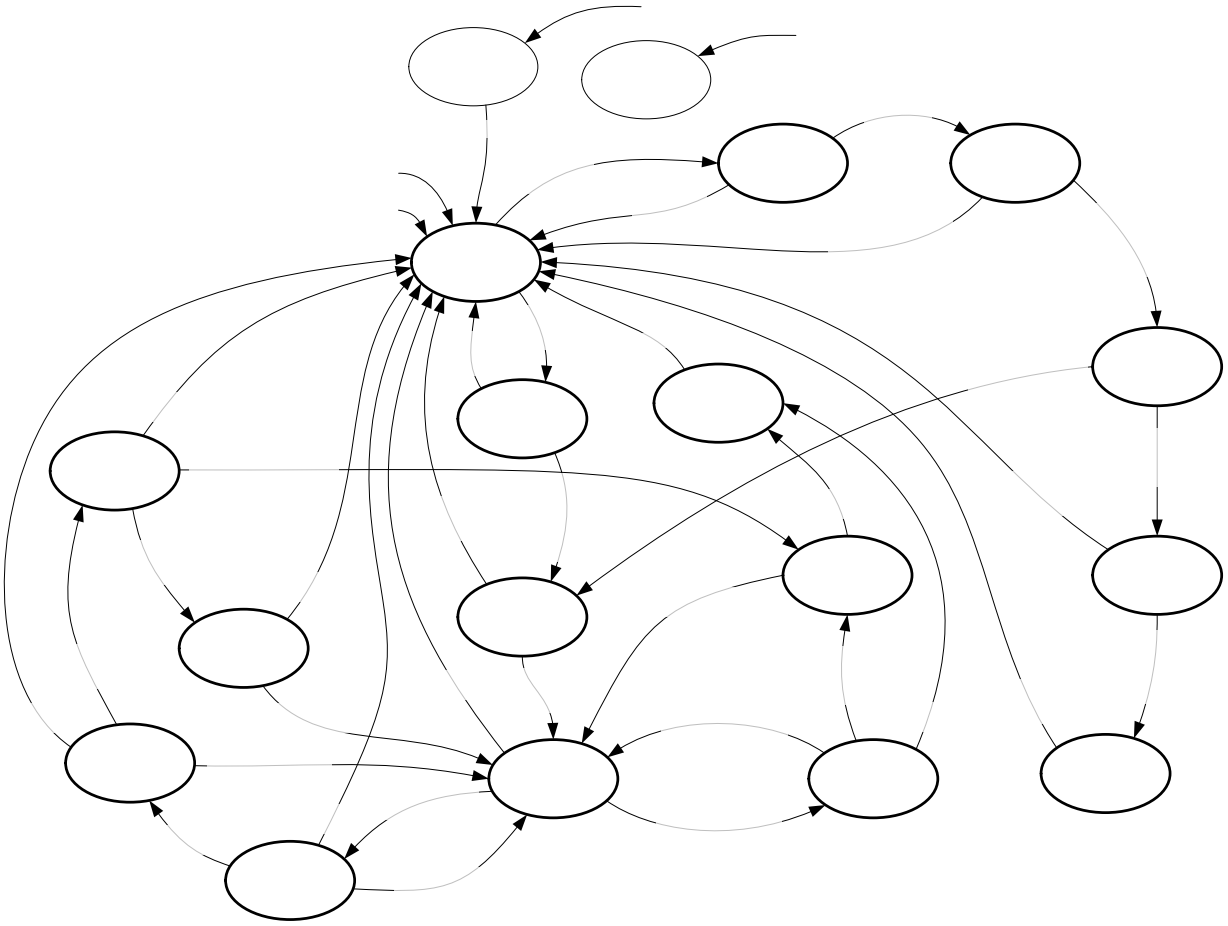
Figure 4-18 Connection State Diagram: Charge-Through VPD



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-18 说明了通过 VCONN 充电的 USB 设备的连接状态图。

图 4-18 连接状态图：充电直通 VPD



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2 Connection State Machine Requirements

Entry into any unattached state when "directed from any state" shall not be used to override tDRP toggle.

A DRP or a Sink may consume default power from VBUS in any state where it is not required to provide VBUS.

The following two tables define the electrical states for a CC pin in both a Source and a Sink. Every port has CC1 and CC2 pins, each with its own individual CC pin state. The combination of a port's CC1 and CC2 pin states are be used to define the conditions under which a port transitions from one state to another.

Table 4-14 Source Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rp
SRC.Open	**Open, Rp**	Above vOPEN
SRC.Rd	**Rd**	Within the vRd range (i.e., between minimum vRd and maximum vRd)
SRC.Ra	**Ra**	Below maximum vRa

Table 4-15 Sink Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rd
SNK.Rp	**Rp**	Above minimum vRd-Connect
SNK.Open	**Open, Ra, Rd**	Below maximum vRa

4.5.2.2.1 Disabled State

This state appears in Figure 4-12, Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16 and Figure 4-17.

The Disabled state is where the port prevents connection from occurring by removing all terminations from the CC pins.

The port should transition to the Disabled state from any other state when directed. When the port transitions to the Disabled state from Attached.SNK, it shall keep all terminations on the CC pins removed for a minimum of tErrorRecovery.

A port may choose not to support the Disabled state. If the Disabled state is not supported, the port shall be directed to either the Unattached.SNK or Unattached.SRC states after power-on.

4.5.2.2.1.1 Disabled State Requirements

The port shall not drive VBUS or VCONN, and shall present a high-impedance to ground (above zOPEN) on its CC1 and CC2 pins.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2 连接状态机要求

当“从任何状态指示”时，进入任何未附加状态不得用于覆盖 tDRP 切换。

在任何不需要提供 VBUS 的状态下，DRP 或 Sink 都可以消耗来自 VBUS 的默认电源。

以下两个表定义了源和接收器中 CC 引脚的电气状态。每个端口都有 CC1 和 CC2 引脚，每个引脚都有各自的 CC 引脚状态。端口的 CC1 和 CC2 引脚状态组合可用于定义端口从一种状态转换为另一种状态的条件。

表 4-14 源端口 CC 引脚状态

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rp
SRC.Open	**Open, Rp**	Above vOPEN
SRC.Rd	**Rd**	Within the vRd range (i.e., between minimum vRd and maximum vRd)
SRC.Ra	**Ra**	Below maximum vRa

表 4-15 接收端口 CC 引脚状态

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rd
SNK.Rp	**Rp**	Above minimum vRd-Connect
SNK.Open	**Open, Ra, Rd**	Below maximum vRa

4.5.2.2.1 禁用状态

该状态出现在图4-12、图4-13、图4-14、图4-15、图4-16和图4-17中。

在禁用状态下，端口通过移除 CC 引脚上的所有终端来阻止连接。

端口应在收到指示后从任何其他状态转换为禁用状态。当端口从 Attached.SNK 转换为禁用状态时，它应保持 CC 引脚上的所有终端被移除，持续时间至少为 tErrorRecovery。

端口可以选择不支持Disabled状态。如果不支持Disabled状态，则端口在通电后应定向到Unattached.SNK或Unattached.SRC状态。

4.5.2.2.1.1 残疾人士状态要求

该端口不得驱动 VBUS 或 VCONN，并且应在其 CC1 和 CC2 引脚上呈现对地高阻抗（高于 zOPEN）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.1.2 Exiting From Disabled State

A Sink shall transition to Unattached.SNK when directed.

A Source shall transition to Unattached.SRC when directed.

A DRP shall transition to either Unattached.SNK or Unattached.SRC when directed.

4.5.2.2.2 ErrorRecovery State

This state appears in Figure 4-12, Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16 and Figure 4-17.

The ErrorRecovery state is where the port removes the terminations from the CC1 and CC2 pins for tErrorRecovery followed by transitioning to the appropriate Unattached.SNK or Unattached.SRC state based on port type. This is the equivalent of forcing a detach event and looking for a new attach.

The port should transition to the ErrorRecovery state from any other state when directed.

A port may choose not to support the ErrorRecovery state. If the ErrorRecovery state is not supported, the port shall be directed to the Disabled state if supported. If the Disabled state is not supported, the port shall be directed to either the Unattached.SNK or Unattached.SRC states.

4.5.2.2.2.1 ErrorRecovery State Requirements

The port shall not drive VBUS or VCONN, and shall present a high-impedance to ground (above zOPEN) on its CC1 and CC2 pins.

4.5.2.2.2.2 Exiting From ErrorRecovery State

A Sink shall transition to Unattached.SNK after tErrorRecovery.

A Source shall transition to Unattached.SRC after tErrorRecovery.

A DRP (Figure 4-15) and a DRP with Accessory and Try.SNK Support (Figure 4-17) shall transition to Unattached.SNK after tErrorRecovery.

A DRP with Accessory and Try.SRC Support (Figure 4-16) shall transition to Unattached.SRC after tErrorRecovery.

4.5.2.2.3 Unattached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the Unattached.SNK state, the port is waiting to detect the presence of a Source.

A port with a dead battery shall enter this state while unpowered.

4.5.2.2.3.1 Unattached.SNK Requirements

The port shall not drive VBUS or VCONN.

Both CC1 and CC2 pins shall be independently terminated to ground through Rd.

A Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS, and independently terminate its Charge-Through port's CC1 and CC2 pins and Host-side port's CC pin to ground through Rd.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.1.2 退出禁用状态

当收到指示时，Sink 应当转换至 Unattached.SNK。

一当直接 特德。

当收到指示时，DRP 应转换至 Unattached.SNK 或 Unattached.SRC。

4.5.2.2.2 错误恢复状态

该状态出现在图4-12、图4-13、图4-14、图4-15、图4-16和图4-17中。

在 ErrorRecovery 状态下，端口会移除 CC1 和 CC2 引脚的终端，并根据端口类型转换到相应的 Unattached.SNK 或 Unattached.SRC 状态。这相当于强制断开连接事件并寻找新的连接。

当收到指示时，端口应该从任何其他状态转换到 ErrorRecovery 状态。

端口可以选择不支持 ErrorRecovery 状态。如果不支持 ErrorRecovery 状态，则端口应定向到 Disabled 状态（如果支持）。如果不支持 Disabled 状态，则端口应定向到 Unattached.SNK 或 Unattached.SRC 状态。

4.5.2.2.2.1 错误恢复状态要求

该端口不得驱动 VBUS 或 VCONN，并且应在其 CC1 和 CC2 引脚上呈现对地高阻抗（高于 zOPEN）。

4.5.2.2.2.2 退出错误恢复状态

tErrorRecovery 之后，Sink 应转换至 Unattached.SNK。

tErrorRecovery 之后，源应转换到 Unattached.SRC。

DRP（图 4-15）和具有附件和 Try.SNK 支持的 DRP（图 4-17）应在 tErrorRecovery 之后转换为 Unattached.SNK。

具有附件和 Try.SRC 支持的 DRP（图 4-16）应在 tErrorRecovery 之后转换到 Unattached.SRC。

4.5.2.2.3 未附加的.SNK 状态

该状态出现在图4-13、图4-14、图4-15、图4-16、图4-17和图4-18中。

当处于 Unattached.SNK 状态时，端口正在等待检测源的存在。

电池没电的端口在无电源的情况下应进入此状态。

4.5.2.2.3.1 未附加的.SNK 要求

该端口不得驱动VBUS或VCONN。

CC1 和 C C2 引脚应独立接地 通过路

通过 VCONN 充电的 USB 设备应将其主机侧端口与其通过充电端口（包括 CC 和 VBUS）隔离，并通过 Rd 独立地终止其通过充电端口的 CC1 和 CC2 引脚以及主机侧端口的 CC 引脚到地。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.3.2 Exiting from Unattached.SNK State

If the port supports *USB PD* or accessories, the port shall transition to AttachWait.SNK when the SNK.Rp state is present on at least one of its CC pins.

The maximum times that a Port shall take to transition to AttachWait.SNK are the following:

- tNoToggleConnect when neither Port Partner is toggling
- tOnePortToggleConnect when one Port Partner only is toggling

When both Port Partners are toggling, a Port should transition to AttachWait.SNK within tTwoPortToggleConnect. Note that when both Port Partners are DRPs it is indeterminate whether the local port will transition to AttachWait.SRC or AttachWait.SNK.

Note: The times tOnePortToggleConnect and tTwoPortToggleConnect relate to how long toggling ports may take to sync and detect a connection.

A *USB 2.0* only Sink that doesn't support accessories and is self-powered or requires only default power and does not support *USB PD* may transition directly to Attached.SNK when VBUS is detected.

A DRP shall transition to Unattached.SRC within tDRPTransition after the state of both CC pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.

A Sink with Accessory support shall transition to Unattached.Accessory within tDRPTransition after the state of both the CC1 and CC2 pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.

A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SRC within tDRPTransition after the state of the Host-side port's CC pin is SNK.Open for tDRP – dcSRC.DRP · tDRP and both of the following is detected on the Charge-Through port.

- SNK.Rp state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce
- VBUS is detected

A Charge-Through VCONN-Powered USB Device shall transition to Attached.SNK when a Source connection is detected, as indicated by the SNK.Rp state on its Host-side port's CC pin.

4.5.2.2.4 AttachWait.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the AttachWait.SNK state, the port has detected the SNK.Rp state on at least one of its CC pins and is waiting for VBUS.

When in the AttachWait.SNK state, the Charge-Through VCONN-Powered USB Device has detected the SNK.Rp state on its Host-side port's CC pin and is waiting for host-side VBUS.

4.5.2.2.4.1 AttachWait.SNK Requirements

The port shall not drive VBUS or VCONN.

Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.3.2 退出未连接的.SNK 状态

如果端口支持 *USB PD* 或附件，则当至少一个 CC 引脚上存在 SNK.Rp 状态时，端口应转换到 AttachWait.SNK。

端口转换到 AttachWait.SNK 的最大时间如下：

- tNoToggleConnect 当两个端口伙伴均未切换时 • tOnePortToggleConnect 当只有一个端口伙伴切换时

当两个端口伙伴都在切换时，端口应在 tTwoPortToggleConnect 内转换为 AttachWait.SNK。请注意，当两个端口伙伴都是 DRP 时，本地端口是否将转换为 AttachWait.SRC 或 AttachWait.SNK 尚不确定。

注意：tOnePortToggleConnect 和 tTwoPortToggleConnect 的时间与切换端口同步和检测连接所需的时间有关。

仅有 *USB 2.0* 的 Sink 不支持配件并且自供电或者只需要默认电源并且不支持 *USB PD*，当检测到 VBUS 时，可能会直接转换到 Attached.SNK。

在两个 CC 引脚的状态均为 tDRP – dcSRC.DRP · tDRP 的 SNK.Open 之后，或者如果得到指示，DRP 应在 tDRPTransition 内转换到 Unattached.SRC。

在 CC1 和 CC2 引脚的状态均为 tDRP – dcSRC.DRP · tDRP 的 SNK.Open 之后，或者如果指示，具有附件支持的接收器应在 tDRPTransition 内转换为 Unattached.Accessory。

主机端端口的 CC 引脚状态为 SNK.Open，持续时间为 tDRP – dcSRC.DRP · tDRP，并且在直通充电端口上检测到以下两种情况后，直通充电 VCONN 供电 USB 设备应在 tDRPTransition 内转换为 Unattached.SRC。

在至少 tCCDebounce 时间内，在 CC1 或 CC2 引脚之一上检测到 • SNK.Rp 状态

当检测到源连接时，通过 VCONN 充电的 USB 设备将转换为 Attached.SNK，如其主机侧端口的 CC 引脚上的 SNK.Rp 状态所示。

4.5.2.2.4 AttachWait.SNK 状态

该状态出现在图4-13、图4-14、图4-15、图4-16、图4-17和图4-18中。

当处于 AttachWait.SNK 状态时，端口已在其至少一个 CC 引脚上检测到 SNK.Rp 状态，并且正在等待 VBUS。

当处于 AttachWait.SNK 状态时，通过 VCONN 充电的 USB 设备已检测到其主机侧端口的 CC 引脚上的 SNK.Rp 状态，并正在等待主机侧 VBUS。

4.5.2.2.4.1 AttachWait.SNK 要求

该端口不得驱动VBUS或VCONN。

CC1 和 CC2 引脚均应通过 Rd 独立接地。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS, and independently terminate its Charge-Through port's CC1 and CC2 pins and Host-side port's CC pin to ground through Rd.

It is strongly recommended that a USB 3.2 SuperSpeed device hold off VBUS detection to the device controller until the Attached.SNK state or the DebugAccessory.SNK state is reached, i.e. at least one CC pin is in the SNK.Rp state. Otherwise, it may connect as *USB 2.0* when attached to a legacy host or hub's DFP.

4.5.2.2.4.2 Exiting from AttachWait.SNK State

A Sink shall transition to Unattached.SNK when the state of both the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.

A DRP shall transition to Unattached.SRC when the state of both the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.

The port shall transition to Attached.SNK after the state of only one of the CC1 or CC2 pins is SNK.Rp for at least tCCDebounce and VBUS is detected. Note the Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on one of the CC pins with the state of the other CC pin remaining SNK.Open, but this event will not exceed tPDDebounce.

If the port is a VCONN-Powered Accessory or a VCONN-Powered USB Device, the port shall transition to Attached.SNK when either VCONN or VBUS is detected. The port may transition without waiting tCCDebounce on CC.

If the port supports Debug Accessory Mode, the port shall transition to DebugAccessory.SNK if the state of both the CC1 and CC2 pins is SNK.Rp for at least tCCDebounce and VBUS is detected. Note the DAM Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on one of the CC pins with the state of the other CC pin remaining SNK.Rp, but this event will not exceed tPDDebounce.

A Charge-Through VCONN-Powered USB Device shall transition to Attached.SNK after the state of the Host-side port's CC pin is SNK.Rp for at least tCCDebounce and either host-side VCONN or VBUS is detected.

A DRP that strongly prefers the Source role may optionally transition to Try.SRC instead of Attached.SNK when the state of only one CC pin has been SNK.Rp for at least tCCDebounce and VBUS is detected.

4.5.2.2.5 Attached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the Attached.SNK state, the port is attached and operating as a Sink. When the port initially enters this state it is also operating as a UFP. The power and data roles can be changed using *USB PD* commands.

A port that entered this state directly from Unattached.SNK due to detecting VBUS shall not determine orientation or availability of higher than Default USB Power and shall not use *USB PD*.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

通过 VCONN 充电的 USB 设备应将其主机侧端口与其通过充电端口（包括 CC 和 VBUS）隔离，并通过 Rd 独立地终止其通过充电端口的 CC1 和 CC2 引脚以及主机侧端口的 CC 引脚到地。

强烈建议 USB 3.2 SuperSpeed 设备推迟对设备控制器的 VBUS 检测，直到达到 Attached.SNK 状态或 DebugAccessory.SNK 状态，即至少一个 CC 引脚处于 SNK.Rp 状态。否则，当连接到旧式主机或集线器的 DFP 时，它可能以 *USB 2.0* 连接。

4.5.2.2.4.2 退出 AttachWait.SNK 状态

当 CC1 和 CC2 引脚的状态均为 SNK.Open 且持续至少 tPDDebounce 时，Sink 应转换至 Unattached.SNK。

当 CC1 和 CC2 引脚的状态均为 SNK.Open 且持续至少 tPDDebounce 时，DRP 应转换至 Unattached.SRC。

当 CC1 或 CC2 引脚中只有一个处于 SNK.Rp 状态且至少持续 tCCDebounce 时间并检测到 VBUS 时，端口应转换为 Attached.SNK。请注意，源可能会启动 *USB PD* 通信，这将导致其中一个 CC 引脚短暂处于 SNK.Open 状态，而另一个 CC 引脚的状态仍为 SNK.Open，但此事件不会超过 tPDDebounce。

如果端口是 VCONN 供电的配件或 VCONN 供电的 USB 设备，则当检测到 VCONN 或 VBUS 时，端口应转换为 Attached.SNK。端口可以转换，而无需等待 CC 上的 tCCDebounce。

如果端口支持调试附件模式，则如果 CC1 和 CC2 引脚的状态均为 SNK.Rp 且至少持续 tCCDebounce 且检测到 VBUS，则端口应转换为 DebugAccessory.SNK。请注意，DAM 源可能会启动 *USB PD* 通信，这将导致其中一个 CC 引脚上的 SNK.Open 状态短暂存在，而另一个 CC 引脚的状态仍为 SNK.Rp，但此事件不会超过 tPDDebounce。

在主机端端口的 CC 引脚状态为 SNK.Rp 至少持续 tCCDebounce 并且检测到主机端 VCONN 或 VBUS 后，通过 VCONN 充电供电的 USB 设备应转换为 Attached.SNK。

当只有一个 CC 引脚的状态为 SNK.Rp 至少 tCCDebounce 并且检测到 VBUS 时，强烈倾向于源角色的 DRP 可以选择转换为 Try.SRC 而不是 Attached.SNK。

4.5.2.2.5 Attached.SNK 状态

该状态出现在图4-13、图4-14、图4-15、图4-16、图4-17和图4-18中。

当处于 Attached.SNK 状态时，端口已连接并作为接收器运行。当端口最初进入此状态时，它还作为 UFP 运行。可以使用 *USB PD* 命令更改电源和数据角色。

由于检测 VBUS 而直接从 Unattached.SNK 进入此状态的端口不得确定方向或高于默认 USB 电源的可用性，并且不得使用 *USB PD*。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.5.1 Attached.SNK Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to this state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the SNK.Rp state).

If the port supports signaling on SuperSpeed USB pairs, it shall functionally connect the SuperSpeed USB pairs and maintain the connection during and after a *USB PD* PR_Swap.

If the port has entered the Attached.SNK state from the AttachWait.SNK or TryWait.SNK states, only one the CC1 or CC2 pins will be in the SNK.Rp state. The port shall continue to terminate this CC pin to ground through Rd.

If the port has entered the Attached.SNK state from the Attached.SRC state following a *USB PD* PR_Swap, the port shall terminate the connected CC pin to ground through Rd.

The port shall meet the Sink Power Sub-State requirements specified in Section 4.5.2.2.22.

If the port is a VCONN-Powered USB Device, it shall respond to *USB PD* cable identity queries on SOP'. It shall not send or respond to messages on SOP. It shall ensure there is sufficient capacitance on CC to meet cReceiver as defined in *USB PD*.

A Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS, present a high-impedance to ground (above zOPEN) on its Charge-Through port's CC1 and CC2 pins and terminate its Host-side port's CC pin to ground through Rd.

A Charge-Through VCONN-Powered USB Device shall start a Charge-Through Support Timer when it enters the Attached.SNK state. If a Charge-Through VCONN-Powered USB Device fails to exit the Attached.SNK state before the Charge-Through Support Timer exceeds tAMETimeout, it shall present a USB Billboard Device Class interface indicating that it does not support Charge-Through.

A Charge-Through VCONN-Powered USB Device shall reset the Charge-Through Support Timer when it first receives any *USB PD* Structured VDM Command it supports. If a Charge-Through VCONN-Powered USB Device receives a Structured VDM Command multiple times, it shall only reset the Charge-Through Support Timer once. This ensures a Charge-Through VCONN-Powered USB Device will present a USB Billboard Device Class interface if it fails to exit Attached.SNK while receiving repeated or continuous Structured VDM Commands (e.g., Discover Identity).

A Charge-Through VCONN-Powered USB Device shall reset the Charge-Through Support Timer when it receives any Data Message it supports. A Charge-Through VCONN-Powered USB Device shall hold the Charge-Through Support Timer in reset while it is in any *USB PD* BIST mode.

Except for a VCONN-Powered USB Device or Charge-Through VCONN-Powered USB Device, the port may negotiate a *USB PD* PR_Swap, DR_Swap or VCONN_Swap.

If the port supports Charge-Through VCONN-Powered USB Device, and an explicit *USB PD* contract has failed to be negotiated, the port shall query the identity of the cable via *USB PD* on SOP'.

By default, upon entry from AttachWait.SNK or Unattached.SNK, VCONN shall not be supplied in the Attached.SNK state. If Attached.SNK is entered from Attached.SRC as a result of a *USB PD* PR_Swap, it shall maintain VCONN supply state, whether on or off, and its data role/connections. A *USB PD* DR_Swap has no effect on which port sources VCONN.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.5.1 Attached.SNK 要求

如果端口需要确定连接器的方向，则它应仅在进入此状态时通过检测哪个 CC1 或 CC2 引脚通过电缆连接（即处于 SNK.Rp 状态的 CC 引脚）来执行此操作。

如果端口支持超高速 USB 对上的信号传输，则它应在功能上连接超高速 USB 对，并在 *USB PD* PR_Swap 期间和之后保持连接。

如果端口已从 AttachWait.SNK 或 TryWait.SNK 状态进入 Attached.SNK 状态，则 CC1 或 CC2 引脚中只有一个将处于 SNK.Rp 状态。端口应继续通过 Rd 将此 CC 引脚终止于地。

如果端口在 *USB PD* PR_Swap 之后从 Attached.SRC 状态进入 Attached.SNK 状态，则端口应通过 Rd 将连接的 CC 引脚终止于地。

该端口应满足第 4.5.2.2.22 节规定的 Sink Power Sub-State 要求。

如果端口是 VCONN 供电的 USB 设备，它应响应 SOP ’ 上的 *USB PD* 电缆身份查询。它不得发送或响应 SOP 上的消息。它应确保 CC 上有足够的电容来满足 *USB PD* 中定义的 cReceiver。

通过 VCONN 充电的 USB 设备应将其主机侧端口与其通过充电端口隔离，包括 CC 和 VBUS，在其通过充电端口的 CC1 和 CC2 引脚上呈现对地高阻抗（高于 zOPEN），并通过 Rd 将其主机侧端口的 CC 引脚终止于地。

充电直通 VCONN 供电 USB 设备在进入 Attached.SNK 状态时应启动充电直通支持计时器。如果充电直通 VCONN 供电 USB 设备发生故障
在 Charge-Through 支持计时器超过 tAMETimeout 之前退出 Attached.SNK 状态，它应呈现一个 USB Billboard 设备类接口，表明它不支持 Charge-Through。

通过 VCONN 充电的 USB 设备在首次收到其支持的任何 *USB PD* 结构化 VDM 命令时应重置通过 VCONN 充电支持计时器。如果通过 VCONN 充电的 USB 设备多次收到结构化 VDM 命令，则应仅重置一次通过 VCONN 充电支持计时器。这可确保通过 VCONN 充电的 USB 设备在收到重复或连续的结构化 VDM 命令（例如发现身份）时无法退出 Attached.SNK，则将显示 USB Billboard 设备类界面。

当通过 VCONN 充电的 USB 设备接收到其支持的任何数据消息时，应重置通过 VCONN 充电的支持计时器。当通过 VCONN 充电的 USB 设备处于任何 *USB PD* BIST 模式时，应保持通过 VCONN 充电的支持计时器处于重置状态。

除 VCONN 供电的 USB 设备或通过 VCONN 充电的 USB 设备外，
端口可以协商 *USB PD* PR_Swap、DR_Swap 或 VCONN_Swap。

如果端口支持通过 VCONN 供电的 USB 设备充电，并且明确的 *USB PD* 合同未能协商，则端口应通过 SOP ’ 上的 *USB PD* 查询电缆的身份。

默认情况下，从 AttachWait.SNK 或 Unattached.SNK 进入时，VCONN 不得在 Attached.SNK 状态下供应。如果由于 *USB PD* PR_Swap 从 Attached.SRC 进入 Attached.SNK，则它应保持 VCONN 供应状态（无论开启还是关闭）及其数据角色/连接。*USB PD* DR_Swap 对哪些端口源 VCONN 没有影响。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The port may negotiate a *USB PD* VCONN_Swap. When the port successfully executes *USB PD* VCONN_Swap operation and was not sourcing VCONN, it shall start sourcing VCONN within tVCONNON. The port shall execute the VCONN_Swap in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes *USB PD* VCONN_Swap operation and was sourcing VCONN, it shall stop sourcing VCONN within tVCONNOFF.

4.5.2.2.5.2 Exiting from Attached.SNK State

A port that is not a VCONN-Powered USB Device and is not in the process of a *USB PD* PR_Swap or a *USB PD* Hard Reset or a *USB PD* FR_Swap shall transition to Unattached.SNK within tSinkDisconnect when VBUS falls below vSinkDisconnect for VBUS operating at or below 5 V or below vSinkDisconnectPD when negotiated by *USB PD* to operate above 5 V.

A VCONN-Powered USB Device shall return to Unattached.SNK when VBUS has fallen below vSinkDisconnect and VCONN has fallen below vVCONNDisconnect.

A port that has entered into *USB PD* communications with the Source and has seen the CC voltage exceed vRd-USB may monitor the CC pin to detect cable disconnect in addition to monitoring VBUS.

A port that is monitoring the CC voltage for disconnect (but is not in the process of a *USB PD* PR_Swap or *USB PD* FR_Swap) shall transition to Unattached.SNK within tSinkDisconnect after the CC voltage remains below vRd-USB for tPDDebounce.

If supplying VCONN, the port shall cease to supply it within tVCONNOFF of exiting Attached.SNK.

A Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD if VCONN is present and the state of its Host-side port's CC pin is SNK.Open for tVPDCTDD.

A port that via SOP' has detected an attached Charge-Through VCONN-Powered USB Device shall transition to TryWait.SRC if implemented, or transition to Unattached.SRC or Unattached.Accessory if TryWait.SRC is not supported. This transition may be delayed until the device has sufficient battery charge needed to remain powered until it reaches the CTAttached.SNK state.

After receiving a *USB PD* PS_RDY from the original Source during a *USB PD* PR_Swap, the port shall transition directly to the Attached.SRC state (i.e., remove Rd from CC, assert Rp on CC and supply VBUS), but shall maintain its VCONN supply state, whether off or on, and its data role/connections.

4.5.2.2.6 UnattachedWait.SRC State

This state appears in Figure 4-12.

When in the UnattachedWait.SRC state, the port is discharging the CC pin that was providing VCONN in the previous Attached.SRC state.

4.5.2.2.6.1 UnattachedWait.SRC Requirements

The port shall not enable VBUS or VCONN.

The port shall complete the VCONN turn off initiated when leaving the previous Attached.SRC state.

The port shall continue to provide an Rp termination, as specified in Table 4-24, on the CC pin not being discharged.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

端口可以协商 *USB PD* VCONN_Swap。当端口成功执行 *USB PD* VCONN_Swap 操作并且未提供 VCONN 时，它应在 tVCONNON 内开始提供 VCONN。端口应按照先接后断的顺序执行 VCONN_Swap，以保持活动的 USB Type-C 到 USB Type-C 电缆供电。当端口成功执行 *USB PD* VCONN_Swap 操作并且提供 VCONN 时，它应在 tVCONNOFF 内停止提供 VCONN。

4.5.2.2.5.2 退出 Attached.SNK 状态

如果端口不是 VCONN 供电的 USB 设备，并且未处于 *USB PD* PR_Swap 或 *USB PD* 硬重置或 *USB PD* FR_Swap 过程中，则当 VBUS 降至低于 vSinkDisconnect（对于在 5 V 或以下运行的 VBUS）或低于 vSinkDisconnectPD（当由 *USB PD* 协商为在 5 V 以上运行时）时，该端口应在 tSinkDisconnect 内转换为 Unattached.SNK。

当 VBUS 降至 vSinkDisconnect 以下且 VCONN 降至 vVCONNDisconnect 以下时，VCONN 供电的 USB 设备应返回到 Unattached.SNK。

已与源进入 *USB PD* 通信且发现 CC 电压超过 vRd-USB 的端口除了监控 VBUS 之外，还可以监控 CC 引脚以检测电缆断开连接。

监控 CC 电压是否断开（但不处于 *USB PD* PR_Swap 或 *USB PD* FR_Swap 过程中）的端口应在 CC 电压保持低于 vRd-USB 并持续 tPDDebounce 后，在 tSinkDisconnect 内转换为 Unattached.SNK。

如果提供 VCONN，则端口应在退出 Attached.SNK 后的 tVCONNOFF 时间内停止提供 VCONN。

如果 VCONN 存在且其主机端端口的 CC 引脚的状态为 SNK.Open，持续时间为 tVPDCTDD，则通过 VCONN 充电的供电 USB 设备应转换为 CTUnattached.VPD。

通过 SOP ’ 检测到连接的通过 VCONN 充电的 USB 设备的端口应转换为 TryWait.SRC（如果已实现），或转换为 Unattached.SRC 或 Unattached.Accessory（如果不支持 TryWait.SRC）。此转换可能会延迟，直到设备有足够的电池电量来保持供电，直到达到 CTAttached.SNK 状态。

在 *USB PD* PR_Swap 期间从原始源接收到 *USB PD* PS_RDY 后，端口应直接转换到 Attached.SRC 状态（即，从 CC 中移除 Rd、在 CC 上断言 Rp 并提供 VBUS），但应保持其 VCONN 供电状态（无论是关闭还是打开）及其数据角色/连接。

4.5.2.2.6 UnattachedWait.SRC 状态

此状态如图 4-12 所示。

当处于 UnattachedWait.SRC 状态时，端口正在放电在之前的 Attached.SRC 状态下提供 VCONN 的 CC 引脚。

4.5.2.2.6.1 UnattachedWait.SRC 要求

该端口不得启用VBUS或VCONN。

端口应完成在离开之前的 Attached.SRC 状态时启动的 VCONN 关闭。

当 CC 引脚未放电时，端口应继续提供如表 4-24 所示的 Rp 终端。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The port shall not provide an Rp termination on the CC pin being discharged.

The port shall provide an Rdch termination on the CC pin being discharged.

The port shall discharge the CC pin being discharged below vVCONNDischarge.

4.5.2.2.6.2 Exiting from UnattachedWait.SRC State

The port shall transition to Unattached.SRC when both VCONN is turned off and the CC pin is below vVCONNDischarge.

4.5.2.2.7 Unattached.SRC State

This state appears in Figure 4-12, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the Unattached.SRC state, the port is waiting to detect the presence of a Sink or an Accessory.

When in the Unattached.SRC state, the Charge-Through VCONN-Powered USB Device has detected a Source on its Charge-Through port and is independently monitoring its Host-side port to detect the presence of a Sink.

4.5.2.2.7.1 Unattached.SRC Requirements

The port shall not drive VBUS or VCONN.

The port shall source current on both the CC1 and CC2 pins independently.

The port shall provide a separate Rp termination on the CC1 and CC2 pins as specified in Table 4-24. Note: A Source with a captive cable or just a plug presents a single Rp termination on its CC pin (A5).

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VBUS from the Charge-Through port.

Upon entry into this state, the Charge-Through VCONN-Powered USB Device shall remove its Rd termination to ground on the Host-side port CC and provide an Rp termination instead advertising Default USB Power, as specified in Table 4-24, and continue to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through Rd.

4.5.2.2.7.2 Exiting from Unattached.SRC State

The port shall transition to AttachWait.SRC when:

- The SRC.Rd state is present on either the CC1 or CC2 pin or
- The SRC.Ra state is present on both the CC1 and CC2 pins.

The maximum times that a Port shall take to transition to AttachWait.SRC are the following:

- tNoToggleConnect when neither Port Partner is toggling
- tOnePortToggleConnect when one Port Partner only is toggling

When both Port Partners are toggling, a Port should transition to AttachWait.SRC within tTwoPortToggleConnect. Note that when both Port Partners are DRPs it is indeterminate whether the local port will transition to AttachWait.SRC or AttachWait.SNK.

Note: The times tOnePortToggleConnect and tTwoPortToggleConnect relate to how long toggling ports may take to sync and detect a connection.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

该端口不得在正在放电的 CC 引脚上提供 Rp 终端。
港口应当 在 CC 引脚上提供一个 Rdch 终端 攻击。

端口应将 CC 引脚放电至低于 vVCONNDischarge。

4.5.2.2.6.2 退出 UnattachedWait.SRC 状态

当 VCONN 都关闭并且 CC 引脚低于 vVCONNDischarge 时，端口应转换至 Unattached.SRC。

4.5.2.2.7 未附加的.SRC 状态

该状态出现在图4-12、图4-15、图4-16、图4-17和图4-18中。

当处于 Unattached.SRC 状态时，端口正在等待检测 Sink 或 Accessory 的存在。

当处于未连接 SRC 状态时，通过 VCONN 供电的充电 USB 设备已检测到其充电端口上的源，并正在独立监控其主机侧端口以检测接收器的存在。

4.5.2.2.7.1 未附加的.SRC 要求

该端口不得驱动VBUS或VCONN。

该端口应独立地在 CC1 和 CC2 引脚上提供电流。

端口应在 CC1 和 CC2 引脚上提供单独的 Rp 终端，如表 4-24 中所述。注意：带有固定电缆或仅带插头的源在其 CC 引脚 (A5) 上提供单个 Rp 终端。

通过 VCONN 充电的 USB 设备应将其主机端端口与其通过 VCONN 充电的端口隔离，包括 CC 和 VBUS。通过 VCONN 充电的 USB 设备应确保由通过 VCONN 充电的端口的 VBUS 供电。

进入此状态后，通过 VCONN 供电的充电式 USB 设备应移除主机侧端口 CC 上其至地的 Rd 终端，并提供 Rp 终端来代替通告默认 USB 电源，如表 4-24 所示，并继续通过 Rd 独立地将其充电式端口的 CC1 和 CC2 引脚接地。

4.5.2.2.7.2 退出 Unattached.SRC 状态

当出现以下情况时，端口应转换到 AttachWait.SRC：

- SRC.Rd 状态出现在 CC1 或 CC2 引脚上，或者
- SRC.Ra 状态存在于 CC1 和 CC2 引脚上。

最大t 端口转换到 AttachWait 状态所需的时间 .SRC 如下：

- tNoToggleConnect 当两个端口伙伴均未切换时 • tOnePortToggleConnect 当只有一个端口伙伴切换时

当两个端口伙伴都在切换时，端口应在 tTwoPortToggleConnect 内转换为 AttachWait.SRC。请注意，当两个端口伙伴都是 DRP 时，本地端口是否转换为 AttachWait.SRC 或 AttachWait.SNK 尚不确定。

注意：tOnePortToggleConnect 和 tTwoPortToggleConnect 的时间与切换端口同步和检测连接所需的时间有关。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Note: A cable without an attached device can be detected, when the SRC.Ra state is detected on one of the CC1 or CC2 pins and the other CC pin is SRC.Open. However in this case, the port shall not transition to AttachWait.SRC.

The Charge-Through VCONN-Powered USB Device shall transition to AttachWait.SRC when host-side VBUS is vSafe0V and SRC.Rd state is detected on the Host-side port's CC pin.

A DRP shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.

A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if Charge-Through VBUS is removed.

4.5.2.2.8 AttachWait.SRC State

This state appears in Figure 4-12, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

The AttachWait.SRC state is used to ensure that the state of both of the CC1 and CC2 pins is stable after a Sink is connected.

When in the AttachWait.SRC state, the Charge-Through VCONN-Powered USB Device ensures that the state of Host-side port's CC pin is stable after a Sink is connected.

4.5.2.2.8.1 AttachWait.SRC Requirements

The requirements for this state are identical to Unattached.SRC.

4.5.2.2.8.2 Exiting from AttachWait.SRC State

The port shall transition to Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to Try.SNK when the host-side VBUS is at vSafe0V and the SRC.Rd state is on the Host-side port's CC pin for at least tCCDebounce.

If the port supports Audio Adapter Accessory Mode, it shall transition to AudioAccessory when the SRC.Ra state is detected on both the CC1 and CC2 pins for at least tCCDebounce.

If the port supports Debug Accessory Mode, it shall transition to UnorientedDebugAccessory.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on both the CC1 and CC2 pins for at least tCCDebounce.

A Source shall transition to Unattached.SRC and a DRP to Unattached.SNK when the SRC.Open state is detected on both the CC1 and CC2 pins. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.

A Source shall transition to Unattached.SRC and a DRP to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin and the other CC pin is SRC.Ra. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.

A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK when the SRC.Open state is detected on the Host-side port's CC or if Charge-Through VBUS falls below vSinkDisconnect. The Charge-Through VCONN-Powered USB Device shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

注意：当在 CC1 或 CC2 引脚之一上检测到 SRC.Ra 状态且另一个 CC 引脚为 SRC.Open 时，可以检测到未连接设备的电缆。但是在这种情况下，端口不得转换为 AttachWait.SRC。

当主机端 VBUS 为 vSafe0V 并且在主机端端口的 CC 引脚上检测到 SRC.Rd 状态时，通过 VCONN 充电的 USB 设备应转换到 AttachWait.SRC。

在 dcSRC.DRP · tDRP 之后，或者在指示的情况下，DRP 应在 tDRPTransition 内转换为 Unattached.SNK。

通过 VCONN 充电的 USB 设备应在 dcSRC.DRP · tDRP 之后的 tDRPTransition 内转换到 Unattached.SNK，或者如果通过 VBUS 充电被移除。

4.5.2.2.8 AttachWait.SRC 状态

该状态出现在图4-12、图4-15、图4-16、图4-17和图4-18中。

AttachWait.SRC状态用于确保Sink连接后，CC1和CC2引脚的状态都稳定。

当处于 AttachWait.SRC 状态时，Charge-Through VCONN-Powered USB Device 可确保在 Sink 连接后，Host 侧端口的 CC 引脚状态稳定。

4.5.2.2.8.1 AttachWait.SRC 要求

此状态的要求与 Unattached.SRC 相同。

4.5.2.2.8.2 退出 AttachWait.SRC 状态

当 VBUS 处于 vSafe0V 并且在至少 tCCDebounce 的 CC1 或 CC2 引脚之一上检测到 SRC.Rd 状态时，端口应转换到 Attached.SRC。

当主机端 VBUS 处于 vSafe0V 并且主机端端口的 CC 引脚上存在 SRC.Rd 状态至少 tCCDebounce 时，通过 VCONN 充电供电的 USB 设备应转换到 Try.SNK。

如果端口支持音频适配器附件模式，则当在 CC1 和 CC2 引脚上检测到 SRC.Ra 状态至少 tCCDebounce 时，它应转换到音频附件。

如果端口支持调试附件模式，则当 VBUS 处于 vSafe0V 并且在 CC1 和 CC2 引脚上检测到 SRC.Rd 状态至少 tCCDebounce 时，它应转换到 UnientedDebugAccessory.SRC。

当在 CC1 和 CC2 引脚上检测到 SRC.Open 状态时，源应转换为 Unattached.SRC，DRP 应转换为 Unattached.SNK。源应在 tSRCDisconnect 内检测 SRC.Open 状态，但应尽快检测。

当在 CC1 或 CC2 引脚上检测到 SRC.Open 状态且另一个 CC 引脚为 SRC.Ra 时，源应转换为 Unattached.SRC，DRP 应转换为 Unattached.SNK。源应在 tSRCDisconnect 内检测 SRC.Open 状态，但应尽快检测。

当在主机端端口的 CC 上检测到 SRC.Open 状态或当 Charge-Through VBUS 低于 vSinkDisconnect 时，Charge-Through VCONN 供电 USB 设备应转换为 Unattached.SNK。Charge-Through VCONN 供电 USB 设备应在 tSRCDisconnect 内检测到 SRC.Open 状态，但应尽快检测到。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A DRP that strongly prefers the Sink role may optionally transition to Try.SNK instead of Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce.

4.5.2.2.9 Attached.SRC State

This state appears in Figure 4-12, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the Attached.SRC state, the port is attached and operating as a Source. When the port initially enters this state it is also operating as a DFP. Subsequently, the initial power and data roles can be changed using *USB PD* commands.

When in the Attached.SRC state, the Charge-Through VCONN-Powered USB Device has detected a Sink on its Host-side port and has connected the Charge-Through port VBUS to the Host-side port VBUS.

4.5.2.2.9.1 Attached.SRC Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to the Attached.SRC state by detecting which of the CC1 or CC2 pins is connected through the cable, i.e., which CC pin is in the SRC.Rd state.

If the port has entered this state from the AttachWait.SRC state or the Try.SRC state, the SRC.Rd state will be on only one of the CC1 or CC2 pins. The port shall source current on this CC pin and monitor its state.

If the port has entered this state from the Attached.SNK state as the result of a *USB PD* PR_Swap, the port shall source current on the connected CC pin and monitor its state.

The port shall provide an Rp as specified in Table 4-24.

The port shall supply VBUS current at the level it advertises on Rp.

The port shall supply VBUS within tVBUSON of entering this state, and for as long as it is operating as a power source.

The port shall not initiate any *USB PD* communications until VBUS reaches vSafe5V.

If the port supports signaling on SuperSpeed USB pairs, it shall:

- Functionally connect the SuperSpeed USB pairs
- For VCONN, do one of two things:
  - Supply VCONN unconditionally to the CC pin not in the SRC.Rd state, or
  - Supply VCONN to the CC pin in the SRC.Ra state.

A port that does not support signaling on SuperSpeed USB pairs may supply VCONN in the same manner described above.

The port may negotiate a *USB PD* PR_Swap, DR_Swap or VCONN_Swap.

If the port supplies VCONN, it shall do so within tVCONNON.

The port may query the identity of the cable via *USB PD* on SOP'. If it detects that it is connected to a VCONN-Powered USB Device, the port may remove VBUS and discharge it to vSafe0V, while continuing to remain in this state with VCONN applied. The port may also initiate other SOP' communication.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

当 VBUS 处于 vSafe0V 并且在至少 tCCDebounce 的时间内于 CC1 或 CC2 引脚之一上检测到 SRC.Rd 状态时，强烈倾向于 Sink 角色的 DRP 可以选择转换为 Try.SNK 而不是 Attached.SRC。

4.5.2.2.9 Attached.SRC 状态

该状态出现在图4-12、图4-15、图4-16、图4-17和图4-18中。

当处于 Attached.SRC 状态时，端口已连接并作为源运行。当端口最初进入此状态时，它还作为 DFP 运行。随后，可以使用 *USB PD* 命令更改初始电源和数据角色。

当处于 Attached.SRC 状态时，通过 VCONN 充电的 USB 设备已检测到其主机侧端口上的 Sink，并已将通过 VCONN 充电端口 VBUS 连接到主机侧端口 VBUS。

4.5.2.2.9.1 附件.SRC 要求

如果端口需要确定连接器的方向，则它应仅在进入 Attached.SRC 状态时通过检测 CC1 或 CC2 引脚中的哪个引脚通过电缆连接（即哪个 CC 引脚处于 SRC.Rd 状态）来执行此操作。

如果端口已从 AttachWait.SRC 状态或 Try.SRC 状态进入此状态，则 SRC.Rd 状态将仅出现在 CC1 或 CC2 引脚之一上。端口应在此 CC 引脚上提供电流并监视其状态。

如果端口由于 *USB PD* PR_Swap 而从 Attached.SNK 状态进入此状态，则端口应在连接的 CC 引脚上提供电流并监视其状态。

端口应提供表4-2中规定的Rp 4.

该端口应按照 Rp 上公布的水平提供 VBUS 电流。

端口应在进入此状态的 tVBUSON 时间内供应 VBUS，并且只要它作为电源运行，就一直供应。

在 VBUS 达到 vSafe5V 之前，端口不得发起任何 *USB PD* 通信。

如果端口支持超高速 USB 对上的信号传输，则它应当：

- 功能性地连接超高速 USB 对
- 对于 VCONN，请执行以下操作之一：
  - 在非 SRC.Rd 状态下无条件地向 CC 引脚提供 VCONN，或
  - 在 SRC.Ra 状态下向 CC 引脚提供 VCONN。

不支持超高速 USB 对上信号传输的端口可以采用上述相同的方式提供 VCONN。

该端口可能会协商*USB PD* PR_Swap、DR_Swap 或 VCONN_Swap。

如果端口提供 VCONN，则应在 tVCONNON 内提供。

端口可通过 SOP’上的 *USB PD* 查询电缆的身份。如果检测到它已连接到 VCONN 供电的 USB 设备，端口可能会移除 VBUS 并将其放电至 vSafe0V，同时继续保持此状态并应用 VCONN。端口还可以启动其他 SOP’通信。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The port shall not supply VCONN if it has entered this state as a result of a *USB PD* PR_Swap and was not previously supplying VCONN. A *USB PD* DR_Swap has no effect on which port sources VCONN.

The port may negotiate a *USB PD* VCONN_Swap. When the port successfully executes *USB PD* VCONN_Swap operation and was sourcing VCONN, it shall stop sourcing VCONN within tVCONNOFF. The port shall execute the VCONN_Swap in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes *USB PD* VCONN_Swap operation and was not sourcing VCONN, it shall start sourcing VCONN within tVCONNON.

The Charge-Through VCONN-Powered USB Device shall continue to isolate its Host-side port's CC pin from its Charge-Through CC pins.

The Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising Default USB Power on the Host-side port's CC pin, and continue to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through Rd.

The Charge-Through VCONN-Powered USB Device shall immediately connect the Charge-Through port's VBUS through to the Host-side port's VBUS.

The Charge-Through VCONN-Powered USB Device shall ensure that it is powered entirely by VBUS.

The Charge-Through VCONN-Powered USB Device shall only respond to *USB PD* Discover Identity queries on SOP' on its Host-side port and complete any active queries prior to exiting this state. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in *USB PD*.

4.5.2.2.9.2 Exiting from Attached.SRC State

A Source that is supplying VCONN or has yielded VCONN source responsibility to the Sink through *USB PD* VCONN_Swap messaging shall transition to UnattachedWait.SRC when the SRC.Open state is detected on the monitored CC pin. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.

A Source that is not supplying VCONN and has not yielded VCONN responsibility to the Sink through *USB PD* VCONN_Swap messaging shall transition to Unattached.SRC when the SRC.Open state is detected on the monitored CC pin. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.

When the SRC.Open state is detected on the monitored CC pin, a DRP shall transition to Unattached.SNK unless it strongly prefers the Source role. In that case, it shall transition to TryWait.SNK. This transition to TryWait.SNK is needed so that two devices that both prefer the Source role do not loop endlessly between Source and Sink. In other words, a DRP that would enter Try.SRC from AttachWait.SNK shall enter TryWait.SNK for a Sink detach from Attached.SRC.

A DRP that supports Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.SNK if the connected device identifies itself as a Charge-Through VCONN-Powered USB Device in its Discover Identity Command response. The DRP may delay this transition in order to perform further SOP' communication.

A port shall cease to supply VBUS within tVBUSOFF of exiting Attached.SRC.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

如果端口因 *USB PD* PR_Swap 而进入此状态且之前未提供 VCONN，则端口不得提供 VCONN。*USB PD* DR_Swap 对哪个端口提供 VCONN 没有影响。

端口可以协商 *USB PD* VCONN_Swap。当端口成功执行 *USB PD* VCONN_Swap 操作并且正在提供 VCONN 时，它应在 tVCONNOFF 内停止提供 VCONN。端口应按照先接后断的顺序执行 VCONN_Swap，以保持活动的 USB Type-C 到 USB Type-C 电缆供电。当端口成功执行 *USB PD* VCONN_Swap 操作并且没有提供 VCONN 时，它应在 tVCONNON 内开始提供 VCONN。

通过 VCONN 充电的 USB 设备应继续将其主机侧端口的 CC 引脚与其通过充电的 CC 引脚隔离。

通过 VCONN 供电的充电 USB 设备应维持其 Rp 终端在主机侧端口的 CC 引脚上通告默认 USB 电源，并继续通过 Rd 独立地将其通过充电端口的 CC1 和 CC2 引脚终止于地。

通过 VCONN 充电的 USB 设备应立即将通过 VCONN 充电端口的 VBUS 连接至主机端端口的 VBUS。

通过 VCONN 充电的 USB 设备应确保其完全由 VBUS 供电。

通过 VCONN 充电的 USB 设备应仅响应其主机端端口 SOP 上的 *USB PD* 发现身份查询，并在退出此状态之前完成所有主动查询。它应确保主机端端口 CC 上有足够的电容来满足 *USB PD* 中定义的 cReceiver。

4.5.2.2.9.2 退出 Attached.SRC 状态

当在受监控的 CC 引脚上检测到 SRC.Open 状态时，正在提供 VCONN 或已通过 *USB PD* VCONN_Swap 消息将 VCONN 源责任让给 Sink 的 Source 应转换为 UnattachedWait.SRC。Source 应在 tSRCDisconnect 内检测到 SRC.Open 状态，但应尽快检测到。

如果源未提供 VCONN，并且未通过 *USB PD* VCONN_Swap 消息将 VCONN 责任移交给接收器，则当在受监控的 CC 引脚上检测到 SRC.Open 状态时，源应转换为 Unattached.SRC。源应在 tSRCDisconnect 内检测到 SRC.Open 状态，但应尽快检测到。

当在受监控的 CC 引脚上检测到 SRC.Open 状态时，DRP 应转换为 Unattached.SNK，除非它强烈倾向于 Source 角色。在这种情况下，它应转换为 TryWait.SNK。需要转换为 TryWait.SNK，以便两个都倾向于 Source 角色的设备不会在 Source 和 Sink 之间无休止地循环。换句话说，从 AttachWait.SNK 进入 Try.SRC 的 DRP 应进入 TryWait.SNK，以便 Sink 从 Attached.SRC 分离。

如果连接的设备在其发现身份命令响应中将自己标识为通过 VCONN 充电的 USB 设备，则支持通过 VCONN 充电的 USB 设备的 DRP 将转换为 CTUnattached.SNK。DRP 可能会延迟此转换以执行进一步的 SOP 通信。

端口应在退出 Attached.SRC 后的 tVBUSOFF 时间内停止提供 VBUS。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A port that is supplying VCONN shall cease to supply it within tVCONNOFF of exiting Attached.SRC, unless it is exiting as a result of a *USB PD* PR_Swap or is transitioning into the CTUnattached.SNK state.

After a *USB PD* PR_Swap is accepted (i.e., either an Accept message is received or acknowledged), a DRP shall transition directly to the Attached.SNK state (i.e., remove Rp from CC, assert Rd on CC and stop supplying VBUS) and maintain its current data role, connection and VCONN supply state.

A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK when VBUS falls below vSinkDisconnect or the Host-side port's CC pin is SRC.Open. The Charge-Through VCONN-Powered USB Device shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.

4.5.2.2.10 Try.SRC State

This state appears in Figure 4-16.

When in the Try.SRC state, the port is querying to determine if the port partner supports the Sink role.

Note: if both Try.SRC and Try.SNK mechanisms are implemented, only one shall be enabled by the port at any given time. Deciding which of these two mechanisms is enabled is product design-specific.

4.5.2.2.10.1 Try.SRC Requirements

The port shall not drive VBUS or VCONN.

The port shall source current on both the CC1 and CC2 pins independently.

The port shall provide an Rp as specified in Table 4-24.

4.5.2.2.10.2 Exiting from Try.SRC State

The port shall transition to Attached.SRC when the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tTryCCDebounce.

The port shall transition to TryWait.SNK after tDRPTry and the SRC.Rd state has not been detected and VBUS is within vSafe0V, or after tTryTimeout and the SRC.Rd state has not been detected.

4.5.2.2.11 TryWait.SNK State

This state appears in Figure 4-16.

When in the TryWait.SNK state, the port has failed to become a Source and is waiting to attach as a Sink. Alternatively the port is responding to the Sink being removed while in the Attached.SRC state.

4.5.2.2.11.1 TryWait.SNK Requirements

The port shall not drive VBUS or VCONN.

Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

正在提供 VCONN 的端口应在退出 Attached.SRC 后的 tVCONNOFF 时间内停止提供 VCONN，除非它是由于 *USB PD* PR_Swap 而退出或转换到 CTUnattached.SNK 状态。

在接受 *USB PD* PR_Swap 之后（即，收到或确认接受消息），DRP 应直接转换到 Attached.SNK 状态（即，从 CC 中移除 Rp、在 CC 上断言 Rd 并停止提供 VBUS）并维持其当前数据角色、连接和 VCONN 供应状态。

当 VBUS 低于 vSinkDisconnect 或主机端端口的 CC 引脚为 SRC.Open 时，通过 VCONN 充电的 USB 设备应转换为 Unattached.SNK。通过 VCONN 充电的 USB 设备应在 tSRCDisconnect 内检测 SRC.Open 状态，但应尽快检测。

4.5.2.2.10 Try.SRC 状态

此状态如图 4-16 所示。

当处于 Try.SRC 状态时，端口正在查询以确定端口伙伴是否支持 Sink 角色。

注意：如果同时实现了 Try.SRC 和 Try.SNK 机制，则端口在任何给定时间只能启用其中一种。决定启用这两种机制中的哪一种取决于产品设计。

4.5.2.2.10.1 Try.SRC 要求

该端口不得驱动VBUS或VCONN。

港口应当 在 CC1 和 CC2 引脚上独立地提供电流 牙齿地。

端口应提供如表4-24所规定的Rp。

4.5.2.2.10.2 退出 Try.SRC 状态

当在至少 tTryCCDebounce 时间内在 CC1 或 CC2 引脚之一上检测到 SRC.Rd 状态时，端口应转换到 Attached.SRC。

在 tDRPTry 之后且未检测到 SRC.Rd 状态并且 VBUS 在 vSafe0V 内，或者在 tTryTimeout 之后且未检测到 SRC.Rd 状态，端口应转换到 TryWait.SNK。

4.5.2.2.11 TryWait.SNK 状态

此状态如图 4-16 所示。

当处于 TryWait.SNK 状态时，端口无法成为 Source，正在等待作为 Sink 连接。或者，当处于 Attached.SRC 状态时，端口正在响应 Sink 被移除的情况。

4.5.2.2.11.1 TryWait.SNK 要求

该端口不得驱动VBUS或VCONN。

CC1 和 CC2 引脚均应通过 Rd 独立接地。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.11.2 Exiting from TryWait.SNK State

The port shall transition to Attached.SNK after tCCDebounce if or when VBUS is detected. Note the Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on both the CC1 and CC2 pins, but this event will not exceed tPDDebounce.

The port shall transition to Unattached.SNK when the state of both of the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.

4.5.2.2.12 Try.SNK State

This state appears in Figure 4-14, Figure 4-17 and Figure 4-18.

When in the Try.SNK state, the port is querying to determine if the port partner supports the Source role.

When in the Try.SNK state, the Charge-Through VCONN-Powered USB Device is querying to determine if the port partner on the Host-side port supports the Source role.

Note: if both Try.SRC and Try.SNK mechanisms are implemented, only one shall be enabled by the port at any given time. Deciding which of these two mechanisms is enabled is product design-specific.

4.5.2.2.12.1 Try.SNK Requirements

The port shall not drive VBUS or VCONN.

Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VBUS from the Charge-Through port.

The Charge-Through VCONN-Powered USB Device shall remove its Rp termination (Default USB Power advertisement) on the Host-side port CC and provide an Rd termination to ground instead, as specified in Table 4-24 and remain to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through Rd.

4.5.2.2.12.2 Exiting from Try.SNK State

The port shall wait for tDRPTry and only then begin monitoring the CC1 and CC2 pins for the SNK.Rp state.

The port shall then transition to Attached.SNK when the SNK.Rp state is detected on exactly one of the CC1 or CC2 pins for at least tTryCCDebounce and VBUS is detected.

Alternatively, the port shall transition to TryWait.SRC if SNK.Rp state is not detected for tTryCCDebounce.

The Charge-Through VCONN-Powered USB Device shall wait for tDRPTry and only then begin monitoring the Host-side port's CC pin for the SNK.Rp state.

The Charge-Through VCONN-Powered USB Device shall then transition to Attached.SNK when the SNK.Rp state is detected on the Host-side port's CC pin for at least tTryCCDebounce and VBUS or VCONN is detected on Host-side port.

Alternatively, the Charge-Through VCONN-Powered USB Device shall transition to TryWait.SRC if Host-side SNK.Rp state is not detected for tTryCCDebounce.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.11.2 退出 TryWait.SNK 状态

如果检测到 VBUS，端口应在 tCCDebounce 之后转换为 Attached.SNK。请注意，源可能会启动 *USB PD* 通信，这将导致 CC1 和 CC2 引脚上出现短暂的 SNK.Open 状态，但此事件不会超过 tPD Debounce。

当 CC1 和 CC2 引脚的状态均为 SNK.Open 且持续至少 tPDDebounce 时，端口应转换至 Unattached .SNK。

4.5.2.2.12 Try.SNK 状态

该状态如图 4-14、图 4-17 和图 4-18 所示。

当处于 Try.SNK 状态时，端口正在查询以确定端口伙伴是否支持源角色。

当处于 Try.SNK 状态时，通过 VCONN 供电的 USB 设备正在查询以确定主机侧端口上的端口伙伴是否支持源角色。

注意：如果同时实现了 Try.SRC 和 Try.SNK 机制，则端口在任何给定时间只能启用其中一种。决定启用这两种机制中的哪一种取决于产品设计。

4.5.2.2.12.1 Try.SNK 要求

该端口不得驱动VBUS或VCONN。

CC1 和 d CC2 引脚应独立地端接至地 nd 穿过路。

通过 VCONN 充电的 USB 设备应将其主机端端口与其通过 VCONN 充电的端口隔离，包括 CC 和 VBUS。通过 VCONN 充电的 USB 设备应确保由通过 VCONN 充电的端口的 VBUS 供电。

通过 VCONN 供电的充电式 USB 设备应移除主机侧端口 CC 上的 Rp 终端（默认 USB 电源广告），并提供一个接地的 Rd 终端，如表 4-24 所示，并继续通过 Rd 将其充电式端口的 CC1 和 CC2 引脚独立接地。

4.5.2.2.12.2 退出 Try.SNK 状态

端口应等待 tDRPTry，然后才开始监控 CC1 和 CC2 引脚的 SNK.Rp 状态。

当在 CC1 或 CC2 引脚之一上检测到 SNK.Rp 状态至少 tTryCCDebounce 并且检测到 VBUS 时，端口应转换到 Attached.SNK。

或者，如果未检测到 tTryCCDebounce 的 SNK.Rp 状态，则端口应转换到 TryWait.SRC。

通过 VCONN 充电的 USB 设备应等待 tDRPTry，然后才开始监控主机侧端口的 CC 引脚的 SNK.Rp 状态。

当在主机端端口的 CC 引脚上检测到 SNK.Rp 状态至少持续 tTryCCDebounce 并且在主机端端口上检测到 VBUS 或 VCONN 时，通过 VCONN 充电供电的 USB 设备应转换为 Attached.SNK。

或者，如果在 tTryCCDebounce 期间未检测到主机端 SNK.Rp 状态，则通过 VCONN 充电的 USB 设备应转换至 TryWait.SRC。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A Sink with Accessory Support shall transition to Unsupported.Accessory if SNK.Rp state is not detected for tDRPTryWait.

Note: The Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on both the CC1 and CC2 pins, but this event will not exceed tTryCCDebounce.

4.5.2.2.13 TryWait.SRC State

This state appears in Figure 4-17 and Figure 4-18.

When in the TryWait.SRC state, the port has failed to become a Sink and is waiting to attach as a Source.

When in the TryWait.SRC state, the Charge-Through VCONN-Powered USB Device has failed to become a Sink on its Host-side port and is waiting to attach as a Source on its Host-side port.

4.5.2.2.13.1 TryWait.SRC Requirements

The requirements for this state are identical to Unattached.SRC.

4.5.2.2.13.2 Exiting from TryWait.SRC State

The port shall transition to Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC pins for at least tTryCCDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to Attached.SRC when host-side VBUS is at vSafe0V and the SRC.Rd state is detected on the Host-side port's CC pin for at least tTryCCDebounce.

The port shall transition to Unattached.SNK after tDRPTry if neither of the CC1 or CC2 pins are in the SRC.Rd state.

The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK after tDRPTry if the Host-side port's CC pin is not in the SRC.Rd state.

4.5.2.2.14 Unattached.Accessory State

This state appears in Figure 4-14.

The Unattached.Accessory state allows accessory-supporting Sinks to connect to audio or VCONN-Powered Accessories.

This state is functionally equivalent to the Unattached.SRC state in a DRP, except that Attached.SRC is not supported.

4.5.2.2.14.1 Unattached.Accessory Requirements

The port shall not drive VBUS or VCONN.

The port shall source current on both the CC1 and CC2 pins independently.

The port shall provide an Rp as specified in Table 4-24.

4.5.2.2.14.2 Exiting from Unattached.Accessory State

A port that supports Audio Adapter Accessory Mode shall transition to AttachWait.Accessory when the state of both CC pins is SRC.Ra.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

如果在 tDRPTryWait 中未检测到 SNK.Rp 状态，则具有附件支持的接收器应转换为 Unsupported.Accessory。

注意：源可能会启动 *USB PD* 通信，这将导致 CC1 和 CC2 引脚上出现短暂的 SNK.Open 状态，但此事件不会超过 tTryCCDebounce。

4.5.2.2.13 TryWait.SRC 状态

该状态如图 4-17 和图 4-18 所示。

当处于 TryWait.SRC 状态时，端口无法成为 Sink，正在等待作为 Source 连接。

当处于 TryWait.SRC 状态时，通过 VCONN 充电的 USB 设备无法在其主机端端口上成为接收端，并且正在等待在其主机端端口上作为源进行连接。

4.5.2.2.13.1 TryWait.SRC 要求

此状态的要求与 Unattached.SRC 相同。

4.5.2.2.13.2 退出 TryWait.SRC 状态

当 VBUS 处于 vSafe0V 并且在至少 tTryCCDebounce 的时间内恰好在其中一个 CC 引脚上检测到 SRC.Rd 状态时，端口应转换到 Attached.SRC。

当主机端 VBUS 处于 vSafe0V 并且在主机端端口的 CC 引脚上检测到 SRC.Rd 状态至少 tTryCCDebounce 时，通过 VCONN 充电供电的 USB 设备应转换到 Attached.SRC。

如果 CC1 或 CC2 引脚均未处于 SRC.Rd 状态，则端口应在 tDRPTry 之后转换至 Unattached.SNK。

如果主机端端口的 CC 引脚未处于 SRC.Rd 状态，则通过 VCONN 充电的 USB 设备应在 tDRPTry 之后转换为 Unattached.SNK。

4.5.2.2.14 未连接附件状态

此状态如图 4-14 所示。

Unattached.Accessory 状态允许支持配件的接收器连接到音频或 VCONN 供电的配件。

此状态在功能上等同于 DRP 中的 Unattached.SRC 状态，只是不支持 Attached.SRC。

4.5.2.2.14.1 独立附件要求

该端口不得驱动VBUS或VCONN。

该端口应独立地在 CC1 和 CC2 引脚上提供电流。

端口应提供如表4-24所规定的Rp。

4.5.2.2.14.2 退出未连接附件状态

当两个 CC 引脚的状态为 SRC.Ra 时，支持音频适配器附件模式的端口应转换为 AttachWait.Accessory。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A port that supports VCONN-Powered Accessories also shall transition to AttachWait.Accessory when the state of either CC1 or CC2 pin is SRC.Ra and the other CC pin is SRC.Rd.

The maximum time the local port shall take to transition from Unattached.Accessory to the AttachWait.Accessory state when an Audio Adapter Accessory or VCONN-Powered Accessory is present is tOnePortToggleConnect.

Otherwise, the port shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.

4.5.2.2.15 AttachWait.Accessory State

This state appears in Figure 4-14.

The AttachWait.Accessory state is used to ensure that the state of both of the CC1 and CC2 pins is stable after a cable is plugged in.

4.5.2.2.15.1 AttachWait.Accessory Requirements

The requirements for this state are identical to Unattached.Accessory.

4.5.2.2.15.2 Exiting from AttachWait.Accessory State

If the port supports Audio Adapter Accessory Mode, it shall transition to AudioAccessory when the state of both the CC1 and CC2 pins is SRC.Ra for at least tCCDebounce.

The port shall transition to Unattached.SNK when the state of either the CC1 or CC2 pin is SRC.Open for at least tCCDebounce.

If the port supports VCONN-Powered Accessories, it shall transition to PoweredAccessory state if the state of either the CC1 or CC2 pin is SRC.Rd and the other CC pin is SRC.Ra concurrently for at least tCCDebounce.

4.5.2.2.16 AudioAccessory State

This state appears in Figure 4-12, Figure 4-14, Figure 4-16 and Figure 4-17.

The AudioAccessory state is used for the Audio Adapter Accessory Mode specified in Appendix A.

4.5.2.2.16.1 AudioAccessory Requirements

The port shall reconfigure its pins as detailed in Appendix A.

The port shall not drive VBUS or VCONN. A port that sinks current from the audio accessory over VBUS shall not draw more than 500 mA.

The port shall provide an Rp as specified in Table 4-24.

The port shall source current on at least one of the CC1 or CC2 pins and monitor to detect when the state is no longer SRC.Ra. If the port sources and monitors only one of CC1 or CC2, then it shall ensure that the termination on the unmonitored CC pin does not affect the monitored signal when the port is connected to an Audio Accessory that may short both CC1 and CC2 pins together.

4.5.2.2.16.2 Exiting from AudioAccessory State

If the port is a Sink, the port shall transition to Unattached.SNK when the state of the monitored CC1 or CC2 pin(s) is SRC.Open for at least tCCDebounce.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

当 CC1 或 CC2 引脚的状态为 SRC.Ra 且另一个 CC 引脚的状态为 SRC.Rd 时，支持 VCONN 供电配件的端口也应转换到 AttachWait.Accessory。

当存在音频适配器附件或 VCONN 供电附件时，本地端口从 Unattached.Accessory 转换到 AttachWait.Accessory 状态所需的最大时间为 tOnePortToggleConnect。

否则，端口应在 dcSRC.DRP · tDRP 之后的 tDRPTransition 内转换到 Unattached.SNK，或者根据指示转换。

4.5.2.2.15 AttachWait.Accessory 状态

此状态如图 4-14 所示。

AttachWait.Accessory 状态用于确保插入电缆后 CC1 和 CC2 引脚的状态都稳定。

4.5.2.2.15.1 AttachWait.Accessory 要求

此状态的要求与 Unattached.Accessory 相同。

4.5.2.2.15.2 退出 AttachWait.Accessory 状态

如果端口支持音频适配器附件模式，则当 CC1 和 CC2 引脚的状态均为 SRC.Ra 且持续至少 tCCDebounce 时，它应转换至音频附件。

当 CC1 或 CC2 引脚的状态为 SRC.Open 至少 tCCDebounce 时，端口应转换至 Unattached.SNK。

如果端口支持 VCONN 供电配件，则当 CC1 或 CC2 引脚的状态为 SRC.Rd 且另一个 CC 引脚的状态为 SRC.Ra 且同时持续至少 tCCDebounce 时，它将转换到 PoweredAccessory 状态。

4.5.2.2.16 音频配件状态

此州应用程序 图 4-12、图 4-14、图 4-16 和图 重新4-17。

AudioAccessory 状态用于附录 A 中指定的音频适配器附件模式。

4.5.2.2.16.1 音频配件要求

该端口应按照附录 A 中详细说明重新配置其引脚。

该端口不得驱动 VBUS 或 VCONN。通过 VBUS 从音频配件吸收电流的端口不得超过 500 mA。

端口应提供如表4-24所规定的Rp。

端口应在 CC 1 或 CC2 引脚中的至少一个上提供电流，并进行监控以检测状态何时不再为 SRC.Ra。如果端口仅提供并监控 CC1 或 CC2 中的一个，则应确保当端口连接到可能将 CC 1 和 CC2 引脚短接在一起的音频配件时，未监控的 CC 引脚上的端接不会影响监控信号。

4.5.2.2.16.2 退出音频配件状态

如果端口是 Sink，则当监控的 CC1 或 CC2 引脚的状态为 SRC.Open 至少 tCCDebounce 时，端口应转换到 Unattached.SNK。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

If the port is a Source or DRP, the port shall transition to Unattached.SRC when the state of the monitored CC1 or CC2 pin(s) is SRC.Open for at least tCCDebounce.

4.5.2.2.17 UnorientedDebugAccessory.SRC

This state appears in Figure 4-12, Figure 4-16 and Figure 4-17.

The UnorientedDebugAccessory.SRC state is used for the Debug Accessory Mode specified in Appendix B.

4.5.2.2.17.1 UnorientedDebugAccessory.SRC Requirements

This mode is for debug only and shall not be used for communicating with commercial products.

The port shall provide an Rp as specified in Table 4-24 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.

The port shall supply VBUS current at the level it advertises on Rp. The port shall not drive VCONN.

The port may connect any non-orientation specific debug signals for Debug Accessory Mode operation only after entry to this state.

4.5.2.2.17.2 Exiting from UnorientedDebugAccessory.SRC State

If the port is a Source, the port shall transition to Unattached.SRC when the SRC.Open state is detected on either the CC1 or CC2 pin.

If the port is a DRP, the port shall transition to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin.

The port shall transition to OrientedDebugAccessory.SRC state if orientation is required and detected as described in Section B.2.6.1.2.

4.5.2.2.18 OrientedDebugAccessory.SRC State

This state appears in Figure 4-12, Figure 4-16 and Figure 4-17.

The OrientedDebugAccessory.SRC state is used for the Debug Accessory Mode specified in Appendix B.

4.5.2.2.18.1 OrientedDebugAccessory.SRC State Requirements

This mode is for debug only and shall not be used for communicating with commercial products.

The port shall provide an Rp as specified in Table 4-24 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.

The port shall supply VBUS current at the level it advertises on Rp. The port shall not drive VCONN.

The port shall connect any orientation specific debug signals for Debug Accessory Mode operation only after entry to this state. Any non-orientation specific debug signals for Debug Accessory Mode operation shall be connected or remain connected in this state.

If the port needs to establish *USB PD* communications, it shall do so only after entry to this state. The port shall not initiate any *USB PD* communications until VBUS reaches vSafe5V. In this state, the port takes on the initial *USB PD* role of DFP/Source.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

如果端口是源或 DRP，则当监控的 CC1 或 CC2 引脚的状态为 SRC.Open 至少 tCCDebounce 时，端口应转换到 Unattached.SRC。

4.5.2.2.17 无方向调试附件.SRC

该状态如图 4-12、图 4-16 和图 4-17 所示。

UnientedDebugAccessory.SRC状态用于附录B中指定的调试附件模式。

4.5.2.2.17.1 UnientedDebugAccessory.SRC 要求

此模式仅用于调试，不可用于与商业产品通信。

端口应在 CC1 和 CC2 引脚上提供如表 4-24 所指定的 Rp，并监控以检测任一引脚的状态何时为 SRC.Open。

该端口应按 Rp 上公布的水平提供 VBUS 电流。该端口不得驱动 VCONN。

只有进入此状态后，端口才可以连接任何非方向特定的调试信号以进行调试附件模式操作。

4.5.2.2.17.2 退出 UnientedDebugAccessory.SRC 状态

如果端口是源，则当在 CC1 或 CC2 引脚上检测到 SRC.Open 状态时，端口应转换到 Unattached.SRC。

如果端口是 DRP，则当在 CC1 或 CC2 引脚上检测到 SRC.Open 状态时，端口应转换到 Unattached.SNK。

如果需要并检测到方向，则端口应转换到 OrientedDebugAccessory.SRC 状态，如第 B.2.6.1.2 节所述。

4.5.2.2.18 OrientedDebugAccessory.SRC 状态

该状态如图 4-12、图 4-16 和图 4-17 所示。

OrientedDebugAccessory.SRC状态用于附录B中指定的调试附件模式。

4.5.2.2.18.1 OrientedDebugAccessory.SRC 状态要求

此模式仅用于调试，不可用于与商业产品通信。

端口应在 CC1 和 CC2 引脚上提供如表 4-24 所指定的 Rp，并监控以检测任一引脚的状态何时为 SRC.Open。

该端口应按 Rp 上公布的水平提供 VBUS 电流。该端口不得驱动 VCONN。

仅当进入此状态后，端口才应连接任何特定于方向的调试信号以进行调试附件模式操作。任何非特定于方向的调试信号都应在此状态下连接或保持连接。

如果端口需要建立 *USB PD* 通信，则应仅在进入此状态后才进行。在 VBUS 达到 vSafe5V 之前，端口不得发起任何 *USB PD* 通信。在此状态下，端口承担 DFP/Source 的初始 *USB PD* 角色。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.18.2 Exiting from OrientedDebugAccessory.SRC State

If the port is a Source, the port shall transition to Unattached.SRC when the SRC.Open state is detected on either the CC1 or CC2 pin.

If the port is a DRP, the port shall transition to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin.

4.5.2.2.19 DebugAccessory.SNK

This state appears in Figure 4-13, Figure 4-14, Figure 4-16 and Figure 4-17.

The DebugAccessory.SNK state is used for the Debug Accessory Mode specified in Appendix B.

4.5.2.2.19.1 DebugAccessory.SNK Requirements

This mode is for debug only and shall not be used for communicating with commercial products.

The port shall not drive VBUS or VCONN.

The port shall provide an Rd as specified in Table 4-25 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.

If supported, orientation is determined as outlined in Section B.2.6.1.1. The port shall connect any debug signals for Debug Accessory Mode operation only after entry to this state.

4.5.2.2.19.2 Exiting from DebugAccessory.SNK State

The port shall transition to Unattached.SNK when VBUS is no longer present.

4.5.2.2.20 PoweredAccessory State

This state appears in Figure 4-14.

When in the PoweredAccessory state, the port is powering a VCONN–Powered Accessory or VCONN-Powered USB Device.

4.5.2.2.20.1 PoweredAccessory Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to the PoweredAccessory state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., which CC pin is in the SRC.Rd state).

The SRC.Rd state is detected on only one of the CC1 or CC2 pins. The port shall advertise either 1.5 A or 3.0 A (see Table 4-24) on this CC pin and monitor its state.

The port shall supply VCONN on the unused CC pin within tVconnON-PA of entering the PoweredAccessory state.

The port shall not drive VBUS.

When the port initially enters the PoweredAccessory state it shall operate as a *USB Power Delivery* Source with a DFP data role. In addition, the port shall support at least one of the following:

- Use *USB PD* to establish an explicit contract and then use Structured Vendor Defined Messages (Structured VDMs) to identify a VCONN–Powered Accessory and enter an Alternate Mode.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.18.2 退出 OrientedDebugAccessory.SRC 状态

如果端口是源，则当在 CC1 或 CC2 引脚上检测到 SRC.Open 状态时，端口应转换到 Unattached.SRC。

如果端口是 DRP，则当在 CC1 或 CC2 引脚上检测到 SRC.Open 状态时，端口应转换到 Unattached.SNK。

4.5.2.2.19 调试附件.SNK

该状态出现在图4-13、图4-14、图4-16和图4-17中。

DebugAccessory.SNK 状态用于附录 B 中指定的调试附件模式。

4.5.2.2.19.1 DebugAccessory.SNK 要求

此模式仅用于调试，不可用于与商业产品通信。

该端口不得驱动VBUS或VCONN。

端口应在 CC1 和 CC2 引脚上提供如表 4-25 所指定的 Rd，并监控以检测任一引脚的状态是否为 SRC.Open。

如果支持，方向将按照 B.2.6.1.1 节中概述的方式确定。仅当进入此状态后，端口才应连接任何调试信号以进行调试附件模式操作。

4.5.2.2.19.2 退出DebugAccessory.SNK状态

当 VBUS 不再存在时，端口应转换至 Unattached.SNK。

4.5.2.2.20 供电附件状态

此状态如图 4-14 所示。

当处于 PoweredAccessory 状态时，端口正在为 VCONN 供电配件或 VCONN 供电 USB 设备供电。

4.5.2.2.20.1 供电附件要求

如果端口需要确定连接器的方向，则它应仅在进入 PoweredAccessory 状态时通过检测哪个 CC1 或 CC2 引脚通过电缆连接（即哪个 CC 引脚处于 SRC.Rd 状态）来执行此操作。

仅在 CC1 或 CC2 引脚之一上检测到 SRC.Rd 状态。端口应在此 CC 引脚上通告 1.5 A 或 3.0 A（见表 4-24）并监视其状态。

端口应在进入 PoweredAccessory 状态的 tVconnON-PA 时间内在未使用的 CC 引脚上提供 VCONN。

该端口不得驱动VBUS。

当端口最初进入 PoweredAccessory 状态时，它应作为具有 DFP 数据角色的 *USB Power Delivery* 源运行。此外，端口应支持以下至少一项：

- 使用*USB PD*建立明确的合同，然后使用结构化供应商定义消息（结构化VDM）来识别VCONN供电配件并进入替代模式。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- Use *USB PD* to query the identity of a VCONN-Powered USB Device (that operates as a cable plug responding to SOP').

4.5.2.2.20.2 Exiting from PoweredAccessory State

The port shall transition to Unattached.SNK when the SRC.Open state is detected on the monitored CC pin.

The port shall transition to Try.SNK if the attached device is not a VCONN–Powered Accessory or VCONN-Powered USB Device. For example, the attached device does not support *USB PD* or does not respond to *USB PD* commands required for a VCONN–Powered Accessory (e.g., Discover SVIDs, Discover Modes, etc.) or is a Sink or DRP attached through a Powered Cable.

The port shall transition to Unsupported.Accessory if the attached device is a VCONN–Powered Accessory but the port has not successfully entered an Alternate Mode within tAMETimeout (see Appendix E).

A port that supports Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.SNK if the connected device identifies itself as a Charge-Through VCONN-Powered USB Device in its Discover Identity Command response. The port may delay this transition in order to perform further SOP' communication.

The port shall cease to supply VCONN within tVCONNOFF of exiting the PoweredAccessory state unless it is transitioning into the CTUnattached.SNK state.

4.5.2.2.21 Unsupported.Accessory State

This state appears in Figure 4-14.

If a VCONN–Powered Accessory does not enter an Alternate Mode, the Unsupported.Accessory state is used to wait until the accessory is unplugged before continuing.

4.5.2.2.21.1 Unsupported.Accessory Requirements

Only one of the CC1 or CC2 pins shall be in the SRC.Rd state. The port shall advertise Default USB Power (see Table 4-24) on this CC pin and monitor its voltage.

The port shall not drive VBUS or VCONN.

A Sink with either VCONN–Powered Accessory or VCONN-Powered USB Device support shall provide user notification that it does not recognize or support the attached accessory or device.

4.5.2.2.21.2 Exiting from Unsupported.Accessory

The port shall transition to Unattached.SNK when the SRC.Open state is detected on the monitored CC pin.

4.5.2.2.22 CTUnattached.VPD State

This state appears in Figure 4-18.

When in the CTUnattached.VPD state, the Charge-Through VCONN-Powered USB Device has detected SNK.Open on its host port for tVPDCTDD, indicating that it is connected to a Charge-Through capable Source, and is independently monitoring its Charge-Through port for the presence of a pass-through Power Source.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- 使用 *USB PD* 查询 VCONN 供电 USB 设备的身份（作为响应 SOP ’ 的电缆插头运行）。

4.5.2.2.20.2 退出 PoweredAccessory 状态

当在监控的 CC 引脚上检测到 SRC.Open 状态时，端口应转换至 Unattached.SNK。

如果所连接的设备不是 VCONN 供电配件或 VCONN 供电 USB 设备，则端口应转换为 Try.SNK。例如，所连接的设备不支持 *USB PD* 或不响应 VCONN 供电配件所需的 *USB PD* 命令（例如，发现 SVID、发现模式等），或者是通过供电电缆连接的接收器或 DRP。

如果所连接设备是 VCONN 供电配件，但端口未在 tAMETimeout 内成功进入备用模式，则端口应转换为不受支持的配件（参见附录 E）。

如果连接的设备在其发现身份命令响应中将自己标识为通过 VCONN 充电的 USB 设备，则支持通过 VCONN 充电的 USB 设备的端口应转换为 CTUnattached.SNK。端口可能会延迟此转换以执行进一步的 SOP 通信。

除非端口正在转换到 CTUnattached.SNK 状态，否则端口应在退出 PoweredAccessory 状态后的 tVCONNOFF 时间内停止提供 VCONN。

4.5.2.2.21 不支持的配件状态

此状态如图 4-14 所示。

如果 VCONN 供电配件未进入备用模式，则将使用不支持的配件状态等待，直到拔下配件后再继续。

4.5.2.2.21.1 不支持的配件要求

CC1 或 CC2 引脚中只有一个应处于 SRC.Rd 状态。端口应在此 CC 引脚上通告默认 USB 电源（见表 4-24）并监控其电压。

该端口不得驱动VBUS或VCONN。

具有 VCONN 供电配件或 VCONN 供电 USB 设备支持的接收器应向用户发出通知，告知其不识别或支持所连接的配件或设备。

4.5.2.2.21.2 退出 Unsupported.Accessory

当在监控的 CC 引脚上检测到 SRC.Open 状态时，端口应转换至 Unattached.SNK。

4.5.2.2.22 CTUnattached.VPD 状态

此状态如图 4-18 所示。

当处于 CTUnattached.VPD 状态时，通过 VCONN 充电的 USB 设备已在其主机端口上检测到 SNK.Open，持续时间为 tVPDCTDD，这表明它已连接到具有充电功能的电源，并且正在独立监控其充电端口是否存在直通电源。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

This state may also have been entered through detach of a Power Source on the Charge-Through port or detach of a sink from the CTVPD's Charge-through port.

4.5.2.2.22.1 CTUnattached.VPD Requirements

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (*USB 3.2*) / ICCSH (*USB 2.0*) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

Upon entry into this state, the device shall remove its Rd termination to ground (if present) on the Host-side port CC and provide an Rp termination advertising 3.0 A instead, as specified in Table 4-24. Note that because VBUS is not provided, the Rp termination signals continued connection to the port partner but does not carry with it any current advertisement.

The Charge-Through VCONN-Powered USB Device shall only respond to *USB PD* Discover Identity queries on SOP' on its Host-side port. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in *USB PD*.

The Charge-Through VCONN-Powered USB Device shall independently terminate both the Charge-Through port's CC1 and CC2 pins to ground through Rd.

The Charge-Through VCONN-Powered USB Device shall provide a bypass capacitance of CCTB on the Charge-Through Port's VBUS pins.

4.5.2.2.22.2 Exiting from CTUnattached.VPD

The Charge-Through VCONN-Powered USB Device shall transition to CTAttachWait.VPD when a Source connection is detected on the Charge-Through port, as indicated by the SNK.Rp state on exactly one of the Charge-Through port's CC pins.

Debug accessories are not supported on the Charge-Through port.

The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDisconnect.

The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.Unsupported within tDRPTransition after the state of both the Charge-Through port's CC1 and CC2 pins is SNK.Open for tDRP − dcSRC.DRP · tDRP, or if directed.

4.5.2.2.23 CTAttachWait.VPD State

This state appears in Figure 4-18.

When in the CTAttachWait.VPD state, the device has detected the SNK.Rp state on exactly one of its Charge-Through port's CC pins and is waiting for VBUS on the Charge-Through port.

4.5.2.2.23.1 CTAttachWait.VPD Requirements

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (*USB 3.2*) / ICCSH (*USB 2.0*) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

也可能通过断开充电端口上的电源或断开 CTVPD 充电端口上的接收器而进入此状态。

4.5.2.2.22.1 CTUnattached.VPD 要求

通过 VCONN 充电的 USB 设备应将其主机端端口与其通过 VCONN 充电的端口隔离，包括 CC 和 VBUS。通过 VCONN 充电的 USB 设备应确保其由 VCONN 供电，不会从 VBUS 消耗超过 ICCS (*USB 3.2*)/ICCSH (*USB 2.0*) 的电量进行监控，并且与 VBUS 充分隔离以承受通过 VCONN 充电操作期间的高电压。

进入此状态后，设备应移除主机端端口 CC 上的接地 Rd 终端（如果存在），并提供 Rp 终端来通告 3.0 A，如表 4-24 中所述。请注意，由于未提供 VBUS，Rp 终端会发出与端口伙伴继续连接的信号，但不携带任何电流通告。

通过 VCONN 充电的 USB 设备应仅响应其主机端端口上 SOP 上的 *USB PD* 发现身份查询。它应确保主机端端口 CC 上有足够的电容来满足 *USB PD* 中定义的 cReceiver。

通过 VCONN 充电的 USB 设备应通过 Rd 独立地将通过 VCONN 充电端口的 CC1 和 CC2 引脚接地。

通过 VCONN 充电的 USB 设备应在通过充电端口的 VBUS 引脚上提供 CCTB 的旁路电容。

4.5.2.2.22.2 退出 CTUnattached.VPD

当以下情况发生时，通过 VCONN 供电的 USB 设备应转换至 CTAttachWait.VPD：
在 Charge-Through 端口上检测到源连接，如 Charge-Through 端口的其中一个 CC 引脚上的 SNK.Rp 状态所示。

Charge-Through 端口不支持调试配件。

如果 VCONN 低于 vVCONNDisconnect，则通过 VCONN 充电的 USB 设备应转换为 Unattached.SNK。

在充电端口的 CC1 和 CC2 引脚的状态均为 SNK.Open（tDRP – dcSRC.DRP · tDRP）之后，或者如果指示，充电直通 VCONN 供电 USB 设备应在 tDRPTransition 内转换为 CTUnattached.Unsupported。

4.5.2.2.23 CTAttachWait.VPD 状态

此状态如图 4-18 所示。

当处于 CTAttachWait.VPD 状态时，设备已在其 Charge-Through 端口的 CC 引脚之一上检测到 SNK.Rp 状态，并且正在等待 Charge-Through 端口上的 VBUS。

4.5.2.2.23.1 CTAttachWait.VPD 要求

通过 VCONN 充电的 USB 设备应将其主机端端口与其通过 VCONN 充电端口隔离，包括 CC 和 VBUS。通过 VCONN 充电的 USB 设备应确保其由 VCONN 供电，不会从 VBUS 消耗超过 ICCS (*USB 3.2*)/ICCSH (*USB 2.0*) 的电量进行监控，并且与 VBUS 充分隔离以在通过 VCONN 充电操作期间承受高电压。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising 3.0 A on the Host-side port's CC pin, as well as the independent terminations to ground through Rd on the Charge-Through port's CC1 and CC2 pins.

The Charge-Through VCONN-Powered USB Device shall only respond to *USB PD* Discover Identity queries on SOP' on its Host-side port, and complete any active queries prior to exiting this state. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in *USB PD*.

4.5.2.2.23.2 Exiting from CTAttachWait.VPD

The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when the state of both the Charge-Through port's CC1 and CC2 pins are SNK.Open for at least tPDDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to CTAttached.VPD after the state of only one of the Charge-Through port's CC1 or CC2 pins is SNK.Rp for at least tCCDebounce and VBUS on the Charge-Through port is detected.

Note the Charge-Through Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on one of the Charge-Through port's CC pins with the state of the Charge-Through port's other CC pin remaining SNK.Open, but this event will not exceed tPDDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to CTDisabled.VPD if VCONN falls below vVCONNDisconnect.

4.5.2.2.24 CTAttached.VPD State

This state appears in Figure 4-18.

When in the CTAttached.VPD state, the Charge-Through VCONN-Powered USB Device has detected a Power Source on its Charge-Through port and has connected the Charge-Through port's CC and VBUS pins directly to the Host-side port's CC and VBUS pins. Hence all power delivery, negotiation and *USB PD* communication are performed directly between the unit on Host-side port and the Power Source connected to the Charge-Through port.

4.5.2.2.24.1 CTAttached.VPD Requirements

Upon entry to this state, the Charge-Through VCONN-Powered USB Device shall detect which of the Charge-Through port's CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the SNK.Rp state). The device shall then immediately, in the following order:

1. Remove or reduce any additional capacitance on the Host-side CC port that was introduced in order to meet cReceiver as defined in *USB PD* to present on CC a value equal to or less than two times the maximum value for cCablePlug_CC.
2. Disable the Rp termination advertising 3.0 A on the host port's CC pin.
3. Passively multiplex the detected Charge-Through port's CC pin through to the host port's CC pin with an impedance of less than RccCON.
4. Disable the Rd on the Charge-Through port's CC1 and CC2 pins.
5. Connect the Charge-Through port's VBUS through to the host port's VBUS.

These steps shall be completed within tVPDDetach minimum of entering this state.

The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (*USB 3.2*) / ICCSH (*USB 2.0*) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

通过 VCONN 充电的 USB 设备应维持其 Rp 终端在主机端端口的 CC 引脚上提供 3.0 A 电流，以及通过通过 Rd 在充电端口的 CC1 和 CC2 引脚上独立接地。

通过 VCONN 充电的 USB 设备应仅响应其主机端端口上 SOP ’ 上的 *USB PD* 发现身份查询，并在退出此状态之前完成所有主动查询。它应确保主机端端口 CC 上有足够的电容来满足 *USB PD* 中定义的 cReceiver。

4.5.2.2.23.2 退出 CTAttachWait.VPD

当通过 VCONN 供电的 USB 设备充电时，应转换为 CTUnattached.VPD
Charge-Through 端口的 CC1 和 CC2 引脚的状态均为 SNK.Open，持续时间至少为 tPDDebounce。

在充电直通端口的 CC1 或 CC2 引脚中只有一个引脚的状态为 SNK.Rp 至少持续 tCCDebounce 并且检测到充电直通端口上的 VBUS 后，充电直通 VCONN 供电 USB 设备应转换到 CTAttached.VPD。

请注意，充电直通源可能会启动 *USB PD* 通信，这将导致充电直通端口的其中一个 CC 引脚上出现短暂的 SNK.Open 状态，而充电直通端口的另一个 CC 引脚的状态仍为 SNK.Open，但此事件不会超过 tPDDebounce。

如果 VCONN 低于 vVCONNDisconnect，则通过 VCONN 充电的 USB 设备应转换为 CTDisabled.VPD。

4.5.2.2.24 CTAttached.VPD 状态

此状态如图 4-18 所示。

当处于 CTAttached.VPD 状态时，通过 VCONN 供电的充电式 USB 设备已检测到其充电式端口上的电源，并将充电式端口的 CC 和 VBUS 引脚直接连接到主机端端口的 CC 和 VBUS 引脚。因此，所有电力输送、协商和 *USB PD* 通信均直接在主机端端口上的设备与连接到充电式端口的电源之间进行。

4.5.2.2.24.1 CTAttached.VPD 要求

进入此状态后，通过 VCONN 充电的 USB 设备应检测通过电缆连接的是充电端口的 CC1 还是 CC2 引脚（即 CC 引脚
即处于 SNK.Rp 状态）。设备应立即按照以下顺序：

1. 移除或减少主机端 CC 端口上的任何额外电容，这些电容是为了满足 *USB PD* 中定义的 cReceiver 而引入的，以便在 CC 上显示一个值
等于或小于 cCablePlug_CC 最大值的两倍。2. 禁用 Rp 终端，在主机端口的 CC 引脚上通告 3.0 A。3. 被动地将检测到的 Charge-Through 端口的 CC 引脚复用到主机端口的 CC 引脚，阻抗小于 RccCON。4. 禁用 Charge-Through 端口的 CC1 和 CC2 引脚上的 Rd。5. 将 Charge-Through 端口的 VBUS 连接到主机端口的 VBUS。

这些步骤应在进入该状态后的至少 tVPDDetach 时间内完成。

通过 VCONN 充电的 USB 设备应确保由 VCONN 供电，不会从 VBUS 消耗超过 ICCS (*USB 3.2*) / ICCSH (*USB 2.0*) 的电量进行监控，并且与 VBUS 充分隔离以承受通过充电操作期间的高电压。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The Charge-Through VCONN-Powered USB Device shall not respond to any *USB PD* communication on any CC pin in this state. Any active queries on SOP' shall have been completed prior to entering this state.

4.5.2.2.24.2 Exiting from CTAttached.VPD

The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when VBUS falls below vSinkDisconnect and the state of the passed-through CC pin is SNK.Open for tVPDCTDD.

The Charge-Through VCONN-Powered USB Device shall transition to CTDisabled.VPD if VCONN falls below vVCONNDisconnect.

4.5.2.2.25 CTDisabled.VPD State

This state appears in Figure 4-18.

When in the CTDisabled.VPD state, the Charge-Through VCONN-Powered USB Device has detected the detach on its Host-side port but may still potentially be connected to a Power Source on the Charge-Through port, and is thus ensuring that the VBUS from the Power Source is removed.

4.5.2.2.25.1 CTDisabled.VPD Requirements

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS.

The device shall present a high-impedance to ground (above zOPEN) on the Host-side port's CC pin and on the Charge-Through port CC1 and CC2 pins.

The Charge-Through VCONN-Powered USB Device shall ensure that it is powered entirely by VBUS.

4.5.2.2.25.2 Exiting from CTDisabled.VPD

The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK after tVPDDisable.

4.5.2.2.26 CTUnattached.SNK State

This state appears in Figure 4-14, Figure 4-16 and Figure 4-17.

When in the CTUnattached.SNK state, the port has detected that it is attached to a Charge-Through VCONN-Powered USB Device and is ready if a Power Source is attached to the Charge-Through VCONN-Powered USB Device.

This state may also have been entered through detach of a Charge-Through Power Source.

4.5.2.2.26.1 CTUnattached.SNK Requirements

Upon entry to this state, the port shall remove its Rp termination (if present) and terminate CC to ground through Rd.

The port shall continue to supply VCONN.

The port shall stop sourcing or sinking VBUS and discharge it.

In *USB PD* Version 2.0, the port shall act as a bus master for the purposes of initiating PD messages.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

在此状态下，通过 VCONN 充电的 USB 设备不得响应任何 CC 引脚上的任何 *USB PD* 通信。
在进入此状态之前，必须先完成对 SOP ’ 的任何活动查询。

4.5.2.2.24.2 退出 CTAttached.VPD

当 VBUS 低于 vSinkDisconnect 且直通 CC 引脚的状态为 SNK.Open 且持续时间为 tVPDCTDD 时，通过 VCONN 充电的 USB 设备应转换为 CTUnattached.VPD。

如果 VCONN 低于 vVCONNDisconnect，则通过 VCONN 充电的 USB 设备应转换为 CTDisabled.VPD。

4.5.2.2.25 CTDisabled.VPD 状态

此状态如图 4-18 所示。

当处于 CTDisabled.VPD 状态时，通过 VCONN 充电供电的 USB 设备已检测到其主机侧端口上的断开连接，但仍有可能连接到通过充电端口上的电源，因此确保已移除来自电源的 VBUS。

4.5.2.2.25.1 CTDisabled.VPD 要求

通过 VCONN 充电供电的 USB 设备应将其主机侧端口与其通过充电端口隔离，包括 CC 和 VBUS。

设备应在主机端端口上呈现对地高阻抗（高于 zOPEN）。
CC 引脚以及 Charge-Through 端口 CC1 和 CC2 引脚上。

通过 VCONN 充电的 USB 设备应确保其完全由 VBUS 供电。

4.5.2.2.25.2 退出 CTDisabled.VPD

通过 VCONN 充电的 USB 设备应在 tVPDDisable 之后转换为 Unattached.SNK。

4.5.2.2.26 CTUnattached.SNK 状态

该状态如图 4-14、图 4-16 和图 4-17 所示。

当处于 CTUnattached.SNK 状态时，端口已检测到它已连接到通过 VCONN 充电的 USB 设备，并且如果电源已连接到通过 VCONN 充电的 USB 设备，则端口已准备就绪。

也可能通过断开充电电源进入此状态。

4.5.2.2.26.1 CTUnattached.SNK 要求

进入此状态后，端口应移除其 Rp 终端（如果存在）并通过 Rd 将 CC 终止于地。

该端口应继续向 VCONN 供电。

该端口应停止供应或吸收 VBUS 并将其放电。

在 *USB PD* 版本 2.0 中，端口应充当总线主机，以启动 PD 消息。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The port may query the state of the attached VCONN-Powered USB Device by sending SOP' messages on *USB PD* to read the VPD's eMarker.

4.5.2.2.26.2 Exiting from CTUnattached.SNK

The port shall transition to CTAttached.SNK when VBUS is detected. Note that by this point, the VCONN-Powered USB Device has already de-bounced the passed-through CC pin.

The port shall transition to Unattached.SNK if the state of the CC pin is SNK.Open for tVPDDetach after VBUS is vSafe0V.

4.5.2.2.27 CTAttached.SNK State

This state appears in Figure 4-14, Figure 4-16 and Figure 4-17.

When in the CTAttached.SNK state, the port is connected to a Charge-Through VCONN-Powered USB Device, which in turn is passing through the connection to a Power Source.

4.5.2.2.27.1 CTAttached.SNK Requirements

The port shall continue to terminate CC to ground through Rd. Since there is now a Power Source connected through to VBUS and CC, the port shall operate in one of the Sink Power Sub-States shown in Figure 4-19, and remain within the Sink Power Sub-States, until either VBUS is removed or a *USB PD* contract is established with the source.

The port shall not negotiate a voltage on VBUS higher than the maximum voltage specified in the Charge-Through VCONN-Powered USB Device's Discover Identity Command response.

The port shall continue to supply VCONN.

The port shall reject a VCONN swap request.

The port shall not perform *USB BC 1.2* primary detection, as that will interfere with VPD functionality.

In *USB PD* Version 2.0, the port shall act as a bus slave for the purposes of initiating *USB PD* messages, although it remains a DFP for USB data.

The port shall neither initiate nor respond to any SOP' communication.

The port shall meet the Sink Power Sub-State requirements specified in Section 4.5.2.2.29.

The port shall meet the additional maximum current constraints described in Section 4.6.2.5.

The port shall follow the restrictions on *USB PD* messages described in Section 4.10.2.

The port shall alter its advertised capabilities to UFP role/sink only role as described in Section 4.10.2.

4.5.2.2.27.2 Exiting from CTAttached.SNK

A port that is not in the process of a *USB PD* Hard Reset shall transition to CTUnattached.SNK within tSinkDisconnect when VBUS falls below vSinkDisconnect for VBUS operating at or below 5 V or below vSinkDisconnectPD when negotiated by *USB PD* to operate above 5 V.

A port that has entered into *USB PD* communications with the Source and has seen the CC voltage exceed vRd-USB may monitor the CC pin to detect cable disconnect in addition to monitoring VBUS.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

端口可以通过在 *USB PD* 上发送 SOP 消息来读取 VPD 的 eMarker，从而查询所连接的 VCONN 供电 USB 设备的状态。

4.5.2.2.26.2 退出 CTUnattached.SNK

当检测到 VBUS 时，端口应转换到 CTAttached.SNK。请注意，此时，VCONN 供电的 USB 设备已消除了直通 CC 引脚的抖动。

如果 VBUS 为 vSafe0V 后 CC 引脚的状态为 SNK.Open，则端口应在 tVPDDetach 内转换为 Unattached.SNK。

4.5.2.2.27 CTAttached.SNK 状态

该状态如图 4-14、图 4-16 和图 4-17 所示。

当处于 CTAttached.SNK 状态时，端口连接到通过 VCONN 充电的 USB 设备，该设备又通过连接连接到电源。

4.5.2.2.27.1 CTAttached.SNK 要求

端口应继续通过 Rd 将 CC 终止于地。由于现在有一个电源连接到 VBUS 和 CC，端口应在图 4-19 所示的其中一个 Sink 电源子状态中运行，并保持在 Sink 电源子状态中，直到 VBUS 被移除或与电源建立 *USB PD* 合同。

端口协商的 VBUS 电压不得高于通过 VCONN 充电的 USB 设备的发现身份命令响应中指定的最大电压。

该端口应继续向 VCONN 供电。

端口应拒绝 VCONN 交换请求。

端口不得执行 *USB BC 1.2* 主要检测，因为这会干扰 VPD 功能。

在 *USB PD* 版本 2.0 中，该端口应充当总线从属设备，以启动 *USB PD* 消息，尽管它仍然是 USB 数据的 DFP。

端口不得发起或响应任何 SOP 通信。

该端口应满足第 4.5.2.2.29 节规定的 Sink Power Sub-State 要求。

该端口应满足第 4.6.2.5 节描述的额外最大电流限制。

该端口应遵循第 4.10.2 节中描述的对 *USB PD* 消息的限制。

端口应将其通告的能力更改为 UFP 角色/仅接收器角色，如第 4.10.2 节所述。

4.5.2.2.27.2 退出 CTAttached.SNK

当 VBUS 降至低于 vSinkDisconnect（对于在 5 V 或以下运行的 VBUS）或低于 vSinkDisconnectPD（当由 *USB PD* 协商为在 5 V 以上运行时）时，未处于 *USB PD* 硬重置过程中的端口应在 tSinkDisconnect 内转换为 CTUnattached.SNK。

已与源进入 *USB PD* 通信且发现 CC 电压超过 vRd-USB 的端口除了监控 VBUS 之外，还可以监控 CC 引脚以检测电缆断开连接。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A port that is monitoring the CC voltage for disconnect shall transition to CTUnattached.SNK within tSinkDisconnect after the CC voltage remains below vRd-USB for tPDDebounce.

4.5.2.2.28 CTUnattached.Unsupported State

This state appears in Figure 4-18.

When in the CTUnattached.Unsupported state, the Charge-Through VCONN-Powered USB Device has previously detected SNK.Open on its host port for tVPDCTDD, indicating that it is connected to a Charge-Through Capable Source, and is now monitoring its Charge-Through port for the presence of an unsupported sink.

A Charge-Through VCONN-Powered USB Device does not support Sinks, Debug Accessory Mode, or Audio Adapter Accessory Mode.

4.5.2.2.28.1 CTUnattached.Unsupported Requirements

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (*USB 3.2*) / ICCSH (*USB 2.0*) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

Upon entry into this state, the Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising 3.0 A on the Host-side port's CC pin, remove its Rd terminations to ground on the Charge-Through port's CC1 and CC2 pins, and provide a Rp termination advertising Default USB Power instead.

The Charge-Through VCONN-Powered USB Device shall only respond to *USB PD* Discover Identity queries on SOP' on its Host-side port. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in *USB PD*.

4.5.2.2.28.2 Exiting from CTUnattached.Unsupported

The Charge-Through VCONN-Powered USB Device shall transition to CTAttachWait.Unsupported when a Sink connection is detected on the Charge-Through port, as indicated by the SRC.Rd state on at least one of the Charge-Through port's CC pins or SRC.Ra state on both the CC1 and CC2 pins.

The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDisconnect.

Otherwise, a Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD within tDRPTransition after dcSRC.DRP · tDRP, or if directed.

4.5.2.2.29 CTAttachWait.Unsupported State

This state appears in Figure 4-18.

The CTAttachWait.Unsupported state is used to ensure that the state of both the Charge-Through Port's CC1 and CC2 pins are stable for at least tCCDebounce.

4.5.2.2.29.1 CTAttachWait.Unsupported Requirements

The requirements for this state are identical to CTUnattached.Unsupported state.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

当 CC 电压在 tPDDebounce 时间内保持低于 vRd-USB 时，监控 CC 电压是否断开的端口应在 tSinkDisconnect 时间内转换至 CTUnattached.SNK。

4.5.2.2.28 CTUnattached.Unsupported 状态

此状态如图 4-18 所示。

当处于 CTUnattached.Unsupported 状态时，由 VCONN 供电的充电直通 USB 设备先前已在其主机端口上检测到 SNK.Open 并持续 tVPDCTDD，这表明它已连接到具有充电直通能力的源，并且现在正在监控其充电直通端口是否存在不受支持的接收端。

通过 VCONN 充电的 USB 设备不支持接收器、调试附件模式或音频适配器附件模式。

4.5.2.2.28.1 CTUnattached.不支持的要求

通过 VCONN 充电的 USB 设备应将其主机端端口与其通过 VCONN 充电的端口隔离，包括 CC 和 VBUS。通过 VCONN 充电的 USB 设备应确保其由 VCONN 供电，不会从 VBUS 消耗超过 ICCS (*USB 3.2*)/ICCSH (*USB 2.0*) 的电量进行监控，并且与 VBUS 充分隔离以承受通过 VCONN 充电操作期间的高电压。

进入此状态后，通过 VCONN 充电的 USB 设备应保持其在主机端端口的 CC 引脚上，Rp 终端通告 3.0 A，移除充电端口的 CC1 和 CC2 引脚上将其 Rd 终端接地，并提供一个 Rp 终端通告默认 USB 电源。

通过 VCONN 充电的 USB 设备应仅响应其主机端端口上 SOP 上的 *USB PD* 发现身份查询。它应确保主机端端口 CC 上有足够的电容来满足 *USB PD* 中定义的 cReceiver。

4.5.2.2.28.2 退出 CTUnattached.Unsupported

当在 Charge-Through 端口上检测到 Sink 连接时，Charge-Through VCONN 供电 USB 设备应转换为 CTAttachWait.Unsupported，这可由 Charge-Through 端口的至少一个 CC 引脚上的 SRC.Rd 状态或 CC1 和 CC2 引脚上的 SRC.Ra 状态指示。

如果 VCONN 低于 vVCONNDisconnect，则通过 VCONN 充电的 USB 设备应转换为 Unattached.SNK。

否则，通过 VCONN 充电的 USB 设备应在 dcSRC.DRP · tDRP 之后的 tDRPTransition 内转换至 CTUnattached.VPD，或者根据指示转换。

4.5.2.2.29 CTAttachWait.Unsupported 状态

此状态如图 4-18 所示。

CTAttachWait.Unsupported 状态用于确保充电端口的 CC1 和 CC2 引脚的状态至少在 tCCDebounce 内保持稳定。

4.5.2.2.29.1 CTAttachWait.不支持的要求 国家标准要求

此状态的 ts 与 CTUnattached.Unsupp 相同 排序状态。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.29.2 Exiting from CTAttachWait.Unsupported

The Charge-Through VCONN-Powered USB Device shall transition to CTTry.SNK if the state of at least one of the Charge-Through port's CC pins is SRC.Rd, or if the state of both the CC1 and CC2 pins is SRC.Ra for at least tCCDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when the state of either the Charge-Through Port's CC1 or CC2 pin is SRC.Open for at least tCCDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDisconnect.

4.5.2.2.30 CTTry.SNK State

This state appears in Figure 4-18.

When in the CTTry.SNK state, the Charge-Through VCONN-Powered USB Device is querying to determine if the port partner on the Charge-Through port supports the source role.

4.5.2.2.30.1 CTTry.SNK Requirements

The requirements for this state is identical to CTUnattached.VPD state.

4.5.2.2.30.2 Exiting from CTTry.SNK

The Charge-Through VCONN-Powered USB Device shall wait for tDRPTry and only then begin monitoring the Charge-Through port's CC pins for the SNK.Rp state.

The Charge-Through VCONN-Powered USB Device shall then transition to CTAttached.VPD when the SNK.Rp state is detected on the Charge-Through port's CC pins for at least tTryCCDebounce and VBUS is detected on Charge-Through port.

A Charge-Through VCONN-Powered USB Device shall transition to CTAttached.Unsupported if SNK.Rp state is not detected for tDRPTryWait.

Note: The Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on both the CC1 and CC2 pins, but this event will not exceed tTryCCDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDisconnect.

4.5.2.2.31 CTAttached.Unsupported State

This state appears in Figure 4-18.

If the port partner to the Charge-Through VCONN-Powered USB Device's Charge-Through port either does not support the source power role, or failed to negotiate the source role, the CTAttached.Unsupported state is used to wait until that device is unplugged before continuing.

4.5.2.2.31.1 CTAttached.Unsupported Requirements

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (*USB 3.2*) / ICCSH (*USB 2.0*) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.29.2 退出 CTAttachWait.Unsupported

如果至少有一个 Charge-Through 端口的 CC 引脚的状态为 SRC.Rd，或者 CC1 和 CC2 引脚的状态均为 SRC.Ra，并且持续时间至少为 tCCDebounce，则 Charge-Through VCONN 供电 USB 设备应转换为 CTTry.SNK。

当充电端口的 CC1 或 CC2 引脚的状态为 SRC.Open 至少持续 tCCDebounce 时，充电 VCONN 供电 USB 设备应转换为 CTUnattached.VPD。

如果 VCONN 低于 vVCONNDisconnect，则通过 VCONN 充电的 USB 设备应转换为 Unattached.SNK。

4.5.2.2.30 CTTry.SNK 状态

此状态如图 4-18 所示。

当处于 CTTry.SNK 状态时，通过 VCONN 供电的 Charge-Through USB 设备正在查询以确定 Charge-Through 端口上的端口伙伴是否支持源角色。

4.5.2.2.30.1 CTTry.SNK 要求

此状态的要求与 CTUnattached.VPD 状态相同。

4.5.2.2.30.2 退出 CTTry.SNK

通过 VCONN 充电的 USB 设备应等待 tDRPTry，然后才开始监控通过 VCONN 充电端口的 CC 引脚的 SNK.Rp 状态。

当在 Charge-Through 端口的 CC 引脚上检测到 SNK.Rp 状态至少持续 tTryCCDebounce 并且在 Charge-Through 端口上检测到 VBUS 时，Charge-Through VCONN 供电 USB 设备应转换到 CTAttached.VPD。

如果在 tDRPTryWait 期间未检测到 SNK.Rp 状态，则通过 VCONN 供电的 USB 设备将转换为 CTAttached.Unsupported。

注意：源可能会启动 *USB PD* 通信，这将导致 CC1 和 CC2 引脚上出现短暂的 SNK.Open 状态，但此事件不会超过 tTryCCDebounce。

如果 VCONN 低于 vVCONNDisconnect，则通过 VCONN 充电的 USB 设备应转换为 Unattached.SNK。

4.5.2.2.31 CTAttached.Unsupported 状态

此状态如图 4-18 所示。

如果通过 VCONN 供电的 USB 设备的充电端口的端口伙伴不支持源电源角色，或者无法协商源角色，则使用 CTAttached.Unsupported 状态等待，直到该设备拔出后再继续。

4.5.2.2.31.1 CTAttached.不支持的要求

通过 VCONN 充电的 USB 设备应将其主机端端口与其通过 VCONN 充电的端口隔离，包括 CC 和 VBUS。通过 VCONN 充电的 USB 设备应确保其由 VCONN 供电，不会从 VBUS 消耗超过 ICCS (*USB 3.2*)/ICCSH (*USB 2.0*) 的电量进行监控，并且与 VBUS 充分隔离以承受通过 VCONN 充电操作期间的高电压。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Upon entry into this state, the Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising 3.0 A on the Host-side port's CC pin, remove its Rd terminations to ground on the Charge-Through port's CC1 and CC2 pins, and provide a Rp termination advertising Default USB Power instead.

At least one of the CC1 or CC2 pins will be in the SRC.Rd state or both will be in the SRC.Ra state. The Charge-Through port shall advertise Default USB Power (see Table 4-24) on its CC pins and monitor their voltage.

The Charge-Through VCONN-Powered USB Device shall present a USB Billboard Device Class interface indicating that it does not recognize or support the attached accessory or device.

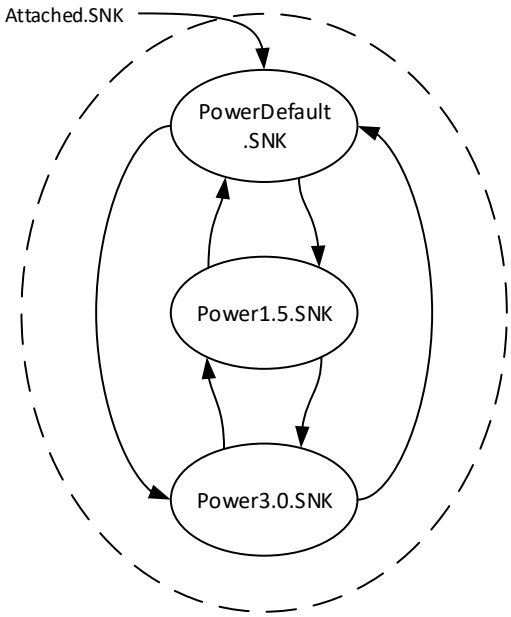
4.5.2.2.31.2 Exiting from CTAttached.Unsupported

The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when SRC.Open state is detected on both the Charge-Through port's CC pins or the SRC.Open state is detected on one CC pin and SRC.Ra is detected on the other CC pin.

4.5.2.3 Sink Power Sub-State Requirements

When in the Attached.SNK or CTAttached.SNK states and the Source is supplying default VBUS, the port shall operate in one of the sub-states shown in Figure 4-19. The initial Sink Power Sub-State is PowerDefault.SNK. Subsequently, the Sink Power Sub-State is determined by Source's USB Type-C current advertisement. The port in Attached.SNK shall remain within the Sink Power Sub-States until either VBUS is removed or a *USB PD* contract is established with the Source.

Figure 4-19 Sink Power Sub-States



The Sink is only required to implement Sink Power Sub-State transitions if the Sink wants to consume more than default USB current.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

进入此状态后，通过 VCONN 供电的充电 USB 设备应维持其在主机端端口的 CC 引脚上通告 3.0 A 的 Rp 终端，移除在充电端口的 CC1 和 CC2 引脚上通告接地的 Rd 终端，并提供一个通告默认 USB 电源的 Rp 终端。

CC1 或 CC2 引脚中至少有一个将处于 SRC.Rd 状态，或者两个引脚都将处于 SRC.Ra 状态。Charge-Through 端口应在其 CC 引脚上通告默认 USB 电源（见表 4-24）并监控其电压。

通过 VCONN 充电的 USB 设备应显示 USB 公告牌设备类接口，表明它不识别或支持所连接的配件或设备。

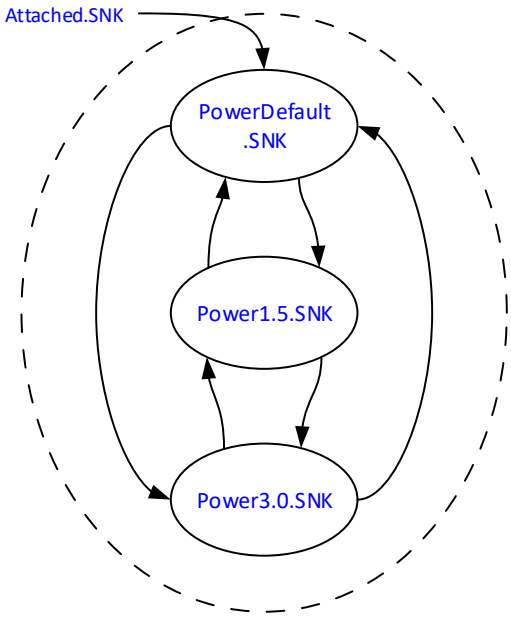
4.5.2.2.31.2 退出 CTAttached.Unsupported

当在两个 Charge-Through 端口的 CC 引脚上都检测到 SRC.Open 状态，或者在一个 CC 引脚上检测到 SRC.Open 状态并在另一个 CC 引脚上检测到 SRC.Ra 时，Charge-Through VCONN 供电 USB 设备应转换至 CTUnattached.VPD。

4.5.2.3 接收器电源子状态要求

当处于 Attached.SNK 或 CTAttached.SNK 状态且源提供默认 VBUS 时，端口应在图 4-19 所示的子状态之一中运行。初始 Sink 电源子状态为 PowerDefault.SNK。随后，Sink 电源子状态由源的 USB Type-C 电流通告决定。处于 Attached.SNK 的端口应保持在 Sink 电源子状态中，直到 VBUS 被移除或与源建立 *USB PD* 合同。

图 4-19 接收器电源子状态



仅当 Sink 想要消耗超过默认 USB 电流时，Sink 才需要实现 Sink 电源子状态转换。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Note that for the CTAttached.SNK state, there are further limitations on maximum current (see Section 4.6.2.5).

4.5.2.3.1 PowerDefault.SNK Sub-State

This sub-state supports Sinks consuming current within the lowest range (default) of Source-supplied current.

4.5.2.3.1.1 PowerDefault.SNK Requirements

The port shall draw no more than the default USB power from VBUS. See Section 4.6.2.1.

If the port wants to consume more than the default USB power, it shall monitor vRd to determine if more current is available from the Source.

4.5.2.3.1.2 Exiting from PowerDefault.SNK

For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tRpValueChange.

For a vRd in the vRd-1.5 range, the port shall transition to the Power1.5.SNK Sub-State.

For a vRd in the vRd-3.0 range, the port shall transition to the Power3.0.SNK Sub-State.

4.5.2.3.2 Power1.5.SNK Sub-State

This sub-state supports Sinks consuming current within the two lower ranges (default and 1.5 A) of Source-supplied current.

4.5.2.3.2.1 Power1.5.SNK Requirements

The port shall draw no more than 1.5 A from VBUS.

The port shall monitor vRd while it is in this sub-state.

4.5.2.3.2.2 Exiting from Power1.5.SNK

For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tRpValueChange.

For a vRd in the vRd-USB range, the port shall transition to the PowerDefault.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

For a vRd in the vRd-3.0 range, the port shall transition to the Power3.0.SNK Sub-State.

4.5.2.3.3 Power3.0.SNK Sub-State

This sub-state supports Sinks consuming current within all three ranges (default, 1.5 A and 3.0 A) of Source-supplied current.

4.5.2.3.3.1 Power3.0.SNK Requirements

The port shall draw no more than 3.0 A from VBUS.

The port shall monitor vRd while it is in this sub-state.

4.5.2.3.3.2 Exiting from Power3.0.SNK

For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tRpValueChange.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

请注意，对于 CTAttached.SNK 状态，最大电流有进一步的限制（参见第 4.6.2.5 节）。

4.5.2.3.1 PowerDefault.SNK 子状态

该子状态支持接收器消耗源供电电流最低范围（默认）内的电流。

4.5.2.3.1.1 PowerDefault.SNK 要求

端口从 V BUS 获得的功率不得超过默认 USB 功率。请参阅第 4.6.2.1 节。

如果端口要消耗超过默认 USB 功率，它应监控 vRd 以确定源端是否有更多电流可用。

4.5.2.3.1.2 退出 PowerDefault.SNK

对于指示允许功率变化的任何 vRd 变化，端口不得转换，直到新的 vRd 至少稳定 tRpValueChange。

对于 vRd-1.5 范围内的 vRd，端口应转换到 Power1.5.SNK 子状态。

对于 vRd-3.0 范围内的 vRd，端口应转换到 Power3.0.SNK 子状态。

4.5.2.3.2 Power1.5.SNK 子状态

该子状态支持接收器消耗源供电电流的两个较低范围（默认和 1.5 A）内的电流。

4.5.2.3.2.1 Power1.5.SNK 要求

该端口从 VBUS 吸取的电流不得超过 1.5 A。

当端口处于此子状态时，它应监视 vRd。

4.5.2.3.2.2 退出 Power1.5.SNK

对于指示允许功率变化的任何 vRd 变化，端口不得转换，直到新的 vRd 至少稳定 tRpValueChange。

对于 vRd-USB 范围内的 vRd，端口应转换到 PowerDefault.SNK 子状态并将其功耗降低到 tSinkAdj 内的新范围。

对于 vRd-3.0 范围内的 vRd，端口应转换到 Power3.0.SNK 子状态。

4.5.2.3.3 Power3.0.SNK 子状态

该子状态支持接收器消耗源供电电流的所有三个范围（默认、1.5 A 和 3.0 A）内的电流。

4.5.2.3.3.1 Power3.0.SNK 要求

该端口从 VBUS 吸取的电流不得超过 3.0 A。

当端口处于此子状态时，它应监视 vRd。

4.5.2.3.3.2 退出 Power3.0.SNK

对于指示允许功率变化的任何 vRd 变化，端口不得转换，直到新的 vRd 至少稳定 tRpValueChange。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

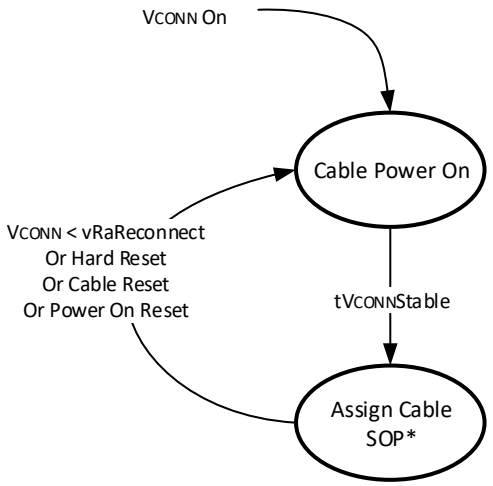
For a vRd in the vRd-USB range, the port shall transition to the PowerDefault.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

For a vRd in the vRd-1.5 range, the port shall transition to the Power1.5.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

4.5.2.4 Cable State Machine Requirements

Figure 4-20 illustrates the cable eMarker connection state diagram.

Figure 4-20 Cable eMarker State Diagram



4.5.2.4.1 Cable Power On State

This state appears in Figure 4-20. This is the initial power on state for each eMarker in the cable when VCONN is applied.

4.5.2.4.1.1 Cable Power On State Requirements

Each eMarker in the cable shall present Ra when no VCONN is applied.

Each eMarker in the cable shall power on and may continue to present Ra in this state.

The cable shall not respond to SOP' and SOP" commands in this state.

4.5.2.4.1.2 Exiting from Cable Power On State

Each eMarker in a passive or active cable shall transition to Assign Cable SOP* when it has completed its boot process. Each eMarker shall transition to Assign Cable SOP* within tVCONNStable.

4.5.2.4.2 Assign Cable SOP* State

This state appears in Figure 4-20.

Typically, a passive cable has only one eMarker powered at a time. This cable eMarker in a passive cable shall respond to SOP' in this state. If two eMarkers are powered at the same time in a passive cable, then one shall respond to a pre-set SOP' and the other to SOP''.

Each cable eMarker in an active cable shall respond to a pre-set SOP' or SOP''. If only one eMarker exists in the cable, it shall only respond to SOP'.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

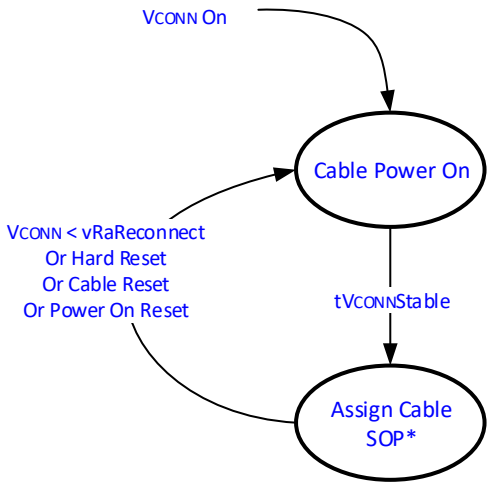
对于 vRd-USB 范围内的 vRd，端口应转换到 PowerDefault.SNK 子状态并将其功耗降低到 tSinkAdj 内的新范围。

对于 vRd-1.5 范围内的 vRd，端口应转换到 Power1.5.SNK 子状态并将其功耗降低到 tSinkAdj 内的新范围。

4.5.2.4 电缆状态机要求

图4-20为电缆eMarker连接状态图。

图 4-20 线缆 eMarker 状态图



4.5.2.4.1 电缆通电状态

此状态如图 4-20 所示。这是应用 VCONN 时电缆中每个 eMarker 的初始通电状态。

4.5.2.4.1.1 电缆通电状态要求

当未应用 VCONN 时，电缆中的每个 eMarker 都应显示 Ra。

电缆中的每个 eMarker 都应通电，并可在此状态下继续呈现 Ra。

在此状态下，电缆不得响应SOP ’ 和SOP ” 命令。

4.5.2.4.1.2 退出电缆通电状态

无源或有源电缆中的每个 eMarker 在其启动过程完成后都应转换为分配电缆 SOP*。每个 eMarker 都应在 tVCONNStable 内转换为分配电缆 SOP*。

4.5.2.4.2 分配电缆 SOP* 状态

此状态如图 4-20 所示。

通常，无源线缆一次只能为一个 eMarker 供电。无源线缆中的该线缆 eMarker 应在此状态下响应 SOP ’。如果无源线缆中同时为两个 eMarker 供电，则其中一个应响应预设的 SOP ’，另一个应响应 SOP ’ ’。

有源电缆中的每个电缆 eMarker 都应响应预设的 SOP ’ 或 SOP ’ ’。如果电缆中只有一个 eMarker，则它仅应响应 SOP ’。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.4.2.1 Assign Cable SOP* State Requirements

Each eMarker in the passive or active cable shall be able to respond to any *USB PD* communication sent to its pre-set SOP' or SOP''. For a passive cable, only one eMarker should be powered at a time and shall respond to SOP' only. If two eMarkers exist in a passive or active cable and are powered at the same time, then only one shall respond to SOP' and the other shall respond to SOP''. The assignment of SOP' and SOP'' is fixed for each eMarker in a cable and shall not be dynamically set when power is applied to VCONN.

Each eMarker in the cable shall weaken or remove Ra if it has not already done so.

Passive cables shall meet the Power for electronically marked passive cables defined in Table 4-6.

Active Cables shall meet the Power for Active cables in Table 4-6.

4.5.2.4.2.2 Exiting from Assign Cable SOP* State

Each eMarker in the cable shall transition to Cable Power On upon sensing VCONN less than vRaReconnect or upon a Power On Reset event.

Each eMarker in the cable shall transition to Cable Power On upon sensing a Hard Reset or Cable Reset.

4.5.2.5 Connection States Summary

Table 4-16 defines the mandatory and optional states for each type of port.

Table 4-16 Mandatory and Optional States

	SOURCE	SINK	DRP	USB PD Communication
Disabled	Optional	Optional	Optional	Not Permitted
ErrorRecovery	Mandatory[10]	Mandatory[10]	Mandatory[10]	Not Permitted
Unattached.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachWait.SNK	N/A	Mandatory[1]	Mandatory	Not Permitted
Attached.SNK	N/A	Mandatory	Mandatory	Permitted
UnattachedWait.SRC	Mandatory or N/A[7]	N/A	N/A	Not Permitted
Unattached.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachWait.SRC	Mandatory	N/A	Mandatory	Not Permitted
Attached.SRC	Mandatory	N/A	Mandatory	Permitted
Try.SRC[4]	N/A	N/A	Optional	Not Permitted
TryWait.SNK[2]	N/A	N/A	Optional	Not Permitted
Try.SNK[4, 8]	N/A	N/A	Optional	Not Permitted
TryWait.SRC[5, 8]	N/A	N/A	Optional	Not Permitted
AudioAccessory	Optional	Optional	Optional	Not Permitted
UnorientedDebugAccessory.SRC	Optional[6]	N/A	Optional[6]	Not Permitted
OrientedDebugAccessory.SRC	Optional[6]	N/A	Optional[6]	Permitted
DebugAccessory.SNK	N/A	Optional	Optional	Permitted

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.2.4.2.1 分配电缆 SOP* 状态要求

无源或有源电缆中的每个 eMarker 都应能够响应发送到其预设 SOP ’ 或 SOP ” 的任何 *USB PD* 通信。对于无源电缆，一次只能给一个 eMarker 供电，并且只能响应 SOP ’。如果无源或有源电缆中有两个 eMarker 并且同时供电，则只有一个响应 SOP ’，另一个响应 SOP ”。电缆中每个 eMarker 的 SOP ’ 和 SOP ” 分配都是固定的，当 V CONN 通电时不能动态设置。

如果电缆中的每个 eMarker 尚未削弱或移除 Ra，则应削弱或移除 Ra。

无源电缆应满足表 4-6 定义的电子标记无源电缆的功率。

活动 e 电缆应满足表中有源电缆的功率要求 4-6。

4.5.2.4.2.2 退出分配电缆 SOP* 状态

当感测到 VCONN 小于 vRaReconnect 或发生开机复位事件时，电缆中的每个 eMarker 都应转换为电缆开机。

当感测到硬重置或电缆重置时，电缆中的每个 eMarker 都应转换到电缆通电状态。

4.5.2.5 连接状态摘要

表 4-16 定义了每种端口类型的强制状态和可选状态。

表 4-16 强制和可选状态

	SOURCE	SINK	DRP	USB PD Communication
Disabled	Optional	Optional	Optional	Not Permitted
ErrorRecovery	Mandatory[10]	Mandatory[10]	Mandatory[10]	Not Permitted
Unattached.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachWait.SNK	N/A	Mandatory[1]	Mandatory	Not Permitted
Attached.SNK	N/A	Mandatory	Mandatory	Permitted
UnattachedWait.SRC	Mandatory or N/A[7]	N/A	N/A	Not Permitted
Unattached.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachWait.SRC	Mandatory	N/A	Mandatory	Not Permitted
Attached.SRC	Mandatory	N/A	Mandatory	Permitted
Try.SRC[4]	N/A	N/A	Optional	Not Permitted
TryWait.SNK[2]	N/A	N/A	Optional	Not Permitted
Try.SNK[4, 8]	N/A	N/A	Optional	Not Permitted
TryWait.SRC[5, 8]	N/A	N/A	Optional	Not Permitted
AudioAccessory	Optional	Optional	Optional	Not Permitted
UnorientedDebugAccessory.SRC	Optional[6]	N/A	Optional[6]	Not Permitted
OrientedDebugAccessory.SRC	Optional[6]	N/A	Optional[6]	Permitted
DebugAccessory.SNK	N/A	Optional	Optional	Permitted

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

	SOURCE	SINK	DRP	USB PD Communication
Unattached.Accessory	N/A	Optional	N/A	Not Permitted
AttachWait.Accessory	N/A	Optional	N/A	Not Permitted
PoweredAccessory	N/A	Optional	N/A	Permitted
Unsupported.Accessory[3]	N/A	Optional	N/A	Not Permitted
CTUnattached.VPD	N/A	N/A	Optional	SOP' Permitted
CTAttachWait.VPD[8]	N/A	N/A	Optional	SOP' Permitted
CTAttached.VPD[8]	N/A	N/A	Optional	Not Permitted
CTDisabled.VPD[8]	N/A	N/A	Optional	Not Permitted
CTUnattached.SNK	N/A	N/A	Optional	SOP' Permitted
CTAttached.SNK[9]	N/A	N/A	Optional	Permitted
CTUnattached.Unsupported[8]	N/A	N/A	Optional	SOP' Permitted
CTAttachWait.Unsupported[8]	N/A	N/A	Optional	SOP' Permitted
CTTry.SNK[8]	N/A	N/A	Optional	SOP' Permitted
CTAttached.Unsupported[8]	N/A	N/A	Optional	SOP' Permitted
PowerDefault.SNK	N/A	Mandatory	Mandatory	Permitted
Power1.5.SNK	N/A	Optional	Optional	Permitted
Power3.0.SNK	N/A	Optional	Optional	Permitted

Notes:

1. Optional for UFP applications that are USB 2.0-only, consume USB Default Power and do not support *USB PD* or accessories.
2. TryWait.SNK is mandatory when Try.SRC is supported.
3. Unsupported.Accessory is mandatory when PoweredAccessory is supported.
4. Try.SRC and Try.SNK shall not be supported at the same time, although an unattached device may dynamically choose between Try.SRC and Try.SNK state machines based on external factors.
5. TryWait.SRC is mandatory when Try.SNK is supported.
6. UnorientedDebugAccessory.SRC is required for any Source or DRP that supports Debug Accessory Mode. OrientedDebugAccessory.SRC is only required if orientation detection is necessary in Debug Accessory Mode.
7. Mandatory for a DFP that was providing VCONN in the previous Attached.SRC state. N/A for a DFP that was not providing VCONN in the previous Attached.SRC state.
8. CTAttachWait.VPD, CTAttached.VPD, CTDisabled.VPD, Try.SNK, TryWait.SRC, CTUnattached.Unsupported, CTAttachWait.Unsupported, CTAttached.Unsupported, and CTTry.SNK are mandatory when CTUnattached.VPD is supported.
9. CTAttached.SNK is mandatory when CTUnattached.SNK is supported.
10. Optional for non-*USB4* implementations.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

	SOURCE	SINK	DRP	USB PD Communication
Unattached.Accessory	N/A	Optional	N/A	Not Permitted
AttachWait.Accessory	N/A	Optional	N/A	Not Permitted
PoweredAccessory	N/A	Optional	N/A	Permitted
Unsupported.Accessory[3]	N/A	Optional	N/A	Not Permitted
CTUnattached.VPD	N/A	N/A	Optional	SOP' Permitted
CTAttachWait.VPD[8]	N/A	N/A	Optional	SOP' Permitted
CTAttached.VPD[8]	N/A	N/A	Optional	Not Permitted
CTDisabled.VPD[8]	N/A	N/A	Optional	Not Permitted
CTUnattached.SNK	N/A	N/A	Optional	SOP' Permitted
CTAttached.SNK[9]	N/A	N/A	Optional	Permitted
CTUnattached.Unsupported[8]	N/A	N/A	Optional	SOP' Permitted
CTAttachWait.Unsupported[8]	N/A	N/A	Optional	SOP' Permitted
CTTry.SNK[8]	N/A	N/A	Optional	SOP' Permitted
CTAttached.Unsupported[8]	N/A	N/A	Optional	SOP' Permitted
PowerDefault.SNK	N/A	Mandatory	Mandatory	Permitted
Power1.5.SNK	N/A	Optional	Optional	Permitted
Power3.0.SNK	N/A	Optional	Optional	Permitted

笔记：

1. 对于仅支持 USB 2.0、消耗 USB 默认电源且不支持 *USB PD* 或附件的 UFP 应用程序，这是可选项。2. 当支持 Try.SRC 时，TryWait.SNK 是必需的。3. 当支持 PoweredAccessory 时，Unsupported.Accessory 是必需的。4. Try.SRC 和 Try.SNK 不得同时受支持，尽管未连接的设备可以根据外部因素在 Try.SRC 和 Try.SNK 状态机之间动态选择。5. 当支持 Try.SNK 时，TryWait.SRC 是必需的。6. 对于支持调试附件模式的任何源或 DRP，UnientedDebugAccessory.SRC 是必需的。仅当在调试附件模式下需要方向检测时，OrientedDebugAccessory.SRC 才是必需的。7. 对于在之前的 Attached.SRC 状态下提供 VCONN 的 DFP，这是必需的。对于在之前的 Attached.SRC 状态下未提供 VCONN 的 DFP，则不适用。8. CTAttachWait.VPD、CTAttached.VPD、CTDisabled.VPD、Try.SNK、TryWait.SRC、CTUnattached.Unsupported、CTAttachedWait.Unsupported、CTAttached.Unsupported 和 CTTry.SNK 在支持 CTUnattached.VPD 时为必需项。9. CTAttached.SNK 在支持 CTUnattached.SNK 时为必需项。10. 对于非 *USB4* 实现，则为可选项。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.3 USB Port Interoperability Behavior

This section describes interoperability behavior between USB Type-C to USB Type-C ports and between USB Type-C to legacy USB ports.

4.5.3.1 USB Type-C Port to USB Type-C Port Interoperability Behaviors

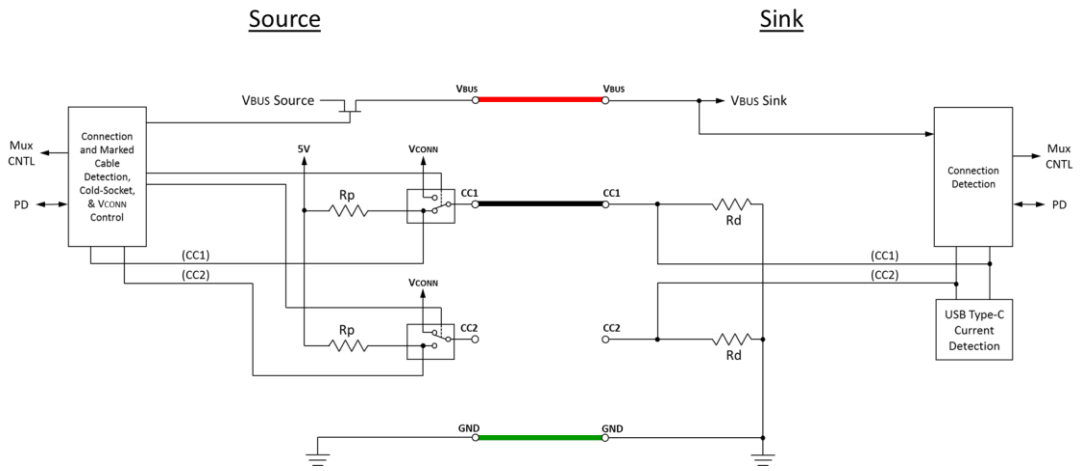
The following sub-sections describe typical port-to-port interoperability behaviors for the various combinations of USB Type-C Source, Sink and DRPs as presented in Table 4-9. In all of the described behaviors, the impact of *USB PD*-based swaps (PR_Swap, DR_Swap or VCONN_Swap) are not considered.

The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete.

4.5.3.1.1 Source to Sink Behavior

Figure 4-21 illustrates the functional model for a Source connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

Figure 4-21 Source to Sink Functional Model



The following describes the behavior when a Source is connected to a Sink.

1. Source and Sink in the unattached state
2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   - Source detects the Sink's pull-down on CC and enters Attached.SRC through AttachWait.SRC
   - Source turns on VBUS and VCONN
3. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK. Sink may skip AttachWait.SNK if it is USB 2.0 only and does not support accessories.
   - Sink detects VBUS and enters Attached.SNK through AttachWait.SNK
4. While the Source and Sink are in the attached state:
   - Source adjusts Rp as needed to limit the current the Sink may draw
   - Sink detects and monitors vRd for available current on VBUS
   - Source monitors CC for detach and when detected, enters Unattached.SRC
   - Sink monitors VBUS for detach and when detected, enters Unattached.SNK

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.3 USB 端口互操作性行为

本节介绍 USB Type-C 与 USB Type-C 端口之间以及 USB Type-C 与传统 USB 端口之间的互操作性行为。

4.5.3.1 USB Type-C 端口至 USB Type-C 端口互操作性行为

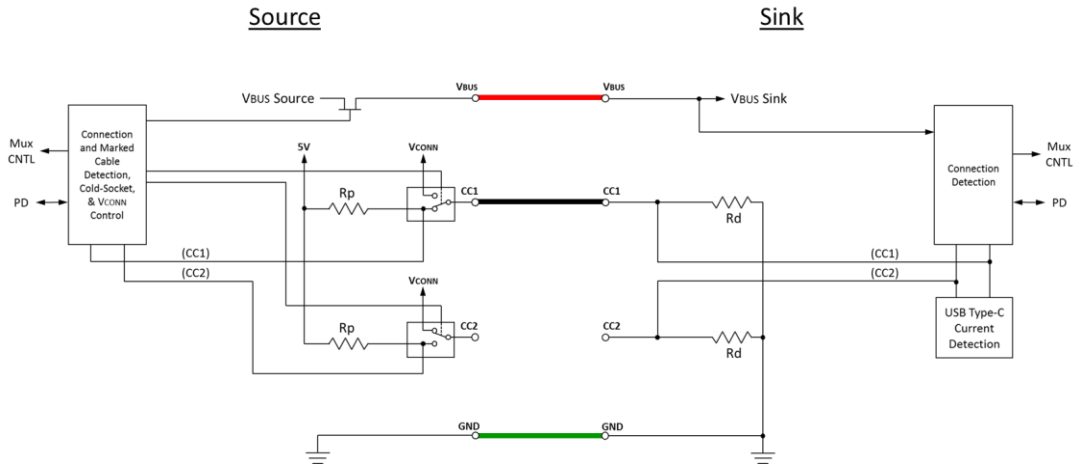
以下小节描述了表 4-9 中所示的各种 USB Type-C 源、接收器和 DRP 组合的典型端口到端口互操作性行为。在所有描述的行为中，均未考虑基于 *USB PD* 的交换（PR_Swap、DR_Swap 或 VCONN_Swap）的影响。

以下章节中的图说明了 CC 检测过程完成后的 CC1 和 CC2 路由。

4.5.3.1.1 源到接收器行为

图 4-21 说明了源端连接到接收器的功能模型。标准电缆中的单条 CC 线仅显示在四种可能的连接路线中的一种中，即 CC1 到 CC1。

图 4-21 源到汇功能模型



下面描述了当Source连接到Sink时的行为。

1. 源和接收器处于未连接状态 2. 源通过 AttachWait.SRC • 从 Unattached.SRC 转换为 Attached.SRC 源检测到接收器在 CC 上的下拉，并通过 AttachWait.SRC • 进入 Attached.SRC 源打开 VBUS 和 VCONN 3. 接收器通过 AttachWait.SNK 从 Unattached.SNK 转换为 Attached.SNK。如果接收器仅支持 USB 2.0 且不支持配件，则接收器可能会跳过 AttachWait.SNK

。

•Sink 检测到 VBUS，通过 AttachWait.SNK 进入 Attached.SNK

4. 当Source和Sink处于连接状态时：

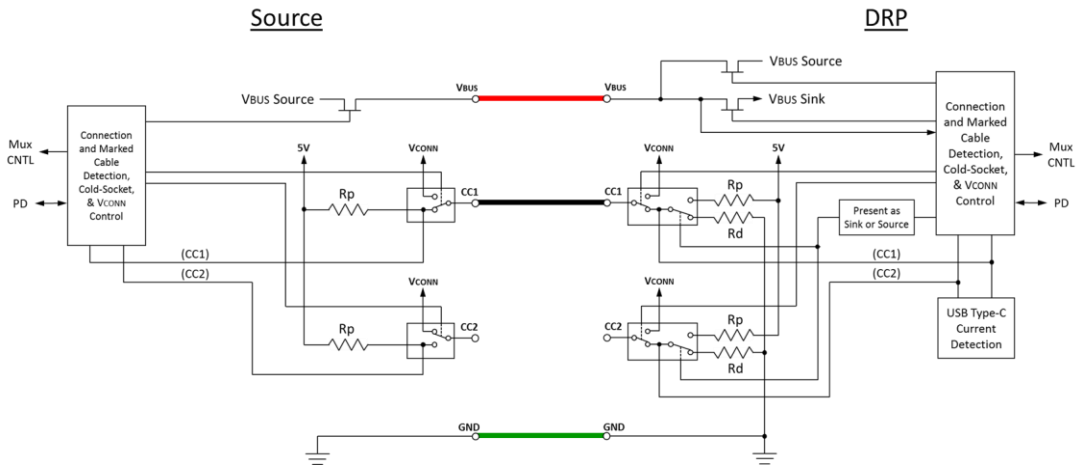
• 源端根据需要调整 Rp，以限制吸端可能吸收的电流 • 吸端检测并监控 vRd，以了解 VBUS 上的可用电流 • 源端监控 CC 是否断开，检测到断开后进入未连接状态。SRC • 吸端监控 VBUS 是否断开，检测到断开后进入未连接状态。SNK

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.3.1.2 Source to DRP Behavior

Figure 4-22 illustrates the functional model for a Source connected to a DRP. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

Figure 4-22 Source to DRP Functional Model



The following describes the behavior when a Source is connected to a DRP.

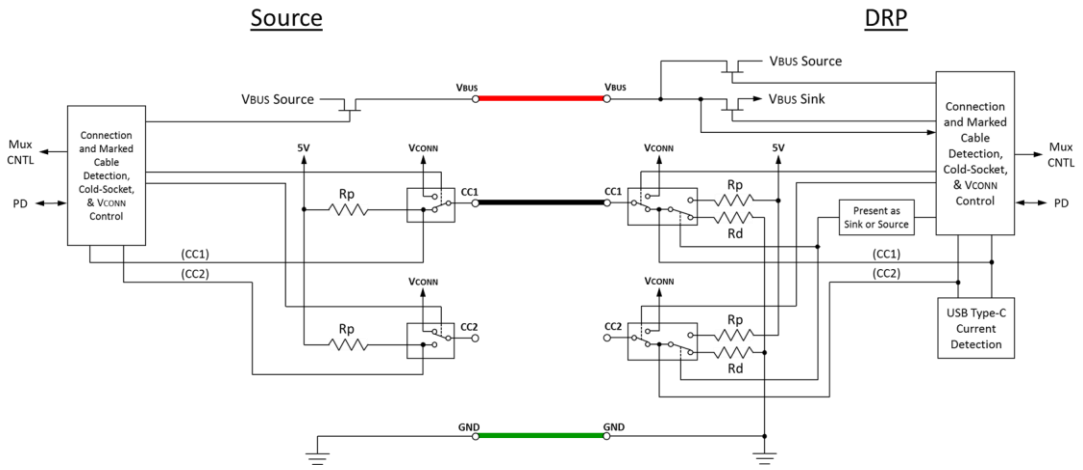
1. Source and DRP in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   - Source detects the DRP's pull-down on CC and enters AttachWait.SRC. After tCCDebounce it then enters Attached.SRC.
   - Source turns on VBUS and VCONN
3. DRP transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK
   - DRP in Unattached.SNK detects pull up on CC and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters Attached.SNK.
4. While the Source and DRP are in their respective attached states:
   - Source adjusts Rp as needed to limit the current the DRP (as Sink) may draw
   - DRP (as Sink) detects and monitors vRd for available current on VBUS
   - Source monitors CC for detach and when detected, enters Unattached.SRC
   - DRP (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.3.1.2 源到 DRP 行为

图 4-22 说明了连接到 DRP 的源的功能模型。标准电缆中的单条 CC 线仅显示在四种可能的连接路线之一中，即 CC1 到 CC1。

图 4-22 源到 DRP 功能模型



下面描述了源连接到 DRP 时的行为。

1. 源和 DRP 处于未连接状态 • DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替 2. 源通过 AttachWait.SRC 从 Unattached.SRC 转换为 Attached.SRC • 源检测到 DRP 在 CC 上的下拉并进入 AttachWait.SRC。tCCDebounce 之后，它进入 Attached.SRC。• 源打开 VBUS 和 VCONN 3. DRP 通过 AttachWait.SNK 从 Unattached.SNK 转换为 Attached.SNK • Unattached.SNK 中的 DRP 检测到 CC 上的上拉并进入 AttachWait.SNK。该状态持续 tCCDebounce 并检测到 VBUS 后，它进入 Attached.SNK。

4. 当源和 DRP 处于各自的连接状态时：

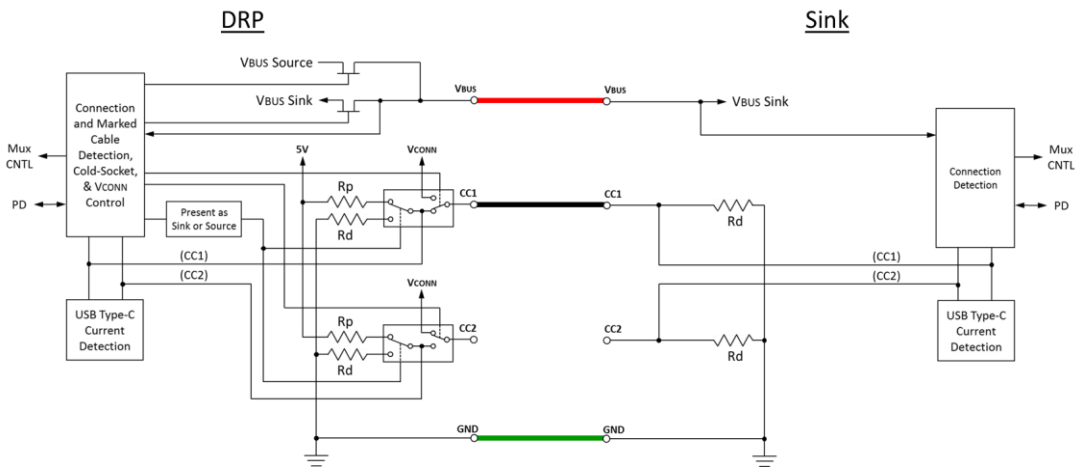
• 源端根据需要调整 Rp，以限制 DRP（作为吸端）可能吸收的电流 • DRP（作为吸端）检测并监控 vRd，以了解 VBUS 上的可用电流 • 源端监控 CC 是否断开，检测到断开后进入 Unattached.SRC • DRP（作为吸端）监控 VBUS 是否断开，检测到断开后进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换）

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.3.1.3 DRP to Sink Behavior

Figure 4-23 illustrates the functional model for a DRP connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

Figure 4-23 DRP to Sink Functional Model



The following describes the behavior when a DRP is connected to a Sink.

1. DRP and Sink in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. DRP transitions from Unattached.SRC to AttachWait.SRC to Attached.SRC
   - DRP in Unattached.SRC detects one of the CC pull-downs of Sink which is in Unattached.SNK and DRP enters AttachWait.SRC
   - DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and turns on VBUS and VCONN
3. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK if required.
   - Sink detects VBUS and enters Attached.SNK
4. While the DRP and Sink are in their respective attached states:
   - DRP (as Source) adjusts Rp as needed to limit the current the Sink may draw
   - Sink detects and monitors vRd for available current on VBUS
   - DRP (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)
   - Sink monitors VBUS for detach and when detected, enters Unattached.SNK

4.5.3.1.4 DRP to DRP Behavior

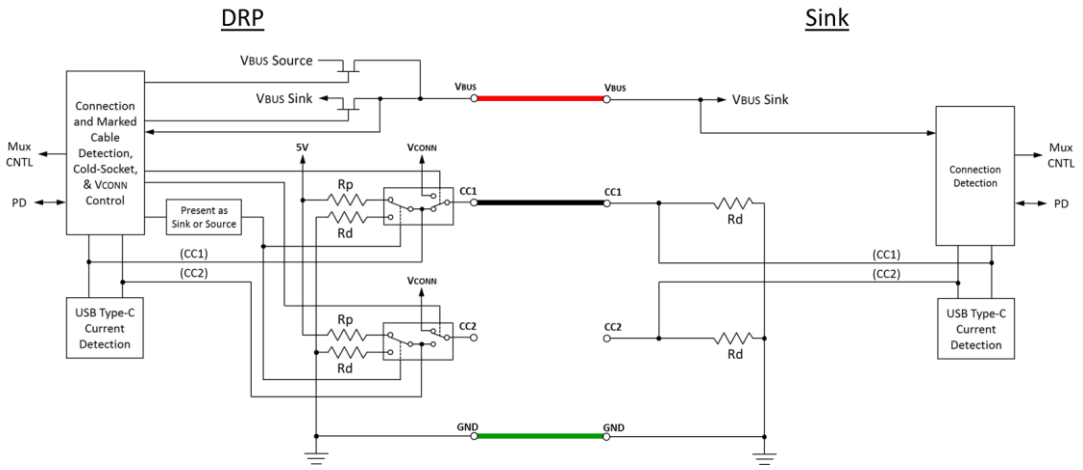
Two behavior descriptions based on the connection state diagrams are provided below. In the first case, the two DRPs accept the resulting Source-to-Sink relationship achieved randomly whereas in the second case the DRP #2 chooses to drive the random result to the opposite result using the Try.SRC mechanism.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.3.1.3 DRP 到接收器行为

图 4-23 说明了连接到接收器的 DRP 的功能模型。标准电缆中的单条 CC 线仅显示在四种可能的连接路线之一中，即 CC1 到 CC1。

图 4-23 DRP 到 Sink 功能模型



下面描述了DRP连接到Sink时的行为。

1. DRP 和 Sink 处于未连接状态 • DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替 2. DRP 从 Unattached.SRC 转换到 AttachWait.SRC 再到 Attached.SRC • Unattached.SRC 中的 DRP 检测到 Sink 的 CC 下拉之一，该 Sink 处于 Unattached.SNK 中，并且 DRP 进入 AttachWait.SRC • AttachWait.SRC 中的 DRP 检测到 CC 上的下拉持续了 tCCDebounce。

然后进入 Attached.SRC 并打开 VBUS 和 VCONN

3. 如果需要，Sink 通过 AttachWait.SNK 从 Unattached.SNK 转换到 Attached.SNK。

• Sink 检测 VBUS 并进入 Attached.SNK 4. 当 DRP 和 Sink 处于各自的连接状态时：• DRP（作为 Source）根据需要调整 Rp 以限制 Sink 可能吸收的电流 • Sink 检测并监控 vRd 以获取 VBUS 上的可用电流 • DRP（作为 Source）监控 CC 是否断开，检测到断开后，进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换）• Sink 监控 VBUS 是否断开，检测到断开后，进入 Unattached.SNK

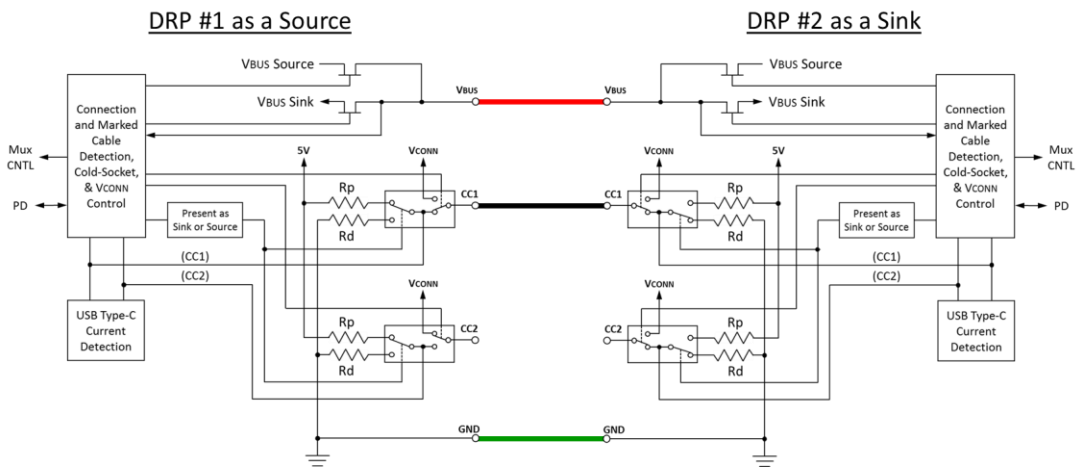
4.5.3.1.4 DRP 到 DRP 行为

下面基于连接状态图给出了两种行为描述。第一种情况下，两个 DRP 接受随机实现的 Source-to-Sink 关系，而第二种情况下，DRP #2 选择使用 Try.SRC 机制将随机结果驱动为相反的结果。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-24 illustrates the functional model for a DRP connected to a DRP in the first case described. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

Figure 4-24 DRP to DRP Functional Model – CASE 1



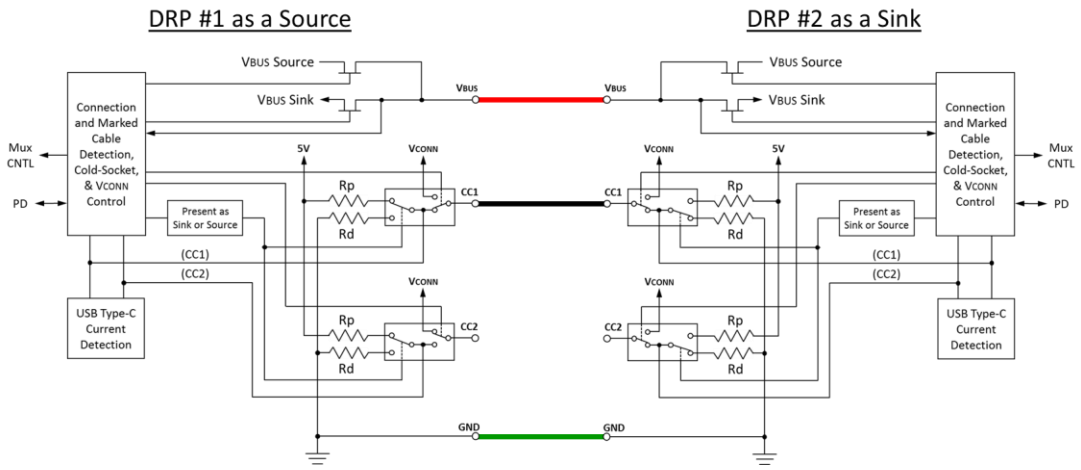
CASE 1: The following describes the behavior when a DRP is connected to another DRP. In this flow, the two DRPs accept the resulting Source-to-Sink relationship achieved randomly.

1. Both DRPs in the unattached state
   - DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK
2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC
   - DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC
3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK
   - DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK
4. DRP #1 transitions from AttachWait.SRC to Attached.SRC
   - DRP #1 in AttachWait.SRC continues to see CC pull down of DRP #2 for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN
5. DRP #2 transitions from AttachWait.SNK to Attached.SNK.
   - DRP #2 after having been in AttachWait.SNK for tCCDebounce and having detected VBUS, enters Attached.SNK
6. While the DRPs are in their respective attached states:
   - DRP #1 (as Source) adjusts Rp as needed to limit the current DRP #2 (as Sink) may draw
   - DRP #2 (as Sink) detects and monitors vRd for available current on VBUS
   - DRP #1 (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-24 说明了上述第一种情况下 DRP 连接到 DRP 的功能模型。标准电缆中的单条 CC 线仅显示在四种可能的连接路线之一中，即 CC1 到 CC1。图中已任意分配端口号，以帮助读者理解过程描述。

图 4-24 DRP 到 DRP 功能模型 – 案例 1



CASE 1：以下描述了一个 DRP 连接到另一个 DRP 时的行为。在此流程中，两个 DRP 接受随机实现的 Source-to-Sink 关系。

1. 两个 DRP 都处于未连接状态 • DRP #1 和 DRP #2 在 Unattached.SRC 和 Unattached.SNK 之间交替 2. DRP #1 从 Unattached.SRC 转换到 AttachWait.SRC • Unattached.SRC 中的 DRP #1 检测到 Unattached.SNK 中的 DRP #2 的 CC 下拉

并进入 AttachWait.SRC 3. DRP #2 从 Unattached.SNK 转换到 AttachWait.SNK • Unattached.SNK 中的 DRP #2 检测到 CC 上的上拉并进入 AttachWait.SNK 4. DRP #1 从 AttachWait.SRC 转换到 Attached.SRC • AttachWait.SRC 中的 DRP #1 继续看到 DRP #2 的 CC 下拉持续 tCCDebounce，进入 Attached.SRC 并打开 VBUS 和 VCONN 5. DRP #2 从 AttachWait.SNK 转换到 Attached.SNK。• DRP #2 在 AttachWait.SNK 中持续 tCCDebounce 并检测到 VBUS 后，进入 Attached.SNK

6. 当 DRP 处于各自的附加状态时：

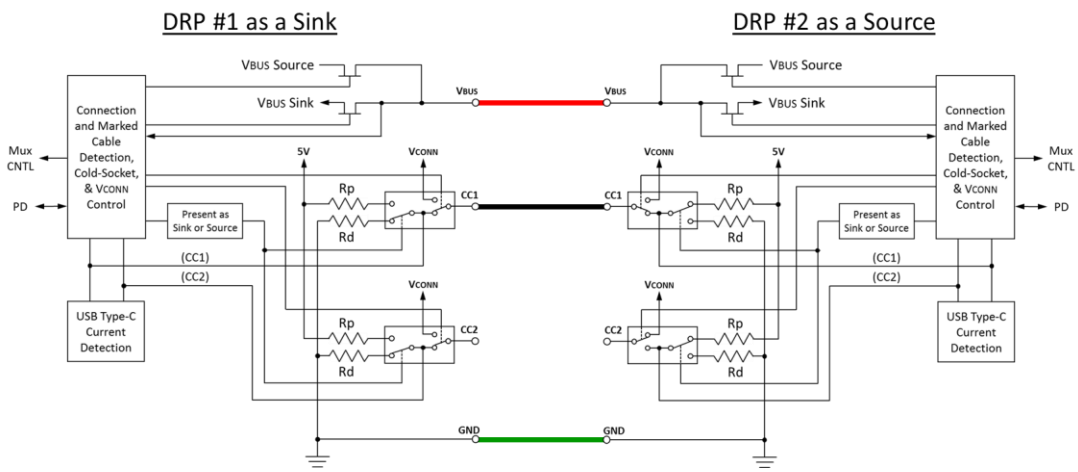
• DRP #1（作为源）根据需要调整 Rp，以限制 DRP #2（作为接收器）可能吸收的电流 • DRP #2（作为接收器）检测并监控 vRd，以确定 VBUS 上的可用电流 • DRP #1（作为源）监控 CC 是否断开，检测到断开后，进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换）

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- DRP #2 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

Figure 4-25 illustrates the functional model for a DRP connected to a DRP in the second case described.

Figure 4-25 DRP to DRP Functional Model – CASE 2 & 3



CASE 2: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #2 chooses to drive the random result to the opposite result using the Try.SRC mechanism.

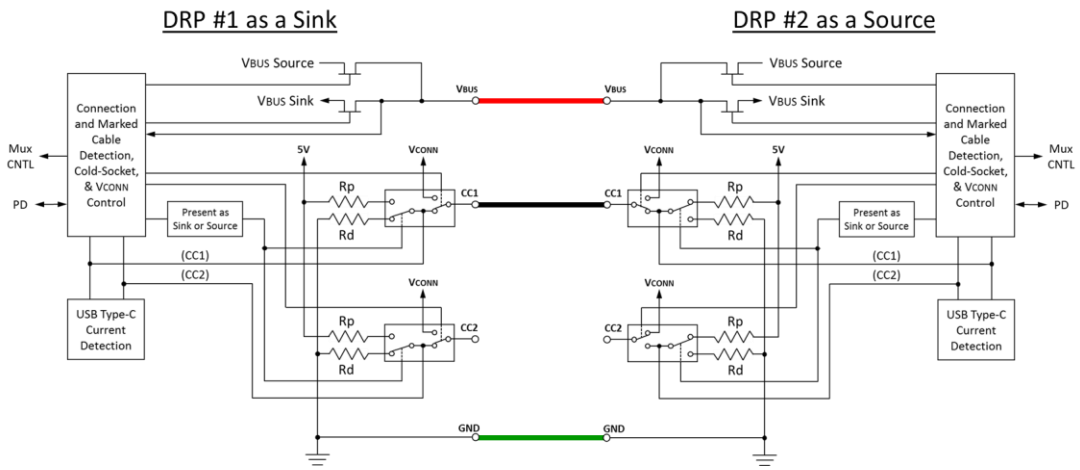
1. Both DRPs in the unattached state
   - DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK
2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC
   - DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC
3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK
   - DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK
4. DRP #1 transitions from AttachWait.SRC to Attached.SRC
   - DRP #1 in AttachWait.SRC continues to see CC pull down of DRP #2 for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN
5. DRP #2 transitions from AttachWait.SNK to Try.SRC.
   - DRP #2 in AttachWait.SNK has been in this state for tCCDebounce and detects VBUS but strongly prefers the Source role, so transitions to Try.SRC
   - DRP #2 in Try.SRC asserts a pull-up on CC and waits
6. DRP #1 transitions from Attached.SRC to Unattached.SNK to AttachWait.SNK
   - DRP #1 in Attached.SRC no longer detects DRP #2's pull-down on CC and transitions to Unattached.SNK.
   - DRP #1 in Unattached.SNK turns off VBUS and VCONN and applies a pull-down on CC

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• DRP #2（作为 Sink）监控 VBUS 是否分离，检测到分离后进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换）

图 4-25 说明了所述第二种情况下的 DRP 连接到 DRP 的功能模型。

图 4-25 DRP 到 DRP 功能模型 – 案例 2 和 3



案例 2：以下描述了一个 DRP 连接到另一个 DRP 时的行为。在此流程中，DRP #2 选择使用 Try.SRC 机制将随机结果驱动为相反的结果。

1. 两个 DRP 都处于未连接状态 • DRP #1 和 DRP #2 在 Unattached.SRC 和 Unattached.SNK 之间交替 2. DRP #1 从 Unattached.SRC 转换到 AttachWait.SRC • Unattached.SRC 中的 DRP #1 检测到 Unattached.SNK 中的 DRP #2 的 CC 下拉并进入 AttachWait.SRC 3. DRP #2 从 Unattached.SNK 转换到 AttachWait.SNK • Unattached.SNK 中的 DRP #2 检测到 CC 上拉并进入 AttachWait.SNK 4. DRP #1 从 AttachWait.SRC 转换到 Attached.SRC • AttachWait.SRC 中的 DRP #1 继续看到 DRP #2 的 CC 下拉并持续 tCCDebounce，进入 Attached.SRC 并打开 VBUS 和 VCONN

5. DRP #2 从 AttachWait.SNK 转换到 Try.SRC。

AttachWait.SNK 中的 • DRP #2 一直处于此状态达 tCCDebounce 并检测到 VBUS，但强烈倾向于源角色，因此转换为 Try.SRC Try.SRC 中的 • DRP #2 在 CC 上断言上拉并等待

6. DRP #1 从 Attached.SRC 转换到 Unattached.SNK 再到 AttachWait.SNK

• Attached.SRC 中的 DRP #1 不再检测 DRP #2 在 CC 上的下拉，并转换到 Unattached.SNK。• Unattached.SNK 中的 DRP #1 关闭 VBUS 和 VCONN，并在 CC 上应用下拉

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- DRP #1 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK

7. DRP #2 transitions from Try.SRC to Attached.SRC
   - DRP #2 in Try.SRC detects the DRP #1 in Unattached.SNK's pull-down on CC and enters Attached.SRC
   - DRP #2 in Attached.SRC turns on VBUS and VCONN
8. DRP #1 transitions from AttachWait.SNK to Attached.SNK
   - DRP #1 in AttachWait.SNK after tCCDebounce and detecting VBUS, enters Attached.SNK
9. While the DRPs are in their respective attached states:
   - DRP #2 (as Source) adjusts Rp as needed to limit the current DRP #1 (as Sink) may draw
   - DRP #1 (as Sink) detects and monitors vRd for available current on VBUS
   - DRP #2 (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)
   - DRP #1 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

CASE 3: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #1 chooses to drive the random result to the opposite result using the Try.SNK mechanism.

1. Both DRPs in the unattached state
   - DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK
2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC
   - DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC
3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK
   - DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK
4. DRP #1 transitions from AttachWait.SRC to Try.SNK
   - DRP #1 in AttachWait.SRC has been in this state for tCCDebounce and detects DRP #2's pull-down on CC but strongly prefers the Sink role, so transitions to Try.SNK
   - DRP #1 in Try.SNK asserts a pull down on CC and waits
5. DRP #2 transitions from AttachWait.SNK to Unattached.SRC to AttachWait.SRC.
   - DRP #2 in AttachWait.SNK no longer detects DRP #1's pull up on CC and transitions to Unattached.SRC
   - DRP #2 in Unattached.SRC applies a pull up on CC
   - DRP #2 in Unattached.SRC detects a pull down on a CC pin and enters AttachWait.SRC
   - DRP #1 detects DRP #2's pull up on CC and remains in Try.SNK
6. DRP #2 transitions from AttachWait.SRC to Attached.SRC

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Unattached.SNK 中的 • DRP #1 检测到 CC 上的上拉并进入 AttachWait.SNK

7. DRP #2 从 Try.SRC 转换为 Attached.SRC

• Try.SRC 中的 DRP #2 检测到 Unattached.SNK 中的 DRP #1 在 CC 上的下拉并进入 Attached.SRC • Attached.SRC 中的 DRP #2 打开 VBUS 和 VCONN

8. DRP #1 从 AttachWait.SNK 转换为 Attached.SNK

AttachWait.SNK 中的 • DRP #1 在 tCCDebounce 和检测 VBUS 之后进入 Attached.SNK

9. 当 DRP 处于各自的附着状态时：

• DRP #2（作为源）根据需要调整 Rp，以限制当前 DRP #1（作为接收器）可能会绘制 • DRP #1（作为 Sink）检测并监控 vRd 以获取 VBUS 上的可用电流 • DRP #2（作为 Source）监控 CC 是否分离，当检测到时，进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换）• DRP #1（作为 Sink）监控 VBUS 是否分离，当检测到时，进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换）

案例 3：以下描述了一个 DRP 连接到另一个 DRP 时的行为。在此流程中，DRP #1 选择使用 Try.SNK 机制将随机结果驱动为相反的结果。

1. 两个 DRP 都处于未连接状态

• DRP #1 和 DRP #2 在 Unattached.SRC 和 Unattached.SNK 之间交替

2. DRP #1 从 Unattached.SRC 转换为 AttachWait.SRC

Unattached.SRC 中的 • DRP #1 检测到 Unattached.SNK 中的 DRP #2 的 CC 下拉，并进入 AttachWait.SRC

3. DRP #2 从 Unattached.SNK 转换为 AttachWait.SNK

Unattached.SNK 中的 • DRP #2 检测到 CC 上的上拉并进入 AttachWait.SNK

4. DRP #1 从 AttachWait.SRC 转换为 Try.SNK

• AttachWait.SRC 中的 DRP #1 已处于此状态达 tCCDebounce 并检测到 DRP #2 对 CC 的下拉但强烈倾向于 Sink 角色，因此转换到 Try.SNK • Try.SNK 中的 DRP #1 断言对 CC 的下拉并等待 5. DRP #2 从 AttachWait.SNK 转换到 Unattached.SRC 再到 AttachWait.SRC。

AttachWait.SNK 中的 • DRP #2 不再检测 CC 上的 DRP #1 上拉，并且转换到 Unattached.SRC • Unattached.SRC 中的 DRP #2 对 CC 施加上拉 • Unattached.SRC 中的 DRP #2 检测到 CC 引脚上的下拉并进入 AttachWait.SRC • DRP #1 检测到 DRP #2 对 CC 的上拉并保持在 Try.SNK 中

6. DRP #2 从 AttachWait.SRC 转换到 Attached.SRC

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

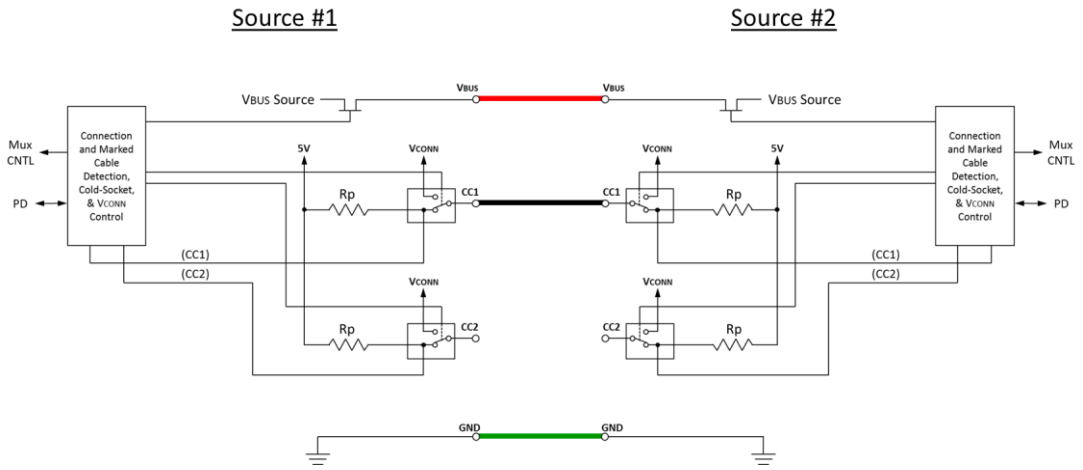
- DRP #2 in AttachWait.SRC times out (tCCDebounce) and transitions to Attached.SRC
- DRP #2 in Attached.SRC turns on VBUS and VCONN

7. DRP #1 transitions from Try.SNK to Attached.SNK
   - DRP #1 in Try.SNK after detecting VBUS, enters Attached.SNK
8. While the DRPs are in their respective attached states:
   - DRP #2 (as Source) adjusts Rp as needed to limit the current DRP #1 (as Sink) may draw
   - DRP #1 (as Sink) detects and monitors vRd for available current on VBUS
   - DRP #2 (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)
   - DRP #1 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

4.5.3.1.5 Source to Source Behavior

Figure 4-26 illustrates the functional model for a Source connected to a Source. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

Figure 4-26 Source to Source Functional Model



The following describes the behavior when a Source is connected to another Source.

1. Both Sources in the unattached state
   - Source #1 fails to detect a Sink's pull-down on CC and remains in Unattached.SRC
   - Source #2 fails to detect a Sink's pull-down on CC and remains in Unattached.SRC

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

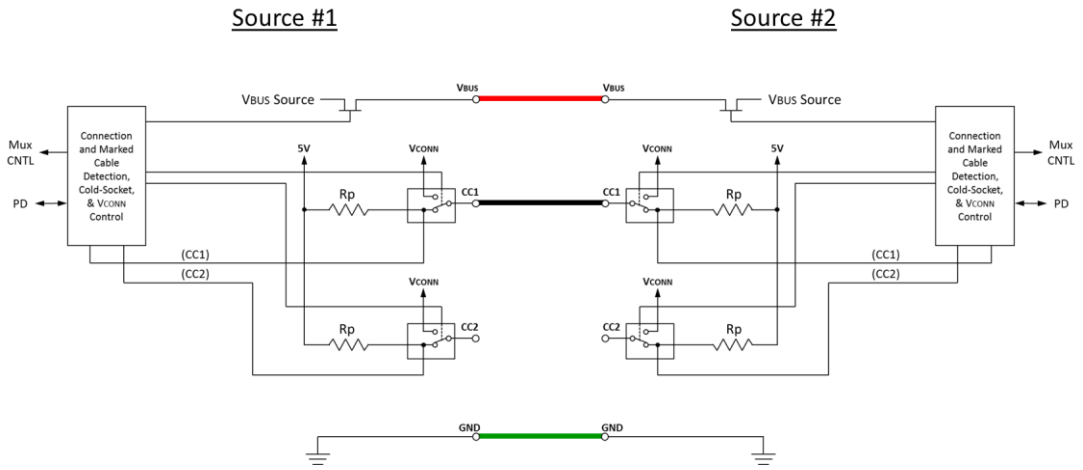
• AttachWait.SRC 中的 DRP #2 超时 (tCCDebounce) 并转换到 Attached.SRC • Attached.SRC 中的 DRP #2 打开 VBUS 和 VCONN 7. DRP #1 从 Try.SNK 转换到 Attached.SNK • Try.SNK 中的 DRP #1 在检测到 VBUS 后，进入 Attached.SNK 8. 当 DRP 处于各自的连接状态时：• DRP #2 (作为源) 根据需要调整 Rp 以限制 DRP #1 (作为接收器) 可能吸收的电流 • DRP #1 (作为接收器) 检测并监控 vRd 以获取 VBUS 上的可用电流 • DRP #2 (作为源) 监控 CC 是否断开连接，并在检测到断开连接时进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换）• DRP #1 (作为Sink 监控 VBUS 是否断开连接，检测到断开连接后进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换）

4.5.3.1.5 源到源行为

图 4-26 显示了源与源连接的功能模型。标准电缆中的单条 CC 线仅显示在四种可能的连接路线之一中，即 CC1 到 CC1。图中任意分配了端口号，以协助

读者能够理解该过程的描述。

Figure 4-26 Source to Source Functional Model



下面描述了一个源连接到另一个源时的行为。

1. 两个源都处于未连接状态

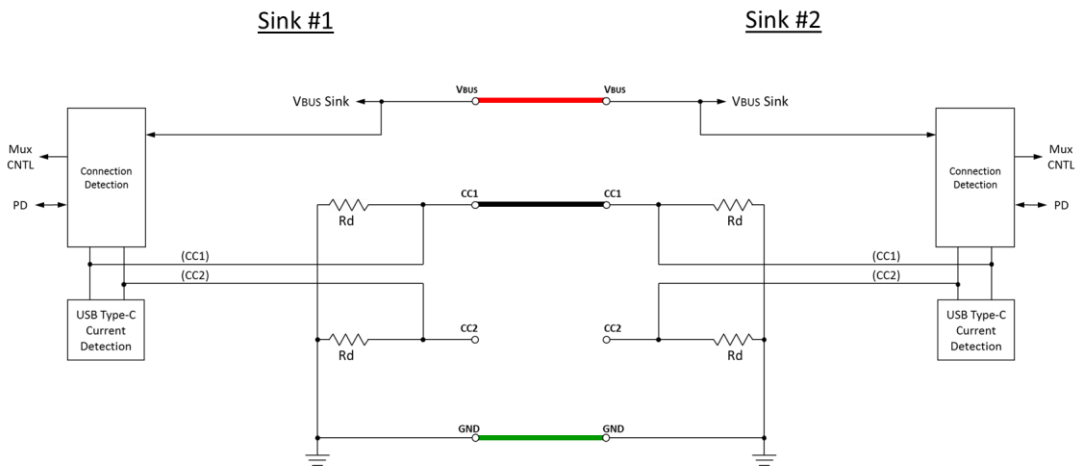
• 源 #1 未能检测到 CC 上的接收器下拉，并保持未连接状态。SRC • 源 #2 未能检测到 CC 上的接收器下拉，并保持未连接状态。SRC

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.3.1.6 Sink to Sink Behavior

Figure 4-27 illustrates the functional model for a Sink connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

Figure 4-27 Sink to Sink Functional Model



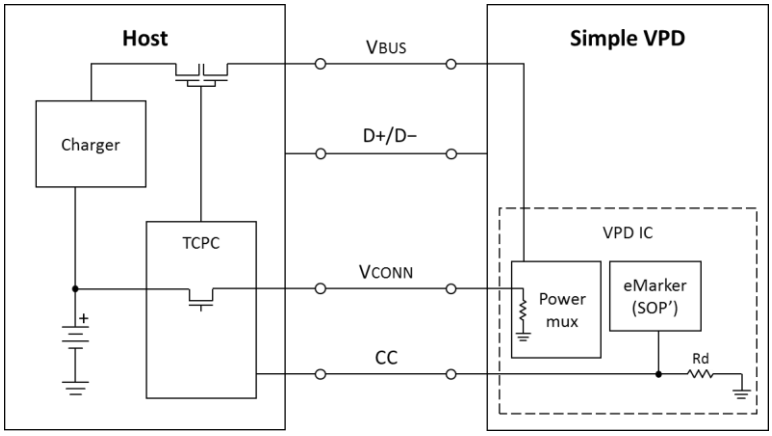
The following describes the behavior when a Sink is connected to another Sink.

1. Both Sinks in the unattached state
   - Sink #1 fails to detect pull up on CC or VBUS supplied by a Source and remains in Unattached.SNK
   - Sink #2 fails to detect pull up on CC or VBUS supplied by a Source and remains in Unattached.SNK

4.5.3.1.7 DRP to VCONN-Powered USB Device (VPD) Behavior

Figure 4-28 illustrates the functional model for a DRP connected to a VCONN-Powered USB Device that does not feature charge-through functionality.

Figure 4-28 DRP to VPD Model

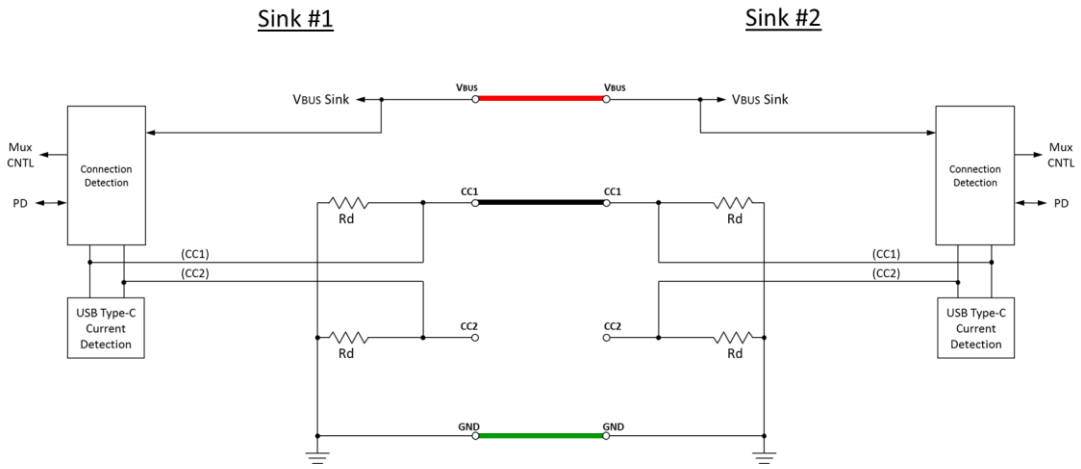


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.3.1.6 接收器到接收器行为

图 4-27 说明了 Sink 连接到 Sink 的功能模型。标准电缆中的单条 CC 线仅显示在四种可能的连接路线之一中，即 CC1 到 CC1。图中已任意分配端口号，以帮助读者理解过程描述。

图 4-27 Sink 到 Sink 功能模型



下面描述了一个Sink连接到另一个Sink时的行为。

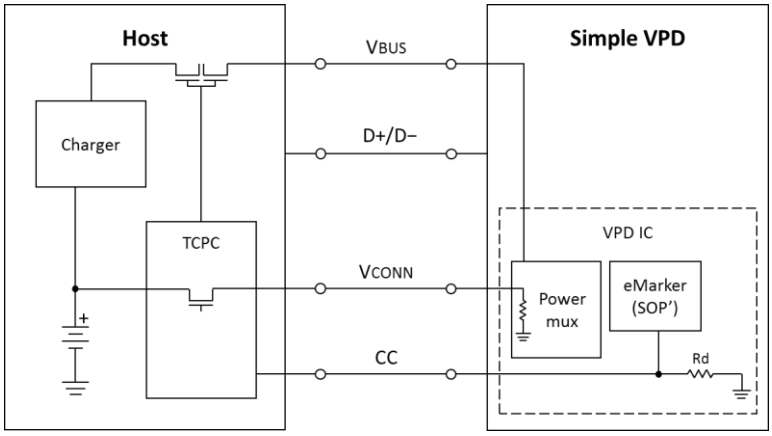
1. 两个 Sink 都处于未连接状态

   • 接收器 #1 无法检测到由源提供的 CC 或 VBUS 上的上拉，并保持未连接状态。SNK • 接收器 #2 无法检测到由源提供的 CC 或 VBUS 上的上拉，并保持未连接状态。SNK

4.5.3.1.7 DRP 至 VCONN 供电 USB 设备 (VPD) 行为

图 4-28 说明了连接到不具备充电功能的 VCONN 供电 USB 设备的 DRP 功能模型。

图 4-28 DRP 到 VPD 模型



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

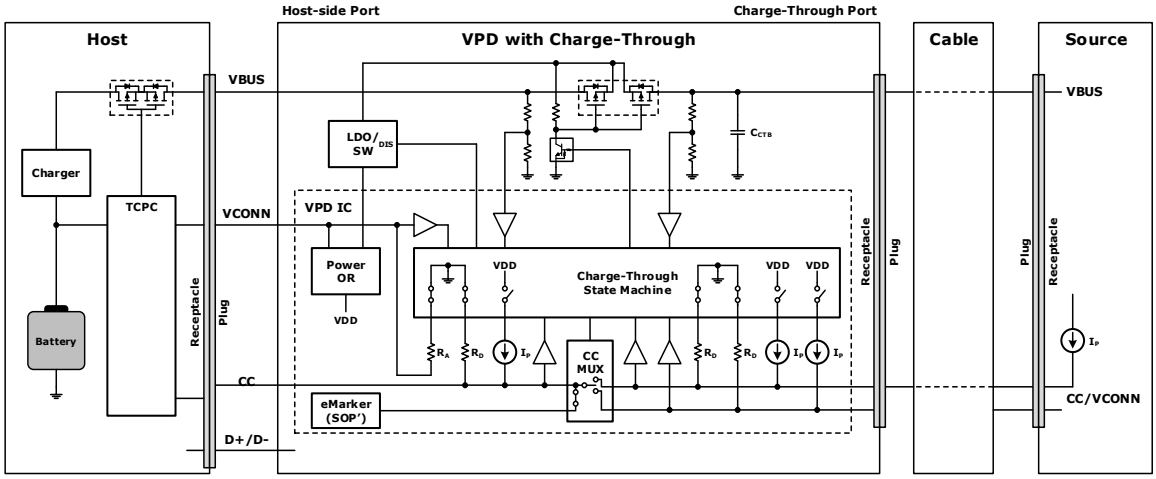
The following describes the behavior when a DRP that supports VPDs is connected to a VPD.

1. DRP and VPD in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. DRP transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   - DRP in Unattached.SRC detects the CC pull-down of VPD which is in Unattached.SNK and DRP enters AttachWait.SRC
   - DRP in AttachWait.SRC detects that pull-down on CC persists for tCCDebounce. It then enters Attached.SRC and turns on VBUS and VCONN
3. VPD transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK
   - VPD detects VCONN and enters Attached.SNK
4. While DRP and VPD are in their respective attached states, DRP discovers the VPD and removes VBUS
   - DRP (as Source) queries the cable identity via *USB PD* on SOP'.
   - VPD responds on SOP', advertising that it is a VCONN-Powered USB Device that does not support charge-through
   - DRP (as Source) removes VBUS
   - DRP (as Source) maintains its Rp
5. DRP and VPD for detach
   - DRP (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)
   - VPD monitors VCONN for detach and when detected, enters Unattached.SNK

4.5.3.1.8 DRP to Charge-Through VCONN-Powered USB Device (CTVPD) Behavior

Figure 4-29 illustrates the functional model for a DRP connected to a Charge-Through VCONN-Powered USB Device, with a Source attached to the Charge-Through port on the VCONN-Powered USB Device.

Figure 4-29 Example DRP to Charge-Through VCONN-Powered USB Device Model



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

下面描述了支持 VPD 的 DRP 连接到 VPD 时的行为。

1. DRP 和 VPD 处于未连接状态 • DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替 2. DRP 通过 AttachWait.SRC 从 Unattached.SRC 转换到 Attached.SRC • Unattached.SRC 中的 DRP 检测到 Unattached.SNK 中的 VPD 的 CC 下拉，并且 DRP 进入 AttachWait.SRC • AttachWait.SRC 中的 DRP 检测到 CC 上的下拉持续了 tCCDebounce。

然后进入 Attached.SRC 并打开 VBUS 和 VCONN

3. VPD 通过 AttachWait.SNK 从 Unattached.SNK 转换为 Attached.SNK

• VPD 检测到 VCONN 并进入 Attached.SNK

4. 当 DRP 和 VPD 处于各自的连接状态时，DRP 发现 VPD 并移除 VBUS

• DRP（作为源）通过 SOP ’ 上的 *USB PD* 查询电缆身份。• VPD 在 SOP ’ 上做出响应，宣布它是一个 VCONN 供电的 USB 设备，不支持直通充电 • DRP（作为源）移除 VBUS • DRP（作为源）保持其 Rp

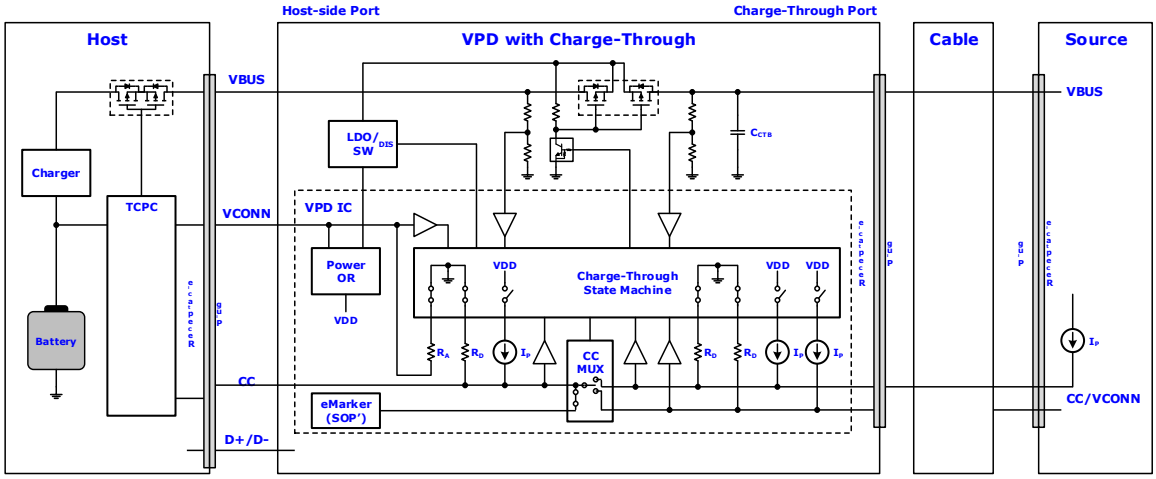
5. 分离的 DRP 和 VPD

• DRP（作为源）监控 CC 是否分离，检测到分离后进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换）• VPD 监控 VCONN 是否分离，检测到分离后进入 Unattached.SNK

4.5.3.1.8 DRP 到通过 VCONN 供电的 USB 设备 (CTVPD) 充电的行为

图 4-29 说明了连接到通过 VCONN 供电的 USB 设备的充电式 DRP 的功能模型，其中源连接到 VCONN 供电的 USB 设备上的充电式端口。

图 4-29 DRP 至通过 VCONN 充电的 USB 设备模型示例



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

CASE 1: The following describes the behavior when a DRP is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with no Power Source attached to the Charge-Through port on the CTVPD.

1. DRP and CTVPD are both in the unattached state
    a. DRP alternates between Unattached.SRC and Unattached.SNK
    b. CTVPD has applied Rd on its Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin
2. DRP transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
    a. DRP in Unattached.SRC detects a CC pull down of CTVPD which is in Unattached.SNK and DRP enters AttachWait.SRC
    b. DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN
3. CTVPD transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK
    a. CTVPD detects the host-side CC pull-up of the DRP and CTVPD enters AttachWait.SNK
    b. CTVPD in AttachWait.SNK detects that pull up on the Host-side port's CC persists for tCCDebounce, VCONN present and enters Attached.SNK
    c. CTVPD present a high-impedance to ground (above zOPEN) on its Charge-Through port's CC1 and CC2 pins
4. While DRP and CTVPD are in their respective attached states, DRP discovers the CTVPD and transitions to CTUnattached.SNK
    a. DRP (as Source) queries the device identity via *USB PD* (Device Identity Command) on SOP'
    b. CTVPD responds on SOP', advertising that it is a Charge-Through VCONN-Powered USB Device
    c. DRP (as Source) removes VBUS
    d. DRP (as Source) changes its Rp to a Rd
    e. DRP (as Sink) continues to provide VCONN and enters CTUnattached.SNK
5. CTVPD transitions to CTUnattached.VPD
    a. CTVPD detects VBUS removal, VCONN presence, the low Host-side CC pin and enters CTUnattached.VPD
    b. CTVPD changes its host-side Rd to a Rp advertising 3.0 A
    c. CTVPD isolates itself from VBUS
    d. CTVPD apply Rd on its Charge-Through port's CC1 and CC2 pins
6. While the CTVPD in CTUnattached.VPD state and the DRP in CTUnattached.SNK state:
    a. CTVPD monitors Charge-Though CC pins for a source or sink; when a Power Source attach is detected, enters CTAttachWait.VPD; when a sink is detected, enters CTAttachWait.Unsupported
    b. CTVPD monitors VCONN for Host detach and when detected, enters Unattached.SNK
    c. DRP monitors VBUS and CC for CTVPD detach for tVPDDetach and when detected, enters Unattached.SNK
    d. DRP monitors VBUS for Power Source attach and when detected, enters CTAttached.SNK

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

情况 1：以下描述了当 DRP 连接到通过 VCONN 充电的 USB 设备（缩写为 CTVPD）时的行为，且 CTVPD 上的充电端口没有连接电源。

1. DRP 和 CTVPD 均处于未连接状态

   a. DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替 b. CTVPD 已将 Rd 应用于其 Charge-Through 端口的 CC1 和 CC2 引脚，并将 Rd 应用于主机端端口的 CC 引脚

2. DRP通过AttachWait.SRC从Unattached.SRC过渡到Attached.SRC

   a. Unattached.SRC 中的 DRP 检测到 Unattached.SNK 中的 CTVPD 的 CC 下拉，并且 DRP 进入 AttachWait.SRC b. AttachWait.SRC 中的 DRP 检测到 CC 上的下拉持续了 tCCDebounce，进入 Attached.SRC 并打开 VBUS 和 VCONN

3. CTVPD 通过 AttachWait.SNK 从 Unattached.SNK 转换为 Attached.SNK

   a. CTVPD 检测到 DRP 的主机侧 CC 上拉，并且 CTVPD 进入 AttachWait.SNK b. AttachWait.SNK 中的 CTVPD 检测到主机侧端口的 CC 上的上拉持续了 tCCDebounce，VCONN 存在并进入 Attached.SNK c. CTVPD 在其 Charge-Through 端口的 CC1 和 CC2 引脚上呈现高阻抗接地（高于 zOPEN）

4. 当 DRP 和 CTVPD 处于各自的连接状态时，DRP 发现 CTVPD 并转换为 CTUnattached.SNK

   a. DRP（作为源）在 SOP ’ 上通过 *USB PD*（设备标识命令）查询设备标识 b. CTVPD 在 SOP ’ 上做出响应，通告它是通过 VCONN 充电的 USB 设备 c. DRP（作为源）移除 VBUS d. DRP（作为源）将其 Rp 更改为 Rd e. DRP（作为接收器）继续提供 VCONN 并进入 CTUnattached.SNK

5. CTVPD 转换为 CTUnattached.VPD

   a. CTVPD 检测到 VBUS 移除、VCONN 存在、主机端 CC 引脚低电平，并进入 CTUnattached.VPD b. CTVPD 将其主机端 Rd 更改为 Rp 通告 3.0 A c. CTVPD 将自身与 VBUS 隔离 d. CTVPD 将 Rd 应用于其 Charge-Through 端口的 CC1 和 CC2 引脚

6. 当 CTVPD 处于 CTUnattached.VPD 状态且 DRP 处于 CTUnattached.SNK 状态时：

   a. CTVPD 监控充电通过 CC 引脚是否有源或接收器；当检测到电源连接时，进入 CTAttachWait.VPD；当检测到接收器时，进入 CTAttachWait.Unsupported b. CTVPD 监控 VCONN 是否有主机分离，当检测到时，进入 Unattached.SNK c. DRP 监控 VBUS 和 CC 是否有 CTVPD 分离 tVPDDetach，当检测到时，进入 Unattached.SNK d. DRP 监控 VBUS 是否有电源连接，当检测到时，进入 CTAttached.SNK

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

CASE 2: The following describes the behavior when a Power Source is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with a Host already attached to the Host-side port on the CTVPD.

1. DRP is in CTUnattached.SNK state, CTVPD in CTUnattached.VPD, and Power Source in the unattached state
    a. CTVPD has applied Rd on the Charge-Through port's CC1 and CC2 pins and Rp termination advertising 3.0 A on the Host-side port's CC pin
2. Power Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
    a. Power Source detects the CC pull-down of the CTVPD and enters AttachWait.SRC
    b. Power Source in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS
3. CTVPD transitions from CTUnattached.VPD through CTAttachWait.VPD to CTAttached.VPD
    a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, and transitions to CTAttachWait.VPD
    b. CTVPD finishes any active *USB PD* communication on SOP' and ceases to respond to SOP' queries
    c. CTVPD in CTAttachWait.VPD detects that the pull up on Charge-Through CC pin persists for tCCDebounce, detects VBUS and enters CTAttached.VPD
    d. CTVPD connects the active Charge-Through CC pin to the Host-side port's CC pin
    e. CTVPD disables its Rp termination advertising 3.0 A on the Host-side port's CC pin
    f. CTVPD disables its Rd on the Charge-Through CC pins
    g. CTVPD connects VBUS from the Charge-Through side to the Host side
4. DRP (as Sink) transitions to CTAttached.SNK
    a. DRP (as Sink) detects VBUS, monitors vRd for available current and enter CTAttached.SNK
5. While the devices are all in their respective attached states:
    a. CTVPD monitors VCONN for DRP detach and when detected, enters CTDisabled.VPD
    b. CTVPD monitors VBUS and CC for Power Source detach and when detected, enters CTUnattached.VPD within tVPDCTDD
    c. DRP (as Sink) monitors VBUS for Charge-Through Power Source detach and when detected, enters CTUnattached.SNK
    d. DRP (as Sink) monitors VBUS and CC for CTVPD detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)
    e. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

情况 2：以下描述了当电源连接到通过 VCONN 充电的 USB 设备（缩写为 CTVPD）时的行为，并且主机已连接到 CTVPD 上的主机侧端口。

1. DRP 处于 CTUnattached.SNK 状态，CTVPD 处于 CTUnattached.VPD 状态，电源处于未连接状态
   a. CTVPD 已在 Charge-Through 端口的 CC1 和 CC2 引脚上施加 Rd，并在主机端端口的 CC 引脚上施加 3.0 A 的 Rp 终端电流
2. Power Source 通过 AttachWait.SRC 从 Unattached.SRC 转换到 Attached.SRC
   a. 电源检测到 CTVPD 的 CC 下拉并进入 AttachWait.SRC b. AttachWait.SRC 中的电源检测到 CC 上的下拉持续了 tCCDebounce，进入 Attached.SRC 并打开 VBUS
3. CTVPD 从 CTUnattached.VPD 经过 CTAttachWait.VPD 转换到 CTAttached.VPD
   a. CTVPD 在其一个 Charge-Through CC 引脚上检测到源的 Rp，并转换到 CTAttachWait.VPD b. CTVPD 完成 SOP’ 上的任何活动 *USB PD* 通信并停止响应 SOP’ 查询 c. CTAttachWait.VPD 中的 CTVPD 检测到 Charge-Through CC 引脚上的上拉持续了 tCCDebounce，检测到 VBUS 并进入 CTAttached.VPD d. CTVPD 将活动的 Charge-Through CC 引脚连接到主机端端口的 CC 引脚 e. CTVPD 禁用其 Rp 终端，在主机侧端口的 CC 引脚上通告 3.0 A f. CTVPD 禁用其在 Charge-Through CC 引脚上的 Rd g. CTVPD 将 VBUS 从 Charge-Through 侧连接到主机侧
4. DRP（作为接收器）转换为 CTAttached.SNK
   a. DRP（作为 Sink）检测 VBUS，监控 vRd 的可用电流并输入 CTAttached.SNK
5. 当所有设备都处于各自的连接状态时：
   a. CTVPD 监控 VCONN 以检测 DRP 是否分离，检测到后进入 CTDisabled.VPD b. CTVPD 监控 VBUS 和 CC 以检测电源是否分离，检测到后在 tVPDCTDD 内进入 CTUnattached.VPD c. DRP（作为 Sink）监控 VBUS 以检测充电电源是否分离，检测到后进入 CTUnattached.SNK d. DRP（作为 Sink）监控 VBUS 和 CC 以检测 CTVPD 是否分离，检测到后进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换） e. 电源监控 CC 以检测 CTVPD 是否分离，检测到后进入 Unattached.SRC

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

CASE 3: The following describes the behavior when a Power Source is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with no Host attached to the Host-side port on the CTVPD.

1. CTVPD and Power Source are both in the unattached state
    a. CTVPD has applied Rd on the Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin
2. Power Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
    a. Power Source detects the CC pull-down of the CTVPD and enters AttachWait.SRC
    b. Power Source in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS
3. CTVPD alternates between Unattached.SNK and Unattached.SRC
    a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, detects VBUS for tCCDebounce and starts alternating between Unattached.SRC and Unattached.SNK
4. While the CTVPD alternates between Unattached.SRC and Unattached.SNK state and the Power Source in Attached.SRC state:
    a. CTVPD monitors the Host-side port's CC pin for device attach and when detected, enters AttachWait.SRC
    b. CTVPD monitors VBUS for Power Source detach and when detected, enters Unattached.SNK
    c. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC

CASE 4: The following describes the behavior when a DRP is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with a Power Source already attached to the Charge-Through side on the CTVPD.

1. DRP and CTVPD are in unattached state and Power Source in Attached.SRC state
    a. DRP alternates between Unattached.SRC and Unattached.SNK
    b. CTVPD alternates between Unattached.SRC and Unattached.SNK
    c. CTVPD has applied Rd on its Charge-Through port's CC1 and CC2 pins
    d. Power Source has applied VBUS
2. DRP transitions from Unattached.SNK to AttachWait.SNK
    a. DRP in Unattached.SNK detects the CC pull-up of CTVPD which is in Unattached.SRC and DRP enters AttachWait.SNK
3. CTVPD transitions from Unattached.SRC to Try.SNK through AttachWait.SRC
    a. CTVPD in Unattached.SRC detects the CC pull-down of DRP which is in Unattached.SNK and CTVPD enters AttachWait.SRC
    b. CTVPD in AttachWait.SRC detects that pull down on CC persists for tCCDebounce and enters Try.SNK
    c. CTVPD disables Rp termination advertising Default USB Power on the Host-side port's CC pin
    d. CTVPD enables Rd on the Host-side port's CC pin

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

情况 3：以下描述了当电源连接到通过 VCONN 充电的 USB 设备（缩写为 CTVPD）且没有主机连接到 CTVPD 上的主机侧端口时的行为。

1. CTVPD 和电源均处于未连接状态
   a. CTVPD 已将 Rd 施加到 Charge-Through 端口的 CC1 和 CC2 引脚上，并将 Rd 施加到主机端端口的 CC 引脚上
2. Power Source 通过 AttachWait.SRC 从 Unattached.SRC 转换到 Attached.SRC
   a. 电源检测到 CTVPD 的 CC 下拉并进入 AttachWait.SRC b. AttachWait.SRC 中的电源检测到 CC 上的下拉持续了 tCCDebounce，进入 Attached.SRC 并打开 VBUS
3. CTVPD 在 Unattached.SNK 和 Unattached.SRC 之间交替
   a. CTVPD 在其一个 Charge-Through CC 引脚上检测到源的 Rp，检测 VBUS 的 tCCDebounce 并开始在 Unattached.SRC 和 Unattached.SNK 之间交替
4. 当 CTVPD 在 Unattached.SRC 和 Unattached.SNK 状态之间交替并且电源处于 Attached.SRC 状态时：
   a. CTVPD 监控主机端端口的 CC 引脚是否连接设备，检测到后进入 AttachWait.SRC b. CTVPD 监控 VBUS 是否断开电源，检测到后进入 Unattached.SNK c. 电源监控 CC 是否断开 CTVPD，检测到后进入 Unattached.SRC

情况 4：以下描述了当 DRP 连接到通过 VCONN 充电的 USB 设备（缩写为 CTVPD）时的行为，其中电源已连接到 CTVPD 上的通过充电侧。

1. DRP 和 CTVPD 处于未连接状态，电源处于连接.SRC 状态
   a. DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替 b. CTVPD 在 Unattached.SRC 和 Unattached.SNK 之间交替 c. CTVPD 已在其 Charge-Through 端口的 CC1 和 CC2 引脚上应用 Rd d. 电源已应用 VBUS
2. DRP 从 Unattached.SNK 转换为 AttachWait.SNK
   a. Unattached.SNK 中的 DRP 检测到 Unattached.SRC 中的 CTVPD 的 CC 上拉，DRP 进入 AttachWait.SNK
3. CTVPD 通过 AttachWait.SRC 从 Unattached.SRC 转换到 Try.SNK
   a. Unattached.SRC 中的 CTVPD 检测到 Unattached.SNK 中的 DRP 的 CC 下拉，并且 CTVPD 进入 AttachWait.SRC b. AttachWait.SRC 中的 CTVPD 检测到 CC 上的下拉持续了 tCCDebounce 并进入 Try.SNK c. CTVPD 禁用 Rp 终止广告主机端端口 CC 引脚上的默认 USB 电源 d. CTVPD 在主机端端口的 CC 引脚上启用 Rd

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4. DRP transitions from AttachWait.SNK to Attached.SRC through Unattached.SRC and AttachWait.SRC
    a. DRP in AttachWait.SNK detects the CC pull-up removal of CTVPD which is in Try.SNK and DRP enters Unattached.SRC
    b. DRP in Unattached.SRC detects the CC pull-down of CTVPD which is in Try.SNK and DRP enters AttachWait.SRC
    c. DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and enable VBUS and VCONN
5. CTVPD transitions from Try.SNK to Attached.SNK
    a. CTVPD detects the CC pull-up of the DRP persists for tTryCCDebounce
    b. CTVPD detects VBUS on the Host-side port and enters Attached.SNK
6. While DRP and CTVPD are in their respective attached states, DRP discovers the Charge-Through CTVPD and transitions to CTUnattached.SNK
    a. DRP (as Source) queries the device identity via *USB PD* (Discover Identity Command) on SOP'
    b. CTVPD responds on SOP', advertising that it is a Charge-Through VCONN-Powered USB Device
    c. DRP (as Source) removes VBUS
    d. DRP (as Source) changes its Rp into an Rd
    e. DRP (as Sink) continues to provide VCONN and enters CTUnattached.SNK
7. CTVPD transitions to CTUnattached.VPD
    a. CTVPD detects VBUS removal, VCONN presence, and the low CC pin on its host port and enters CTUnattached.VPD
    b. CTVPD changes its host-side Rd into an Rp termination advertising 3.0 A
    c. CTVPD isolates itself from VBUS
8. CTVPD transitions from CTUnattached.VPD through CTAttachWait.VPD to CTAttached.VPD
    a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, and transitions to CTAttachWait.VPD
    b. CTVPD in CTAttachWait.VPD detects that the pull up on Charge-Through CC pin persists for tCCDebounce, detects VBUS and enters CTAttached.VPD
    c. CTVPD finishes any active *USB PD* communication on SOP' and ceases to respond to SOP' queries
    d. CTVPD connects the active Charge-Through CC pin to the Host-side port's CC pin
    e. CTVPD disables its Rp termination advertising 3.0 A on the Host-side port's CC pin
    f. CTVPD disables its Rd on the Charge-Through CC pins
    g. CTVPD connects VBUS from the Charge-Through side to the Host side
9. DRP (as Sink) transitions to CTAttached.SNK
    a. DRP (as Sink) detects VBUS and monitors vRd for available current and enter CTAttached.SNK
10. While the devices are all in their respective attached states:

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4. DRP 通过 Unattached.SRC 和 AttachWait.SRC 从 AttachWait.SNK 转换到 Attached.SRC

a. AttachWait.SNK 中的 DRP 检测到 Try.SNK 中 CTVPD 的 CC 上拉移除，然后 DRP 进入 Unattached.SRC b. Unattached.SRC 中的 DRP 检测到 Try.SNK 中 CTVPD 的 CC 下拉，然后 DRP 进入 AttachWait.SRC c. AttachWait.SRC 中的 DRP 检测到 CC 的下拉持续了 tCCDebounce。然后它进入 Attached.SRC 并启用 VBUS 和 VCONN

5. CTVPD 从 Try.SNK 转换为 Attached.SNK

a. CTVPD 检测到 DRP 的 CC 上拉持续 tTryCCDebounce

b. CTVPD 检测到主机端端口上的 VBUS 并进入 Attached.SNK

6. 当 DRP 和 CTVPD 处于各自的连接状态时，DRP 发现 Charge-Through CTVPD 并转换为 CTUnattached.SNK

a. DRP（作为源）通过 *USB PD*（发现身份命令）在 SOP ’ 上 b. CTVPD 在 SOP ’ 上做出响应，宣布它是通过 VCONN 充电的 USB 设备 c. DRP（作为源）移除 VBUS d. DRP（作为源）将其 Rp 更改为 Rd e. DRP（作为接收器）继续提供 VCONN 并进入 CTUnattached.SNK

7. CTVPD 转换为 CTUnattached.VPD

a. CTVPD 检测到 VBUS 移除、VCONN 存在以及主机端口上的低 CC 引脚，并进入 CTUnattached.VPD b. CTVPD 将其主机端 Rd 更改为 Rp 终端，通告 3.0 A c. CTVPD 将自身与 VBUS 隔离

8. CTVPD 从 CTUnattached.VPD 经过 CTAttachWait.VPD 转换到 CTAttached.VPD

a. CTVPD 在其一个 Charge-Through CC 引脚上检测到源的 Rp，并转换到 CTAttachWait.VPD b. CTAttachWait.VPD 中的 CTVPD 检测到 Charge-Through CC 引脚上的上拉持续了 tCCDebounce，检测到 VBUS 并进入 CTAttached.VPD c. CTVPD 完成 SOP ’ 上的任何活动 *USB PD* 通信并停止响应 SOP ’ 查询 d. CTVPD 将活动的 Charge-Through CC 引脚连接到主机端端口的 CC

引脚 e. CTVPD 禁用其 Rp 终端，在主机侧端口的 CC 引脚上通告 3.0 A f. CTVPD 禁用其在 Charge-Through CC 引脚上的 Rd g. CTVPD 将 VBUS 从 Charge-Through 侧连接到主机侧

9. DRP（作为接收器）转换为 CTAttached.SNK

a. DRP（作为 Sink）检测 VBUS 并监控 vRd 的可用电流并输入 CTAttached.SNK

10. 当所有设备都处于各自的连接状态时：

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

a. CTVPD monitors VCONN for DRP detach and when detected, enters CTDisabled.VPD

b. CTVPD monitors VBUS and CC for Power Source detach and when detected, enters CTUnattached.VPD within tVPDCTDD

c. DRP (as Sink) monitors VBUS for Charge-Through Power Source detach and when detected, enters CTUnattached.SNK

d. DRP (as Sink) monitors VBUS and CC for CTVPD detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

e. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC

CASE 5: The following describes the behavior when a Power Source is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with a DRP (with dead battery) attached to the Host-side port on the CTVPD.

1. DRP, CTVPD and Power Source are all in the unattached state
   a. DRP apply dead battery Rd
   b. CTVPD apply Rd on the Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin
2. Power Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   a. Power Source detects the CC pull-down of the CTVPD and enters AttachWait.SRC
   b. Power Source in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS
3. CTVPD alternates between Unattached.SNK and Unattached.SRC
   a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, detects VBUS for tCCDebounce and starts alternating between Unattached.SRC and Unattached.SNK
4. CTVPD transitions from Unattached.SRC to Try.SNK through AttachWait.SRC
   a. CTVPD in Unattached.SRC detects the CC pull-down of DRP which is in Unattached.SNK and CTVPD enters AttachWait.SRC
   b. CTVPD in AttachWait.SRC detects that pull down on CC persists for tCCDebounce and enters Try.SNK
   c. CTVPD disables Rp termination advertising Default USB Power on the Host-side port's CC pin
   d. CTVPD enables Rd on the Host-side port's CC pin
5. DRP in dead battery condition remains in Unattached.SNK
6. CTVPD transitions from Try.SNK to Attached.SRC through TryWait.SRC
   a. CTVPD didn't detect the CC pull-up of the DRP for tTryCCDebounce after tDRPTry and enters TryWait.SRC
   b. CTVPD disables Rp on the Host-side port's CC pin
   c. CTVPD enables Rp termination advertising Default USB Power on the Host-side port's CC pin

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

a. CTVPD 监控 VCONN 以检测 DRP 是否分离，检测到后进入 CTDisabled.VPD b. CTVPD 监控 VBUS 和 CC 以检测电源是否分离，检测到后在 tVPDCTDD 内进入 CTUnattached.VPD c. DRP（作为 Sink）监控 VBUS 以检测充电电源是否分离，检测到后进入 CTUnattached.SNK d. DRP（作为 Sink）监控 VBUS 和 CC 以检测 CTVPD 是否分离，检测到后进入 Unattached.SNK（并恢复在 Unattached.SNK 和

未连接.SRC) e. 电源监控 CC 以检测 CTVPD 是否断开，当检测到时，进入未连接.SRC

案例 5：以下描述了当电源连接到通过 VCONN 充电的 USB 设备（缩写为 CTVPD）时的行为，其中 DRP（电池没电）连接到 CTVPD 上的主机侧端口。

1. DRP、CTVPD 和电源均处于未连接状态

   a. DRP 将 Rd 应用于电量耗尽的电池 b. CTVPD 将 Rd 应用于 Charge-Through 端口的 CC1 和 CC2 引脚，将 Rd 应用于主机端端口的 CC 引脚

2. Power Source 通过 AttachWait.SRC 从 Unattached.SRC 转换到 Attached.SRC

   a. 电源检测到 CTVPD 的 CC 下拉并进入 AttachWait.SRC b. AttachWait.SRC 中的电源检测到 CC 上的下拉持续了 tCCDebounce，进入 Attached.SRC 并打开 VBUS

3. CTVPD 在 Unattached.SNK 和 Unattached.SRC 之间交替

   a. CTVPD 在其一个 Charge-Through CC 引脚上检测到源的 Rp，检测 VBUS 的 tCCDebounce 并开始在 Unattached.SRC 和 Unattached.SNK 之间交替

4. CTVPD 通过 AttachWait.SRC 从 Unattached.SRC 转换到 Try.SNK

   a. Unattached.SRC 中的 CTVPD 检测到 Unattached.SNK 中的 DRP 的 CC 下拉，并且 CTVPD 进入 AttachWait.SRC b. AttachWait.SRC 中的 CTVPD 检测到 CC 上的下拉持续了 tCCDebounce 并进入 Try.SNK c. CTVPD 禁用 Rp 终止广告主机端端口 CC 引脚上的默认 USB 电源 d. CTVPD 启用主机端端口 CC 引脚上的 Rd

5. 电池没电状态下的 DRP 仍处于 Unattached.SNK 状态
6. CTVPD 通过 TryWait.SRC 从 Try.SNK 转换到 Attached.SRC

   a. CTVPD 在 tDRPTry 之后的 tTryCCDebounce 期间未检测到 DRP 的 CC 上拉，并进入 TryWait.SRC b. CTVPD 禁用主机端端口 CC 引脚上的 Rp c. CTVPD 启用 Rp 终端，在主机端端口的 CC 引脚上通告默认 USB 电源

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

   d. CTVPD detects the CC pull-down of the DRP for tTryCCDebounce and enters Attached.SRC
   e. CTVPD connects VBUS from the Charge-Through side to the Host side
7. DRP transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK
   a. DRP in Unattached.SNK detects the CC pull-up of CTVPD which is in Attached.SRC and DRP enters AttachWait.SNK
   b. DRP in AttachWait.SNK detects that pull up on CC persists for tCCDebounce, VBUS present and enters Attached.SNK
8. While the devices are all in their respective attached states:
   a. CTVPD monitors the Host-side port's CC pin for device attach and when detected, enters Unattached.SNK
   b. CTVPD monitors VBUS for Power Source detach and when detected, enters Unattached.SNK
   c. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC
   d. DRP monitors VBUS for CTVPD detach and when detected, enters Unattached.SNK
   e. Additionally, the DRP may query the identity of the cable via *USB PD* on SOP' when it has sufficient battery power and when a Charge-Through VPD is identified enters TryWait.SRC if implemented, or enters Unattached.SRC if TryWait.SRC is not supported

CASE 6: The following describes the behavior when a DRP is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD) and a Sink is attached to the Charge-Through port on the CTVPD.

1. DRP, CTVPD and Sink are all in the unattached state
   a. DRP alternates between Unattached.SRC and Unattached.SNK
   b. CTVPD has applied Rd on its Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin
2. DRP transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   a. DRP in Unattached.SRC detects the CC pull-down of CTVPD which is in Unattached.SNK and DRP enters AttachWait.SRC
   b. DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and enable VBUS and VCONN
3. CTVPD transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK
   a. CTVPD detects the host-side CC pull-up of the DRP and CTVPD enters AttachWait.SNK
   b. CTVPD in AttachWait.SNK detects that pull up on the Host-side port's CC persists for tCCDebounce, VCONN present and enters Attached.SNK
   c. CTVPD present a high-impedance to ground (above zOPEN) on its Charge-Through port's CC1 and CC2 pins
4. While DRP and CTVPD are in their respective attached states, DRP discovers the Charge-Through CTVPD and transitions to CTUnattached.SNK

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

d. CTVPD 检测到 DRP 的 CC 下拉，持续时间为 tTryCCDebounce，并进入 Attached.SRC e. CTVPD 将 VBUS 从 Charge-Through 侧连接到主机侧

7. DRP 通过 AttachWait.SNK 从 Unattached.SNK 转换为 Attached.SNK

a. Unattached.SNK 中的 DRP 检测到 Attached.SRC 中的 CTVPD 的 CC 上拉，并且 DRP 进入 AttachWait.SNK b. AttachWait.SNK 中的 DRP 检测到 CC 上的上拉持续了 tCCDebounce，VBUS 存在并进入 Attached.SNK

8. 虽然设备都处于各自的连接状态 状态：

a. CTVPD 监控主机端端口的 CC 引脚以检测设备连接，检测到后进入 Unattached.SNK b. CTVPD 监控 VBUS 以检测电源分离，检测到后进入 Unattached.SNK c. 电源监控 CC 以检测 CTVPD 分离，检测到后进入 Unattached.SRC d. DRP 监控 VBUS 以检测 CTVPD 分离，检测到后进入 Unattached.SNK e. 此外，DRP 可以通过 SOP 上的 *USB PD* 查询电缆的身份

，

当电池电量充足并且识别出 Charge-Through VPD 时，如果已实现，则进入 TryWait.SRC，如果不支持 TryWait.SRC，则进入 Unattached.SRC

案例 6： 下面描述了当 DRP 连接到通过 VCONN 充电的 USB 设备（缩写为 CTVPD）并且 Sink 连接到 CTVPD 上的通过充电端口时的行为。

1. DRP、CTVPD、Sink都处于未附着状态

a. DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替 b. CTVPD 已将 Rd 应用于其 Charge-Through 端口的 CC1 和 CC2 引脚，并将 Rd 应用于主机端端口的 CC 引脚

2. DRP通过AttachWait.SRC从Unattached.SRC过渡到Attached.SRC

a. Unattached.SRC 中的 DRP 检测到 Unattached.SNK 中的 CTVPD 的 CC 下拉，并且 DRP 进入 AttachWait.SRC b. AttachWait.SRC 中的 DRP 检测到 CC 上的下拉持续了 tCCDebounce。然后它进入 Attached.SRC 并启用 VBUS 和 VCONN

3. CTVPD 通过 AttachWait.SNK 从 Unattached.SNK 转换为 Attached.SNK

a. CTVPD 检测到 DRP 的主机侧 CC 上拉，并且 CTVPD 进入 AttachWait.SNK b. AttachWait.SNK 中的 CTVPD 检测到主机侧端口的 CC 上的上拉持续了 tCCDebounce，VCONN 存在并进入 Attached.SNK c. CTVPD 在其 Charge-Through 端口的 CC1 和 CC2 引脚上呈现高阻抗接地（高于 zOPEN）

4. 当 DRP 和 CTVPD 处于各自的连接状态时，DRP 发现 Charge-Through CTVPD 并转换为 CTUnattached.SNK

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

   a. DRP (as Source) queries the device identity via *USB PD* (Discover Identity Command) on SOP'
   b. CTVPD responds on SOP', advertising that it is a Charge-Through VCONN-Powered USB Device
   c. DRP (as Source) removes VBUS
   d. DRP (as Source) changes its Rp into an Rd
   e. DRP (as Sink) continues to provide VCONN and enters CTUnattached.SNK
5. CTVPD transitions to CTUnattached.VPD
   a. CTVPD detects VBUS removal, VCONN presence, and the low CC pin on its host port and enters CTUnattached.VPD
   b. CTVPD changes its host-side Rd into an Rp termination advertising 3.0 A
   c. CTVPD isolates itself from VBUS
   d. CTVPD apply Rd on its Charge-Through port's CC1 and CC2 pins
6. CTVPD alternates between CTUnattached.VPD and CTUnattached.Unsupported
   a. CTVPD detects SRC.Open on its Charge-Through CC pins and starts alternating between CTUnattached.VPD and CTUnattached.Unsupported
7. CTVPD transitions from CTUnattached.Unsupported to CTTry.SNK through CTAttachWait.Unsupported
   a. CTVPD in CTUnattached.Unsupported detects the CC pull-down of the Sink which is in Unattached.SNK and CTVPD enters CTAttachWait.Unsupported
   b. CTVPD in CTAttachWait.Unsupported detects that pull down on CC persists for tCCDebounce and enters CTTry.SNK
   c. CTVPD disables Rp termination advertising Default USB Power on the Charge-Through port's CC pins
   d. CTVPD enables Rd on the Charge-Through port's CC pins
8. CTVPD transitions from CTTry.SNK to CTAttached.Unsupported
   a. CTVPD didn't detect the CC pull-up of the potential Source for tDRPTryWait after tDRPTry and enters CTAttached.Unsupported
9. While the CTVPD in CTAttached.Unsupported state, the DRP in CTUnattached.SNK state and the Sink in Unattached.SNK state:
   a. CTVPD disables the Rd termination on the Charge-Through port's CC pins and applies Rp termination advertising Default USB Power
   b. CTVPD exposes a USB Billboard Device Class to the DRP indicating that it is connected to an unsupported device on its Charge Through port
   c. CTVPD monitors Charge-Though CC pins for Sink detach and when detected, enters CTUnattached.VPD
   d. CTVPD monitors VCONN for Host detach and when detected, enters Unattached.SNK
   e. DRP monitors CC for CTVPD detach for tVPDDetach and when detected, enters Unattached.SNK
   f. DRP monitors VBUS for CTVPD Charge-Through source attach and, when detected, enters CTAttached.SNK

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

a. DRP（作为源）通过 *USB PD*（发现身份
命令）在 SOP ’ 上 b. CTVPD 在 SOP ’ 上做出响应，宣布它是通过 VCONN 充电的 USB 设备 c. DRP（作为源）移除 VBUS d. DRP（作为源）将其 Rp 更改为 Rd e. DRP（作为接收器）继续提供 VCONN 并进入 CTUnattached.SNK

5. CTVPD 转换为 CTUnattached.VPD

a. CTVPD 检测到 VBUS 移除、VCONN 存在以及主机端口上的低 CC 引脚，并进入 CTUnattached.VPD b. CTVPD 将其主机端 Rd 更改为 Rp 终端，通告 3.0 A c. CTVPD 将自身与 VBUS 隔离 d. CTVPD 将 Rd 应用于其 Charge-Through 端口的 CC1 和 CC2 引脚

6. CTVPD 在 CTUnattached.VPD 和 CTUnattached.Unsupported 之间交替

a. CTVPD 在其 Charge-Through CC 引脚上检测到 SRC.Open，并开始在 CTUnattached.VPD 和 CTUnattached.Unsupported 之间交替

7. CTVPD 通过 CTAttachWait.Unsupported 从 CTUnattached.Unsupported 转换为 CTTry.SNK

a. CTUnattached.Unsupported 中的 CTVPD 检测到 Unattached.SNK 中的 Sink 的 CC 下拉，并且 CTVPD 进入 CTAttachWait.Unsupported b. CTAttachWait.Unsupported 中的 CTVPD 检测到 CC 上的下拉持续了 tCCDebounce 并进入 CTTry.SNK c. CTVPD 禁用 Rp 终止广告 在 Charge-Through 端口的 CC 引脚上启用默认 USB 电源 d. CTVPD 在 Charge-Through 端口的 CC 引脚上启用 Rd

8. CTVPD 从 CTTry.SNK 转换为 CTAttached.Unsupported

a. CTVPD 在 tDRPTry 之后未检测到 tDRPTryWait 潜在源的 CC 上拉，并进入 CTAttached.Unsupported

9. 当 CTVPD 处于 CTAttached.Unsupported 状态、DRP 处于 CTUnattached.SNK 状态且 Sink 处于 Unattached.SNK 状态时：

a. CTVPD 禁用 Charge-Through 端口 CC 引脚上的 Rd 终端，并应用 Rp 终端通告默认 USB 电源 b. CTVPD 向 DRP 公开 USB 广告牌设备类，表明它已连接到 Charge-Through 端口上不受支持的设备 c. CTVPD 监控 Charge-Through CC 引脚以检测 Sink 断开情况，当检测到时，

进入 CTUnattached.VPD d. CTVPD 监控 VCONN 以检测主机分离，检测到后进入 Unattached.SNK e. DRP 监控 CC 以检测 tVPDDetach 的 CTVPD 分离，检测到后进入 Unattached.SNK f. DRP 监控 VBUS 以检测 CTVPD 充电源连接，检测到后进入 CTAttached.SNK

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

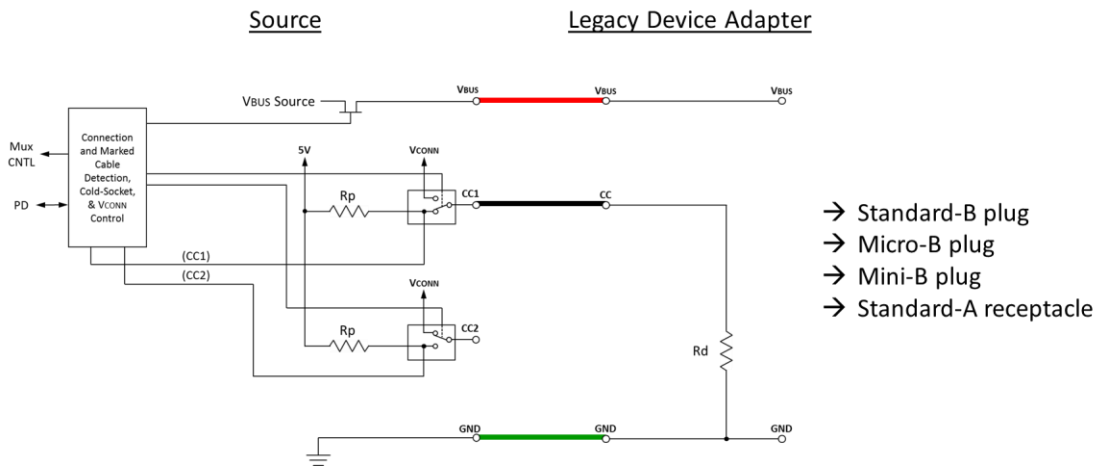
4.5.3.2 USB Type-C port to Legacy Port Interoperability Behaviors

The following sub-sections describe port-to-port interoperability behaviors for the various combinations of USB Type-C Source, Sink and DRPs and legacy USB ports.

4.5.3.2.1 Source to Legacy Device Port Behavior

Figure 4-30 illustrates the functional model for a Source connected to a legacy device port. This model is based on having an adapter present as a Sink to the Source. This adapter has a USB Type-C plug on one end plugged into the Source and either a USB Standard-B plug, USB Micro-B plug, USB Mini-B plug, or a USB Standard-A receptacle on the other end.

Figure 4-30 Source to Legacy Device Port Functional Model



The following describes the behavior when a Source is connected to a legacy device adapter that has an Rd to ground so as to mimic the behavior of a Sink.

1. Source in the unattached state
2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   - Source detects the Sink's pull-down on CC and enters AttachWait.SRC. After tCCDebounce, it enters Attached.SRC.
   - Source turns on VBUS and VCONN
3. While the Source is in the attached state:
   - Source monitors CC for detach and when detected, enters Unattached.SRC

4.5.3.2.2 Legacy Host Port to Sink Behavior

Figure 4-31 illustrates the functional model for a legacy host port connected to a Sink. This model is based on having an adapter that presents itself as a Source to the Sink, this adapter is either a USB Standard-A legacy plug or a USB Micro-B legacy receptacle on one end and the USB Type-C plug on the other end plugged into a Sink.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

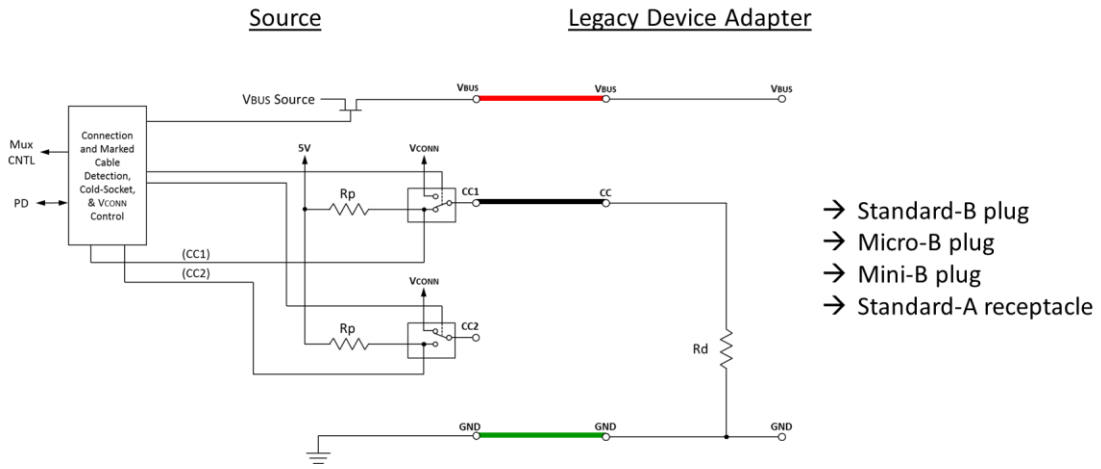
4.5.3.2 USB Type-C 端口与传统端口互操作性行为

以下小节描述了 USB Type-C 源端、接收端和 DRP 以及传统 USB 端口的各种组合的端口到端口互操作性行为。

4.5.3.2.1 源到旧设备端口行为

图 4-30 说明了连接到旧设备端口的源的功能模型。此模型基于将适配器作为源的接收器。此适配器的一端有一个 USB Type-C 插头插入源，另一端有一个 USB 标准-B 插头、USB Micro-B 插头、USB Mini-B 插头或 USB 标准-A 插座。

如图 Figure 4-30 源到旧设备端口功能模型



下面描述了当源端连接到具有 Rd 接地的传统设备适配器时的行为，以模拟接收器的行为。

1. 源处于未连接状态 2. 源通过 AttachWait.SRC 从 Unattached.SRC 转换到 Attached.SRC

   - Source 检测到 Sink 的 CC 下拉，进入 AttachWait.SRC。经过 tCCDebounce 后，进入 Attached.SRC。• Source 打开 VBUS 和 VCONN

3. 当源处于连接状态时：

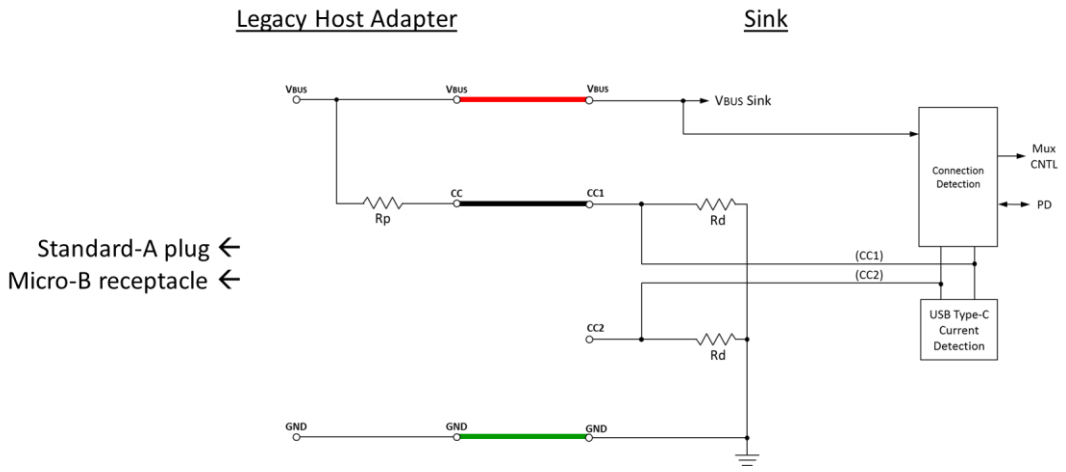
   - 源监控 CC 是否断开连接，检测到断开连接后，进入 Unattached.SRC

4.5.3.2.2 传统主机端口到接收器行为

图 4-31 显示了连接到 Sink 的传统主机端口的功能模型。此模型基于一个适配器，该适配器将自身作为 Sink 的 Source，该适配器一端是 USB Standard-A 传统插头或 USB Micro-B 传统插座，另一端是插入 Sink 的 USB Type-C 插头。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-31 Legacy Host Port to Sink Functional Model

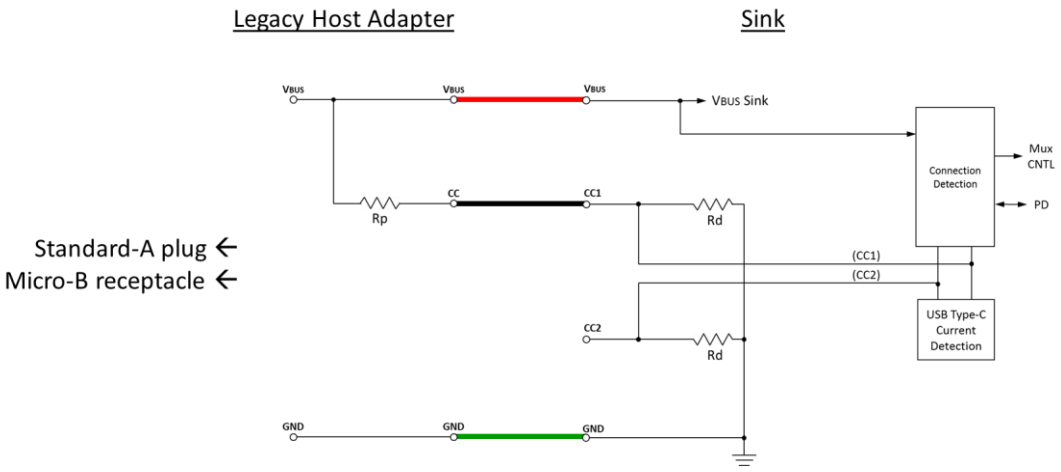


The following describes the behavior when a legacy host adapter that has an Rp to VBUS so as to mimic the behavior of a Source that is connected to a Sink. The value of Rp shall indicate an advertisement of Default USB Power (See Table 4-24), even though the cable itself can carry 3 A. This is because the cable has no knowledge of the capabilities of the power source, and any higher current is negotiated via *USB BC 1.2*.

1. Sink in the unattached state
2. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK if needed.
   - While in Unattached.SNK, if device is not USB 2.0 only, supports accessories or requires more than default power, it enters AttachWait.SNK when it detects a pull up on CC and ignores VBUS. Otherwise, it may enter Attached.SNK directly when VBUS is detected.
   - Sink detects VBUS and enters Attached.SNK
3. While the Sink is in the attached state:
   - Sink monitors VBUS for detach and when detected, enters Unattached.SNK

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-31 传统主机端口至接收器功能模型



下面描述了当传统主机适配器具有 Rp 到 VBUS 以模拟连接到接收器的源的行为时的行为。Rp 的值应指示默认 USB 电源的通告（见表 4-24），即使电缆本身可以承载 3 A。这是因为电缆不知道电源的能力，任何更高的电流都是通过 *USB BC 1.2* 协商的。

1. 接收器处于未连接状态 2. 如果需要，接收器通过 AttachWait.SNK 从 Unattached.SNK 转换到 Attached.SNK。

- 在 Unattached.SNK 中，如果设备不是仅 USB 2.0、支持配件或需要超过默认功率，则当检测到 CC 上拉时，它会进入 AttachWait.SNK 并忽略 VBUS。否则，当检测到 VBUS 时，它可能直接进入 Attached.SNK。• Sink 检测到 VBUS 并进入 Attached.SNK

3. 当水槽处于连接状态时：

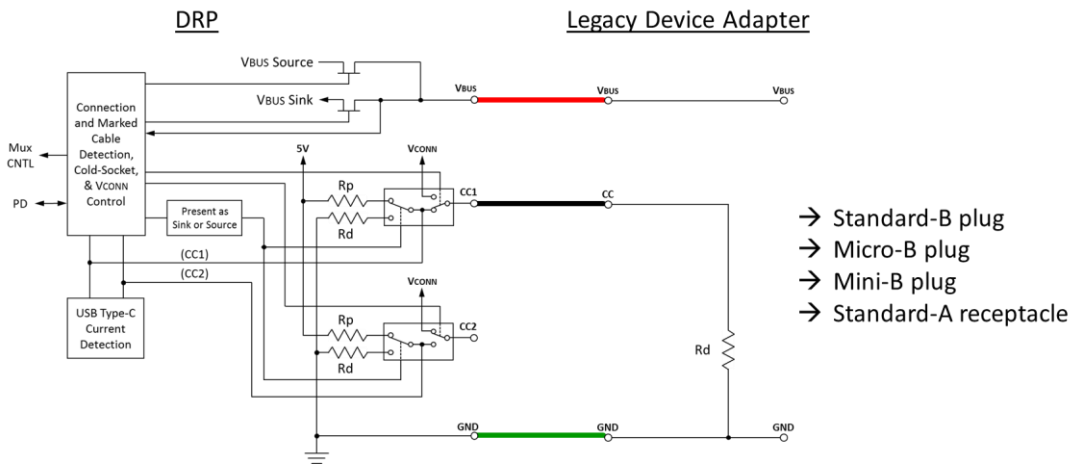
- Sink 监控 VBUS 是否断开连接，检测到断开连接后，进入未连接状态。SNK

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.3.2.3 DRP to Legacy Device Port Behavior

Figure 4-32 illustrates the functional model for a DRP connected to a legacy device port. This model is based on having an adapter present as a Sink (Device) to the DRP. This adapter has a USB Type-C plug on one end plugged into a DRP and either a USB Standard-B plug, USB Micro-B plug, USB Mini-B plug, or a USB Standard-A receptacle on the other end.

Figure 4-32 DRP to Legacy Device Port Functional Model



The following describes the behavior when a DRP is connected to a legacy device adapter that has an Rd to ground so as to mimic the behavior of a Sink.

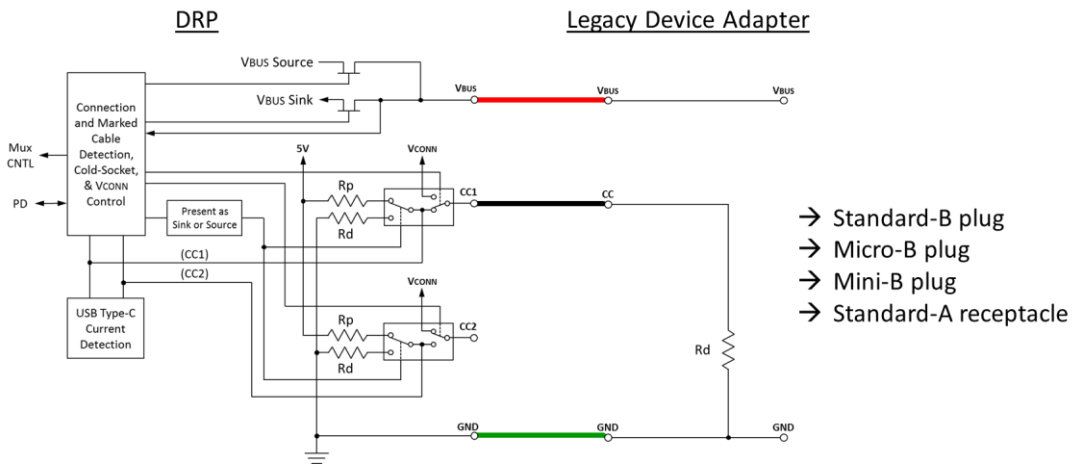
1. DRP in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. DRP transitions from Unattached.SRC to Attached.SRC
   - DRP in Unattached.SRC detects the adapter's pull-down on CC and enters AttachWait.SRC
   - DRP in AttachWait.SRC times out (tCCDebounce) and transitions to Attached.SRC
   - DRP in Attached.SRC turns on VBUS and VCONN
   - DRP in AttachWait.SRC may support Try.SNK and if so, may transition through Try.SNK and TryWait.SRC prior to entering Attached.SRC
3. While the DRP is in the attached state:
   - DRP monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.3.2.3 DRP 到传统设备端口行为

图 4-32 说明了连接到传统设备端口的 DRP 的功能模型。此模型基于将适配器作为 DRP 的接收器（设备）存在。此适配器的一端有一个 USB Type-C 插头，插入 DRP，另一端有一个 USB 标准 B 插头、USB Micro-B 插头、USB Mini-B 插头或 USB 标准 A 插座。

图 4-32 DRP 至传统设备端口功能模型



下面描述了当 DRP 连接到具有 Rd 接地的传统设备适配器时的行为，以模拟 Sink 的行为。

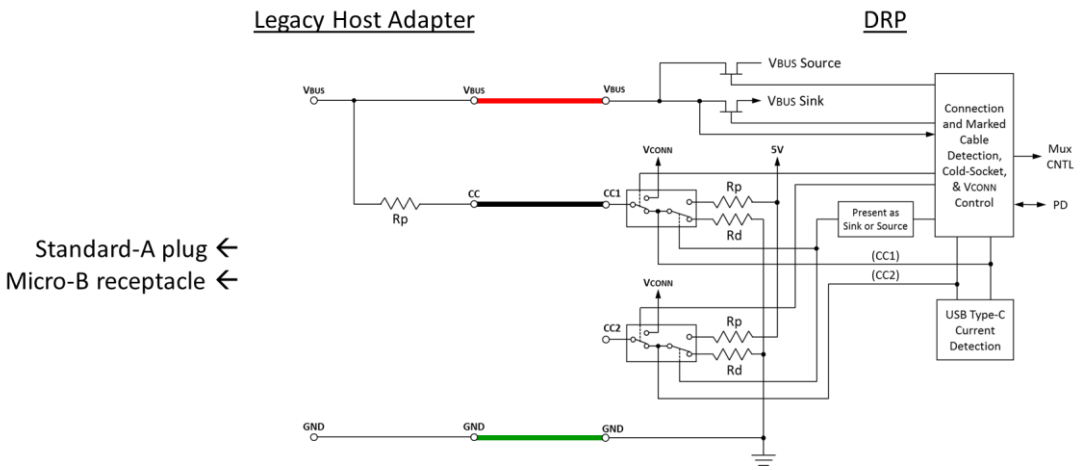
1. 未连接状态下的 DRP
   - DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替
2. DRP 从 Unattached.SRC 转换为 Attached.SRC
   - Unattached.SRC 中的 DRP 检测到适配器在 CC 上的下拉并进入 AttachWait.SRC • AttachWait.SRC 中的 DRP 超时 (tCCDebounce) 并转换到 Attached.SRC • Attached.SRC 中的 DRP 打开 VBUS 和 VCONN • AttachWait.SRC 中的 DRP 可能支持 Try.SNK，如果是，则可能在进入 Attached.SRC 之前通过 Try.SNK 和 TryWait.SRC 进行转换
3. 当 DRP 处于附着状态时：
   - DRP 监控 CC 是否分离，当检测到时，进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换）

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.3.2.4 Legacy Host Port to DRP Behavior

Figure 4-33 illustrates the functional model for a legacy host port connected to a DRP operating as a Sink. This model is based on having an adapter that presents itself as a Source (Host) to the DRP operating as a Sink, this adapter is either a USB Standard-A legacy plug or a USB Micro-B legacy receptacle on one end and the USB Type-C plug on the other end plugged into a DRP.

Figure 4-33 Legacy Host Port to DRP Functional Model



The following describes the behavior when a legacy host adapter that has an Rp to VBUS so as to mimic the behavior of a Source is connected to a DRP. The value of Rp shall indicate an advertisement of Default USB Power (See Table 4-24), even though the cable itself can carry 3 A. This is because the cable has no knowledge of the capabilities of the power source, and any higher current is negotiated via *USB BC 1.2*.

1. DRP in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. DRP transitions from Unattached.SNK to AttachWait.SNK to Attached.SNK
   - DRP in Unattached.SNK detects pull up on CC and enters AttachWait.SNK.
   - DRP in AttachWait.SNK detects VBUS and enters Attached.SNK
   - DRP in AttachWait.SNK may support Try.SRC and if so, may transition through Try.SRC and TryWait.SNK prior to entering Attached.SNK
3. While the DRP is in the attached state:
   - DRP monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

4.6 Power

Power delivery over the USB Type-C connector takes advantage of the existing USB methods as defined by: the *USB 2.0* and *USB 3.2* specifications, the *USB BC 1.2* specification and the *USB Power Delivery* specification. Power for *USB4* operation requires a *USB PD* explicit contract as defined in Section 5.3 and the *USB Power Delivery* specification. Prior to entering a *USB PD* explicit contract, a *USB4* port operates as a *USB 3.2* port regarding power.

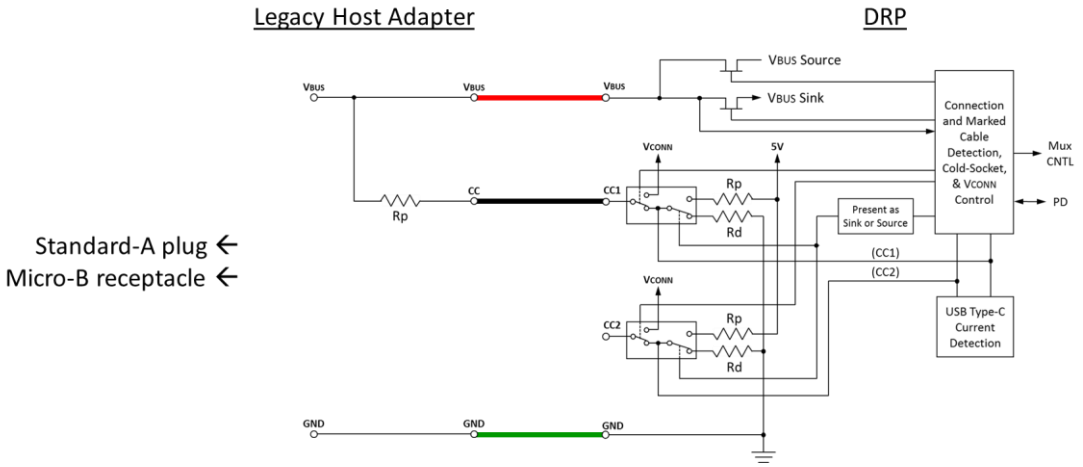
The USB Type-C Current mechanism allows the Source to offer more current than defined by the *USB BC 1.2* specification. A USB power source shall not provide more than 20 V nominal

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.5.3.2.4 传统主机端口到 DRP 行为

图 4-33 说明了连接到作为接收器的 DRP 的传统主机端口的功能模型。此模型基于一个适配器，该适配器将自己呈现为接收器的 DRP 的源（主机），该适配器一端是 USB 标准 A 传统插头或 USB Micro-B 传统插座，另一端是插入 DRP 的 USB Type-C 插头。

图 4-33 传统主机端口至 DRP 功能模型



下面描述了当旧式主机适配器具有 Rp 至 VBUS 以模仿源的行为并连接到 DRP 时的行为。Rp 的值应指示默认 USB 电源的通告（见表 4-24），即使电缆本身可以承载 3 A 的电流。这是因为电缆不了解电源的能力，任何更高的电流都是通过 *USB BC 1.2* 协商的。

1. 未连接状态下的 DRP

• DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替 2. DRP 从 Unattached.SNK 转换为 AttachWait.SNK 再转换为 Attached.SNK • Unattached.SNK 中的 DRP 检测到 CC 上的上拉并进入 AttachWait.SNK。• AttachWait.SNK 中的 DRP 检测到 VBUS 并进入 Attached.SNK • AttachWait.SNK 中的 DRP 可能支持 Try.SRC，如果是，则可能通过

在进入 Attached.SNK 之前 Try.SRC 和 TryWait.SNK

3. 当 DRP 处于附着状态时：

• DRP 监控 VBUS 是否断开，检测到断开后进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换）

4.6 电源

通过 USB Type-C 连接器供电可利用现有的 USB 方法，具体定义如下：*USB 2.0* 和 *USB 3.2* 规范、*USB BC 1.2* 规范和 *USB Power Delivery* 规范。*USB4* 操作的供电需要第 5.3 节和 *USB Power Delivery* 规范中定义的 *USB PD* 显式合同。在输入 *USB PD* 显式合同之前，*USB4* 端口在供电方面充当 *USB 3.2* 端口。

USB Type-C 电流机制允许电源提供超过 *USB BC 1.2* 规范定义的电流。USB 电源不得提供超过 20 V 的标称值

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

on VBUS. *USB PD* power sources that deliver power over a USB Type-C connector shall follow the power rules as defined in Section 10 of the *USB Power Delivery* specification.

All USB Type-C-based devices shall support USB Type-C Current and may support other USB-defined methods for power. The following order of precedence of power negotiation shall be followed: *USB BC 1.2* supersedes the *USB 2.0* and *USB 3.2* specifications, USB Type-C Current at 1.5 A and 3.0 A supersedes *USB BC 1.2*, and *USB Power Delivery* supersedes USB Type-C Current. Table 4-17 summarizes this order of precedence of power source usage.

Table 4-17 Precedence of power source usage

Precedence	Mode of Operation		Nominal Voltage	Maximum Current
Highest	*USB PD*		Configurable	5 A
	USB Type-C Current @ 3.0 A		5 V	3.0 A
↓	USB Type-C Current @ 1.5 A		5 V	1.5 A
	USB BC 1.2		5 V	Up to 1.5 A[1]
	Default USB Power	*USB 3.2*	5 V	See USB 3.2
Lowest		*USB 2.0*	5 V	See USB 2.0

Notes:

1. *USB BC 1.2* permits a power provider to be designed to support a level of power between 0.5 A and 1.5 A. If the *USB BC 1.2* power provider does not support 1.5 A, then it is required to follow power droop requirements. A *USB BC 1.2* power consumer may consume up to 1.5 A provided that the voltage does not drop below 2 V, which may occur at any level of power above 0.5 A.

For example, once the PD mode (e.g. a power contract has been negotiated) has been entered, the device shall abide by that power contract ignoring any other previously made or offered by the USB Type-C Current, *USB BC 1.2* or *USB 2.0* and *USB 3.2* specifications. When the PD mode is exited, the device shall fallback in order to the USB Type-C Current, *USB BC 1.2* or *USB 2.0* and *USB 3.2* specification power levels.

All USB Type-C ports shall tolerate being connected to USB power source supplying default USB power, e.g. a host being connected to a legacy USB charger that always supplies VBUS.

4.6.1 Power Requirements during USB Suspend

USB Type-C implementations with USB Type-C Current, *USB PD* and VCONN, along with active cables, requires the need to expand the traditional USB suspend definition.

4.6.1.1 VBUS Requirements during USB Suspend

The *USB 2.0* and *USB 3.2* specifications define the amount of current a Sink is allowed to consume during suspend.

USB suspend power rules shall apply when the USB Type-C Current is at the Default USB Power level or when *USB PD* is being used and the Suspend bit is set appropriately.

When USB Type-C Current is set at 1.5 A or 3.0 A, the Sink is allowed to continue to draw current from VBUS during USB suspend. During USB suspend, the Sink's requirement to track and meet the USB Type-C Current advertisement remains in force (See Section 4.5.2.3).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

在 VBUS 上。通过 USB Type-C 连接器供电的 *USB PD* 电源应遵循 *USB Power Delivery* 规范第 10 节中定义的电源规则。

所有基于 USB Type-C 的设备都应支持 USB Type-C Current，并可支持 USB 定义的其他供电方法。应遵循以下电源协商优先顺序：*USB BC 1.2* 取代 *USB 2.0* 和 *USB 3.2* 规范，1.5 A 和 3.0 A 的 USB Type-C Current ~~取代 *USB BC 1.2*~~，*USB Power Delivery* 取~~代 USB~~ Type-C Current。~~表 4-17 总结~~了电源使用优先顺序。

表4-17 电源使用优先顺序

Precedence	Mode of Operation		Nominal Voltage	Maximum Current
Highest	*USB PD*		Configurable	5 A
	USB Type-C Current @ 3.0 A		5 V	3.0 A
↓	USB Type-C Current @ 1.5 A		5 V	1.5 A
	USB BC 1.2		5 V	Up to 1.5 A[1]
	Default USB Power	*USB 3.2*	5 V	See USB 3.2
Lowest		*USB 2.0*	5 V	See USB 2.0

注：1. *USB BC 1.2* 允许电源设计为支持 0.5 A 至 1.5 A 之间的功率水平。如果 *USB BC 1.2* 电源不支持 1.5 A，则需要遵循功率下降要求。*USB BC 1.2* 电源消费者最多可以消耗 1.5 A 的电流，前提是电压不会低于 2 V，这可能发生在任何高于 0.5 A 的功率水平下。

例如，一旦进入 PD 模式（例如已协商好供电合同），设备应遵守该供电合同，忽略 USB Type-C Current、*USB BC 1.2* 或 *USB 2.0* 和 *USB 3.2* 规范之前制定或提供的任何其他合同。退出 PD 模式后，设备应回退到 ~~USB Type-C Current、*USB BC*、*1.2*~~ 或 ~~*USB 2.0*~~ 和 ~~*USB 3.2*~~ 规范的功率级别。

所有 USB Type-C 端口均可连接到提供默认 USB 电源的 USB 电源，例如，主机连接到始终提供 VBUS 的传统 USB 充电器。

4.6.1 USB 暂停期间的电源要求

采用 USB Type-C Current、*USB PD* 和 VCONN 以及有源电缆的 USB Type-C 实现需要扩展传统的 USB 暂停定义。

4.6.1.1 USB 暂停期间的 VBUS 要求

USB 2.0 和 *USB 3.2* 规范定义了 Sink 在挂起期间允许消耗的电流量。

当 USB Type-C 电流处于默认 USB 电源级别或使用 *USB PD* 且暂停位设置适当时，应适用 USB 暂停电源规则。

当 USB Type-C 电流设置为 1.5 A 或 3.0 A 时，Sink 可以在 USB 挂起期间继续从 VBUS 汲取电流。在 USB 挂起期间，Sink 跟踪和满足 USB Type-C 电流通告的要求仍然有效（参见第 4.5.2.3 节）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

USB PD provides a method for the Source to communicate to the Sink whether or not the Sink has to follow the USB power rules for suspend.

4.6.1.2 VCONN Requirements during USB Suspend

If the Source supplies VBUS power during USB suspend, it shall also supply VCONN and meet the requirements defined in Table 4-5.

Electronically Marked Cables shall meet the requirements in Table 4-6 during USB suspend.

VCONN powered accessories shall meet the requirements defined in Table 4-7 during USB suspend.

4.6.2 VBUS Power Provided Over a USB Type-C Cable

The minimum requirement for VBUS power supplied over the USB Type-C cable assembly matches the existing requirement for VBUS supplied over existing legacy USB cable assemblies. *USB Power Delivery* is intended to work over un-modified USB Type-C to USB Type-C cables, therefore any USB Type-C cable assembly that incorporates electrical components or electronics shall ensure that it tolerate, or be protected from, a VBUS voltage of 21 V.

4.6.2.1 USB Type-C Current

Default USB voltage and current are defined by the *USB 2.0* and *USB 3.2* specifications. All USB Type-C Current advertisements are at the USB VBUS voltage defined by these specifications.

The USB Type-C Current feature provides the following extensions:

- Higher current than defined by the *USB 2.0*, the *USB 3.2* or the *BC 1.2* specifications
- Allows the power source to manage the current it provides

The USB Type-C connector uses CC pins for configuration including an ability for a Source to advertise to its port partner (Sink) the amount of current it shall supply:

- Default is the as-configured for high-power operation current value as defined by the USB Specification (500 mA for USB 2.0 ports; 900 mA or 1,500 mA for *USB 3.2* ports in single-lane or dual-lane operation, respectively)
- 1.5 A
- 3.0 A

When a Source is advertising USB Type-C Default current, the Sink behavior is defined as follows:

- It connects as a *USB 2.0* or *USB 3.2* device, after which the Sink shall follow the appropriate USB specification.
- It enters a *USB PD* contract, after which the Sink shall follow the *USB PD* specification to determine the current (e.g., Rp will no longer be Default as it is superseded by the *USB PD* contract).
- It detects a USB BC 1.2 charging port, after which the Sink shall follow the USB BC 1.2 specification.
- It attaches as a USB Type-C Power Sinking Device (PSD), after which the Sink may draw up to 500 mA.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

USB PD 提供了一种方法，让源端与接收器沟通，了解接收器是否必须遵循 USB 电源挂起规则
。

4.6.1.2 USB 暂停期间的 VCONN 要求

如果源在 USB 挂起期间提供 VBUS 电源，则它也应为 VCONN 供电并满足表 4-5 中定义的要求。

USB 暂停期间，电子标记电缆应满足表 4-6 中的要求。

USB 暂停期间，VCONN 供电配件应满足表 4-7 中定义的要求。

4.6.2 通过 USB Type-C 电缆提供的 VBUS 电源

通过 USB Type-C 电缆组件提供的 VBUS 电源的最低要求与通过现有传统 USB 电缆组件提供的 V
BUS 电源的现有要求一致。*USB Power Delivery* 旨在通过未修改的 USB Type-C 到 USB Type-C
电缆工作，因~~此任何包含电气元件~~或电子设备的 USB Type-C 电缆组件都应确保其能够承受或免受
VBUS 电压的影响

21 V。

4.6.2.1 USB Type-C 电流

默认 USB 电压和电流由 *USB 2.0* 和 *USB 3.2* 规范定义。所有 USB Type-C 电流通告均处于这些规
范定义的 USB VBUS 电压。

USB Type-C 电流特性提供以下扩展：

- 电流高于 *USB 2.0*、*USB 3.2* 或 *BC 1.2* 规格所定义的电流 • 允许电源管理其提供的电流

USB Type-C 连接器使用 CC 引脚进行配置，包括源端向其端口伙伴（接收器）通告其应提供的电流
量的能力：

- 默认值为 USB 规范定义的高功率操作电流值（USB 2.0 端口为 500 mA；单通道或双通道操作
中 *USB 3.2* 端口分别为 900 mA 或 1,500 mA）• 1.5 A • 3.0 A

当源端广播 USB Type-C 默认电流时，吸端行为定义如下：

- 它作为 *USB 2.0* 或 *USB 3.2* 设备连接，此后 Sink 应遵循相应的 USB 规范。• 它进入 *USB PD*
合同，此后 Sink 应遵循 *USB PD* 规范

来确定电流（例如，Rp 将不再是默认值，因为它已被 *USB PD* 合同取代）。• 它检测到 US
B BC~~ 1.2 充~~电端口，此后 Sink 应遵循 USB BC 1.2 规范。• 它作为 USB Type-C 电源接收设备 (P
SD) 连接，此后 Sink 可能会吸收高达 500 mA 的电流。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A PSD shall fully support USB Type-C Current operation, should support *USB PD* and may support USB BC 1.2. A PSD may be a Sink or a DRP operating in Sink mode. A PSD shall not have a USB or USB Type-C Alternate Mode communications function.

The relationship of USB Type-C Current and the equivalent *USB PD* Power (PDP) value is shown in Table 4-18.

Table 4-18 USB Type-C Current Advertisement and PDP Equivalent

USB Type-C Current		PDP Equivalent
Default	500 mA (*USB 2.0*)	2.5 W
	900 mA (*USB 3.2* single-lane)	4.5 W
	1,500 mA (*USB 3.2* dual-lane)	7.5 W
1.5 A		7.5 W
3.0 A		15 W

A Sink that takes advantage of the additional current offered (e.g., 1.5 A or 3.0 A) shall monitor the CC pins and shall adjust its current consumption within tSinkAdj to remain within the value advertised by the Source. While a *USB PD* contract is in place, a Sink is not required to monitor USB Type-C current advertisements and shall not respond to USB Type-C current advertisements.

The Source shall supply VBUS to the Sink within tVBUSON. VBUS shall be in the specified voltage range at the advertised current.

A Source (port supplying VBUS) shall protect itself from a Sink that draws current in excess of the port's USB Type-C Current advertisement.

The Source adjusts Rp (or current source) to advertise which of the three current levels it supports. See Table 4-24 for the termination requirements for the Source to advertise currents.

The value of Rp establishes a voltage (vRd) on CC that is used by the Sink to determine the maximum current it may draw.

Table 4-35 defines the CC voltage range observed by the Sink that only support default USB current.

If the Sink wants to consume more than the default USB current, it shall track vRd to determine the maximum current it may draw. See Table 4-36.

Figure 4-34 and Figure 4-35 illustrate where the Sink monitors CC for vRd to detect if the host advertises more than the default USB current.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

PSD 应完全支持 USB Type-C 电流操作，应支持 *USB PD* 并可支持 USB BC 1.2。PSD 可以是 Sink 或以 Sink 模式运行的 DRP。PSD 不得具有 USB 或 USB Type-C 备用模式通信功能。

USB Type-C Current与等效*USB PD*Power（PDP）值关系如表4-18所示。

表 4-18 USB Type-C 电流通告和 PDP 等效

USB Type-C Current		PDP Equivalent
Default	500 mA (*USB 2.0*)	2.5 W
	900 mA (*USB 3.2* single-lane)	4.5 W
	1,500 mA (*USB 3.2* dual-lane)	7.5 W
1.5 A		7.5 W
3.0 A		15 W

利用提供的额外电流（例如 1.5 A 或 3.0 A）的 Sink 应监控 CC 引脚，并应在 tSinkAdj 内调整其电流消耗，以保持在 Source 所通告的值范围内。在 *USB PD* 合同生效期间，Sink 无需监控 USB Type-C 电流通告，也不应对 USB Type-C 电流通告做出响应。

源端应在 tVBUSON 内向吸端提供 VBUS。VBUS 应在标称电流下处于指定电压范围内。

源端（提供 VBUS 的端口）应保护自己，以免受到吸收端（吸收的电流超过端口的 USB Type-C 电流公告）的影响。

源端调整 Rp（或电流源）以通告其支持三种电流等级中的哪一种。有关源端通告电流的终端要求，请参阅表 4-24。

Rp 的值在 CC 上建立了一个电压 (vRd)，Sink 使用该电压来确定其可能吸收的最大电流。

表 4-35 定义了仅支持默认 USB 电流的 Sink 观察到的 CC 电压范围。

如果 Sink 想要消耗超过默认 USB 电流，它应跟踪 vRd 以确定其可能消耗的最大电流。见表 4-36。

图 4-34 和图 4-35 说明了 Sink 监视 CC 中的 vRd，以检测主机是否通告超过默认 USB 电流。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-34 Sink Monitoring for Current in Pull-Up/Pull-Down CC Model

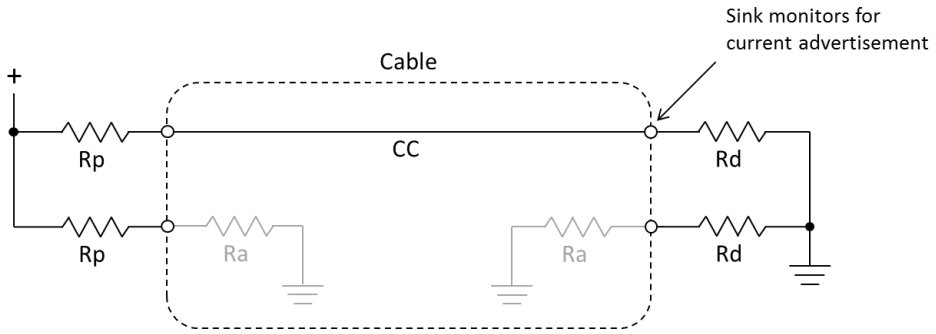
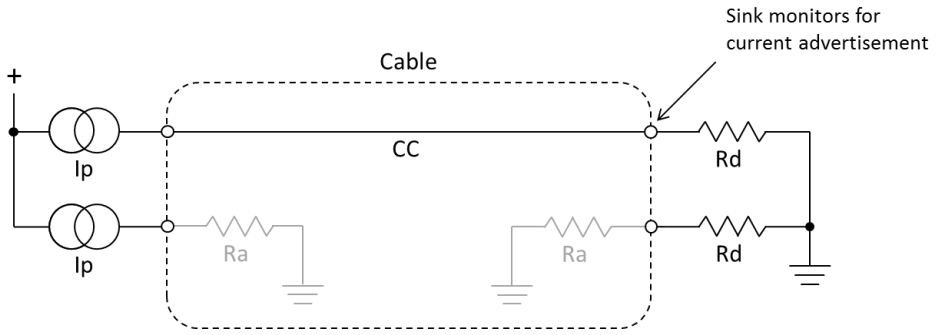


Figure 4-35 Sink Monitoring for Current in Current Source/Pull-Down CC Model



4.6.2.2 USB Battery Charging 1.2

USB Battery Charging Specification, Revision 1.2 defines a method that uses the USB 2.0 D+ and D− pins to advertise VBUS can supply up to 1.5 A. Support for *USB BC 1.2* charging is optional.

A USB Type-C port that implements *BC 1.2* that is capable of supplying at least 1.5 A shall advertise USB Type-C Current at the 1.5 A level within tVBUSON of entering the Attached.SRC state, otherwise the port shall advertise USB Type-C Current at the Default USB Power level. A USB Type-C port that implements *BC 1.2* that also supports USB Type-C Current at 3.0 A may advertise USB Type-C Current at 3.0 A.

If a Sink that supports *BC 1.2* detection, detects Rp at the Default USB Power level and does not discover a *BC 1.2*-compliant Source, then it shall limit its maximum current consumption to the standard USB levels based on Table 4-17. This will ensure maximum current limits are not exceeded when connected to a Source which does not support *BC 1.2*.

4.6.2.3 Proprietary Power Source

This section has been deprecated. Devices with USB Type-C connectors shall only employ signaling methods defined in USB specifications to negotiate power.

4.6.2.4 USB Power Delivery

USB Power Delivery is a feature on the USB Type-C connector. When *USB PD* is implemented, *USB PD* Bi-phase Mark Coded (BMC) carried on the CC wire shall be used for *USB PD* communications between USB Type-C ports.

At attach, VBUS shall be operationally stable prior to initiating *USB PD* communications.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-34 上拉/下拉 CC 模型中的电流吸收监测

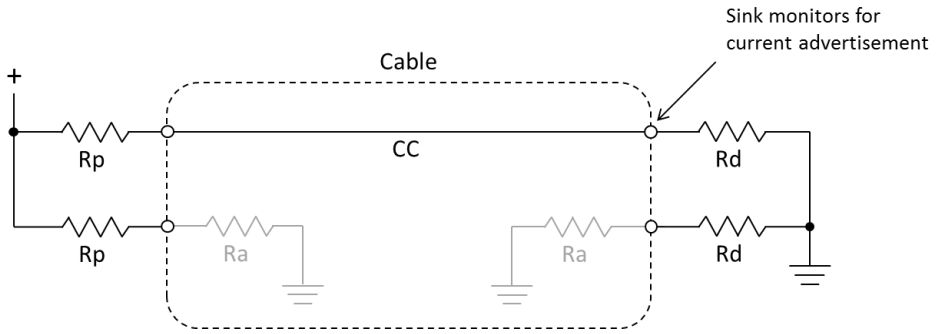
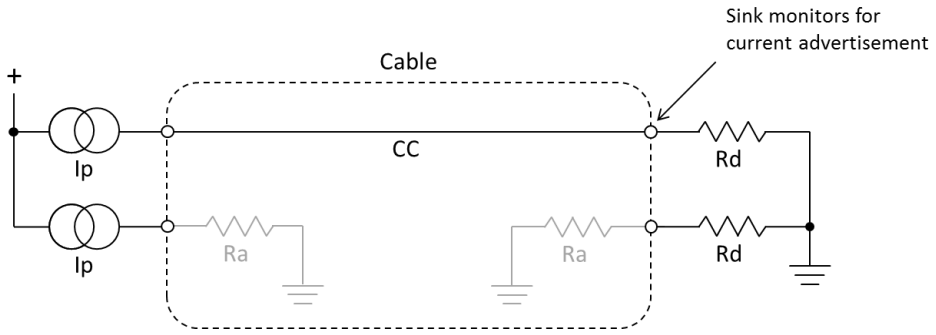


图 4-35 电流源/下拉 CC 模型中的电流吸收器监控



4.6.2.2 USB 电池充电 1.2

USB Battery Charging Specification, Revision 1.2 定义了一种使用 USB 2.0 D+ 和 D– 引脚的方法来宣传 VBUS 可以提供高达 1.5 A 的电流。对 *USB BC 1.2* 充电的支持~~是可选的。~~

实现 *BC 1.2* 且能够提供至少 1.5 A 电流的 USB Type-C 端口应在进入 Attached.SRC 状态的 tVBUSON 内以 1.5 ~~A 级别通告 USB Type~~-C 电流，否则端口应以默~~认 USB 功~~率级别通告 USB ~~Type-C 电流~~。实现 *BC 1.2* 且支持 3.0 A USB Type-C 电流~~的 USB Type-C 端口~~可以以 3.0 A 级别通告 USB Type-C 电流。

如果支持 *BC 1.2* 检测的 Sink 在默认 USB 电源级别检测到 Rp 且未发现符合 *BC 1.2* 的 Source，则它应根据表 4-17 将~~其最~~大电流消耗限制为标准 USB 级别。这将确保在连接到不支持 *BC 1.2* 的 Source 时不会超过最大电流限制。

4.6.2.3 专有电源

此部分已弃用。带有 USB Type-C 连接器的设备应仅采用 USB 规范中定义的信号传输方法来协商电源。

4.6.2.4 USB 供电

USB Power Delivery 是 USB Type-C 连接器上的一项功能。实施 *USB PD* 时，CC 线上承载的 ~~*USB PD*~~ 双相标记编码 (BMC) 将用于 USB Type-C 端口之间的 *USB PD* 通信。

连接时，VBUS 应在启动 *USB PD* 通信之前处于运行稳定状态。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-36 illustrates how the *USB PD* BMC signaling is carried over the USB Type-C cable's CC wire.

Figure 4-36 USB PD over CC Pins

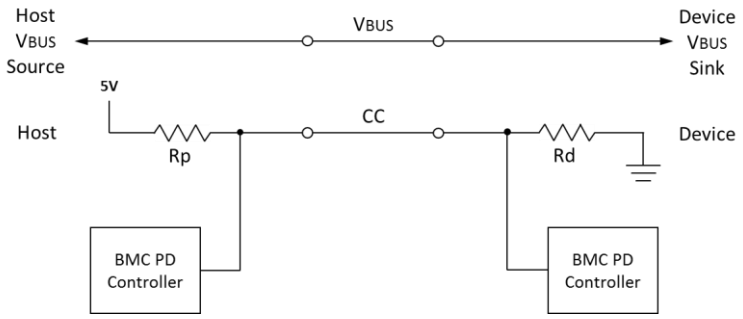
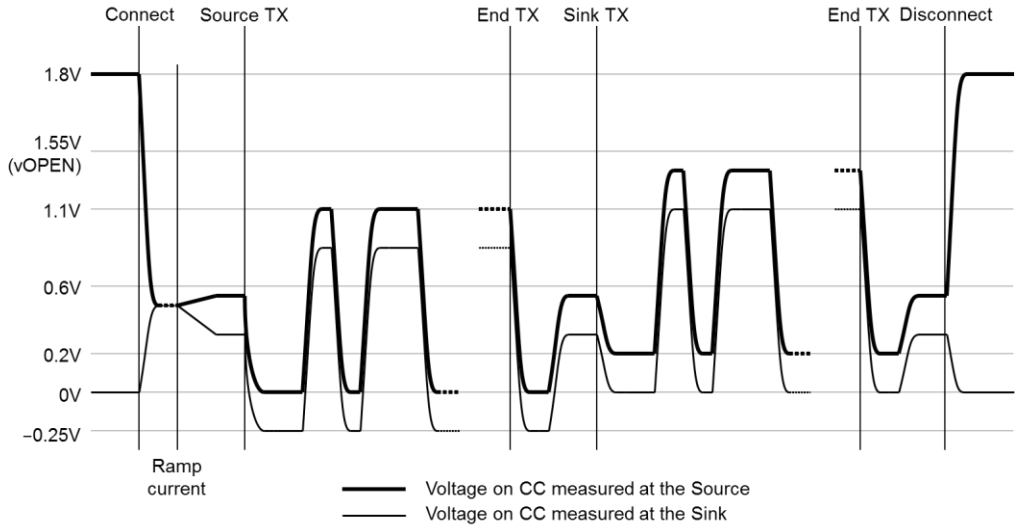


Figure 4-37 illustrates *USB PD* BMC signaling as seen on CC from both the perspective of the Source and Sink. The breaks in the signaling are intended to represent the passage of time.

Figure 4-37 USB PD BMC Signaling over CC



When not in an Explicit Contract, *USB PD* Sources that are, based on their PDP, capable of supplying:

- 5 V at 3 A or greater shall advertise USB Type-C Current at the 3 A level
- 5 V at 1.5A or greater but less than 3 A shall advertise USB Type-C Current at the 1.5 A level
- 5 V at less than 1.5A shall advertise USB Type-C Current at the Default USB Power level

within tVBUSON of entering the Attached.SRC state. For Multi-Port Shared Capacity Chargers, a *USB PD* Source capable of supplying 5 V at 3A or greater may initially offer USB Type-C Current at the 1.5 A level and subsequently increase the offer after attach (see Section 4.8.6.2). During USB Suspend a *USB PD* Source may set its Rp value to default to indicate that the Sink shall only draw USB suspend current as defined in Section 4.6.1.1.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-36 说明了 *USB PD* BMC 信号如何通过 USB Type-C 电缆的 CC 线传输。

图 4-36 USB PD 通过 CC 引脚

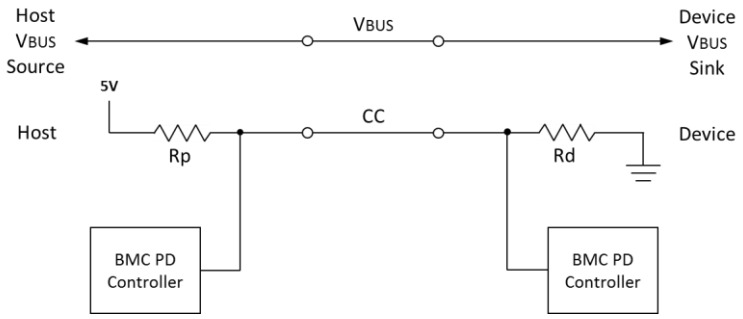
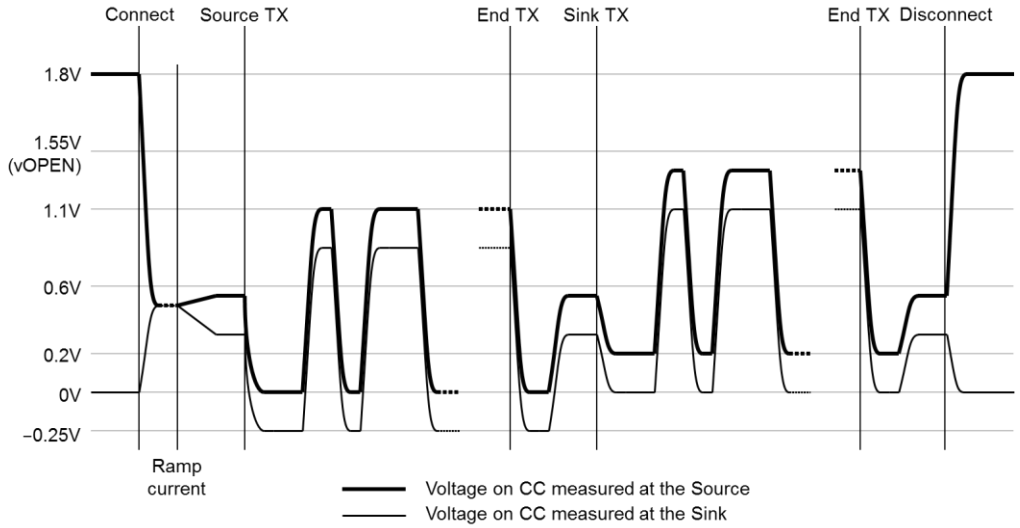


图 4-37 说明了从源和接收器的角度在 CC 上看到的 *USB PD* BMC 信号。信号中的中断旨在表示时间的流逝。

图 4-37 USB PD BMC 通过 CC 发送信号



当没有明确合同时，*USB PD* 来源基于其 PDP，能够提供：

- 5 V 时电流为 3 A 或更大时，应宣传 USB Type-C 电流为 3 A 级别 • 5 V 时电流为 1.5 A 或更大但小于 3 A 时，应宣传 USB Type-C 电流为 1.5

  低于 1.5A 的 • 5 V 级别应在默认 USB 电源级别上通告 USB Type-C 电流

在进入 Attached.SRC 状态的 tVBUSON 内。对于多端口共享容量充电器，能够提供 5 V 3A 或更大电流的 *USB PD* 源最初可以提供 1.5 A 级别的 USB Type-C 电流，然后在连接后增加电流（参见第 4.8.6.2 节）。在 USB 暂停期间，*USB PD* 源可以将其 Rp 值设置为默认值，以指示接收器应仅吸收第 4.6.1.1 节中定义的 USB 暂停电流。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

While a *USB PD* Explicit Contract is in place, a Source compliant with *USB PD* Revision 2 shall advertise a USB Type-C Current of either 1.5 A or 3.0 A. The *USB PD* Revision 2 Source upon entry into an Explicit Contract shall advertise an Rp value of 1.5 A or 3.0 A after it receives the GoodCRC in response to the first PS_RDY Message.

While a *USB PD* Explicit Contract is in place, a Source compliant with USB PD Revision 3 shall set the Rp value according to the collision avoidance scheme defined in Section 5.7 of the *USB PD* Revision 3 specification. The *USB PD* Revision 3 Source upon entry into an Explicit Contract shall advertise an Rp value consistent with the *USB PD* Revision 3 collision avoidance scheme.

Refer to Section 1.6 of the *USB Power Delivery* specification for a definition of an Explicit Contract.

4.6.2.5 Charge-Through VCONN-Powered USB Device (CTVPD) Current Limitations

Since Charge-Through VCONN-Powered USB Devices implement charging by passively connecting the Source's CC and VBUS to the Host, the VCONN-Powered USB Device is effectively increasing the impedance on VBUS, GND, and CC between the Power Source and the Host, resulting in impedances that can exceed the maximum allowed for cables. To avoid communication issues and false disconnects from the increased GND and VBUS drops, the following shall occur:

1. The Charge-Through VCONN-Powered USB Device shall report its worst-case GND and VBUS impedance (including the extra mated connector pair and FETs) in its *USB PD* Discover Identity Command response on SOP'.
2. The Host that supports Charge-Through VCONN-Powered USB Device shall use this information, along with inferred information about the cable, to limit its maximum current in the case where the Power Source advertises a current greater than what the Charge-Through VCONN-Powered USB Device would allow.

The Host has no way to query the cable, as its VCONN source is consumed by the VCONN-Powered USB Device. Instead, the Host may assume the cable is 5 A for the purposes of calculating the Charge-Through current limit only if it receives a *USB PD* SourceCapability PDO of greater than 3 A (even if the Host ultimately does not Request that PDO, or if the host requests a current of 3 A or less).

The Host shall further limit its maximum current beyond that advertised by the Power Source, based on the reported GND impedance and the inferred cable capability. GND impedance is reported in the VPD Discover Identity Command Response in 1-milliohm steps and is used in the following formulas:

- GND-limited current with a 3A cable inferred = 0.25 V / (0.25 V / 3 A + VPD_GND_DCR)
- GND-limited current with a 5A cable inferred = 0.25 V / (0.25 V / 5 A + VPD_GND_DCR)

Some examples are in Table 4-19.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

在实施 *USB PD* 显式契约期间，符合 *USB PD* 修订版 2 的源应公布 1.5 A 或 3.0 A 的 USB Type-C 电流。在签订显式契约后，*USB PD* 修订版 2 源应在收到对第一个 PS_RDY 消息的响应中的 GoodCRC 后，公布 1.5 A 或 3.0 A 的 Rp 值。

在 *USB PD* 显式合同生效期间，符合 USB PD 修订版 3 的源应根据 *USB PD* 修订版 3 规范第 5.7 节中定义的防碰撞方案设置 Rp 值。*USB PD* 修订版 3 源在签订显式合同后，应通告与 *USB PD* 修订版 3 防碰撞方案一致的 Rp 值。

有关显式契约的定义，请参阅 *USB Power Delivery* 规范的第 1.6 节。

4.6.2.5 通过 VCONN 供电的 USB 设备 (CTVPD) 充电的电流限制

由于通过 VCONN 充电的 USB 设备通过将电源的 CC 和 VBUS 被动连接到主机来实现充电，因此 VCONN 供电的 USB 设备实际上增加了电源和主机之间 VBUS、GND 和 CC 的阻抗，导致阻抗可能超过电缆允许的最大值。为了避免因 GND 和 V BUS 电压下降增加而导致通信问题和错误断开连接，应采取以下措施：

1. 通过 VCONN 充电的 USB 设备应报告其最坏情况的 GND 和 VBUS 阻抗（包括额外配对的连接器对和 FET）在 SOP ’ 上的 *USB PD* 发现身份命令响应中。2. 支持通过 VCONN 充电的 USB 设备的主机应使用此信息以及有关电缆的推断信息，在电源通告的电流大于通过 VCONN 充电的 USB 设备允许的电流的情况下限制其最大电流。

主机无法查询电缆，因为其 VCONN 源被 VCONN 供电的 USB 设备消耗。相反，只有当主机收到大于 3 A 的 *USB PD* SourceCapability PDO 时（即使主机最终不请求该 PDO，或者主机请求的电流为 3 A 或更低），主机才可以假设电缆为 5 A，以便计算 Charge-Through 电流限制。

根据报告的 GND 阻抗和推断的电缆能力，主机应进一步限制其最大电流，使其超出电源所宣传的最大电流。GND 阻抗在 VPD 发现身份命令响应中以 1 毫欧姆为步长报告，并用于以下公式：

- 带有 3A 电缆的 GND 限制电流推断 = 0.25 V / (0.25 V / 3 A + VPD_GND_DCR)
- 带有 5A 电缆的 GND 限制电流推断 = 0.25 V / (0.25 V / 5 A + VPD_GND_DCR)

表 4-19 中列举了一些示例。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 4-19 Precedence of power source usage

Reported GND Impedance	3A Cable Inferred[1]	5A Cable Inferred[2]
0.010 Ω	2.679 A	4.167 A
0.015 Ω	2.542 A	3.846 A
0.020 Ω	2.419 A	3.571 A
0.025 Ω	2.308 A	3.333 A
0.030 Ω	2.206 A	3.125 A
0.035 Ω	2.113 A	2.941 A
0.040 Ω	2.027 A	2.778 A

Notes:

1. As calculated by 0.25 V / (0.25 V / 3 A + VPD_GND_DCR).
2. As calculated by 0.25 V / (0.25 V / 5 A + VPD_GND_DCR).

In addition, the increased VBUS impedance could result in a greater than 1 V VBUS drop as measured at the input to the Host. Based on the VBUS impedance reported in the VPD Discover Identity Command Response in 2-milliohm steps and the inferred cable capability, the Host shall either lower its VBUS detach threshold or further limit its maximum current based on the following formulas:

- VBUS and GND-limited current with a 3A cable inferred = 0.75 V / (0.75 V / 3 A + VPD_VBUS_DCR + VPD_GND_DCR)
- VBUS and GND-limited current with a 5A cable inferred = 0.75 V / (0.75 V / 5 A + VPD_VBUS_DCR + VPD_GND_DCR)

Table 4-20 Example Charge-Through VPD Sink Maximum Currents based on VBUS Impedance and GND Impedance

Reported VBUS Impedance[4]	Reported GND Impedance[4]	3A Cable Inferred[1]	5A Cable Inferred[2]
0.020 Ω	0.010 Ω	2.679 A	4.167 A
0.030 Ω	0.015 Ω	2.542 A	3.846 A
0.040 Ω	0.020 Ω	2.419 A	3.571 A
0.050 Ω	0.025 Ω	2.308 A	3.333 A
0.060 Ω	0.030 Ω	2.206 A	3.125 A
0.070 Ω	0.035 Ω	2.113 A	2.941 A
0.080 Ω	0.040 Ω	2.027 A	2.778 A

Notes:

1. As calculated by 0.75 V / (0.75 V / 3 A + VPD_VBUS_DCR + VPD_GND_DCR).
2. As calculated by 0.75 V / (0.75 V / 5 A + VPD_VBUS_DCR + VPD_GND_DCR).
3. Table does not show all allowable combinations, only a subset provided for illustration.
4. The ratio of the reported VBUS impedance to the reported GND impedance is 2:1.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表4-19 电源使用优先顺序

Reported GND Impedance	3A Cable Inferred[1]	5A Cable Inferred[2]
0.010 Ω	2.679 A	4.167 A
0.015 Ω	2.542 A	3.846 A
0.020 Ω	2.419 A	3.571 A
0.025 Ω	2.308 A	3.333 A
0.030 Ω	2.206 A	3.125 A
0.035 Ω	2.113 A	2.941 A
0.040 Ω	2.027 A	2.778 A

注释：1. 根据 0.25 V / (0.25 V / 3 A + VPD_GND_DCR) 计算得出。2. 根据 0.25 V / (0.25 V / 5 A + VPD_GND_DCR) 计算得出。

此外，VBUS 阻抗增加可能会导致主机输入端测量到的 VBUS 电压下降超过 1 V。根据 VPD 发现身份命令响应中报告的 VBUS 阻抗（步长为 2 毫欧姆）和推断出的电缆能力，主机应根据以下公式降低其 VBUS 分离阈值或进一步限制其最大电流：

- VBUS 和 GND 限制电流，使用 3A 电缆推断 = 0.75 V / (0.75 V / 3 A + VPD_VBUS_DCR + VPD_GND_DCR) • VBUS 和 GND 限制电流，使用 5A 电缆推断 = 0.75 V / (0.75 V / 5 A + VPD_VBUS_DCR + VPD_GND_DCR)

表 4-20 充电直通 VPD 最大吸收电流示例
基于 VBUS 阻抗和 GND 阻抗

Reported VBUS Impedance[4]	Reported GND Impedance[4]	3A Cable Inferred[1]	5A Cable Inferred[2]
0.020 Ω	0.010 Ω	2.679 A	4.167 A
0.030 Ω	0.015 Ω	2.542 A	3.846 A
0.040 Ω	0.020 Ω	2.419 A	3.571 A
0.050 Ω	0.025 Ω	2.308 A	3.333 A
0.060 Ω	0.030 Ω	2.206 A	3.125 A
0.070 Ω	0.035 Ω	2.113 A	2.941 A
0.080 Ω	0.040 Ω	2.027 A	2.778 A

笔记：

1. 根据 0.75 V / (0.75 V / 3 A + VPD_VBUS_DCR + VPD_GND_DCR) 计算得出。2. 根据 0.75 V / (0.75 V / 5 A + VPD_VBUS_DCR + VPD_GND_DCR) 计算得出。3. 表格并未显示所有允许的组合，仅提供了用于说明的子集。4. 报告的 VBUS 阻抗与报告的 GND 阻抗之比为 2:1。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.7 USB Hubs

USB 2.0, *USB 3.2*, and *USB4* hubs are defined by the *USB 2.0*, *USB 3.2*, and *USB4* specifications, respectively. USB hubs implemented with one or more USB Type-C connectors shall comply with these specification as relevant to a USB Type-C implementation. All the downstream facing USB Type-C ports on a USB hub should support the same functionality or shall be clearly marked as to the functionality supported.

USB hubs shall have an upstream facing port (to connect to a host or hub higher in the USB tree) that may be a Sourcing Device (See Section 4.8.4). The hub shall clearly identify to the user its upstream facing port. This may be accomplished by physical isolation, labeling or a combination of both.

USB hub's downstream facing ports shall not have Dual-Role-Data (DRD) capabilities. However, these ports may have Dual-Role-Power (DRP) capabilities.

CC pins are used for port-to-port connections and shall be supported on all USB Type-C connections on the hub.

For *USB 2.0* and *USB 3.2* hubs, downstream-facing ports shall not implement or pass-through Alternate or Accessory Modes and SBU pins shall not be connected (zSBUTermination) on any USB hub port. For *USB4* hubs, see Section 5.2.3.2 regarding support for Alternate Modes.

The USB hub's DFPs shall support power source requirements for a Source. See Section 4.8.1.

Additional requirements for *USB4* hubs are in Chapter 5.

4.8 Power Sourcing and Charging

This section defines requirements and recommendations related to using USB Type-C ports for delivering power. Any USB Type-C port that offers more than Default Current and/or supports USB Power Delivery shall meet the requirements as if it is a charger.

The following lists the most applicable subsections by USB Type-C ports on:

- Host systems: 4.8.1 and 4.8.5. Note: 4.8.6 is not intended for host systems.
- Devices that can supply power: 4.8.4.
- Hubs:
  - Traditional hubs – Refer to USB 2.0/USB 3.2 base specifications and 4.8.1 as applicable if *USB BC 1.2* is supported.
  - Hubs that can supply power beyond the base specs – 4.8.1, 4.8.4, 4.8.5 and 4.8.6.
- Dedicated chargers:
  - Single-port chargers – 4.8.1.
  - Multi-port chargers – 4.8.1 and 4.8.6.

4.8.1 DFP as a Power Source

Sources (e.g. battery chargers, hub downstream ports and hosts) may all be used for battery charging. When a charger is implemented with a USB Type-C receptacle or a USB Type-C captive cable, it shall follow all the applicable requirements.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.7 USB 集线器

USB 2.0、*USB 3.2* 和 *USB4* 集线器分别由 *USB 2.0*、*USB 3.2* 和 *USB4* 规范定义。使用一个或多个 USB Type-C 连接器实现的 USB 集线器应遵守与 USB Type-C 实现相关的这些规范。USB 集线器上所有面向下游的 USB Type-C 端口都应支持相同的功能，或应明确标记所支持的功能。

USB 集线器应具有一个面向上游的端口（用于连接到 USB 树中较高的主机或集线器），该端口可以是源设备（请参阅第 4.8.4 节）。集线器应向用户清楚地标识其面向上游的端口。这可以通过物理隔离、标签或两者结合来实现。

USB 集线器的下游端口不得具有双重角色数据 (DRD) 功能。
但是，这些端口可能具有双角色电源 (DRP) 功能。

CC 引脚用于端口到端口的连接，并且应在集线器上的所有 USB Type-C 连接上受支持。

对于 *USB 2.0* 和 *USB 3.2* 集线器，面向下游的端口不得实现或传递备用模式或附件模式，并且不得在任何 USB 集线器端口上连接 SBU 引脚（zSBUTermination）。对于 *USB4* 集线器，请参阅第 5.2.3.2 节有关备用模式的支持。

USB 集线器的 DFP 应支持源的电源要求。请参阅第 4.8.1 节。

USB4 集线器的附加要求在第 5 章中。

4.8 电源和充电

本节定义了使用 USB Type-C 端口传输电源的相关要求和建议。任何提供超过默认电流和/或支持 USB 电源传输的 USB Type-C 端口都应满足充电器的要求。

以下列出了 USB Type-C 端口最适用的子部分：

- 主机系统：4.8.1 和 4.8.5。注意：4.8.6 不适用于主机系统。
- 可提供电源的设备：4.8.4。
- 集线器：
  - o 传统集线器 – 如果支持 *USB BC 1.2*，请参阅 USB 2.0/USB 3.2 基本规范和 4.8.1（如适用）。
  - o 可提供超出基本规范的电源的集线器 – 4.8.1、4.8.4、4.8.5 和 4.8.6。
- 专用充电器：
  - o 单端口充电器 – 4.8.1。
  - o 多端口充电器 – 4.8.1 和 4.8.6。

4.8.1 DFP 作为电源

电源（例如电池充电器、集线器下游端口和主机）均可用于电池充电。当充电器采用 USB Type-C 插座或 USB Type-C 固定电缆时，应遵循所有适用要求。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- A Source shall expose its power capabilities using the USB Type-C Current method and it may additionally support other USB-standard methods (*USB BC 1.2* or *USB-PD*).
- A Source advertising its current capability using *USB BC 1.2* shall meet the requirements in Section 4.6.2.2 regarding USB Type-C Current advertisement.
- A Source that has negotiated a *USB-PD* contract shall meet the requirements in Section 4.6.2.4 regarding USB Type-C Current advertisement.
- If a Source is capable of supplying a voltage greater than default VBUS, it shall fully conform to the *USB-PD* specification and shall negotiate its power contracts using only *USB-PD*.
- If a Source is capable of reversing source and sink power roles, it shall fully conform to the *USB-PD* specification and shall negotiate its power contracts using only *USB-PD*.
- If a Source is capable of supplying a current greater than 3.0 A, it shall use the *USB-PD* Discover Identity to determine the current carrying capacity of the cable.

4.8.1.1 USB-based Chargers with USB Type-C Receptacles

- A USB-based charger with a USB Type-C receptacle (Source) shall only apply power to VBUS when it detects a Sink is attached and shall remove power from VBUS when it detects the Sink is detached (vOPEN).
- A USB-based charger with a USB Type-C receptacle shall not advertise current exceeding 3.0 A except when it uses the *USB-PD* Discover Identity mechanism to determine the cable's actual current carrying capability and then it shall limit the advertised current accordingly.
- A USB-based charger with a USB Type-C receptacle (Source) which is not capable of data communication shall advertise USB Type-C Current of at least 1.5 A within tVBUSON of entering the Attached.SRC state and shall short D+ and D− together with a resistance less than 200 ohms. This will ensure backwards compatibility with legacy sinks which may use *USB BC 1.2* for charger detection.

4.8.1.2 USB-based Chargers with USB Type-C Captive Cables

- A USB-based charger with a USB Type-C captive cable that supports USB PD shall only apply power to VBUS when it detects a Sink is attached and shall remove power from VBUS when it detects the Sink is detached (vOPEN).
- A USB-based charger with a USB Type-C captive cable that does not support USB PD may supply VBUS at any time. It is recommended that such a charger only apply power to VBUS when it detects a Sink is present and remove power from VBUS when it detects the Sink is not present (vOPEN).
- A USB-based charger with a USB Type-C captive cable shall limit its current advertisement so as not to exceed the current capability of the cable (up to 5 A).
- A USB-based charger with a USB Type-C captive cable which is not capable of data communication shall advertise USB Type-C Current of at least 1.5 A. It is recommended that such a charger short D+ and D− together with a resistance less than 200 ohms.
- The voltage as measured at the plug of a USB-based charger with a USB Type-C captive cable may be up to $0.75 \times I / 3$ V ($0 < I \leq 3$ A), or $0.75 \times I / 5$ V ($0 < I \leq 5$ A) lower than the standard tolerance range for the chosen voltage, where I is the actual current being drawn.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• 源应使用 USB Type-C 电流方法公开其供电能力，并且还可以支持其他 USB 标准方法（*USB BC 1.2* 或 *USB- PD*）。• 使用 *USB BC 1.2* 宣传其电流能力的源应满足第 4.6.2.2 节中有关 USB Type-C 电流宣传的要求。• 已协商 *USB-PD* 合同的源应满足第 4.6.2.4 节中有关 USB Type-C 电流宣传的要求。• 如果源能够提供高于默认 VBUS 的电压，则它应完全符合 *USB-PD* 规范，并且应仅使用 *USB-PD* 协商其供电合同。• 如果源能够反转源和接收器电源角色，则它应完全符合

符合 *USB-PD* 规范，并应仅使用 *USB- PD* 来协商其电力合同。• 如果电源能够提供大于 3.0 A 的电流，则应使用 *USB- PD* 发现身份来确定电缆的载流能力。

4.8.1.1 带有 USB Type-C 插座的 USB 充电器

• 带有 USB Type-C 插座（电源）的 USB 充电器应仅在检测到接收器已连接时向 VBUS 供电，并在检测到接收器已连接时从 VBUS 切断电源。

检测到 Sink 已断开（vOPEN）。• 带有 USB Type-C 插座的 USB 充电器不得通告超过 3.0 A 的电流，除非它使用 *USB-PD* 发现身份机制确定电缆的实际载流能力，然后它应相应地限制通告的电流。• 带有 USB Type-C 插座（Source）且无法进行数据通信的 USB 充电器应在进入 Attached.SRC 状态后的 tVBUSON 内通告至少 1.5 A 的 USB Type-C 电流，并将 D+ 和 D− 与小于 200 欧姆的电阻短接。这将确保与可能使用 *USB BC 1.2* 进行充电器检测的传统 Sink 的向后兼容性。

4.8.1.2 带有 USB Type-C 固定线缆的 USB 充电器

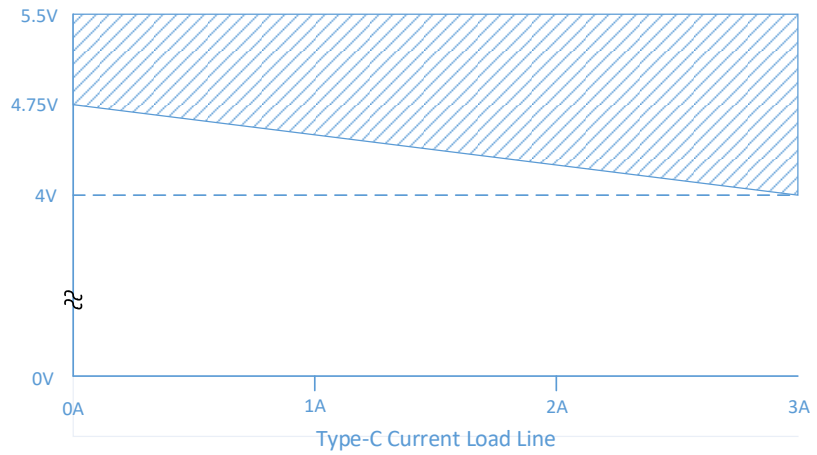
• 带有支持 USB PD 的 USB Type-C 固定电缆的 USB 充电器应仅在检测到 Sink 已连接时向 VBUS 供电，并在检测到 Sink 已断开时从 VBUS 切断电源 (vOPEN)。• 带有不支持 USB PD 的 USB Type-C 固定电缆的 USB 充电器可随时为 VBUS 供电。建议此类充电器仅在检测到 Sink 存在时向 VBUS 供电，并在检测到 Sink 断开时从 VBUS 切断电源。

检测到 Sink 不存在 (vOPEN)。• 带有 USB Type-C 固定电缆的 USB 充电器应限制其电流通告，以免超过电缆的电流能力（最高 5 A）。• 带有无法进行数据通信的 USB Type-C 固定电缆的 USB 充电器应通告至少 1.5 A 的 USB Type-C 电流。建议此类充电器将 D+ 和 D − 短接在一起，电阻小于 200 欧姆。 • 使用 USB Type-C 固定电缆在 USB 充电器插头处测量的电压可能比所选电压的标准公差范围低高达 0.75 × I / 3 V（0 < I ≤ 3 A）或 0.75 × I / 5 V（0 < I ≤ 5 A），其中 I 是实际消耗的电流。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

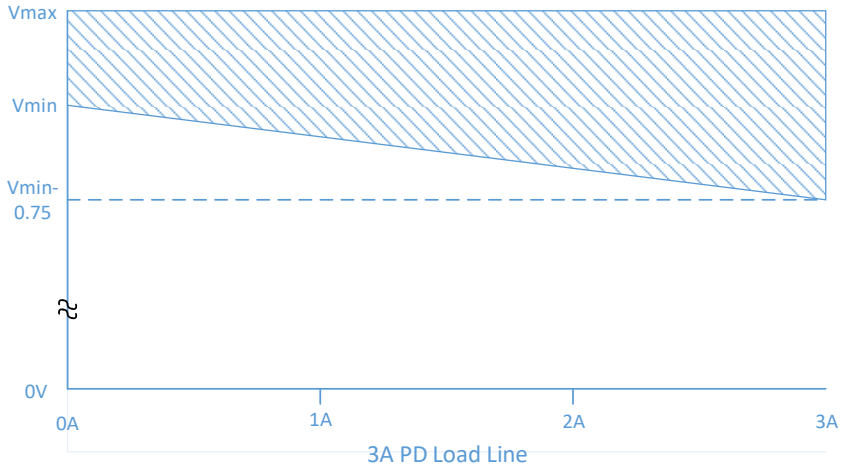
- A USB-based charger that advertises USB Type-C Current shall output a voltage in the range of 4.75 V – 5.5 V when no current is being drawn and between 4.0 V – 5.5 V at 3 A. The output voltage as a function of load up to the advertised USB Type-C Current (default, 1.5 A and 3 A) shall remain within the cross-hatched area shown in Figure 4-38.

Figure 4-38 USB Type-C Cable's Output as a Function of Load for Non-PD-based USB Type-C Charging



- A USB PD-based charger that has negotiated a voltage V at ≤ 3 A shall output a voltage in the range of Vmax (V + 5%) and Vmin (V – 5%) when no current is being drawn and Vmax and Vmin – 0.75 V at 3 A. Under all loads, the output voltage shall remain within the cross-hatched area shown in Figure 4-39.

Figure 4-39 0 – 3 A USB PD-based Charger USB Type-C Cable's Output as a Function of Load

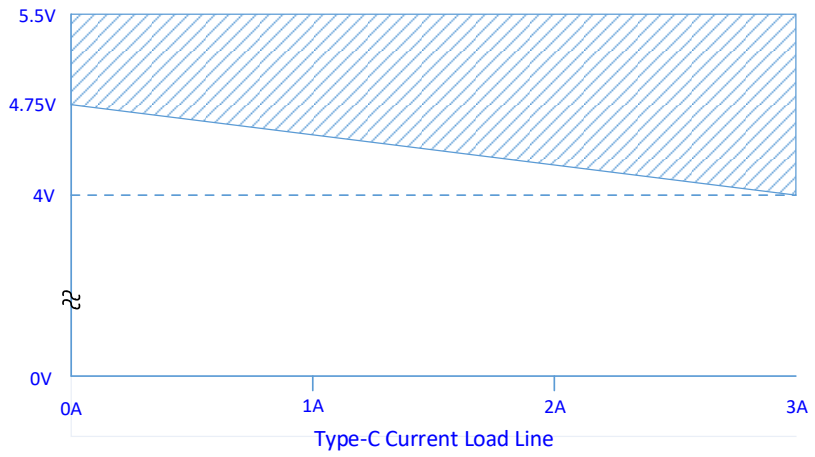


- A USB PD-based charger that has negotiated a voltage V at between 3 A and 5 A shall output a voltage in the range of Vmax (V + 5%) and Vmin (V – 5%) when no current is being drawn and Vmax and Vmin – 0.75 V at 5 A. Under

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

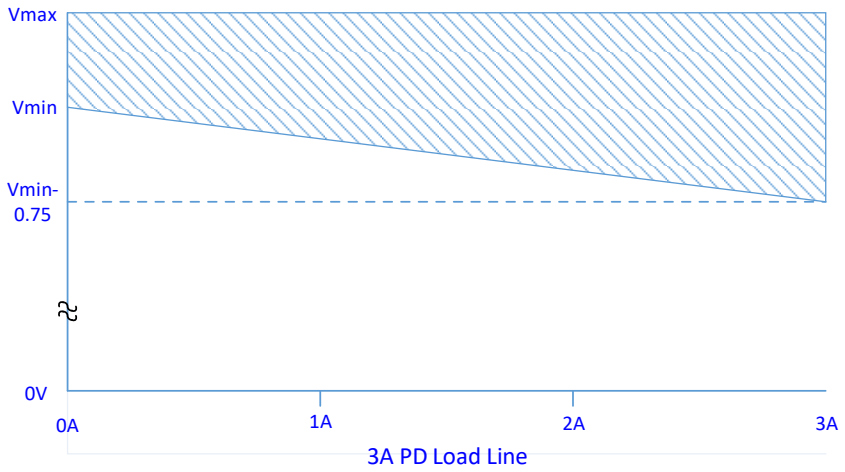
o 宣传 USB Type-C 电流的 USB 充电器在没有电流流过时应输出 4.75 V – 5.5 V 范围内的电压，在 3 A 时应输出 4.0 V – 5.5 V 之间的电压。输出电压作为负载的函数，最高可达宣传的 USB Type-C 电流（默认值为 1.5 A 和 3 A），应保持在图 4-38 所示的交叉影线区域内。

图 4-38 USB Type-C 线缆输出与非 PD USB Type-C 充电负载的关系



o 在 ≤ 3 A 时协商电压 V 的基于 USB PD 的充电器在没有电流流过时应输出在 Vmax（+ 5%）和 Vmin（V – 5%）范围内的电压，在 3 A 时应输出 Vmax 和 Vmin – 0.75 V 范围内的电压。在所有负载下，输出电压应保持在图 4-39 所示的交叉影线区域内。

图 4-39 0 – 3 A USB PD 充电器 USB Type-C 线缆的输出与负载的关系

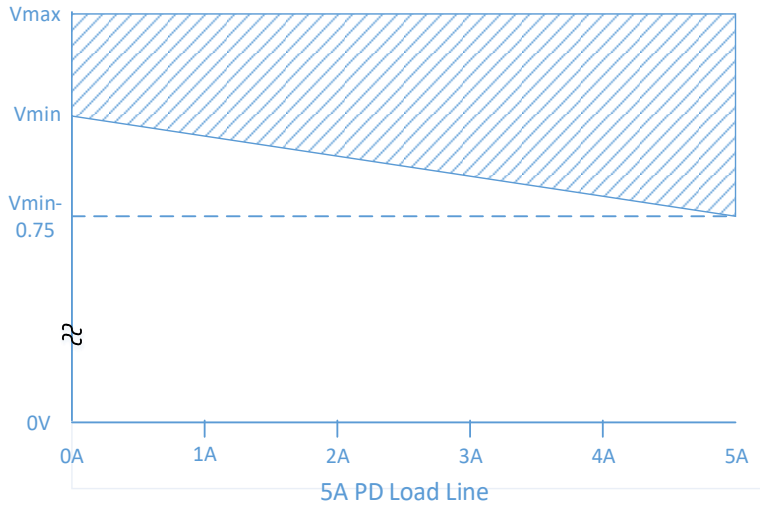


o 已协商电压 V 在 3 A 和 5 A 之间的 USB PD 充电器应在无电流流过时输出 Vmax（+ 5 %）和 Vmin（V – 5%）范围内的电压，在 5 A 时输出 Vmax 和 Vmin – 0.75 V 范围内的电压。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

all loads, the output voltage shall remain within the cross hatched area shown in Figure 4-40.

Figure 4-40 3 – 5 A USB PD-based Charger USB Type-C Cable's Output as a Function of Load



- Note: The maximum allowable cable IR drop for ground is 250 mV (see Section 4.4.1). This is to ensure the signal integrity of the CC wire when used for connection detection and *USB PD* BMC signaling.

4.8.2 Non-USB Charging Methods

A product (Source and/or Sink) with a USB Type-C connector shall only employ signaling methods defined in USB specifications to negotiate power over its USB Type-C connector(s).

4.8.3 Sinking Host

A Sinking Host is a special sub-class of a DRP that is capable of consuming power, but is not capable of acting as a USB device. For example a hub's DFP or a notebook's DFP that operates as a host but not as a device.

The Sinking Host shall follow the rules for a DRP (See Section 4.5.1.4 and Figure 4-15). The Sinking DFP shall support *USB PD* and shall support the DR_Swap command in order to get the Sink into the DFP data role.

4.8.4 Sourcing Device

A Sourcing Device is a special sub-class of a DRP that is capable of supplying power, but is not capable of acting as a USB host. For example a hub's UFP or a monitor's UFP that operates as a device but not as a host.

The Sourcing Device shall follow the rules for a DRP (See Section 4.5.1.4 and Figure 4-15). It shall also follow the requirements for the Source as Power Source (See Section 4.8.1). The Sourcing Device shall support *USB PD* and shall support the DR_Swap command in order to enable the Source to assume the UFP data role.

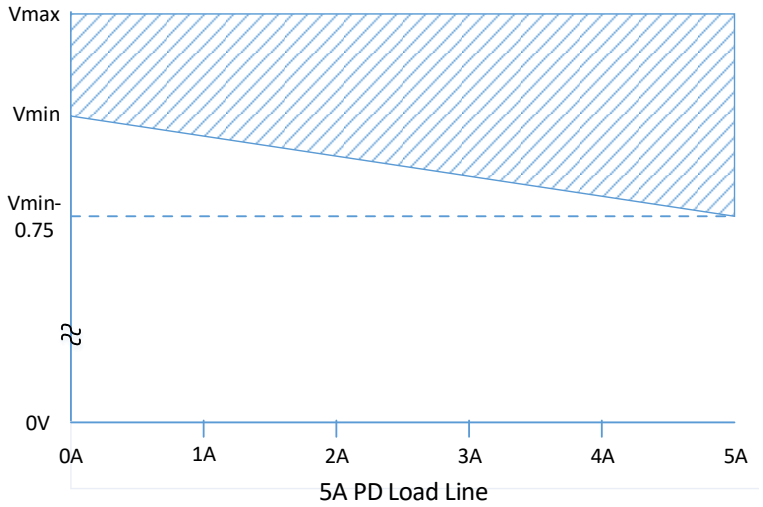
4.8.5 Charging a System with a Dead Battery

A system that supports being charged by USB whose battery is dead shall apply Rd to both CC1 and CC2 and follow all Sink rules. When it is connected to a Source, DRP or Sourcing

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

所有负载下，输出电压应保持在图 4-40 所示的交叉阴影区域内。

图 4-40 3 – 5 A USB PD 充电器 USB Type-C 线缆的输出与负载的关系



• 注意：接地的最大允许电缆 IR 压降为 250 mV（见第 4.4.1 节）。这是为了确保 CC 线用于连接检测和 *USB PD* BMC 信号传输时的信号完整性。

4.8.2 非 USB 充电方式

带有 USB Type-C 连接器的产品（源设备和/或接收器）应仅采用 USB 规范中定义的信号传输方法通过其 USB Type-C 连接器协商电力。

4.8.3 沉没宿主

耗电主机是 DRP 的一个特殊子类，能够消耗电力，但不能充当 USB 设备。例如，集线器的 DFP 或笔记本电脑的 DFP 可作为主机运行，但不能作为设备运行。

接收主机应遵循 DRP 规则（见第 4.5.1.4 节和图 4-15）。接收 DFP 应支持 *USB PD*，并应支持 DR_Swap 命令，以使接收端进入 DFP 数据角色。

4.8.4 采购设备

供电设备是 DRP 的一个特殊子类，能够供电，但不能充当 USB 主机。例如，集线器的 UFP 或显示器的 UFP 可作为设备运行，但不能作为主机运行。

源设备应遵循 DRP 规则（参见第 4.5.1.4 节和图 4-15）。它还应遵循源作为电源的要求（参见第 4.8.1 节）。源设备应支持 *USB PD* 并应支持 DR_Swap 命令，以使源能够承担 UFP 数据角色。

4.8.5 对电池电量耗尽的系统进行充电

支持通过 USB 充电且电池电量耗尽的系统应将 Rd 应用于 CC1 和 CC2，并遵循所有 Sink 规则。当它连接到 Source、DRP 或 Sourcing

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Device, the system will receive the default VBUS. It may use any allowed method to increase the amount of power it can use to charge its battery.

Circuitry to present Rd in a dead battery case only needs to guarantee the voltage on CC is pulled within the same range as the voltage clamp implementation of Rd in order for a Source to recognize the Sink and provide VBUS. For example, a 20% resistor of value Rd in series with a FET with VGTH(max) < VCLAMP(max) with the gate weakly pulled to CC would guarantee detection and be removable upon power up.

When the system with a dead battery has sufficient charge, it may use the *USB PD* DR_Swap message to become the DFP.

4.8.6 USB Type-C Multi-Port Chargers

A USB Type-C Multi-Port Charger is a product that exposes multiple USB Type-C Source ports for the purpose of charging multiple connected devices. A compliant USB Type-C charger may offer on each of its ports a mix of power options as defined in Section 4.6.

Multi-Port Chargers will generally fall into two categories as defined by the following.

1. Assured Capacity Chargers: a multi-port charger where the sum of the maximum capabilities of all of the exposed ports, as indicated to the user, is equal to the total power delivery capacity of the charger.
2. Shared Capacity Chargers: a multi-port charger where the sum of the maximum capabilities of all of the exposed ports, as indicated to the user, is less than the total power delivery capacity of the charger.

A Multi-Port Charger may offer in a single product separate visually identifiable groupings of charging ports. In this case, each group can independently offer either one of the two charging categories, either an Assured Capacity Charger or a Shared Capacity Charger.

This section defines the requirements and provides guidelines for the operation and behavior of a USB Type-C Multi-Port Charger.

4.8.6.1 General Requirements

Individual source ports shall always comply with power negotiation and rules set forth by the USB Type-C and USB Power Delivery specifications, adjusted as needed when available resources change as other ports take more or less power.

The minimum capability of all individual USB Type-C ports of a USB Type-C Multi-Port Charger shall be 5V @ 1.5 A independent of how many of the other ports are in use.

When a USB Type-C Charger includes charging ports that are based on USB Standard-A receptacles, the following requirements shall be met.

- The USB Standard-A ports shall be implemented as an independent group, i.e. USB Standard-A ports shall not be included in a group of USB Type-C ports behaving as a Shared Capacity Charger. Any load change on a USB Type-A port shall not result in a voltage change on any of the USB Type-C ports and vice-versa.
- The minimum capability of each USB Standard-A port shall be 5V @ 500 mA independent of how many of the other ports are in use.

4.8.6.2 Multi-Port Charger Behaviors

Each Source port of Assured Capacity Chargers shall, by design, behave independently and be unaffected by the status and loading of the other ports. An exception to this behavior is allowed if the charger has to take any action necessary to meet an overall product operational safety requirement due to unexpected behavior on any port.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

设备，系统将接收默认 VBUS。它可以使用任何允许的方法来增加其可用于给电池充电的电量。

在电池没电的情况下显示 Rd 的电路只需保证 CC 上的电压与 Rd 的电压钳位实现处于同一范围内，以便源端识别接收器并提供 VBUS。例如，将一个值为 Rd 的 20% 电阻与一个 VGTH(max) < VCLAMP(max) 的 FET 串联，并将栅极弱拉至 CC，即可保证检测，并在通电时可移除。

当电池没电的系统有足够的电量时，它可以使用 *USB PD* DR_Swap 消息成为 DFP。

4.8.6 USB Type-C 多端口充电器

USB Type-C 多端口充电器是一种提供多个 USB Type-C 源端口的产品，用于为多个连接设备充电。符合要求的 USB Type-C 充电器可在其每个端口上提供第 4.6 节中定义的混合电源选项。

多端口充电器通常分为以下两类。

1. 保证容量充电器：多端口充电器，向用户指示的所有暴露端口的最大容量总和等于充电器的总功率输送容量。 2. 共享容量充电器：多端口充电器，向用户指示的所有暴露端口的最大容量总和小于充电器的总功率输送容量。

多端口充电器可以在单个产品中提供单独的可视觉识别的充电端口组。在这种情况下，每个组可以独立提供两种充电类别中的一种，即保证容量充电器或共享容量充电器。

本节定义了 USB Type-C 多端口充电器的操作和行为的要求并提供了指南。

4.8.6.1 一般要求

各个源端口应始终符合 USB Type-C 和 USB 电力传输规范所规定的电源协商和规则，并根据其他端口消耗更多或更少电力而导致可用资源发生变化的情况进行必要调整。

USB Type-C 多端口充电器的所有单个 USB Type-C 端口的最低容量应为 5V @ 1.5 A，与正在使用的其他端口数量无关。

当 USB Type-C 充电器包含基于 USB 标准 -A 插座的充电端口时，应满足以下要求。

- USB 标准 A 端口应作为独立组实施，即 USB 标准 A 端口不应包含在作为共享容量充电器的 USB Type-C 端口组中。USB Type-A 端口上的任何负载变化均不应导致任何 USB Type-C 端口上的电压变化，反之亦然。
- 每个 USB 标准 A 端口的最小容量应为 5V @ 500 mA，与正在使用的其他端口数量无关。

4.8.6.2 多端口充电器行为

保证容量充电器的每个源端口在设计上应独立运行，不受其他端口状态和负载的影响。如果充电器因任何端口出现意外行为而必须采取任何必要措施来满足整体产品操作安全要求，则允许例外。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

For Shared Capacity Chargers, the following behavioral rules shall apply:

- Each of the exposed Source Ports shall have the same power capabilities. Each port of the charger shall be capable of the same maximum capability, minimum capability, and be able to draw from the shared power equally.
- All exposed USB PD unattached Source Ports shall have the same power capabilities.
    - Ports shall have the ability to supply the available shared capacity power up to the port's maximum power.
        - A shared capacity charger's ports may offer less than this value, but shall increase the offer up to the required value when the Sink sets the Capabilities Mismatch bit in its response. This may be done in multiple steps, but all ports in the Shared Capacity Group shall reach the maximum power within three seconds.
    - Whenever a power contract is made or changed on any port, the available shared capacity shall be re-computed and the source shall send updated Source Capability messages as needed.
        - As ports of a Shared Capacity Group are connected, each remaining unattached Source Port shall be capable of advertising the lower of the Maximum Capability of the port OR the Total Shared Capacity – the contracted power for the attached ports – (the number of unattached ports – 1) * the minimum port power.
    - Ports shall offer at least 7.5 W.
    - When calculating the available shared capacity for ports in a Fixed Supply power contract, the shared capacity charger shall use the Voltage times the Maximum Current in the PDO as the power the port is supplying regardless of the actual Operating Current requested in the RDO request.
    - When calculating the available shared capacity for ports in a PPS power contract, the shared capacity charger shall use the Maximum Voltage times the Maximum Current in the APDO as the power the port is supplying regardless of the actual voltage and current in the RDO request.
    - Ports when not in a PD contract shall follow the rules for a shared USB Type-C Current source unless there is sufficient remaining power for each port to advertise 15 W.
- All exposed USB Type-C Current ports shall have the ability to offer the same power capabilities.
    - All ports shall initially offer 1.5 A.
    - Ports shall increase to 3 A after attach if they have sufficient available shared capacity within one second.
    - Ports shall never offer less than 1.5 A – e.g. shall not offer Default.

As Source ports are connected and begin providing power, the remaining Source ports will each have the same power capabilities. The maximum capability may be less than the previously connected ports due to less unused capacity of the total power delivery capacity of the charger. For example, if the total power delivery capacity of a USB Type-C two-port charger is 60 W with a port PDP of 35 W and the first connected Source port has established a 35 W power contract with its connected Sink, then the second Source port will only be able to offer a PDP of 25 W.

Each port should start by offering the minimum capability for the port and increase the offering to the Sink upon a connection. For example, if the maximum capability of a USB Type-C only Source port is 3 A, then all of the exposed Source ports will be able to offer 3

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

对于共享容量充电器，应适用以下行为规则：

• 每个暴露的源端口应具有相同的功率能力。充电器的每个端口应具有相同的最大容量、最小容量、

并能够平等地从共享电源中获取电力。• 所有暴露的 USB PD 未连接源端口应具有相同的供电能力。o 端口应能够提供可用的共享容量电力，直至达到端口的最大功率。 ▪ 共享容量充电器端口可能提供低于此值的电力，但当接收器在其响应中设置 “ 能力不匹配 ” 位时，应将电力增加到所需值。这可以分多个步骤完成，但共享容量组中的所有端口都应在三秒内达到最大功率。o 每当在任何端口上签订或更改电力合同时，应重新计算可用的共享容量，并且源应根据需要发送更新的源能力消息。 ▪ 当共享容量组的端口连接时，每个剩余的未连接的源端口应能够通告端口的最大能力或总共享容量 - 连接端口的合同功率 -（未连接端口的数量 - 1）* 最小端口功率中的较低者。 o 端口应至少提供 7.5 W。o 在计算固定供电合同中端口的可用共享容量时，共享容量充电器应使用 PDO 中的电压乘以最大电流作为端口提供的功率，而不管 RDO 请求中请求的实际工作电流是多少。o 在计算 PPS 供电合同中端口的可用共享容量时，共享容量充电器应使用 APDO 中的最大电压乘以最大电流作为端口提供的功率，而不管 RDO 请求中的实际电压和电流是多少。o 不属于 PD 合同的端口应遵循共享 USB Type - C 电流源的规则，除非每个端口的剩余电量足以达到 15 W。

• 所有暴露的 USB Type-C 电流端口都应能够提供相同的电源功能。

o 所有端口最初应提供 1.5 A。 o 如果端口在一秒钟内具有足够的可用共享容量，则连接后应增加到 3 A。 o 端口绝不能提供低于 1.5 A 的电流 - 例如，不得提供默认值。

当源端口连接并开始供电时，其余源端口将各自具有相同的供电能力。由于充电器总供电能力中未使用的容量较少，最大能力可能低于之前连接的端口。例如，如果 USB Type - C 双端口充电器的总供电能力为 60 W，端口 PDP 为 35 W，并且第一个连接的源端口与其连接的接收器建立了 35 W 的供电协议，则第二个源端口只能提供 25 W 的 PDP。

每个端口应首先提供端口的最低容量，然后在连接时增加对接收器的容量。例如，如果 USB Type-C 专用源端口的最大容量为 3 A，则所有暴露的源端口都将能够提供 3

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A. Each port should start by offering less than the max (such as 1.5 A) and then increase the offering to 3 A after an attach. This would happen for each port as it is connected until the unused shared capacity is exhausted, at which point no other ports would increase to 3 A offering. A sink, in this example, would see a starting advertisement of USB Type-C Current @ 1.5 A at attach and would then see the USB Type-C Current advertisement increase to 3 A. As another example, if the maximum capability of a USB Type-C Source port is to offer *USB PD* with a PDP of 35 W, then all of the exposed Source ports would also support *USB PD* 35 W. Each port would start by offering something less on initial connection, like 15 W, and then increase the offering with new Source Capabilities when it determines the Sink would like more power. If the Sink is not offered the power it requires, it will send a request with the Capability Mismatch bit set to indicate to the source it wants more power. This will happen for each port as it is connected until the unused shared capacity is exhausted, at which point no other ports would increase the power offering.

When establishing the remaining available capacity, a charger that supports policy-based power rebalancing may include the power that can be reclaimed from ports already in use:

1. by adjusting advertised source capabilities equivalent with a reduced PDP to one or more ports that are already in use; or
2. by issuing a *USB PD* GotoMin command to one or more ports already in use.

Policy-based power rebalancing should consider providing good user experience and preserving nominal USB functionality on impacted devices. Fixed rebalancing algorithms that do not factor in overall USB system policy may not be appropriate for power rebalancing implementations.

4.8.6.3 Multi-Port Charger Port Labeling

Multi-port chargers shall have OEM-designed port labeling consistent with the following rules.

- For Assured Capacity Chargers, each exposed Source port shall be labeled to indicate the PDP of the port. In this case, the user will be able to expect that each of the labeled ports will be able to meet power contracts consistent with the labeling independent of how many of the Source ports are in use.
- For Shared Capacity Chargers, each Source port shall be labeled to indicate the same PDP. Additionally, the charger shall have a label that, with a minimum of equal visual prominence, indicates the total power delivery capacity being shared across all of the ports identified as a group.

A Multi-Port Charger that offers in a single product separate groupings of charging ports, each grouping shall be clearly identified as a separate grouping and each grouping shall be individually labeled consistent with that group's behavior model, either as an Assured Capacity Charger or a Shared Capacity Charger.

Refer to the USB Implementers Forum (USB-IF) for USB Type-C Chargers certification along with further labeling guidelines.

4.8.6.4 Multi-Port Charger that include USB Data Hub Functionality

Multi-Port chargers that also incorporate USB data hub capabilities shall meet the same requirements as standalone chargers. These charging-capable hubs shall be self-powered and shall fully operate as a charger independent of the state of the USB data bus connections.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A. 每个端口应从提供小于最大值（例如 1.5 A）的电流开始，然后在连接后将电流增加到 3 A。每个端口在连接时都会发生这种情况，直到未使用的共享容量耗尽，此时没有其他端口会将电流增加到 3 A。在此示例中，接收器将在连接时看到 USB Type-C 电流 @ 1.5 A 的起始广告，然后会看到 USB Type-C 电流广告增加到 3 A。再举一个例子，如果 USB Type-C 源端口的最大能力是提供 PDP 为 35 W 的 *USB PD*，那么所有暴露的源端口也将支持 *USB PD* 35 W。每个端口在初始连接时都会从提供较小的功率开始，例如 15 W，然后在确定接收器需要更多功率时通过新的源功能增加功率。如果接收器没有获得所需的功率，它将发送一个设置了能力不匹配位的请求，以向源指示它需要更多功率。每个端口在连接时都会发生这种情况，直到未使用的共享容量耗尽，此时没有其他端口会增加电力供应。

在确定剩余可用容量时，支持基于策略的功率重新平衡的充电器可能包括可从已在使用的端口回收的功率：

1. 通过调整已在使用的一个或多个端口的通告源功能，使其与降低的 PDP 等效；或者 2. 向一个或多个已在使用的端口发出 *USB PD* GotoMin 命令。

基于策略的电源再平衡应考虑提供良好的用户体验，并保留受影响设备上的正常 USB 功能。不考虑整体 USB 系统策略的固定再平衡算法可能不适合电源再平衡实施。

4.8.6.3 多端口充电器端口标签

多端口充电器应具有符合以下规则的 OEM 设计的端口标签。

• 对于保证容量充电器，每个暴露的源端口都应贴上标签以指示端口的 PDP。在这种情况下，用户可以预期每个带标签的端口都能够满足与标签一致的功率合同，而不管有多少个源端口在使用。• 对于共享容量充电器，每个源端口都应贴上标签以指示相同的 PDP。此外，充电器应有一个标签，该标签至少应具有同等的视觉突出度，指示被标识为一个组的所有端口共享的总功率输送容量。

多端口充电器在单一产品中提供单独的充电端口分组，每个分组应明确标识为单独的分组，并且每个分组应根据该组的行为模型单独标记，作为保证容量充电器或共享容量充电器。

请参阅 USB 实施者论坛 (USB-IF) 了解 USB Type-C 充电器认证以及进一步的标签指南。

4.8.6.4 包含 USB 数据中心功能的多端口充电器

集成 USB 数据集线器功能的多端口充电器应满足与独立充电器相同的要求。这些具有充电功能的集线器应自供电，并且应完全作为充电器运行，与 USB 数据总线连接的状态无关。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

For hub-based Multi-Port Chargers that offer power to the upstream-facing port (to the host), this port may either behave as an Assured Capacity Charging port (e.g. be a dedicated charging port) or as a Shared Capacity Charging port (e.g. sharing capacity with downstream-facing ports). In either case, it should be clearly labeled consistent with its designed behavior, including identifying it as part of a group if it is sharing capacity with other ports.

When the upstream-facing port is sharing capacity with the downstream-facing ports, the PDP of the upstream-facing port can differ from the downstream-facing ports.

4.9 Electronically Marked Cables

All USB Full-Featured Type-C cables shall be electronically marked. USB 2.0 Type-C cables may be electronically marked. An eMarker is element in an Electronically Marked Cable that returns information about the cable in response to a *USB PD* Discover Identity command.

Electronically marked cables shall support *USB Power Delivery* Structured VDM Discover Identity command directed to SOP' (the eMarker). This provides a method to determine the characteristics of the cable, e.g. its current carrying capability, its performance, vendor identification, etc. This may be referred to as the USB Type-C Cable ID function.

Prior to an explicit *USB PD* contract, a Sourcing Device is allowed to use SOP' to discover the cable's identity. After an explicit *USB PD* contract has been negotiated, only the Source shall communicate with SOP' and SOP" (see Section 6.2.1).

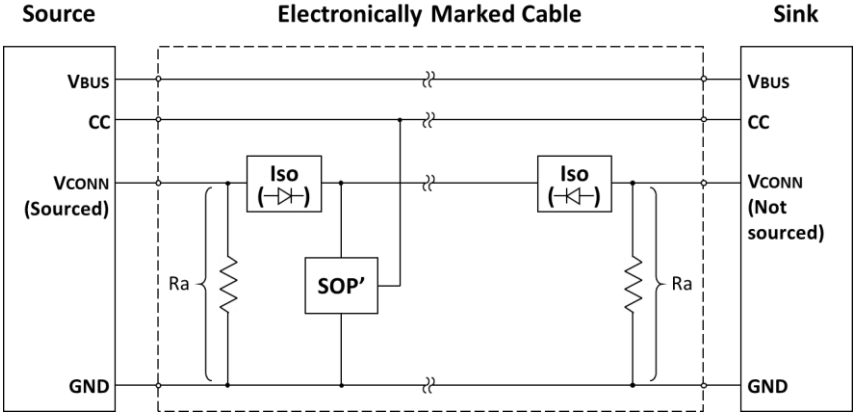
Passive cables that include an eMarker shall follow the Cable State Machine defined in Section 4.5.2.4 and Figure 4-20.

Electronically marked cables are generally powered from VCONN, although VBUS or another source may be used. Cables that include an eMarker shall meet the maximum power defined in Table 4-6.

Refer to Table 4-5 for the requirements of a Source to supply VCONN. When VCONN is not present, a powered cable shall not interfere with normal CC operation including Sink detection, current advertisement and *USB PD* operation.

Figure 4-41 illustrates a typical electronically marked cable. The isolation elements (Iso) shall prevent VCONN from traversing end-to-end through the cable. Ra is required in the cable to allow the Source to determine that VCONN is needed.

Figure 4-41 Electronically Marked Cable with VCONN connected through the cable



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

对于为上游端口（主机）提供电源的基于集线器的多端口充电器，此端口可以用作保证容量充电端口（例如专用充电端口）或共享容量充电端口（例如与下游端口共享容量）。无论哪种情况，都应根据其设计行为明确标记，包括将其标识为某个组的一部分（如果它与其他端口共享容量）。

当上游端口与下游端口共享容量时，上游端口的 PDP 可以与下游端口不同。

4.9 电子标记电缆

所有 USB 全功能 Type-C 电缆都应进行电子标记。USB 2.0 Type-C 电缆可以进行电子标记。eMarker 是电子标记电缆中的元素，它响应 *USB PD* Discover Identity 命令返回有关电缆的信息。

电子标记电缆应支持指向 SOP（eMarker）的 *USB Power Delivery* Structured VDM Discover Identity 命令。这提供了一种确定电缆特性的方法，例如其载流能力、性能、供应商标识等。这可以称为 USB Type-C 电缆 ID 功能。

在明确的 *USB PD* 合同之前，采购设备可以使用 SOP ’ 来发现电缆的身份。在明确的*USB PD*合同谈判完成后，只有源方可以通过 “ SOP ” 和 “ SOP ” 进行沟通（见第6.2.1节）。

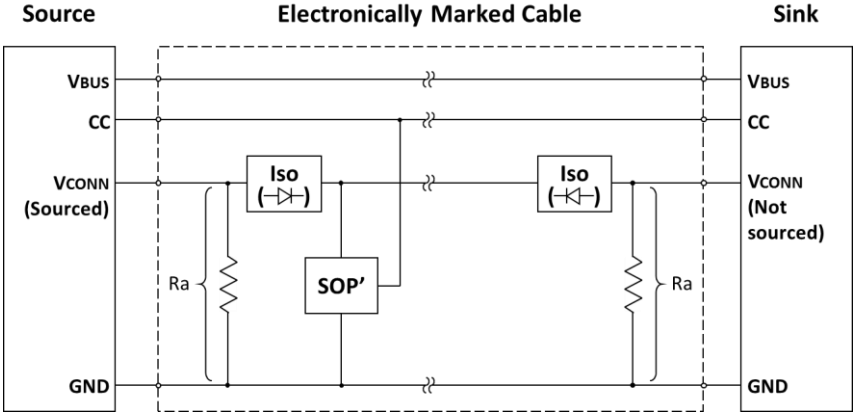
包含 eMarker 的无源电缆应遵循第 4.5.2.4 节和图 4-20 中定义的电缆状态机。

电子标记电缆通常由 VCONN 供电，但也可以使用 VBUS 或其他电源。包含电子标记的电缆应满足表 4-6 中定义的最大功率。

有关为 VCONN 供电的源的要求，请参阅表 4-5。当 VCONN 不存在时，供电电缆不得干扰正常的 CC 操作，包括 Sink 检测、电流通告和 *USB PD* 操作。

图 4-41 显示了典型的电子标记电缆。隔离元件 (Iso) 应防止 VCONN 穿过电缆的端到端。电缆中需要 Ra，以便源端确定需要 VCONN。

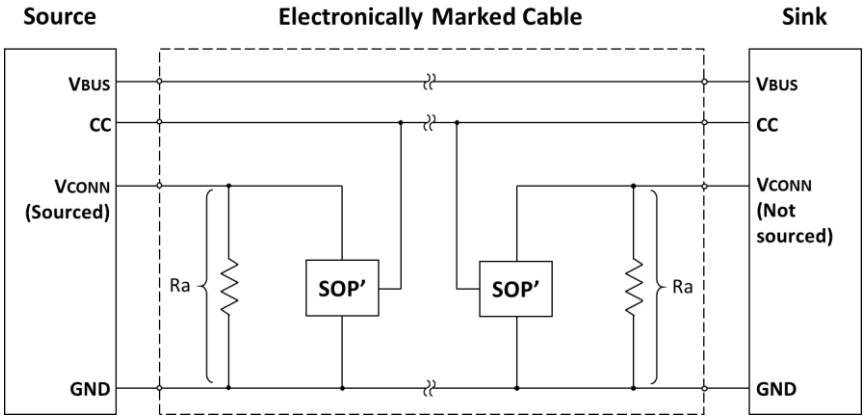
图 4-41 电气 带有 VCONN 标记的电缆通过 电缆



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-42 illustrates an electronically marked cable where the VCONN wire does not extend through the cable, therefore an SOP' (eMarker) element is required at each end of the cable. In this case, no isolation elements are needed.

Figure 4-42 Electronically Marked Cable with SOP' at both ends



For cables that only respond to SOP', the location of the responder is not relevant.

4.9.1 Parameter Values

Table 4-21 provides the power on timing requirements for the eMarker SOP' and SOP" to be ready to communicate.

Table 4-21 SOP' and SOP" Timing

	Maximum	Description
tVCONNStable	50 ms	The time between the application of VCONN until SOP' and SOP" shall be ready for communication.

4.9.2 Active Cables

An active cable is an electronically marked cable that incorporates data bus signal conditioning circuits, for example to allow for implementing longer cables. Active cables with data bus signal conditioning in both plugs shall implement SOP' and may implement SOP". Active cables shall meet the power requirements defined in Table 4-6.

Active cables may support either one TX/RX pair or two TX/RX pairs. The eMarker in the cable shall identify the number of TX/RX lanes supported. Active cables may or may not require configuration management. Active cable configuration management is defined in Section 5.5.4.

4.10 VCONN-Powered Accessories (VPAs) and VCONN-Powered USB Devices (VPDs)

VCONN-Powered Accessories and VCONN-Powered USB Devices are both direct-attach Sinks that can operate with just VCONN.

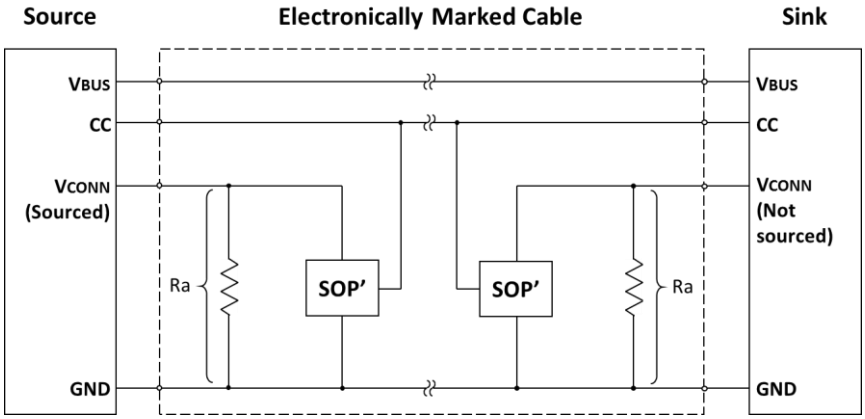
Both expose a maximum impedance to ground of Ra on the VCONN pin and Rd on the CC pin.

The removal of VCONN when VBUS is not present shall be treated as a detach event.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-42 显示了电子标记电缆，其中 VCONN 线未穿过电缆，因此电缆的每一端都需要一个 SOP ’ (eMarker) 元件。在这种情况下，不需要隔离元件。

图 4-42 两端带有 SOP ’ 的电子标记电缆



对于仅响应 SOP ’ 的电缆，响应器的位置并不重要。

4.9.1 参数值

表 4-21 提供了 eMarker SOP ’ 和 SOP ” 准备进行通信的开机时序要求。

表 4-21 SOP ’ 和 SOP ” 时序

	Maximum	Description
tVCONNStable	50 ms	The time between the application of VCONN until SOP' and SOP" shall be ready for communication.

4.9.2 有源电缆

有源电缆是一种电子标记电缆，它包含数据总线信号调节电路，例如，允许实现更长的电缆。两个插头中均带有数据总线信号调节的有源电缆应实施 SOP ’，并可实施 SOP ”。有源电缆应满足表 4-6 中定义的功率要求。

有源电缆可以支持一个 TX/RX 对或两个 TX/RX 对。电缆中的 eMarker 应标识支持的 TX/RX 通道数。有源电缆可能需要或不需要配置管理。有源电缆配置管理在第 5.5.4 节中定义。

4.10 VCONN 供电配件 (VPA) 和 VCONN 供电 USB 设备 (VPD)

VCONN 供电配件和 VCONN 供电 USB 设备都是仅使用 VCONN 即可运行的直连接收器。

两者的最大接地阻抗均为 VCONN 引脚上的 Ra 和 CC 引脚上的 Rd。

当 VBUS 不存在时，VCONN 的移除应被视为分离事件。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.10.1 VCONN-Powered Accessories (VPAs)

A VCONN-Powered Accessory implements an Alternate Mode (See Appendix E).

VCONN-Powered Accessories shall comply with Table 4-7.

When operating in the Sink role and when VBUS is not present, VCONN-Powered Accessories shall treat the application of VCONN as an attach signal, and shall respond to *USB Power Delivery* messages.

When powered by only VCONN, a VCONN-Powered Accessory shall negotiate an Alternate Mode. If it fails to negotiate an Alternate Mode within tAMETimeout, its port partner removes VCONN.

When VBUS is supplied, a VCONN-Powered Accessory is subject to all of the requirements for Alternate Modes, including presenting a *USB Billboard Device Class* interface if negotiation for an Alternate Mode fails.

Should a VCONN-Powered Accessory wish to provide charge-through functionality, it must do so by negotiating voltage and current independently on both the Host and charge-through ports, and possibly re-regulating the voltage from the Source before passing it through to the Sink. The Sink is able to take the full current that is advertised to it by the VCONN-Powered Accessory.

4.10.2 VCONN-Powered USB Devices (VPDs)

A VCONN-Powered USB Device shall implement a USB UFP endpoint.

VCONN-Powered USB Devices shall comply with Table 4-8.

When VBUS is not present, VCONN-Powered USB Devices shall treat the application of VCONN as an attach signal.

A VCONN-Powered USB Device shall respond to *USB PD* messaging on SOP', and shall not respond to other USB PD messaging. A VCONN-Powered USB Device shall respond to USB PD Hard Reset and Cable Reset signaling.

A Charge-Through VCONN -Powered USB Device shall discard all *USB PD* messages while a connection is enabled between the host port CC and Charge-Through port CC.

When VBUS is supplied by the Host, the VCONN-Powered USB Device shall behave like a normal UFP Sink, but still only respond to *USB PD* messaging on SOP'. If VBUS is subsequently removed while VCONN remains applied, the VCONN-Powered USB Device shall remain connected, and use VCONN as the sole detach signal.

Since VCONN-Powered USB Devices do not respond to *USB PD* on SOP, they cannot enter Alternate Modes.

A VCONN -Powered USB Device may provide Charge-Through functionality via VPD Charge-Through. VCONN-Powered USB Devices shall not provide any data pass-through to the Charge-Through port other than the CC wire.

Since the power and CC negotiation is passed through directly, the Sink shall limit its maximum current based on the additional impedance introduced by the VCONN-Powered USB Device.

Additionally, since power can only flow from the Charge-Through port to the Host, VCONN must be provided by the host, and there is no data connection beyond the CC wire passed

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.10.1 VCONN 供电配件 (VPA)

VCONN 供电配件实现了替代模式（参见附录 E）。

VCONN 供电配件应符合表 4-7 的规定。

当以 Sink 角色操作且 VBUS 不存在时，VCONN 供电配件应将 VCONN 的应用视为连接信号，并应响应 *USB Power Delivery* 消息。

当仅由 VCONN 供电时，VCONN 供电配件应协商备用模式。如果它在 tAMETimeout 内无法协商备用模式，则其端口伙伴将移除 VCONN。

当提供 VBUS 时，VCONN 供电配件需要满足备用模式的所有要求，包括在备用模式协商失败时提供 *USB Billboard Device Class* 接口。

如果 VCONN 供电配件希望提供直通充电功能，则必须通过在主机和直通充电端口上独立协商电压和电流来实现，并且可能在将电压传递到接收器之前重新调节来自源的电压。接收器能够接收 VCONN 供电配件向其通告的全部电流。

4.10.2 VCONN 供电 USB 设备 (VPD)

音频控制器 Powered USB 设备应实现 USB UFP 端 观点。

VCONN 供电的 USB 设备应符合表 4-8 的规定。

当 VBUS 不存在时，VCONN 供电的 USB 设备应将 VCONN 的应用视为连接信号。

VCONN 供电的 USB 设备应响应 SOP ’ 上的 *USB PD* 消息，并且不应响应其他 USB PD 消息。VCONN 供电的 USB 设备应响应 USB PD 硬重置和电缆重置信号。

当主机端口 CC 与充电端口 CC 之间建立连接时，通过 VCONN 充电供电的 USB 设备应丢弃所有 *USB PD* 消息。

当 VBUS 由主机供电时，VCONN 供电的 USB 设备应像普通的 UFP 接收器一样运行，但仍仅响应 SOP ’ 上的 *USB PD* 消息。如果随后在 VCONN 保持应用的情况下移除 VBUS，VCONN 供电的 USB 设备应保持连接，并使用 VCONN 作为唯一的断开信号。

由于 VCONN 供电的 USB 设备不响应 SOP 上的 *USB PD*，因此它们无法进入备用模式。

VCONN 供电的 USB 设备可通过 VPD Charge-Through 提供 Charge-Through 功能。VCONN 供电的 USB 设备不得向 Charge-Through 端口提供除 CC 线以外的任何数据直通。

由于电源和 CC 协商是直接进行的，因此 Sink 应根据 VCONN 供电的 USB 设备引入的额外阻抗来限制其最大电流。

此外，由于电源只能从 Charge-Through 端口流向主机，因此 VCONN 必须由主机提供，并且除了通过的 CC 线之外没有数据连接

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

through to the connected source, there are limitations on what the Host can advertise and support via *USB PD*:

- The Host shall not negotiate or accept a PR_Swap or VCONN_Swap
- The Host shall not enable FR_Swap
- The Host may only negotiate a DR_Swap when using *USB PD* Revision 2.0, and only for the purpose of switching which side is the PD bus master. The Host will always remain a DFP for USB data.
- The Host shall not advertise dual-role data or dual-role power in its SourceCapability or SinkCapability messages – Host changes its advertised capabilities to UFP role/sink only role.
- The Host shall not negotiate any Alternate Modes that change the function of pins on the connector.
- The Host shall represent itself to the Charge-Through Source using *USB PD* as if it were a Sink-only, data-less device.

Table 4-22 Charge-Through VPD CC Impedance (RccCON) Requirements

	Minimum	Maximum	Description
RccCON		15 Ω	Impedance in the Charge-Though VPD while a connection is enabled between the host port CC and Charge-Through port CC.
	zOPEN		Impedance between the host port CC and Charge-Through CC when a connection is disabled.

Table 4-23 CTVPD Charge-Through Port VBUS Bypass Requirements

	Minimum	Maximum	Description
CCTB	1 µF	10 µF	Bypass capacitance on Charge-Through port VBUS connection to support ADP max CADP_THR

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

通过连接到源，主机可以通过 *USB PD* 宣传和支持的内容存在限制：

• 主机不得协商或接受 PR_Swap 或 VCONN_Swap • 主机不得启用 FR_Swap • 主机只能在使用 *USB PD* 修订版 2.0 时协商 DR_Swap，并且只能用于切换哪一侧是 PD 总线主控。主机将始终保持 USB 数据的 DFP。• 主机不得在其 SourceCapability 或 SinkCapability 消息中宣传双角色数据或双角色电源 - 主机将其宣传的功能更改为 UFP 角色/仅接收器角色。• 主机不得协商任何改变引脚功能的替代模式

连接器。•主机应使用*USB PD*向充电源展示自己，就好像它是一个仅接收数据、无数据的设备一样。

表 4-22 充电通过 VPD CC 阻抗 (RccCON) 要求

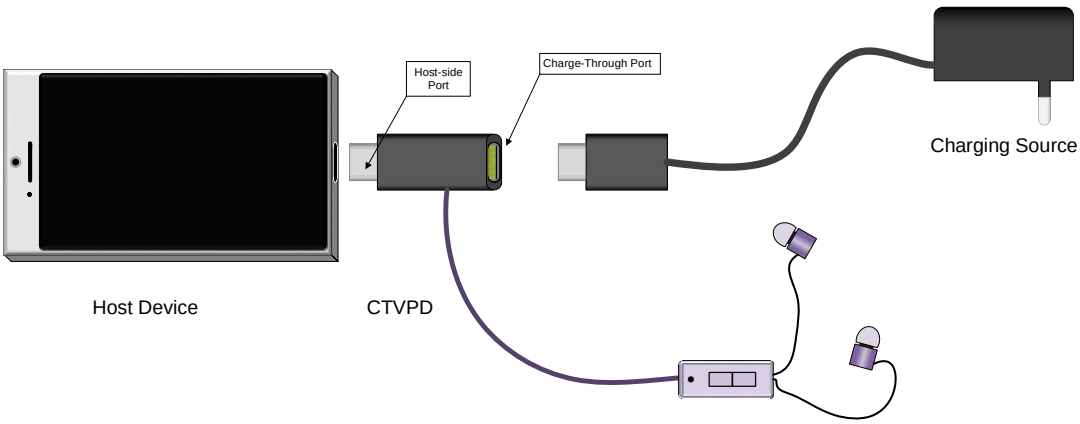
	Minimum	Maximum	Description
RccCON		15 Ω	Impedance in the Charge-Though VPD while a connection is enabled between the host port CC and Charge-Through port CC.
	zOPEN		Impedance between the host port CC and Charge-Through CC when a connection is disabled.

表 4-23 CTVPD 充电端口 VBUS 旁路要求

	Minimum	Maximum	Description
C_{CTB}	1 µF	10 µF	Bypass capacitance on Charge-Through port V_{BUS} connection to support ADP max C_{ADP_THR}

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-43 Example Charge-Through VCONN-Power USB Device Use Case



4.11 Parameter Values

4.11.1 Termination Parameters

Table 4-24 provides the values that shall be used for the Source's Rp or current source. Other pull-up voltages shall be allowed if they remain less than 5.5 V and fall within the correct voltage ranges on the Sink side – see Table 4-32, Table 4-33 and Table 4-34. Note: when two Sources are connected together, they may use different termination methods which could result in unexpected current flow.

Table 4-24 Source CC Termination (Rp) Requirements

Source Advertisement	Current Source to 1.7 – 5.5 V	Resistor pull-up to 4.75 – 5.5 V	Resistor pull-up to 3.3 V ± 5%
Default USB Power	80 µA ± 20%	56 kΩ ± 20% (Note 1)	36 kΩ ± 20%
1.5 A @ 5 V	180 µA ± 8%	22 kΩ ± 5%	12 kΩ ± 5%
3.0 A @ 5 V	330 µA ± 8%	10 kΩ ± 5%	4.7 kΩ ± 5%

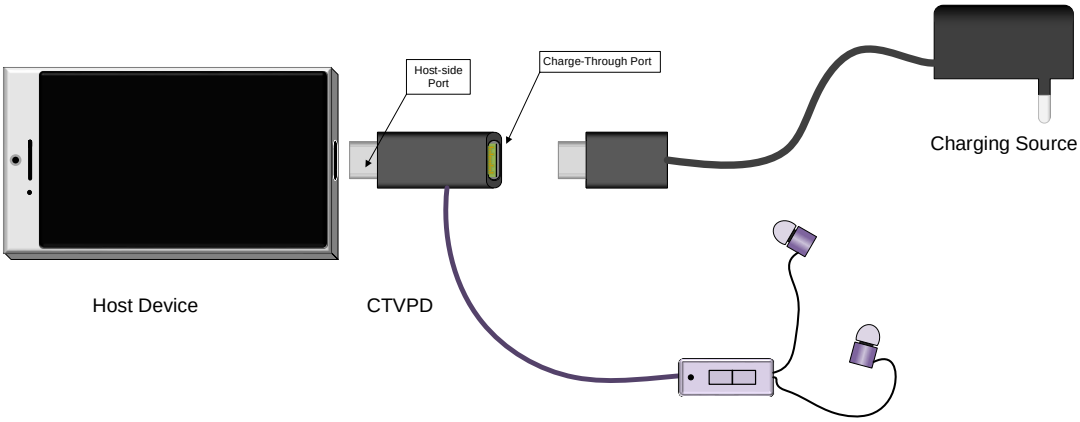
Notes:

1. For Rp when implemented in the USB Type-C plug on a USB Type-C to *USB 3.1* Standard-A Cable Assembly, a USB Type-C to *USB 2.0* Standard-A Cable Assembly, a USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly or a USB Type-C captive cable connected to a USB host, a value of 56 kΩ ± 5% shall be used, in order to provide tolerance to IR drop on VBUS and GND in the cable assembly.

The Sink may find it convenient to implement Rd in multiple ways simultaneously (a wide range Rd when unpowered and a trimmed Rd when powered). Transitions between Rd implementations that do not exceed tCCDebounce shall not be interpreted as exceeding the wider Rd range. Transitions between Rd implementations shall not allow the voltage on CC to go outside the voltage band that defines a connection. Table 4-25 provides the methods and values that shall be used for the Sink's Rd implementation.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-43 通过 VCONN 供电的 USB 设备充电用例示例



4.11 参数值

4.11.1 终止参数

表 4-24 提供了应用于源极 Rp 或电流源的值。如果其他上拉电压保持低于 5.5 V 且在接收器侧的正确电压范围内，则应允许使用 - 请参阅表 4-32、表 4-33 和表 4-34。注意：当两个源极连接在一起时，它们可能使用不同的端接方法，这可能会导致意外的电流流动。

表 4-24 源 CC 终端 (Rp) 要求

Source Advertisement	Current Source to 1.7 – 5.5 V	Resistor pull-up to 4.75 – 5.5 V	Resistor pull-up to 3.3 V ± 5%
Default USB Power	80 µA ± 20%	56 kΩ ± 20% (Note 1)	36 kΩ ± 20%
1.5 A @ 5 V	180 µA ± 8%	22 kΩ ± 5%	12 kΩ ± 5%
3.0 A @ 5 V	330 µA ± 8%	10 kΩ ± 5%	4.7 kΩ ± 5%

笔记：

1. 对于在 USB Type-C 至 *USB 3.1* 标准 A 型电缆组件、USB Type-C 至 *USB 2.0* 标准 A 型电缆组件、USB Type-C 至 *USB 2.0* Micro-B 插座适配器组件或连接到 USB 主机的 USB Type-C 固定电缆上的 USB Type-C 插头中实现的 Rp，应使用 56 kΩ ± 5% 的值，以便为电缆组件中的 VBUS 和 GND 上的 IR 压降提供容差。

Sink 可能会发现同时以多种方式实现 Rd 很方便（未通电时使用宽范围 Rd，通电时使用修剪后的 Rd）。不超过 tCCDebounce 的 Rd 实现之间的转换不应被解释为超出更宽的 Rd 范围。Rd 实现之间的转换不应允许 CC 上的电压超出定义连接的电压带。表 4-25 提供了应用于 Sink 的 Rd 实现的方法和值。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 4-25 Sink CC Termination (Rd) Requirements

Rd Implementation	Nominal value	Can detect power capability?	Max voltage on pin
± 20% voltage clamp[1]	1.1 V	No	1.32 V
± 20% resistor to GND	5.1 kΩ	No	2.18 V
± 10% resistor to GND	5.1 kΩ	Yes	2.04 V

Note:
1. The clamp implementation inhibits *USB PD* communication although the system can start with the clamp and transition to the resistor once it is able to do *USB PD*.

Table 4-26 provides the impedance value to ground on VCONN in powered cables.

Table 4-26 Powered Cable Termination Requirements

	Minimum Impedance	Maximum Impedance
Ra	800 Ω[1]	1.2 kΩ

Note:
1. The minimum impedance may be less when powering active circuitry.

Table 4-27 provides the minimum impedance value to ground on CC for a device (Sink or Source) to be undetected by a Source. This shall apply for ports in the Disabled state or ErrorRecovery state. This shall also apply for Sources when unpowered (for example a power brick unplugged from AC mains).

Table 4-27 CC Termination Requirements for Disabled state, ErrorRecovery state, and Unpowered Source

	Minimum Impedance to GND
zOPEN	126 kΩ

Table 4-28 provides the impedance value for an SBU to appear open.

Table 4-28 SBU Termination Requirements

	Termination	Notes
zSBUTermination	≥ 950 kΩ	Functional equivalent to an open circuit

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 4-25 接收器 CC 终端 (Rd) 要求

Rd Implementation	Nominal value	Can detect power capability?	Max voltage on pin
± 20% voltage clamp[1]	1.1 V	No	1.32 V
± 20% resistor to GND	5.1 kΩ	No	2.18 V
± 10% resistor to GND	5.1 kΩ	Yes	2.04 V

否注意：1. 尽管系统可以从钳位开始，并在能够执行 *USB PD* 时转换到电阻器，但钳位实现会抑制 *USB PD* 通信
。

表 4-26 提供了供电电缆中 VCONN 到地的阻抗值。

表 4-26 供电电缆端接要求

	Minimum Impedance	Maximum Impedance
Ra	800 Ω[1]	1.2 kΩ

注意：1. 为有源电路供电时，最小阻抗可能会更小。

表 4-27 提供了 CC 上设备（接收器或源）无法被源检测到的接地最小阻抗值。这适用于处于禁用状态或错误恢复状态的端口。这也适用于断电时的源（例如从交流电源上拔下的电源块）。

表 4-27 禁用状态下的 CC 终止要求，
错误恢复状态，以及无电源

	Minimum Impedance to GND
zOPEN	126 kΩ

表 4-28 提供了 SBU 出现开路的阻抗值。

表 4-28 SBU 端接要求

	Termination	Notes
zSBUTermination	≥ 950 kΩ	Functional equivalent to an open circuit

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.11.2 Timing Parameters

Table 4-29 provides the timing values that shall be met for delivering power over VBUS and VCONN.

Table 4-29 VBUS and VCONN Timing Parameters

	Minimum	Maximum	Description
tVBUSON	0 ms	275 ms	From entry to Attached.SRC until VBUS reaches the minimum vSafe5V threshold as measured at the source's receptacle.
tVBUSOFF	0 ms	650 ms	From the time the Sink is detached until the Source removes VBUS and reaches vSafe0V (See *USB PD*).
tVCONNON	Note 1	2 ms	From the time the Source supplied VBUS in the Attached.SRC state. Measured from vSafe5V to the minimum VCONN voltage (see Table 4-5)
tVCONNON-PA	0 ms	100 ms	From the time a Sink with accessory support enters the PoweredAccessory state until the Sink sources minimum VCONN voltage (see Table 4-5)
tVCONNOFF	0 ms	35 ms	From the time that a Sink is detached or as directed until the VCONN supply is disconnected.
tSinkAdj	tRpValueChange (Min)	60 ms	Response time for a Sink to adjust its current consumption to be in the specified range due to a change in USB Type-C Current advertisement

Note:

1. VCONN may be applied prior to the application of VBUS

Figure 4-44 illustrates the timing parameters associated with the DRP toggling process. The tDRP parameter represents the overall period for a single cycle during which the port is exposed as both a Source and a Sink. The portion of the period where the DRP is exposed as a Source is established by dcSRC.DRP and the maximum transition time between the exposed states is dictated by tDRPTransition.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4.11.2 时序参数

表 4-29 提供了通过 V BUS 和 VCONN 供电必须满足的时序值。

表 4-29 VBUS 和 VCONN 时序参数

	Minimum	Maximum	Description
tVBUSON	0 ms	275 ms	From entry to Attached.SRC until VBUS reaches the minimum vSafe5V threshold as measured at the source's receptacle.
tVBUSOFF	0 ms	650 ms	From the time the Sink is detached until the Source removes VBUS and reaches vSafe0V (See *USB PD*).
tVCONNON	Note 1	2 ms	From the time the Source supplied VBUS in the Attached.SRC state. Measured from vSafe5V to the minimum VCONN voltage (see Table 4-5)
tVCONNON-PA	0 ms	100 ms	From the time a Sink with accessory support enters the PoweredAccessory state until the Sink sources minimum VCONN voltage (see Table 4-5)
tVCONNOFF	0 ms	35 ms	From the time that a Sink is detached or as directed until the VCONN supply is disconnected.
tSinkAdj	tRpValueChange (Min)	60 ms	Response time for a Sink to adjust its current consumption to be in the specified range due to a change in USB Type-C Current advertisement

注意：1. VCONN 可以先于 VBUS 申请

图 4-44 说明了与 DRP 切换过程相关的时序参数。tDRP 参数表示单个周期内端口同时作为源和接收器暴露的总时间。DRP 作为源暴露的时间段由 dcSRC.DRP 确定，暴露状态之间的最大转换时间由 t DRPTransition 决定。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 4-44 DRP Timing

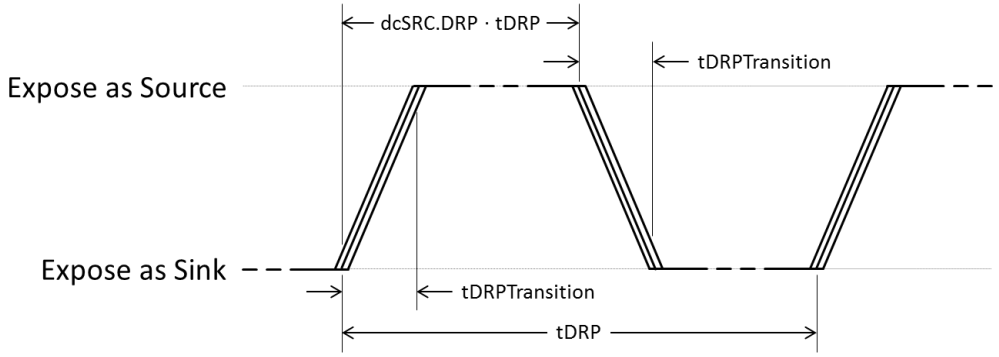


Table 4-30 provides the timing values that shall be met for DRPs. The clock used to control DRP swap should not be derived from a precision timing source such as a crystal, ceramic resonator, etc. to help minimize the probability of two DRP devices indefinitely failing to resolve into a Source-to-Sink relationship. Similarly, the percentage of time that a DRP spends advertising Source not be derived from a precision timing source.

Table 4-30 DRP Timing Parameters

	Minimum	Maximum	Description
tDRP	50 ms	100 ms	The period a DRP shall complete a Source to Sink and back advertisement
dcSRC.DRP	30%	70%	The percent of time that a DRP shall advertise Source during tDRP
tDRPTransition	0 ms	1 ms	The time a DRP shall complete transitions between Source and Sink roles during role resolution
tDRPTry	75 ms	150 ms	Wait time associated with the Try.SRC state.
tDRPTryWait	400 ms	800 ms	Wait time associated with the Try.SNK state.
tTryTimeout	550 ms	1100 ms	Timeout for transition from Try.SRC to TryWait.SNK.
tVPDDetach	10 ms	20 ms	Time for a DRP to detect that the connected Charge-Through VCONN-Powered USB Device has been detached, after VBUS has been removed.

Table 4-31 provides the timing requirement for CC connection behaviors.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 4-44 DRP 时序

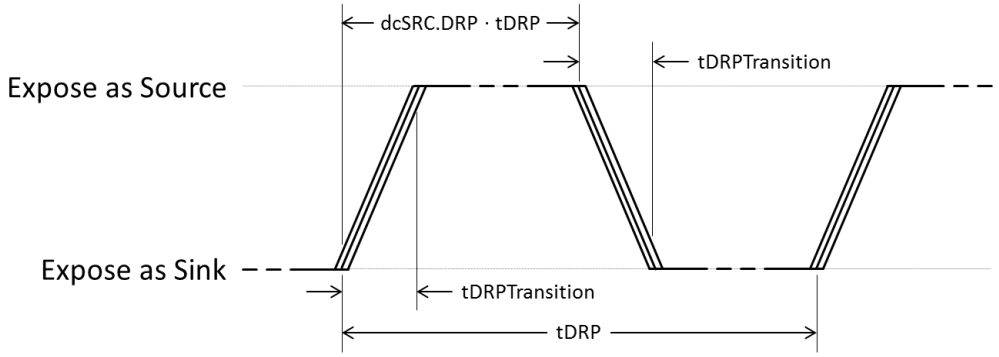


表 4-30 提供了 DRP 应满足的时序值。用于控制 DRP 交换的时钟不应来自精密时序源（例如晶体、陶瓷谐振器等），以帮助最大限度地降低两个 DRP 设备无限期无法解析为源到接收器关系的可能性。同样，DRP 用于通告源的时间百分比不应来自精密时序源。

表 4-30 DRP 时序参数

	Minimum	Maximum	Description
tDRP	50 ms	100 ms	The period a DRP shall complete a Source to Sink and back advertisement
dcSRC.DRP	30%	70%	The percent of time that a DRP shall advertise Source during tDRP
tDRPTransition	0 ms	1 ms	The time a DRP shall complete transitions between Source and Sink roles during role resolution
tDRPTry	75 ms	150 ms	Wait time associated with the Try.SRC state.
tDRPTryWait	400 ms	800 ms	Wait time associated with the Try.SNK state.
tTryTimeout	550 ms	1100 ms	Timeout for transition from Try.SRC to TryWait.SNK.
tVPDDetach	10 ms	20 ms	Time for a DRP to detect that the connected Charge-Through VCONN-Powered USB Device has been detached, after VBUS has been removed.

表 4-31 提供了 CC 连接行为的时序要求。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 4-31 CC Timing

	Minimum	Maximum	Description
tCCDebounce	100 ms	200 ms	Time a port shall wait before it can determine it is attached
tPDDebounce	10 ms	20 ms	Time a Sink port shall wait before it can determine it is detached due to the potential for *USB PD* signaling on CC as described in the state definitions.
tTryCCDebounce	10 ms	20 ms	Time a port shall wait before it can determine it is re-attached during the try-wait process.
tErrorRecovery	25 ms		Time a self-powered port shall remain in the ErrorRecovery state.
	240 ms		Time a source shall remain in the ErrorRecovery state if it was sourcing VCONN in the previous state.
tRpValueChange	10 ms	20 ms	Time a Sink port shall wait before it can determine there has been a change in Rp where CC is not BMC Idle or the port is unable to detect BMC Idle.
	0 ms	5 ms	Time a Sink port shall wait before it can determine that there has been a change in Rp when *USB PD* signaling can be detected by the port and CC line is BMC Idle.
tSRCDisconnect	0 ms	20 ms	Time a Source shall detect the SRC.Open state. The Source should detect the SRC.Open state as quickly as practical.
tNoToggleConnect	0 ms	5 ms	Time to detect connection when neither Port Partner is toggling.
tOnePortToggleConnect	0 ms	80 ms	Time to detect connection when one Port Partner is toggling (0ms … dcSRC.DRP max * tDRP max + 2 * tNoToggleConnect).
tTwoPortToggleConnect	0 ms	510 ms	Time to detect connection when both Port Partners are toggling (0ms … 5 * tDRP max + 2 * tNoToggleConnect).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 4-31 CC 时序

	Minimum	Maximum	Description
tCCDebounce	100 ms	200 ms	Time a port shall wait before it can determine it is attached
tPDDebounce	10 ms	20 ms	Time a Sink port shall wait before it can determine it is detached due to the potential for *USB PD* signaling on CC as described in the state definitions.
tTryCCDebounce	10 ms	20 ms	Time a port shall wait before it can determine it is re-attached during the try-wait process.
tErrorRecovery	25 ms		Time a self-powered port shall remain in the ErrorRecovery state.
	240 ms		Time a source shall remain in the ErrorRecovery state if it was sourcing VCONN in the previous state.
tRpValueChange	10 ms	20 ms	Time a Sink port shall wait before it can determine there has been a change in Rp where CC is not BMC Idle or the port is unable to detect BMC Idle.
	0 ms	5 ms	Time a Sink port shall wait before it can determine that there has been a change in Rp when *USB PD* signaling can be detected by the port and CC line is BMC Idle.
tSRCDisconnect	0 ms	20 ms	Time a Source shall detect the SRC.Open state. The Source should detect the SRC.Open state as quickly as practical.
tNoToggleConnect	0 ms	5 ms	Time to detect connection when neither Port Partner is toggling.
tOnePortToggleConnect	0 ms	80 ms	Time to detect connection when one Port Partner is toggling (0ms … dcSRC.DRP max * tDRP max + 2 * tNoToggleConnect).
tTwoPortToggleConnect	0 ms	510 ms	Time to detect connection when both Port Partners are toggling (0ms … 5 * tDRP max + 2 * tNoToggleConnect).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

	Minimum	Maximum	Description
tVPDCTDD	30 µs	5 ms	Time for a Charge-Through VCONN-Powered USB Device to detect that the Charge-Through source has disconnected from CC after VBUS has been removed, transition to CTUnattached.VPD, and re-apply its Rp termination advertising 3.0 A on the host port CC.
tVPDDisable	25 ms		Time for a Charge-Through VCONN-Powered USB Device shall remain in CTDisabled.VPD state.

4.11.3 Voltage Parameters

Table 4-32, Table 4-33 and Table 4-34 provide the CC voltage values that a Source shall use to detect what is attached based on the USB Type-C Current advertisement (Default USB, 1.5 A @ 5 V, or 3.0 A @ 5 V) that the Source is offering.

Table 4-32 CC Voltages on Source Side – Default USB

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.15 V	0.20 V
Sink (vRd)	0.25 V	1.50 V	1.60 V
No connect (vOPEN)	1.65 V		

Table 4-33 CC Voltages on Source Side – 1.5 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.35 V	0.40 V
Sink (vRd)	0.45 V	1.50 V	1.60 V
No connect (vOPEN)	1.65 V		

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

	Minimum	Maximum	Description
tVPDCTDD	30 µs	5 ms	Time for a Charge-Through VCONN-Powered USB Device to detect that the Charge-Through source has disconnected from CC after VBUS has been removed, transition to CTUnattached.VPD, and re-apply its Rp termination advertising 3.0 A on the host port CC.
tVPDDisable	25 ms		Time for a Charge-Through VCONN-Powered USB Device shall remain in CTDisabled.VPD state.

4.11.3 电压参数

表 4-32、表 4-33 和表 4-34 提供了源应使用的 CC 电压值，该值基于源提供的 USB Type-C 电流公告（默认 USB、1.5 A @ 5 V 或 3.0 A @ 5 V~~）来检测所连接的内~~容。

表 4-32 源侧 CC 电压 – 默认 USB

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.15 V	0.20 V
Sink (vRd)	0.25 V	1.50 V	1.60 V
No connect (vOPEN)	1.65 V		

表 4-33 源侧 CC 电压 – 1.5 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.35 V	0.40 V
Sink (vRd)	0.45 V	1.50 V	1.60 V
No connect (vOPEN)	1.65 V		

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 4-34 CC Voltages on Source Side – 3.0 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.75 V	0.80 V
Sink (vRd)	0.85 V	2.45 V	2.60 V
No connect (vOPEN)	2.75 V		

Table 4-35 provides the CC voltage values that shall be detected across a Sink's Rd for a Sink that does not support higher than default USB Type-C Current Source advertisements.

Table 4-35 Voltage on Sink CC Pins (Default USB Type-C Current only)

Detection	Min voltage	Max voltage	Threshold
vRa	−0.25 V	0.15 V	0.2 V
vRd-Connect	0.25 V	2.18 V	

Table 4-36 provides the CC voltage values that shall be detected across a Sink's Rd for a Sink that implements detection of higher than default USB Type-C Current Source advertisements. This table includes consideration for the effect that the IR drop across the cable GND has on the voltage across the Sink's Rd.

Table 4-36 Voltage on Sink CC pins (Multiple Source Current Advertisements)

Detection	Min voltage	Max voltage	Threshold
vRa	−0.25 V	0.15 V	0.2 V
vRd-Connect	0.25 V	2.04 V	
vRd-USB	0.25 V	0.61 V	0.66 V
vRd-1.5	0.70 V	1.16 V	1.23 V
vRd-3.0	1.31 V	2.04 V	

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 4-34 源侧 CC 电压 – 3.0 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.75 V	0.80 V
Sink (vRd)	0.85 V	2.45 V	2.60 V
No connect (vOPEN)	2.75 V		

表 4-35 提供了在 Sink 的 Rd 上应检测到的 CC 电压值
不支持高于默认 USB Type-C 电流源广告。

表 4-35 灌电流 CC 引脚上的电压（默认 USB Type-C 电流 仅限 nt)

Detection	Min voltage	Max voltage	Threshold
vRa	−0.25 V	0.15 V	0.2 V
vRd-Connect	0.25 V	2.18 V	

表 4-36 提供了在 Sink 的 Rd 上应检测到的 CC 电压值
可实现高于默认 USB Type-C 电流源广告的检测。此表考虑了电缆 GND 上的 IR 压降对 Sink 的 Rd 上电压的影响。

表 4-36 吸电流 CC 引脚电压（多源电流通告）

Detection	Min voltage	Max voltage	Threshold
vRa	−0.25 V	0.15 V	0.2 V
vRd-Connect	0.25 V	2.04 V	
vRd-USB	0.25 V	0.61 V	0.66 V
vRd-1.5	0.70 V	1.16 V	1.23 V
vRd-3.0	1.31 V	2.04 V	

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

5 USB4 Discovery and Entry

USB4™ discovery and operational entry differs significantly from *USB 2.0* and *USB 3.2*. This chapter defines the process of discovering across a USB Type-C® connection that both port partners are *USB4*-capable (or not), having the DFP-side of the link make a decision regarding to enter *USB4* operation (or not), and how operational entry is accomplished.

5.1 Overview of the Discovery and Entry Process

The following provides an overview of the general process for discovery and entry into *USB4* operation.

1. USB Type-C CC Connection State Machines resolve Source/Sink and the initial data roles (DFP/UFP).
2. Initial VBUS and VCONN power is supplied.
3. *USB Power Delivery* protocol is used to establish a power contract between the port partners.
4. *USB PD* Discover Identity process is used by the DFP to identify port partner (SOP) capabilities.
5. *USB PD* Discover Identity process is used by the DFP to identify cable (SOP') capabilities.
6. If the cable and port partner both support USB4 operation, the DFP issues *USB PD* Enter_USB Messages to both the cable and port partner to enter USB4 operation.
7. If both port partners are Dual-Role-Data (DRD) capable, either the DFP or UFP can optionally initiate a data-role swap in order to exchange host (master) and device (slave) roles.

The first three steps above are the same as used for all USB connections for establishing port relationships and power between the port partners. Step 5 where the cable is queried for its capabilities may optionally occur during Step 3, this would most likely be done before if the Source needs to know if the cable supports supplying current beyond 3 A.

Depending on the resulting power source relationship after the first few steps, the use of *USB PD* DR_Swap may be necessary to establish the port partner that is closest to the host as the data role DFP. For example, a hub supplying power to a host and DR_Swap is used to correct the data roles between the hub and host.

After the port partner's capabilities are identified by the DFP, it may be appropriate based on what is discovered about the port partner to also query the port partner using the *USB PD* Alternate Mode SVID discovery process as an extension to Step 4. There are situations where a port partner supports Alternate Modes that may also be useable during *USB4* operation and this would be discovered during this additional query.

After the cable capabilities are identified by the DFP, it may be appropriate based on what is discovered about the cable to also query the cable using the *USB PD* Alternate Mode SVID discovery process as an extension to Step 5. There are situations where a cable that supports Thunderbolt™ 3 Alternate Mode may also be useable for *USB4* operation and this would be discovered during this additional query.

USB4 operation is entered using a *USB PD* USB Enter_USB Message. This message will be sent to both the cable (SOP' and SOP" if present) and the port partner (SOP), each of which will respond with an Accept message to confirm and establish when the cable or port partner is functionally ready for *USB4* operation. If the cable to be used will be operating in

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

5 USB4 发现与入门

USB4™ 发现和操作进入与 *USB 2.0* 和 *USB 3.2* 有很大不同。本章定义了通过 USB Type-C® 连接发现两个端口伙伴是否支持 *USB4* 的过程，让链路的 DFP 端决定是否进入 *USB4* 操作，以及如何完成操作进入。

5.1 发现和进入过程概述

下面概述了发现和进入 *USB4* 操作的一般过程。

1. USB Type-C CC 连接状态机解析源/接收器和初始数据角色（DFP/UFP）。 2. 提供初始 VBUS 和 VCONN 电源。 3. *USB Power Delivery* 协议用于在端口伙伴之间建立电源合约。 4. DFP 使用 *USB PD* 发现身份过程来识别端口伙伴（SOP）功能。 5. DFP 使用 *USB PD* 发现身份过程来识别电缆（SOP ’ ）功能。 6. 如果电缆和端口伙伴都支持 USB4 操作，则 DFP 向电缆和端口伙伴发出 *USB PD* Enter_USB 消息以进入 USB4 操作。 7. 如果两个端口伙伴都具有双角色数据 (DRD) 功能，则 DFP 或 UFP 可以选择启动数据角色交换，以交换主机（主设备）和设备（从设备）角色。

上述前三个步骤与用于所有 USB 连接的步骤相同，用于在端口伙伴之间建立端口关系和电源。步骤 5（查询电缆的功能）可以选择性地在步骤 3 期间进行，如果源端需要知道电缆是否支持提供超过 3 A 的电流，则这很可能在之前完成。

根据前几个步骤后产生的电源关系，可能需要使用 *USB PD* DR_Swap 来建立最靠近主机的端口伙伴作为数据角色 DFP。例如，集线器为主机供电，DR_Swap 用于纠正集线器和主机之间的数据角色。

在 DFP 识别出端口伙伴的功能后，根据对端口伙伴的发现，使用 *USB PD* 备用模式 SVID 发现过程查询端口伙伴可能是适当的，作为步骤 4 的扩展。在某些情况下，端口伙伴支持备用模式，这些模式在 *USB4* 操作期间也可能可用，这将在此次额外查询中发现。

在 DFP 识别出电缆功能后，根据对电缆的发现，可能还需要使用 *USB PD* 备用模式 SVID 发现过程来查询电缆，作为步骤 5 的扩展。在某些情况下，支持 Thunderbolt™ 3 备用模式的电缆也可用于 *USB4* 操作，这将在此次额外查询中发现。

使用 *USB PD* USB Enter_USB 消息输入 *USB4* 操作。此消息将发送到电缆（SOP ’ 和 SOP ” 如果存在）和端口伙伴（SOP），每个都将以接受消息响应以确认和确定电缆或端口伙伴何时在功能上已准备好进行 *USB4* 操作。如果要使用的电缆将以

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Thunderbolt 3 Alternate Mode, then the cable will be enabled using the *USB PD* Enter Mode Command instead of the *USB PD* USB Enter_USB Message (See Appendix F).

USB4 functionally enables an ability for connecting two host platforms and establishing a data channel between the hosts, this is dependent on at least one of these host platforms being capable of Dual-Role-Data operation so that a proper USB Type-C DFP-to-UFP data relationship can be established between them. In most cases, both host platforms will be DRD-capable and once USB4 operation is established, either of these host platforms can choose to initiate a change of its role in the DFP-to-UFP relationship. To accomplish this, the *USB PD* DR_Swap process is used during Step 7 listed above.

5.2 USB4 Functional Requirements

The following functional requirements are for *USB4* hosts and devices.

5.2.1 USB4 Host Functional Requirements

USB4 hosts shall meet the following functional requirements:

- *USB4* hosts with dual-role-data (DRD) support shall respond to *USB PD* Discover Identity command with both DFP and UFP VDOs.

5.2.2 USB4 Device Functional Requirements

USB4 devices shall meet the following functional requirements:

- *USB4* devices shall respond to *USB PD* Discover Identity command with UFP VDOs.
- *USB4* devices shall provide a USB interface exposing a *USB Billboard Device Class* when it cannot connect as a *USB4* device within tUSB4Timeout.
- If the *USB4* device additionally supports Alternate Modes, the device shall complete the *USB4* discovery and entry process (successful or not) before falling back to *USB 3.2* or *USB 2.0* and exposing an appropriate *USB Billboard Device Class*.

5.2.3 USB4 Alternate Mode Support

The *USB4* specification enables products to be designed to support Alternate Modes, specifically *DisplayPort™ Alt Mode* and *Thunderbolt 3 Alt Mode*. Unlike *USB 3.2* and *USB 2.0* hubs, this also includes supporting specific Alternate Modes on *USB4* hubs.

5.2.3.1 USB4 Alternate Mode Support on Hosts

For *USB4* hosts that implement DisplayPort Tunneling, *DP Alt Mode* with Multi-function support (DP_BR 1 channel signaling combined with USB 3.2 Gen 1x1 support) as defined by the *DisplayPort Alt Mode* specification shall be implemented on all of its USB Type-C DFPs.

The *USB4* host shall support the first connected DisplayPort display on any of its USB Type-C ports. Support for subsequently connected DisplayPort displays is optional.

USB4 hosts may optionally implement *TBT3* compatibility support as defined by the *USB4* specification on its USB Type-C DFPs.

5.2.3.2 USB4 Alternate Mode Support on Hubs and USB4-based Docks

USB4 hubs and *USB4*–based docks shall implement *DP Alt Mode* with Multi-function support (DP_BR 1 channel signaling combined with USB 3.2 Gen 1x1 support) as defined by the *DisplayPort Alt Mode* specification on all of its USB Type-C DFPs.

USB4 hubs shall support the first connected DisplayPort display on any of its USB Type-C DFPs. Support for subsequently connected DisplayPort displays is optional.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Thunderbolt 3 备用模式，则将使用 *USB PD* 进入模式命令而不是 *USB PD* USB Enter USB 消息启用电缆（参见附录 F）。

USB4 在功能上实现了连接两个主机平台并在主机之间建立数据通道的能力，这取决于这些主机平台中至少有一个能够进行双角色数据操作，以便可以在它们之间建立正确的 USB Type-C DFP 到 UFP 数据关系。在大多数情况下，两个主机平台都具有 DRD 功能，一旦建立了 USB4 操作，这两个主机平台中的任何一个都可以选择启动其在 DFP 到 UFP 关系中的角色更改。为了实现这一点，在上面列出的第 7 步中使用了 *USB PD* DR_Swap 过程。

5.2 USB4 功能要求

以下功能要求针对的是*USB4*主机和设备。

5.2.1 USB4 主机功能要求

*USB4*主机应满足以下功能要求：

具有双角色数据 (DRD) 支持的 • *USB4* 主机应使用 DFP 和 UFP VDO 响应 *USB PD* 发现身份命令。

5.2.2 USB4 设备功能要求

*USB4*设备应满足以下功能要求：

• *USB4* 设备应使用 UFP VDO 响应 *USB PD* Discover Identity 命令。• *USB4* 设备应提供一个 USB 接口，当它无法在 tUSB4Timeout 内作为 *USB4* 设备连接时，该接口会暴露 *USB Billboard Device Class*。• 如果 *USB4* 设备还支持备用模式，则该设备应完成

USB4 发现和进入过程（成功或失败）然后再回退到 *USB*、*3.2* 或 *USB 2.0* 并暴露适当的 *USB Billboard Device Class*。

5.2.3 USB4 备用模式支持

USB4 规范使产品能够设计为支持备用模式，特别是 *DisplayPort™ Alt Mode* 和 *Thunderbolt 3 Alt Mode*。与 *USB 3.2* 和 *USB 2.0* 集线器不同，这还包括在 *USB4* 集线器上支持特定备用模式。

5.2.3.1 主机上的 USB4 备用模式支持

对于实现 DisplayPort 隧道的 *USB4* 主机，应在其所有 USB Type-C DFP 上实现 *DisplayPort Alt Mode* 规范定义的具有多功能支持的 *DP Alt Mode*（DP_BR 1 通道信令与 USB 3.2 Gen 1x1 支持相结合）。

USB4 主机应支持其任意 USB Type-C 端口上连接的第一个 DisplayPort 显示器。对后续连接的 DisplayPort 显示器的支持是可选的。

USB4 主机可以选择在其 USB Type-C DFP 上实现 *USB4* 规范定义的 *TBT3* 兼容性支持。

5.2.3.2 集线器和基于 USB4 的基座支持 USB4 备用模式

USB4 集线器和基于 *USB4* 的扩展坞应实现具有多功能支持的 *DP Alt Mode*（DP_BR 1 通道信号与 USB 3.2 Gen 1x1 支持相结合），如所有 USB Type-C DFP 上的 *DisplayPort Alt Mode* 规范所定义。

USB4 集线器应支持其任何 USB Type-C DFP 上第一个连接的 DisplayPort 显示器。对后续连接的 DisplayPort 显示器的支持是可选的。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

USB4-based docks shall support the first connected display on any of its USB Type-C DFPs or non-USB display connectors (if present, collectively). Support for subsequently connected displays is optional.

USB4 hubs shall implement *TBT3* compatibility support as defined by the *USB4* specification on its USB Type-C DFPs. *USB4*–based docks shall implement *TBT3* compatibility support as defined by the *USB4* specification on its USB Type-C UFP and USB Type-C DFPs.

For *USB4* hubs, downstream-facing ports shall not implement Alternate Modes that do not have a USB-IF Standard ID (SID) or Accessory Modes.

5.3 USB4 Power Requirements

USB4 requires that the power connection between the port partners be established and maintained using *USB PD* prior to and through-out *USB4* operation. A *USB4* port, prior to entering *USB4* operation, shall operate as a *USB 3.2* port with regarding power (See Section 4.6). *USB4* does not use the USB device protocols defined in *USB 2.0* and *USB 3.2* for managing device power.

5.3.1 Source Power Requirements

For USB Type-C ports that support *USB4* data bus operation, the following requirements shall be met.

- *USB4* ports shall be minimally capable of supplying at least 7.5 W (i.e. 5 V @ 1.5 A) on VBUS to bus-powered *USB4* devices.
- The minimum capability for powering bus powered devices on data-capable ports shall be independently met on each USB Type-C port of a multi-port host or hub.

5.3.2 Sink Power Requirements

For *USB4* devices that rely on bus power to operate (independent of any charging needs), the following requirements shall be met.

- *USB4* devices shall draw only up to 250 mA on VBUS when the Source advertises Default USB power (see Section 4.11.1) prior to a *USB PD* power contract being made between the device and its port partner.
    - *USB4* devices may draw higher levels of power prior to a *USB PD* power contract being made if the Source advertises USB Type-C Current at either 1.5 A or 3.0 A.
- *USB4* devices shall be minimally capable of operating with a Source that only delivers up to 7.5 W (i.e. 5 V @ 1.5 A).
- *USB4* devices shall not enter into *USB4* data bus operation until after a *USB PD* power contract has been established, and while in *USB4* operation, the device shall adhere to *USB PD* power behavioral requirements at all times including appropriately responding to changes in Source capabilities.

In cases where the full functional capabilities or the highest performance of the *USB4* device requires more than the power being offered by the host, the device shall be minimally capable of providing the user with basic functionality as expected for the type and listed functions of the device. This allows for making available a higher level of operation or performance when a higher level of power is supplied, e.g. 15 W for full functionality versus 7.5 W for basic functionality. In this case, the device shall expose a Billboard that indicates functionality is limited by the available power.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

基于 *USB4* 的基座应支持其任何 USB Type-C DFP 或非 USB 显示器连接器（如果存在，则统称）上的第一个连接的显示器。对后续连接的显示器的支持是可选的。

USB4 集线器应在其 USB Type-C DFP 上实现 *USB4* 规范定义的 *TBT3* 兼容性支持。基于 *USB4* 的基座应在其 USB Type-C UFP 和 USB Type-C DFP 上实现 *USB4* 规范定义的 *TBT3* 兼容性支持。

对于 *USB4* 集线器，面向下游的端口不得实现没有 USB-IF 标准 ID (SID) 或附件模式的替代模式。

5.3 USB4 电源要求

USB4 要求在 *USB4* 操作之前和整个操作过程中使用 *USB PD* 建立并维持端口伙伴之间的电源连接。在进入 *USB4* 操作之前，*USB4* 端口应作为具有相关电源的 *USB 3.2* 端口运行（参见第 4.6 节）。*USB4* 不使用 *USB 2.0* 和 *USB 3.2* 中定义的 USB 设备协议来管理设备电源。

5.3.1 电源要求

对于支持*USB4*数据总线操作的USB Type-C端口，应满足以下要求。

- *USB4* 端口至少应能够在 VBUS 上为总线供电的 *USB4* 设备提供至少 7.5 W（即 5 V @ 1.5 A）的功率。• 在多端口主机或集线器的每个 USB Type-C 端口上，应独立满足为数据功能端口上的总线供电设备供电的最低能力。

5.3.2 接收器电源要求

对于依靠总线电源运行（独立于任何充电需求）的 *USB4* 设备，应满足以下要求。

- *USB4* 在设备与其端口伙伴之间建立 *USB PD* 电源合同之前，如果源端公布默认 USB 电源（见第 4.11.1 节），则 *USB4* 设备在 VBUS 上最多只能消耗 250 mA 的电流。 o 如果源端公布的 USB Type-C 电流为 1.5 A 或 3.0 A，则 *USB4* 设备可以在建立 *USB PD* 电源合同之前消耗更高的电量。 • *USB4* 设备至少能够使用仅提供最高 7.5 W（即 5 V @ 1.5 A）的源进行操作。 • *USB4* 设备在建立 *USB PD* 电源合同之前不得进入 *USB4* 数据总线操作，并且在 *USB4* 操作期间，设备应始终遵守 *USB PD* 电源行为要求，包括适当响应源功能的变化。

如果 *USB4* 设备的全部功能或最高性能需要的功率超过主机提供的功率，则设备应至少能够为用户提供设备类型和所列功能所预期的基本功能。这样，当提供更高级别的功率时，就可以提供更高级别的操作或性能，例如，15 W 可实现全部功能，而 7.5 W 可实现基本功能。在这种情况下，设备应显示一个公告牌，表明功能受到可用功率的限制。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

5.3.3 Device Power Management Requirements

For *USB4*, device power management is enabled using a combination of *USB PD* capabilities that operate in conjunction with the *USB4* link states of the device's UFP connection.

The connection between the device's UFP and its DFP port partner can be put into a suspend state based on the value of the USB Suspend Supported Flag in the Source-Capabilities Message used in the *USB PD* explicit power contract.

When the USB Suspend Supported Flag is set by the Source, the Sink shall meet the Suspend power requirement when the *USB4* link is in the CLd state. Prior to the entry of the link into CLd state, it is expected that the host will have placed all of the device's functions into an appropriate suspend state.

Suspend power is defined based on the capabilities of the *USB4* device:

- *USB4* Device that is not capable of remote wake or has remote wake disabled: 25 mW
- *USB4* Device that supports remote wake and has remote wake enabled: 50 mW

If the Source clears the USB Suspend Supported Flag, the Sink shall follow Explicit Contract power requirements regardless of the *USB4* link state. For *USB4*, the use of *USB PD* zero negotiated current is not a valid Suspend entry method since it is not coordinated with the host operating system and the function device drivers.

5.4 USB4 Discovery and Entry Flow Requirements

This section provides the detailed requirements for *USB4* discovery and entry. Additional requirements related to *USB4* operation are in the *USB4 Specification*.

Prior to entering and during *USB4* operation, the functional requirements of Chapter 4 shall be met including all functional interface and configuration channel (CC) requirements.

5.4.1 USB Type-C Initial Connection

For a *USB4*-capable port, prior to initiating *USB4* cable and device discovery, a valid Source-to-Sink connection shall exist and the USB Type-C connection state machine of the port shall either be in the Attached.SRC or Attached.SNK state.

When two *USB4* dual-role-data (DRD) products are connected together, e.g. two *USB4* hosts, USB Type-C connection process will establish the initial data roles between the port partners.

Once the initial data roles are established, the USB Type-C connection will proceed to train the link for both *USB 3.2* and *USB 2.0*. Once the *USB4* DFP completes the training of the links, it shall hold off on enabling the *USB 3.2* and *USB 2.0* enumeration of the attached UFP to allow for the completion of the *USB4* discovery and entry process. Once the *USB4* discovery and entry process has completed, the DFP will enable USB device enumeration on the *USB 3.2* (either via the *USB4* SuperSpeed USB tunnel or natively depending on if the port connection is *USB4* or *USB 3.2*, respectively) and *USB 2.0* data paths that are established with its UFP port partner at that time.

5.4.2 USB Power Delivery Contract

Prior to initiating *USB4* device discovery, the port partners shall negotiate a *USB PD* Explicit Contract.

During the process of establishing a stable *USB PD* Explicit Contract, the Source or Sink may have initiated power-role and VCONN swaps. Prior to moving on to USB4 discovery, the functional data role shall be properly established (e.g. a self-powered hub upstream facing

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

5.3.3 设备电源管理要求

对于 *USB4*，设备电源管理是使用 *USB PD* 功能组合来启用的，该功能与设备的 UFP 连接的 *USB4* 链路状态配合使用。

设备的 UFP 与其 DFP 端口伙伴之间的连接可以处于暂停状态
根据 *USB PD* 显式电源合同中使用的源功能消息中的 USB 暂停支持标志的值来确定状态。

当源端设置 USB 暂停支持标志时，接收器应在 *USB4* 链路处于 CLd 状态时满足暂停功率要求。在链路进入 CLd 状态之前，预计主机会将设备的所有功能置于适当的暂停状态。

暂停 p 权力是根据 *USB4* 的能力来定义的 设备：

- *USB4* 无法远程唤醒或已禁用远程唤醒的设备：25 mW • *USB4* 支持远程唤醒且已启用远程唤醒的设备：50 mW

如果源端清除 USB 暂停支持标志，则无论 *USB4* 链接状态如何，接收器都应遵循显式合同电源要求。对于 *USB4*，使用 *USB PD* 零协商电流不是有效的暂停进入方法，因为它与主机操作系统和功能设备驱动程序不协调。

5.4 USB4 发现和进入流程要求

本节提供了 *USB4* 发现和进入的详细要求。与 *USB4* 操作相关的其他要求请参阅 *USB4 Specification*。

在进入 *USB4* 操作之前和操作期间，应满足第 4 章的功能要求，包括所有功能接口和配置通道 (CC) 要求。

5.4.1 USB Type-C 初始连接

对于支持 *USB4* 的端口，在启动 *USB4* 电缆和设备发现之前，应存在有效的源到接收器连接，并且端口的 USB Type-C 连接状态机应处于 Attached.SRC 或 Attached.SNK 状态。

当两个 *USB4* 双角色数据 (DRD) 产品连接在一起时，例如两个 *USB4* 主机，USB Type-C 连接过程将在端口伙伴之间建立初始数据角色。

一旦建立了初始数据角色，USB Type-C 连接将继续训练 *USB 3.2* 和 *USB 2.0* 的链路。一旦 *USB4* DFP 完成链路训练，它将暂停启用所连接 UFP 的 *USB 3.2* 和 *USB 2.0* 枚举，以完成 *USB4* 发现和进入过程。一旦 *USB4* 发现和进入过程完成，DFP 将在当时与其 UFP 端口伙伴建立的 *USB 3.2*（通过 *USB4* 超高速 USB 隧道或本地方式，具体取决于端口连接是 *USB4* 还是 *USB 3.2*）和 *USB 2.0* 数据路径上启用 USB 设备枚举。

5.4.2 USB 电力输送合同

在启动 *USB4* 设备发现之前，端口合作伙伴应协商 *USB PD* 明确合同。

在建立稳定的 *USB PD* 显式合同的过程中，源或接收器可能已启动电源角色和 VCONN 交换。在继续进行 USB4 发现之前，应正确建立功能数据角色（例如，面向上游的自供电集线器

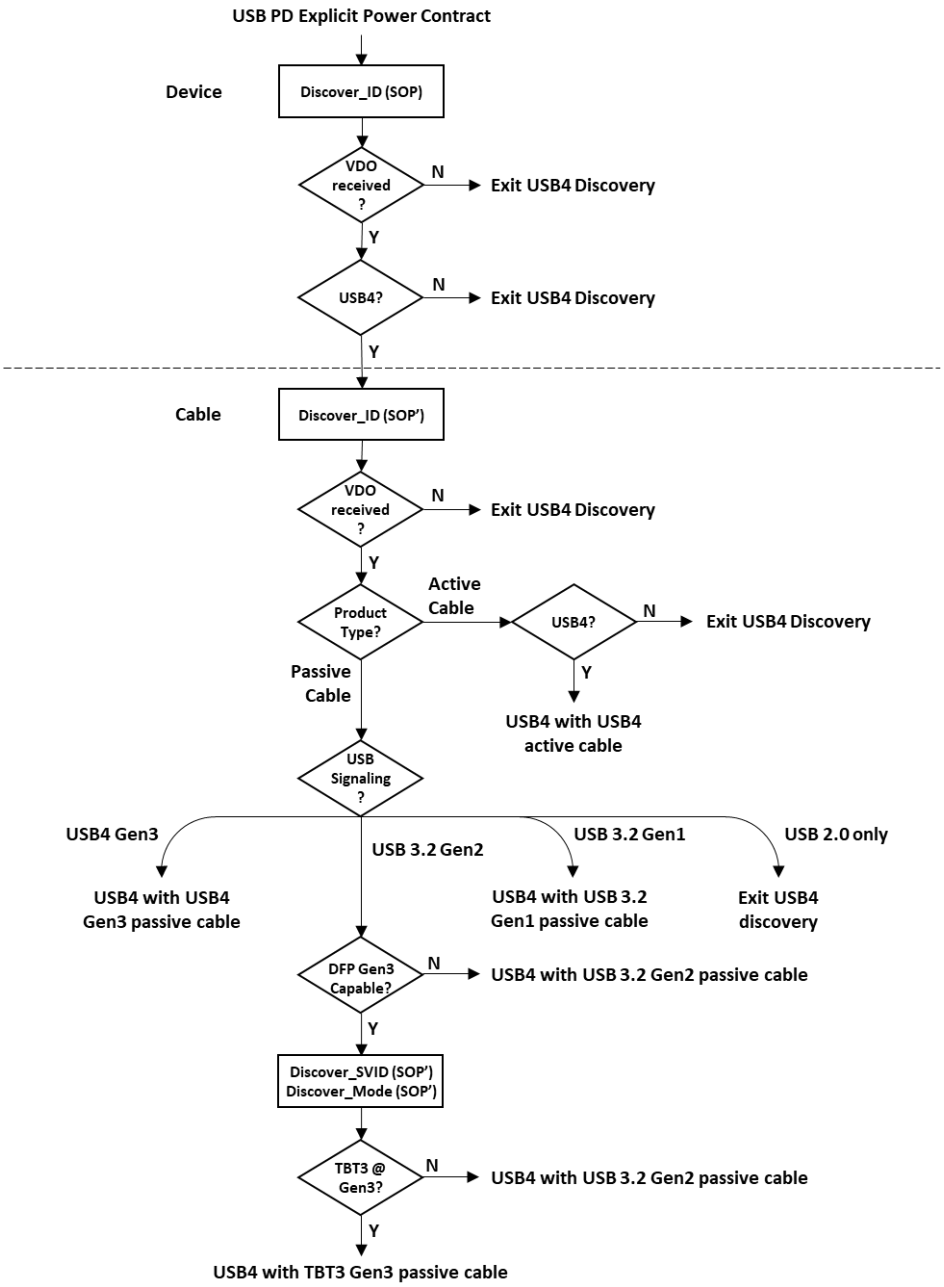
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

port is a DRP and comes up as a Source where DR_Swap is then required to the correct data role to the hub) and the DFP shall be the source of VCONN.

5.4.3 USB4 Discovery and Entry Flow

Figure 5-1 illustrates the basic flow model for *USB4* discovery and entry.

Figure 5-1 USB4 Discovery and Entry Flow Model



5.4.3.1 USB4 Device Discovery (SOP)

USB4 device discovery shall occur only after having a negotiated *USB PD* Explicit Contract.

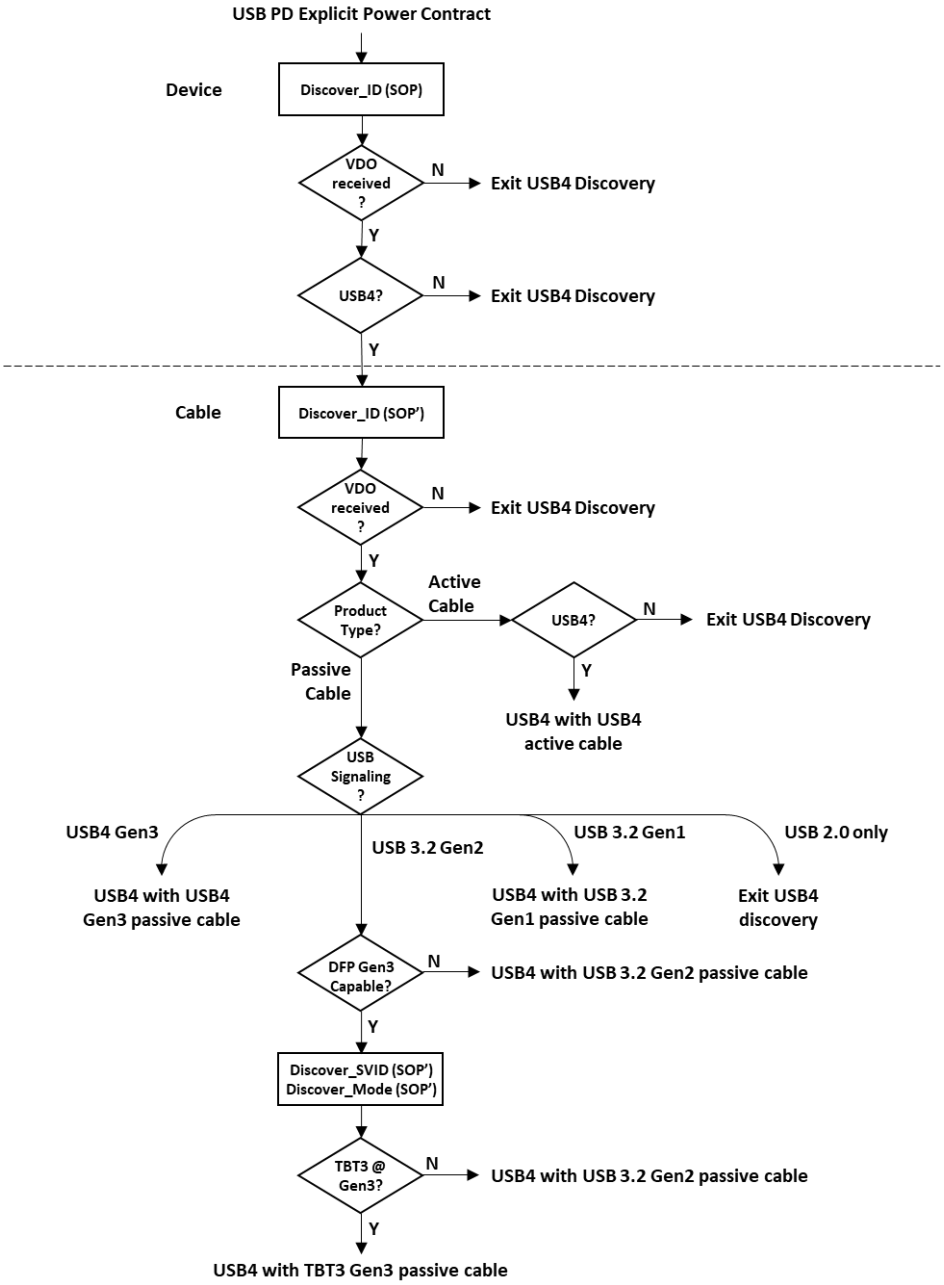
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

端口是 DRP 并作为源出现，此时需要 DR_Swap 将正确的数据角色传输到集线器），并且 DFP 应为 VCONN 的源。

5.4.3 USB4 发现和进入流程

图 5-1 说明了 *USB4* 发现和进入的基本流程模型。

图 5-1 USB4 发现和进入流程模型



5.4.3.1 USB4 设备发现 (SOP)

仅在协商 *USB PD* 明确合同后才能进行 *USB4* 设备发现。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

USB4 device discovery involves the use of the USB PD Discover ID process between the DFP and its port partner (SOP).

5.4.3.2 USB4 Cable Discovery (SOP')

The DFP shall determine that the attached cable is USB4-compatible prior to entering into USB4 operation. In cases where the USB4 device is directly connected or has a captive cable, the USB4 device shall respond to USB4 cable discovery on SOP' as a captive passive cable and indicating the appropriate USB Signaling support.

Table 5-1 summarizes the list of cables that are intended to support USB4-compatible operation. Regarding Active Cables, this list does not include Optically-Isolated Active Cables (OIACs) which are are to be handled as a special case given that these cables do not support USB 2.0 and power delivery over the cable (See Chapter 6).

Table 5-1 Certified Cables Where USB4-compatible Operation is Expected

	Cable Signaling	USB4 Operation	Notes
USB Type-C Full-Featured Cables (Passive)	USB 3.2 Gen1	20 Gbps	This cable will indicate support for USB 3.2 Gen1 (001b) in the USB Signaling field of its Passive Cable VDO response. Note: even though this cable isn't explicitly tested, certified or logo'ed for USB 3.2 Gen2 operation, USB4 Gen2 operation will generally work.
	USB 3.2 Gen2 (USB4 Gen2)	20 Gbps	This cable will indicate support for USB 3.2 Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response.
	USB4 Gen3	40 Gbps	This cable will indicate support for USB4 Gen3 (011b) in the USB Signaling field of its Passive Cable VDO response.
Thunderbolt™ 3 Cables (Passive)	TBT3 Gen2	20 Gbps	This cable will indicate support for USB 3.2 Gen1 (001b) or USB 3.2 Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response.
	TBT3 Gen3	40 Gbps	In addition to indicating support for USB 3.2 Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response, this cable will indicate that it supports TBT3 Gen3 in the Discover Mode VDO response.
USB Type-C Full-Featured Cables (Active)[1]	USB4 Gen2	20 Gbps	This cable will indicate support for USB4 Gen2 (010b) in the USB Signaling field of its Active Cable VDO response.
	USB4 Gen3	40 Gbps	This cable will indicate support for USB4 Gen3 (011b) in the USB Signaling field of its Active Cable VDO response.

Note:

1. SuperSpeed USB active cables do not support USB4–compatible operation.

Determining if the cable is USB4-compatible starts the use of the USB PD Discover ID process between the DFP and the attached cable (SOP'). If no response is received when the DFP issues a USB PD Discover ID command to the cable, then the USB4 discovery process shall be

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

*USB4*设备发现涉及在 DFP 和其端口伙伴（SOP）之间使用 *USB PD* 发现 ID 过程。

5.4.3.2 USB4 电缆发现 (SOP ’)

DFP 应在进入 *USB4* 操作之前确定所连接的电缆是否兼容 *USB4*。如果 *USB4* 设备直接连接或具有固定电缆，则 *USB4* 设备应在 SOP ’ 上将 *USB4* 电缆发现响应为固定无源电缆，并指示适当的 USB 信号支持。

表 5-1 总结了旨在支持 *USB4* 兼容操作的电缆列表。关于有源电缆，此列表不包括光学隔离有源电缆 (OIAC)，这些电缆将作为特殊情况处理，因为这些电缆不支持 *USB 2.0* 和通过电缆传输电力（请参阅第 6 章）。

表 5-1 经过认证的可兼容 USB4 的线缆

	Cable Signaling	USB4 Operation	Notes
USB Type-C Full-Featured Cables (Passive)	*USB 3.2* Gen1	20 Gbps	This cable will indicate support for *USB 3.2* Gen1 (001b) in the USB Signaling field of its Passive Cable VDO response. Note: even though this cable isn’t explicitly tested, certified or logo’ed for *USB 3.2* Gen2 operation, *USB4* Gen2 operation will generally work.
	USB 3.2 Gen2 (*USB4* Gen2)	20 Gbps	This cable will indicate support for *USB 3.2* Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response.
	USB4 Gen3	40 Gbps	This cable will indicate support for *USB4* Gen3 (011b) in the USB Signaling field of its Passive Cable VDO response.
Thunderbolt™ 3 Cables (Passive)	TBT3 Gen2	20 Gbps	This cable will indicate support for *USB 3.2* Gen1 (001b) or *USB 3.2* Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response.
	TBT3 Gen3	40 Gbps	In addition to indicating support for *USB 3.2* Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response, this cable will indicate that it supports TBT3 Gen3 in the Discover Mode VDO response.
USB Type-C Full-Featured Cables (Active)[1]	*USB4* Gen2	20 Gbps	This cable will indicate support for *USB4* Gen2 (010b) in the USB Signaling field of its Active Cable VDO response.
	USB4 Gen3	40 Gbps	This cable will indicate support for *USB4* Gen3 (011b) in the USB Signaling field of its Active Cable VDO response.

笔记：

1. SuperSpeed USB 有源电缆不支持 *USB4* 兼容操作。

确定电缆是否兼容 *USB4* 开始使用 DFP 和所连接电缆 (SOP ’) 之间的 *USB PD* Discover ID 过程。如果 DFP 向电缆发出 *USB PD* Discover ID 命令时未收到任何响应，则应执行 *USB4* 发现过程

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

exited and the DFP shall proceed to establish a functional connection to its UFP port partner following traditional *USB 2.0* process.

USB4-compatible support is generally determined based on the USB Signaling Support indicated in the cable VDO responses appropriate for the type of cable it is, passive or active, with compatible passive cables being those that indicate USB signaling support for Gen1 or higher and with compatible active cables being those that indicate USB signaling support for Gen2 or higher.

When a passive cable is identified as a *USB 3.2* Gen2 cable and the DFP is Gen3 capable, the DFP needs to check further using *USB PD* Alternate Mode process to determine if the cable is a Thunderbolt 3 passive cable supporting Gen3.

Some existing Thunderbolt 3 active cables may support *USB4* operation, such cables will indicate that it supports rounded data rates in the Discover Mode VDO response – discovery and use of this cable is optional.

5.4.3.2.1 Discovering Passive Cables

The *USB PD* specification defines the Passive Cable VDO responses to the Discover Identity Command sent by the DFP to a *USB4*-compatible passive cable.

If the USB Signaling field [B2…0] in the Passive Cable VDO response is 011b (*USB4* Gen3), the *USB4* discovery process is complete and *USB4* operation up to as high as 40 Gbps is supported. In Chapter 3 of this specification, these cable assemblies are those with the following cable references: CC4G3-3 and CC4G3-5 indicated in Table 3-1.

If the USB Signaling field [B2…0] in the Passive Cable VDO response is 000b (*USB 2.0* only), the the *USB4* discovery process will be exited and the DFP shall proceed to establish a functional connection to its UFP port partner following traditional USB 2.0 process.

If the USB Signaling field [B2…0] in the Passive Cable VDO response is either 010b (*USB 3.2* Gen2) or 001b (*USB 3.2* Gen1), the *USB4* discovery process is complete if the DFP is limited to *USB4* Gen2. In Chapter 3 of this specification, these cable assemblies are those with the following cable references: CC3G2-3, CC3G2-5, CC3G1-3, and CC3G1-3 indicated in Table 3-1. Note that *USB 3.2* Gen1 cables, while not tested and certified to be used for *USB 3.2* Gen2 operation, are expected to work for *USB4* Gen2 operation.

If the USB Signaling field [B2…0] in the Passive Cable VDO response is 010b (*USB 3.2* Gen2) but the DFP is capable of *USB4* Gen3 operation, then the DFP shall use the *USB PD* Alternate Mode process to determine if the cable also can be identified as a TBT3 Gen3 cable. Refer to Section 5.4.3.2.3 for TBT3 cable discovery process. If the Cable Speed field of the Discover Modes VDO response is set to 011b, then the *USB4* discovery process is complete and *USB4* operation up to as high as Gen3 is supported using the TBT3 passive cable (see Table F-11).

5.4.3.2.2 Discovering Active Cables

The *USB PD* specification defines the Active Cable VDO responses to the Discover Identity Command sent by the DFP to a *USB4*-compatible active cable.

If the USB Signaling Support field [B2…0] in the Active Cable VDO 1 response is 011b (USB4 Gen3), the *USB4* discovery process is complete and *USB4* operation up to as high as Gen3 is supported.

Optionally, discovery and use of existing TBT3 active cables that indicate support for rounded data rate operation is allowed if the active cable isn't explicitly identified as *USB4*-compatible.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

退出，并且 DFP 将按照传统的 *USB 2.0* 流程继续与其 UFP 端口伙伴建立功能连接。

USB4 兼容支持通常根据电缆 VDO 响应中指示的适用于其类型（无源或有源）的 USB 信号支持来确定，
其中兼容的无源线缆表示支持 Gen1 或更高版本的 USB 信号，而兼容的有源线缆表示支持 Gen2 或更高版本的 USB 信号。

当无源电缆被识别为 *USB 3.2* Gen2 电缆且 DFP 支持 Gen3 时，DFP 需要使用 *USB PD* 备用模式流程进一步检查，以确定该电缆是否为支持 Gen3 的 Thunderbolt 3 无源电缆。

一些现有的 Thunderbolt 3 有源线缆可能支持 *USB4* 操作，此类线缆将表明它支持发现模式 VDO 响应中的舍入数据速率——发现和使用此线缆是可选的。

5.4.3.2.1 发现无源电缆

USB PD 规范定义了无源电缆 VDO 对 DFP 发送到 *USB4* 兼容无源电缆的发现身份命令的响应。

如果无源电缆 VDO 响应中的 USB 信号字段 [B2…0] 为 011b（*USB4* Gen3），则 *USB4* 发现过程已完成，并且支持高达 40 Gbps 的 *USB4* 操作。在本规范的第 3 章中，这些电缆组件是具有以下电缆参考的电缆组件：表 3-1 中所示的 CC4G3-3 和 CC4G3-5。

如果无源电缆 VDO 响应中的 USB 信令字段 [B2…0] 为 000b（仅限 *USB 2.0*），则将退出 *USB4* 发现过程，并且 DFP 应按照传统 USB 2.0 过程继续与其 UFP 端口伙伴建立功能连接。

如果无源电缆 VDO 响应中的 USB 信号字段 [B2…0] 为 010b (*USB 3.2* Gen2) 或 001b (*USB 3.2* Gen1)，则如果 DFP 限制为 *USB4* Gen2，则 *USB4* 发现过程完成。在本规范的第 3 章中，这些电缆组件是具有以下电缆参考的电缆组件：表 3-1 中所示的 CC3G2-3、CC3G2-5、CC3G1-3 和 CC3G1-3。

请注意，虽然 *USB 3.2* Gen1 电缆尚未经过测试和认证可用于 *USB 3.2* Gen2 操作，但预计可以用于 *USB4* Gen2 操作。

如果无源电缆 VDO 响应中的 USB 信号字段 [B2…0] 为 010b（*USB 3.2* Gen2），但 DFP 能够进行 *USB4* Gen3 操作，则 DFP 应使用 *USB PD* 备用模式过程来确定电缆是否也可以识别为 TBT3 Gen3 电缆。有关 TBT3 电缆发现过程，请参阅第 5.4.3.2.3 节。如果发现模式 VDO 响应的电缆速度字段设置为 011b，则 *USB4* 发现过程已完成，并且使用 TBT3 无源电缆支持高达 Gen3 的 *USB4* 操作（参见表 F-11）。

5.4.3.2.2 发现活动电缆

USB PD 规范定义了有源电缆 VDO 对 DFP 发送到 *USB4* 兼容有源电缆的发现身份命令的响应。

如果有源电缆 VDO 1 响应中的 USB 信令支持字段 [B2…0] 为 011b（USB4 Gen3），则 *USB4* 发现过程已完成，并且支持最高至 Gen3 的 *USB4* 操作。

或者，如果没有明确标识为与 *USB4* 兼容，则允许发现和使用表明支持整数数据速率操作的现有 TBT3 有源电缆。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Failure to identify that the attached active cable is *USB4*-compatible will result in exiting the *USB4* discovery process and reverting to following traditional *USB 3.2* and *USB 2.0* process.

5.4.3.2.3 Process for Discovering Thunderbolt 3 Cables

The *USB PD* specification defines the process for discovering Alternate Mode-enabled cables. The following summarizes this process specific to discovering Thunderbolt 3 cables for purposes of determining *USB4*-compatibility. Prior to performing these steps, the *USB PD* Discover Identity process will have already been used to establish if the cable is passive or active.

The following steps are used for discovering Thunderbolt 3 cables and the cable's capabilities using the *USB PD* Alternate Mode process.

1. DFP issues the Discover SVIDs command to the cable SOP'.
2. If the cable's Discover SVID response indicates 0x8087 (Intel/TBT3) as one of its SVIDs, then proceed to next step, otherwise the cable is not a Thunderbolt 3 cable (see Section F.2.4).
3. DFP issues the Discover Modes command with its SVID set to 0x8087 to the cable's SOP'.
4. If this discovery is part of the *USB4*-compatible passive cable discovery process, from the cable's Discover Modes VDO responses (see Section F.2.6), extract the value in the Cable Speed field to complete the process.
5. If this discovery is part of the *USB4*-compatible active cable discovery process, from the cable's Discover Modes VDO responses (see Section F.2.6), extract the value in the TBT_Rounded_Support field to complete the process. [Note: discovery and use of *USB4*-compatible TBT3 active cables is an optional feature that also would require use of *USB PD* Enter Mode command to enable the cable for *USB4* operation.]

5.4.3.3 USB4 Operational Entry

USB4 operational entry shall occur only after having established that the attached cable, if present, and the port partner are *USB4*-capable.

USB4 operational entry involves the use of the *USB PD* Enter_USB Message process between the DFP and both the attached *USB4*-compatible cable and the *USB4*-capable port partner – sending this message is order specific: SOP' first, SOP" second if present, and SOP third.

When using the *USB PD* Enter_USB Message for enabling *USB4* operation, the DFP shall indicate 010b (*USB4*) in the USB Mode field of the Enter_USB Data Object. The remaining fields shall be set appropriately by the DFP based on the capabilities of the DFP and attached cable.

5.4.4 USB4 Post-Entry Operation

5.4.4.1 During USB4 Operation

While in *USB4* operation, the following are allowed:

- The *USB PD* explicit power contract may be re-negotiated.
- Issue an *USB PD* Data_Reset command to change the mode of operation, e.g. from *USB4* to *USB 3.2* or an Alternate Mode.
- Enable Alternate Modes that do not reconfigure the port interface and operate in parallel with *USB4*.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

如果无法确定所连接的活动电缆是否与 *USB4* 兼容，将导致退出 *USB4* 发现过程并恢复到遵循传统的 *USB 3.2* 和 *USB 2.0* 过程。

5.4.3.2.3 发现 Thunderbolt 3 线缆的过程

USB PD 规范定义了发现启用备用模式的电缆的过程。
以下总结了用于确定 *USB4* 兼容性的特定于发现 Thunderbolt 3 电缆的过程。在执行这些步骤之前，*USB PD* 发现身份过程将已用于确定电缆是被动的还是主动的。

以下步骤用于使用 *USB PD* 备用模式过程发现 Thunderbolt 3 电缆及其功能。

1. DFP 向线缆 SOP ’ 发出 Discover SVIDs 命令。 2. 如果线缆的 Discover SVID 响应指示 0x8087（Intel/TBT3）是其 SVID 之一，则继续下一步，否则该线缆不是 Thunderbolt 3 线缆（请参阅第 F.2.4 节）。 3. DFP 向线缆的 SOP ’ 发出 Discover Modes 命令，其 SVID 设置为 0x8087。 4. 如果此发现是兼容 *USB4* 的被动线缆发现过程的一部分，则从线缆的 Discover Modes VDO 响应（请参阅第 F.2.6 节）中提取 Cable Speed 字段中的值以完成该过程。 5. 如果此发现是兼容 *USB4* 的主动线缆发现过程的一部分，则从线缆的 Discover Modes VDO 响应（请参阅第 F.2.6 节）中提取 TBT_Rounded_Support 字段中的值以完成该过程。[注：发现和使用

与 *USB4* 兼容的 TBT3 有源电缆是一项可选功能，它还需要使用 *USB PD* 进入模式命令来启用电缆进行 *USB4* 操作。]

5.4.3.3 USB4操作入口

仅当确定所连接的电缆（如果存在）和端口伙伴具备 *USB4* 功能后，才能进入 *USB4* 操作状态。

USB4 操作进入涉及使用 DFP 和所连接的 *USB4* 兼容电缆以及 *USB4* 兼容端口伙伴之间的 *USB PD* Enter_USB 消息过程 - 发送此消息是特定顺序的：首先发送 SOP ’，如果存在则发送 SOP ”，然后发送 SOP 。

当使用 *USB PD* Enter_USB 消息启用 *USB4* 操作时，DFP 应在 Enter_USB 数据对象的 USB 模式字段中指示 010b (*USB4*)。其余字段应由 DFP 根据 DFP 和所连接电缆的功能进行适当设置。

5.4.4 USB4 进入后操作

5.4.4.1 USB4 操作期间

在 *USB4* 操作中，允许以下操作：

- 可以重新协商 *USB PD* 显式电源合同。
- 发出 *USB PD* Data_Reset 命令来更改操作模式，例如从 *USB4* 更改为 *USB 3.2* 或备用模式。
- 启用不重新配置端口接口并与 *USB4* 并行运行的备用模式。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

5.4.4.2 Exiting USB4 Operation

The *USB PD* Data_Reset process causes USB data connections to be reset and Alternate Modes to be exited. This process does not change the existing power contract and data roles between the port partners. The Data_Reset process shall include the following steps:

- Issue a *USB PD* Data_Reset command to the SOP port partner to reset the data bus, reset the cable, and exit any Alternate Modes while preserving the power on VBUS.
- The tUSB4Timeout and tAMETimeout timers within the UFP shall be reset upon sending or receiving a *USB PD* Data_Reset command.
- Re-enter the *USB4* Discovery and Entry process (Section 5.4.3).

5.5 USB4 Hub Connection Requirements

USB4 hub behavior with regard to managing its DFP connections has *USB4*-specific dependencies on the connection status and capabilities of its single UFP. Additionally, hubs have *USB4*-specific responsibilities for communicating the capabilities of the *USB4* host to downstream-connected *USB4* hubs. This section provides both requirements and guidance for *USB4* hub port connection behavior.

5.5.1 USB4 Hub Port Initial Connection Requirements

The following requirements apply to all hub ports.

1. Run the USB Type-C Connection process,
2. Establish an initial *USB PD* explicit contract,
3. If desired, use PR_Swap to establish the preferred power role, and
4. Use DR_Swap to establish data role to be consistent with the port's position in the USB tree if needed.

5.5.2 USB4 Hub UFP and Host Capabilities Discovery

The *USB4* hub DFPs capabilities are ultimately based on the capabilities seen at its UFP (once it has established a connection to the host). If the *USB4* hub's UFP is connected to an upstream *USB4* hub, then the capabilities over the connection between the two hubs may not initially represent the capabilities all the way back to the host.

The following summarizes the general principles regarding how UFP and host capabilities impact DFP connections.

- The downstream connection to a device or hub that is attached to the *USB4* hub's DFP is based on the capabilities of the hub.
- Once the *USB4* hub's UFP has established a connection, the hub's capabilities are limited to the capabilities of that UFP connection.
- When the *USB4* hub's UFP connection indicates that a host is not present, once the hub is notified that a host becomes present, the hub will limit its capabilities as needed to match those of the host.
    - Any connections on the *USB4* hub's DFPs that existed prior to the host being present are adjusted to align with changes in capabilities if needed.
- Once a host becomes present in a *USB4* tree, all intermediary hubs will update their connections to align with the host capabilities as the host present status is propagated to the downstream connected *USB4* hubs.

The capabilities seen by the hub's UFP are based on one of the following:

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

5.4.4.2 退出USB4操作

USB PD Data_Reset 过程会导致 USB 数据连接重置并退出备用模式。此过程不会改变端口伙伴之间现有的电源合同和数据角色。Data_Reset 过程应包括以下步骤：

- 向 SOP 端口伙伴发出 *USB PD* Data_Reset 命令以重置数据总线、重置电缆并退出任何备用模式，同时保持 VBUS 上的电源。• 发送或接收 *USB PD* Data_Reset 命令时，UFP 内的 tUSB4Timeout 和 tAMETimeout 计时器应重置。• 重新进入 *USB4* 发现和进入过程（第 5.4.3 节）。

5.5 USB4 集线器连接要求

USB4 集线器在管理其 DFP 连接方面的行为对其单个 UFP 的连接状态和功能具有 *USB4* 特定的依赖性。此外，集线器还具有 *USB4* 特定的职责，用于将 *USB4* 主机的功能传达给下游连接的 *USB4* 集线器。本节提供了 *USB4* 集线器端口连接行为的要求和指导。

5.5.1 USB4 集线器端口初始连接要求

以下要求适用于所有枢纽港口。

1. 运行 USB Type-C 连接过程，
2. 建立初始 *USB PD* 显式契约，3. 如果需要，使用 PR_Swap 建立首选电源角色，4. 如果需要，使用 DR_Swap 建立数据角色以与端口在 USB 树中的位置保持一致。

5.5.2 USB4 集线器 UFP 和主机功能发现

USB4 集线器 DFP 的功能最终取决于其 UFP 上显示的功能（一旦它与主机建立连接）。如果 *USB4* 集线器的 UFP 连接到上游 *USB4* 集线器，则两个集线器之间的连接功能最初可能并不代表一直返回到主机的功能。

以下总结了 UFP 和主机功能如何影响 DFP 连接的一般原则。

- 连接到 *USB4* 集线器的 DFP 的设备或集线器的下游连接基于集线器的功能。• 一旦 *USB4* 集线器的 UFP 建立了连接，集线器的功能将仅限于该 UFP 连接的功能。• 当 *USB4* 集线器的 UFP 连接指示主机不存在时，一旦集线器收到主机存在的通知，集线器将根据需要限制其功能以匹配主机的功能。o 在主机被连接到 *USB4* 集线器的 DFP 之前存在的任何连接

  如果需要，当前的状态会被调整以适应功能的变化。• 一旦主机出现在 *USB4* 树中，所有中间集线器都会更新它们的连接以与主机功能保持一致，因为主机的当前状态会传播到下游连接的 *USB4* 集线器。

能力　集线器的 UFP 所看到的功能基于以下之一　以下：

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- An *USB PD* Enter_USB message is received which indicates the USB operation (*USB4*, *USB 3.2* or *USB 2.0*) and associated characteristics supported (*USB4* PCIe-supported, *USB4* DP supported, etc.) by the upstream port partner.
- An *USB PD* Enter Mode command is received to start a supported Alternate Mode (Thunderbolt 3, DisplayPort).
- No *USB PD* Enter_USB message is received within the tUSB4Timeout or *USB PD* Enter Mode message is received within the tAMETimeout indicating only *USB 3.2* and *USB 2.0* are available.

If the *USB4* hub's UFP is connected to an upstream *USB4* hub, then the capabilities reported in the received *USB PD* Enter_USB message shall only be considered the host's capabilities if the Host Present bit is set. If the Host Present bit is reset, then the hub shall wait for a subsequent *USB PD* Enter_USB message to be received with the Host Present bit set. Once the Host Present bit is set, the capabilities as represented in the *USB PD* Enter_USB message can be used as the host's capabilities for the purpose of establishing final DFP connections.

If the *USB4* hub's UFP receives an *USB PD* Enter_USB message which indicates the USB operation as either *USB 3.2* or *USB 2.0*, the *USB4* hub shall not wait for the completion of the tUSB4Timeout before proceeding to establish its UFP and DFP connections following *USB 3.2* or *USB 2.0* hub requirements, respectively.

5.5.3 Hub DFP Connection Requirements

5.5.3.1 Speculative Connections

When a device is attached to the DFP of a *USB4* hub prior to the hub's UFP being connected and the host capabilities are known, the hub will speculatively connect to the attached device based on the following requirements.

- Use *USB PD* Discover ID and the *USB PD* Alternate Mode process to determine the full capabilities of the attached cable and device.
- Based on the discovered capabilities, establish the most capable connection based on the capabilities of the *USB4* hub's DFP in the following priority order:
    1. *USB4*
    2. Thunderbolt 3 Alt Mode
    3. DP Alt Mode
    4. *USB 3.2*
    5. *USB 2.0*
- Inhibit port status notifications and data paths upstream from the *USB4* hub's DFPs while waiting for the *USB4* hub's UFP connection to be established.

5.5.3.2 Operational Connections

Once the *USB4* hub's UFP connection is established and the host capabilities are determined (see Section 5.5.2), the hub shall evaluate each existing DFP connection based on the capabilities associated with the hub's UFP connection and perform one of the following actions.

- If the DFP connection properly aligns with the capabilities of the UFP connection, enable the status notifications and data path for that port.
- If the DFP connection does not properly align with the capabilities of the UFP connection, the DFP connection shall do one of the following:

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• 收到 *USB PD* Enter_USB 消息，表示 USB 操作（*USB4*、*USB 3.2* 或 *USB 2.0*）及其上游端口伙伴支持的相关特性（*USB4* PCIe 支持、*USB4* DP 支持等）。• 收到 *USB PD* Enter Mode 命令以启动支持的备用模式（Thunderbolt 3、DisplayPort）。• 在 tUSB4Timeout 或 *USB PD* Enter 时间内未收到 *USB PD* Enter_USB 消息

在 tAMETimeout 内收到模式消息，表明只有 *USB 3.2* 和 *USB 2.0* 可用。

如果 *USB4* 集线器的 UFP 连接到上游 *USB4* 集线器，则只有在设置了 Host Present 位的情况下，接收到的 *USB PD* Enter_USB 消息中报告的功能才应被视为主机的功能。如果重置了 Host Present 位，则集线器应等待接收设置了 Host Present 位的后续 *USB PD* Enter_USB 消息。设置 Host Present 位后，*USB PD* Enter_USB 消息中所表示的功能可用作主机的功能，以建立最终的 DFP 连接。

如果 *USB4* 集线器的 UFP 收到 *USB PD* Enter_USB 消息，指示 USB 操作为 *USB 3.2* 或 *USB 2.0*，则 *USB4* 集线器不应等待 tUSB4Timeout 完成，而应分别按照 *USB 3.2* 或 *USB 2.0* 集线器要求建立其 UFP 和 DFP 连接。

5.5.3 集线器 DFP 连接要求

5.5.3.1 推测连接

当设备在集线器的 UFP 连接之前连接到 *USB4* 集线器的 DFP 并且主机功能已知时，集线器将根据以下要求推测性地连接到所连接的设备。

• 使用 *USB PD* 发现 ID 和 *USB PD* 备用模式过程来确定所连接电缆和设备的全部功能。• 根据发现的功能，按照以下优先顺序根据 *USB4* 集线器的 DFP 功能建立功能最强的连接：1. *USB4* 2. Thunderbolt 3 备用模式 3. DP 备用模式 4. *USB 3.2* 5. *USB 2.0*

• 在等待 *USB4* 集线器的 UFP 连接建立时，抑制来自 *USB4* 集线器的 DFP 的端口状态通知和数据路径上行。

5.5.3.2 操作连接

一旦建立了 *USB4* 集线器的 UFP 连接并确定了主机功能（参见第 5.5.2 节），集线器应根据与集线器的 UFP 连接相关的功能评估每个现有的 DFP 连接，并执行以下操作之一。

• 如果 DFP 连接与 UFP 连接的功能完全一致，则启用该端口的状态通知和数据路径。• 如果 DFP 连接与 UFP 连接的功能不完全一致，则 DFP 连接应执行以下操作之一：

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- If the UFP remains in *USB4* and the DFP connection is with a downstream *USB4* hub, send a revised *USB PD* Enter_USB message with the Host Present bit set.
- If the UFP changed to *USB 3.2* or *USB 2.0* and the DFP connection is with a downstream *USB4* hub, the DFP shall be reset the connection using *USB PD* Data_Reset followed by sending a revised *USB PD* Enter_USB message indicating *USB 3.2* or *USB 2.0* and the Host Present bit set.
- Otherwise, the DFP shall enter the ErrorRecovery state to reset the connection and establish a new connection that aligns with the hub's UFP capabilities.

5.5.4 Hub Ports Connection Behavior Flow Model

This section illustrates a number of connection flows that assume that the hub's DFP connection is established prior to the hub's UFP connection. In these cases, the host capabilities are unknown at the time that the hub's DFP is connecting with the attached device. Given this, the initial connection established by the hub's DFP is speculatively based only on the hub and device's capabilities and may have to be revised once the host capabilities are known if there is a functional mismatch. When the hub's UFP connection is fully established prior to devices appearing on the hub's DFP, the connection can be established with full knowledge of the host's capabilities – flows associated with this relationship are not illustrated.

For the illustrated flows in this section, the Source/Sink power roles remain as initially resolved by the CC connection state machine with no PR_Swap or DR_Swap activity.

All of the flows intend to minimize the total connection time for enabling the functionality of the device connected to the hub's DFP. This is accomplished by establishing the highest functional connection based on mutual capabilities between the hub and the device even as the hub's UFP capabilities are unknown or not ready for operation. If the speculatively established connection turns out to be valid once the hub's UFP capabilities are established, then the DFP's connection will be enabled as is. If the speculatively established connection turns out to be invalid, the DFP connection shall be reset and a connection that aligns with the hub's UFP capabilities shall be established.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

o 如果 UFP 保持在 *USB4* 并且 DFP 连接与下游 *USB4* 集线器，则发送修改后的 *USB PD* Enter_USB 消息并设置 Host Present 位。o 如果 UFP 更改为 *USB 3.2* 或 *USB 2.0* 并且 DFP 连接与下游 *USB4* 集线器，则 DFP 应使用 *USB PD* Data_Reset 重置连接，然后发送修改后的 *USB PD* Enter_USB 消息（指示 *USB 3.2* 或 *USB 2.0* 并且设置了 Host Present 位）。o 否则，DFP 应进入 ErrorRecovery 状态以重置连接并建立与集线器的 UFP 功能一致的新连接。

5.5.4 集线器端口连接行为流模型

本节说明了许多连接流程，这些流程假设集线器的 DFP 连接先于集线器的 UFP 连接建立。在这些情况下，在集线器的 DFP 与所连接设备连接时，主机功能未知。鉴于此，集线器的 DFP 建立的初始连接仅基于集线器和设备的功能推测，如果存在功能不匹配，则在了解主机功能后可能需要修改。当集线器的 UFP 连接在设备出现在集线器的 DFP 上之前完全建立时，可以在完全了解主机功能的情况下建立连接 - 未说明与此关系相关的流程。

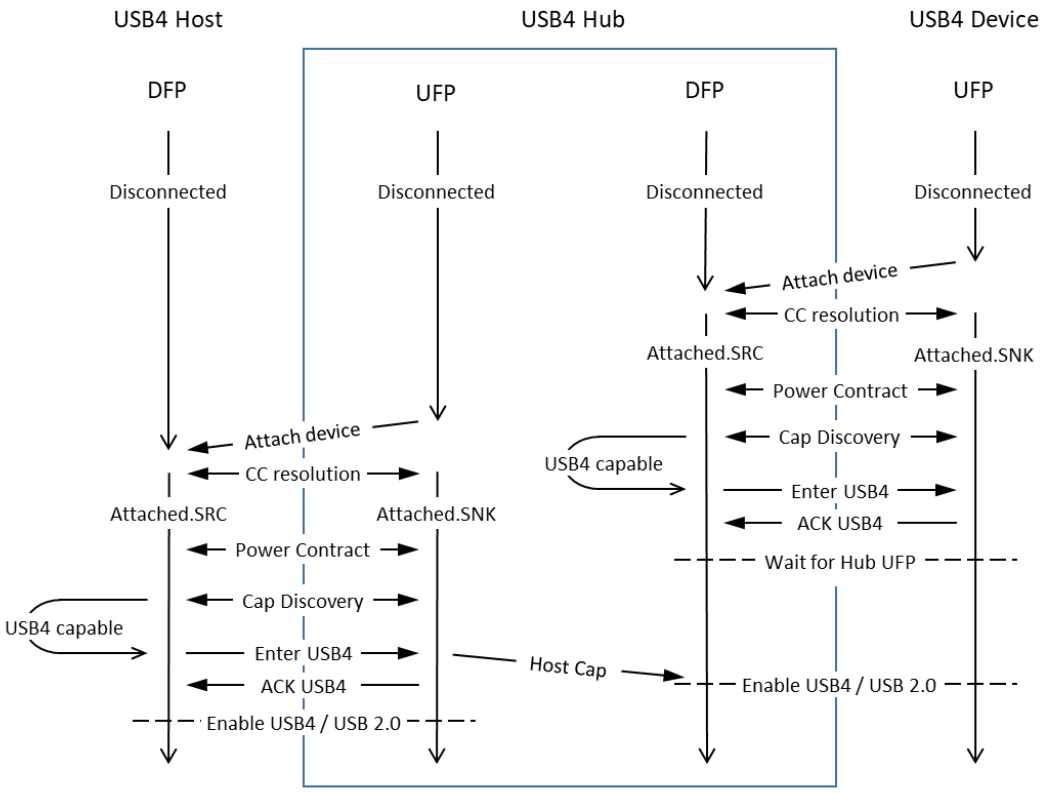
对于本节中所示的流程，源/接收器电源角色保持不变，由 CC 连接状态机最初解析，没有 PR_Swap 或 DR_Swap 活动。

所有流程都旨在最大限度地缩短启用连接到集线器的 DFP 的设备功能的总连接时间。这是通过基于集线器和设备之间的相互能力建立最高功能连接来实现的，即使集线器的 UFP 功能未知或尚未准备好运行。如果在集线器的 UFP 功能建立后推测建立的连接被证明是有效的，则 DFP 的连接将按原样启用。如果推测建立的连接被证明是无效的，则应重置 DFP 连接并建立与集线器的 UFP 功能一致的连接。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 5-2 Illustrates the connection flow model aligned across the combination of a *USB4* host, hub and device. The expected result is the successful enabling of end-to-end *USB4* operation.

Figure 5-2 USB4 Hub with USB4 Host and Device Connection Flow Alignment



In the illustrated flow, Cap Discovery includes all *USB PD* message exchanges needed between the DFP and its UFP port partner to discover the UFP's USB capabilities along with TBT3-compatibility and DP Alt Mode capabilities. For the *USB4* hub's DFP, Cap Discovery is done on a speculative basis whenever it does not already know of the capabilities of the host that will eventually be connected via the hub's UFP.

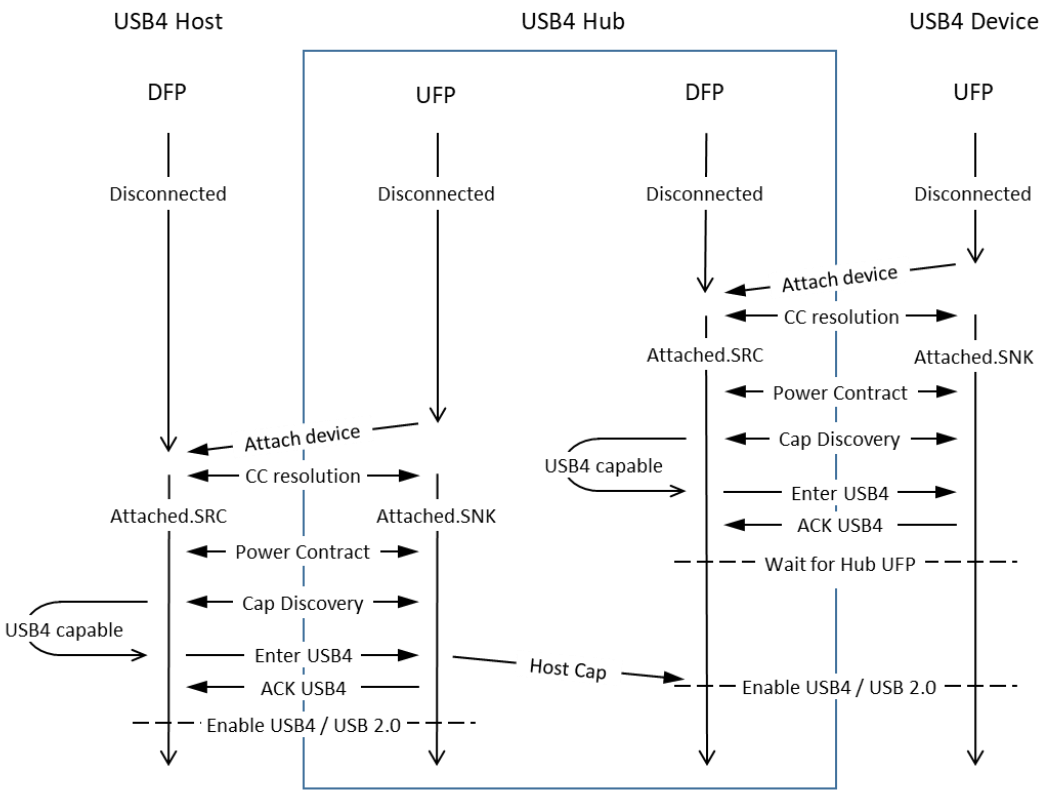
Upon completion of Cap Discovery between the hub's DFP and its UFP port partner, the hub DFP will establish the highest functional connection and then wait for the hub UFP to complete its connection. Once the hub's UFP connection is established, the host capabilities available is used to make a determination of what should be done to complete the hub DFP connection to the UFP port partner.

Host Cap is based on the resulting configuration (e.g. data bus protocol and speed) of the *USB4* Hub's UFP and the Host capabilities information received in the *USB PD* Enter_USB Message from its DFP port partner (see Section 5.5.2). The *USB4* hub uses Host Cap to set the available capabilities of the hub's DFPs.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 5-2 说明了跨 *USB4* 主机、集线器和设备组合的连接流模型。预期结果是成功启用端到端 *USB4* 操作。

图 5-2 USB4 集线器与 USB4 主机和设备连接流程对齐



在图示的流程中，Cap Discovery 包括 DFP 与其 UFP 端口伙伴之间所需的所有 *USB PD* 消息交换，以发现 UFP 的 USB 功能以及 TBT3 兼容性和 DP Alt Mode 功能。对于 *USB4* 集线器的 DFP，当 Cap Discovery 尚不知道最终将通过集线器的 UFP 连接的主机的功能时，Cap Discovery 会以推测的方式进行。

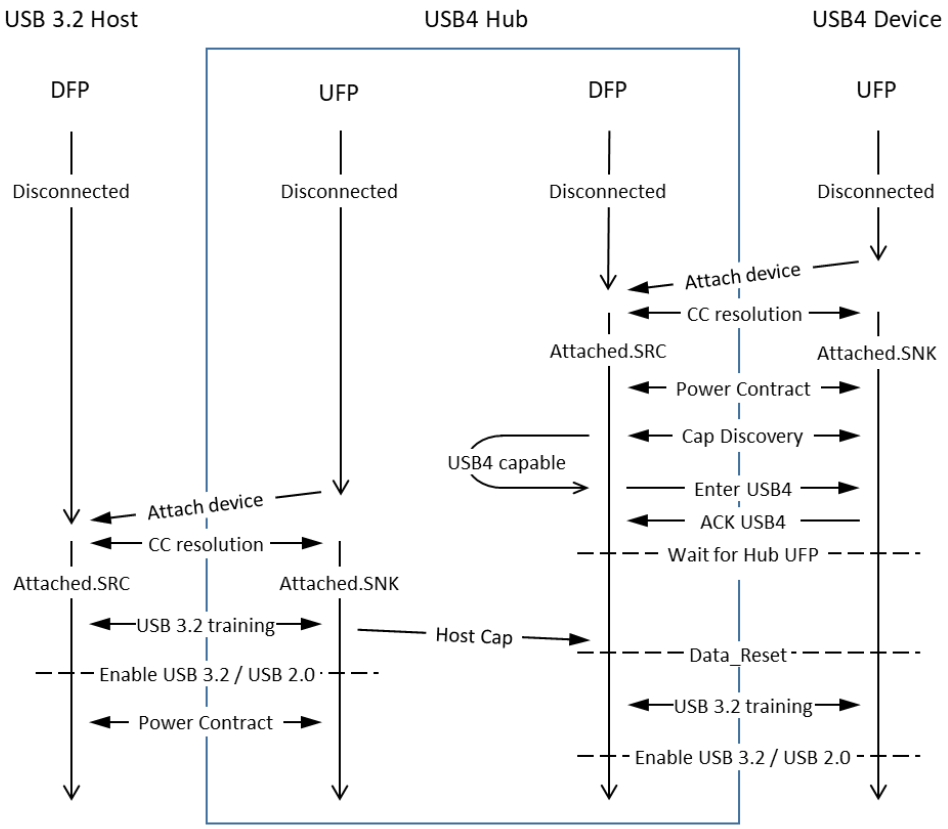
在集线器的 DFP 与其 UFP 端口伙伴之间的 Cap Discovery 完成后，集线器 DFP 将建立最高功能连接，然后等待集线器 UFP 完成其连接。一旦集线器的 UFP 连接建立，可用的主机功能将用于确定应执行哪些操作来完成集线器 DFP 与 UFP 端口伙伴的连接。

Host Cap 基于 *USB4* Hub 的 UFP 的结果配置（例如数据总线协议和速度）以及从其 DFP 端口伙伴收到的 *USB PD* Enter_USB 消息中的主机功能信息（参见第 5.5.2 节）。*USB4* hub 使用 Host Cap 来设置 hub 的 DFP 的可用功能。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 5-3 illustrates the connection flow model aligned across the combination of a *USB 3.2* host, a *USB4* hub and a *USB4* device.

Figure 5-3 USB4 Hub with USB 3.2 Host and USB4 Device Host Connection Flow Model

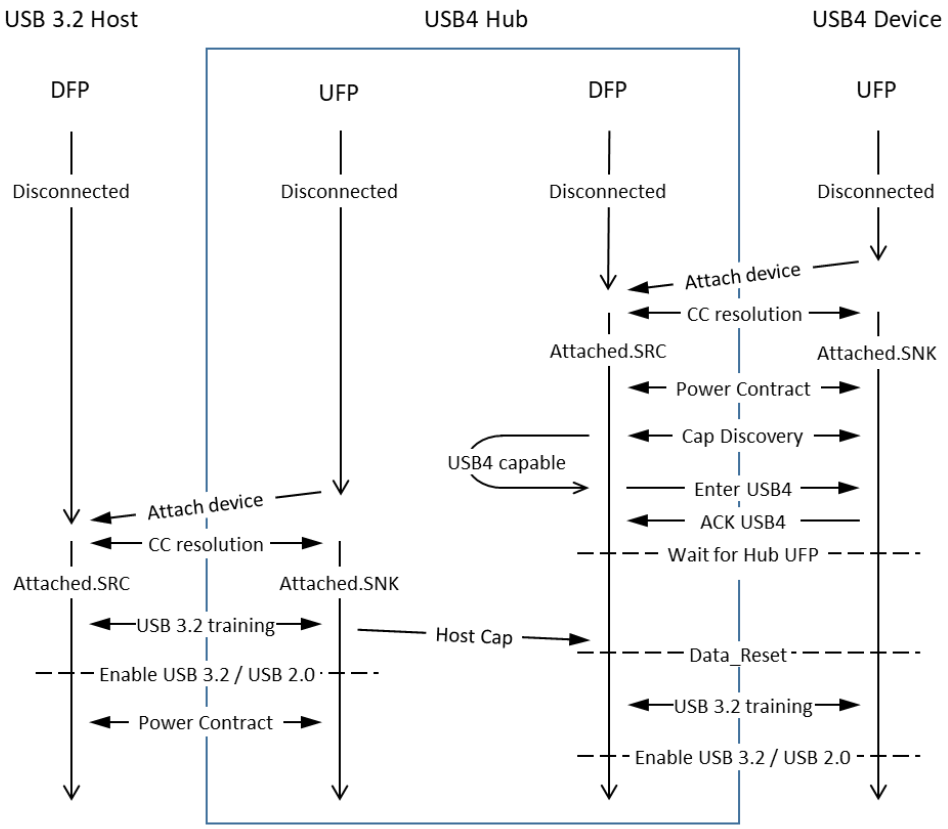


In the flow above, once connected to a *USB 3.2* host, the Host Cap reflects that the hub can only support *USB 3.2* on its DFPs and the speculatively established *USB4* connection on the DFP is exited with the *USB4* hub now operating as a traditional *USB 3.2* hub.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 5-3 说明了跨 *USB 3.2* 主机、*USB4* 集线器和 *USB4* 设备组合的连接流模型。

图 5-3 USB4 Hub 与 USB 3.2 Host 及 USB4 Device Host 连接流程模型

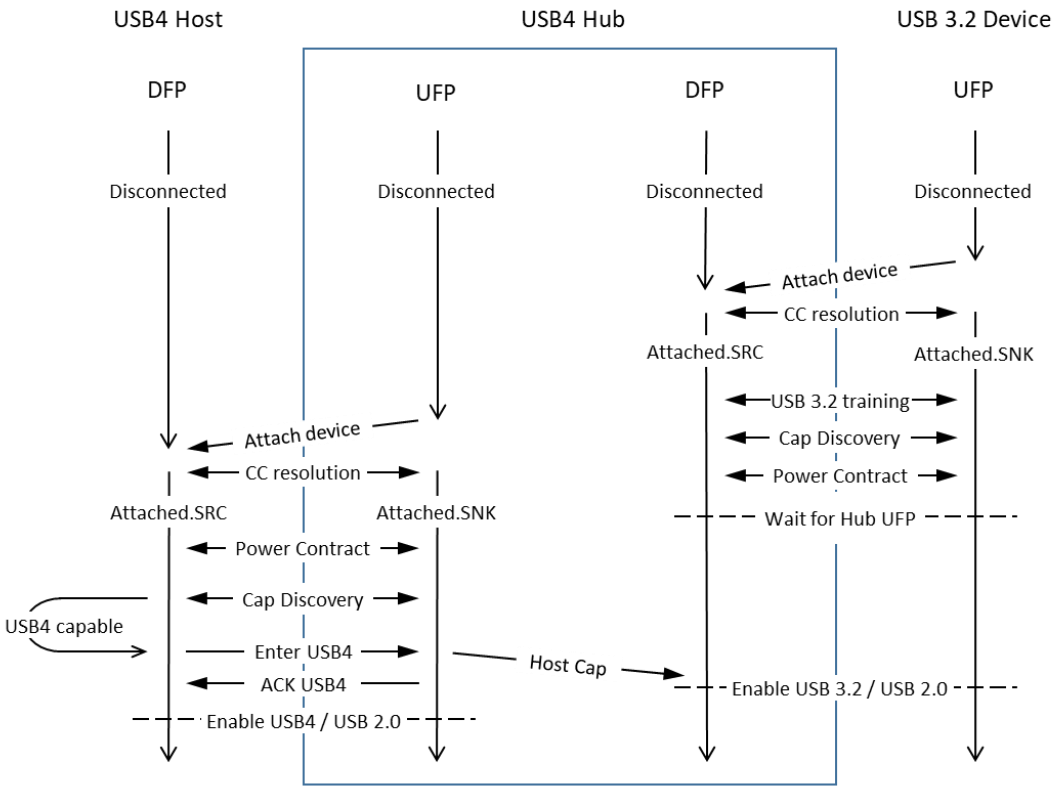


在上面的流程中，一旦连接到 *USB 3.2* 主机，主机容量就会反映出集线器只能在其 DFP 上支持 *USB 3.2*，并且在 DFP 上推测建立的 *USB4* 连接将退出，而 *USB4* 集线器现在作为传统的 *USB 3.2* 集线器运行。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 5-4 illustrates the connection flow model aligned across the combination of a *USB4* hub with a *USB4* host and *USB 3.2* device.

Figure 5-4 USB4 Hub with USB4 Host and USB 3.2 Device Connection Flow Model



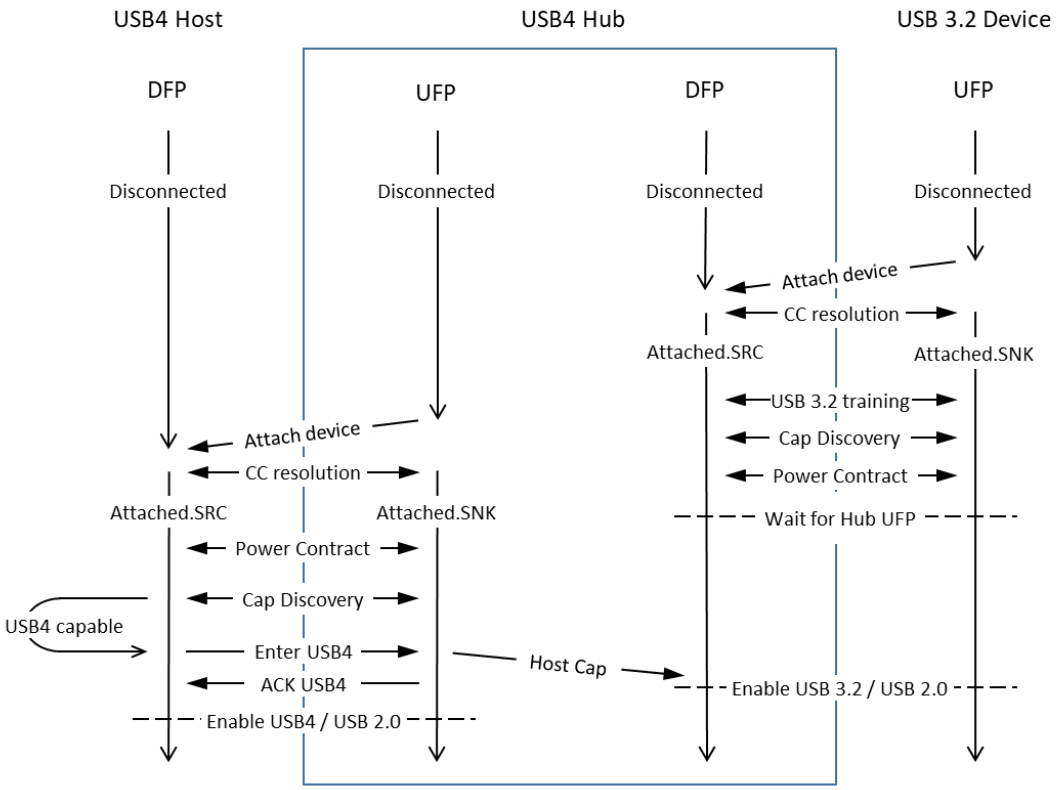
While *USB 3.2* devices won't necessarily respond to the Discover ID (SOP), the *USB4* hub's DFP will attempt to discover the capabilities of the attached device.

In the flow above, after the *USB4* connection of the hub's UFP is established, the DFP connection remains valid with the *USB 3.2* data path of the DFP being serviced by the *USB4* Enhanced SuperSpeed tunnel.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 5-4 说明了 *USB4* 集线器与 *USB4* 主机和 *USB 3.2* 设备组合之间的连接流模型。

图 5-4 USB4 Hub 与 USB4 Host 和 USB 3.2 Device 连接流程模型



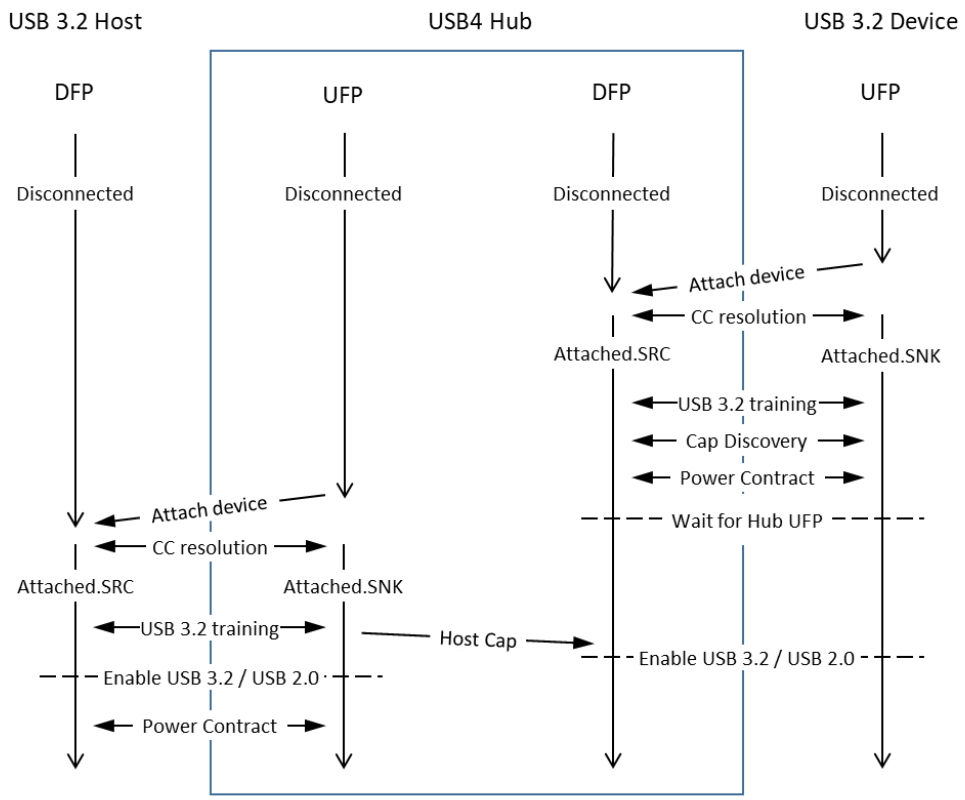
虽然 *USB 3.2* 设备不一定会响应发现 ID（SOP），但 *USB4* 集线器的 DFP 会尝试发现所连接设备的功能。

在上面的流程中，在建立集线器的 UFP 的 *USB4* 连接之后，DFP 连接仍然有效，并且 DFP 的 *USB 3.2* 数据路径由 *USB4* 增强型超高速隧道提供服务。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 5-5 illustrates the connection flow model aligned across the combination of a *USB4* hub with a *USB 3.2* host and device.

Figure 5-5 USB4 Hub with USB 3.2 Host and Device Connection Flow Model



While *USB 3.2* devices won't necessarily respond to the Discover ID (SOP), the *USB4* hub's DFP will attempt to discover the capabilities of the attached device.

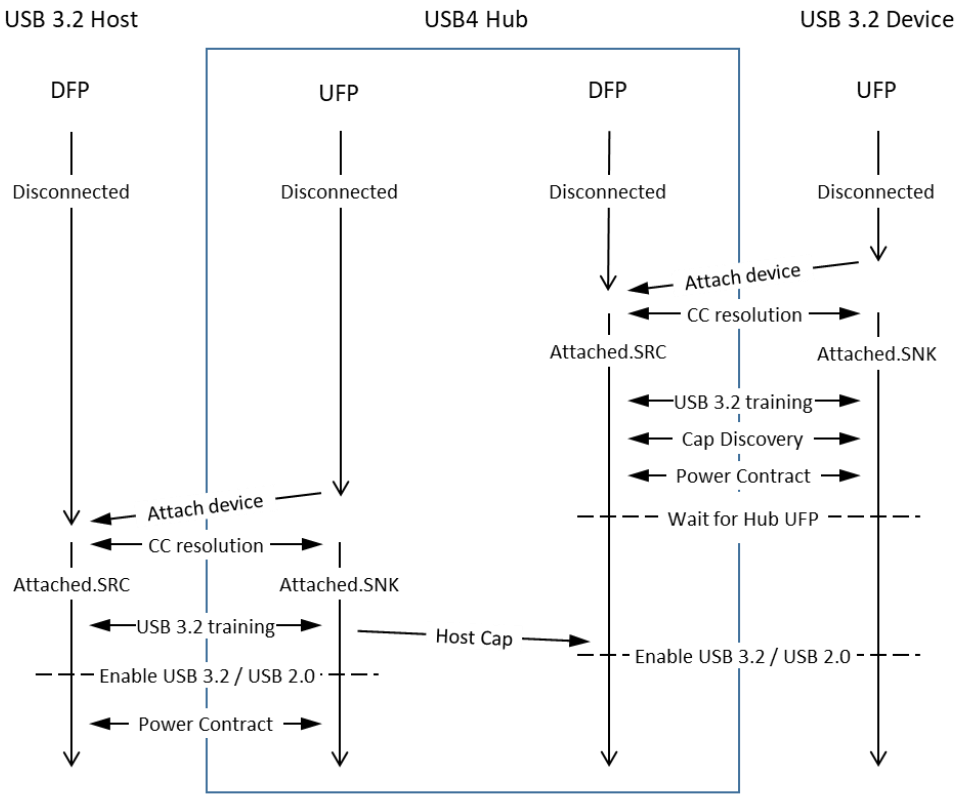
In the flow above, after the *USB 3.2* connection of the hub's UFP is established, the DFP connection remains valid with the *USB4* hub now operating as a traditional *USB 3.2* hub.

Figure 5-6 illustrates the connection flow model aligned across the combination of a *USB4* host, *USB4* hub and a DP Alt Mode device (operating in Multi-function mode). In this case,

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 5-5 说明了 *USB4* 集线器与 *USB 3.2* 主机和设备组合之间的连接流模型。

图 5-5 USB4 Hub 与 USB 3.2 主机和设备的连接流程模型



虽然 *USB 3.2* 设备不一定会响应发现 ID（SOP），但 *USB4* 集线器的 DFP 会尝试发现所连接设备的功能。

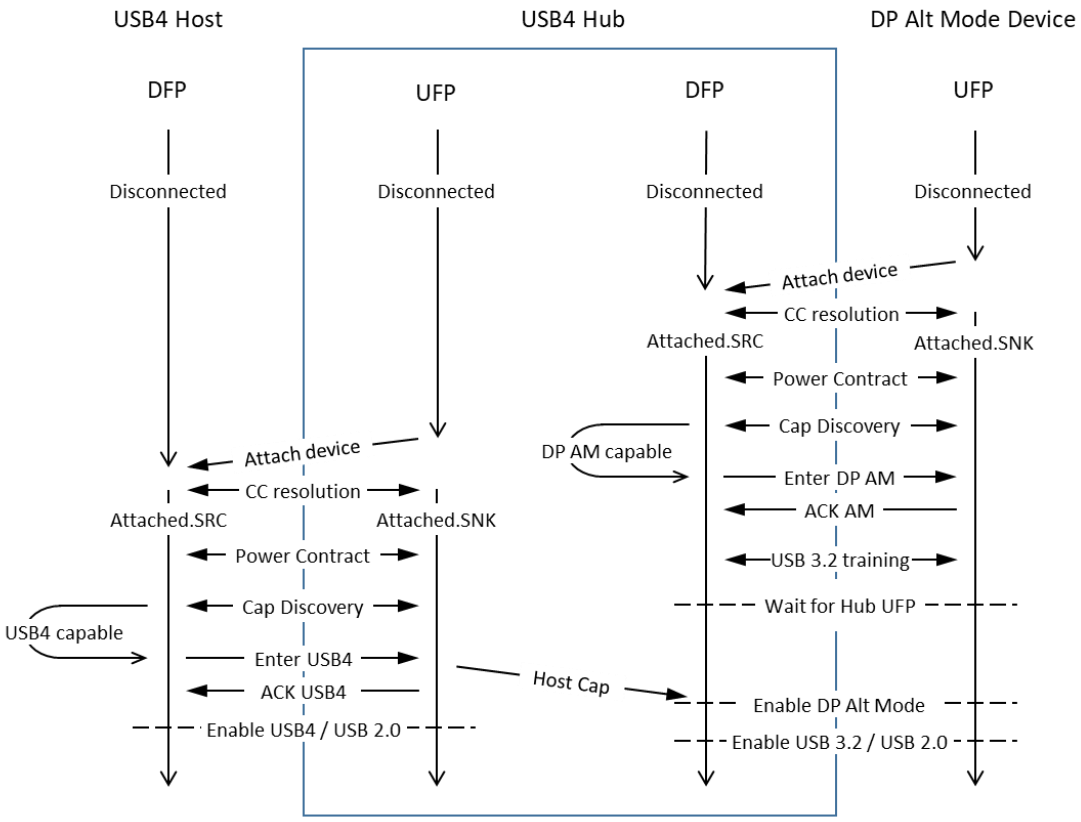
在上面的流程中，在建立集线器的 UFP 的 *USB 3.2* 连接之后，DFP 连接仍然有效，并且 *USB4* 集线器现在作为传统的 *USB 3.2* 集线器运行。

图 5-6 说明了 *USB4* 主机、*USB4* 集线器和 DP Alt Mode 设备（在多功能模式下运行）组合之间的连接流模型。在这种情况下，

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

the expected result is the enabling of the DP Alt Mode as bridged from *USB4* DisplayPort tunneling.

Figure 5-6 USB4 Hub with USB4 Host and DP Alt Mode Device Connection Flow Model

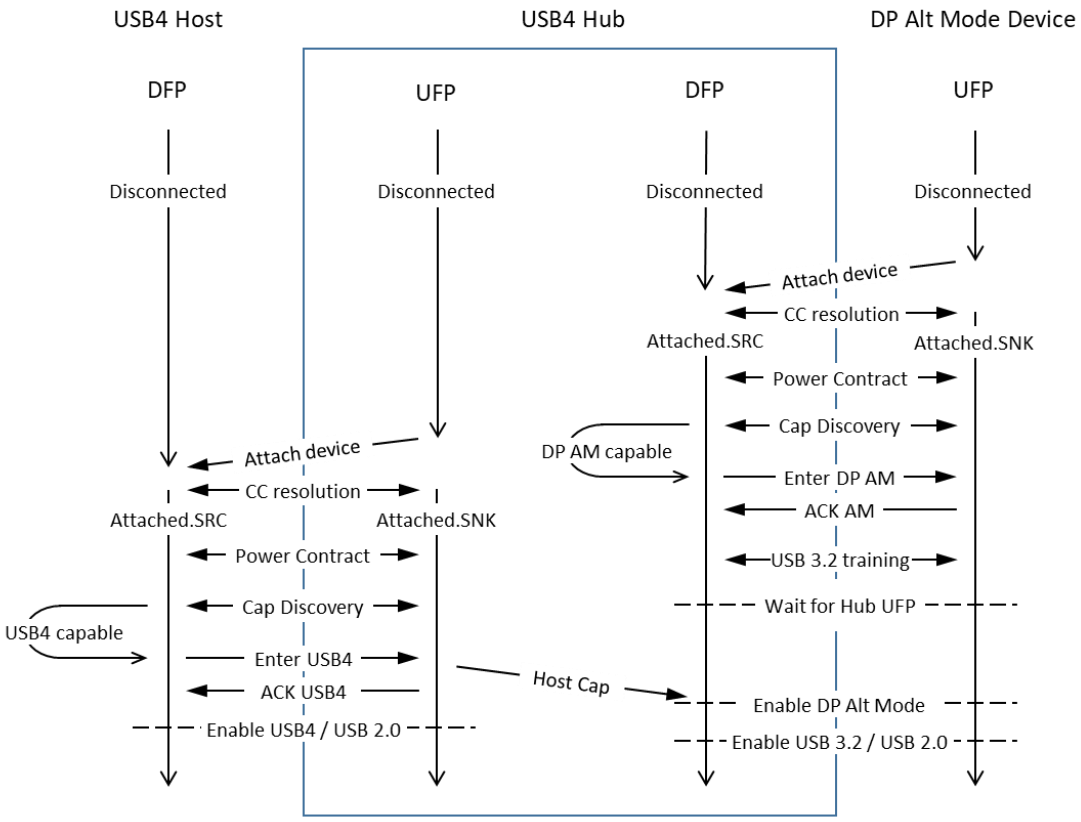


In the flow above, after the *USB4* connection of the hub's UFP is established, the DFP connection remains valid with the DisplayPort and *USB 3.2* data paths of the DFP being serviced by the *USB4* DisplayPort and Enhanced SuperSpeed tunnels.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

预期结果是启用从 *USB4* DisplayPort 隧道桥接的 DP Alt 模式。

图 5-6 USB4 Hub 与 USB4 Host 及 DP Alt Mode Device 连接流程模型

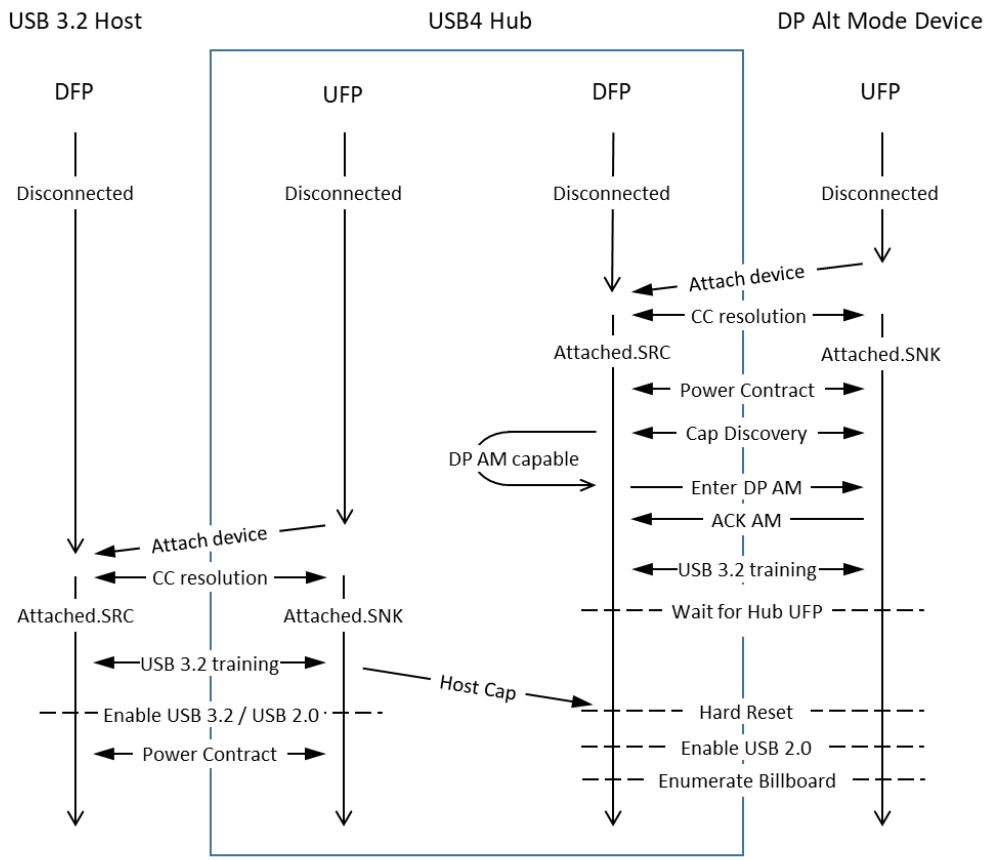


在上面的流程中，在建立集线器的 UFP 的 *USB4* 连接之后，DFP 连接仍然有效，其中 DFP 的 DisplayPort 和 *USB 3.2* 数据路径由 *USB4* DisplayPort 和增强型超高速隧道提供服务。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 5-7 illustrates the connection flow model aligned across the combination of a *USB 3.2* host, a *USB4* hub and a DP Alt Mode device (operating in Multi-function mode). The expected result in this case is that the DP Alt Mode will not be enabled and a Billboard exposed by the device since the host doesn't support *USB4*.

Figure 5-7 USB4 Hub with USB 3.2 Host and DP Alt Mode Device Connection Flow Model



In the flow above, after the *USB 3.2* connection of the hub's UFP is established, the DFP connection is no longer valid with the *USB4* hub now operating as a traditional *USB 3.2* hub. The hub's DFP shall then reset the port which will lead to a *USB 2.0* connection and the exposure of the Billboard device.

5.5.5 Connecting to Downstream USB4 Hubs

When a *USB4* hub is attached on its DFP to the UFP of another *USB4* hub, the *USB4* hub shall use the Host Present bit of the *USB PD* Enter_USB message to inform the downstream hub if the *USB4* capabilities listed in the message reflects the host's capabilities or not. If an initial connection is made with the downstream hub with the Host Present bit reset in the *USB PD* Enter_USB message, the *USB4* hub shall subsequently send a revised *USB PD* Enter_USB message with the Host Present bit set after its UFP has been fully established (see Section 5.5.2).

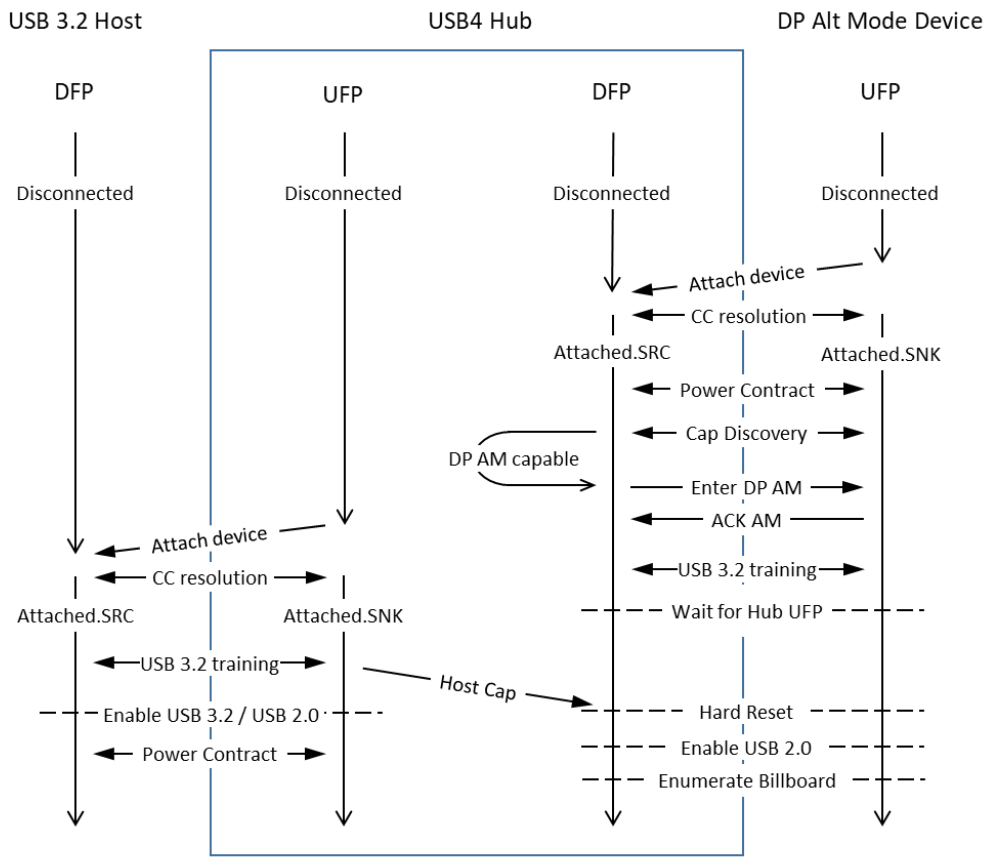
5.5.6 Fallback Functional Requirements for USB4 Hubs

When a *USB4* hub is attached on its UFP to a non-*USB4* DFP, the *USB4* hub shall seamlessly fall back to functioning as and meeting the requirements for a *USB 3.2* hub.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 5-7 展示了 *USB 3.2* 主机、*USB4* 集线器和 DP Alt Mode 设备（在多功能模式下运行）组合的连接流模型。在这种情况下，预期结果是不会启用 DP Alt Mode，并且设备会显示广告牌，因为主机不支持 *USB4*。

图 5-7 USB4 Hub 与 USB 3.2 Host 和 DP Alt Mode Device 连接流程模型



在上面的流程中，在建立集线器的 UFP 的 *USB 3.2* 连接后，DFP 连接不再有效，*USB4* 集线器现在作为传统的 *USB 3.2* 集线器运行。
然后，集线器的 DFP 将重置端口，这将导致 *USB 2.0* 连接和广告牌设备的曝光。

5.5.5 连接到下游 USB4 集线器

当 *USB4* 集线器在其 DFP 上连接到另一个 *USB4* 集线器的 UFP 时，*USB4* 集线器应使用 *USB PD* Enter_USB 消息的 Host Present 位来通知下游集线器消息中列出的 *USB4* 功能是否反映了主机的功能。如果在 *USB PD* Enter_USB 消息中重置 Host Present 位的情况下与下游集线器建立初始连接，则 *USB4* 集线器应在其 UFP 完全建立后随后发送修订的 *USB PD* Enter_USB 消息，其中设置了 Host Present 位（参见第 5.5.2 节）。

5.5.6 USB4 集线器的回退功能要求

当 *USB4* 集线器在其 UFP 上连接到非 *USB4* DFP 时，*USB4* 集线器将无缝恢复为 *USB 3.2* 集线器的功能并满足其要求。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

5.6 USB4 Device Connection Requirements

5.6.1 Fallback Mapping of USB4 Peripheral Functions to USB Device Class Types

USB4 peripheral devices provide functions based on data transferred over one or more of the protocol tunnels of *USB4*: Enhanced SuperSpeed USB, DisplayPort and PCI Express. For all peripheral functions that use the Enhanced SuperSpeed USB protocol tunnel, the mapping of those functions to USB device class specifications is clear but for those based on the other tunneled protocols, this mapping doesn't apply since those functions don't rely on USB device class drivers to operate.

Each function of a *USB4* device shall be mapped to an equivalent USB device class when possible. *USB4* devices that contain mapped USB device class functions shall support operation at *USB 3.2* or *USB 2.0* when connected to non-*USB4* hosts. This requirement is exempted for those functions that rely on DisplayPort or PCIe tunnels for *USB4* data transfer that don't reasonably map to an existing USB device class, e.g. a PCIe graphics adapter.

The performance of the function when mapped to a lower speed connection is expected to scale appropriately while still providing the functional equivalent of the primary capabilities of the peripheral function.

Table 5-2 lists USB Device Class types and the mapping requirements for *USB4* device peripheral functions as it relates to fallback when operating over *USB 3.2* or *USB 2.0*.

Table 5-2 Fallback Mapping USB4 Peripheral Functions to USB Device Class Types

Device Class Category	USB4 Peripheral Function Mapping	Comments
Audio	Required	
Video	Required	
Mass Storage	Required	
Comms/Networking	Required	
Printer	Required	
HID	Required	Only required when an equivently HID subclasss or report usage is defined.
Media Transfer Protocol	Required	
Smart Card	Required	
Still Image Capture	Required	
Monitor Device	Required	Only required in conjunction with providing associated display applications.

For all *USB4* peripheral functions based on DisplayPort and PCIe protocol tunneling that do not map to USB device class equivalents when operating over *USB 3.2* or *USB 2.0*, an appropriate USB Billboard Device Class shall be exposed to enable user notifications by the operating system of the host platform.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

5.6 USB4 设备连接要求

5.6.1 USB4 外设功能到 USB 设备类类型的回退映射

USB4 外围设备提供基于通过 *USB4* 的一个或多个协议隧道传输的数据的功能：增强型超高速 USB、DisplayPort 和 PCI Express。对于所有使用增强型超高速 USB 协议隧道的外围功能，这些功能与 USB 设备类规范的映射很明确，但对于基于其他隧道协议的功能，此映射不适用，因为这些功能不依赖于 USB 设备类驱动程序来运行。

USB4 设备的每个功能应尽可能映射到等效的 USB 设备类。包含映射的 USB 设备类功能的 *USB4* 设备在连接到非 *USB4* 主机时应支持在 *USB 3.2* 或 *USB 2.0* 上运行。对于依赖 DisplayPort 或 PCIe 隧道进行 *USB4* 数据传输且无法合理映射到现有 USB 设备类（例如 PCIe 图形适配器）的功能，此要求不受此限制。

当映射到较低速度的连接时，该功能的性能预计会适当扩展，同时仍提供与外围功能的主要功能等效的功能。

表 5-2 列出了 USB 设备类类型和 *USB4* 设备外围功能的映射要求，因为它与在 *USB 3.2* 或 *USB 2.0* 上操作时的回退有关。

表 5-2 将 USB4 外设功能回退映射到 USB 设备类类型

Device Class Category	USB4 Peripheral Function Mapping	Comments
Audio	Required	
Video	Required	
Mass Storage	Required	
Comms/Networking	Required	
Printer	Required	
HID	Required	Only required when an equivently HID subclasss or report usage is defined.
Media Transfer Protocol	Required	
Smart Card	Required	
Still Image Capture	Required	
Monitor Device	Required	Only required in conjunction with providing associated display applications.

对于基于 DisplayPort 和 PCIe 协议隧道的所有 *USB4* 外围功能，如果在 *USB 3.2* 或 *USB 2.0* 上运行时未映射到 USB 设备类等效项，则应公开适当的 USB 广告牌设备类，以启用主机平台操作系统的用户通知。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

5.7 Parameter Values

5.7.1 Timing Parameters

Table 5-3 provides the timeout requirement for a device that supports *USB4* to enable a *USB Billboard Device Class* interface when the device cannot connect as a *USB4* device during the discovery and entry process (Section 5.4).

Table 5-3 USB Billboard Device Class Availability Following USB4 Device Entry Failure

	Maximum	Description
tUSB4Timeout	1000 ms	The time between (1) a Sink attach or (2) the data connection is reestablished in the *USB PD* Data Reset process until the *USB Billboard Device Class* interface is exposed when *USB4* device entry is not successful.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

5.7 参数值

5.7.1 时序参数

表 5-3 提供了当支持 *USB4* 的设备在发现和进入过程中无法作为 *USB4* 设备进行连接时启用 *USB Billboard Device Class* 接口的超时要求（第 5.4 节）。

表 5-3 USB4 设备进入失败后的 USB Billboard 设备类别可用性

	Maximum	Description
tUSB4Timeout	1000 ms	The time between (1) a Sink attach or (2) the data connection is reestablished in the *USB PD* Data Reset process until the *USB Billboard Device Class* interface is exposed when *USB4* device entry is not successful.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6 Active Cables

Active cables shall minimally support *USB 3.2* Gen 2x1 and may support *USB 3.2* Gen 1x2 or Gen 2x2. As multi-lane *USB 3.2* and multi-lane *USB 3.2* repeaters become common, all active cables will be required to support two lanes. Active cables shall support *USB PD* eMarkers and may support Alternate Modes and advertise them as defined in Section 6.7.

Short active cables supporting lengths up to 5 meters are designed to 'just work' like passive cables with no discernable difference from the user's perspective.

Optically Isolated Active Cables (OIACs) support longer lengths up to 50 meters and provide electrical isolation between the two ends of the cable. OIACs are targeted for Industrial, Machine Vision, Remote Sensor, Pro Video, and Medical applications. OIACs do not 'just work' unlike short active cables. Long OIACs may not function correctly with Hosts, Devices, and Hubs that are not compliant to the *USB 3.2* Specification. Table 6-1 shows the limitations of OIACs with short active cables. Legacy USB3 devices may require using an adapter between the device and the OIAC. This adapter is defined in Section 6.6.4.3.1.

Since no power runs through an OIAC, they can only be used to connect a Source DRD to a Source DRD or a Source DRD to a DFP. *USB PD* Revision 3 must be supported on both port partners for an OIAC to function. Each cable plug of an OIAC is locally powered from VCONN and/or optionally from VBUS. OIACs shall function for *USB 3.2* when VCONN only is provided and may optionally use VBUS if provided. OIACs may require VBUS for Alternate Mode support. OIACs have no functionality when either cable plug is connected to a Sink/UFP only device (Sink/UFP devices are unable to provide power to the cable plug). OIACs require at least one end of the cable plug to be connected to a DRD (DRP and capable of accepting a DR_Swap to USB Device Role).

If a connection to a *USB 2.0* Device is required at the end of an OIAC, an adapter with a *USB 3.2* to *USB 2.0* transaction translator and VBUS/VCONN Source may be connected at the Device side of the cable to convert the *USB 3.2* signals to *USB 2.0* and provide power to the *USB 2.0* Device and the OIAC.

If an OIAC supports Alternate Modes that require the use of SBUs, the SBUs shall be optically isolated.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6 条有源电缆

有源电缆至少应支持 *USB 3.2* Gen 2x1，并可支持 *USB 3.2* Gen 1x2 或 Gen 2x2。随着多通道 *USB 3.2* 和多通道 *USB 3.2* 中继器变得普遍，所有有源电缆都将被要求支持两个通道。有源电缆应支持 *USB PD* eMarker，并可支持备用模式并按照第 6.7 节中的定义进行通告。

支持长达 5 米的短有源电缆被设计为像无源电缆一样“工作”，从用户的角度来看没有明显的区别。

光隔离有源电缆 (OIAC) 支持长达 50 米的电缆长度，并在电缆两端提供电气隔离。OIA C 适用于工业、机器视觉、远程传感器、专业视频和医疗应用。与短有源电缆不同，OIAC 并非“直接工作”。长 OIAC 可能无法与不符合 *USB 3.2* 规范的主机、设备和集线器正常工作。表 6-1 显示了使用短有源电缆的 OIAC 的局限性。旧式 USB3 设备可能需要在设备和 OIAC 之间使用适配器。此适配器在第 6.6.4.3.1 节中定义。

由于没有电源通过 OIAC，因此它们只能用于将源 DRD 连接到源 DRD 或将源 DRD 连接到 DFP。两个端口伙伴都必须支持 *USB PD* 修订版 3，OIAC 才能正常工作。OIAC 的每个电缆插头都由 VCONN 和/或可选的 VBUS 本地供电。当仅提供 VCONN 时，OIAC 应为 *USB 3.2* 工作，并且可以可选地使用 VBUS（如果提供）。OIAC 可能需要 VBUS 来支持备用模式。当任一电缆插头连接到仅 Sink/UFP 的设备时（Sink/UFP 设备无法为电缆插头供电），OIAC 不起作用。OIAC 要求电缆插头的至少一端连接到 DRD（DRP 并能够接受 DR_Swap 到 USB 设备角色）。

如果需要在 OIAC 末端连接 *USB 2.0* 设备，则可以在电缆的设备侧连接一个带有 *USB 3.2* 到 *USB 2.0* 事务转换器和 VBUS/VCONN 源的适配器，以将 *USB 3.2* 信号转换为 *USB 2.0* 并为 *USB 2.0* 设备和 OIAC 供电。

如果 OIAC 支持需要使用 SBU 的替代模式，则 SBU 应进行光学隔离。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 6-1 Comparison of Active Cables

	Short Active Cable	Optically Isolated Active Cable
USB 3.2 Support	*USB 3.2* Repeater	*USB 3.2* Repeater
USB 2.0 Support	Passive Connection	No end-to-end electrical connection. An OIAC Legacy Adapter (Section 6.6.4.3.1) required for *USB 2.0* support.
SBU Support	Passive Connection	Optional normative support in Alternate Modes only
USB PD Communication	All messages supported	Only a subset of messages is supported.
Bus Powered Devices	Supported	Not supported unless a VBUS/VCONN Source is connected between OIAC and Bus Powered Device. An OIAC Legacy Adapter (Section 6.6.4.3.1) is an example of a VBUS/VCONN Source.
End-to-End Electrical Connection	Yes	No
End-to-End Ground and VBUS Connections	Yes	No

Table 6-2 Summary of Active Cable Features

Cable Type	Length	USB PD	VBUS	VCONN Wiring	CC	*USB 2.0*	*USB 3.2* (All required)	SBU
Short	< 5 m	SOP' Required (SOP" Optional)	3 A or 5 A	Same as passive cable	Same as passive cable	Same as passive cable	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	Passive
Optically Isolated	*USB 3.2* Latency[1]	SOP' and SOP" Required	0 A	Local cable plug only	Optical	Not Allowed	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	Optional normative support in Alternate Modes only

Note 1: Length is set by the latency requirement in *USB 3.2*.

All active cables, regardless of length, shall be compliant with this specification, the *USB 3.2* including Appendix E, and the *USB 3.2* Active Cable CTS.

6.1 USB Type-C State Machine

OIAC cable plugs behave as Sinks on an initial cable connection. OIACs use *USB PD* Revision 3 to configure one plug as the DFP and one as the UFP as described in Section 6.2.1.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 6-1 有源电缆比较

	Short Active Cable	Optically Isolated Active Cable
USB 3.2 Support	*USB 3.2* Repeater	*USB 3.2* Repeater
USB 2.0 Support	Passive Connection	No end-to-end electrical connection. An OIAC Legacy Adapter (Section 6.6.4.3.1) required for *USB 2.0* support.
SBU Support	Passive Connection	Optional normative support in Alternate Modes only
USB PD Communication	All messages supported	Only a subset of messages is supported.
Bus Powered Devices	Supported	Not supported unless a VBUS/VCONN Source is connected between OIAC and Bus Powered Device. An OIAC Legacy Adapter (Section 6.6.4.3.1) is an example of a VBUS/VCONN Source.
End-to-End Electrical Connection	Yes	No
End-to-End Ground and VBUS Connections	Yes	No

表 6-2 有源电缆特性摘要

Cable Type	Length	USB PD	VBUS	VCONN Wiring	CC	*USB 2.0*	*USB 3.2* (All required)	SBU
Short	< 5 m	SOP' Required (SOP" Optional)	3 A or 5 A	Same as passive cable	Same as passive cable	Same as passive cable	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	Passive
Optically Isolated	*USB 3.2* Latency[1]	SOP' and SOP" Required	0 A	Local cable plug only	Optical	Not Allowed	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	Optional normative support in Alternate Modes only

注 1：长度由 *USB 3.2* 中的延迟要求设置。

所有有源电缆，无论长度如何，均应符合本规范、*USB 3.2*（包括附录 E）和 *USB 3.2* 有源电缆 CTS。

6.1 USB Type-C 状态机

OIAC 电缆插头在初始电缆连接上充当接收器。OIAC 使用 *USB PD* 修订版 3 将一个插头配置为 DFP，将另一个插头配置为 UFP，如第 6.2.1 节所述。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

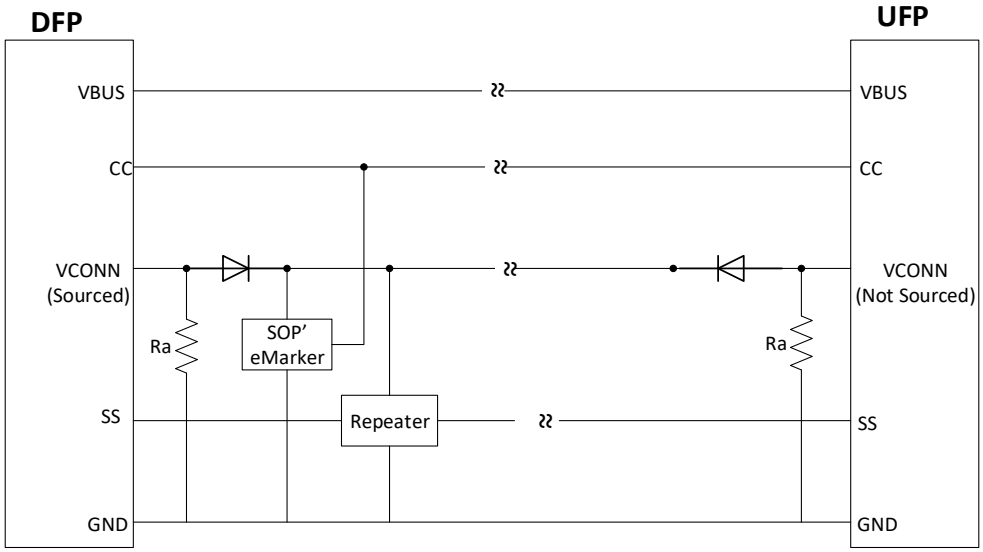
6.2 USB PD Requirements

This specification uses the USB Type-C® terminology for connection states and not the *USB PD* specification terminology.

Active cables shall be electronically marked and wired per Figure 6-1, Figure 6-2, or Figure 6-3.

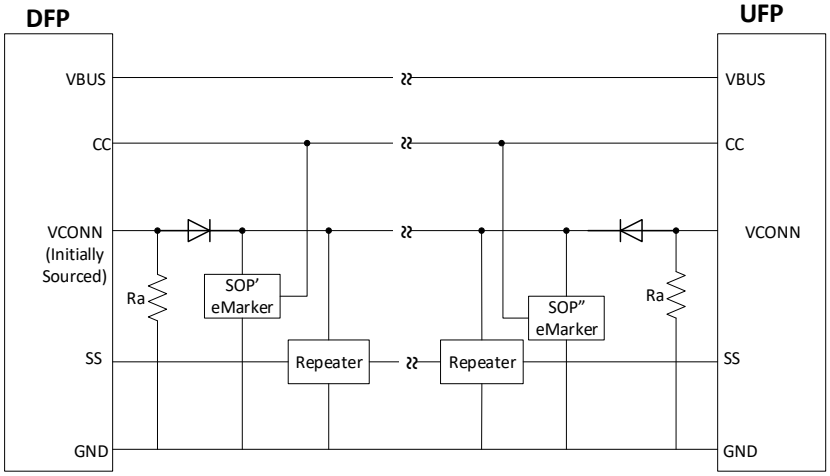
- The temperature sensor shall be co-located with the repeater for accurate thermal reporting.
- An active cable that contains two repeaters shall support both SOP' and SOP".
- An active cable that only contains one repeater internal to the active able (not in the cable plugs) shall implement SOP' and is not required to implement SOP".

Figure 6-1 Electronically Marked Short Active Cable with SOP' Only



Short active cables may optionally be electronically marked on both ends of the cable as illustrated in Figure 6-2.

Figure 6-2 Electronically Marked Short Active Cable with SOP' and SOP"



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.2 USB PD 要求

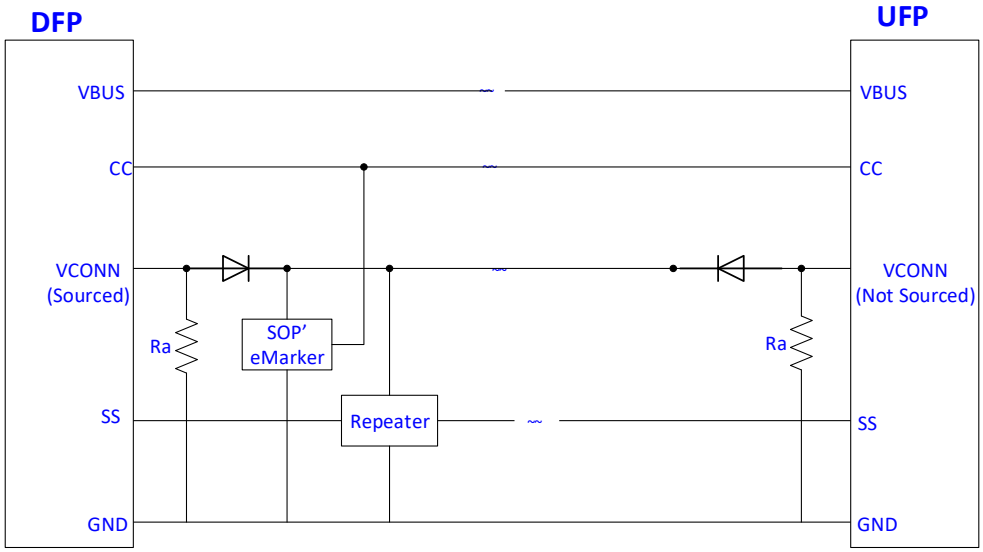
本规范使用 USB Type-C® 术语来表示连接状态，而不是 *USB PD* 规范术语。

有源电缆应按照图 6-1、图 6-2 或图 6-3 进行电子标记和接线。

• 温度传感器应与中继器位于同一位置，以便准确报告热量。• 包含两个中继器的有源电缆应支持 SOP ’ 和 SOP ”。• 仅包含一个中继器的有源电缆位于有源电缆内部（不在

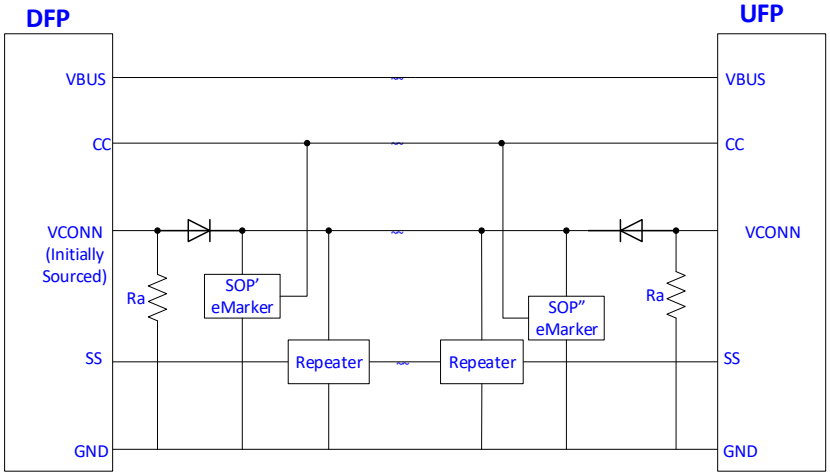
电缆插头）需执行SOP ’，无需执行SOP ”。

图 6-1 仅带 SOP ’ 的电子标记短有源电缆



短有源电缆可以选择性地在电缆两端进行电子标记，如图 6-2 所示。

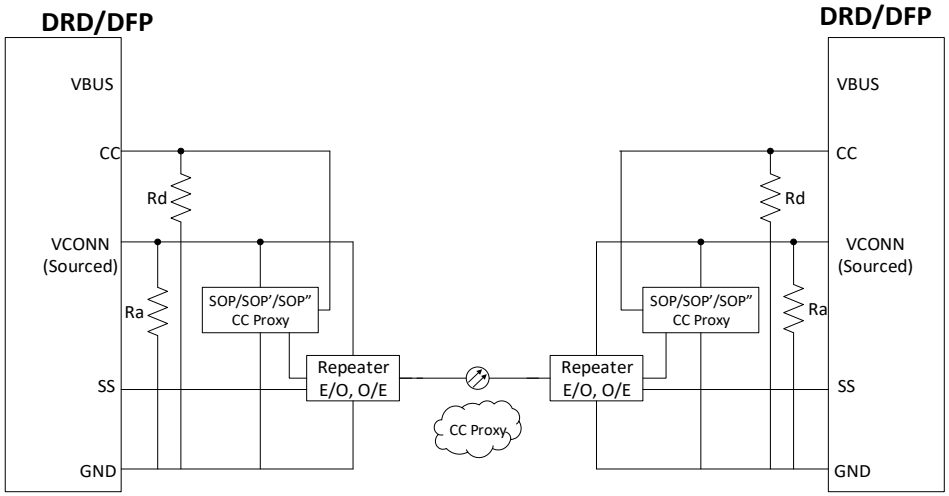
图 6-2 带有 SOP ’ 和 SOP ” 的电子标记短有源电缆



版权所有 © 2019 USB 3.0 Promoter Group。保留所有权利。

Optically isolated active cables shall be electronically marked on both ends of the cable as illustrated in Figure 6-3

Figure 6-3 Electronically Marked Optically Isolated Active Cable



6.2.1 Active Cable USB PD Requirements

Active cables shall support *USB PD* Revision 3, Version 1.2 or later. Active cables shall support *USB PD* Structured VDMs.

6.2.1.1 SOP' and SOP" Requirements

Active cables shall respond to ***Discover_Identity*** and ***Get_Status*** on SOP'. When the SOP'' Controller Present bit is set in the Active Cable VDO, they shall respond ***Get_Status*** on SOP'' as well.

OIACs have a different definition for SOP". SOP" is always the far-end cable plug relative to the message initiator.

6.2.1.2 Discovering Cable Characteristics

The *USB PD* ***Discover_Identity*** Command is used to discover the characteristics of the active cable. This command shall only be sent to SOP'. All active cables shall respond to the ***Discover_Identity*** Command with Active Cable VDOs that returns information about the cable. Note the active cable shall respond using either *USB PD* Revision 2 or *USB PD* Revision 3 following the *USB PD* Interoperability rules.

6.2.1.3 Cable Status

The *USB PD* ***Get_Status*** Command is used to discover the current state of the active cable. Cable status shall be reported on SOP' and shall also be reported on SOP" when the SOP'' Controller Presence bit is set in the Active Cable VDO.

6.2.2 USB PD Messages for OIAC

The following sections outline the *USB PD* Messages for an OIAC.

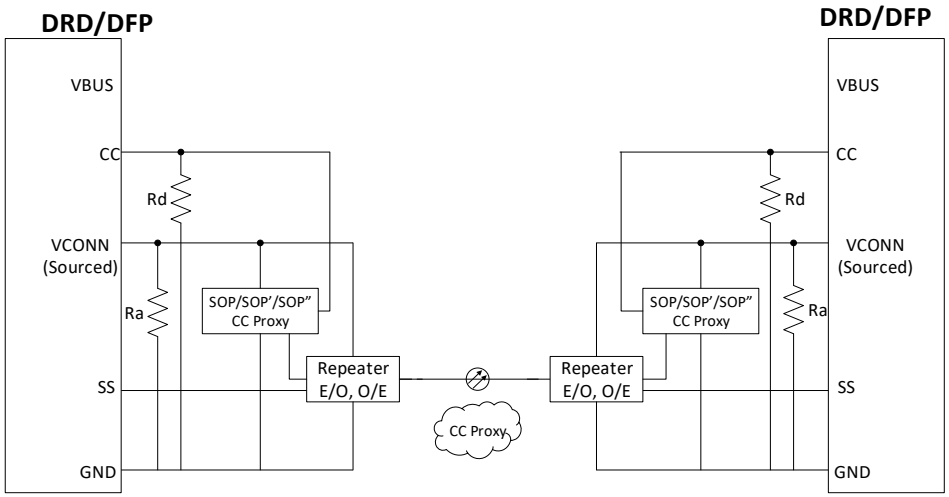
6.2.2.1 USB PD Message Handling on Initial Connection

The OIAC shall not forward *USB PD* messages until after determining the DFP to UFP Connection in the Active State and the Active Cable is configured (Phase 3 complete). The

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

光隔离有源电缆应在电缆两端进行电子标记，如图6-3所示

Figure 6-3 Electronically Marked Optically Isolated Active Cable



6.2.1 有源电缆 USB PD 要求

有源电缆应支持 *USB PD* 修订版 3，版本 1.2 或更高版本。有源电缆应支持 *USB PD* 结构化 VDM。

6.2.1.1 SOP ’ 和SOP ” 要求

有源电缆应响应 SOP ’ 上的 ***Discover_Identity*** 和 ***Get_Status***。当有源电缆 VDO 中的 SOP ’ ’ 控制器存在位被设置时，它们也应响应 SOP ’ ’ 上的 ***Get_Status***。

OIAC 对 “ SOP ” 有不同的定义。“ SOP ” 始终是相对于消息发起者的远端电缆插头。

6.2.1.2 发现电缆特性

USB PD ***Discover_Identity*** 命令用于发现活动电缆的特性。此命令应仅发送到 SOP ’。所有活动电缆都应使用活动电缆 VDO 响应 ***Discover_Identity*** 命令，该命令将返回有关电缆的信息。请注意，活动电缆应根据 *USB PD* 互操作性规则使用 *USB PD* 修订版 2 或 *USB PD* 修订版 3 进行响应。

6.2.1.3 电缆状态

USB PD ***Get_Status*** 命令用于发现活动电缆的当前状态。电缆状态应在 SOP ’ 上报告，并且当活动电缆 VDO 中的 SOP ’ ’ 控制器存在位设置时，还应在 SOP ” 上报告。

6.2.2 OIAC 的 USB PD 消息

以下部分概述了 OIAC 的 *USB PD* 消息。

6.2.2.1 初始连接时的 USB PD 消息处理

在确定 DFP 到 UFP 连接处于活动状态并且活动电缆配置完成（第 3 阶段完成）之前，OIAC 不得转发 *USB PD* 消息。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

OIAC shall process *USB PD* messages locally in the USB Type-C plug as defined in Table 6-3 on an initial connection before the disconnect/reconnect and data role establishment.

Table 6-3 OIAC USB PD Message Behavior on Initial Connection

Message Type	Local Cable Plug SOP	Local Cable Plug SOP'/SOP"	Local Cable Plug SOP	Local Cable Plug SOP'	Local Cable Plug SOP"
Control Messages	**Transmitted Message**		**Received Message**		
Accept	Normative	Normative	Normative	Ignore	Ignore
DR_Swap	Normative	Not Allowed	Wait	Ignore	Ignore
FR_Swap	Not Allowed	Not Allowed	Reject	Ignore	Ignore
Get_Country_Codes	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_PPS_Status	Not Supported	Not Allowed	Not Supported	Ignore	Ignore
Get_Sink_Cap	Not Allowed	Not Allowed	Normative	Ignore	Ignore
Get_Sink_Cap_Extended	Not Supported	Not Allowed	Not Supported	Ignore	Ignore
Get_Source_Cap	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Source_Cap_Extended	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Status	Not Allowed	Not Allowed	Not Supported	Normative	Ignore
GoodCRC	Normative	Normative	Normative	Normative	Ignore
GotoMin	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Not_Supported	Normative	Normative	Normative	Normative	Normative
Ping	Not Allowed	Not Allowed	Ignore	Ignore	Ignore
PR_Swap	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
PS_RDY	Not Allowed	Not Allowed	Normative	Ignore	Ignore
Reject	Not Allowed	Not Allowed	Normative	Ignore	Ignore
Soft_Reset	Normative	Not Allowed	Normative	Ignore	Ignore
Vconn_Swap	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Wait	Normative	Not Allowed	Normative	Ignore	Ignore
Data Messages	**Transmitted Message**		**Received Message**		
Source_Capabilities	Not Allowed	Not Allowed	Normative	Ignore	Ignore
Request	Normative	Not Allowed	Not Supported	Ignore	Ignore
Get_Country_Info	Not Allowed	Not Allowed	Not Supported	Not Supported	Not Supported
BIST	Not Allowed	Not Allowed	Not Supported	Normative	Ignore
Sink_Capabilities	Normative	Not Allowed	Not Supported	Ignore	Ignore
Battery_Status	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Alert	Not Allowed	Not Allowed	Ignore	Ignore	Ignore

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

OIAC 应在断开/重新连接和数据角色建立之前的初始连接上，在 USB Type-C 插头中本地处理 *USB PD* 消息，如表 6-3 所定义。

表 6-3 初始连接时 OIAC USB PD 消息行为

Message Type	Local Cable Plug SOP	Local Cable Plug SOP'/SOP"	Local Cable Plug SOP	Local Cable Plug SOP'	Local Cable Plug SOP"
Control Messages	**Transmitted Message**		**Received Message**		
Accept	Normative	Normative	Normative	Ignore	Ignore
DR_Swap	Normative	Not Allowed	Wait	Ignore	Ignore
FR_Swap	Not Allowed	Not Allowed	Reject	Ignore	Ignore
Get_Country_Codes	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_PPS_Status	Not Supported	Not Allowed	Not Supported	Ignore	Ignore
Get_Sink_Cap	Not Allowed	Not Allowed	Normative	Ignore	Ignore
Get_Sink_Cap_Extended	Not Supported	Not Allowed	Not Supported	Ignore	Ignore
Get_Source_Cap	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Source_Cap_Extended	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Status	Not Allowed	Not Allowed	Not Supported	Normative	Ignore
GoodCRC	Normative	Normative	Normative	Normative	Ignore
GotoMin	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Not_Supported	Normative	Normative	Normative	Normative	Normative
Ping	Not Allowed	Not Allowed	Ignore	Ignore	Ignore
PR_Swap	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
PS_RDY	Not Allowed	Not Allowed	Normative	Ignore	Ignore
Reject	Not Allowed	Not Allowed	Normative	Ignore	Ignore
Soft_Reset	Normative	Not Allowed	Normative	Ignore	Ignore
Vconn_Swap	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Wait	Normative	Not Allowed	Normative	Ignore	Ignore
Data Messages	**Transmitted Message**		**Received Message**		
Source_Capabilities	Not Allowed	Not Allowed	Normative	Ignore	Ignore
Request	Normative	Not Allowed	Not Supported	Ignore	Ignore
Get_Country_Info	Not Allowed	Not Allowed	Not Supported	Not Supported	Not Supported
BIST	Not Allowed	Not Allowed	Not Supported	Normative	Ignore
Sink_Capabilities	Normative	Not Allowed	Not Supported	Ignore	Ignore
Battery_Status	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Alert	Not Allowed	Not Allowed	Ignore	Ignore	Ignore

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 6-3 OIAC USB PD Message Behavior on Initial Connection, cont.

Message Type	Local Cable Plug SOP	Local Cable Plug SOP'/SOP"	Local Cable Plug SOP	Local Cable Plug SOP'	Local Cable Plug SOP"
Extended Messages	**Transmitted Message**		**Received Message**		
Battery_Capabilities	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Country_Codes	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Country_Info	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Firmware_Update_Request	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Firmware_Update_Response	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Battery_Cap	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Battery_Status	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Manufacturer_Info	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Manufacturer_Info	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
PPS_Status	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Security_Response	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Security_Request	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Sink_Capabilities_Extended	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Source_Capabilities_Extended	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Status	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Vendor Defined Messages	**Transmitted Message**		**Received Message**		
Discover Identity	Normative	Not Allowed	NAK	Normative	NAK
Discover SVIDs	Not Allowed	Not Allowed	NAK	Conditional Normative/ NAK	NAK
Discover Modes	Not Allowed	Not Allowed	NAK	Conditional Normative/ NAK	NAK
Enter Mode	Not Allowed	Not Allowed	NAK	NAK	NAK
Exit Mode	Not Allowed	Not Allowed	NAK	NAK	NAK
Attention	Not Allowed	Not Allowed	Ignore	NAK	NAK

6.2.2.2 USB PD Message Handling in the Active State

There are some *USB PD* SOP and SOP" messages that invalid in an OIAC, therefore the next two sections explicitly define all *USB PD* messages that do not traverse the cable either because the message is targeted to SOP' or are invalid and all *USB PD* messages that do traverse the cable to SOP" and SOP.

6.2.2.2.1 USB PD Messages Which Do Not Traverse the Cable in the Active State

The *USB PD* messages which do not traverse the OIAC when Active are defined in Table 6-4. Section 6.2.2.2.2 describes the messages which traverse the OIAC in Active.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 6-3 初始连接时的 OIAC USB PD 消息行为（续）

Message Type	Local Cable Plug SOP	Local Cable Plug SOP'/SOP"	Local Cable Plug SOP	Local Cable Plug SOP'	Local Cable Plug SOP"
Extended Messages	**Transmitted Message**		**Received Message**		
Battery_Capabilities	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Country_Codes	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Country_Info	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Firmware_Update_Request	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Firmware_Update_Response	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Battery_Cap	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Battery_Status	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Manufacturer_Info	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Manufacturer_Info	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
PPS_Status	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Security_Response	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Security_Request	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Sink_Capabilities_Extended	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Source_Capabilities_Extended	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Status	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Vendor Defined Messages	**Transmitted Message**		**Received Message**		
Discover Identity	Normative	Not Allowed	NAK	Normative	NAK
Discover SVIDs	Not Allowed	Not Allowed	NAK	Conditional Normative/ NAK	NAK
Discover Modes	Not Allowed	Not Allowed	NAK	Conditional Normative/ NAK	NAK
Enter Mode	Not Allowed	Not Allowed	NAK	NAK	NAK
Exit Mode	Not Allowed	Not Allowed	NAK	NAK	NAK
Attention	Not Allowed	Not Allowed	Ignore	NAK	NAK

6.2.2.2 活动状态下的 USB PD 消息处理

有一些 *USB PD* SOP 和 SOP ” 消息在 OIAC 中无效，因此接下来的两节明确定义了所有不穿过电缆的 *USB PD* 消息，因为该消息以 SOP ’ 为目标或无效，以及所有穿过电缆的 *USB PD* 消息为 SOP ” 和 SOP。

6.2.2.2.1 活动状态下不经过电缆的 USB PD 消息

表 6-4 定义了活动状态下不穿过 OIAC 的 *USB PD* 消息。
6.2.2.2.2 节描述了 Active 中遍历 OIAC 的消息。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 6-4 OIAC USB PD Messages Which Do Not Traverse in Active State

Message Type	Cable Plug SOP	Cable Plug SOP'/SOP"	Cable Plug SOP	Cable Plug SOP'/SOP"
Control Messages	**Transmitted Message**		**Received Message**	
Accept	Normative	Normative	Normative	Ignore[1]
FR_Swap	Not Allowed	Not Allowed	Reject	Ignore[1]
Get_PPS_Status	Not Supported	Not Allowed	Not Supported	Ignore[1]
Get_Sink_Cap	Not Allowed	Not Allowed	Normative[3]	Ignore[1]
Get_Sink_Cap_Extended	Not Supported	Not Allowed	Normative[3]	Ignore[1]
Get_Source_Cap	Normative	Not Allowed	Not Supported	Ignore[1]
Get_Source_Cap_Extended	Normative	Not Allowed	Not Supported	Ignore[1]
GoodCRC	Normative	Normative	Normative	Normative[2]/ Ignore[1]
GotoMin	Not Allowed	Not Allowed	Ignore	Ignore[1]
Ping	Not Allowed	Not Allowed	Ignore	Ignore[1]
PR_Swap	Not Allowed	Not Allowed	Not Supported	Ignore[1]
PS_RDY	Not Allowed	Not Allowed	Normative	Ignore[1]
Reject	Normative	Not Allowed	Normative	Ignore[1]
Soft_Reset	Normative	Not Allowed	Normative	Ignore[1]
Vconn_Swap	Not Allowed	Not Allowed	Not Supported	Ignore[1]
Wait	Normative[4]	Not Allowed	Normative	Ignore[1]
Data Messages	**Transmitted Message**		**Received Message**	
Source_Capabilities	Not Allowed	Not Allowed	Normative	Ignore[1]
Request	Normative	Not Allowed	Not Supported	Ignore[1]
BIST	Not Allowed	Not Allowed	Not Supported	Normative[2]/ Ignore[1]
Sink_Capabilities	Normative	Not Allowed	Not Supported	Ignore[1]
Extended Messages	**Transmitted Message**		**Received Message**	
PPS_Status	Not Allowed	Not Allowed	Not Supported	Ignore[1]
Sink_Capabilities_Extended	Normative	Not Allowed	Not Supported	Ignore[1]
Source_Capabilities_Extended	Not Allowed	Not Allowed	Not Supported	Ignore[1]

Note:
1. SOP" message may be dropped and not forwarded across the cable.
2. Normative for SOP' and Ignore for SOP".
3. See Section 6.4.2.
4. See Section 6.2.2.5.

6.2.2.2.2 USB PD Messages Which Do Traverse the Cable in the Active State

All *USB PD* SOP messages defined in Table 6-5 are forwarded across the cable on SOP. The messages are sent by the Initiator, forwarded optically through the cable, and then driven on CC from the far side cable plug to the Receiver.

The timing of the message forwarding is defined in Table 6-6. The GoodCRC is generated locally to the cable plug and returned within tTransmit on a valid Message. The OIAC shall be able to handle messages received with a minimum spacing of tInterFrameGap.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 6-4 活动状态下不传输的 OIAC USB PD 消息

Message Type	Cable Plug SOP	Cable Plug SOP'/SOP"	Cable Plug SOP	Cable Plug SOP'/SOP"
Control Messages	**Transmitted Message**		**Received Message**	
Accept	Normative	Normative	Normative	Ignore[1]
FR_Swap	Not Allowed	Not Allowed	Reject	Ignore[1]
Get_PPS_Status	Not Supported	Not Allowed	Not Supported	Ignore[1]
Get_Sink_Cap	Not Allowed	Not Allowed	Normative[3]	Ignore[1]
Get_Sink_Cap_Extended	Not Supported	Not Allowed	Normative[3]	Ignore[1]
Get_Source_Cap	Normative	Not Allowed	Not Supported	Ignore[1]
Get_Source_Cap_Extended	Normative	Not Allowed	Not Supported	Ignore[1]
GoodCRC	Normative	Normative	Normative	Normative[2]/ Ignore[1]
GotoMin	Not Allowed	Not Allowed	Ignore	Ignore[1]
Ping	Not Allowed	Not Allowed	Ignore	Ignore[1]
PR_Swap	Not Allowed	Not Allowed	Not Supported	Ignore[1]
PS_RDY	Not Allowed	Not Allowed	Normative	Ignore[1]
Reject	Normative	Not Allowed	Normative	Ignore[1]
Soft_Reset	Normative	Not Allowed	Normative	Ignore[1]
Vconn_Swap	Not Allowed	Not Allowed	Not Supported	Ignore[1]
Wait	Normative[4]	Not Allowed	Normative	Ignore[1]
Data Messages	**Transmitted Message**		**Received Message**	
Source_Capabilities	Not Allowed	Not Allowed	Normative	Ignore[1]
Request	Normative	Not Allowed	Not Supported	Ignore[1]
BIST	Not Allowed	Not Allowed	Not Supported	Normative[2]/ Ignore[1]
Sink_Capabilities	Normative	Not Allowed	Not Supported	Ignore[1]
Extended Messages	**Transmitted Message**		**Received Message**	
PPS_Status	Not Allowed	Not Allowed	Not Supported	Ignore[1]
Sink_Capabilities_Extended	Normative	Not Allowed	Not Supported	Ignore[1]
Source_Capabilities_Extended	Not Allowed	Not Allowed	Not Supported	Ignore[1]

Note:
1. SOP" message may be dropped and not forwarded across the cable.
2. Normative for SOP' and Ignore for SOP".
3. See Section 6.4.2.
4. See Section 6.2.2.5.

6.2.2.2.2 在活动状态下通过电缆的 USB PD 消息

表 6-5 中定义的所有 *USB PD* SOP 消息都通过 SOP 上的电缆转发。消息由发起方发送，通过电缆以光学方式转发，然后通过 CC 从远端电缆插头驱动到接收方。

消息转发的时间定义在表 6-6 中。GoodCRC 在电缆插头本地生成，并在有效消息的 tTransmit 内返回。OIAC 应能够处理以最小间隔 tInterFrameGap 接收的消息。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The message Initiator expects a response within tSenderResponse and will perform error recovery if no response is received within this time unless the message is a Firmware_Update_Request/Response or a Security_Request/Response. The message Receiver responds within tReceiverResponse unless there is an error. The OIAC shall decide to respond locally or forward the message, send the message across the fiber, and drive the message on the far side plug CC pin within tForward as shown in Figure 6-4 unless the message is Firmware_Update_Request/Response or a Security_Request/Response. The *USB PD* handler shall forward the messages addressed to SOP defined in Table 6-4. The *USB PD* Handler shall only forward to the far-end plug any message addressed to SOP" which are defined below:

- Firmware_Update_Request, Firmware_Update_Response
- Security_Request, Security_Response
- Status
- Enter Mode, Exit Mode, Attention (if the Alternate Modes are supported by the OIAC)

The OIAC shall not forward *USB PD* messages until it completes Phase 3. The cable plug shall send no response if a GoodCRC is not received from the Responder.

Some implementations may implement local copies of the SOP" information on the local cable plug and use an internal mechanism to send/receive responses.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

消息发起者期望在 tSenderResponse 时间内收到响应，如果在此时间内未收到响应，则将执行错误恢复，除非该消息是 Firmware_Update_Request/Response 或 Security_Request/Response。除非出现错误，否则消息接收器将在 tReceiverResponse 内做出响应。OIAC 应决定在本地响应或转发消息，通过光纤发送消息，并在 tForward 内将消息驱动到远端插头 CC 引脚，如图 6-4 所示，除非消息是 Firmware_Update_Request/Response 或 Security_Request/Response。*USB PD* 处理程序应转发表 6-4 中定义的发送到 SOP 的消息。*USB PD* 处理程序应仅将发送到 SOP 的任何消息转发到远端插头，定义如下：

- 固件更新请求、固件更新响应 • 安全请求、安全响应 • 状态 • 进入模式、退出模式、注意（如果 OIAC 支持备用模式）

OIAC 在完成第 3 阶段之前不得转发 *USB PD* 消息。如果未从响应方收到 GoodCRC，则电缆插头不得发送任何响应。

一些实现可以在本地电缆插头上实现“ SOP ”信息的本地副本，并使用内部机制来发送/接收响应。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 6-5 OIAC USB PD Messages Addressed to SOP Which Traverse the OIAC in the Active State

Message Type	SOP
Control Messages	**Forward Message**
DR_Swap	Normative
Get_Country_Codes	Normative
Get_Status	Normative
Not_Supported	Normative
Wait	Normative
Data Messages	**Forward Message**
Get_Country_Info	Normative
Battery_Status	Normative
Alert	Normative
Extended Messages	**Forward Message**
Battery_Capabilities	Normative
Country_Codes	Normative
Country_Info	Normative
Firmware_Update_Request	Normative
Firmware_Update_Response	Normative
Get_Battery_Cap	Normative
Get_Battery_Status	Normative
Get_Manufacturer_Info	Normative
Manufacturer_Info	Normative
Security_Request	Normative
Security_Response	Normative
Status	Normative
Vendor Defined Messages	**Forward Message**
Discover Identity	Normative
Discover SVIDs	Normative
Discover Modes	Normative
Enter Mode	Normative
Exit Mode	Normative
Attention	Normative

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 6-5 在活动状态下遍历 OIAC 的 OIAC USB PD 消息（发送到 SOP）

Message Type	SOP
Control Messages	**Forward Message**
DR_Swap	Normative
Get_Country_Codes	Normative
Get_Status	Normative
Not_Supported	Normative
Wait	Normative
Data Messages	**Forward Message**
Get_Country_Info	Normative
Battery_Status	Normative
Alert	Normative
Extended Messages	**Forward Message**
Battery_Capabilities	Normative
Country_Codes	Normative
Country_Info	Normative
Firmware_Update_Request	Normative
Firmware_Update_Response	Normative
Get_Battery_Cap	Normative
Get_Battery_Status	Normative
Get_Manufacturer_Info	Normative
Manufacturer_Info	Normative
Security_Request	Normative
Security_Response	Normative
Status	Normative
Vendor Defined Messages	**Forward Message**
Discover Identity	Normative
Discover SVIDs	Normative
Discover Modes	Normative
Enter Mode	Normative
Exit Mode	Normative
Attention	Normative

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-4 OIAC USB PD Message Forwarding

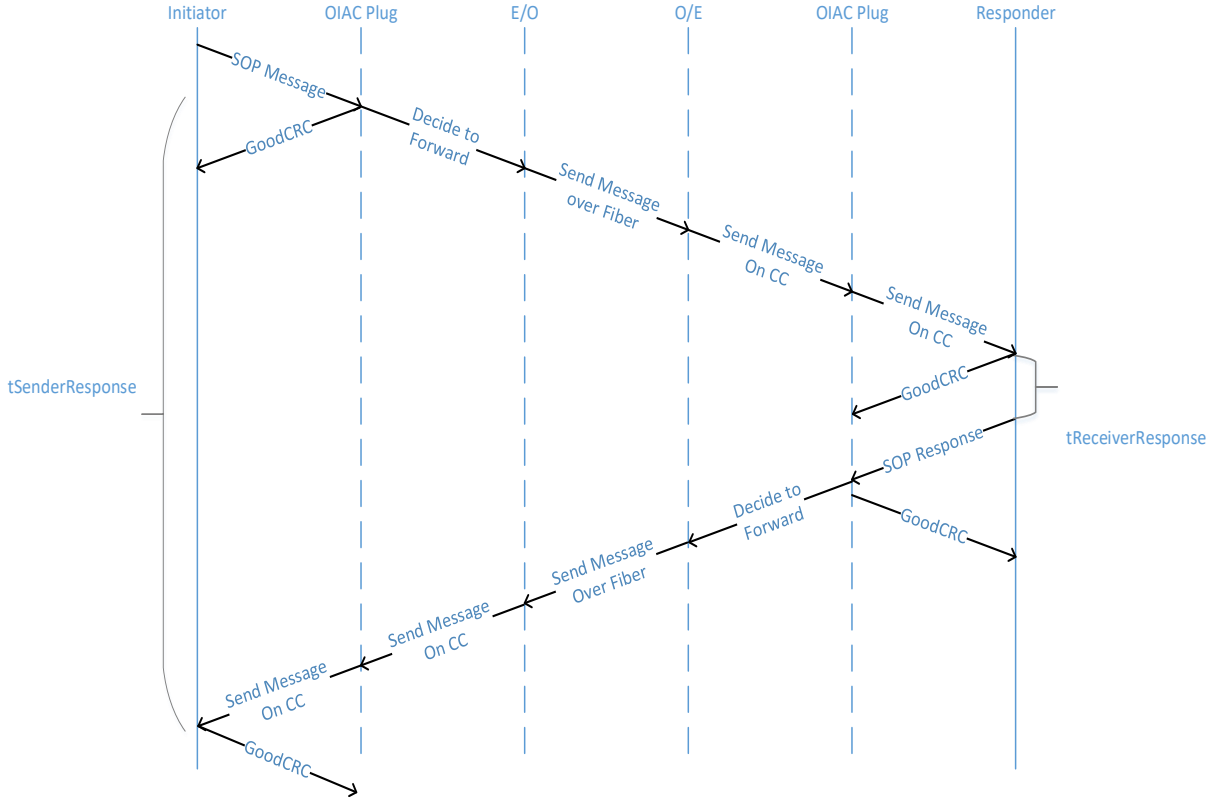


Table 6-6 OIAC USB PD Message Timing

Timer	Value (Min)	Value (Max)	Units	Reference
tDRSwapWait	100		ms	Time to wait if WAIT received before sending another DR_Swap. Defined in the *USB PD* Specification.
tForward		4	ms	Time to forward SOP Message one direction in OIAC.
tTransmit		195	µs	Time to send the GoodCRC. Defined in the *USB PD* Specification.
tInterFrameGap	25		µs	Time from the end of last bit of a Frame until the start of the first bit of the next Preamble. Defined in the *USB PD* Specification.
tReceiverResponse		15	ms	Time for SOP Receiver to respond. Defined in the *USB PD* Specification.
tSenderResponse	24	30	ms	Time for SOP Initiator to receive response. Defined in the *USB PD* Specification.
tBootupCRCHoldoff		50	ms	Hold off on GoodCRC until ready to respond with Operational RDO in Phase 3.

Note: The *USB PD* specification revision shall take precedence over this table if any discrepancies exist.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-4 OIAC USB PD Message Forwarding

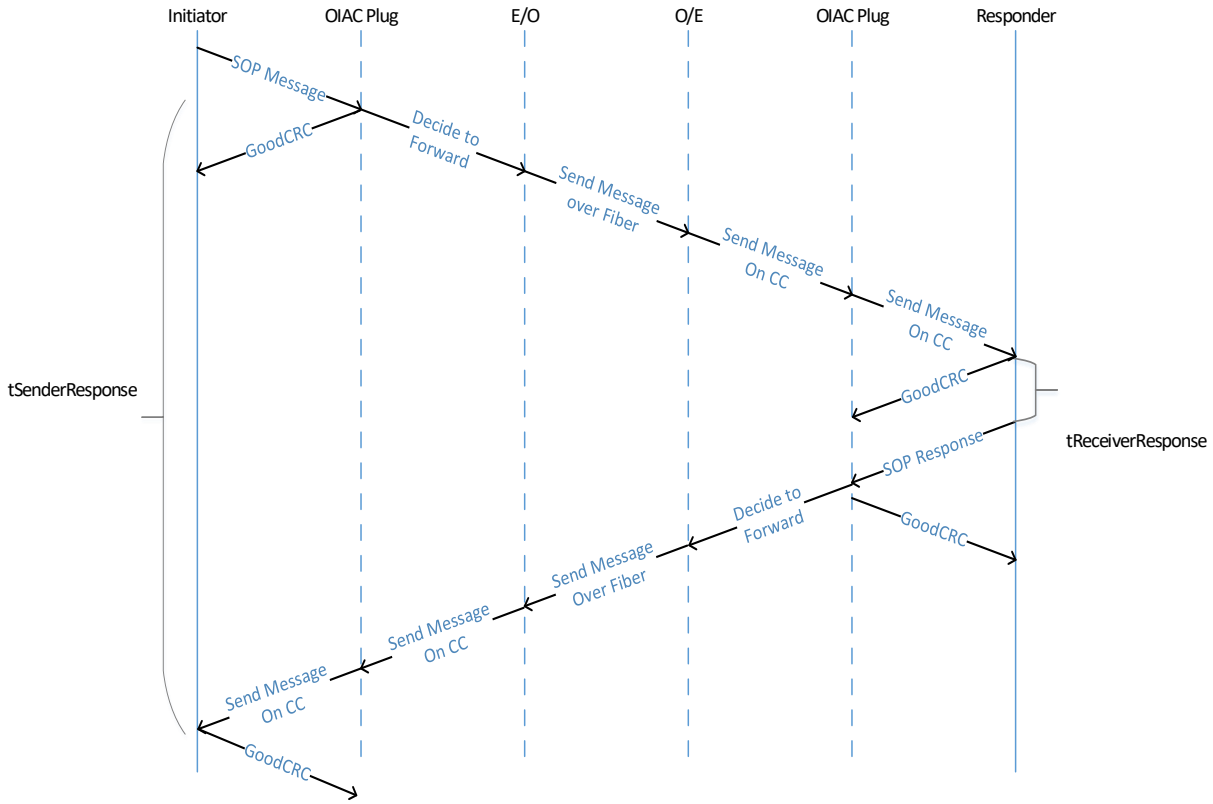


表 6-6 OIAC USB PD 消息时序

Timer	Value (Min)	Value (Max)	Units	Reference
tDRSwapWait	100		ms	Time to wait if WAIT received before sending another DR_Swap. Defined in the *USB PD* Specification.
tForward		4	ms	Time to forward SOP Message one direction in OIAC.
tTransmit		195	µs	Time to send the GoodCRC. Defined in the *USB PD* Specification.
tInterFrameGap	25		µs	Time from the end of last bit of a Frame until the start of the first bit of the next Preamble. Defined in the *USB PD* Specification.
tReceiverResponse		15	ms	Time for SOP Receiver to respond. Defined in the *USB PD* Specification.
tSenderResponse	24	30	ms	Time for SOP Initiator to receive response. Defined in the *USB PD* Specification.
tBootupCRCHoldoff		50	ms	Hold off on GoodCRC until ready to respond with Operational RDO in Phase 3.

注意：如果存在任何差异，则以*USB PD*规范修订为准。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.2.2.3 USB PD Reset Handling

The *USB PD* Reset handling by OIAC is defined in Table 6-7.

The OIAC shall:

1. Detect the Hard Reset ordered set
2. Forward it to the remote plug and remote port
3. Reset its state machine.

Table 6-7 OIAC SOP Messages Which Terminate at the Cable Plug

Ordered Sets	Note
Hard Reset	Resets port partners at each end of the cable and the cable itself
Cable Reset	OIAC shall ignore a Cable reset

A Hard Reset signal can occur at any time during normal operation of the cable and also during the cable initialization. This signal will take precedent over the initialization state machine and immediately forward the Hard Reset Message to the remote plug, using an internal cable message.

6.2.2.4 Internal Cable Messages

All SOP" and SOP messages shall be forwarded or terminated as defined in Section 6.2.2 and will not be further described in this section.

The messages defined in this section provide informative guidance on internal messages for OIACs. The actual definition and implementation of each message is left to the implementer.

In this section and Section 6.3, there is a defined Master/Slave Plug for *USB PD* communication at time of manufacture. These designations are completely internal to the cable, but are used to simplify the cable initialization and internal messaging.

6.2.2.4.1 MSG_Keep_Alive

A low duty cycle message that is meant to inform the remote cable plug that the local cable plug is still operational.

A simple example is that the only the master plug will send MSG_Keep_Alive and the slave must respond with MSG_Keep_Alive_ACK. Each end will have its own timeout for MSG_Keep_Alive and MSG_Keep_Alive_ACK.

6.2.2.4.2 MSG_Keep_Alive_ACK

Acknowledgement message to the MSG_Keep_Alive.

A simple example is that the only the master plug will send MSG_Keep_Alive and the slave must respond with MSG_Keep_Alive_ACK. Each end will have its own timeout for MSG_Keep_Alive and MSG_Keep_Alive_ACK.

6.2.2.4.3 MSG_Port_Capabilities

This message contains all relevant local port capabilities including but not limited to:

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.2.2.3 USB PD 复位处理

OIAC 的 *USB PD* 复位处理在表 6-7 中定义。

OIAC 应当：

1. 检测硬重置有序集2. 将其转发至远程插头和远程端口3. 重置其状态机。

表 6-7 终止于电缆插头的 OIAC SOP 消息

Ordered Sets	Note
Hard Reset	Resets port partners at each end of the cable and the cable itself
Cable Reset	OIAC shall ignore a Cable reset

硬复位信号可能在电缆正常运行期间以及电缆初始化期间的任何时间发生。此信号将优先于初始化状态机，并使用内部电缆消息立即将硬复位消息转发到远程插头。

6.2.2.4 内部电缆信息

所有“ SOP ”和SOP消息应按照第6.2.2节的定义进行转发或终止，本节不再赘述。

本节定义的消息为 OIAC 提供了有关内部消息的信息指导。每条消息的实际定义和实施由实施者决定。

在本节和第 6.3 节中，在制造时定义了用于 *USB PD* 通信的主/从插头。这些指定完全是电缆内部的，但用于简化电缆初始化和内部消息传递。

6.2.2.4.1 MSG_Keep_Alive

低占空比消息旨在通知远程电缆插头本地电缆插头仍可运行。

一个简单的例子是，只有主插头会发送 MSG_Keep_Alive，而从插头必须以 MSG_Keep_Alive_ACK 进行响应。每一端都有自己的 MSG_Keep_Alive 和 MSG_Keep_Alive_ACK 超时时间。

6.2.2.4.2 MSG_Keep_Alive_ACK

向 MSG_Keep_Alive 发送确认消息。

一个简单的例子是，只有主插头会发送 MSG_Keep_Alive，而从插头必须以 MSG_Keep_Alive_ACK 进行响应。每一端都有自己的 MSG_Keep_Alive 和 MSG_Keep_Alive_ACK 超时时间。

6.2.2.4.3 MSG_Port_Capabilities

该消息包含所有相关的本地端口功能，包括但不限于：

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- Chunked/Unchunked capability
- DRD/DFP/UFP capabilities

6.2.2.4.4 MSG_Cable_Config

This message contains the final cable configuration based on known system capabilities.

It will contain both relevant ports' capabilities and the final DFP/UFP roles for the system.

This message will also serve as the signal in Phase 2 for the cable plug to start the reboot process.

6.2.2.4.5 MSG_Release_Remote_SourceCap_GoodCRC

This is a synchronization message to attempt to bring up both ports at the same time.

It is used in Phase 3 and is the signal to release the GoodCRC message to the Source Capabilities message from the attached port. At the beginning of Phase 3, after each plug has been rebooted, and depending on the final DFP/UFP role, each plug should wait for MSG_Release_Remote_SourceCap_GoodCRC before it is allowed to release a GoodCRC in response to a Source_Capabilities message from the port.

6.2.2.4.6 MSG_DR_Swap_Init

Initial DR_Swap sent by the Master Plug to Slave plug to perform a DR_Swap.

6.2.2.4.7 MSG_DR_Swap_Reject

This is message from the slave plug to report that the initial DR_Swap was rejected by its attached port.

This is needed by the master plug to attempt to re-configure the cable such that the slave port can remain a DFP. This is part of the DR_Swap test in Phase 1, shown in the state diagram transition from M3 to M4 (or M3 to M5). It is also possible that this may be needed in Phase 3, if the Slave port rejects the DR_Swap.

6.2.2.4.8 MSG_DR_Swap_Accept

This is message from the slave plug to report that the initial DR_Swap was accepted by its attached port.

This is needed by the master plug to continue (M3 → M6 transition) in Phase 1 in the cable initialization.

6.2.2.4.9 MSG_Force_Detach

This message is to request the remote plug to disconnect from its attached port. The disconnect method can be done by raising the voltage on the CC line to above vRd-Connect or removing Rd.

This will cause the remote port to remove VCONN from the remote plug all the circuitry should be powered down, therefore resetting any action taken by the plug on the CC line to cause the disconnect.

6.2.2.4.10 MSG_Hard_Reset

This message is to forward a Hard_Reset signal to the remote plug and port.

An internal Hard Reset message should be responded to with an Acknowledgement.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• 分块/非分块功能 • DRD/DFP/UFP 功能

6.2.2.4.4 MSG_电缆配置

该消息包含基于已知系统功能的最终电缆配置。

它将包含相关端口的功能和系统的最终 DFP/UFP 角色。

此消息还将作为第 2 阶段中电缆插头启动重启过程的信号。

6.2.2.4.5 MSG_Release_Remote_SourceCap_GoodCRC

这是一个同步消息，用于尝试同时启动两个端口。

它用于第 3 阶段，是将 GoodCRC 消息从所连接端口释放到源功能消息的信号。在第 3 阶段开始时，在每个插头重新启动后，根据最终的 DFP/UFP 角色，每个插头应等待 MSG_Release_Remote_SourceCap_GoodCRC，然后才允许释放 GoodCRC 以响应来自端口的 Source_Capabilities 消息。

6.2.2.4.6 MSG_DR_Swap_Init

主插头向从属插头发送初始 DR_Swap 以执行 DR_Swap。

6.2.2.4.7 MSG_DR_Swap_Reject

这是来自从属插头的消息，报告初始 DR_Swap 被其所连接的端口拒绝。

主插头需要这样做，以尝试重新配置电缆，使从端口可以保持 DFP 状态。这是第 1 阶段 DR_Swap 测试的一部分，如状态图从 M3 到 M4（或从 M3 到 M5）的转换所示。也可能需要这样做

在阶段 3，如果从端口拒绝 DR_Swap。

6.2.2.4.8 MSG_DR_Swap_Accept

这是来自从属插头的消息，报告其所连接端口接受了初始 DR_Swap。

主插头需要在电缆初始化的第 1 阶段继续（M3 → M6 转换）。

6.2.2.4.9 MSG_Force_Detach

此消息用于请求远程插头与其所连接的端口断开连接。断开连接的方法可以通过将 CC 线上的电压升高到 vRd-Connect 以上或移除 Rd 来实现。

这将导致远程端口从远程插头上移除 VCONN，所有电路都应关闭，因此重置 CC 线上的插头采取的任何操作以导致断开连接。

6.2.2.4.10 MSG_Hard_Reset

此消息用于将 Hard_Reset 信号转发到远程插头和端口。

内部硬重置消息应以确认来响应。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.2.2.4.11 MSG_Acknowledgement

This message is to acknowledge that a message was received.

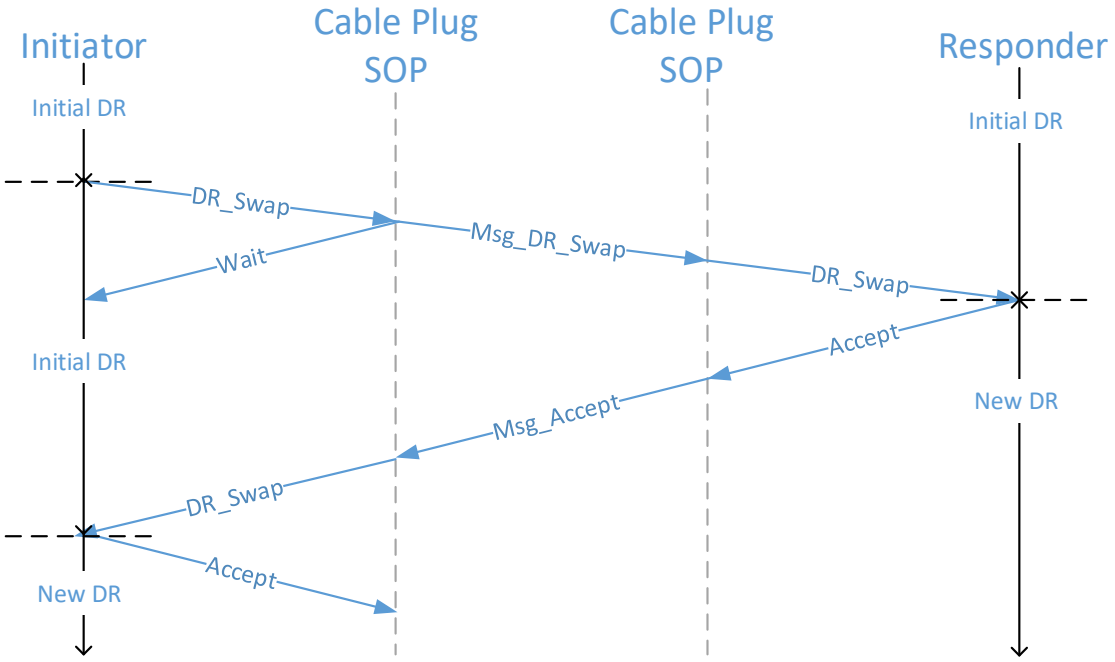
This message has been explicitly defined in a few specific cases but can be used more broadly.

6.2.2.5 Data Role Swap in Active State

OIACs shall support Data Role Swaps on SOP. Each OIAC plug discovers its plug port partner and determines if it is capable of a Data Role Swap during the initialization process described in Section 6.3. OIAC cable plugs generate internal messages to communicate the DR_Swap, Accept, Reject, and Wait to the far side of the cable.

- The flow of a successful DR_Swap is shown in Figure 6-5.
- The flow of a Responder rejecting a DR_Swap is shown in Figure 6-6.
- The flow of a Responder issuing a Wait to a DR_Swap is shown in Figure 6-7. Note: The *USB PD* Wait and Retry timers shall follow all timing requirements in *USB PD*.
- The flow of an Initiator rejecting a cable plug DR_Swap due to an Accept from the Responder is shown in Figure 6-8.
- The flow of an Initiator issuing a Wait to a cable plug DR_Swap due to an Accept from the Responder is shown in Figure 6-9. Note: This does not follow the *USB PD* Wait timing, because a Hard Reset is initiated

Figure 6-5 OIAC Successful Data Role Swap



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.2.2.4.11 MSG_确认

此消息是为了确认已收到消息。

此信息已在一些特定情况下明确定义，但可以更广泛地使用。

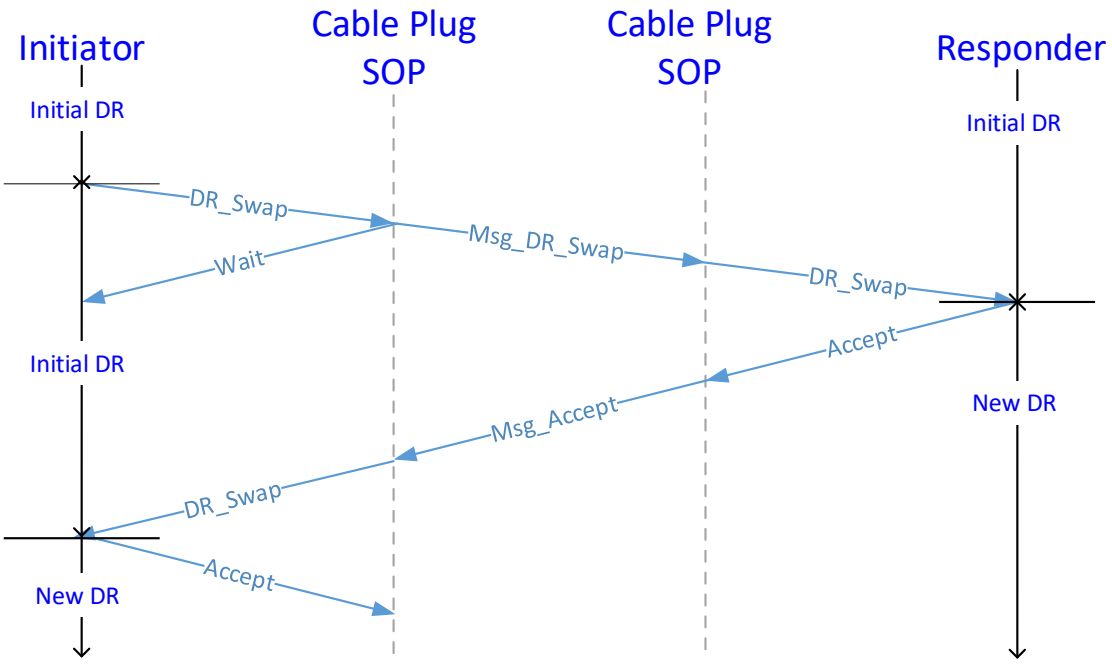
6.2.2.5 活动状态下的数据角色交换

OIAC 应支持 SOP 上的数据角色交换。每个 OIAC 插头都会发现其插头端口伙伴
并确定它是否能够在第 6.3 节描述的初始化过程中进行数据角色交换。OIAC 电缆插头生成内部消息，以将 DR_Swap、Accept、Reject 和 Wait 传达到电缆的远端。

• 成功 DR_Swap 的流程如图 6-5 所示。• 响应方拒绝 DR_Swap 的流程如图 6-6 所示。• 响应方向 DR_Swap 发出等待的流程如图 6-7 所示。注意：*USB PD* 等待和重试计时器应遵循 *USB PD* 中的所有计时要求。• 由于响应方的接受，发起方拒绝电缆插头 DR_Swap 的流程如图 6-8 所示。• 由于响应方的接受，发起方向电缆插头 DR_Swap 发出等待的流程如图 6-9 所示。

响应器如图 6-9 所示。注意：这不遵循 *USB PD* 等待时序，因为启动了硬重置

Figure 6-5 OIAC Successful Data Role Swap



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-6 OIAC Rejected Data Role Swap

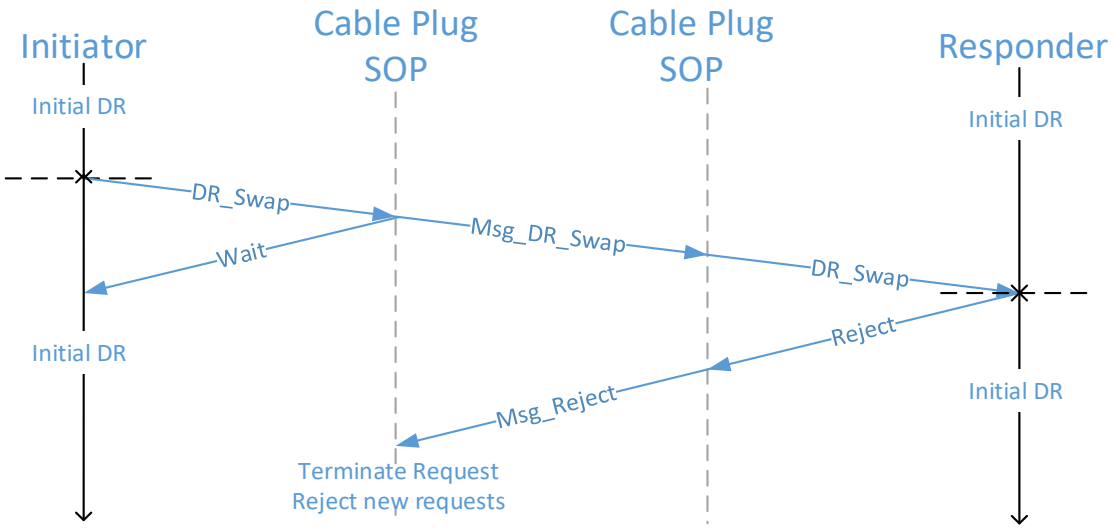
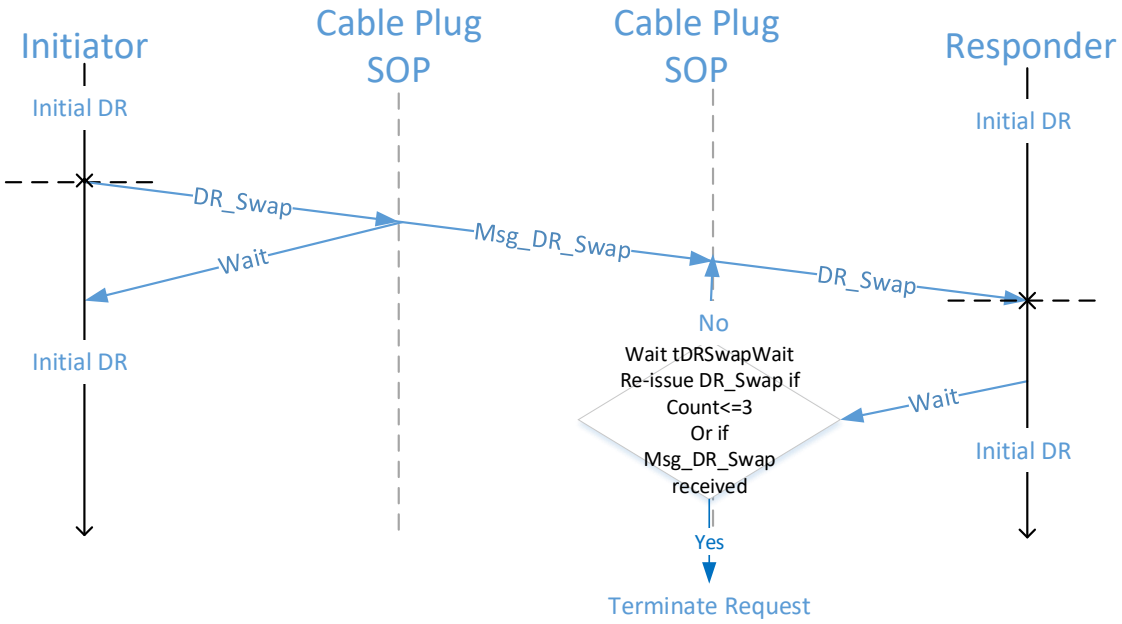


Figure 6-7 OIAC Wait Data Role Swap



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-6 OIAC Rejected Data Role Swap

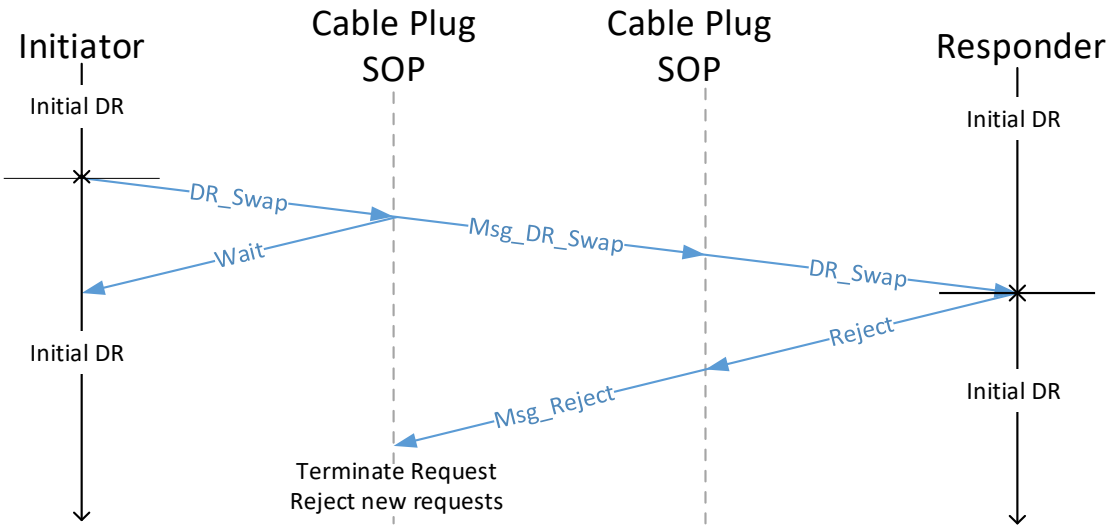
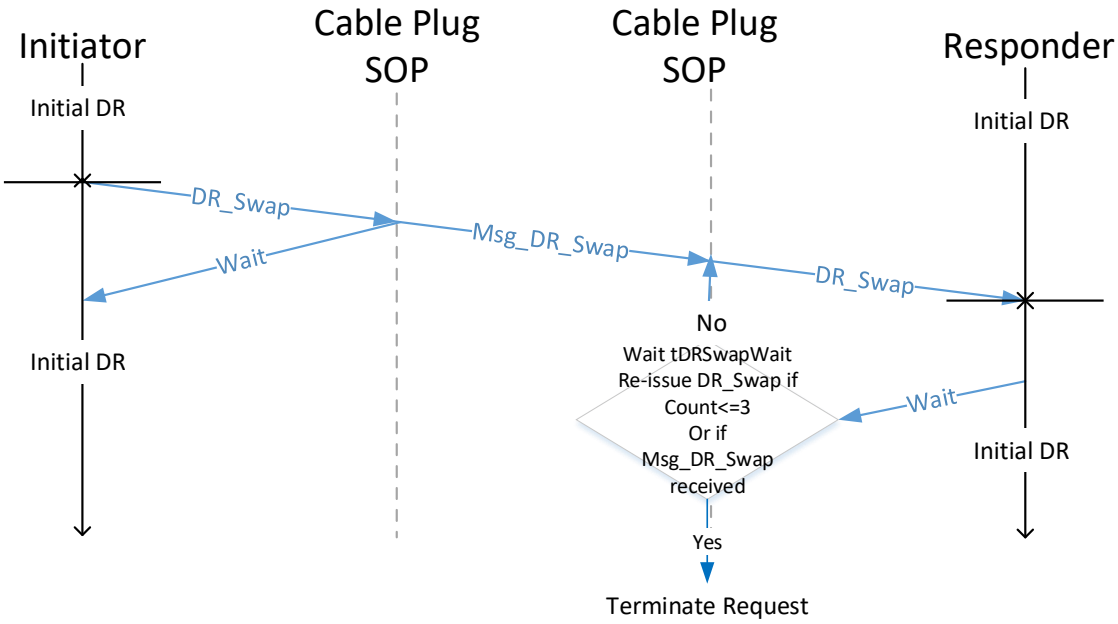
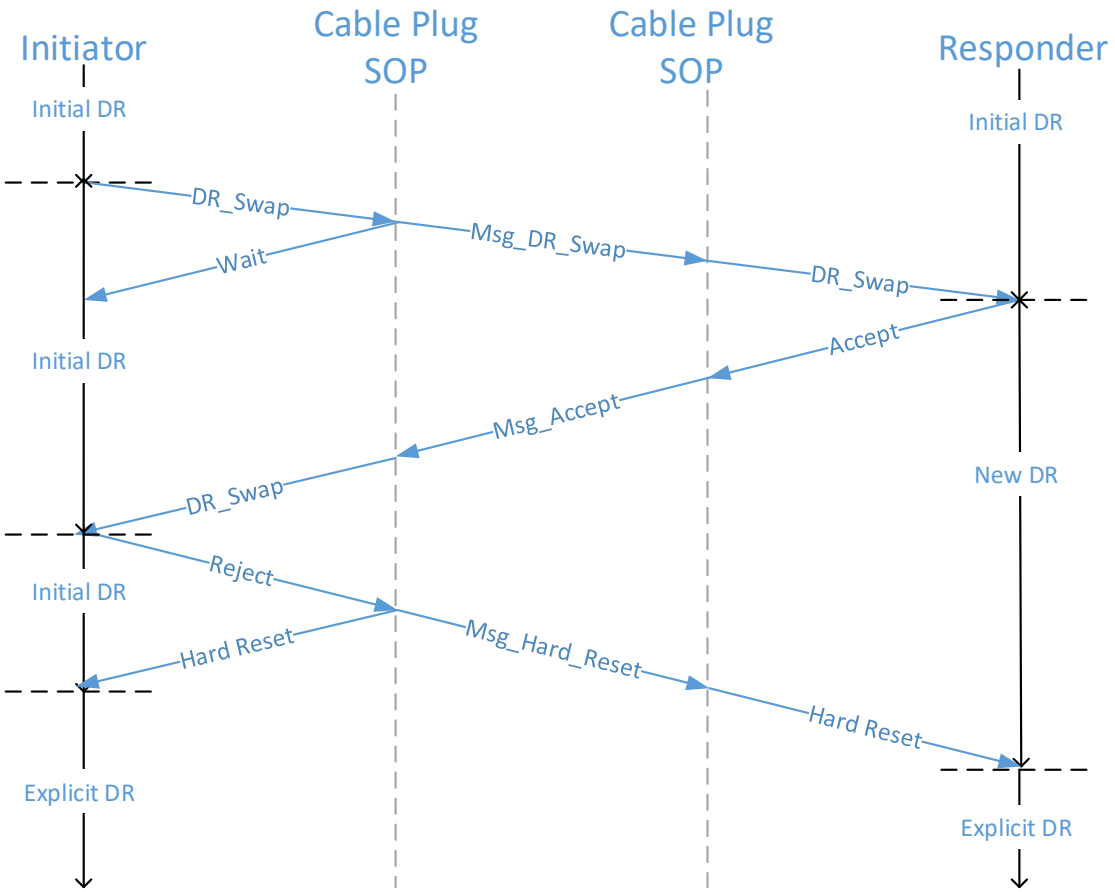


Figure 6-7 OIAC Wait Data Role Swap



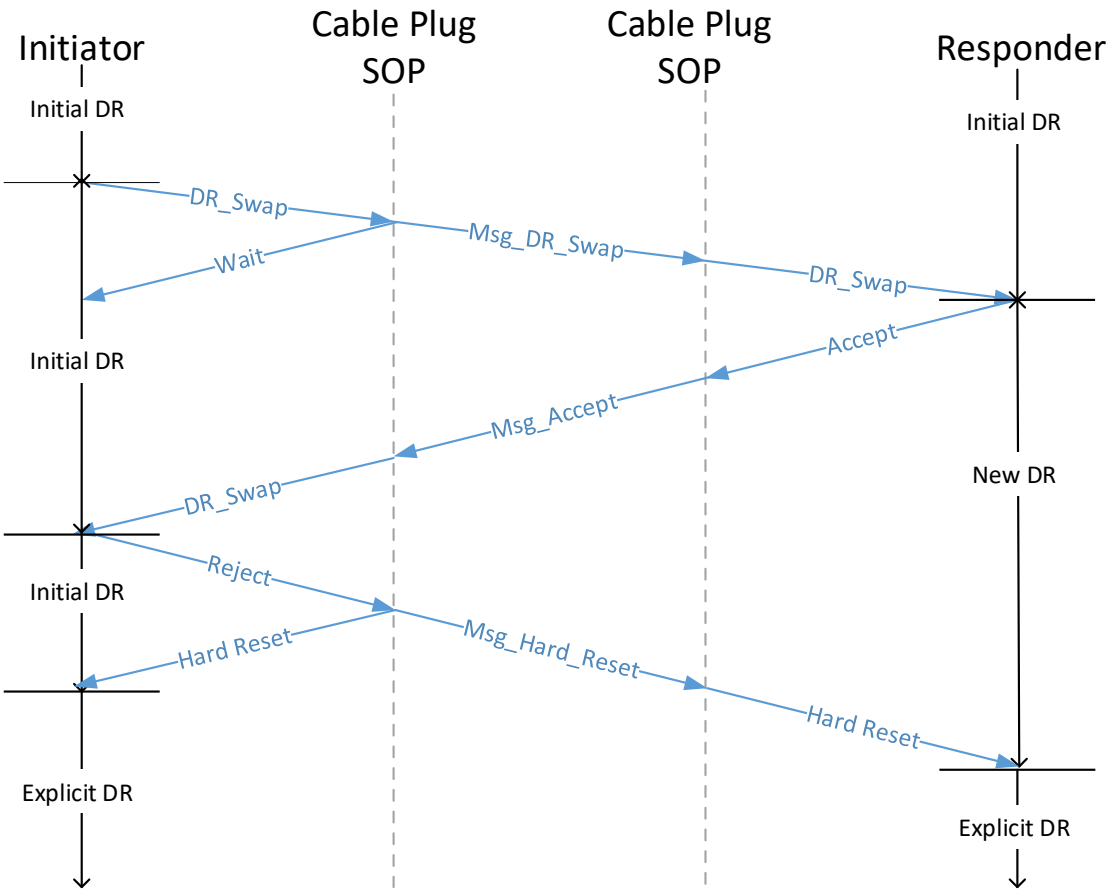
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-8 OIAC Initiator Reject Data Role Swap



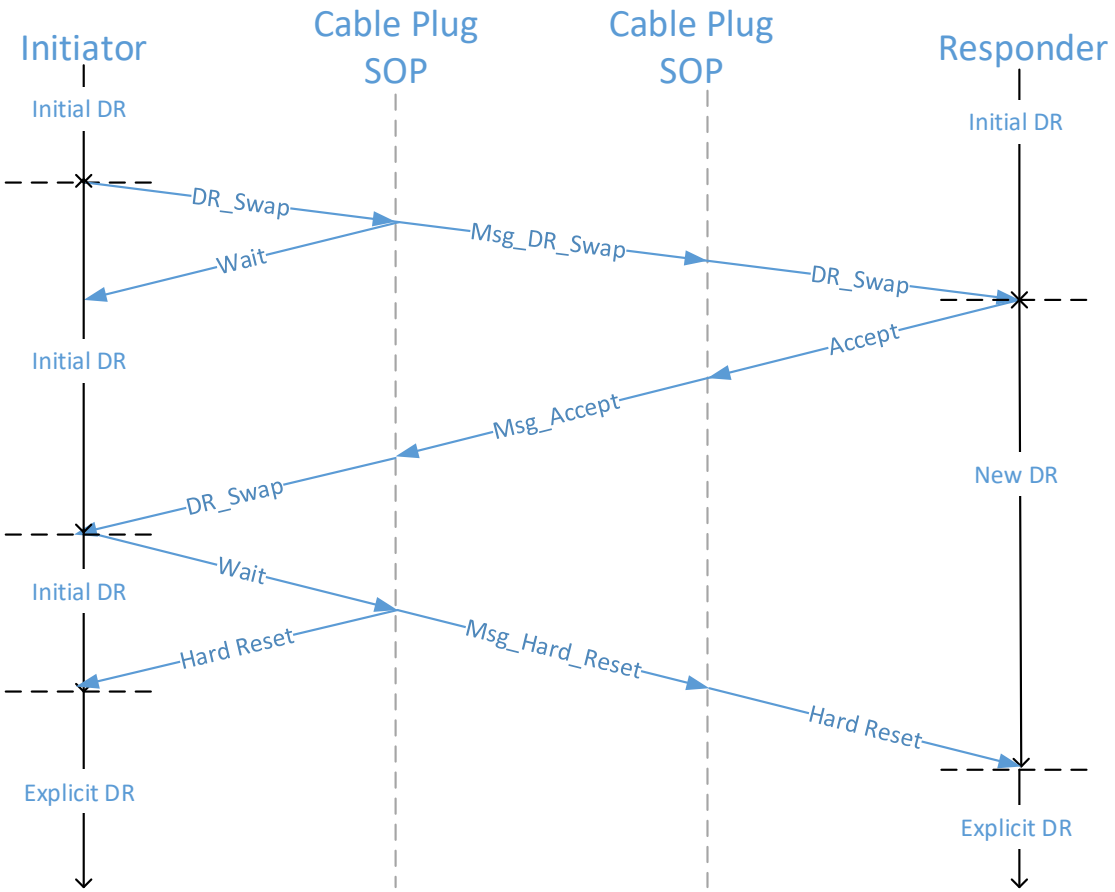
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-8 OIAC Initiator Reject Data Role Swap



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-9 OIAC Initiator Wait Data Role Swap



6.2.3 Short Active Cable Behaviors in Response to Power Delivery Events

Each cable plug of the short active cable shall be capable of communicating on SOP' and SOP" if reported in the Discover_Identity Command.

6.2.3.1 Data Role Swap

Short active cables are transparent to the *USB PD* Data Role swap.

6.2.3.2 Power Role Swap

Short active cables shall maintain *USB 3.2* signaling during a *USB PD* Power Role swap. The source of VCONN is not affected by a Power Role Swap.

6.2.3.3 VCONN Swap

Short active cables shall maintain *USB 3.2* signaling during a *USB PD* VCONN swap. During a VCONN Swap, the original VCONN Source continues to supply VCONN for some time after the new VCONN Source begins to supply VCONN. This ensures that VCONN is never dropped.

6.2.3.4 Fast Role Swap

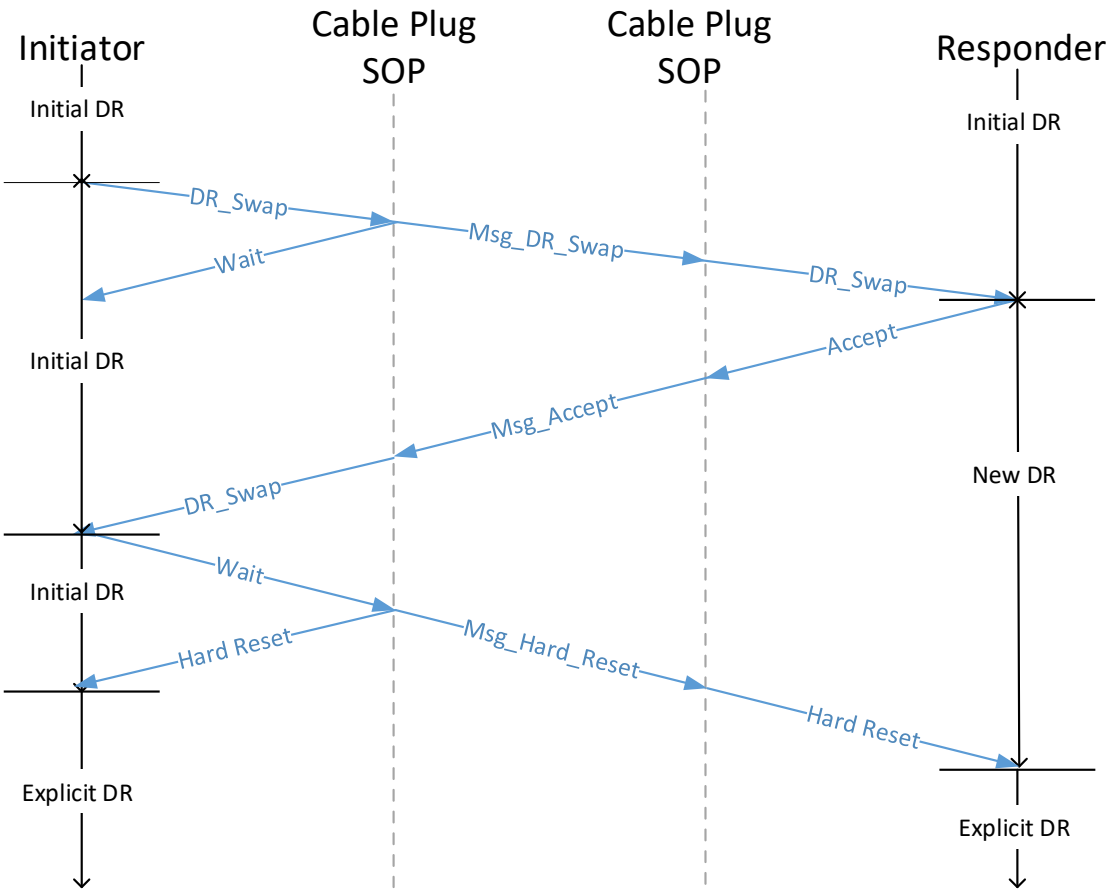
Short active cables will drop *USB 3.2* signaling as a side-effect of a Fast Role Swap if VCONN is not maintained during the Fast Role Swap.

6.3 OIAC Connection Flow and State Diagrams

This section defines the connection state diagrams for the OIAC.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-9 OIAC Initiator Wait Data Role Swap



6.2.3 响应电力输送事件的短有源电缆行为

如果在 Discover_Identity 命令中报告，短有源电缆的每个电缆插头都应能够在 SOP ’ 和 SOP ” 上进行通信。

6.2.3.1 数据角色转换

短有源电缆对于 *USB PD* 数据角色交换是透明的。

6.2.3.2 权力角色互换

短有源电缆应在 *USB PD* 电源角色交换期间保持 *USB 3.2* 信号。VCONN 源不受电源角色交换的影响。

6.2.3.3 VCONN 交换

在 *USB PD* VCONN 交换期间，短有源电缆应保持 *USB 3.2* 信号。在 VCONN 交换期间，在新的 VCONN 源开始提供 VCONN 后，原始 VCONN 源将继续提供 VCONN 一段时间。这可确保 VCONN 永远不会丢失。

6.2.3.4 快速角色交换

如果在快速角色交换期间未维持 VCONN，则短有源电缆将会丢失 *USB 3.2* 信号，这是快速角色交换的副作用。

6.3 OIAC 连接流程和状态图

本节定义了 OIAC 的连接状态图。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

OIAC plug defined at time of manufacture as either a Master or Slave for *USB PD* communication. This in no way indicates the plug has more or less capability, rather it allows for a consistent behavior when making the initial end to end connection.

The OIAC communicates using *USB PD* with its plug partners to determine the partner capabilities. The OIAC performs a series of connect/disconnects to establish the correct UFP/DFP data role for the cable plug. The possible combinations for Master Port, Slave Port, and cable plugs is defined in Table 6-8.

The connection and establishment of data roles is performed in three phases.

Table 6-8 Port and Plug Capabilities

Host/Device Port Capabilities	Cable Configuration		Host/Device Port Capabilities
	Master Plug Role	Slave Plug Role	
DRD	DFP	UFP	DRD
DFP	UFP	DFP	DRD
DRD	DFP	UFP	DFP
DFP	Billboard		DFP
Any	Billboard if possible		UFP
UFP	Billboard if possible		Any

6.3.1 OIAC Connection Flow – Discovery – Phase 1

The OIAC cable plugs discover the capabilities of their port partners in the Discovery Phase.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

OIAC 插头在制造时定义为 *USB PD* 通信的主插头或从插头。这绝不表示插头的功能更多或更少，而是允许在进行初始端到端连接时保持一致的行为。

OIAC 使用 *USB PD* 与其插头伙伴通信以确定伙伴功能。OIAC 执行一系列连接/断开操作，为电缆插头建立正确的 UFP/DFP 数据角色。主端口、从端口和电缆插头的可能组合定义在表 6-8 中。

数据角色的连接和建立分三个阶段进行。

表 6-8 端口和插头功能

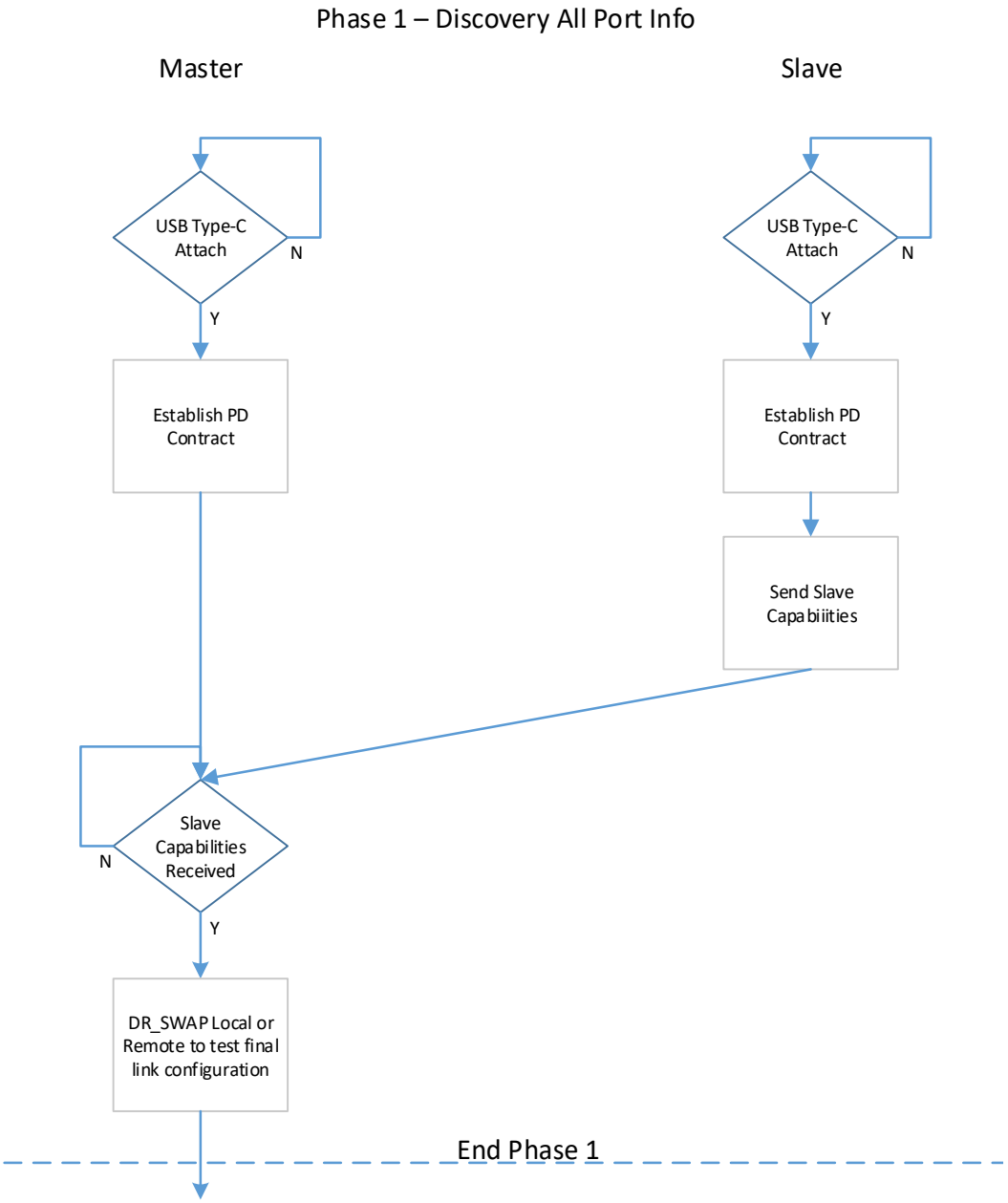
Host/Device Port Capabilities	Cable Configuration		Host/Device Port Capabilities
	Master Plug Role	Slave Plug Role	
DRD	DFP	UFP	DRD
DFP	UFP	DFP	DRD
DRD	DFP	UFP	DFP
DFP	Billboard		DFP
Any	Billboard if possible		UFP
UFP	Billboard if possible		Any

6.3.1 OIAC 连接流程 – 发现 – 第 1 阶段

OIAC 电缆插头在发现阶段发现其端口伙伴的功能。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-10 OIAC Discovery – Phase 1



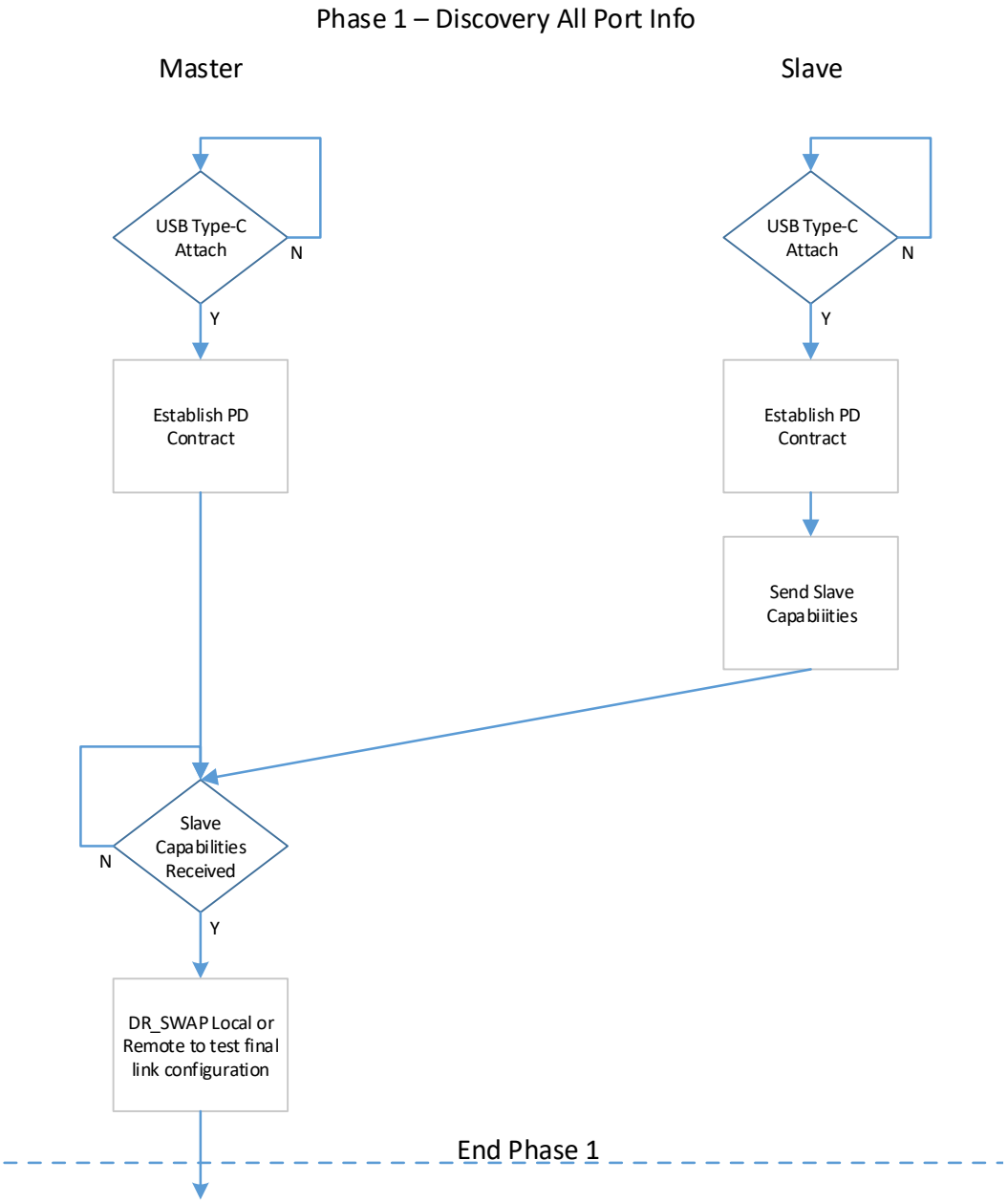
6.3.2 OIAC Connection Flow – Reboot – Phase 2

The OIAC cable plugs forward the capabilities of their plug partners and perform disconnect/reconnect.

- Master will always start with repeating sending "MSG_Cable_Config" to slave to start reboot.
- Slave Reboot.
- Slave sees "MSG_Cable_Config" and holds off on SourceCap GoodCRC until it is allowed to release it.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-10 OIAC Discovery – Phase 1



6.3.2 OIAC 连接流程 – 重启 – 第 2 阶段

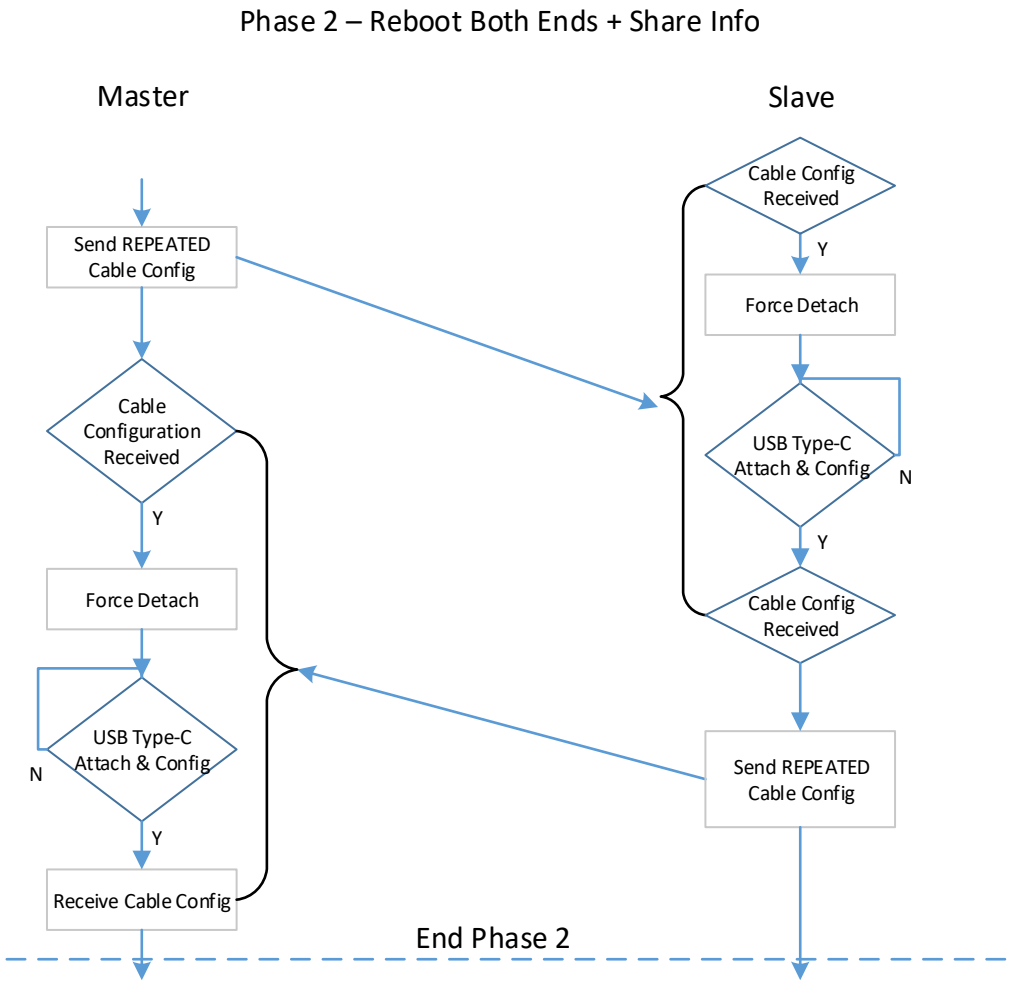
OIAC 电缆插头转发其插头伙伴的功能并执行断开/重新连接。

- 主机将始终重复向从机发送 " MSG_Cable_Config " 以开始重启。• 从机重启。• 从机看到 " MSG_Cable_Config " 并推迟 SourceCap Good CRC，直到允许释放它。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- Slave send "MSG_Cable_Config" to the master.
- Master Reboots.
- Master see "MSG_Cable_Config" and holds off on SourceCap GoodCRC until it is allowed to release it.

Figure 6-11 OIAC Reboot – Phase 2



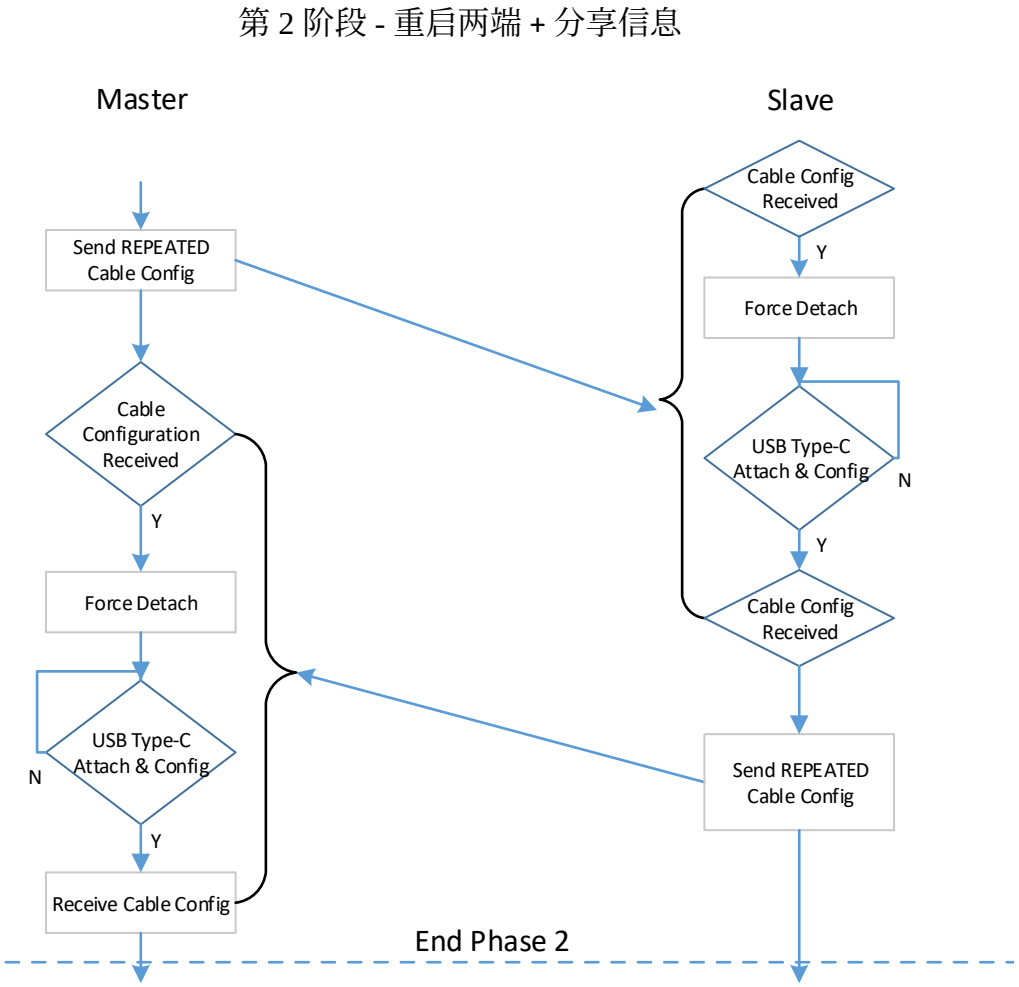
6.3.3 OIAC Connection Flow – Configuration – Phase 3

The OIAC master plug determines DFP/UFP roles for the master and slave plugs. The master release the PLUG to be configured as the DFP and initiates a DR_Swap. The side that issues the DR_Swap send a DR_Swap and releases the other side SourceCap GoodCRC.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• 从属设备向主设备发送 “ MSG_Cable_Config ”。• 主设备重新启动。• 主设备看到 “ MSG_Cable_Config ” 并推迟 SourceCap GoodCRC，直到允许其释放它。

图 6-11 OIAC 重启 – 第 2 阶段



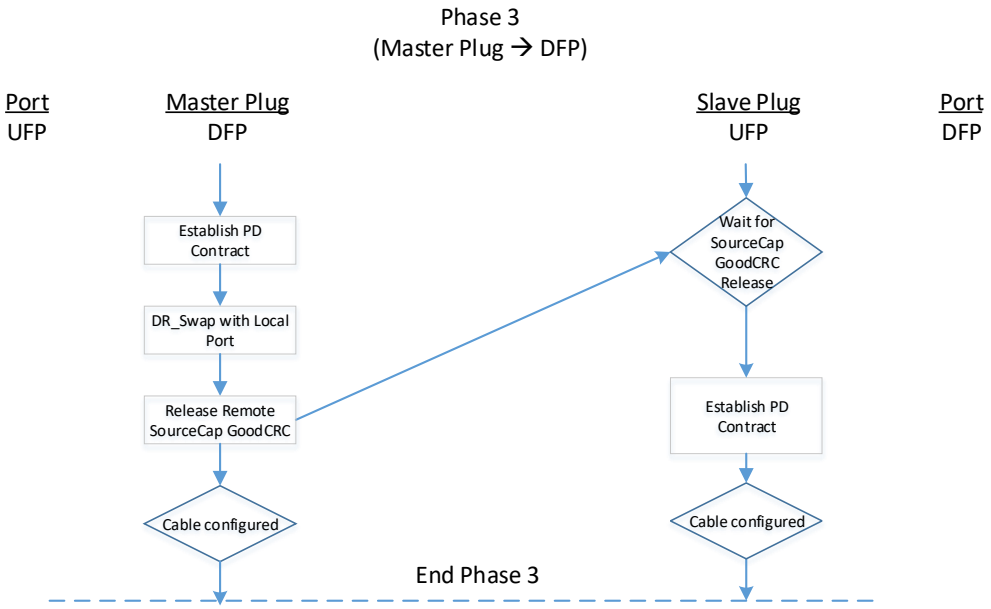
6.3.3 OIAC 连接流程 – 配置 – 阶段 3

OIAC 主插头确定主插头和从插头的 DFP/UFP 角色。主插头释放 PLUG 以配置为 DFP，并发起 DR_Swap。发出 DR_Swap 的一方发送 DR_Swap 并释放另一方 SourceCap GoodCRC。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-12 OIAC Master Plug Configure as DFP – Phase 3

Host/Device Port		Cable			Host/Device Port
		Master Plug	Slave Plug		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any

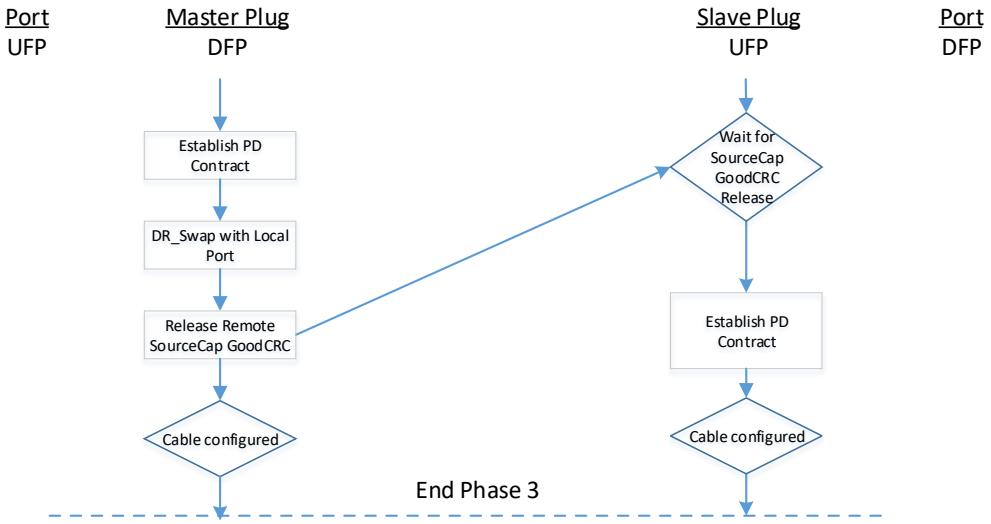


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 6-12 OIAC 主插头配置为 DFP – 阶段 3

Host/Device Port		Cable			Host/Device Port
		Master Plug	Slave Plug		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any

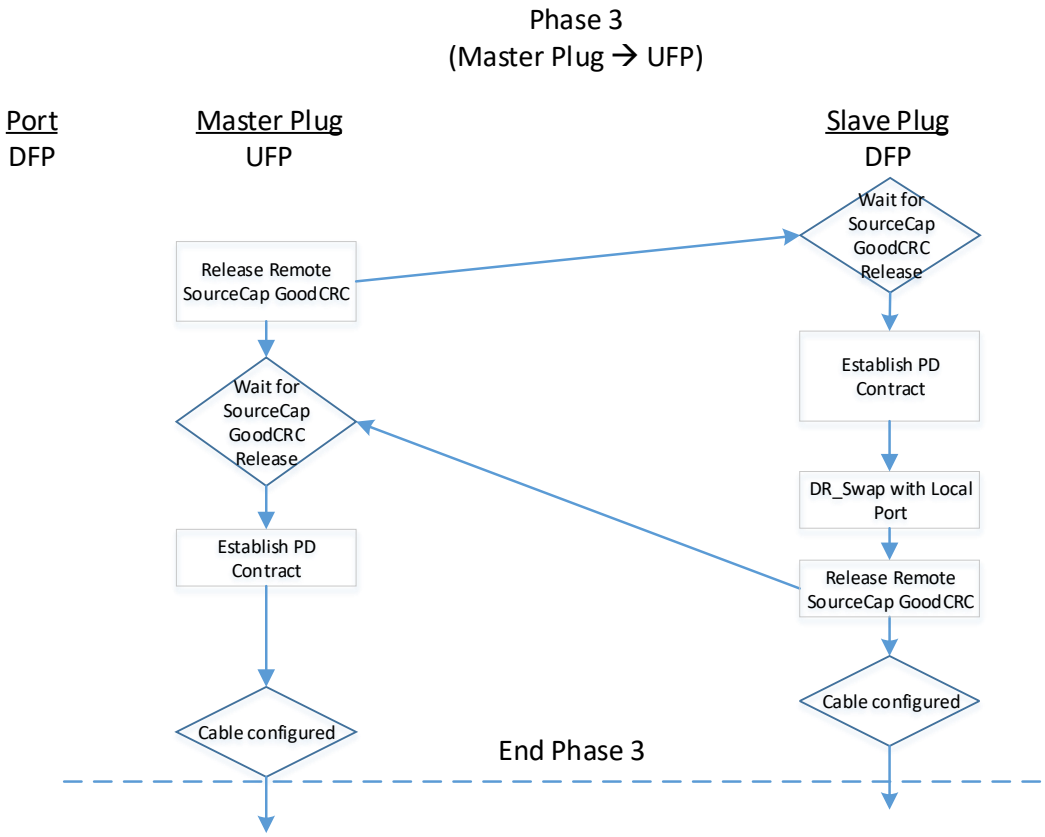
阶段 3（主插头 → DFP）



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-13 OIAC Master Plug Configure as UFP – Phase 3

Host/Device Port		Cable			Host/Device Port
		Master Plug	Slave Plug		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any

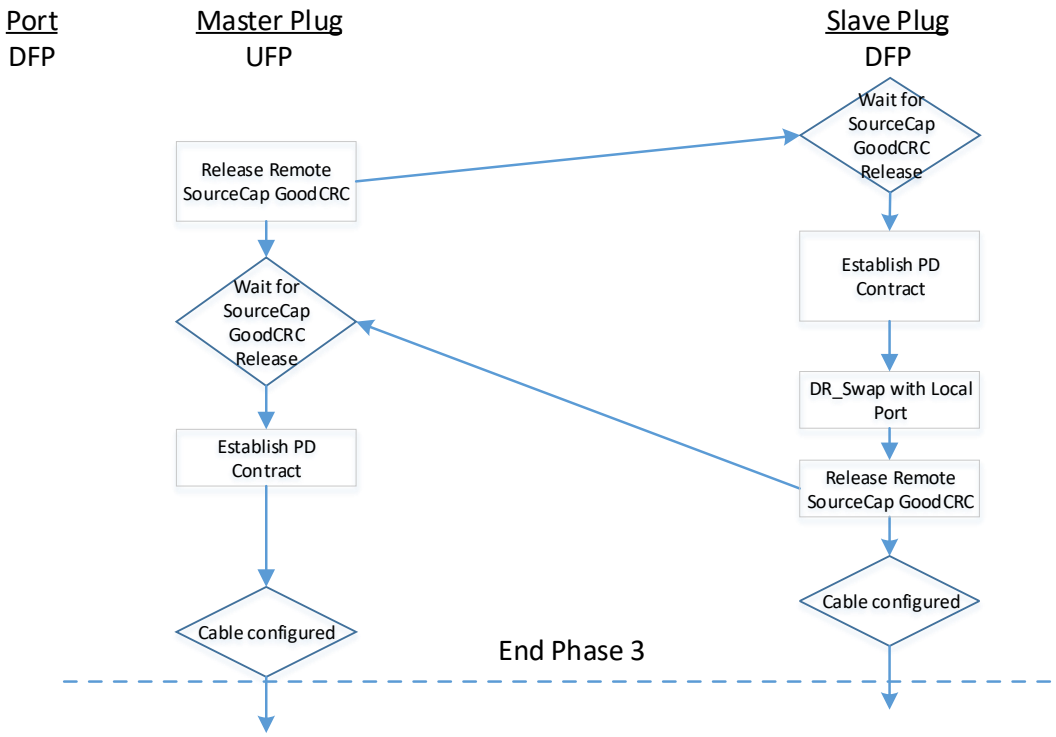


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 6-13 OIAC 主插头配置为 UFP – 第 3 阶段

Host/Device Port		Cable			Host/Device Port
		Master Plug	Slave Plug		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any

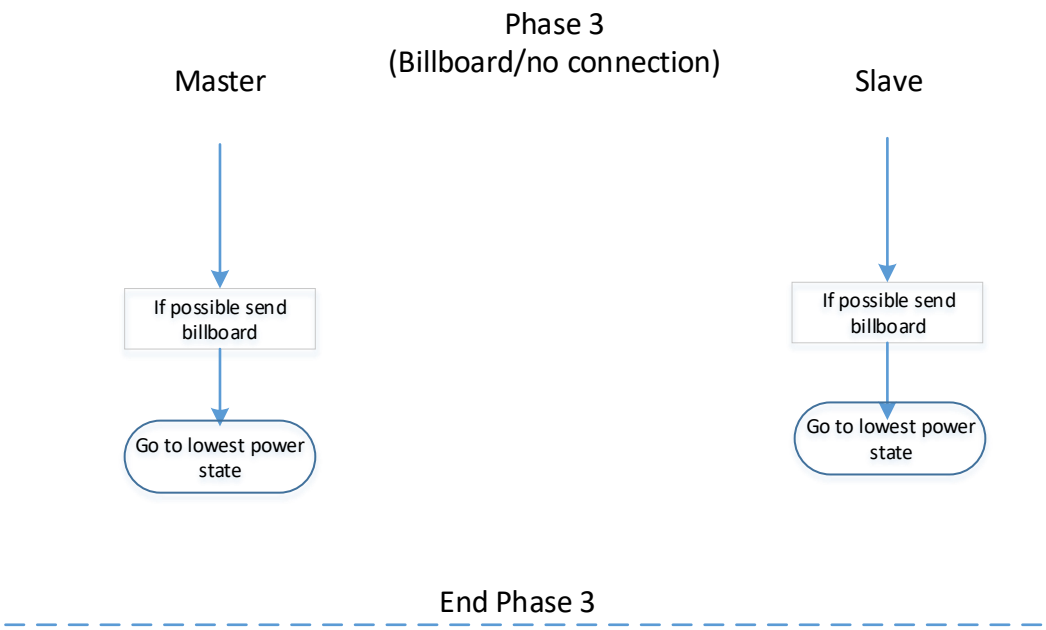
阶段 3（主插头 → UFP）



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-14 OIAC Master Plug No Connection Possible Billboard – Phase 3

Host/Device Port		Cable			Host/Device Port
		Master Plug	Slave Plug		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any



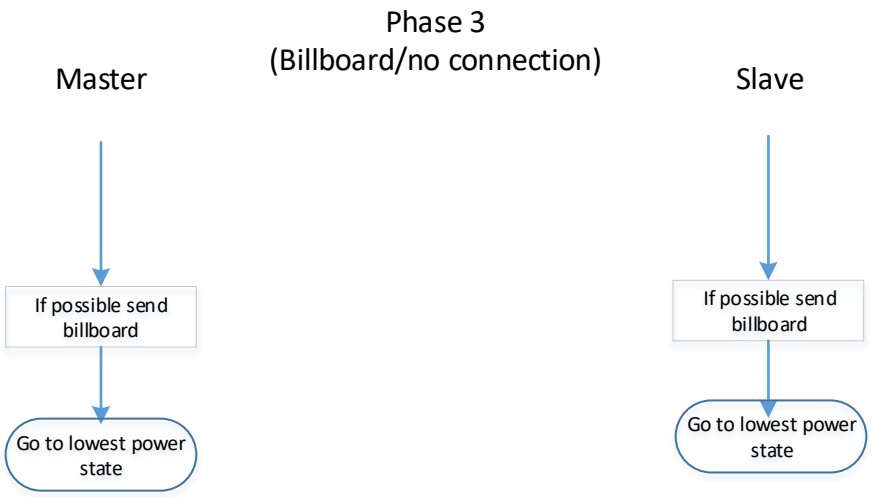
6.3.4 OIAC Connection State Diagram Master

The following sections details a possible OIAC state diagram for the Master Plug.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 6-14 OIAC 主插头无法连接广告牌 – 第 3 阶段

Host/Device Port		Cable			Host/Device Port
		Master Plug	Slave Plug		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any



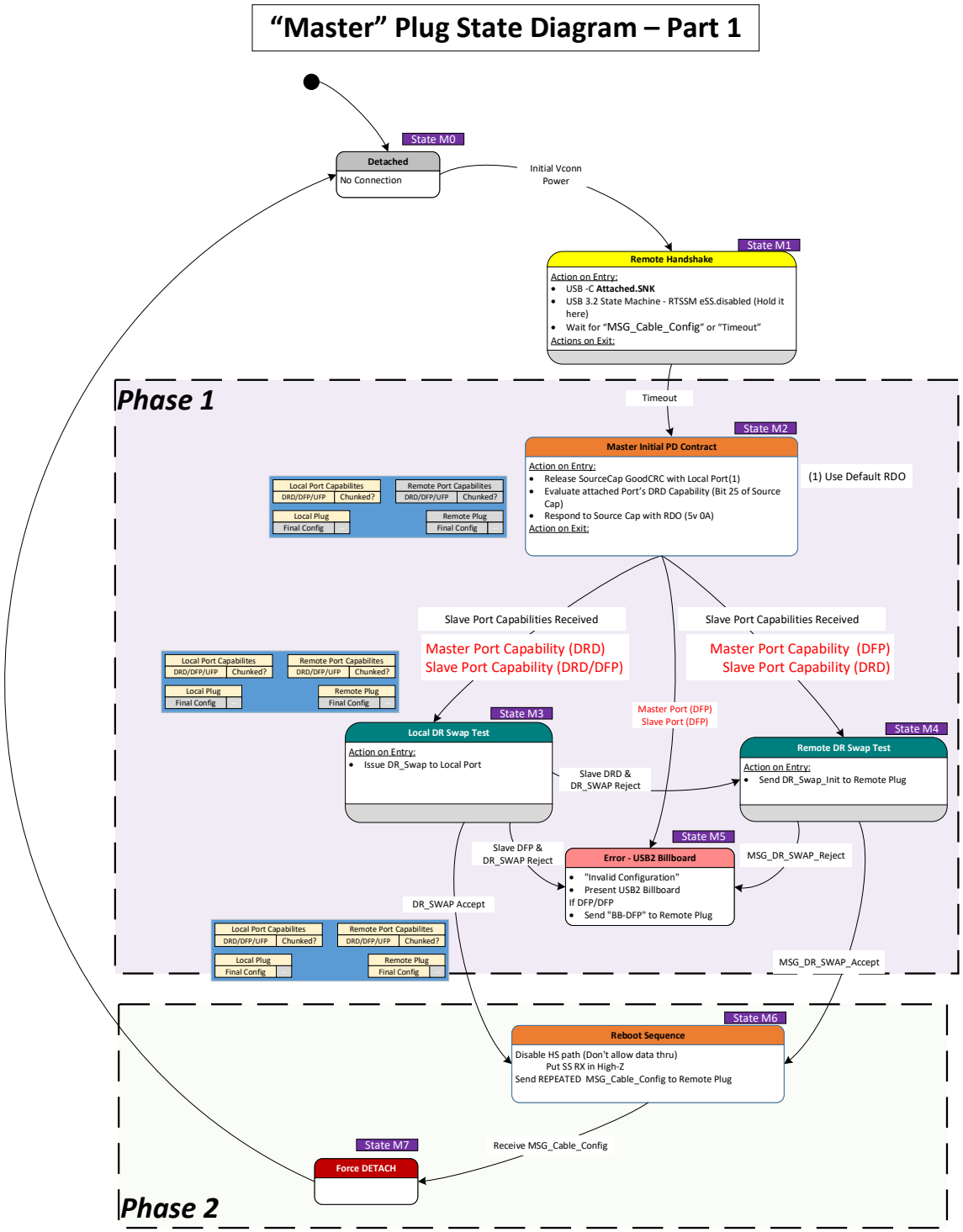
End Phase 3

6.3.4 OIAC连接状态图主机

以下 章节详细介绍了 M 的可能 OIAC 状态图 紫苑花插头。

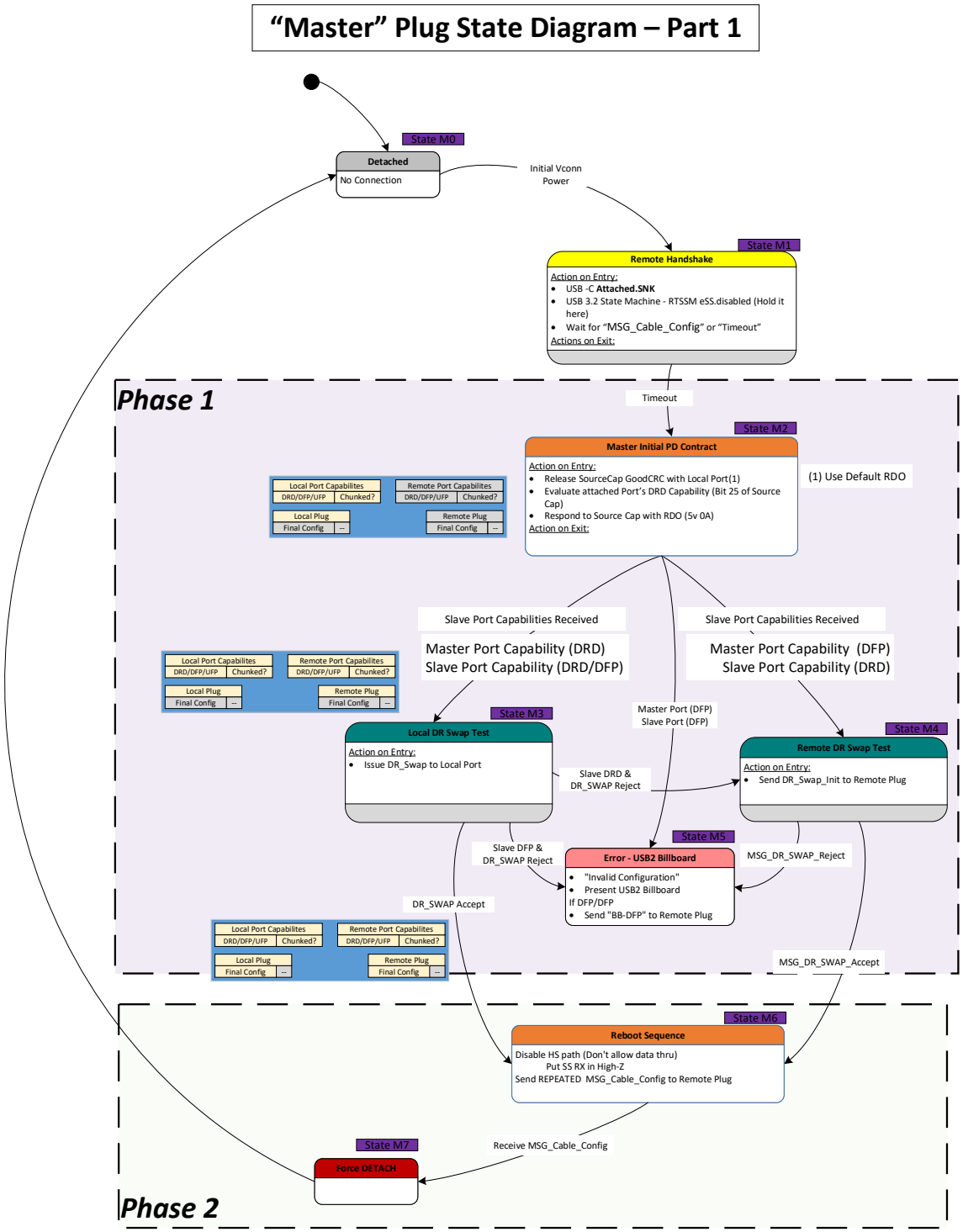
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-15 OIAC Master Plug State Diagram Part 1 (Phase 1 and 2)



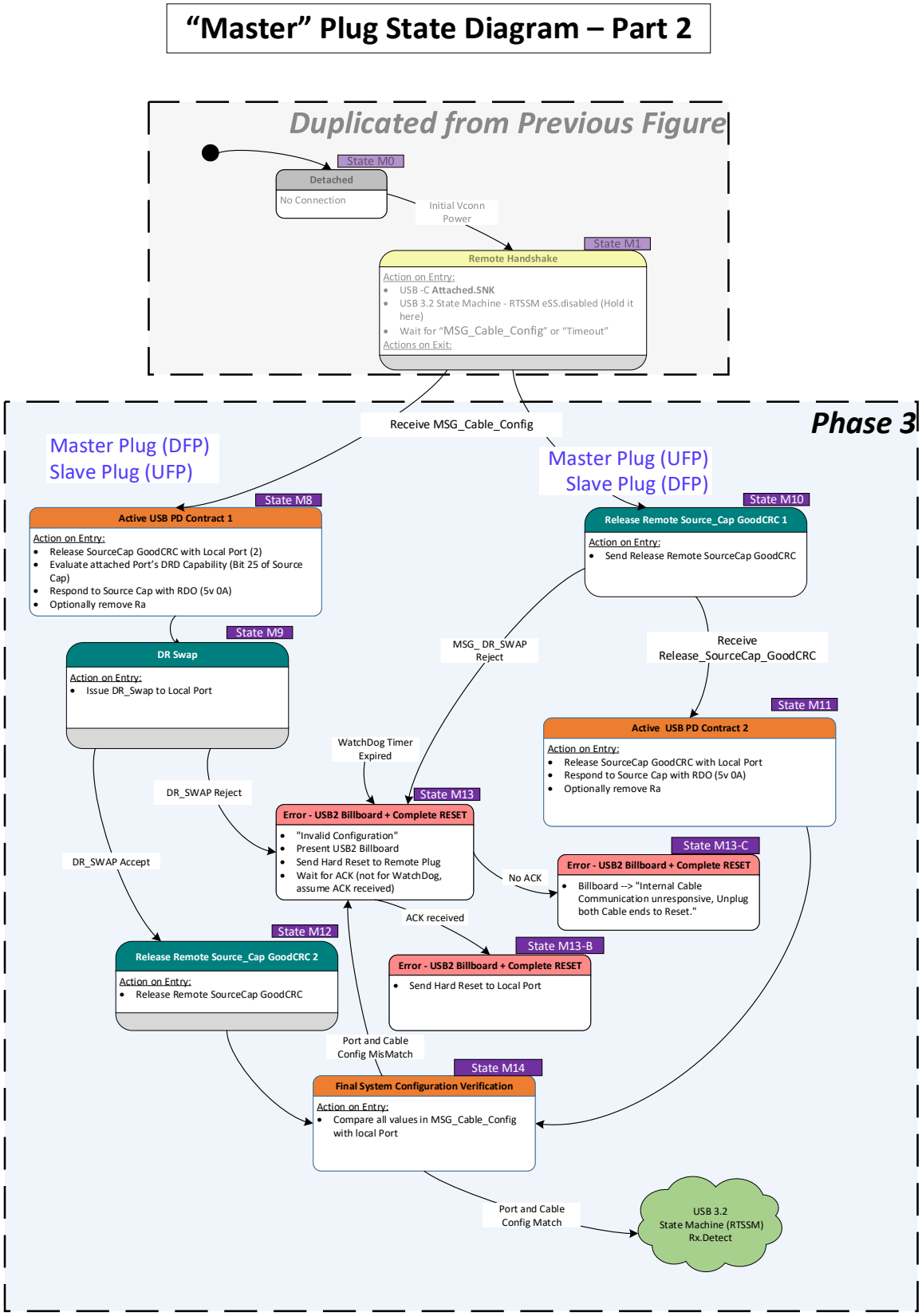
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 6-15 OIAC 主插头状态图第 1 部分（第 1 阶段和第 2 阶段）



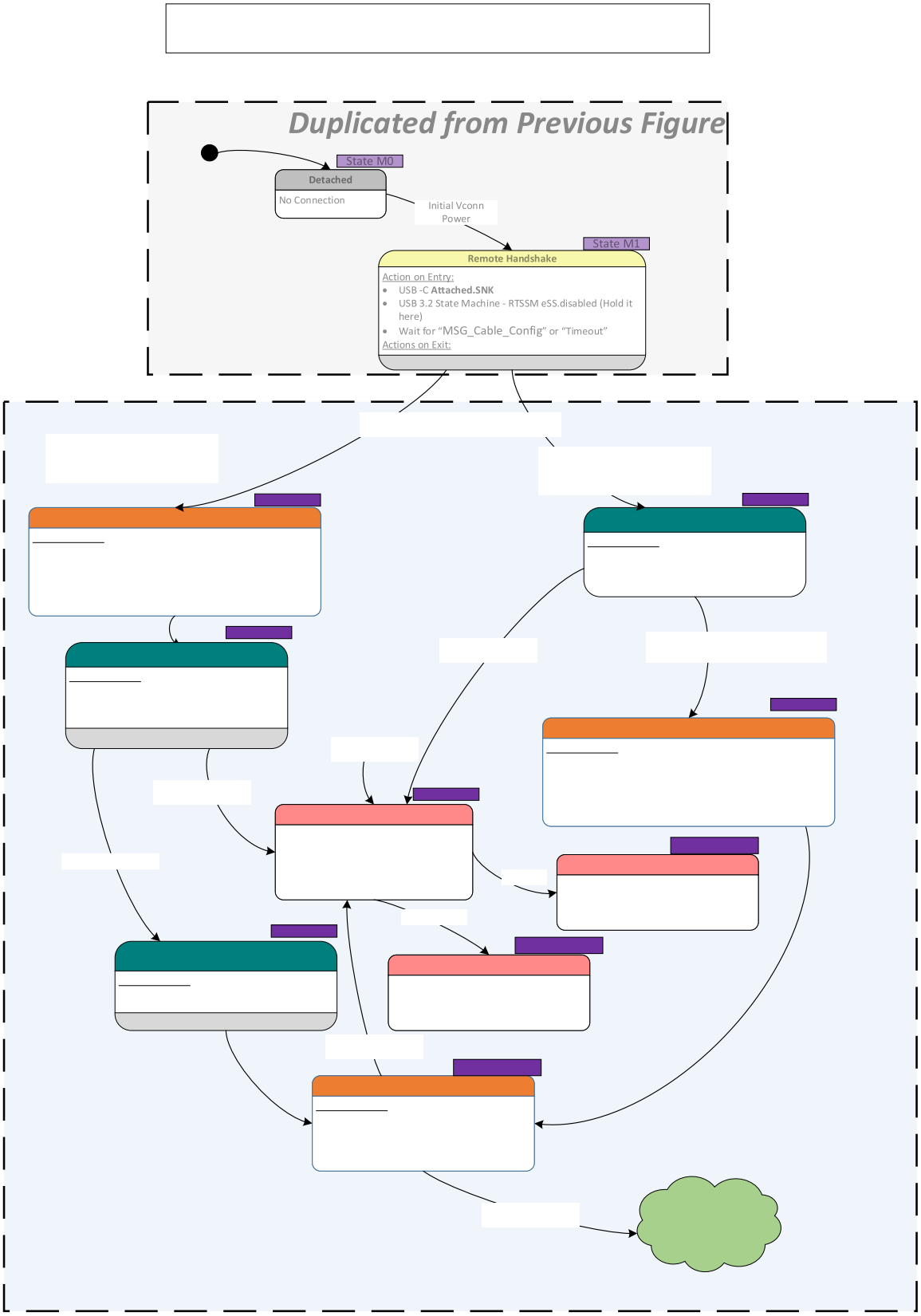
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-16 OIAC Master Plug State Diagram Part 2 (Phase 3)



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 6-16 OIAC 主插头状态图第 2 部分（第 3 阶段）



版权所有 © 2019 USB 3.0 Promoter Group。保留所有权利。

6.3.4.1 Detached State (M0)

The plug is in ***Detached*** (M0) when no power is applied. The plug transitions to ***Remote Handshake*** (M1) when VCONN is applied.

6.3.4.2 Remote Handshake State (M1)

The plug is waiting for the "Timeout" timer expiration or a "MSG_Cable_Config" message from the slave plug.

Recommended Timeout time = ~100ms

The Timeout time is dependent on the duty cycle of the Slave Plug's Repeat Port Capabilities messages and the maximum cable latency.

The plug starts in the *USB 3.2* RTSSM eSS.Disabled and remains in eSS.Disabled until cable initialization is complete at the end of Phase 3.

6.3.4.2.1 Entry to Remote Handshake

The plug enters Attached.SNK followed by entry to ***Remote Handshake*** (M1).

6.3.4.2.2 Exit from Remote Handshake

The plug transitions to:

- ***Master Initial PD Contract*** (M2) when the "Timeout" timer has expired,
- ***Active USB PD Contract 1*** (M8) upon receipt of a "MSG_Cable_Config" message when the Master Plug resolves to a DFP and the Slave Plug will resolve to a UFP, or
- ***Release Remote Source_Cap GoodCRC 1*** (M10) upon receipt of a "MSG_Cable_Config" message when the Master Plug resolves to a UFP and the Slave Plug will resolve to a DFP.

6.3.4.3 Master Initial PD Contract State (M2)

When the plug is in ***Master Initial PD Contract***, the plug has established an initial *USB PD* contract and evaluated its local port's DRD capability.

6.3.4.3.1 Entry to Master Initial DP Contract

On Entry to ***Master Initial PD Contract***, the plug shall:

1. Send a GoodCRC in response to a Source Capabilities message from the local attached port
2. Evaluate the local attached port's DRD capability (Bit 25 of the Source Capabilities message)
3. Respond to the Source Capabilities message with the "default" RDO specified in Table 6-10.

6.3.4.3.2 Exit from Master Initial DP Contract

The OIAC plug shall transition to:

- ***Local DR Swap Test*** (M3) upon receipt of a MSG_Port_Capabilities where the Master Port is a DRD and the Slave Port is either a DRD or DFP,
- ***Remote DR Swap Test*** (M4) upon receipt of a MSG_Port_Capabilities where the Master Port is a DFP and the Slave Port is DRD, or

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.4.1 分离状态（M0）

未通电时，插头处于 ***Detached*** (M0)。通电后，插头转换至 ***Remote Handshake*** (M1)。

6.3.4.2 远程握手状态（M1）

插头正在等待“ 超时 ”计时器到期或来自从属插头的“ MSG_Cable_Config ”消息。

建议超时时间= ~100ms

超时时间取决于从属插头的重复端口功能消息的占空比和最大电缆延迟。

插头从 *USB 3.2* RTSSM eSS.Disabled 开始，并保持在 eSS.Disabled 状态，直到第 3 阶段结束时电缆初始化完成。

6.3.4.2.1 进入远程握手

插头进入 Attached.SNK，然后进入 ***Remote Handshake***（M1）。

6.3.4.2.2 退出远程握手

插头转换至：

- ***Master Initial PD Contract*** (M2) 当“ 超时 ”计时器到期时，• ***Active USB PD Contract 1*** (M8) 当主插头解析为 DFP 且从属插头将解析为 UFP 时收到“ MSG_Cable_Config ”消息时，或
- ***Release Remote Source_Cap GoodCRC 1*** (M10) 当收到“ MSG_Cable_Config ”消息时

当主插头解析为 UFP 并且从属插头解析为 DFP 时，会显示消息。

6.3.4.3 主初始 PD 合约状态（M2）

当插头处于***Master Initial PD Contract***状态时，该插头已经建立了初始*USB PD*合同并评估了其本地端口的DRD能力。

6.3.4.3.1 进入初始DP主合同

进入 ***Master Initial PD Contract*** 时，插头应：

1. 发送 GoodCRC 以响应来自本地连接端口的源功能消息 2. 评估本地连接端口的 DRD 功能（源功能消息的第 25 位） 3. 使用表 6-10 中指定的“ 默认 ”RDO 响应源功能消息。

6.3.4.3.2 退出初始DP主合同

OIAC 插头应过渡至：

- ***Local DR Swap Test*** （M3）收到 MSG_Port_Capabilities 后，其中主端口为 DRD 且从属端口为 DRD 或 DFP，• ***Remote DR Swap Test*** （M4）收到 MSG_Port_Capabilities 后，其中主端口为 DFP 且从属端口为 DRD，或者

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- ***Error – USB2 Billboard*** (M5) upon determination both Master and Slave plugs are connected to DFPs.

6.3.4.4 Local DR Swap Test State (M3)

The ***Local DR Swap Test*** is a test to ensure that the Master Port that is defined as a DRD will accept a DR_Swap request.

6.3.4.4.1 Entry to Local DR Swap Test

On entry to ***Local DR Swap Test***, the plug shall issue DR_Swap request to its local port.

If the local port responds to the DR Swap with "Wait," then the plug shall follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state ***Error – USB2 Billboard*** (M5).

6.3.4.4.2 Exit from Local DR Swap Test

The OIAC plug shall transition to:

- ***Remote DR Swap Test*** (M4) upon receipt of a Reject and the Slave port reported that it is a DRD,
- ***Error – USB2 Billboard*** (M5) upon receipt of a Reject and the Slave port reported that it is a DFP, or
- ***Reboot Sequence*** (M6) upon receipt of an Accept.

6.3.4.5 Remote DR Swap Test State (M4)

The ***Remote DR Swap Test*** is a test to ensure that the Slave Port that is defined as a DRD will accept a DR_Swap request.

6.3.4.5.1 Entry to Remote DR Swap Test

On entry to ***Remote DR Swap Test***, the plug shall issue a DR_Swap_Init to the remote plug.

6.3.4.5.2 Exit from Remote DR Swap Test

The OIAC plug shall transition to:

- ***Reboot Sequence*** (M6) upon receipt of a MSG_DR_Swap_Accept, or
- ***Error – USB2 Billboard*** (M5) upon receipt of a MSG_DR_Swap_Reject.

6.3.4.6 Error – USB2 Billboard (M5)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: A DFP only device connected to one of the plugs."

6.3.4.6.1 Entry to Error – USB2 Billboard

On entry ***Error – USB2 Billboard***, the plug shall issue present a Billboard message over *USB 2.0* and then power down to its lowest possible state.

6.3.4.6.2 Exit from Error – USB2 Billboard

The only means of exiting this Error state, is either from a Reset that disconnects V_{CONN} power or a disconnect event which also disconnects V_{CONN} power.

6.3.4.7 Reboot Sequence State (M6)

When the plug is in the ***Reboot Sequence***, it will disable the High Speed Data path and start to initiate a remote plug reboot.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- ***Error – USB2 Billboard***（M5）确定主插头和从插头均已连接到 DFP。

6.3.4.4 本地 DR 交换测试状态（M3）

Local DR Swap Test 是一个测试，用于确保定义为 DRD 的主端口将接受 DR_Swap 请求。

6.3.4.4.1 进入本地 DR 交换测试

进入 ***Local DR Swap Test*** 时，插头应向其本地端口发出 DR_Swap 请求。

如果本地端口以“等待”响应 DR 交换，则插头应遵循 tDRSwapWait 计时器并重试最多 3 次，之后它将出错并转换到状态 ***Error – USB2 Billboard***（M5）。

6.3.4.4.2 退出本地 DR 交换测试

OIAC 插头应过渡至：

- ***Remote DR Swap Test***（M4）收到拒绝后，从端口报告它是一个 DRD，在收到拒绝后，• ***Error – USB2 Billboard***（M5）并且从端口报告它是一个 DFP，或者在收到接受后，• ***Reboot Sequence***（M6）。

6.3.4.5 远程 DR 交换测试状态（M4）

Remote DR Swap Test 是一个测试，用于确保定义为 DRD 的从属端口将接受 DR_Swap 请求。

6.3.4.5.1 进入远程 DR 交换测试

进入 ***Remote D R Swap Test***，插头应向 t 发出 DR_Swap_Init 遥控插头。

6.3.4.5.2 退出远程 DR 交换测试

OIAC 插头应过渡至：

收到 MSG_DR_Swap_Accept 后，• ***Reboot Sequence***（M6），或收到 MSG_D R_Swap_Reject 后，• ***Error – USB2 Billboard***（M5）。

6.3.4.6 错误 – USB2 广告牌 (M5)

插头上会显示一个公告牌，表明存在无效配置。例如：“错误：一个仅限 DFP 的设备连接到其中一个插头。”

6.3.4.6.1 进入错误 – USB2 公告牌

在进入 ***Error – USB2 Billboard*** 时，插头应通过 *USB 2.0* 发出广告牌消息，然后关闭电源至~~最低可能~~状态。

6.3.4.6.2 退出错误 – USB2 广告牌

退出此错误状态的唯一方法是通过重置断开 V CONN 电源，或者通过断开事件也断开 VCONN 电源。

6.3.4.7 重启序列状态（M6）

当插头位于 ***Reboot Sequence*** 时，它将禁用高速数据路径并开始启动远程插头重启。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.4.7.1 Entry to Reboot Sequence

On entry to Reboot Sequence, the plug shall:

1) Disable the HS path by changing the SS RX termination to High-Z;
2) Determine and store the final System Configuration for this link.
    a. The System Configuration will contain:
        i. Host/Device Port information
        ii. Final Master/Slave Plug roles
            1. If coming from State M3
                a. Master Plug → DFP (DR_Swap)
                b. Slave Plug → UFP
            2. If coming from State M4
                a. Master Plug → UFP
                b. Slave Plug → DFP (DR_Swap)
            3. If coming from State M9
                a. Master Plug → UFP
                b. Slave Plug → DFP (DR_Swap)
3) Continuously send "MSG_Cable_Config" message to the remote plug.

6.3.4.7.2 Exit from Reboot Sequence

The OIAC plug shall transition to the ***Force Detach*** (M7) when a "MSG_Cable_Config" message is received that matches the final configuration that the Master Plug sent to the Slave Plug.

6.3.4.8 Force Detach State (M7)

The plug shall transition to SRC.Open on both CC and VCONN and maintain this state for at least tSRCDisconnect.

6.3.4.8.1 Entry to Force Detach

On entry to ***Force Detach***, the plug shall raise the voltage on the CC-wire above vRd-Connect.

6.3.4.8.2 Exit from Force Detach

The plug transitions to ***Detached*** upon exit from ***Force Detach***.

6.3.4.9 Active USB PD Contract 1 State (M8)

Active USB Contract 1 is where OIAC Master Plug creates at *USB PD* contract with the local port.

6.3.4.9.1 Entry to Active USB PD Contract 1

The OIAC plug shall follow the steps listed below:

1. Begin responding to *USB PD* messages from its port partner with GoodCRCs.
2. Evaluate b25 in the Fixed 5V PDO in the Source Capabilities message to check if its port partner is a DRD.
3. Request for a 5 V @ 0 A power contract.
4. May remove Ra to save power.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.4.7.1 进入重启序列

进入重启序列时，插头应：

1) 通过将 SS RX 终端更改为 High-Z 来禁用 HS 路径；

2) 确定并存储此链路的最终系统配置。a. 系统配置将包含：i. 主机/设备端口信息 ii. 最终主/从插头角色 1. 如果来自状态 M3 a. 主插头 → DFP（DR_Swap）b. 从插头 → UFP 2. 如果来自状态 M4 a. 主插头 → UFP b. 从插头 → DFP（DR_Swap）3. 如果来自状态 M9 a. 主插头 → UFP b. 从插头 → DFP（DR_Swap）

3）连续发送“ MSG_Cable_Config ”消息到远程插头。

6.3.4.7.2 退出重启顺序

当收到与主插头发送给从属插头的最终配置匹配的“ MSG_Cable_Config ”消息时，OIAC 插头应转换到 ***Force Detach*** (M7)。

6.3.4.8 强制分离状态（M7）

插头应在 CC 和 VCONN 上转换至 SRC.Open，并维持此状态至少 tSRCDisconnect。

6.3.4.8.1 进入强制分离

进入 ***Force Detach*** 时，插头应将 CC 线上的电压升高至 vRd-Connect 以上。

6.3.4.8.2 退出强制分离

当从 ***Force Detach*** 退出时，插头转换到 ***Detached***。

6.3.4.9 活动 USB PD 收缩 1 状态（M8）

Active USB Contract 1 是 OIAC Master Plug 在 *USB PD* 与本地端口创建合约的地方。

6.3.4.9.1 进入主动 USB PD 契约 1

OIAC 插头应遵循以下步骤：

1. 开始使用 GoodCRC 响应来自其端口伙伴的 *USB PD* 消息。2. 评估源功能消息中固定 5V PDO 中的 b25，以检查其端口伙伴是否为 DRD。3. 请求 5 V @ 0 A 电源合同。4. 可以移除 Ra 以节省电量。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.4.9.2 Exit from Active USB PD Contract 1

The plug transitions to the ***DR Swap*** (M9) when it receives an Accept followed by a PS_RDY message from its port partner.

6.3.4.10 DR Swap State (M9)

The ***DR Swap*** is used to set the final data role of the OIAC's Master Plug and signal to the OIAC Slave Plug to complete its configuration.

6.3.4.10.1 Entry to DR Swap

The OIAC plug shall issue a DR_Swap to its port partner.

If the local port responds to the DR_Swap with "Wait," then the plug shall follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state ***Error – USB2 Billboard*** (M5).

6.3.4.10.2 Exit from DR Swap

If the DR_Swap message is responded to with:

- An Accept, it shall transition to the ***Release Remote Source_Cap GoodCRC 2 State*** (M12), or
- A Reject it shall transition to the ***Error - USB2 Billboard + Complete Reset*** (M13).

6.3.4.11 Release Remote Source_Cap GoodCRC 1 State (M10)

The OIAC is waiting to for Release_Remote_Source_Cap_GoodCRC to better synchronize the power on of the two OIAC plug ends.

6.3.4.11.1 Entry to Release Remote Source_Cap GoodCRC 1

The OIAC plug shall release the Remote SourceCap GoodCRC.

6.3.4.11.2 Exit from Release Remote Source_Cap GoodCRC 1

The OIAC plug shall transition to:

- ***Active USB PD Contract 2 State*** (M11), when a "MSG_ Release_Remote_SourceCap_GoodCRC" message is received, or
- ***Error – USB2 Billboard + Complete Reset*** (M13) upon receipt of a MSG_DR_Swap_Reject.

6.3.4.12 Active USB PD Contract 2 State (M11)

Active USB Contract 2 is where OIAC Master Plug creates at *USB PD* contract with the local port and should end with viable link.

6.3.4.12.1 Entry to Active USB PD Contract 2

The OIAC plug shall follow the steps listed below:

1. Begin responding to USB PD messages from its port partner with GoodCRCs.
2. Request a 5 V @ 0 A power contract.
3. May remove Ra to save power.

6.3.4.12.2 Exit from Active USB PD Contract 2

The plug shall transition to ***Final System Configuration Verification*** (M13) for final system verification.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.4.9.2 退出活动 USB PD 契约 1

当插头从其端口伙伴处收到一个 Accept 消息并且随后收到 PS_RDY 消息时，插头转换到 ***DR Swap*** (M9)。

6.3.4.10 DR 交换状态（M9）

DR Swap用于设置 OIAC 主插头的最终数据角色，并向 OIAC 从属插头发出信号以完成其配置。

6.3.4.10.1 进入 DR 互换

OIAC 插头应向其端口伙伴发出 DR_Swap 呃。

如果本地端口以“等待”响应 DR_Swap，则插头应遵循 tDRSwapWait 计时器并重试最多 3 次，之后它将出错并转换到状态 ***Error – USB2 Billboard***（M5）。

6.3.4.10.2 退出 DR 交换

如果 DR_Swap 消息的响应为：

- 如果是接受，则应转换至 ***Release Remote Source_Cap GoodCRC 2 State***（M12），或
- 如果是拒绝，则应转换至 ***Error - USB2 Billboard + Complete Reset***（M13）。

6.3.4.11 释放远程 Source_Cap GoodCRC 1 状态 (M10)

OIAC 正在等待 Release_Remote_Source_Cap_GoodCRC 以更好地同步两个 OIAC 插头端的电源开启。

6.3.4.11.1 进入释放远程 Source_Cap GoodCRC 1

OIAC 插头应释放 Remote SourceCap GoodCRC。

6.3.4.11.2 退出释放远程 Source_Cap GoodCRC 1

OIAC 插头应过渡至：

- ***Active USB PD Contract 2 State*** (M11)，当收到“MSG_ Release_Remote _SourceCap_GoodCRC”消息时，或
- ***Error – USB2 Billboard + Complete Reset*** (M13) 收到 MSG_DR_Swap_Reject 时。

6.3.4.12 活动 USB PD 合同 2 状态（M11）

Active USB Contract 2 是 OIAC Master Plug 在 *USB PD* 与本地端口创建合约的地方，并且应该以可行链接结束。

6.3.4.12.1 进入主动 USB PD 契约 2

OIAC 插头应遵循以下步骤：

1. 开始使用 GoodCRC 响应来自其端口伙伴的 USB PD 消息。
2. 请求 5 V @ 0 A 电源合同。
3. 可以移除 Ra 以节省电力。

6.3.4.12.2 退出活动 USB PD 契约 2

该插头应过渡至***Final System Configuration Verification*** (M13) 以进行最终系统验证。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.4.13 Release Remote Source_Cap GoodCRC 2 State (M12)

OIAC Source Plug configuration is completed and the *USB 3.2* begins looking for a connection.

6.3.4.13.1 Entry to Release Remote Source_Cap GoodCRC 2

The OIAC plug shall release the Remote SourceCap GoodCRC.

6.3.4.13.2 Exit from Release Remote Source_Cap GoodCRC 2

The plug shall transition to ***Final System Configuration Verification*** (M13) for final system verification.

6.3.4.14 Error – USB2 Billboard + Complete Reset (M13)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: An invalid configuration occurred. Full link will be reset."

6.3.4.14.1 Entry to Error – USB2 Billboard + Complete Reset (M13)

On entry Error – USB2 Billboard + Complete Reset, the plug shall:

1) Present a USB2 Billboard message
2) Send a MSG_Hard_Reset to the remote Plug
3) Wait for Hard Reset Ack from Remote Plug (Unless entry is from an expired WatchDog Timer, in which case, go directly to M13-B)

   Received ACK (State M13-B):

4) Send Hard Reset to the Local Port

   Did NOT receive ACK (State M13-C):

5) Present USB2 Billboard Message: "Error: Internal Cable Communication Error. Unplug both cable ends to reset."

6.3.4.14.2 Exit from Error – USB2 Billboard + Complete Reset (M13 B/C)

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power from each port.

6.3.4.14.3 WatchDog Timer Entry

A watchdog timer should be implemented for internal cable messages that require a response. The watchdog timer will also provide an entry to an ***Error State*** (M13) if the far end plug is unresponsive for any reason.

There are a few states where the watchdog timer shall NOT be implemented including but not limited to M2, where it is possible that only a single end of the OIAC is connected and M6, where the reboot sequence can take a few seconds.

6.3.4.15 Final System Configuration Verification (M14)

Final System Configuration Verification is used to do one final check there were no unforeseen changes the local port and the final cable configuration defined by the master plug.

6.3.4.15.1 Entry to Final System Configuration Verification

The OIAC plug shall check all values in the MSG_Cable_Config match that of the current local port's configuration.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.4.13 释放远程 Source_Cap GoodCRC 2 状态（M12）

OIAC 源插头配置已完成并且 *USB 3.2* 开始寻找连接。

6.3.4.13.1 进入释放远程 Source_Cap GoodCRC 2

OIAC 插头应释放 Remote SourceCap GoodCRC。

6.3.4.13.2 退出释放远程 Source_Cap GoodCRC 2

该插头应过渡至***Final System Configuration Verification*** (M13) 以进行最终系统验证。

6.3.4.14 错误 – USB2 Billboard **+** 完全重置 (M13)

插件会显示一个公告牌，表明存在无效配置。例如：“ 错误：发生无效配置。整个链接将被重置。 ”

6.3.4.14.1 进入错误 – USB2 公告牌 **+** 完全重置 (M13)

进入错误 – USB2 Billboard + 完全重置后，插头应：

1) 显示 USB2 广告牌消息 2) 向远程插头发送 MSG_Hard_Reset 3) 等待来自远程插头的硬重置确认（除非条目来自过期的看门狗计时器，在这种情况下直接转到 M13-B）收到 ACK（状态 M13-B）：4) 向本地端口发送硬重置未收到 ACK（状态 M13-C）：5) 显示 USB2 广告牌消息：“ 错误：内部电缆通信错误。

拔掉电缆两端即可重置。 ”

6.3.4.14.2 退出错误 – USB2 Billboard **+** 完全重置 (M13 B/C)

退出此错误状态的唯一方法是通过重置断开 VCONN 电源，或者通过断开事件断开每个端口的 VCONN 电源。

6.3.4.14.3 看门狗定时器条目

应为需要响应的内部电缆消息实施看门狗定时器。如果远端插头因任何原因无响应，看门狗定时器还将提供 ***Error State*** (M13) 的条目。

在一些状态下，不得实施看门狗定时器，包括但不限于 M2（其中可能仅连接 OIAC 的一端）和 M6（其中重启序列可能需要几秒钟）。

6.3.4.15 最终系统配置验证（M14）

Final System Configuration Verification 用于进行最后检查，确保本地端口和主插头定义的最终电缆配置没有发生不可预见的变化。

6.3.4.15.1 进入最终系统配置验证

OIAC 插头应检查 MSG_Cable_Config 中的所有值是否与当前本地端口的配置相匹配。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.4.15.2 Exit from Final System Configuration Verification

The plug shall transition to:

- ***Rx.Detect***, and start far-end receiver termination detection and the *USB 3.2* RTSSM State Machine after a successful match of the MSG_Cable_Config and the local port's configuration, or
- ***Error - USB2 Billboard + Complete RESET*** (State M14) after unsuccessful match of the MSG_Cable_Config and the local port's configuration.

6.3.5 OIAC Connection State Diagram Slave

The following sections details a possible OIAC state diagram for the Slave Plug.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.4.15.2 退出最终系统配置验证

插头应过渡到：

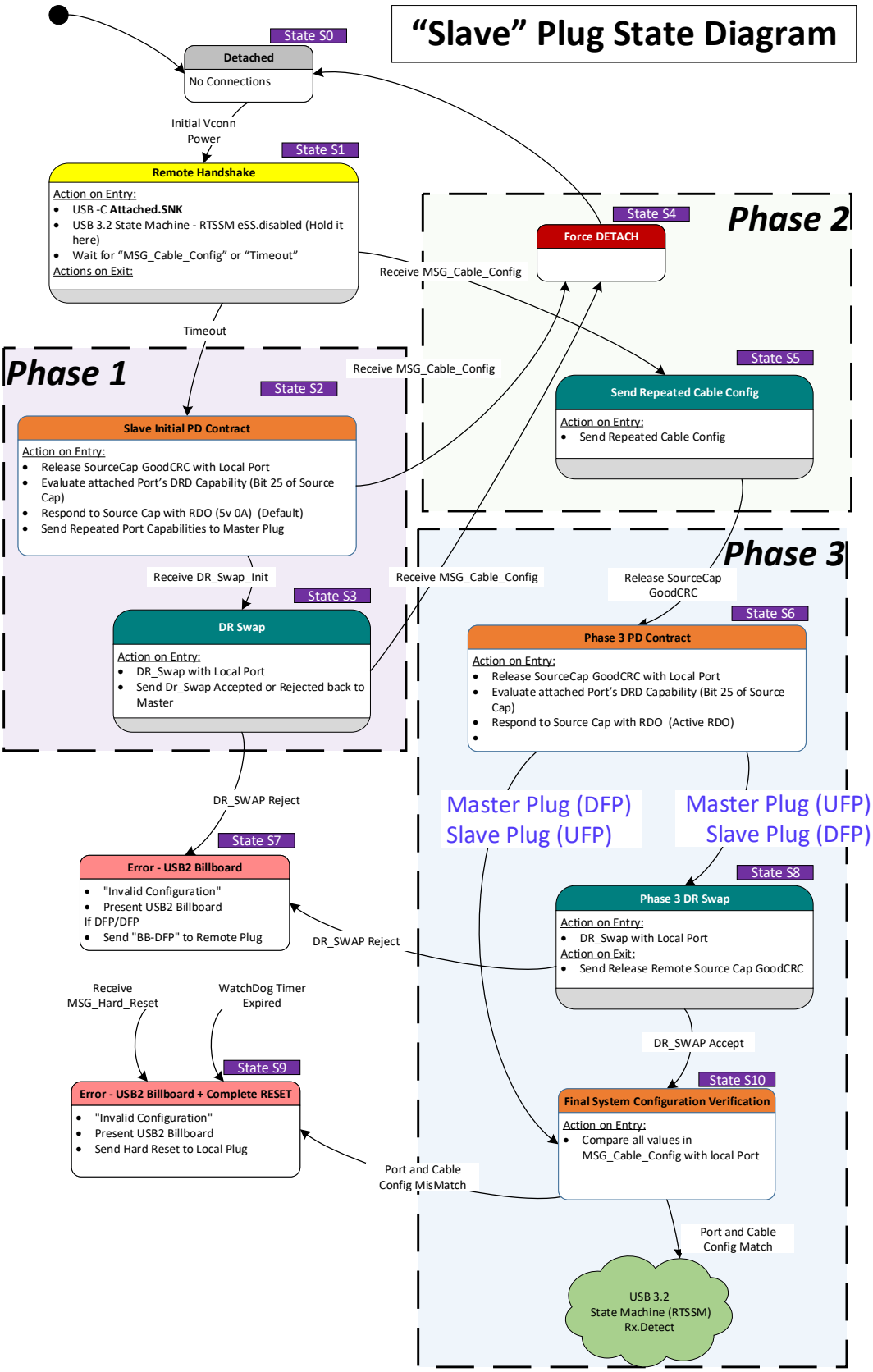
- ***Rx.Detect***，并在 MSG_Cable_Config 与本地端口配置匹配成功后启动远端接收器终止检测和 *USB 3.2* RTSSM 状态机，或在 MSG_Cable_Config 与本地端口配置匹配不成功后启动 • ***Error - USB2 Billboard + Complete RESET***（状态 M14）。

6.3.5 OIAC 连接状态图从机

以下部分详细介绍了从属插头的可能的 OIAC 状态图。

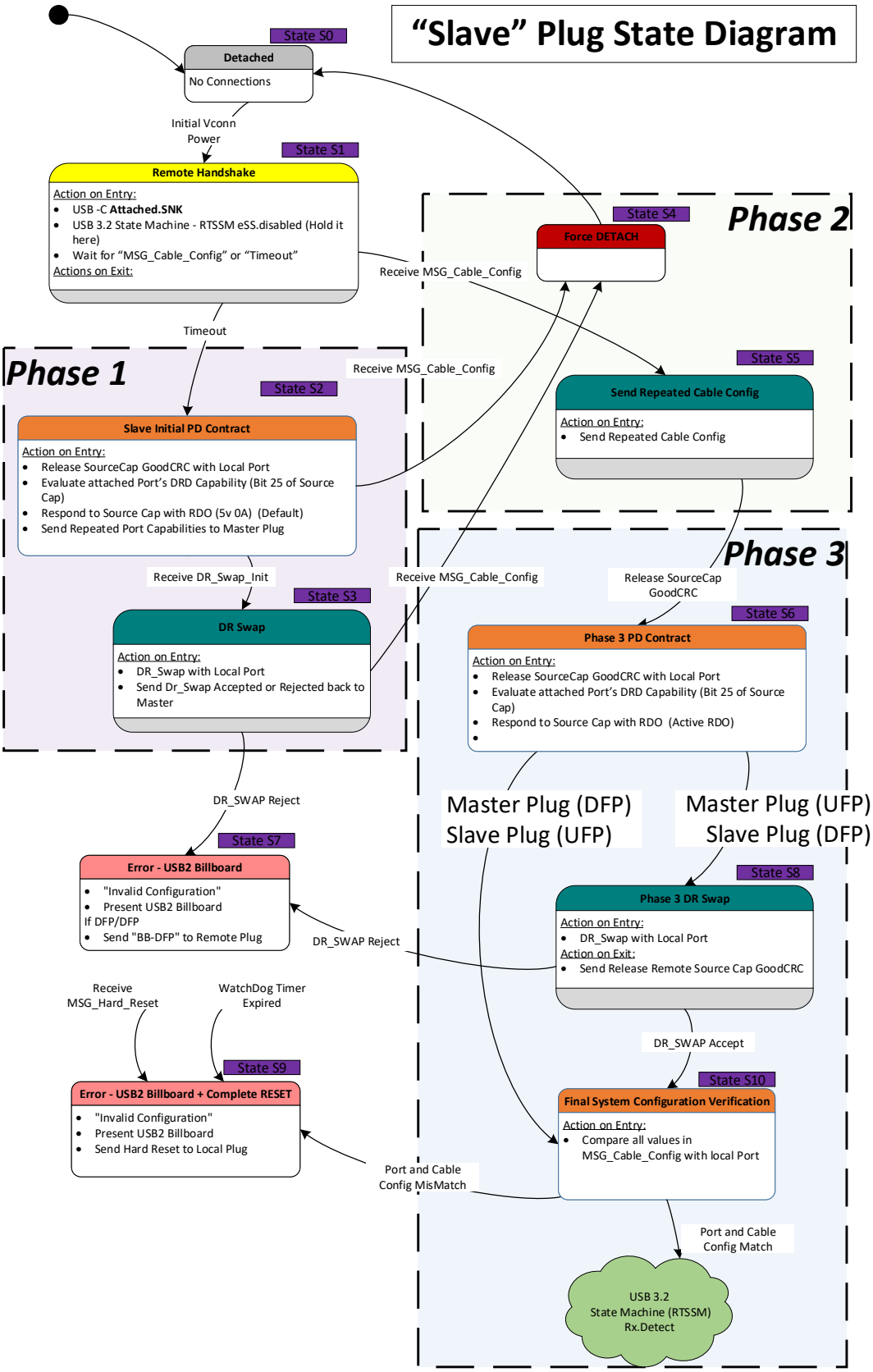
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-17 OIAC Slave Plug State Diagram



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 6-17 OIAC 从属插头状态图



版权所有 © 2019 USB 3.0 Promoter Group。保留所有权利。

6.3.5.1 Detached State (S0)

The plug is in ***Detached*** (S0) when no power is applied. The plug transitions to ***Remote Handshake*** (S1) when VCONN is applied.

6.3.5.2 Remote Handshake State (S1)

The plug is waiting for the "Timeout" timer expiration or a "MSG_Cable_Config" message from the master plug.

Recommended Timeout time = ~100ms

The Timeout time is dependent on the duty cycle of the Master Plug's Repeat MSG_Cable_Config messages and the maximum cable latency.

6.3.5.2.1 Entry to Remote Handshake

The plug enters Attached.SNK followed by entry to ***Remote Handshake*** (S1).

The plug starts in the USB 3.2 RTSSM eSS.Disabled and remains in eSS.Disable until cable initialization is complete at the end of Phase 3.

6.3.5.2.2 Exit from Remote Handshake

The plug transitions to:

- ***Slave Initial PD Contract*** (S2) when the "Timeout" timer has expired, or
- ***Send Repeated Cable Config*** (S5) upon receipt of a "MSG_Cable_Config" message.

6.3.5.3 Slave Initial DP Contract (S2)

The plug takes the following actions in the order defined:

1. Send a GoodCRC in response to a Source Capabilities message from the local attached port.
2. Evaluate the local attached port's DRD Capability (Bit 25 of the Source Capabilities message).
3. Send the initial RDO (5 V/0 A) and negotiate an explicit power contract.
4. Send "MSG_Port_Capabilities" to the master plug. The plug shall continue to send "MSG_Port_Capabilities" until it exits this state.

6.3.5.3.1 Entry to Slave Initial DP Contract

The plug enters ***Slave Initial PD Contract*** (S2) upon "Timeout" timer expiration.

6.3.5.3.2 Exit from Slave Initial DP Contract

The plug transitions to:

- ***DR Swap*** (S3) upon receipt of a "DR_Swap_Init" message from the master plug, or
- ***Force Detach*** (S4) upon receipt of a "MSG_Cable_Config" message from the master plug.

6.3.5.4 DR Swap (S3)

The plug determines if a DR_Swap can be performed with the local attached port or the master plug configured itself.

6.3.5.4.1 Entry to DR Swap

Upon entry into DR Swap (S3) the plug shall:

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.5.1 分离状态（S0）

未通电时，插头处于 ***Detached***（S0）。通电后，插头转换到 ***Remote Handshake*** (S1)。

6.3.5.2 远程握手状态（S1）

插头正在等待“ 超时 ”计时器到期或来自主插头的“ MSG_Cable_Config ”消息。

建议超时时间= ~100ms

超时时间取决于主插头的重复 MSG_Cable_Config 消息的占空比和最大电缆延迟。

6.3.5.2.1 进入远程握手

插头进入 Attached.SNK，然后进入 ***Remote Handshake***（S1）。

插头从 USB 3.2 RTSSM eSS.Disabled 开始，并保持在 eSS.Disable 状态，直到第 3 阶段结束时电缆初始化完成。

6.3.5.2.2 退出远程握手

插头转换至：

- ***Slave Initial PD Contract*** （S2）当“ 超时 ”计时器到期时，或
- ***Send Repeated Cable Config***（S5）收到“ MSG_Cable_Config ”消息后。

6.3.5.3 从属初始DP合约（S2）

插头按照定义的顺序执行以下操作：

1. 发送 GoodCRC 以响应本地附加设备的源功能消息
端口。2. 评估本地连接端口的 DRD 功能（源功能消息的第 25 位）。3. 发送初始 RDO（5 V/0 A）并协商明确的电源合同。4. 向主插头发送“ MSG_Port_Capabilities ”。插头应继续发送“ MSG_Port_Capabilities ”，直到退出此状态。

6.3.5.3.1 进入从属初始DP合约

“ 超时 ”计时器到期后，插头进入 ***Slave Initial PD Contract*** (S2)。

6.3.5.3.2 退出从属初始 DP 合约

插头转换至：

- ***DR Swap*** (S3) 在收到来自主插头的“ DR_Swap_Init ”消息后，或 • ***Force Detach*** (S4) 在收到来自主插头的“ MSG_Cable_Config ”消息后。

6.3.5.4 DR 交换（S3）

插头确定是否可以使用本地连接端口或自行配置的主插头执行 DR_Swap。

6.3.5.4.1 进入 DR 互换

进入 DR 交换 (S3) 后，插头应：

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

1. Send DR_Swap message to the local attached port.
2. Send MSG_DR_Swap_Accept when the plug receives Accept message from the local attached port.
3. Send MSG_DR_Swap_Reject when the plug receives Reject message from the local attached port.

If the local port responds to the DR Swap with "Wait," then the plug shall follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state ***Error – USB2 Billboard*** (S7).

6.3.5.4.2 Exit from DR Swap

The plug shall transition to:

- ***Error – USB2 Billboard*** (S7) upon rejection of the local attached port DR_Swap, or
- ***Force Detach*** (S4) upon receipt of a "MSG_Cable_Config" message from the master plug.

6.3.5.5 Force Detach (S4)

The plug shall transition to SRC.Open on both CC and VCONN and maintain this state for at least tSRCDisconnect.

6.3.5.5.1 Entry to Force Detach

The plug enters ***Force Detach*** (S4) upon receipt of a "MSG_Cable_Config"" message from the master plug.

6.3.5.5.2 Exit from Force Detach

The plug transitions to ***Detached*** (S0) upon exit from ***Force Detach***.

6.3.5.6 Send Repeated Cable Config (S5)

The plug repeatedly sends "MSG_Cable_Config" messages in this state to inform the master plug of the configuration of the local attached port.

6.3.5.6.1 Entry to Send Repeated Cable Config

The plug enters ***Repeated Cable Config*** (S5) upon receipt of a "MSG_Cable_Config" message from the master plug.

6.3.5.6.2 Exit from Send Repeated Cable Config

The plug transitions to ***Phase 3 PD Contract*** (S6) upon receipt of a "Release SourceCap GoodCRC" message from the master port.

6.3.5.7 Phase 3 PD Contract (S6)

The plug performs the following actions in this state:

1. Send a GoodCRC in response to a Source Capabilities message from the local attached port.
2. Evaluate the attached local attached port's DRD Capability (Bit 25 of the Source Capabilities message).
3. Send the initial RDO (5 V/0 A) in response to the Source Capabilities message and negotiate an explicit power contract.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

1. 向本地连接端口发送 DR_Swap 消息。 2. 当插头从本地连接端口收到 Accept 消息时，发送 MSG_DR_Swap_Accept。 3. 当插头从本地连接端口收到 Reject 消息时，发送 MSG_DR_Swap_Reject。

如果本地端口以“等待”响应 DR 交换，则插头应遵循 tDRSwapWait 计时器并重试最多 3 次，之后它将出错并转换到状态 ***Error – USB2 Billboard***（S7）。

6.3.5.4.2 退出 DR 交换

插头应过渡到：

- ***Error – USB2 Billboard*** （S7）在拒绝本地连接端口 DR_Swap 时，或
- ***Force Detach***（S4）收到来自主插头的“MSG_Cable_Config”消息。

6.3.5.5 强制分离（S4）

插头应在 CC 和 VCONN 上转换至 SRC.Open，并维持此状态至少 tSRCDisconnect。

6.3.5.5.1 进入强制分离

当插头收到主插头发来的“MSG_Cable_Config”消息时，插头进入***Force Detach***（S4）。

6.3.5.5.2 退出强制分离

从 ***Force Detach*** 退出后，插头转换到 ***Detached*** (S0)。

6.3.5.6 发送重复电缆配置（S5）

插头在此状态下重复发送“MSG_Cable_Config”消息，以告知主插头本地连接端口的配置。

6.3.5.6.1 发送重复电缆配置条目

当插头收到主插头发来的“MSG_Cable_Config”消息时，插头进入***Repeated Cable Config***（S5）。

6.3.5.6.2 退出发送重复电缆配置

当从主端口接收到“Release SourceCap GoodCRC”消息时，插头转换到 ***Phase 3 PD Contract***（S6）。

6.3.5.7 第三阶段 PD 合同（S6）

插头在此状态下执行以下操作：

1. 发送 GoodCRC 以响应本地附加设备的源功能消息
端口。2. 评估连接的本地连接端口的 DRD 功能（源功能消息的第 25 位）。3. 发送初始 RDO（5 V/0 A）以响应源功能消息并协商明确的电源合同。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.5.7.1 Entry to Phase 3 PD Contract

The plug enters ***Phase 3 PD Contract*** upon receipt of a "Release SourceCap GoodCRC" message from the master plug.

6.3.5.7.2 Exit from Phase 3 PD Contract

The plug transitions to:

- ***Final System Configuration Verification*** (S10) for final system verification upon determination the master plug is acting as a DFP and it is acting as a UFP, or
- ***Phase 3 DR Swap*** (S8) upon determination the master plug is acting as a UFP and it is acting as a DFP.

6.3.5.8 Error – USB2 Billboard (S7)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: A DFP only device connected to one of the plugs."

6.3.5.8.1 Entry to Error – USB2 Billboard

The plug transitions to this state upon rejection of a DR_Swap by the local attached port.

6.3.5.8.2 Exit from Error – USB2 Billboard

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.

6.3.5.9 Phase 3 DR Swap State (S8)

The plug issues a DR_Swap with its local attached port in this state.

6.3.5.9.1 Entry to Phase 3 DR Swap

The plug enters ***Phase 3 DR Swap*** upon determination the master plug is connected as a UFP and the slave plug should connect as a DFP.

6.3.5.9.2 Exit from Phase 3 DR Swap

The plug shall transition to:

- ***Final System Configuration Verification*** (S10) for final system verification after successful completion of the DR_Swap with the local attached port, or
- ***Error – USB2 Billboard*** (S7) after unsuccessful completion of the DR_Swap with the local attached port.

6.3.5.10 Error – USB2 Billboard + Complete RESET (S9)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: An invalid configuration occurred. Full link will be reset."

6.3.5.10.1 Entry to Error – USB2 Billboard + Complete RESET

On entry ***Error – USB2 Billboard + Complete RESET***, the plug shall:

1. Present a USB2 Billboard message.
2. Send Hard_Reset to the Local Plug.

6.3.5.10.2 Exit from Error – USB2 Billboard + Complete RESET

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.5.7.1 进入第 3 阶段 PD 合同

当插头收到主插头发来的“ Release SourceCap GoodCRC ”消息时，插头进入 ***Phase 3 PD Contract***。

6.3.5.7.2 退出第 3 阶段 PD 合同

插头转换至：

- ***Final System Configuration Verification*** (S10) 用于最终系统验证，确定主插头充当 DFP 并且充当 UFP，或 • ***Phase 3 DR Swap*** (S8) 在确定主插头充当 UFP 并且充当

  充当 DFP。

6.3.5.8 错误 – USB2 广告牌 (S7)

插头上会显示一个公告牌，表明存在无效配置。例如：“ 错误：一个仅限 DFP 的设备连接到其中一个插头。 ”

6.3.5.8.1 进入错误 – USB2 公告牌

当本地连接端口拒绝 DR_Swap 时，插头将转换到此状态。

6.3.5.8.2 退出错误 – USB2 公告牌

退出此错误状态的唯一方法是通过重置断开 VCONN 电源，或者通过断开事件也断开 VCONN 电源。

6.3.5.9 第 3 阶段 DR 交换状态（S8）

处于这种状态的插头向其本地连接端口发出 DR_Swap 请求。

6.3.5.9.1 进入第 3 阶段 DR 互换

当确定主插头作为 UFP 连接并且从属插头应作为 DFP 连接时，插头进入 ***Phase 3 DR Swap***。

6.3.5.9.2 退出第 3 阶段 DR 交换

插头应过渡到：

- ***Final System Configuration Verification***（S10）用于成功完成本地连接端口的 DR_Swap 之后的最终系统验证，或 • ***Error – USB2 Billboard***（S7）用于未成功完成 DR_Swap 之后

  本地连接端口。

6.3.5.10 错误 – USB2 广告牌 **+** 完全重置 (S9)

插件会显示一个公告牌，表明存在无效配置。例如：“ 错误：发生无效配置。整个链接将被重置。 ”

6.3.5.10.1 进入错误 – USB2 公告牌 **+** 完成重置

在进入 ***Error – USB2 Billboard + Complete RESET*** 时，插头应：

1. 显示 USB2 Billboard 消息。 2. 向本地插头发送 Hard_Reset。

6.3.5.10.2 退出错误 – USB2 Billboard **+** 完成重置

退出此错误状态的唯一方法是通过重置断开 V CONN 电源，或者通过断开事件也断开 VCONN 电源。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.5.10.3 WatchDog Timer Entry

A watchdog timer should be implemented for internal cable messages that require a response. The watchdog timer will also provide an entry to an ***Error State*** (M13) if the far end plug is unresponsive for any reason.

There are a few states where the watchdog timer shall NOT be implemented including but not limited to S5, where the reboot sequence can take a few seconds.

6.3.5.11 Final System Configuration Verification (S10)

The ***Final System Configuration Verification*** is used to one final check there were no unforeseen changes the local port and the final cable configuration defined by the master plug.

6.3.5.11.1 Entry to Final System Configuration Verification

The OIAC plug shall check all values in the MSG_Cable_Config match that of the current local port's configuration.

6.3.5.11.2 Exit from Final System Configuration Verification

The plug shall transition to:

- ***Rx.Detect***, and start far-end receiver termination detection and the *USB 3.2* RTSSM State Machine after a successful match of the MSG_Cable_Config and the local port's configuration, or
- ***Error – USB2 Billboard + Complete RESET*** (State S9) after unsuccessful match of the MSG_Cable_Config and the local port's configuration.

6.4 Active Cable Power Requirements

6.4.1 VBUS Requirements

Short active cables shall meet the limits of the IR Drop on VBUS and ground defined in Section 4.4.1.

Short active cables shall provide VBUS and support at least 3 A and optionally 5 A current.

6.4.2 OIAC VBUS Requirements

The OIAC cable plugs have two power contracts. The first contract is defined at first connection of the cable. The second contract is after the data role establishment in the Active state.

6.4.2.1 OIAC VBUS Requirements on Initial Connection

The OIAC cable plugs shall negotiate a power contract with their plug partners as defined in this section on Initial Connection. The *USB PD* Sink Capabilities PDO presented by the OIAC cable plug (SOP) on Initial Connection is defined in Table 6-9. The Sink RDO (SOP) before data role establishment is defined in Table 6-10.

The OIAC cable plug (SOP) shall wait tTypeCSinkWaitCap after VBUS is presented before issuing a Hard Reset to restart sending of the Source_Capabilities.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.3.5.10.3 看门狗定时器条目

应为需要响应的内部电缆消息实施看门狗定时器。如果远端插头因任何原因无响应，看门狗定时器还将提供 ***Error State*** (M13) 的条目。

在一些状态下不得实施看门狗定时器，包括但不限于 S5，其中重启序列可能需要几秒钟。

6.3.5.11 最终系统配置验证（S10）

Final System Configuration Verification 用于最后检查本地端口和主插头定义的最终电缆配置是否发生不可预见的变化。

6.3.5.11.1 进入最终系统配置验证

OIAC 插头应检查 MSG_Cable_Config 中的所有值是否与当前本地端口的配置相匹配。

6.3.5.11.2 退出最终系统配置验证

插头应过渡到：

- ***Rx.Detect***，并在 MSG_Cable_Config 与本地端口配置匹配成功后启动远端接收器终止检测和 *USB 3.2* RTSSM 状态机，或在 MSG_Cable_Config 与本地端口配置匹配不成功后启动 • ***Error – USB2 Billboard + Complete RESET***（状态 S9）。

6.4 有源电缆功率要求

6.4.1 VBUS 要求

短有源电缆应满足第 4.4.1 节中定义的 V BUS 和地面上的 IR 压降限值。

短活动驾驶室 les 应提供 VBUS 并支持至少 3 A 和 op 最大电流为5A。

6.4.2 OIAC VBUS 要求

OIAC 电缆插头有两个电源合同。第一个合同是在电缆首次连接时定义的。第二个合同是在 A ctive 状态下数据角色建立之后定义的。

6.4.2.1 初始连接的 OIAC VBUS 要求

OIAC 电缆插头应与其插头伙伴协商电源合同，如本节初始连接中所述。初始连接时 OIAC 电缆插头 (SOP) 提供的 *USB PD* 接收器功能 PDO 定义在表 6-9 中。数据角色建立之前的接收器 RDO (SOP) 定义在表 6-10 中。

OIAC 电缆插头 (SOP) 应在 V BUS 出现后等待 tTypeCSinkWaitCap，然后发出硬重置以重新开始发送 Source_Capabilities。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 6-9 OIAC Sink_Capabilities PDO (SOP) on Initial Connection

Bit(s)	Value	Parameter
B31..30	00b	Fixed Supply
B29	0b	Not Dual-Role Power
B28	0b	Not higher capability
B27	0b	Not unconstrained power
B26	X	USB Communications Capable – Don't care
B25	X	Dual-Role Data – Don't care
B24..23	00b	Fast Role Swap not supported
B22..20	000b	Reserved
B19..10	0001100100b	5V in 50mV units
B9..0	Design defined	Operational current in 10mA units

Table 6-10 OIAC Sink_Capabilities_Extended PDO (SOP) on Initial Connection

Offset	Field	Size	Value	Description
0	VID	2	Numeric	Vendor ID (assigned by the USB-IF)
2	PID	2	Numeric	Product ID (assigned by the manufacturer)
4	XID	4	Numeric	Value provided by the USB-IF assigned to the product
8	FW Version	1	Numeric	Firmware version number
9	HW Version	1	Numeric	Hardware version number
10	SKEDB Version	1	Numeric	SKEDB Version (not the specification Version): Version 1.0 = 1 Values 0 and 2-255 are Reserved and shall not be used.
11	Load Step	1	Bit Field	0x00
12	Sink Load Characteristics	2	Bit field	0x00
14	Compliance	1	Bit Field	0x00
15	Touch Temp	1	Value	0
16	Battery Info	1	Byte	0x00
17	Sink Modes	1	Bit field	0x00
18	Sink Minimum PDP	1	Byte	0x00
19	Sink Operational PDP	1	Byte	0x00
20	Sink Maximum PDP	1	Byte	0x00

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 6-9 初始连接时的 OIAC Sink_Capabilities PDO（SOP）

Bit(s)	Value	Parameter
B31..30	00b	Fixed Supply
B29	0b	Not Dual-Role Power
B28	0b	Not higher capability
B27	0b	Not unconstrained power
B26	X	USB Communications Capable – Don't care
B25	X	Dual-Role Data – Don't care
B24..23	00b	Fast Role Swap not supported
B22..20	000b	Reserved
B19..10	0001100100b	5V in 50mV units
B9..0	Design defined	Operational current in 10mA units

表 6-10 初始连接时的 OIAC Sink_Capabilities_Extended PDO (SOP)

Offset	Field	Size	Value	Description
0	VID	2	Numeric	Vendor ID (assigned by the USB-IF)
2	PID	2	Numeric	Product ID (assigned by the manufacturer)
4	XID	4	Numeric	Value provided by the USB-IF assigned to the product
8	FW Version	1	Numeric	Firmware version number
9	HW Version	1	Numeric	Hardware version number
10	SKEDB Version	1	Numeric	SKEDB Version (not the specification Version): Version 1.0 = 1 Values 0 and 2-255 are Reserved and shall not be used.
11	Load Step	1	Bit Field	0x00
12	Sink Load Characteristics	2	Bit field	0x00
14	Compliance	1	Bit Field	0x00
15	Touch Temp	1	Value	0
16	Battery Info	1	Byte	0x00
17	Sink Modes	1	Bit field	0x00
18	Sink Minimum PDP	1	Byte	0x00
19	Sink Operational PDP	1	Byte	0x00
20	Sink Maximum PDP	1	Byte	0x00

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 6-11 OIAC Sink RDO (SOP) on Initial Connection

Bit(s)	Value	Parameter
B31	0b	Reserved
B20..28	001b	Object Position
B27	0b	No GiveBack flag
B26	0b	No Capabilities Mismatch
B25	1b	USB Communication Capable
B24	1b	No USB Suspend
B23	0b	Unchunked Extended Messages Not Supported
B22..20	000b	Reserved
B19..10	0	Operating Current in 10 mA units
B9..0	0	Maximum current in 10 mA units

6.4.3 USB PD Rules in Active State

The OIAC cable plugs shall negotiate a power contract with their plug partners as defined in this section in the Active State. The OIAC shall follow the message applicability rules defined in Table 6-3 until entry to the Active State.

The minimum USB PD Sink Capabilities PDO presented by the OIAC cable plug (SOP) is defined in Table 6-12. The OIAC may request additional Sink Capabilities (higher voltages and currents) for performance optimization. The minimum Sink RDO is provided as an example in Table 6-13. The OIAC shall function when receiving the minimum Source PDO.

The OIAC cable plug (SOP) shall wait tTypeCSinkWaitCap after V_{BUS} is presented before issuing a Hard Reset to restart sending of the Source_Capabilities

Table 6-12 OIAC Active Sink RDO (SOP)

Bit(s)	Value	Parameter
B31	0b	Reserved
B20..28	As required	Object Position
B27	0b	No GiveBack flag
B26	0b	No Capabilities Mismatch
B25	1b	USB Communication Capable
B24	1b	USB Suspend
B23	As reported from remote end	Unchunked Extended Messages
B22..20	000b	Reserved
B19..10	Design Defined	Operating Current in 10 mA units[1]
B9..0	Design Defined	Maximum current in 10 mA units[1]

Note 1: Thermal design must be considered.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 6-11 初始连接时的 OIAC 接收器 RDO（SOP）

Bit(s)	Value	Parameter
B31	0b	Reserved
B20..28	001b	Object Position
B27	0b	No GiveBack flag
B26	0b	No Capabilities Mismatch
B25	1b	USB Communication Capable
B24	1b	No USB Suspend
B23	0b	Unchunked Extended Messages Not Supported
B22..20	000b	Reserved
B19..10	0	Operating Current in 10 mA units
B9..0	0	Maximum current in 10 mA units

6.4.3 USB PD 活动状态规则

OIAC 电缆插头应在活动状态下与本节定义的插头伙伴协商电力合同。OIAC 应遵循表 6-3 中定义的消息适用性规则，直到进入活动状态。

OIAC 电缆插头 (SOP) 提供的最小 USB PD Sink 能力 PDO 定义在表 6-12 中。OIAC 可能会请求额外的 Sink 能力（更高的电压和电流）以优化性能。表 6-13 中提供了最小 Sink RDO 的示例。OIAC 应在收到最小 Source PDO 时发挥作用。

OIAC 电缆插头 (SOP) 应在 V BUS 出现后等待 tTypeCSinkWaitCap，然后发出硬复位以重新启动 Source_Capabilities 的发送

表 6-12 OIAC 主动接收器 RDO (SOP)

Bit(s)	Value	Parameter
B31	0b	Reserved
B20..28	As required	Object Position
B27	0b	No GiveBack flag
B26	0b	No Capabilities Mismatch
B25	1b	USB Communication Capable
B24	1b	USB Suspend
B23	As reported from remote end	Unchunked Extended Messages
B22..20	000b	Reserved
B19..10	Design Defined	Operating Current in 10 mA units[1]
B9..0	Design Defined	Maximum current in 10 mA units[1]

注 1：必须考虑热设计。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 6-13 OIAC Sink_Capabilities PDO (SOP) in Active

Bit(s)	Value	Parameter
B31..30	00b	Fixed Supply
B29	0b	Not Dual-Role Power
B28	0b	Not higher capability
B27	0b	Not unconstrained power
B26	1b	USB Communications Capable
B25	As reported from Remote End	Dual-Role Data[1]
B24..23	00b	Fast Role Swap not supported
B22..20	000b	Reserved
B19..10	0001100100b	5 V in 50 mV units
B9..0	Design defined	Operational current in 10 mA units[2]

Notes: 1. Reflection of far side connection; 2. Thermal design must be considered.

6.4.4 VCONN Requirements

Active Cables shall:

- Meet the VCONN sink requirement defined in Table 4-6 and Table 6-19.
- Connect VCONN as shown in Figure 2-1 or Figure 2-2.

Short Active Cables shall be capable of being powered from VCONN from only one port.

OIAC shall be powered from VCONN from each port.

6.5 Mechanical

All active cables shall meet the mechanical requirements defined in the Section 3.8.

6.5.1 Thermal

6.5.1.1 Thermal Shutdown

All active cables shall implement a temperature sensor and place the *USB 3.2* signals in the eSS.Disabled state when the plug skin temperature reaches the maximum defined in Table 6-14. Active cables shall indicate they are in thermal shutdown if queried via the *USB PD* ***Get_Status*** command.

OIACs shall billboard in shutdown. For example: “Error: The Optical Cable has experienced a thermal shutdown.”

The Thermal Shutdown is cleared by the following events:

- Disconnect
- *USB PD* Hard Reset

6.5.1.2 Maximum Skin Temperature

Active cable plug’s skin temperature shall not exceed a maximum operating temperature of 30 °C above the ambient temperature for a plastic/rubber housing and 15 °C for a metal housing in any operating mode.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 6-13 OIAC Sink_Capabilities PDO（SOP）处于活动状态

Bit(s)	Value	Parameter
B31..30	00b	Fixed Supply
B29	0b	Not Dual-Role Power
B28	0b	Not higher capability
B27	0b	Not unconstrained power
B26	1b	USB Communications Capable
B25	As reported from Remote End	Dual-Role Data[1]
B24..23	00b	Fast Role Swap not supported
B22..20	000b	Reserved
B19..10	0001100100b	5 V in 50 mV units
B9..0	Design defined	Operational current in 10 mA units[2]

注意：1. 远侧连接的反射；2. 必须考虑热设计。

6.4.4 VCONN 要求

有源电缆应：

- 满足表 4-6 和表 6-19 中定义的 VCONN 接收器要求。• 按照图 2-1 或图 2-2 所示连接 VCONN。

短有源电缆应能够仅从一个端口由 V CONN 供电。

OIAC 应由每个端口的 VCONN 供电。

6.5 机械

所有有源电缆应满足第 3.8 节定义的机械要求。

6.5.1 热

6.5.1.1 热关断

所有有源电缆都应安装温度传感器，并在插头外皮温度达到表 6-14 中定义的最大值时将 *USB 3.2* 信号置于 eSS.Disabled 状态。如果通过 *USB PD* ***Get_Status*** 命令查询，有源电缆应指示它们处于热关机状态。

OIAC 应在关机时发布公告。例如：“ 错误：光缆发生热关机。 ”

热关断由以下事件清除：

- 断开连接•*USB PD*硬重置

6.5.1.2 最高皮肤温度

在任何工作模式下，有源电缆插头的外皮温度不得超过环境温度以上 30°C（对于塑料/橡胶外壳）和 15°C（对于金属外壳）。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.5.1.3 Thermal Reporting

Active cables shall implement reporting their maximum internal operating temperature in the *USB PD* ***Discover_ID*** Command. Active cables shall implement reporting their current internal operating temperature in the *USB PD* ***Get_Status*** Command on SOP' and SOP" when supported. Active cables shall update their reported Internal Temperature at least every 500 ms.

The plug's Internal Temperature is reported in °C and shall be monotonic. It is not the plug's skin temperature, but cable manufacturers shall correlate the maximum internal operating temperature with the maximum plug skin temperature to ensure shutdown when the maximum plug skin temperature is reached.

Sources and/or Sinks may take action to reduce VBUS current to reduce the cable plug internal operating temperature to below the reported maximum operating temperature. It is recommended Sources and/or Sinks poll the plug's Internal Temperature every 2 seconds.

Table 6-14 Cable Temperature Requirements

Temperature Requirements	
Maximum Internal to Skin Temperature Offset	Design Specific
Maximum Internal Operating Temperature	Design Specific
Maximum Skin Temperature Plastic/Rubber[1]	80 °C
Maximum Skin Temperature Metal[1]	55 °C

Note 1: IEC 69950-1 reduced by 5 °C

6.5.2 Plug Spacing

Active cables will support the USB Type-C vertical and horizontal spacing defined Section 3.10.2 when functioning in *USB 3.2* x1 operation. However, this spacing may impose thermal constraints. Appendix D provides system design guidance to minimize the thermal impact due to connector spacing. It is recommended that products designed for *USB 3.2* x2 operation with multiple adjacent USB Type-C connectors follow the design guidance in Appendix D to minimize the likelihood the active cable will go into thermal shutdown.

6.6 Electrical Requirements

6.6.1 Shielding Effectiveness Requirement

All active cables shall meet the shielding effectiveness requirement defined in Section 3.7.7 and Figure 3-65.

6.6.2 Low Speed Signal Requirement

6.6.2.1 CC Channel Requirements

Active cables shall meet the Low-Speed Signal Requirements in Section 3.7.2.4.

6.6.2.2 SBU Requirements

6.6.2.2.1 Short Active Cables

Short active cables SBU wires shall meet the requirements defined in Table 6-15 and shall meet the crosstalk requirements both near-end and far-end between the low speed signals as defined in Section 3.7.2.4.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.5.1.3 热报告

有源电缆应在 *USB PD* ***Discover_ID*** 命令中报告其最大内部工作温度。有源电缆应在 SOP ’ 和 SOP ” ~~上的 *USB PD* ***Get_Status***~~ 命令中报告其当前内部工作温度（如果支持）。有源电缆应至少每 500 毫秒更新一次其报告的内部温度。

插头的内部温度以 °C 为单位报告，且应为单调的。它不是插头的外皮温度，但电缆制造商应将最高内部工作温度与最高插头外皮温度关联起来，以确保在达到最高插头外皮温度时关闭。

源和/或接收器可能会采取措施降低 VBUS 电流，以将电缆插头内部工作温度降低到报告的最大工作温度以下。建议源和/或接收器每 2 秒轮询一次插头的内部温度。

表 6-14 电缆温度要求

Temperature Requirements	
Maximum Internal to Skin Temperature Offset	Design Specific
Maximum Internal Operating Temperature	Design Specific
Maximum Skin Temperature Plastic/Rubber[1]	80 °C
Maximum Skin Temperature Metal[1]	55 °C

注 1：IEC 69950-1 降低 5°C

6.5.2 插头间距

在 *USB 3.2* x1 操作下运行时，有源电缆将支持第 3.10.2 节定义的 USB Type-C 垂直和水平间距。但是，此间距可能会造成热限制~~。附录~~ D 提供了系统设计指南，以尽量减少连接器间距造成的热影响。建议为具有~~多个相邻 US~~B Type-C 连接器的 *USB 3.2* x2 操作而设计的产品遵循附录 D 中的设计指南，以尽量减少有源电缆进入热关机状态的可能性。

6.6 电气要求

6.6.1 屏蔽效能要求

所有有源电缆应满足第 3.7.7 节和图 3-65 定义的屏蔽效能要求。

6.6.2 低速信号要求

6.6.2.1 CC 通道要求

有源电缆应满足第 3.7.2.4 节中的低速信号要求。

6.6.2.2 SBU 要求

6.6.2.2.1 短有源电缆

短有源电缆SBU线应满足表6-15定义的要求，并应满足第3.7.2.4节定义的低速信号之间的近端和远端串扰要求。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

SBUs have no guaranteed performance when Vconn is not provided to the cable. The Host or Device shall not provide any signal beyond what is defined in Table 6-15 when VCONN has not been provided.

Table 6-15 Summary of Active Cable Features

Name	Description	Min	Max	Units
zCable_SBU	Cable characteristic impedance on the SBU wires	32	53	Ω
tCableDelay_SBU	Cable propagation delay on the SBU wire		26	ns
rCable_SBU	DC resistance of SBU wires in the cable in USB		40	Ω
vCable_SBU	Cable voltage swing on SBU wires	−0.3	4.0	V
Insertion Loss[1]	Cable insertion Loss		5 @ 0.5 MHz 7 @ 1 MHz 12 @ 10 MHz 13 @ 25 MHz 15 @ 50 MHz 16 @ 100 MHz	dB
iCableSBU	Maximum end-to-end current	−25	+25	mA

Note 1: Measurement referenced to 50 Ohms.

6.6.2.2.2 Optically Isolated Cables

OIACs are not required to support SBU1/2 for *USB 3.2* support. SBUs are not usable until the cable has entered an Alternate Mode. OIACs which choose to support SBU signals shall meet the requirements of the Alternate Mode(s) they support. Definition of the SBU requirements for Alternate Modes is outside the scope of this document.

6.6.3 USB 2.0

The *USB 2.0* support depends on the type of active cable.

6.6.3.1 Short Active Cables

Short active cables shall meet the *USB 2.0* requirements defined in Section 3.7.2.4 and 3.7.2.6.

Note: Active Cables greater than 5m report the number of hub hops consumed in the Active Cable VDOs.

6.6.3.2 Optically Isolated Active Cables

OIACs forward *USB 3.2* and do not forward *USB 2.0*. The OIAC will take action to reset the link when the USB Device drops from *USB 3.2* to *USB 2.0*.

During the initial connection the OIAC shall present as a *USB 2.0* DFP and provide a 15K Ohm pull down on the D+/D− pins on both ends of the cable. The cable plug shall not issue a *USB 2.0* Reset in this state.

The OIAC cable plug shall issue a *USB 2.0* Reset upon detecting a *USB 2.0* connection on D+/D− (LS, FS, or HS *USB 2.0* connection). The cable plug shall issue a *USB 2.0* Bus Reset by pulling D+ and D− low for at least 50 ms.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

当电缆未提供 Vconn 时，SBU 的性能无法保证。当未提供 VCONN 时，主机或设备不得提供表 6-15 中定义以外的任何信号。

表 6-15 有源电缆特性摘要

Name	Description	Min	Max	Units
zCable_SBU	Cable characteristic impedance on the SBU wires	32	53	Ω
tCableDelay_SBU	Cable propagation delay on the SBU wire		26	ns
rCable_SBU	DC resistance of SBU wires in the cable in USB		40	Ω
vCable_SBU	Cable voltage swing on SBU wires	−0.3	4.0	V
Insertion Loss[1]	Cable insertion Loss		5 @ 0.5 MHz 7 @ 1 MHz 12 @ 10 MHz 13 @ 25 MHz 15 @ 50 MHz 16 @ 100 MHz	dB
iCableSBU	Maximum end-to-end current	−25	+25	mA

注 1：测量参考 50 欧姆。

6.6.2.2.2 光隔离电缆

OIAC 无需支持 SBU1/2 即可支持 *USB 3.2*。在电缆进入备用模式之前，SBU 不可用。选择支持 SBU 信号的 OIAC 应满足其支持的备用模式的要求。备用模式的 SBU 要求定义超出了本文档的范围。

6.6.3 USB 2.0

USB 2.0 的支持取决于有源电缆的类型。

6.6.3.1 短有源电缆

短有源电缆应满足第 3.7.2.4 和 3.7.2.6 节定义的*USB 2.0*要求。

注意：长度超过 5 米的有源电缆会报告有源电缆 VDO 中消耗的集线器跳数。

6.6.3.2 光隔离有源电缆

OIAC 转发 *USB 3.2* 但不转发 *USB 2.0*。当 USB 设备从 *USB 3.2* 降至 *USB 2.0* 时，OIAC 将采取行动重置链接。

在初始连接期间，OIAC 应显示为 *USB 2.0* DFP，并在电缆两端的 D+/D − 引脚上提供 15K 欧姆下拉电阻。在此状态下，电缆插头不应发出 *USB 2.0* 重置。

OIAC 电缆插头应在检测到 D+/D − 上的 *USB 2.0* 连接（LS、FS 或 HS *USB 2.0* 连接）时发出 *USB 2.0* 复位。电缆插头应通过将 D+ 和 D − 拉低至少 50 毫秒来发出 *USB 2.0* 总线复位。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The OIAC shall implement a tDisableCount counter to determine how many times the cable has transitioned from *USB 3.2* to *USB 2.0*. The tDisableCount counter shall be reset to zero on either condition:

- Power on Reset of the OIAC, or
- Successful transition to *USB 3.2* U0.

The OIAC shall present and latch a *USB 2.0* billboard when tDisableCount counter reaches three.

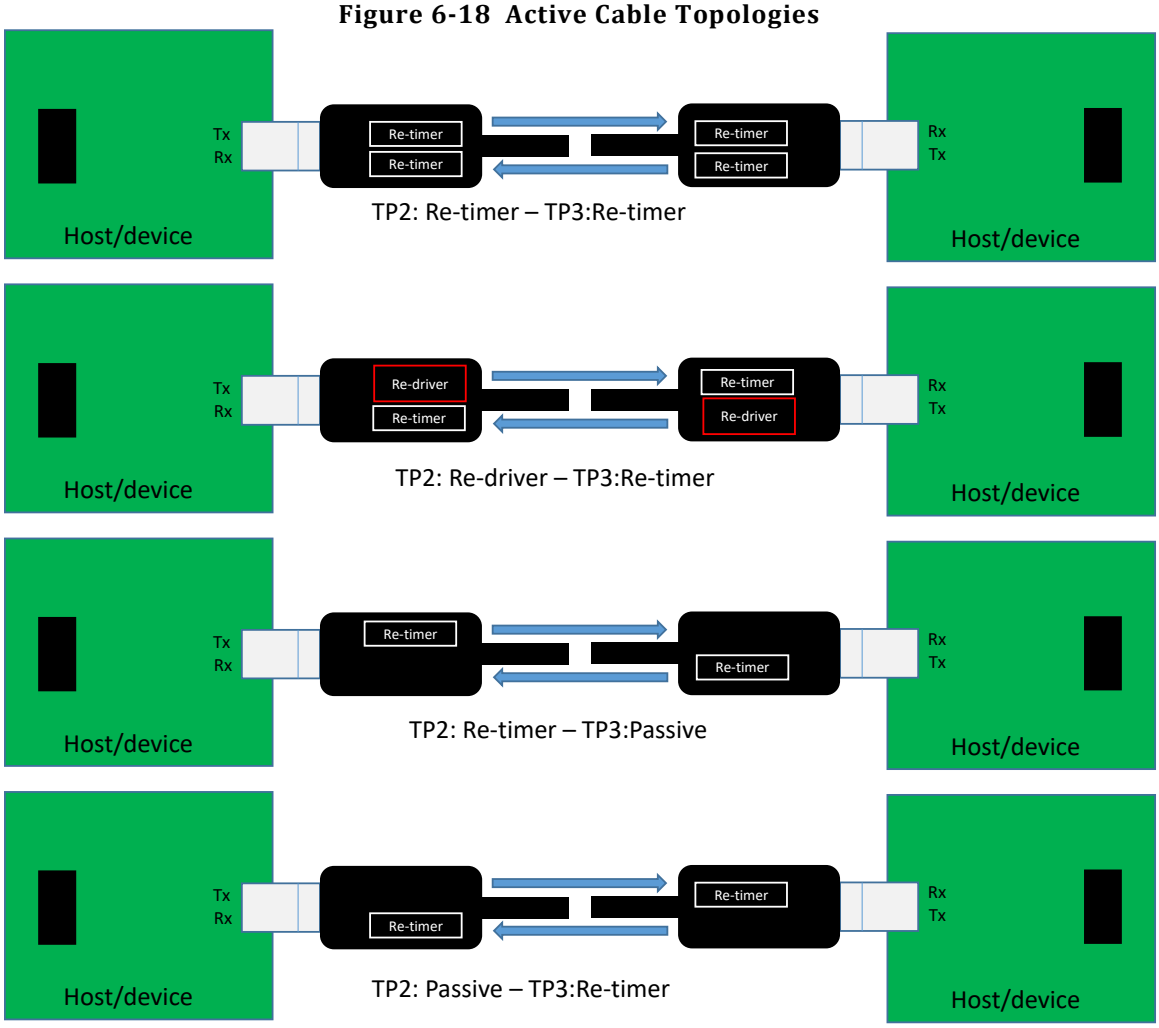
6.6.4 USB 3.2

Active cables shall meet the requirements in this section regardless of length. Active cables shall incorporate AC-coupling from the plug to repeater on both the *USB 3.2* TX and RX signals. Active cables shall provide a discharge path for discharging the AC-coupling capacitors in the cable on unplug per *USB 3.2*.

6.6.4.1 USB 3.2 Active Cable Architectures

Active cables may have the combinations of re-timers and re-drivers as illustrated in Figure 6-18. Active cables without at least one re-timer are out of scope. Active cables without re-timers connected to TP3 are out of scope. Active cables shall support the features defined in Table 6-2.

Figure 6-18 Active Cable Topologies



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

OIAC 应实现 tDisableCount 计数器来确定电缆从 *USB 3.2* 转换到 *USB 2.0* 的次数。在以下任一情况下，tDisableCount 计数器应重置为零：

• OIAC 上电复位，或 • 成功转换至 *USB 3.2* U0。

当 tDisableCount 计数器达到三时，OIAC 应显示并锁存 *USB 2.0* 广告牌。

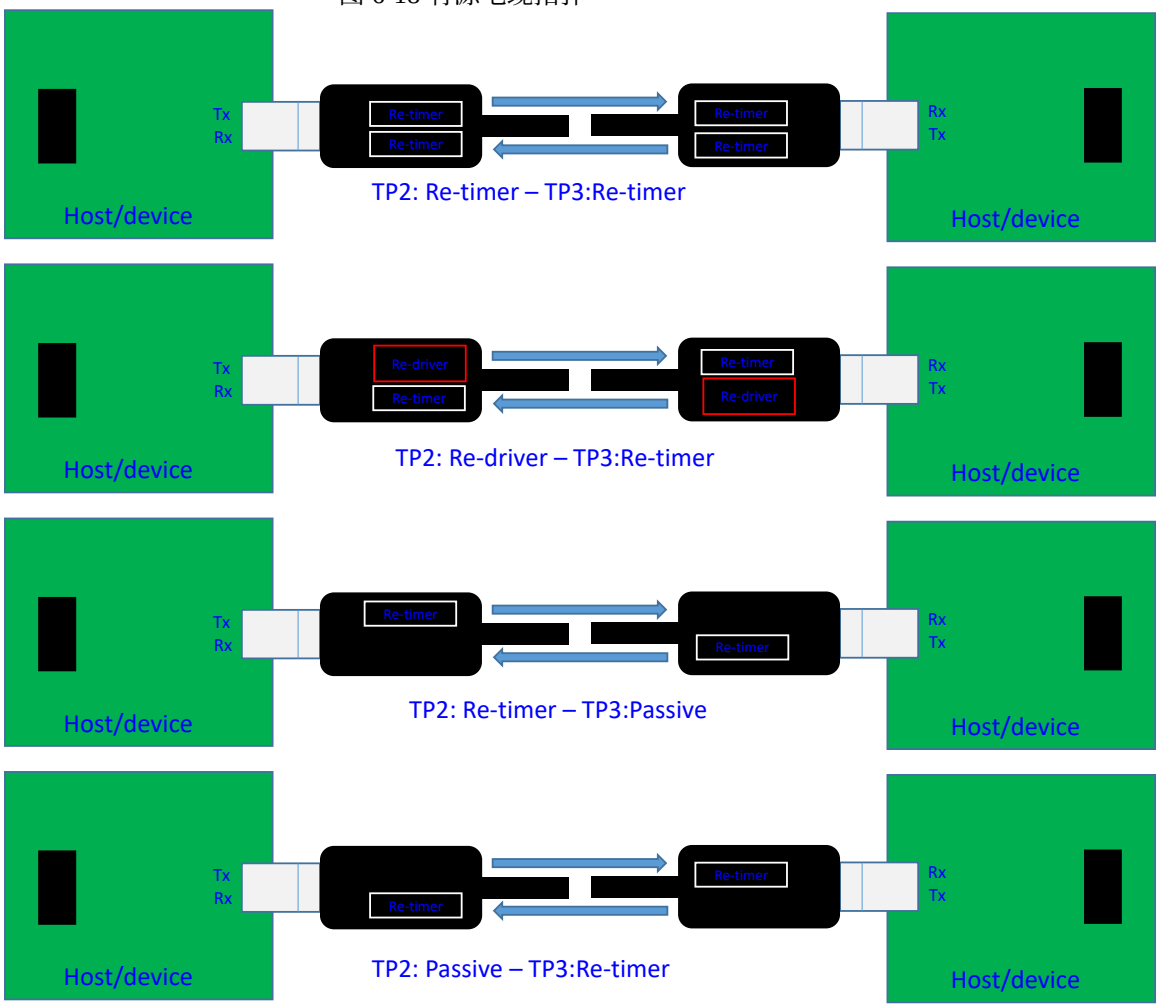
6.6.4 USB 3.2

有源电缆无论长度如何都应满足本节的要求。有源电缆应在 *USB 3.2* TX 和 RX 信号上包含从插头到中继器的交流耦合。有源电缆应提供放电路径，以便在拔出插头时放电电缆中的交流耦合电容器（按照 *USB 3.2*）。

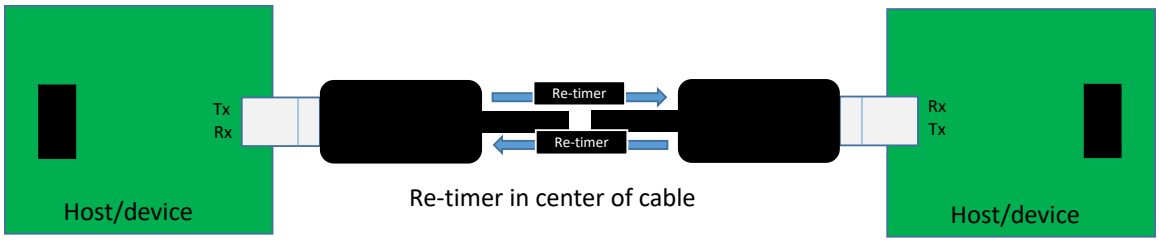
6.6.4.1 USB 3.2 有源电缆架构

有源电缆可能具有如图 6-18 所示的重定时器和重驱动器组合。没有至少一个重定时器的有源电缆不在范围内。没有连接到 TP3 的重定时器的有源电缆不在范围内。有源电缆应支持表 6-2 中定义的功能。

图 6-18 有源电缆拓扑



版权所有 © 2019 USB 3.0 Promoter Group。保留所有权利。



6.6.4.2 USB 3.2 Power-on and Rx.Detect

Active cables shall present a high impedance to ground of $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ when not powered. Active cables shall present a high impedance to ground of $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ at initial power-on. The active cable shall perform far-end receiver termination detection on both cable ends upon receiving V_{CONN}. Upon detecting a far-end low-impedance receiver termination ($R_{RX\text{-}DC}$), the active cable shall enable its low-impedance receiver termination ($R_{RX\text{-}DC}$) to mirror the presence of the Host/Device. The active cable shall perform far-end receiver termination detection for Repeaters per *USB 3.2* including in low power states U2/U3.

An active cable shall complete power-on and far-end receiver termination detection through the cable within $t_{FWD_RX.DETECT}$.

Table 6-16 Active Cable Power-on Requirements

Name	Minimum	Maximum	Units
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	Per *USB 3.2*	Per *USB 3.2*	
$R_{RX\text{-}DC}$	Per *USB 3.2*	Per *USB 3.2*	
$t_{FWD_RX.DETECT}$		42[1]	Ms

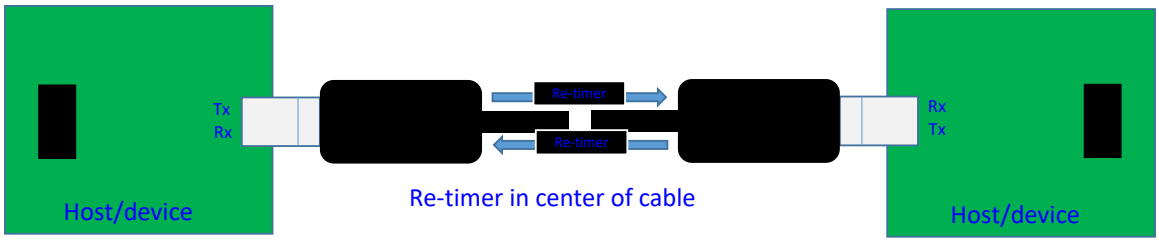
Note 1: 84 ms – (2 * 12 ms + 18 ms) worst case.

Active cables including OIACs shall reflect the receiver terminations across the cable to replicate the behavior of a passive cable.

6.6.4.3 USB 3.2 U0 Delay

All active cables shall meet the *USB 3.2* delay defined in Table 6-17.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.



6.6.4.2 USB 3.2 开机和接收检测

未通电时，有源电缆对地应呈现 $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ 的高阻抗。首次通电时，有源电缆对地应呈现 $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ 的高阻抗。有源电缆在接收 VCONN 时应在电缆两端执行远端接收器终端检测。检测到远端低阻抗接收器终端 ($R_{RX\text{-}DC}$) 后，有源电缆应启用其低阻抗接收器终端 ($R_{RX\text{-}DC}$) 以镜像主机/设备的存在。有源电缆应根据 *USB 3.2* 对中继器执行远端接收器终端检测，包括在低功率状态 U2/U3 下。

有源电缆应在 $t_{FWD_RX.DETECT}$ 内通过电缆完成电源开启和远端接收器终端检测。

表 6-16 有源电缆通电要求

Name	Minimum	Maximum	Units
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	Per *USB 3.2*	Per *USB 3.2*	
$R_{RX\text{-}DC}$	Per *USB 3.2*	Per *USB 3.2*	
$t_{FWD_RX.DETECT}$		42[1]	Ms

注 1：84 毫秒 – (2 * 12 毫秒 + 18 毫秒) 最坏情况。

包括 OIAC 在内的有源电缆应反映电缆上的接收器端接，以复制无源电缆的行为。

6.6.4.3 USB 3.2 U0 延迟

所有有源电缆应满足表 6-17 中定义的 *USB 3.2* 延迟。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table 6-17 OIAC Maximum USB 3.2 U0 Delay

USB 3.2 Gen	Cable Maximum U0 Delay	Description
Gen1	3000 ns	Active cables with *USB 3.2* Gen1 latency larger than 125 ns may not function correctly when used in conjunction with host, devices, and hubs which do not support the extended timers required in the USB 3.1 Specification Revision 1.0 (July 26, 2013) and USB 3.1 Pending_HP_Timer ECN.
Gen2	3000 ns	Active cables with *USB 3.2* Gen2 latency larger than 305 ns may not function correctly when used in conjunction with host, devices, and hubs which do not support the extended timers required in the USB 3.1 Specification Revision 1.0 (July 26, 2013) and USB 3.1 Pending_HP_Timer ECN.

6.6.4.3.1 OIAC Legacy Adapter

Table 6-18 defines the all scenarios in which an OIAC will not function without an OIAC legacy adapter between the OIAC and the Legacy Device, Hub, or Host.

The OIAC Adapter requires the following capabilities:

1. USB Type-C DRP/Source on the upward facing port connected to the OIAC,
2. *USB PD* on the upward facing port connected to the OIAC,
3. *USB 3.2* Hub incorporating the Pending_HP_Timer ECN, and
4. Optional: *USB 2.0* to *USB 3.2* transaction translator on the downstream facing port (only needed if connecting to *USB 2.0*-only devices, hubs, or hosts).

Table 6-18 Usages for OIAC That Require an Adapter or Hub

USB Device, Hub, or Host Scenarios which require an OIAC Adapter					
Connector	**Power Role**	**Data Role**	**USB PD**	**USB 3.2 Generation**	**USB 2.0**
USB Type-C	Sink only	-	-	-	-
	-	UFP only	-	-	-
	DRP	UFP only DRD	No USB PD	-	-
			USB PD R2/R3	USB 3.2 without the Pending_HP_Timer ECN	-
			-	-	USB 2.0 only
Any non-USB Type-C	-	-	-	-	-

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 6-17 OIAC 最大 USB 3.2 U0 延迟

USB 3.2 Gen	Cable Maximum U0 Delay	Description
Gen1	3000 ns	Active cables with *USB 3.2* Gen1 latency larger than 125 ns may not function correctly when used in conjunction with host, devices, and hubs which do not support the extended timers required in the USB 3.1 Specification Revision 1.0 (July 26, 2013) and USB 3.1 Pending_HP_Timer ECN.
Gen2	3000 ns	Active cables with *USB 3.2* Gen2 latency larger than 305 ns may not function correctly when used in conjunction with host, devices, and hubs which do not support the extended timers required in the USB 3.1 Specification Revision 1.0 (July 26, 2013) and USB 3.1 Pending_HP_Timer ECN.

6.6.4.3.1 OIAC 旧版适配器

表 6-18 定义了如果 OIAC 与旧设备、集线器或主机之间没有 OIAC 旧适配器，OIAC 将无法运行的所有场景。

OIAC 适配器需要以下功能：

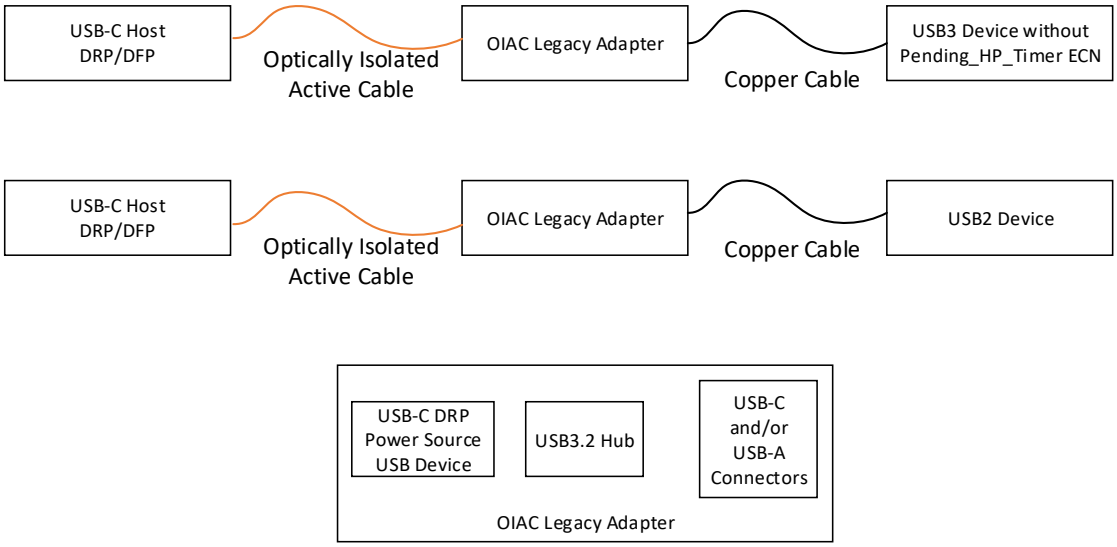
1. 连接到 OIAC 的向上端口上的 USB Type-C DRP/Source，2. 连接到 OIAC 的向上端口上的 *USB PD*，3. 包含 Pending_HP_Timer ECN 的 *USB 3.2* Hub，以及 4. 可选：向下端口上的 *USB 2.0* 至 *USB 3.2* 事务转换器（仅在连接到仅限 *USB 2.0* 的设备、集线器或主机时才需要）。

表 6-18 需要适配器或集线器的 OIAC 用法

USB Device, Hub, or Host Scenarios which require an OIAC Adapter					
Connector	**Power Role**	**Data Role**	**USB PD**	**USB 3.2 Generation**	**USB 2.0**
USB Type-C	Sink only	-	-	-	-
	-	UFP only	-	-	-
	DRP	UFP only DRD	No USB PD	-	-
			USB PD R2/R3	USB 3.2 without the Pending_HP_Timer ECN	-
			-	-	USB 2.0 only
Any non-USB Type-C	-	-	-	-	-

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure 6-19 Illustrations of Usages for OIAC That Require an Adapter or Hub



6.6.4.4 USB 3.2 U-State Power Requirements

Active cables shall meet the VCONN power requirements in Table 6-19. These requirements are for the entire cable not just a cable plug.

Table 6-19 USB 3.2 U-State Requirements

State	Maximum Power Consumption VCONN	Target Power Consumption VCONN	Power Consumption Notes
U0	1.0 W single-lane 1.5 W dual-lane		Applies to POLLING.LFPS, TRAINING, and RECOVERY states.
U1	≤ U0 power		Forwarding LFPS is required
U2	≤ U1 power		Forwarding LFPS is required
U3	5 mW	2 mW	eMarker in sleep.
Rx.Detect	5 mW	2 mW	Rx.Detect period may be lengthened when no *USB 3.2* terminations have been detected. eMarker in sleep.
eSS.Disabled	5 mW	1 mW	*USB 3.2* is disabled. eMarker in sleep.

Note: Ra must be completely removed or very high impedance to meet the power requirements in U3, Rx.Detect, and eSS.Disabled.

6.6.4.5 USB 3.2 U-State Exit Latency

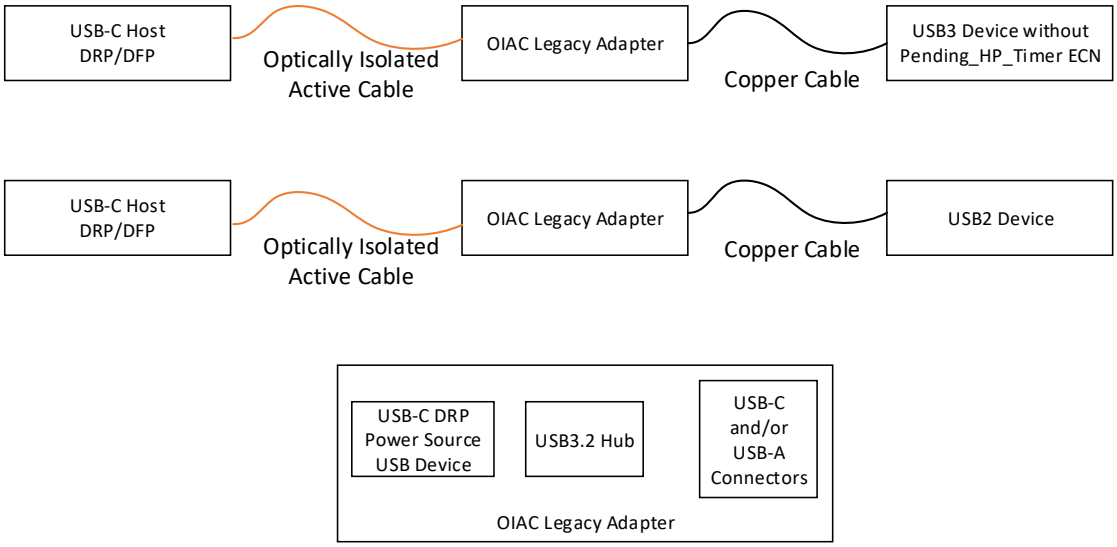
Active cables shall meet the U-state exit latency defined in *USB 3.2* Appendix E.

6.6.4.6 USB 3.2 Signal Swing

An active cable transmitter only has to drive 8.5 dB insertion loss at 5 GHz to the Host/Device controller receiver for *USB 3.2* Gen2, if the transmitter is located in the cable plug next to the receiving port.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 6-19 需要适配器或集线器的 OIAC 用法说明



6.6.4.4 USB 3.2 U 状态电源要求

有源线缆应满足表 6-19 中的 VCONN 电源要求。这些要求适用于整条线缆，而不仅仅是线缆插头。

表 6-19 USB 3.2 U-State 要求

State	Maximum Power Consumption VCONN	Target Power Consumption VCONN	Power Consumption Notes
U0	1.0 W single-lane 1.5 W dual-lane		Applies to POLLING.LFPS, TRAINING, and RECOVERY states.
U1	≤ U0 power		Forwarding LFPS is required
U2	≤ U1 power		Forwarding LFPS is required
U3	5 mW	2 mW	eMarker in sleep.
Rx.Detect	5 mW	2 mW	Rx.Detect period may be lengthened when no *USB 3.2* terminations have been detected. eMarker in sleep.
eSS.Disabled	5 mW	1 mW	*USB 3.2* is disabled. eMarker in sleep.

注意：必须完全移除 Ra 或使其具有非常高的阻抗才能满足 U3、Rx.Detect 和 eSS.Disabled 中的功率要求。

6.6.4.5 USB 3.2 U 状态退出延迟

有源电缆应满足*USB 3.2*附录 E 中定义的 U 状态退出延迟。

6.6.4.6 USB 3.2 信号摆幅

对于 *USB 3.2* Gen2，如果有源电缆发射器位于接收端口旁边的电缆插头中，则它仅需在 5 GHz 下向主机/设备控制器接收器驱动 8.5 dB 的插入损耗。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A Host/Device controller transmitter must drive a total loss of 23 dB at 5 GHz to the far side for *USB 3.2* Gen2. The difference in loss budget allows the active cable transmitter swing to be reduced. An active cable receiver can assume a larger receiver swing than in the Host/Device for the same reason.

Figure 6-20 defines the SuperSpeed electrical test points and is copied from the *USB 3.2* specification. Figure 6-21 indicates the test points and test equipment connections.

Figure 6-20 SuperSpeed USB Electrical Test Points

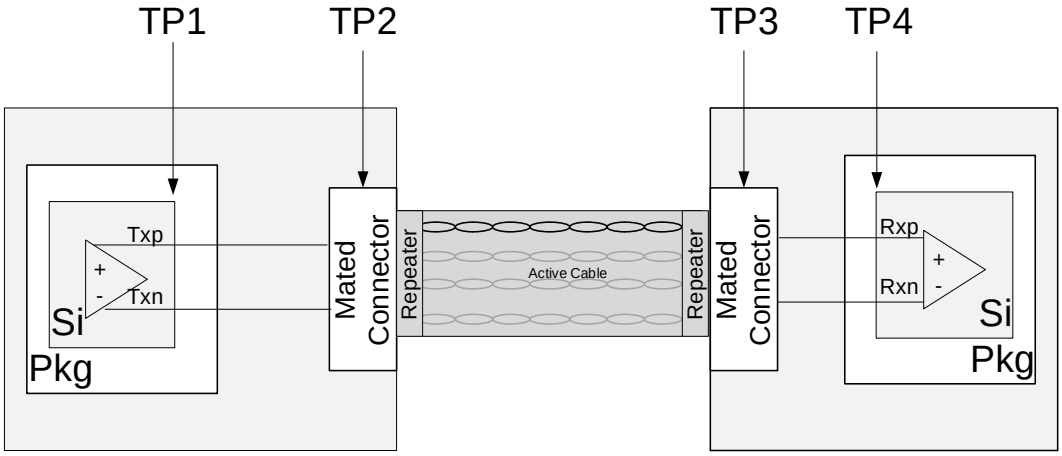
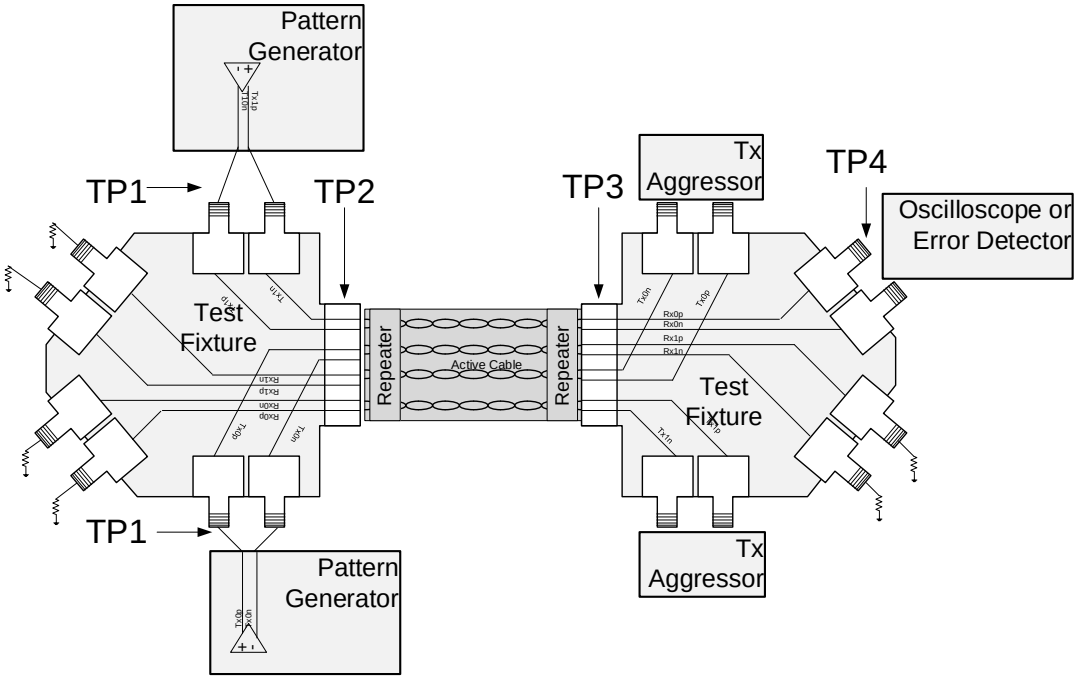


Figure 6-21 SuperSpeed USB Compliance Test Setup



6.6.4.6.1 TP1 – Active Cable Input Stressed Source

The active cable input stressed source is generated at TP1 per Table 6-20 for amplitude and per Table 6-21 for jitter. SSC shall be present in the stressed signal at TP1. Table 6-20 is a subset of the *USB 3.2* Table 6-18. Table 6-21 is a subset of *USB 3.2* Table 6-28. If any

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

对于 *USB 3.2* Gen2，主机/设备控制器发射器必须在 5 GHz 下将总损耗驱动至远端 23 dB。损耗预算的差~~异允许~~降低有源电缆发射器摆幅。出于同样的原因，有源电缆接收器可以假设比主机/设备中更大的接收器摆幅。

图 6-20 定义了超高速电气测试点，是从 *USB 3.2* 规范中复制而来。图 6-21 显示了测试点和测试设备连接。

图 6-20 超高速 USB 电气测试点

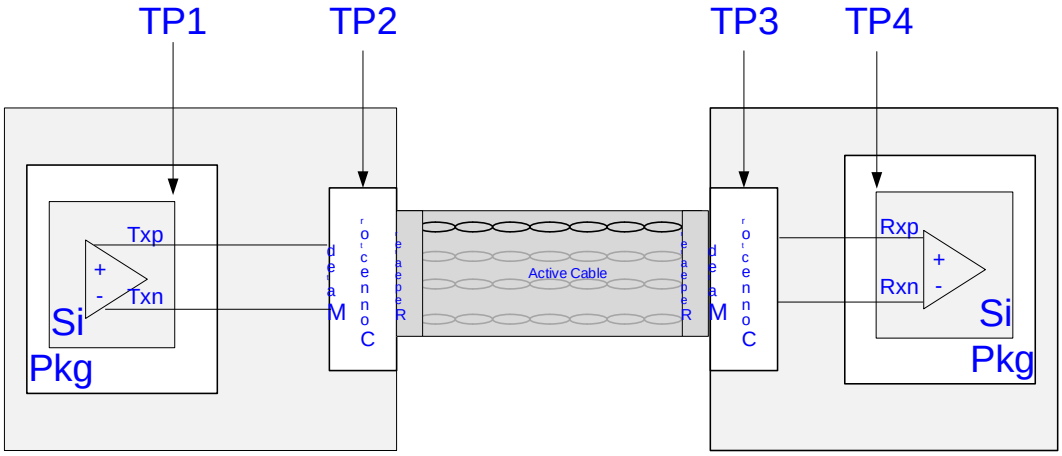
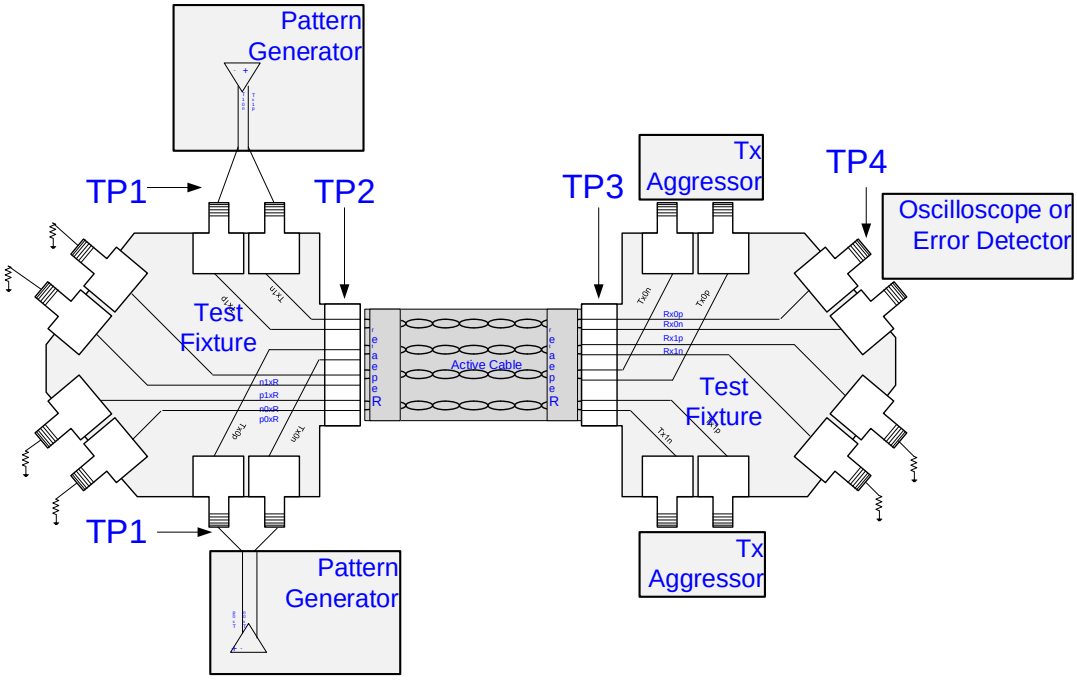


图 6-21 SuperSpeed USB 一致性测试设置



6.6.4.6.1 TP1 – 有源电缆输入应力源

有源电缆输入应力源在 TP1 处生成，幅度见表 6-20，抖动见表 6-21。SSC 应出现在 TP1 处的应力信号中。表 6-20 是 *USB 3.2* 表 6-18 的子集。表 6-21 是 *USB 3.2* 表 6-28 的子集。如果有

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

discrepancy exists between this specification and the *USB 3.2* specification, the *USB 3.2* specification shall take precedence.

The maximum swing with the maximum de-emphasis and pre-shoot shall be tested with the minimum loss compliance test board. The minimum swing with the minimum de-emphasis and pre-shoot shall be tested with the maximum loss compliance test board. The input jitter composition is the same for both the minimum and maximum swing stressed sources.

The active cable shall function over the range of parameter in *USB 3.2* Table 6-17 and Table 6-20.

Table 6-20 Active Cable USB 3.2 Stressed Source Swing, TP1

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p TX voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX\text{-}DE\text{-}RATIO}$	TX de-emphasis	*USB 3.2* Table 6-17	−3.1 ± 1.0	dB	Nominal is 3.5 dB for Gen1 operation. Gen2 transmitter equalization requirements are described in *USB 3.2* Section 6.7.5.2.
$V_{PRESHOOT}$	TX Preshoot	*USB 3.2* Table 6-17	2.2 ± 1.0	dB	Gen2 transmitter equalization requirements are described in *USB 3.2* Section 6.7.5.2.

Table 6-21 Active Cable USB 3.2 Stressed Source Jitter, TP1

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.0100	UI rms	1
$J_{Rj_p\text{-}p}$	Random Jitter peak-peak at 10^{-12}	0.17	0.14	UI p-p	1,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2	4.76	UI p-p	1,2,3
J_{Pj_1Mhz}	Sinusoidal Jitter	1	2.03	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	0.87	UI p-p	1,2,3
J_{Pj_4MHz}	Sinusoidal Jitter	N/A	0.37	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p	1,2,3

Notes:

1. All parameters measured at TP1. The test point is shown in Figure 6-20 and Figure 6-21.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the RX is required to tolerate Pj at all frequencies between the compliance test points.
3. During the RX tolerance test, SSC is generated by test equipment and present at all times. Each JPj source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the RX tolerance test.
5. The JTOL specs for Gen2 comprehend jitter peaking with re-timers in the system and has a 25 dB/decade slope.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

若本规范与*USB 3.2*规范存在差异，则以*USB 3.2*规范为准。

最大摆幅与最大去加重和预冲应使用最小损耗合规性测试板进行测试。最小摆幅与最小去加重和预冲应使用最大损耗合规性测试板进行测试。最小和最大摆幅应力源的输入抖动成分相同。

有源电缆应在*USB 3.2*表 6-17 和表 6-20 中的参数范围内发挥作用。

表 6-20 有源电缆 USB 3.2 压力源摆幅，TP1

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p TX voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX\text{-}DE\text{-}RATIO}$	TX de-emphasis	*USB 3.2* Table 6-17	−3.1 ± 1.0	dB	Nominal is 3.5 dB for Gen1 operation. Gen2 transmitter equalization requirements are described in *USB 3.2* Section 6.7.5.2.
$V_{PRESHOOT}$	TX Preshoot	*USB 3.2* Table 6-17	2.2 ± 1.0	dB	Gen2 transmitter equalization requirements are described in *USB 3.2* Section 6.7.5.2.

表 6-21 有源电缆 USB 3.2 压力源抖动，TP1

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.0100	UI rms	1
$J_{Rj_p\text{-}p}$	Random Jitter peak-peak at 10^{-12}	0.17	0.14	UI p-p	1,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2	4.76	UI p-p	1,2,3
J_{Pj_1Mhz}	Sinusoidal Jitter	1	2.03	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	0.87	UI p-p	1,2,3
J_{Pj_4MHz}	Sinusoidal Jitter	N/A	0.37	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p	1,2,3

不 测试：1. 所有参数均在 TP1 处测量。测试点如图 6-20 和图 6-21 所示。2. 由于合规性测试的时间限制，只能测试一部分频率。但是，要求 RX 能够容忍合规性测试点之间所有频率的 Pj。3. 在 RX 容忍度测试期间，测试设备会生成 SSC，并且始终存在。然后添加每个 JPj 源，并逐个测试其是否符合规范限制。4. 在 RX 容忍度测试期间也存在随机抖动。5. Gen2 的 JTOL 规范包括系统中重定时器的抖动峰值，斜率为 25 dB/十进制。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.6.4.6.2 TP2 – Active Cable Input (Informative)

The values in Table 6-22 indicate the informative input signal swings at TP2 for an active cable. Table 6-22 is included to provide guidance beyond the normative requirements of Table 6-20 and Table 6-21. An active cable can be fully compliant with the normative requirements of this specification and not meet all the values in Table 6-22. Similarly, an active cable that meets all the values in Table 6-22, is not guaranteed to be in fully compliance with the normative part of this specification.

Table 6-22 Active Cable USB 3.2 Input Swing at TP2 (Informative)

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p TX voltage swing	250 (min) 1000 (max)	250 (min) 850 (max)	mV	Nominal is 550 mV p-p
$V_{TX\text{-}DE\text{-}RATIO}$	TX de-emphasis	0 (min) 4.0 (max)	2.1 (min) 4.1 (max)	dB	There is no de-emphasis requirement for Gen1.
$V_{PRESHOOT}$	TX Preshoot	NA	1.2 (min) 3.2 (max)	dB	Applicable to *USB 3.2* Gen2 operation only.

6.6.4.6.3 TP3 – Active Cable Output (Informative)

The values in Table 6-23 indicate the informative output signal swings at TP3 for an active cable. Table 6-23 is included to provide guidance beyond the normative requirements of Table 6-20 and Table 6-21. An active cable can be fully compliant with the normative requirements of this specification and not meet all the values in Table 6-23. Similarly, an active cable that meets all the values in Table 6-23, is not guaranteed to be in full compliance with the normative part of this specification.

Table 6-23 Active Cable USB 3.2 Output Swing at TP3 (Informative)

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential RX peak-to-peak voltage	300 (min) 850 (max)	300 (min) 850 (max)	mV	Measured after the RX EQ function Nominal is 0.5 V p-p
$V_{TX\text{-}DE\text{-}RATIO\text{-}GEN1}$	TX de-emphasis	0 (min) 4.0 (max)	NA	dB	No pre-shoot allowed
$V_{TX\text{-}DE\text{-}RATIO}$ + $V_{PRESHOOT\text{-}GEN2}$	TX de-emphasis + TX Preshoot	NA	0 (min) 3.0 (max)	dB	Sum of the de-emphasis and pre-shoot. There is no de-emphasis and pre-shoot requirement.

6.6.4.6.4 TP4 – Active Cable Output

The active cable transmitter output is defined at TP4 for both high and low loss channels. The requirements for TP4 are defined in the *USB 3.2* specification Table 6-20. The input signal for the test shall be applied at TP1 as defined in the *USB 3.2* specification.

The low loss test board shall be used to test the maximum output swing. The maximum loss test board shall be used to test the minimum output swing. Jitter must be met with both test boards.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

6.6.4.6.2 TP2 – 有源电缆输入（参考）

表 6-22 中的值表示有源电缆在 TP2 处的输入信号摆动情况。表 6-22 旨在提供超出表 6-20 和表 6-21 的规范要求的指导。有源电缆可以完全符合本规范的规范要求，但不能满足表 6-22 中的所有值。同样，满足表 6-22 中所有值的有源电缆不能保证完全符合本规范的规范部分。

表 6-22 TP2 处的有源电缆 USB 3.2 输入摆幅（参考）

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p TX voltage swing	250 (min) 1000 (max)	250 (min) 850 (max)	mV	Nominal is 550 mV p-p
$V_{TX\text{-}DE\text{-}RATIO}$	TX de-emphasis	0 (min) 4.0 (max)	2.1 (min) 4.1 (max)	dB	There is no de-emphasis requirement for Gen1.
$V_{PRESHOOT}$	TX Preshoot	NA	1.2 (min) 3.2 (max)	dB	Applicable to *USB 3.2* Gen2 operation only.

6.6.4.6.3 TP3 – 有源电缆输出（参考）

表 6-23 中的值表示有源电缆在 TP3 处的输出信号摆幅。表 6-23 旨在提供超出表 6-20 和表 6-21 规范要求的指导。有源电缆可以完全符合本规范的规范要求，但不能满足表 6-23 中的所有值。同样，满足表 6-23 中所有值的有源电缆不能保证完全符合本规范的规范部分。

表 6-2 3 有源电缆 USB 3.2 在 TP3 处的输出摆幅（信息 原生的)

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential RX peak-to-peak voltage	300 (min) 850 (max)	300 (min) 850 (max)	mV	Measured after the RX EQ function Nominal is 0.5 V p-p
$V_{TX\text{-}DE\text{-}RATIO\text{-}GEN1}$	TX de-emphasis	0 (min) 4.0 (max)	NA	dB	No pre-shoot allowed
$V_{TX\text{-}DE\text{-}RATIO}$ + $V_{PRESHOOT\text{-}GEN2}$	TX de-emphasis + TX Preshoot	NA	0 (min) 3.0 (max)	dB	Sum of the de-emphasis and pre-shoot. There is no de-emphasis and pre-shoot requirement.

6.6.4.6.4 TP4 – 有源电缆输出

有源电缆发射器输出在 TP4 处定义，适用于高损耗和低损耗通道。TP4 的要求在 *USB 3.2* 规范表 6-20 中定义。测试的输入信号应按照 *USB 3.2* 规范中的定义应用于 TP1。

低损耗测试板用来测试最大输出摆幅，最大损耗测试板用来测试最小输出摆幅，两块测试板均需满足抖动要求。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

The active cable bit-error-rate shall be tested at TP4 and meet or exceed a BER of 10^{-12}. The error detector used shall have the ability to remove SKP ordered sets.

6.6.5 Return Loss

Return loss is defined in the *USB 3.2* specification.

6.7 Active Cables That Support Alternate Modes

Active cables may support Alternate Modes. Active cables that support Alternate Modes shall be discoverable via *USB PD*. They shall use the standard *USB PD* mechanisms to discover, enter and exit Alternate Modes.

6.7.1 Discover SVIDs

Active cables that support an Alternate Mode shall report support for SVIDs on SOP' only.

6.7.2 Discover Modes

Active cables that support an Alternate Mode shall report support for Modes on SOP' only.

6.7.3 Enter/Exit Modes

Enter and ***Exit*** mode shall be communicated on SOP' and on SOP'' when the SOP'' Controller Present bit is set in the Active Cable. It is recommended that ***Enter Mode*** be sent initially to SOP' and then SOP" if supported and then SOP. It is recommended ***Exit Mode*** be sent initially to SOP and then to SOP" if supported and then SOP'.

6.7.4 Power in Alternate Modes

The power dissipation in an active cable's Alternate Mode shall maintain the plug's Maximum Skin Temperature below the requirement defined in Table 6-14.

Alternate Modes should reduce power in active cables in sleep states for best user experience.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

应在 TP4 处测试活动电缆的误码率，并达到或超过 BER 10^{-12}。所用的错误检测器应能够删除 SKP 有序集。

6.6.5 回波损耗

回波损耗在*USB 3.2*规范中定义。

6.7 支持交替模式的有源电缆

有源电缆可能支持备用模式。支持备用模式的有源电缆应可通过 *USB PD* 发现。它们应使用标准 *USB PD* 机制来发现、进入和退出备用模式。

6.7.1 发现 SVID

有源电缆 支持替代模式应报告对 S 的支持 仅限 SOP 上的 VID。

6.7.2 发现模式

支持替代模式的有源电缆应仅报告对 SOP 上的模式的支持。

6.7.3 进入/退出模式

当活动电缆中的 SOP’’控制器存在位被设置时，***Enter*** 和 ***Exit*** 模式应在 SOP’和 SOP’’上进行通信。建议首先将 ***Enter Mode*** 发送到 SOP’，然后如果支持则发送到 SOP”，然后发送到 SOP。建议首先将 ***Exit Mode*** 发送到 SOP，然后如果支持则发送到 SOP”，然后发送到 SOP’。

6.7.4 备用模式下的电源

有源电缆交替模式下的功率耗散应保持插头的最高表面温度低于表 6-14 定义的要求。

替代模式应减少睡眠状态下活动电缆的功率，以获得最佳用户体验。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A Audio Adapter Accessory Mode

A.1 Overview

Analog audio headsets are supported by multiplexing four analog audio signals onto pins on the USB Type-C® connector when in the Audio Adapter Accessory Mode. The four analog audio signals are the same as those used by a traditional 3.5 mm headset jack. This makes it possible to use existing analog headsets with a 3.5 mm to USB Type-C adapter. The audio adapter architecture allows for an audio peripheral to provide up to 500 mA back to the system for charging.

An analog audio adapter could be a very basic USB Type-C adapter that only has a 3.5 mm jack or it could be an analog audio adapter with a 3.5 mm jack and a USB Type-C receptacle to enable charge-through. The analog audio headset shall not use a USB Type-C plug to replace the 3.5 mm plug.

A USB host that implements support for USB Type-C Analog Audio Adapter Accessory mode shall also support USB Type-C Digital Audio (TCDA) with nominally equivalent functionality and performance. A USB device that implements support for USB Type-C Analog Audio Adapter Accessory mode should also support TCDA with nominally equivalent audio functionality and performance.

A.2 Detail

An analog audio adapter shall use a captive cable with a USB Type-C plug or include an integrated USB Type-C plug.

The analog audio adapter shall identify itself by presenting a resistance to GND of ≤ Ra on both A5 (CC) and B5 (V_{CONN}) of the USB Type-C plug. If pins A5 and B5 are shorted together, the effective resistance to GND shall be less than Ra/2.

A DFP that supports analog audio adapters shall detect the presence of an analog audio adapter by detecting a resistance to GND of less than Ra on both A5 (CC) and B5 (VCONN).

Table A-1 shows the pin assignments at the USB Type-C plug that shall be used to support analog audio.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

音频适配器附件模式

A.1 概述

在音频适配器附件模式下，通过将四个模拟音频信号多路复用到 USB Type-C® 连接器上的引脚上，可支持模拟音频耳机。这四个模拟音频信号与传统 3.5 毫米耳机插孔使用的信号相同。这样就可以使用带有 3.5 毫米至 USB Type-C 适配器的现有模拟耳机。音频适配器架构允许音频外设向系统提供高达 500 mA 的电流进行充电。

模拟音频适配器可以是仅具有 3.5 毫米插孔的非常基本的 USB Type-C 适配器，也可以是具有 3.5 毫米插孔和 USB Type-C 插座的模拟音频适配器，以便实现直通充电。模拟音频耳机不得使用 USB Type-C 插头代替 3.5 毫米插头。

实现对 USB Type-C 模拟音频适配器附件模式的支持的 USB 主机还应支持具有名义上等效功能和性能的 USB Type-C ~~数字音频 (TCDA)。实现对 USB Type-C~~ 模拟音频适配器附件模式的支持的 USB 设备还应支持具有名义上等效音频功能和性能的 TCDA。

A.2 详细信息

模拟音频适配器应使用带有 USB Type-C 插头的固定电缆或包含集成的 USB Type-C 插头。

模拟音频适配器应通过在 USB Type-C 插头的 A5 (CC) 和 B5 (VCONN) 上呈现 ≤ Ra 的 GND 电阻来识别自身。如果引脚 A5 和 B5 短接在一起，则有效 GND 电阻应小于 Ra/2。

支持模拟音频适配器的 DFP 应通过检测 A5 (CC) 和 B5 (VCONN) 上小于 Ra 的 GND 电阻来检测模拟音频适配器的存在。

表 A-1 显示了用于支持模拟音频的 USB Type-C 插头的引脚分配。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

一个

Table A-1 USB Type-C Analog Audio Pin Assignments

Plug Pin	USB Name	Analog Audio Function	Location on 3.5 mm Jack	Notes
A5	CC			Connected to digital GND with resistance ≤ Ra. System uses for presence detect.
B5	VCONN			Connected to digital GND with resistance ≤ Ra. System uses for presence detect.
A6/B6	Dp	Right	Ring 1	Analog audio right channel A6 and B6 shall be shorted together in the adapter.
A7/B7	Dn	Left	Tip	Analog audio left channel A7 and B7 shall be shorted together in the adapter.
A8	SBU1	Mic/AGND	Ring 2	Analog audio microphone (OMTP & YD/T) or Audio GND (CTIA).
B8	SBU2	AGND/Mic	Sleeve	Audio GND (OMTP & YD/T or analog audio microphone (CTIA).
A1/A12 B1/B12	GND			Digital GND (DGND) used as the ground reference and current return for CC1, CC2, and VBUS.
A4/A9 B4/B9	VBUS			Not connected unless the audio adapter uses this connection to provide 5 V @ 500 mA for charging the system's battery.
Others				Other pins shall not be connected.

The analog audio signaling presented by the headset on the 3.5 mm jack is expected to comply with at least one of the following:

- The traditional American headset jack pin assignment, with the jack sleeve used for the microphone signal, supported by CTIA-The Wireless Association
- "Local Connectivity: Wired Analogue Audio" from the Open Mobile Terminal Forum (OMTP) forum
- "Technical Requirements and Test Methods for Wired Headset Interface of Mobile Communication Terminal" (YT/D 1885-2009) from the China Communications Standards Association

When in the Audio Adapter Accessory Mode, the system shall not provide VCONN power on either CC1 or CC2. Failure to do this may result in VCONN being shorted to GND when an analog audio peripheral is present.

The system shall connect A6/B6, A7/B7, A8 and B8 to an appropriate audio codec upon entry into the Audio Adapter Accessory Mode. The connections for A8 (SBU1) and B8 (SBU2) pins are dependent on the adapter's orientation. Depending on the orientation, the microphone and analog ground pins may be swapped. These pins are already reversed between the two major standards for headset jacks and support for this is built into the headset connection of many codecs or can be implemented using an autonomous audio headset switch. The system shall work correctly with either configuration.

A.3 Electrical Requirements

The maximum ratings for pin voltages are referenced to GND (pins A1, A12, B1, and B12). The non-GND pins on the plug shall be isolated from GND on the USB Type-C connector and shall be isolated from the USB plug shell. To minimize the possibility of ground loops

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 A-1 USB Type-C 模拟音频引脚分配

Plug Pin	USB Name	Analog Audio Function	Location on 3.5 mm Jack	Notes
A5	CC			Connected to digital GND with resistance ≤ Ra. System uses for presence detect.
B5	VCONN			Connected to digital GND with resistance ≤ Ra. System uses for presence detect.
A6/B6	Dp	Right	Ring 1	Analog audio right channel A6 and B6 shall be shorted together in the adapter.
A7/B7	Dn	Left	Tip	Analog audio left channel A7 and B7 shall be shorted together in the adapter.
A8	SBU1	Mic/AGND	Ring 2	Analog audio microphone (OMTP & YD/T) or Audio GND (CTIA).
B8	SBU2	AGND/Mic	Sleeve	Audio GND (OMTP & YD/T or analog audio microphone (CTIA).
A1/A12 B1/B12	GND			Digital GND (DGND) used as the ground reference and current return for CC1, CC2, and VBUS.
A4/A9 B4/B9	VBUS			Not connected unless the audio adapter uses this connection to provide 5 V @ 500 mA for charging the system's battery.
Others				Other pins shall not be connected.

3.5 毫米插孔上耳机呈现的模拟音频信号预计至少符合以下要求之一：

- 传统美式耳机插孔引脚分配，插孔套管用于麦克风信号，由美国无线通信和互联网协会 (CTIA) 支持 • “ 本地连接：有线模拟音频 ”，来自开放移动终端论坛 (OMTP) 论坛 • “ 移动通信终端有线耳机接口技术要求及测试方法 ” (YT/D 1885-2009)，来自中国通信标准化协会

当处于音频适配器附件模式时，系统不应在 CC1 或 CC2 上提供 VCONN 电源。如果未这样做，则当存在模拟音频外设时，可能会导致 V CONN 短路至 GND。

系统应在进入音频适配器附件模式时将 A6/B6、A7/B7、A8 和 B8 连接到适当的音频编解码器。A8 (SBU1) 和 B8 (SBU2) 引脚的连接取决于适配器的方向。根据方向，麦克风和模拟接地引脚可能会互换。这些引脚已经在两种主要耳机插孔标准之间反转，并且许多编解码器的耳机连接都内置了对此的支持，或者可以使用自主音频耳机开关来实现。系统应在任一配置下正常工作。

A.3 电气要求

引脚电压的最大额定值以 GND（引脚 A1、A12、B1 和 B12）为基准。插头上的非 GND 引脚应与 USB Type-C 连接器上的 GND 隔离，并与 USB 插头外壳隔离。为了最大限度地减少接地环路的可能性

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

between systems, AGND shall be connected to GND only within the system containing the USB Type-C receptacle. Both the system and audio device implementations shall be able to tolerate the Right, Left, Mic, and AGND signals being shorted to GND. The current provided by the amplifier driving the Right and Left signals shall not exceed ±150 mA per audio channel, even when driving a 0 Ω load.

Table A-2 shows allowable voltage ranges on the pins in the USB Type-C plug that shall be met.

Table A-2 USB Type-C Analog Audio Pin Electrical Parameter Ratings

Plug Pin	USB Name	Analog Audio Function	Min	Max	Units	Notes
A6/B6	Dp	Right	−3.0	3.0	V	A6 and B6 shall be shorted together in the analog audio adapter
A7/B7	Dn	Left	−3.0	3.0	V	A7 and B7 shall be shorted together in the analog audio adapter
A8	SBU1	Mic/AGND	−0.4	3.3	V	
B8	SBU2	AGND/Mic	−0.4	3.3	V	

The maximum voltage ratings for Left and Right signals are selected to encompass a 2 Vrms sine wave (2.828 Vp = 5.657 Vpp = 6 dBV) which is a common full-scale voltage for headset audio output.

Headset microphones operate on a positive bias voltage provided by the system's audio codec and AC-couple the audio signal onto it. Some headsets may produce an audio signal level up to 0.5 Vrms (0.707 Vp = 1.414 Vpp = -6 dBV) but this is biased so that the voltage does not swing below GND. The bias voltage during operation is typically around 1.25 V but it varies quite a bit depending on the specifics of the manufacturer's design, therefore the maximum voltage rating for the SBU pins is selected to allow a variety of existing solutions.

While one SBU pin carries the Mic signal, the other SBU pin serves as AGND carrying the return current for Left, Right, and Mic. If we assume a worst-case headset speaker impedance of 16 Ω per speaker, then the worst-case return current for the speakers is ± 0.2 A. If we assume that the worst-case resistance from the AGND pin to GND within the USB Type-C system is 1 Ω (due to FET R_{ON} within the signal multiplexer, contact, and trace resistances), then the voltage of the AGND pin with respect to USB Type-C GND can vary between ± 0.2 V. The minimum voltage rating for the SBU pins has been selected to allow for this scenario with some additional margin to account for Mic signal return current and tolerances.

The system shall exhibit no more than -48 dB linear crosstalk between the Left and Right audio channels and exhibit no more than -51 dB linear crosstalk from the Left or Right channel to the Mic channel. Crosstalk measurements shall be made using a measurement adapter plug that supports USB Type-C analog audio connections according to Table A-1. In the measurement adapter, the Left and Right channels are terminated with 32 Ω resistors to AGND, the Mic channel is terminated with 2k Ω resistor to AGND; AGND is connected to USB Type-C Plug Pin A8, and the Mic channel is connected to USB Type-C Plug Pin B8.

Crosstalk shall be measured by using the system to drive a sine wave signal to the Left output channel and zero signal to the Right output channel. The system shall configure the Mic channel according to the default Mic operating mode supported by the system. AC voltage levels at the Left, Right and Mic channels are measured across the corresponding termination resistors using a third-octave filter at the sine signal frequency. Left – Right

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

系统之间，AGND 应仅在包含 USB Type-C 插座的系统内连接到 GND。系统和音频设备实现都应能够容忍右、左、麦克风和 AGND 信号短路到 GND。驱动右和左信号的放大器提供的电流不得超过每个音频通道 ±150 mA，即使在驱动 0 Ω 负载时也是如此。

表 A-2 显示了 USB Type-C 插头中引脚上应满足的允许电压范围。

表 A-2 USB Type-C 模拟音频引脚电气参数额定值

Plug Pin	USB Name	Analog Audio Function	Min	Max	Units	Notes
A6/B6	Dp	Right	−3.0	3.0	V	A6 and B6 shall be shorted together in the analog audio adapter
A7/B7	Dn	Left	−3.0	3.0	V	A7 and B7 shall be shorted together in the analog audio adapter
A8	SBU1	Mic/AGND	−0.4	3.3	V	
B8	SBU2	AGND/Mic	−0.4	3.3	V	

左信号和右信号的最大额定电压被选定为包含 2 Vrms 正弦波（2.828 Vp = 5.657 Vpp = 6 dBV），这是耳机音频输出的常见满量程电压。

耳机麦克风在系统音频编解码器提供的正偏置电压下工作，并将音频信号交流耦合到该电压上。一些耳机可能产生高达 0.5 Vrms（0.707 Vp = 1.414 Vpp = -6 dBV）的音频信号电平，但这是偏置的，因此电压不会低于 GND。工作期间的偏置电压通常约为 1.25 V，但根据制造商设计的具体情况会有很大差异，因此选择 SBU 引脚的最大额定电压以允许各种现有解决方案。

一个 SBU 引脚承载麦克风信号，而另一个 SBU 引脚则用作 AGND，承载左、右和麦克风的返回电流。如果我们假设最坏情况下的耳机扬声器阻抗为每个扬声器 16 Ω，则扬声器的最坏情况返回电流为 ± 0.2 A。如果我们假设 USB Type-C 系统内从 AGND 引脚到 GND 的最坏情况电阻为 1 Ω（由于信号多路复用器、接触和走线电阻内的 FET R_{ON}），则 AGND 引脚相对于 USB Type-C GND 的电压可以在 ± 0.2 V 之间变化。已选择 SBU 引脚的最小电压额定值以允许这种情况，并留有一些额外的余量来考虑麦克风信号返回电流和公差。

系统在左声道和右声道之间的线性串扰不得超过 -48 dB，从左声道或右声道到麦克风声道的线性串扰不得超过 -51 dB。串扰测量应使用支持 USB Type-C 模拟音频连接的测量适配器插头（如表 A-1 所示）进行。在测量适配器中，左声道和右声道通过 32 Ω 电阻端接至 AGND，麦克风声道通过 2k Ω 电阻端接至 AGND；AGND 连接到 USB Type-C 插头引脚 A8，麦克风声道连接到 USB Type-C 插头引脚 B8。

测量串扰时，应使用系统将正弦波信号驱动至左输出通道，将零信号驱动至右输出通道。系统应根据系统支持的默认麦克风操作模式配置麦克风通道。使用正弦信号频率的三分之一倍频程滤波器，在相应的终端电阻上测量左、右和麦克风通道的交流电压电平。左 - 右

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

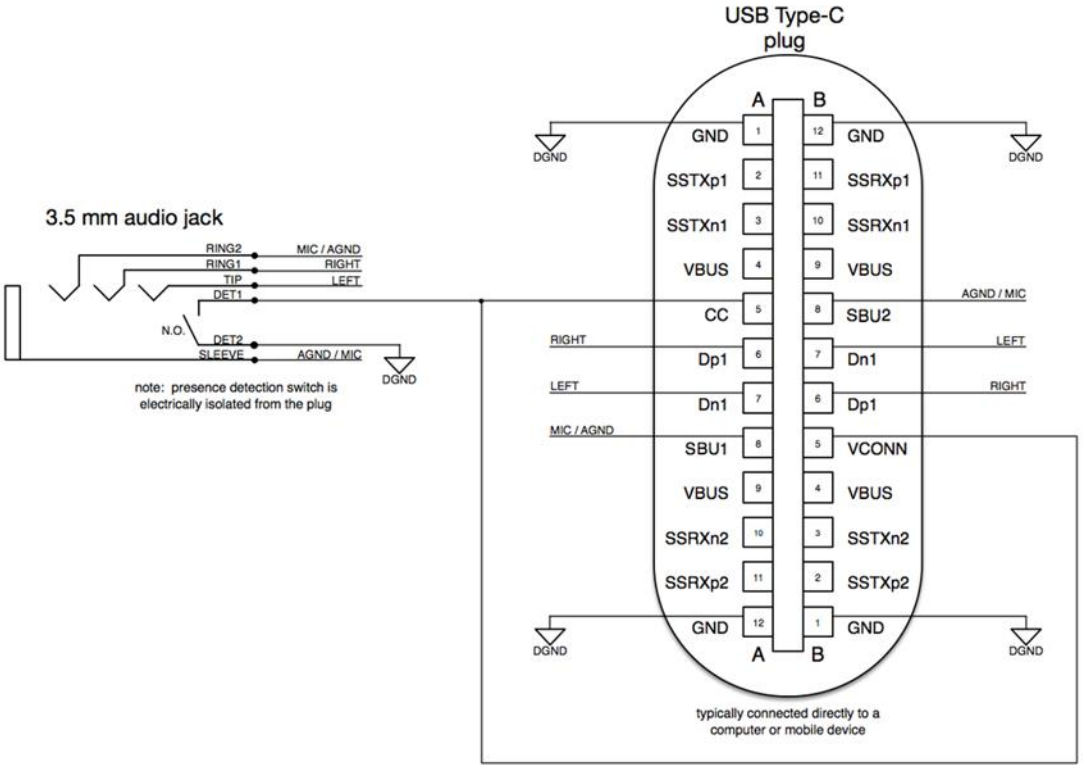
crosstalk is reported as ratio of the Right channel voltage to the Left channel voltage expressed in decibels. Similarly, the Left – Mic crosstalk is reported. The measurements shall be conducted at 31.5, 63, 125, 250, 500, 1000, 2000, 4000, 8000 and 16000 Hz frequencies. The measurements shall be repeated so that the sine wave signal is driven to the Right channel and Right – Left and Right – Mic crosstalk results are obtained. Both USB Type-C plug orientations shall be measured."

A.4 Example Implementations

A.4.1 Passive 3.5 mm to USB Type-C Adapter – Single Pole Detection Switch

Figure A-1 illustrates how a simple 3.5 mm analog audio adapter can be made. In this design, there is an audio plug that contains a single-pole detection switch that is used to completely disconnect the CC and VCONN pins from digital GND when no 3.5 mm plug is inserted. This has the effect of triggering the USB Type-C presence detect logic upon insertion or removal of either the 3.5 mm plug or the audio adapter itself.

Figure A-1 Example Passive 3.5 mm to USB Type-C Adapter



A.4.2 3.5 mm to USB Type-C Adapter Supporting 500 mA Charge-Through

Figure A-2 illustrates a 3.5 mm analog audio adapter that supports charge-through operation. Charging power comes into the adapter through a USB Type-C receptacle and is routed directly to the adapter's USB Type-C plug, which is plugged into the device being charged. This design is limited to providing 500 mA of charge-through current since it has no way to advertise greater current-sourcing capability. The USB Type-C receptacle presents Rd on both of its CC pins because a CC pull-down must be present for the receptacle to indicate that it wants to consume VBUS current. USB Type-C systems that support analog audio should ensure that charging is not interrupted by insertion or removal of the 3.5 mm audio plug and that audio is not interrupted by insertion or removal of the cable connected

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

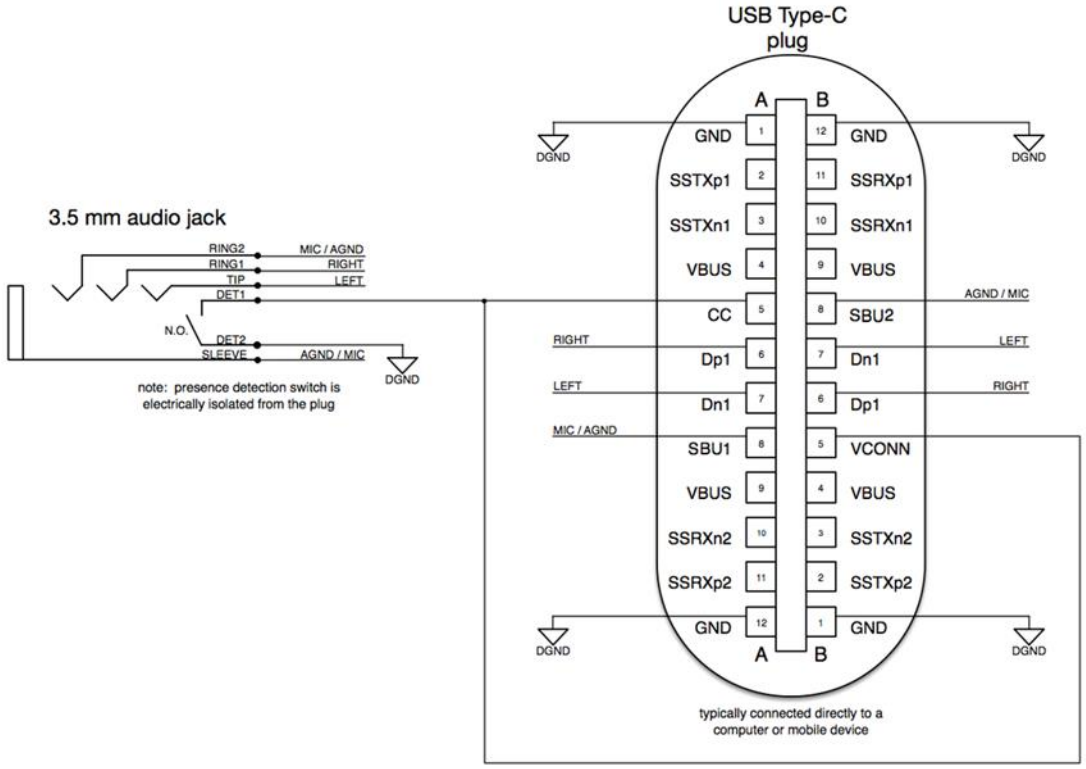
串扰以分贝表示，为右声道电压与左声道电压之比。同样，左-麦克风串扰也以分贝表示。测量应在 31.5、63、125、250、500、1000、2000、4000、8000 和 16000 Hz 频率下进行。应重复测量，以便将正弦波信号驱动到右声道并获得右-左和右-麦克风串扰结果。应测量两个 USB Type-C 插头方向。 ”

A.4 示例实现

A.4.1 无源 3.5 毫米至 USB Type-C 适配器 – 单极检测开关

图 A-1 说明了如何制作一个简单的 3.5 毫米模拟音频适配器。在此设计中，有一个音频插头，其中包含一个单极检测开关，用于在未插入 3.5 毫米插头时将 CC 和 VCONN 引脚与数字 GND 完全断开。这可以在插入或移除 3.5 毫米插头或音频适配器本身时触发 USB Type-C 存在检测逻辑。

如图图 A-1 示例 被动式 3.5 毫米转 USB Type-C A 适配器



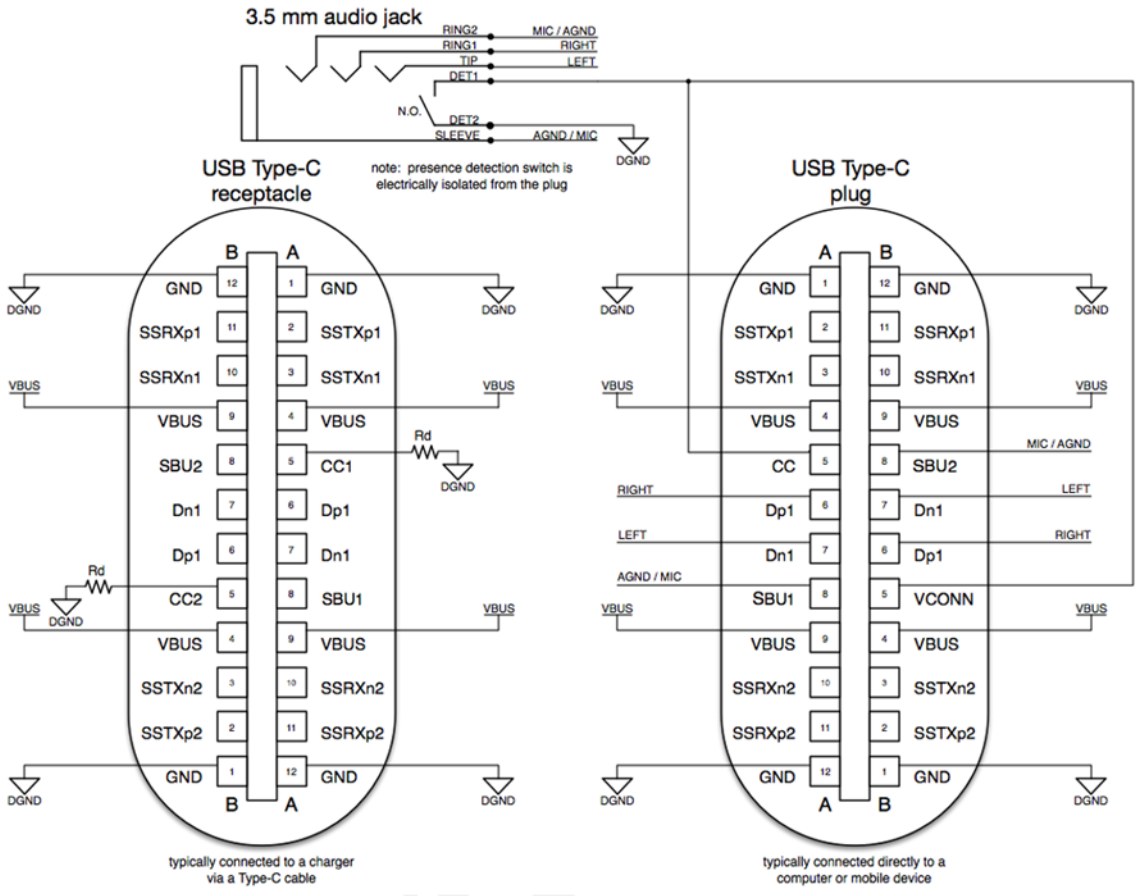
A.4.2 支持 500 mA 充电的 3.5 mm 至 USB Type-C 适配器

图 A-2 展示了支持充电操作的 3.5 毫米模拟音频适配器。充电电源通过 USB Type-C 插座进入适配器，并直接路由到适配器的 USB Type-C 插头，该插头插入正在充电的设备。由于无法提供更大的电流供应能力，因此此设计仅限于提供 500 mA 的充电电流。USB Type-C 插座在其两个 CC 引脚上都显示 Rd，因为必须存在 CC 下拉，插座才能指示它要消耗 VBUS 电流。支持模拟音频的 USB Type-C 系统应确保充电不会因插入或拔出 3.5 毫米音频插头而中断，并且音频不会因插入或拔出连接的电缆而中断

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

to the audio adapter's USB Type-C receptacle by using the system's presence detection logic monitoring the states of both the CC1 and CC2 pins and VBUS.

Figure A-2 Example 3.5 mm to USB Type-C Adapter Supporting 500 mA Charge-Through

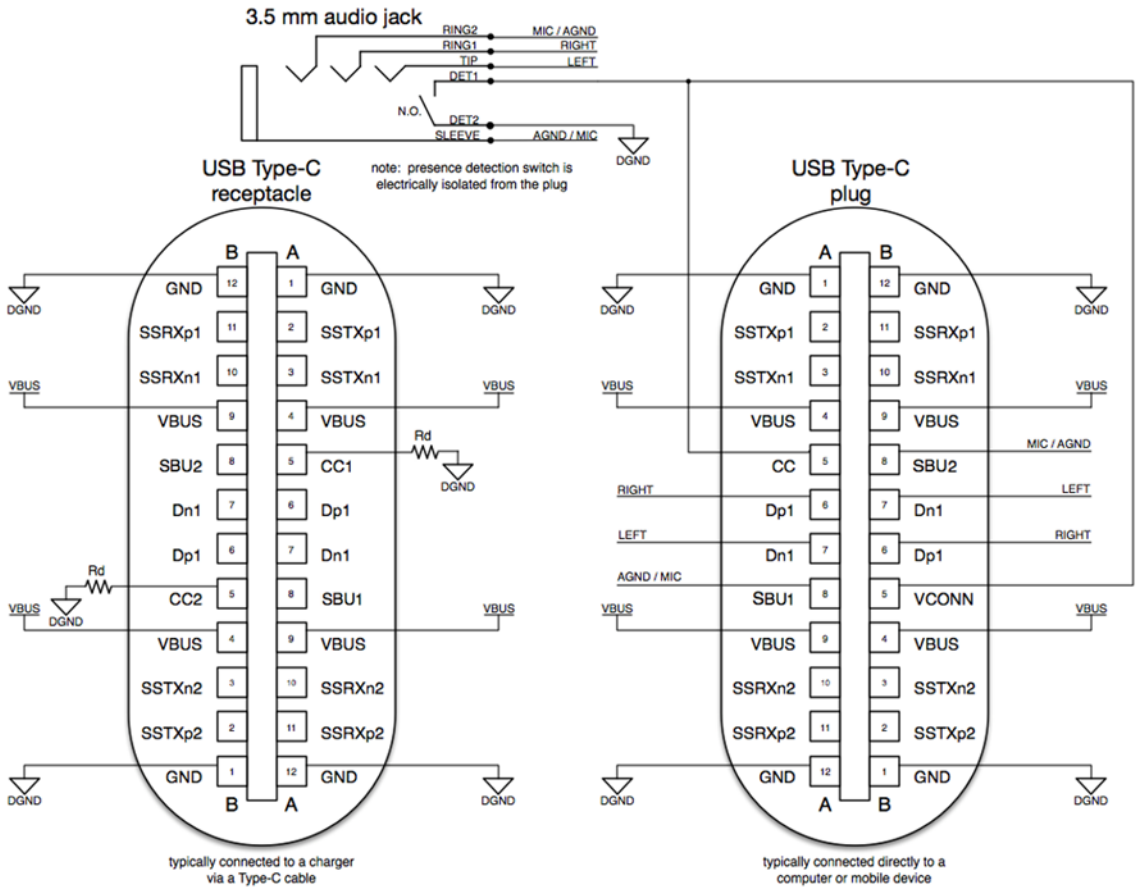


Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

通过使用系统的存在检测逻辑监控 CC1 和 CC2 引脚以及 VBUS 的状态，连接到音频适配器的 USB Type-C 插座。

图 A-2 支持 500 mA 充电的 3.5 mm 至 USB Type-C 适配器示例

Through



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B Debug Accessory Mode

B.1 Overview

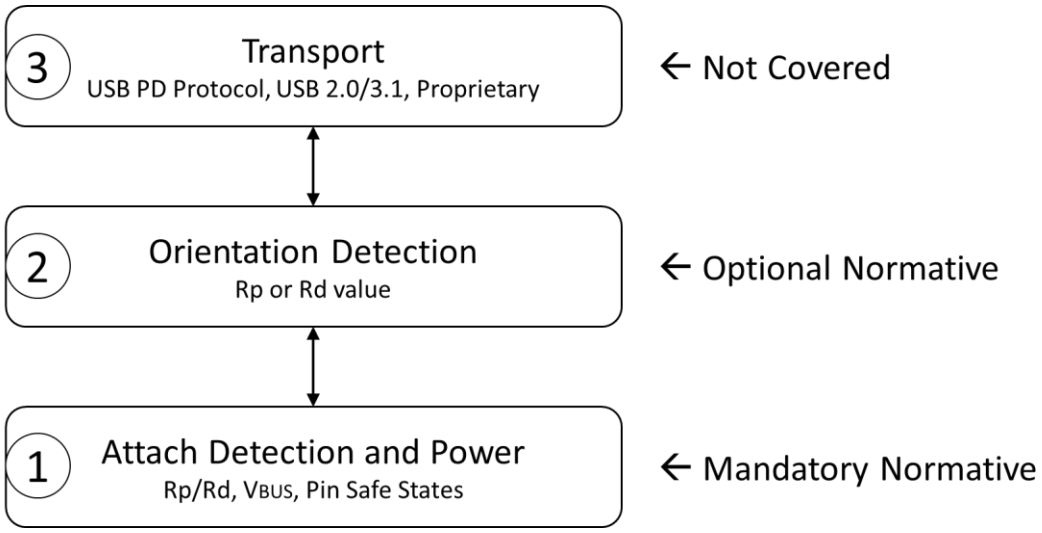
This appendix covers the functional requirements for the USB Type-C® Debug Accessory Mode (DAM), Debug and Test System (DTS), and Target System (TS). The USB Type-C connector is ideal for debug of closed-chassis, form-factor devices. Debug covers many areas, ranging from detailed JTAG Test Access Port (TAP)-level debug in a lab to high-level debug of software applications in production. Lab debug requires early debug access to hardware registers soon after reset, whereas software debug uses kernel debuggers, etc. to access software state. Debug Accessory Mode in USB Type-C enables debug of closed-chassis, form-factor devices by re-defining the USB Type-C ports for debug purposes.

Basic debug requirements are defined as a standard feature, and additional debug features may be added as per vendor specifications.

B.2 Functional

The USB Type-C Debug Accessory Mode follows a layered structure as shown in Figure B-1, defining the minimum physical layer for Attach, Detection and Power. Orientation detection is optional normative. The transport layer is left proprietary and is not covered in this document.

Figure B-1 USB Type-C Debug Accessory Layered Behavior



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

乙 调试附件模式

B.1 概述

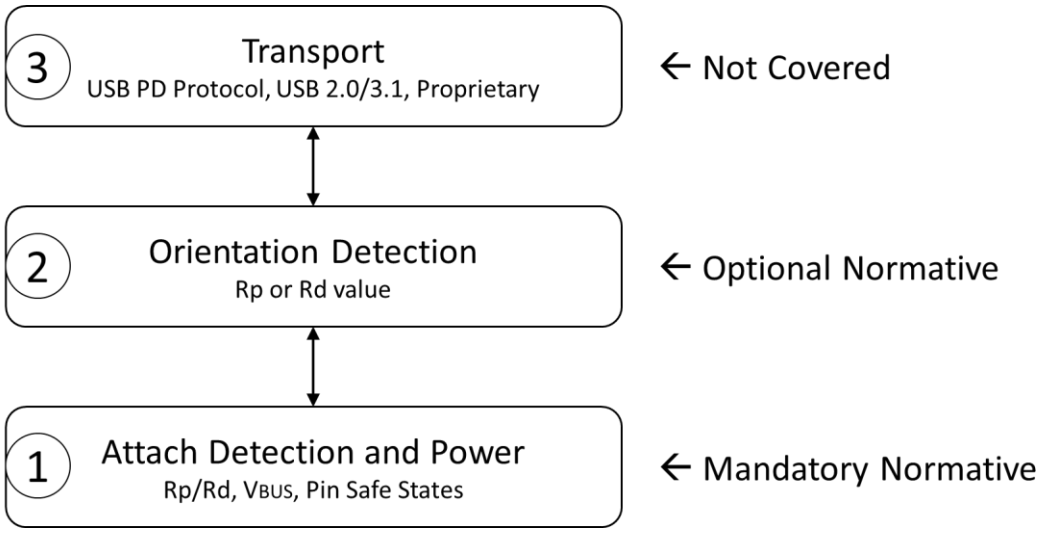
本附录涵盖了 USB Type-C® 调试附件模式 (DAM)、调试和测试系统 (DTS) 以及目标系统 (TS) 的功能要求。USB Type-C 连接器非常适合用于调试封闭式机箱、外形尺寸的设备。调试涵盖许多领域，从实验室中详细的 JTAG 测试访问端口 (TAP) 级调试到生产中软件应用程序的高级调试。实验室调试需要在重置后立即对硬件寄存器进行早期调试访问，而软件调试则使用内核调试器等来访问软件状态。USB Type-C 中的调试附件模式通过重新定义 USB Type-C 端口以进行调试，实现了对封闭式机箱、外形尺寸设备的调试。

基本调试要求被定义为标准功能，并且可以根据供应商规范添加额外的调试功能。

B.2 功能

USB Type-C 调试附件模式遵循如图 B-1 所示的分层结构，定义了连接、检测和供电的最小物理层。方向检测是可选的规范。传输层是专有的，本文档不涉及。

Fi图 B-1 USB Type-C 调试附件分层 行为



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B.2.1 Signal Summary

Figure B-2 shows the pin assignments of the DTS plug that are used to support DAM. The pins highlighted in yellow are those available to be configured for debug signals. Both CC1 and CC2 are used for current advertisement and optional orientation detection.

Figure B-2 DTS Plug Interface

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2-	VBUS	SBU1	D-	D+	CC1	VBUS	TX1-	TX1+	GND
GND	TX2+	TX2-	VBUS	CC2	D+	D-	SBU2	VBUS	RX1-	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

The DTS and TS must follow the USB Safe State as defined in the *USB PD* specification at all times (whether in DAM or not).

B.2.2 Port Interoperability

Table B-1 summarizes the expected results when interconnecting a DTS Source, Sink or DRP port to a TS Source, Sink or DRP port.

Table B-1 DTS to TS Port Interoperability

	DTS Source	DTS Sink	DTS DRP
TS Sink	Functional	Non-functional[1]	Functional
TS Sink w/ Accessory Support	Functional	Non-functional[1]	Functional
TS DRP	Functional	Functional	Functional
TS Source	Non-functional[1]	Functional	Functional

1. In the cases where no function results, neither port shall be harmed by this connection. Following the USB Safe State ensures this.

B.2.3 Debug Accessory Mode Entry

The typical flow for the configuration of the interface in the general case of a DTS to a TS is as follows:

1. Detect a valid connection between the DTS (Source, Sink, or DRP) and TS (Source, Sink, or DRP)
2. Optionally determine orientation of the plug in the receptacle
3. Optionally establish *USB PD* communication over CC for advanced power delivery negotiation and Alternate Modes. *USB PD* communication is allowed only if the optional orientation of the plug is determined.
4. Establish test access connections with the available USB Type-C signals

The DTS DRP will connect as either a Source or a Sink, but its state diagram gives preference to the Source role.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B.2.1 信号摘要

图 B-2 显示了用于支持 DAM 的 DTS 插头的引脚分配。黄色突出显示的引脚是可配置为调试信号的引脚。CC1 和 CC2 均用于电流广播和可选的方向检测。

图 B-2 DTS 插头接口

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2-	VBUS	SBU1	D-	D+	CC1	VBUS	TX1-	TX1+	GND
GND	TX2+	TX2-	VBUS	CC2	D+	D-	SBU2	VBUS	RX1-	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

DTS 和 TS 必须始终遵循 *USB PD* 规范中定义的 USB 安全状态（无论是否在 DAM 中）。

B.2.2 端口互操作性

表 B-1 总结了将 DTS 源、接收器或 DRP 端口互连到 TS 源、接收器或 DRP 端口时的预期结果。

表 B-1 DTS 到 TS 端口互操作性

	DTS Source	DTS Sink	DTS DRP
TS Sink	Functional	Non-functional[1]	Functional
TS Sink w/ Accessory Support	Functional	Non-functional[1]	Functional
TS DRP	Functional	Functional	Functional
TS Source	Non-functional[1]	Functional	Functional

1. 如果无法正常工作，则此连接不会损害任何端口。遵循 USB 安全状态可确保这一点。

B.2.3 调试附件模式进入

一般情况下DTS到TS的接口配置典型流程如下：

1. 检测 DTS（源、接收器或 DRP）和 TS（源、接收器或 DRP）之间的有效连接 2. 可选择确定插头在插座中的方向 3. 可选择通过 CC 建立 *USB PD* 通信，以进行高级电力传输协商和备用模式。仅当确定了插头的可选方向后才允许进行 *USB PD* 通信。 4. 使用可用的 USB Type-C 信号建立测试访问连接

DTS DRP 将作为源或接收器进行连接，但其状态图优先考虑源角色。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B.2.3.1 Detecting a Valid DTS-to-TS Connection

The general concept for setting up a valid connection between a DTS and TS is based on being able to detect the typical USB Type-C termination resistances. However, detecting a Debug Accessory Mode connection requires that both CC pins must detect a pull-up (Rp) or pull-down (Rd) termination. A USB Type-C Cable does not pass both CC wires so a receptacle to receptacle Debug Accessory Mode connection cannot be detected.

A DTS is only allowed to connect to a TS that is presenting either Rp/Rp or Rd/Rd. Otherwise, the TS does not support Debug Accessory Mode.

To detect either an Rp/Rp or Rd/Rd, the DTS must be a captive cable or a direct-attach device with a USB Type-C plug and the TS must have a USB Type-C receptacle.

B.2.4 Connection State Diagrams

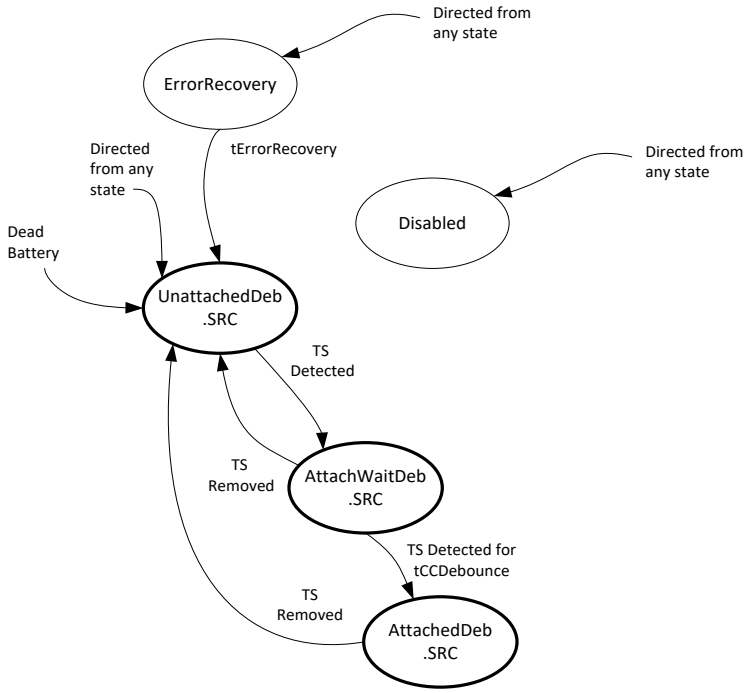
This section provides reference connection state diagrams for CC-based behaviors of the DTS. The TS connection state diagrams are found in Section 4.5.2.

Refer to Section B.2.4.1 for the specific state transition requirements related to each state shown in the diagrams.

Refer to Section B.2.4.3 for a description of which states are mandatory for each port type and a list of states where *USB PD* communication is permitted.

Figure B-3 illustrates a connection state diagram for a DTS Source.

Figure B-3 Connection State Diagram: DTS Source



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B.2.3.1 检测有效的 DTS 到 TS 连接

在 DTS 和 TS 之间建立有效连接的一般概念是基于能够检测典型的 USB Type-C 终端电阻。但是，检测调试附件模式连接需要两个 CC 引脚都必须检测上拉 (Rp) 或下拉 (Rd) 终端。USB Type-C 电缆不会通过两根 CC 线，因此无法检测到插座到插座的调试附件模式连接。

DTS 只允许连接到呈现 Rp/Rp 或 Rd/Rd 的 TS。
否则，TS 不支持调试附件模式。

要检测 Rp/Rp 或 Rd/Rd，DTS 必须是固定电缆或带有 USB Type-C 插头的直连设备，并且 TS 必须具有 USB Type-C 插座。

B.2.4 连接状态图

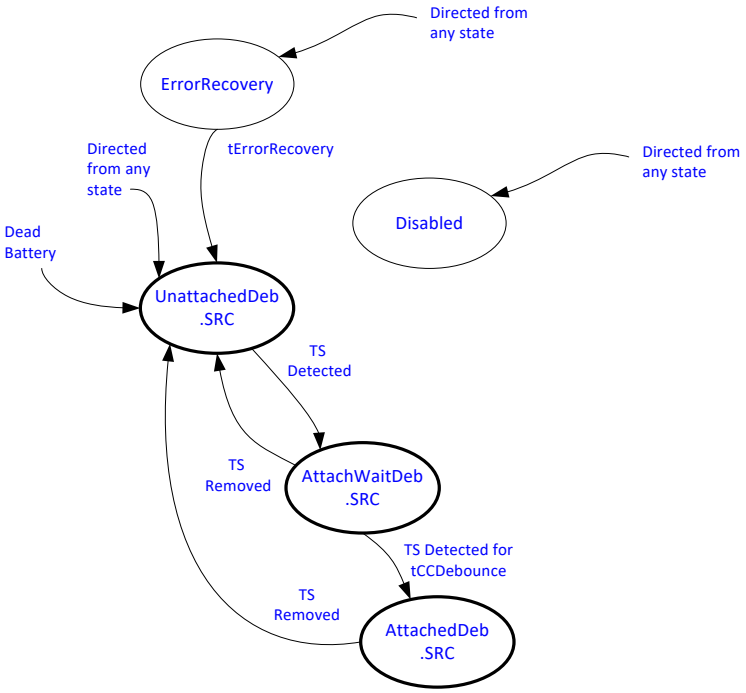
本节提供 DTS 基于 CC 的行为的参考连接状态图。TS 连接状态图请参见第 4.5.2 节。

有关图中所示每个状态的具体状态转换要求，请参阅第 B.2.4.1 节。

有关每种端口类型强制执行的状态的描述以及允许 *USB PD* 通信的状态列表，请参阅第 B.2.4.3 节。

图 B-3 说明了 DTS 源的连接状态图。

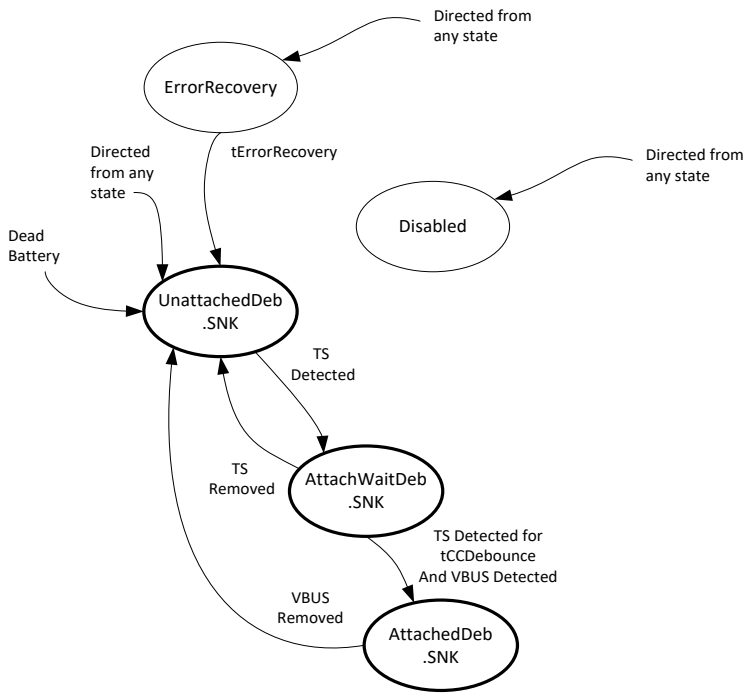
图 B-3 连接状态图：DTS 源



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure B-4 illustrates a connection state diagram for a simple DTS Sink.

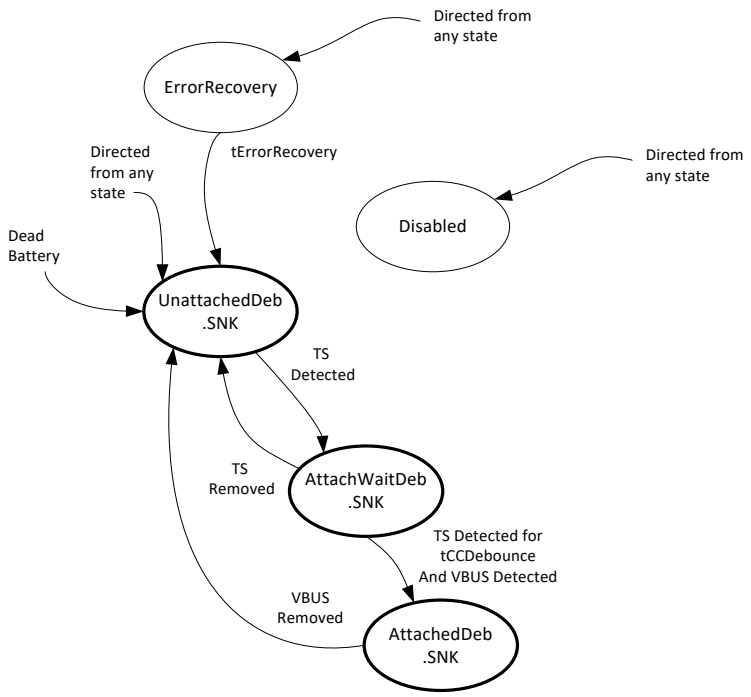
Figure B-4 Connection State Diagram: DTS Sink



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 B-4 说明了简单的 DTS Sink 的连接状态图。

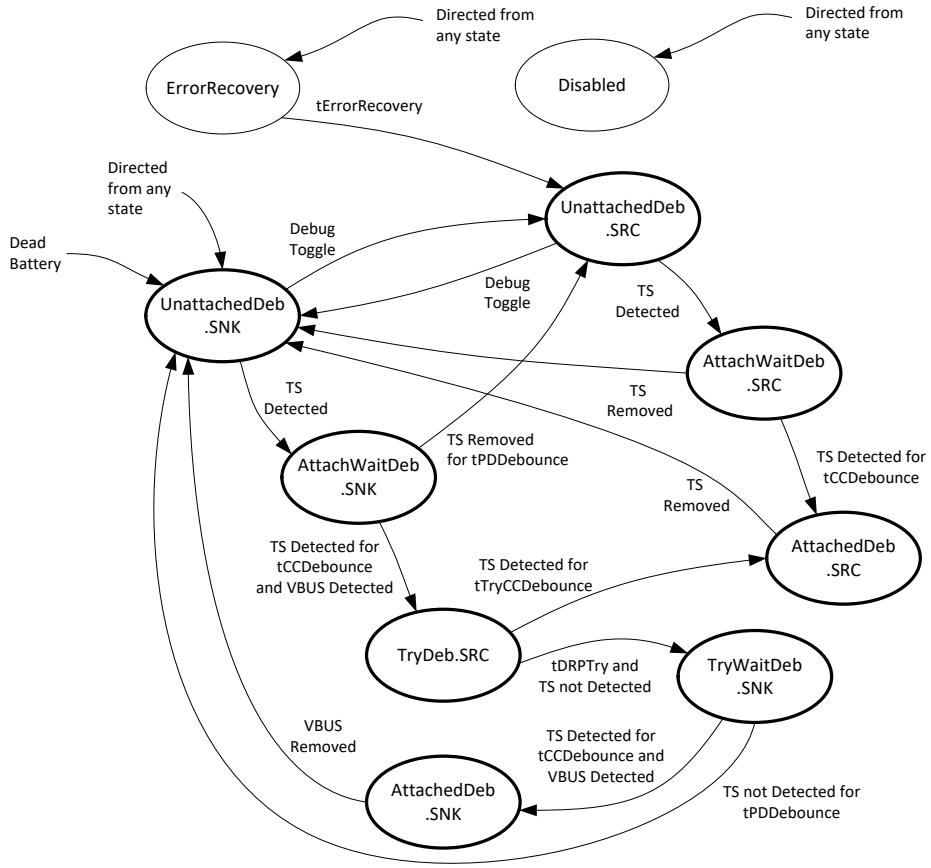
图 B-4 连接状态图：DTS 接收器



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure B-5 illustrates a connection state diagram for a DTS DRP.

Figure B-5 Connection State Diagram: DTS DRP



B.2.4.1 Connection State Machine Requirements

The DTS state machine requirements follow those outlined in Section 4.5.2.2 for the general USB Type-C state machines with the additional following states defined.

Note, VCONN shall not be driven by any DTS or TS port in any state.

B.2.4.1.1 Exiting From ErrorRecovery State

This state appears in Figure B-3, Figure B-4, and Figure B-5.

The ErrorRecovery state is where the DTS cycles its connection by removing all terminations from the CC pins for tErrorRecovery followed by transitioning to the appropriate UnattachedDeb.SNK or UnattachedDeb.SRC state based on DTS type.

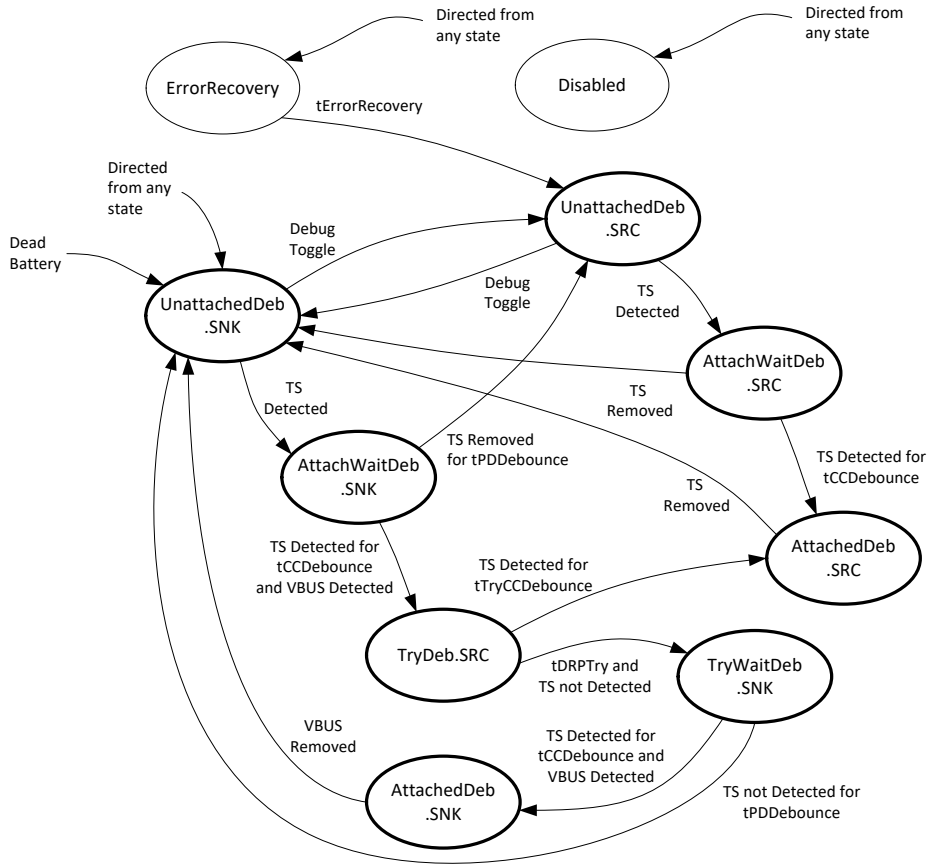
The DTS should transition to the ErrorRecovery state from any other state when directed.

A DTS may choose not to support the ErrorRecovery state. If the ErrorRecovery state is not supported, the DTS shall be directed to the Disabled state if supported. If the Disabled state is not supported, the DTS shall be directed to either the UnattachedDeb.SNK or UnattachedDeb.SRC states.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 B-5 说明了 DTS DRP 的连接状态图。

图 B-5 连接状态图：DTS DRP



B.2.4.1 连接状态机要求

DTS 状态机要求遵循第 4.5.2.2 节中概述的通用 USB Type-C 状态机要求，并定义了以下附加状态。

注意，任何状态下，VCONN 都不能由任何 DTS 或 TS 端口驱动。

B.2.4.1.1 退出错误恢复状态

此状态出现在图 B-3、图 B-4 和图 B-5 中。

在 ErrorRecovery 状态下，DTS 通过从 CC 引脚移除 tErrorRecovery 的所有终端来循环其连接，然后根据 DTS 类型转换到适当的 UnattachedDeb.SNK 或 UnattachedDeb.SRC 状态。

当收到指示时，DTS 应该从任何其他状态转换到 ErrorRecovery 状态。

DTS 可以选择不支持 ErrorRecovery 状态。如果不支持 ErrorRecovery 状态，则 DTS 应定向到 Disabled 状态（如果支持）。如果不支持 Disabled 状态，则 DTS 应定向到 UnattachedDeb.SNK 或 UnattachedDeb.SRC 状态。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A DTS Sink shall transition to UnattachedDeb.SNK after tErrorRecovery.

A DTS Source shall transition to UnattachedDeb.SRC after tErrorRecovery.

A DTS DRP shall transition to UnattachedDeb.SRC after tErrorRecovery.

B.2.4.1.2 UnattachedDeb.SNK State

This state appears in Figure B-4 and Figure B-5.

When in the UnattachedDeb.SNK state, the DTS is waiting to detect the presence of a TS Source.

A DTS with a dead battery shall enter this state while unpowered.

B.2.4.1.2.1 UnattachedDeb.SNK Requirements

The DTS shall not drive VBUS.

Both CC pins shall be independently terminated to ground through Rd.

B.2.4.1.2.2 Exiting from UnattachedDeb.SNK State

The DTS shall transition to AttachWaitDeb.SNK when a TS Source connection is detected, as indicated by the SNK.Rp state on both of its CC pins.

A DTS DRP shall transition to UnattachedDeb.SRC within tDRPTransition after the state of one or both CC pins is SNK.Open for tDRP − dcSRC.DRP · tDRP, or if directed.

B.2.4.1.3 AttachWaitDeb.SNK State

This state appears in Figure B-4 and Figure B-5.

When in the AttachWaitDeb.SNK state, the DTS has detected the SNK.Rp state on both CC pins and is waiting for VBUS.

B.2.4.1.3.1 AttachWaitDeb.SNK Requirements

The requirements for this state are identical to UnattachedDeb.SNK.

B.2.4.1.3.2 Exiting from AttachWaitDeb.SNK State

A DTS Sink shall transition to UnattachedDeb.SNK when the state of one or both CC pins is SNK.Open for at least tPDDebounce.

A DTS DRP shall transition to UnattachedDeb.SRC when the state of one or both CC pins is SNK.Open for at least tPDDebounce.

A DTS Sink shall transition to AttachedDeb.SNK when neither CC pin is SNK.Open after tCCDebounce and VBUS is detected.

A DTS DRP shall transition to TryDeb.SRC when neither CC pin is SNK.Open after tCCDebounce and VBUS is detected.

B.2.4.1.4 AttachedDeb.SNK State

This state appears in Figure B-4 and Figure B-5.

When in the AttachedDeb.SNK state, the DTS is attached and operating as a DTS Sink.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

tErrorRecovery 之后，DTS Sink 应转换至 UnattachedDeb.SNK。

DTS 源应在 tErrorRecovery 之后转换到 UnattachedDeb.SRC。

DTS DRP 应在 tErrorRecovery 之后转换到 UnattachedDeb.SRC。

B.2.4.1.2 UnattachedDeb.SNK 状态

此状态如图 B-4 和图 B-5 所示。

当处于 UnattachedDeb.SNK 状态时，DTS 正在等待检测 TS 源的存在。

电池没电的 DTS 在断电时将进入此状态。

B.2.4.1.2.1 UnattachedDeb.SNK 要求

DTS 不得驱动 VBUS。

两个 CC 引脚应通过 Rd 独立接地。

B.2.4.1.2.2 退出 UnattachedDeb.SNK 状态

当检测到 TS 源连接时，DTS 应转换到 AttachWaitDeb.SNK，如其两个 CC 引脚上的 SNK.Rp 状态所示。

在一个或两个 CC 引脚的状态为 tDRP – dcSRC.DRP · tDRP 的 SNK.Open 之后，或者如果指示，DTS DRP 应在 tDRPTransition 内转换到 UnattachedDeb.SRC。

B.2.4.1.3 AttachWaitDeb.SNK 状态

此状态如图 B-4 和图 B-5 所示。

当处于 AttachWaitDeb.SNK 状态时，DTS 已检测到两个 CC 引脚上的 SNK.Rp 状态，并且正在等待 VBUS。

B.2.4.1.3.1 AttachWaitDeb.SNK 要求

此状态的要求与UnattachedDeb.SNK相同。

B.2.4.1.3.2 退出 AttachWaitDeb.SNK 状态

当一个或两个 CC 引脚的状态为 SNK.Open 至少持续 tPDDebounce 时，DTS Sink 应转换到 UnattachedDeb.SNK。

当一个或两个 CC 引脚的状态为 SNK.Open 至少 tPDDebounce 时，DTS DRP 应转换到 UnattachedDeb.SRC。

当 tCCDebounce 之后 CC 引脚都不是 SNK.Open 并且检测到 VBUS 时，DTS Sink 应转换到 AttachedDeb.SNK。

当 tCCDebounce 之后 CC 引脚都不是 SNK.Open 并且检测到 VBUS 时，DTS DRP 将转换到 TryDeb.SRC。

B.2.4.1.4 AttachedDeb.SNK 状态

此状态如图 B-4 和图 B-5 所示。

当处于 AttachedDeb.SNK 状态时，DTS 已连接并作为 DTS Sink 运行。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B.2.4.1.4.1 AttachedDeb.SNK Requirements

This mode is for debug only

The port shall not drive VBUS.

The port shall provide an Rd as specified in Table 4-15 on both CC pins if orientation is not needed. See Section B.2.6 for orientation detection.

The port shall monitor to detect when VBUS is removed.

If the DTS needs to establish a *USB PD* communications, it shall do so only after entry to this state. In this state, the DTS takes on the initial *USB PD* role of UFP/Sink.

The DTS shall connect the debug signals for Debug Accessory Mode operation only after entry to this state.

The DTS may follow the DAM Sink Power Sub-State behavior specified in Section 4.5.2.3.

B.2.4.1.4.2 Exiting from AttachedDeb.SNK State

A DTS shall transition to UnattachedDeb.SNK when VBUS is no longer present

B.2.4.1.5 UnattachedDeb.SRC State

This state appears in Figure B-3 and Figure B-5.

When in the UnattachedDeb.SRC state, the DTS is waiting to detect the presence of a TS Sink

B.2.4.1.5.1 UnattachedDeb.SRC Requirements

The DTS shall not drive VBUS.

The DTS shall source current on both CC pins independently.

The DTS shall provide a unique Rp value on each CC pin as specified in Section 4.5.2.3.

B.2.4.1.5.2 Exiting from UnattachedDeb.SRC State

The DTS shall transition to AttachWaitDeb.SRC when the SRC.Rd state is detected on both CC pins.

A DTS DRP shall transition to UnattachedDeb.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.

B.2.4.1.6 AttachWaitDeb.SRC State

This state appears in Figure B-3 and Figure B-5.

The AttachWaitDeb.SRC state is used to ensure that the state of both of the CC pins is stable after a TS Sink is connected.

B.2.4.1.6.1 AttachWaitDeb.SRC Requirements

The requirements for this state are identical to UnattachedDeb.SRC.

B.2.4.1.6.2 Exiting from AttachWaitDeb.SRC State

The DTS shall transition to AttachedDeb.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on both of the CC pins for at least tCCDebounce.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B.2.4.1.4.1 AttachedDeb.SNK 要求

此模式仅用于调试

该端口不得驱动VBUS。

如果不需要方向，端口应在两个 CC 引脚上提供表 4-15 中指定的 Rd。有关方向检测，请参阅第 B .2.6 节。

该端口应监控以检测何时移除 VBUS。

如果 DTS 需要建立 *USB PD* 通信，则它只能在进入此状态后才可以这样做。在此状态下，DTS 承担 UFP/Sink 的初始 *USB PD* 角色。

只有进入此状态后，DTS 才应连接调试附件模式操作的调试信号。

DTS 可能遵循第 4.5.2.3 节中指定的 DAM Sink Power 子状态行为。

B.2.4.1.4.2 退出 AttachedDeb.SNK 状态

当 VBUS 不再存在时，DTS 应转换为 UnattachedDeb.SNK

B.2.4.1.5 UnattachedDeb.SRC 状态

此状态出现在图 B-3 和图 B-5 中。

当处于 UnattachedDeb.SRC 状态时，DTS 正在等待检测 TS Sink 的存在

B.2.4.1.5.1 UnattachedDeb.SRC 要求

DTS 不得驱动 VBUS。

DTS 应独立地在两个 CC 引脚上提供电流。

DTS 应在每个 CC 引脚上提供唯一的 Rp 值，如第 4.5.2.3 节所述。

B.2.4.1.5.2 退出 UnattachedDeb.SRC 状态

当在两个 CC 引脚上检测到 SRC.Rd 状态时，DTS 应转换到 AttachWaitDeb.SRC。

DTS DRP 应在 dcSRC.DRP · tDRP 之后的 tDRPTransition 内转换为 UnattachedDeb.SNK，或者在有指示的情况下转换。

B.2.4.1.6 AttachWaitDeb.SRC 状态

此状态出现在图 B-3 和图 B-5 中。

AttachWaitDeb.SRC 状态用于确保 TS Sink 连接后两个 CC 引脚的状态都稳定。

B.2.4.1.6.1 AttachWaitDeb.SRC 要求

此状态的要求与UnattachedDeb.SRC相同。

B.2.4.1.6.2 退出 AttachWaitDeb.SRC 状态

当 VBUS 处于 vSafe0V 并且在两个 CC 引脚上都检测到 SRC.Rd 状态至少 tCCDebounce 时，DTS 应转换到 AttachedDeb.SRC。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

A DTS Source shall transition to UnattachedDeb.SRC and a DTS DRP to UnattachedDeb.SNK when the SRC.Open state is detected on either of the CC pins.

B.2.4.1.7 AttachedDeb.SRC State

This state appears in Figure B-3 and Figure B-5.

When in the AttachedDeb.SRC state, the DTS is attached and operating as a DTS Source.

B.2.4.1.7.1 AttachedDeb.SRC Requirements

The DTS shall provide a unique Rp value on each CC pin as specified in Section B.2.4.2.

The DTS shall supply VBUS current at the level it advertises. See Section B.2.6.1.1 for advertising current level.

The DTS shall supply VBUS within tVBUSON of entering this state, and for as long as it is operating as a power source.

If the DTS needs to establish *USB PD* communications, it shall do so only after entry to this state. The DTS shall not initiate any *USB PD* communications until VBUS reaches vSafe5V. In this state, the DTS takes on the initial *USB PD* role of DFP/Source.

The DTS shall connect the debug signals for Debug Accessory Mode operation only after entry to this state.

B.2.4.1.7.2 Exiting from AttachedDeb.SRC State

A DTS Source shall transition to UnattachedDeb.SRC when the SRC.Open state is detected on either CC pin.

A DTS DRP shall transition to UnattachedDeb.SNK when SRC.Open is detected on either CC pin.

A DTS shall cease to supply VBUS within tVBUSOFF of exiting AttachedDeb.SRC.

B.2.4.1.8 TryDeb.SRC State

This state appears in Figure B-5.

When in the TryDeb.SRC state, the DTS DRP is querying to determine if the TS is also a DRP, to favor the DTS taking the Source role.

B.2.4.1.8.1 TryDeb.SRC Requirements

The DTS shall not drive VBUS.

The DTS shall source current on both CC pins independently.

The DTS shall provide a unique Rp value on each CC pin as specified in Section B.2.4.2.

B.2.4.1.8.2 Exiting from TryDeb.SRC State

The DTS shall transition to AttachedDeb.SRC when the SRC.Rd state is detected on both CC pins for at least tTryCCDebounce.

The DTS shall transition to TryWaitDeb.SNK after tDRPTry if the state of both CC pins is not SRC.Rd.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

当在任一 CC 引脚上检测到 SRC.Open 状态时，DTS 源应转换至 UnattachedDeb.SRC，并且 DTS DRP 应转换至 UnattachedDeb.SNK。

B.2.4.1.7 AttachedDeb.SRC 状态

此状态出现在图 B-3 和图 B-5 中。

当处于 AttachedDeb.SRC 状态时，DTS 已连接并作为 DTS 源运行。

B.2.4.1.7.1 AttachedDeb.SRC 要求

DTS 应按照第 B.2.4.2 节的规定在每个 CC 引脚上提供唯一的 Rp 值。

DTS 应按其宣传的级别提供 VBUS 电流。有关宣传电流级别，请参阅第 B.2.6.1.1 节。

DTS 应在进入此状态的 tVBUSON 时间内供应 VBUS，并且只要它作为电源运行。

如果 DTS 需要建立 *USB PD* 通信，则应仅在进入此状态后才这样做。在 VBUS 达到 vSafe5V 之前，DTS 不得发起任何 *USB PD* 通信。在此状态下，DTS 承担 DFP/Source 的初始 *USB PD* 角色。

只有进入此状态后，DTS 才应连接调试附件模式操作的调试信号。

B.2.4.1.7.2 退出 AttachedDeb.SRC 状态

当检测到 SRC.Open 状态时，DTS 源应转换为 UnattachedDeb.SRC
任一 CC 引脚。

当在任一 CC 引脚上检测到 SRC.Open 时，DTS DRP 应转换至 UnattachedDeb.SNK。

DTS 应在退出 AttachedDeb.SRC 后的 tVBUSOFF 时间内停止提供 VBUS。

B.2.4.1.8 TryDeb.SRC 状态

此状态如图 B-5 所示。

当处于 TryDeb.SRC 状态时，DTS DRP 正在查询以确定 TS 是否也是 DRP，以支持 DTS 承担源角色。

B.2.4.1.8.1 TryDeb.SRC 要求

DTS 不得驱动 VBUS。

DTS 应独立地在两个 CC 引脚上提供电流。

DTS 应按照第 B.2.4.2 节的规定在每个 CC 引脚上提供唯一的 Rp 值。

B.2.4.1.8.2 退出 TryDeb.SRC 状态

当在两个 CC 引脚上检测到 SRC.Rd 状态至少持续 tTryCCDebounce 时，DTS 应转换到 AttachedDeb.SRC。

如果两个 CC 引脚的状态都不是 SRC.Rd，则 DTS 应在 tDRPTry 之后转换到 TryWaitDeb.SNK。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B.2.4.1.9 TryWaitDeb.SNK State

This state appears in Figure B-5.

When in the TryWaitDeb.SNK state, the DTS has failed to become a DTS Source and is waiting to attach as a DTS Sink.

B.2.4.1.9.1 TryWaitDeb.SNK Requirements

The DTS shall not drive VBUS.

Both CC pins shall be independently terminated to ground through Rd.

B.2.4.1.9.2 Exiting from TryWaitDeb.SNK State

The DTS shall transition to AttachedDeb.SNK when neither CC pin is SNK.Open after tCCDebounce and VBUS is detected.

The DTS shall transition to UnattachedDeb.SNK when the state of one of the CC pins is SNK.Open for at least tPDDebounce or if VBUS is not detected within tPDDebounce.

B.2.4.2 Power Sub-State Requirements

B.2.4.2.1 TS Sink Power Sub-State Requirements

When in the DebugAccessory.SNK state and the DTS Source is supplying default VBUS, the TS Sink shall operate in one of the sub-states shown in Figure B-6. The initial TS Sink Power Sub-State is PowerDefaultDeb.SNK. Subsequently, the TS Sink Power Sub-State is determined by the DTS Source's USB Type-C current advertisement determined by the Rp value on each CC pin as shown in Table B-2. The TS Sink in the attached state shall remain within the TS Sink Power Sub-States until either VBUS is removed or a *USB PD* contract is established with the Source.

The TS Sink is only required to implement TS Sink Power Sub-State transitions if the TS Sink wants to consume more than default USB current.

Note, a TS Source will not use the values in Table B-2. A TS Source will present the same Rp on each CC pin using the standard Rp value for the desired current advertisement.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B.2.4.1.9 TryWaitDeb.SNK 状态

此状态如图 B-5 所示。

当处于 TryWaitDeb.SNK 状态时，DTS 无法成为 DTS Source，正在等待作为 DTS Sink 连接。

B.2.4.1.9.1 TryWaitDeb.SNK 要求

DTS 不得驱动 VBUS。

两个 CC 引脚应通过 Rd 独立接地。

B.2.4.1.9.2 退出 TryWaitDeb.SNK 状态

当 tCCDebounce 之后 CC 引脚都不是 SNK.Open 并且检测到 VBUS 时，DTS 应转换到 AttachedDeb.SNK。

当其中一个 CC 引脚的状态为 SNK.Open 至少持续 tPDDebounce 时，或者在 tPDDebounce 内未检测到 VBUS 时，DTS 应转换到 UnattachedDeb.SNK。

B.2.4.2 电源子状态要求

B.2.4.2.1 TS 接收器电源子状态要求

当处于 DebugAccessory.SNK 状态且 DTS 源提供默认 VBUS 时，TS 接收器应在图 B-6 所示的子状态之一下运行。初始 TS 接收器电源子状态为 PowerDefaultDeb.SNK。随后，TS 接收器电源子状态由 DTS 源的 USB Type-C 电流通告决定，该通告由每个 CC 引脚上的 Rp 值决定，如表 B-2 所示。处于连接状态的 TS 接收器应保持在 TS 接收器电源子状态中，直到 VBUS 被移除或与源建立 *USB PD* 合同。

仅当 TS Sink 想要消耗超过默认 USB 电流时，TS Sink 才需要实现 TS Sink 电源子状态转换。

请注意，TS 源不会使用表 B-2 中的值。TS 源将使用所需电流通告的标准 Rp 值在每个 CC 引脚上呈现相同的 Rp。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure B-6 TS Sink Power Sub-States

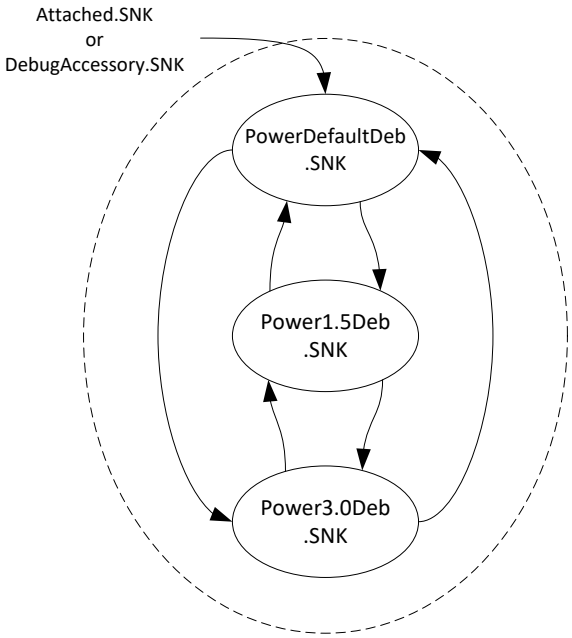


Table B-2 Rp/Rp Charging Current Values for a DTS Source

Mode of Operation	CC1	CC2
Default USB Power	Rp for 3 A	Rp for 1.5 A
USB Type-C Current @ 1.5 A	Rp for 1.5 A	Rp for Default
USB Type-C Current @ 3 A	Rp for 3 A	Rp for Default

B.2.4.2.2 PowerDefaultDeb.SNK Sub-State

This sub-state supports DAM Sinks consuming current within the lowest range (default) of Source-supplied current.

B.2.4.2.2.1 PowerDefaultDeb.SNK Requirements

The port shall draw no more than the default USB power from VBUS. See Section 4.6.2.1.

If the DTS Sink wants to consume more than the default USB power, it shall monitor vRd on both CC pins to determine if more current is available from the Source.

B.2.4.2.2.2 Exiting from PowerDefaultDeb.SNK

For any change on CC indicating a change in allowable power, the DAM Sink shall not transition until the new vRd voltages on each CC pin have been stable for at least tRpValueChange.

For vRd voltages on the CC pins indicating 1.5 A mode, the DAM Sink shall transition to the Power1.5Deb.SNK Sub-State.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 B-6 TS 接收器电源子状态

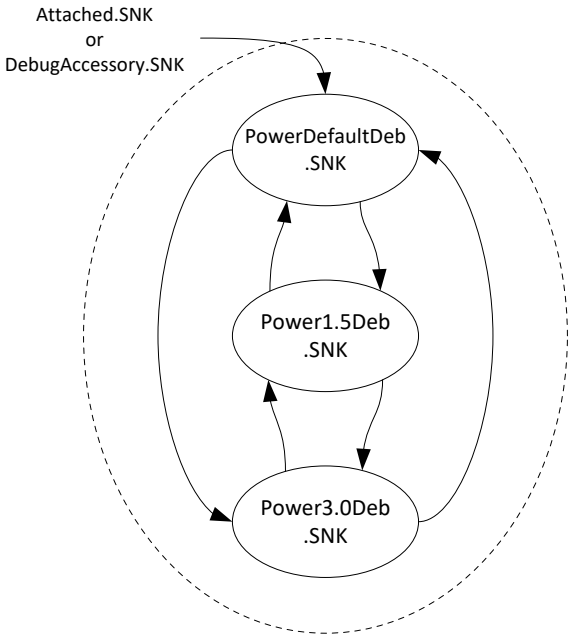


表 B-2 DTS 源的 Rp/Rp 充电电流值

Mode of Operation	CC1	CC2
Default USB Power	Rp for 3 A	Rp for 1.5 A
USB Type-C Current @ 1.5 A	Rp for 1.5 A	Rp for Default
USB Type-C Current @ 3 A	Rp for 3 A	Rp for Default

B.2.4.2.2 PowerDefaultDeb.SNK 子状态

该子状态支持 DAM 接收器消耗源供电电流最低范围 (默认) 内的电流。

B.2.4.2.2.1 PowerDefaultDeb.SNK 要求

端口从 V BUS 获得的功率不得超过默认 USB 功率。请参阅第 4.6.2.1 节。

如果 DTS Sink 想要消耗超过默认的 USB 电量，它应监控两个 CC 引脚上的 vRd，以确定是否有更多来自 Sour ce 的电流可用。

B.2.4.2.2.2 退出 PowerDefaultDeb.SNK

对于 CC 上的任何变化（表明允许功率的变化），DAM Sink 不得转换，直到每个 CC 引脚上的新 vRd 电压至少稳定 ~~tRp~~ValueChange。

对于指示 1.5 A 模式的 CC 引脚上的 vRd 电压，DAM Sink 应转换至 Power1.5Deb.SNK 子状态。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

For vRd voltages on the CC pins indicating 3 A mode, the DAM Sink shall transition to the Power3.0Deb.SNK Sub-State.

B.2.4.2.3 Power1.5Deb.SNK Sub-State

This sub-state supports DAM Sinks consuming current within the two lower ranges (default and 1.5 A) of DAM Source-supplied current.

B.2.4.2.3.1 Power1.5Deb.SNK Requirements

The DAM Sink shall draw no more than 1.5 A from VBUS.

The DAM Sink shall monitor both vRd voltages while it is in this sub-state.

B.2.4.2.3.2 Exiting from Power1.5Deb.SNK

For any change on the CC pins indicating a change in allowable power, the DAM Sink shall not transition until the new vRd voltages on both CC pins have been stable for at least tRpValueChange.

For vRd voltages on the CC pins indicating Default USB Power mode, the port shall transition to the PowerDefaultDeb.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

For vRd voltages on the CC pins indicating 3 A mode, the port shall transition to the Power3.0Deb.SNK Sub-State.

B.2.4.2.4 Power3.0Deb.SNK Sub-State

This sub-state supports DAM Sinks consuming current within all three ranges (default, 1.5 A and 3.0 A) of DAM Source-supplied current.

B.2.4.2.4.1 Power3.0Deb.SNK Requirements

The port shall draw no more than 3.0 A from VBUS.

The port shall monitor both vRd voltages while it is in this sub-state.

B.2.4.2.4.2 Exiting from Power3.0Deb.SNK

For any change on the CC pins indicating a change in allowable power, the port shall not transition until the new vRd voltages on both CC pins have been stable for at least tRpValueChange.

For vRd voltages on the CC pins indicating Default USB Power mode, the port shall transition to the PowerDefaultDeb.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

For vRd voltages on the CC pins indicating 1.5 A mode, the DAM Sink shall transition to the Power1.5Deb.SNK Sub-State.

B.2.4.2.5 DTS Sink Power Sub-State Requirements

A DTS Sink follows the same power sub-states defined in Section 4.5.2.2.22. The TS Source will be advertising current with a standard Rp value that is the same for each CC pin. If optional orientation detection is performed, the DTS Sink will only be able to determine the Rp value from the CC pin that is set for *USB PD* communication.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

对于指示 3 A 模式的 CC 引脚上的 vRd 电压，DAM Sink 应转换至 Power3.0Deb.SNK 子状态。

B.2.4.2.3 Power1.5Deb.SNK 子状态

该子状态支持 DAM 接收器消耗 DAM 源供给电流的两个较低范围（默认和 1.5 A）内的电流。

B.2.4.2.3.1 Power1.5Deb.SNK 要求

DAM Sink 从 V BUS 吸取的电流不得超过 1.5 A。

当 DAM Sink 处于此子状态时，它应监控两个 vRd 电压。

B.2.4.2.3.2 退出 Power1.5Deb.SNK

对于 CC 引脚上的任何变化（表明允许功率的变化），DAM Sink 不得转换，直到两个 CC 引脚上的新 vRd 电压至少稳定 tRpV~~alue~~Change。

对于 CC 引脚上的 vRd 电压，指示默认 USB 电源模式，端口应转换到 PowerDefaultDeb.SNK 子状态并将其功耗降低到 tSinkAdj 内的新范围内。

对于指示 3 A 模式的 CC 引脚上的 vRd 电压，端口应转换至 Power3.0Deb.SNK 子状态。

B.2.4.2.4 Power3.0Deb.SNK 子状态

该子状态支持 DAM 接收器消耗 DAM 源提供电流的所有三个范围（默认、1.5 A 和 3.0 A）内的电流。

B.2.4.2.4.1 Power3.0Deb.SNK 要求

该端口从 VBUS 吸取的电流不得超过 3.0 A。

当端口处于此子状态时，它应监控两个 vRd 电压。

B.2.4.2.4.2 退出 Power3.0Deb.SNK

对于 CC 引脚上的任何变化（表明允许功率的变化），端口不得转换，直到两个 CC 引脚上的新 vRd 电压至少稳定 tRpV~~alue~~Change。

对于 CC 引脚上的 vRd 电压，指示默认 USB 电源模式，端口应转换到 PowerDefaultDeb.SNK 子状态并将其功耗降低到 tSinkAdj 内的新范围内。

对于指示 1.5 A 模式的 CC 引脚上的 vRd 电压，DAM Sink 应转换至 Power1.5Deb.SNK 子状态。

B.2.4.2.5 DTS 接收器电源子状态要求

DTS Sink 遵循第 4.5.2.2.22 节中定义的相同电源子状态。TS Source 将以标准 Rp 值（对于每个 CC 引脚相同）通告电流。如果执行可选的方向检测，DTS Sink 将只能确定

为 *USB PD* 通信设置的 CC 引脚的 Rp 值。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B.2.4.3 Connection States Summary

Table B-3 defines the mandatory and optional states for each type of port. For states allowing *USB PD* communication, DAM connections requiring *USB PD* communication shall determine orientation by the steps described in Section B.2.6.

Table B-3 Mandatory and Optional States

	DTS Source	DTS SINK	DTS DRP	USB PD Communication and/or Debug Signal Activity
UnattachedDeb.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachWaitDeb.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachedDeb.SNK	N/A	Mandatory	Mandatory	Permitted
UnattachedDeb.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachWaitDeb.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachedDeb.SRC	Mandatory	N/A	Mandatory	Permitted
TryDeb.SRC	N/A	N/A	Mandatory	Not Permitted
TryWaitDeb.SNK	N/A	N/A	Mandatory	Not Permitted

B.2.5 DTS Port Interoperability Behavior

This section describes interoperability behavior between DTS ports and TS ports.

B.2.5.1 DTS Port to TS Port Interoperability Behaviors

The following sub-sections describe typical port-to-port interoperability behaviors for the various combinations of DTS and TS Sources, Sinks and DRPs as presented in Table B-1.

B.2.5.1.1 DTS Source to TS Sink Behavior

The following describes the behavior when a DTS Source is connected to a TS Sink.

1. DTS Source and TS Sink in the unattached state
2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS Source detects the TS Sink's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC
   - DTS Source turns on VBUS
3. TS Sink transitions from Unattached.SNK to DebugAccessory.SNK through AttachWait.SNK
   - TS Sink in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters DebugAccessory.SNK
4. While the DTS Source and TS Sink are in the attached state:
   - DTS Source adjusts both Rp values as needed for offered current

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B.2.4.3 连接状态摘要

表 B-3 定义了每种端口类型的强制状态和可选状态。对于允许 *USB PD* 通信的状态，需要 *USB PD* 通信的 DAM 连接应按照 B.2.6 节中描述的步骤确定方向。

表 B-3 强制状态和可选状态

	DTS Source	DTS SINK	DTS DRP	USB PD Communication and/or Debug Signal Activity
UnattachedDeb.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachWaitDeb.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachedDeb.SNK	N/A	Mandatory	Mandatory	Permitted
UnattachedDeb.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachWaitDeb.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachedDeb.SRC	Mandatory	N/A	Mandatory	Permitted
TryDeb.SRC	N/A	N/A	Mandatory	Not Permitted
TryWaitDeb.SNK	N/A	N/A	Mandatory	Not Permitted

B.2.5 DTS 端口互操作性行为

本节描述 DTS 端口和 TS 端口之间的互操作行为。

B.2.5.1 DTS 端口到 TS 端口互操作性行为

以下小节描述了表 B-1 中所示的 DTS 和 TS 源、接收器和 DRP 的各种组合的典型端口到端口互操作性行为。

B.2.5.1.1 DTS 源到 TS 接收器的行为

下面描述了 DTS Source 连接到 TS Sink 时的行为。

1. DTS Source 和 TS Sink 处于未连接状态 2. DTS Source 通过 AttachWaitDeb.SRC 从 UnattachedDeb.SRC 转换为 AttachedDeb.SRC

• DTS Source 检测到 TS Sink 在两个 CC 引脚上的下拉，并进入 AttachWaitDeb.SRC。tCCDebounce 之后，它进入 AttachedDeb.SRC • DTS Source 打开 VBUS

3. TS Sink 通过 AttachWait.SNK 从 Unattached.SNK 转换到 DebugAccessory.SNK • Unattached.SNK 中的 TS Sink 检测到两个 CC 引脚上的 DTS Source 上拉电阻

并进入 AttachWait.SNK。该状态持续 tCCDebounce 后，它
检测到 VBUS 后，进入 DebugAccessory.SNK 4. 当 DTS Source 和 TS Sink 处于连接状态时：• DTS Source 根据需要调整两个 Rp 值以提供电流

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- TS Sink detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required
- DTS Source monitors both CC pins for detach and when detected on either pin, enters UnattachedDeb.SRC
- TS Sink monitors VBUS for detach and when detected, enters Unattached.SNK

B.2.5.1.2 DTS Source to TS DRP Behavior

The following describes the behavior when a DTS Source is connected to a TS DRP.

1. DTS Source and TS DRP in the unattached state
   - TS DRP alternates between Unattached.SRC and Unattached.SNK
2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS Source detects the TS DRP's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC
   - DTS Source turns on VBUS
3. TS DRP transitions from Unattached.SNK to DebugAccessory.SNK through AttachWait.SNK
   - TS DRP in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters DebugAccessory.SNK
4. While the DTS Source and TS DRP are in their respective attached states:
   - DTS Source adjusts both Rp values as needed for offered current
   - TS DRP detects and monitors vRd on both CC pins for available current on VBUS and performs any orientation required
   - DTS Source monitors both CC pins for detach and when detected, enters UnattachedDeb.SRC
   - TS DRP monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

B.2.5.1.3 DTS Sink to TS Source Behavior

The following describes the behavior when a DTS Sink is connected to a TS Source.

1. TS Source and DTS Sink in the unattached state
2. TS Source transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC
   - TS Source detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.SRC. After tCCDebounce, it enters UnorientedDebugAccessory.SRC.
   - TS Source turns on VBUS
3. DTS Sink transitions from UnattachedDeb.SNK to AttachedDeb.SNK through AttachWaitDeb.SNK.
   - DTS Sink in UnattachedDeb.SNK detects the TS Source's pull-ups on both CC pins and enters AttachWaitDeb.SNK.
   - DTS Sink in AttachWaitDeb.SNK detects that the pull-ups on both CC pins persist for tCCDebounce and it detects VBUS. It enters AttachedDeb.SNK
   - DTS sink determines advertised current from vRd on either CC pin.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• TS Sink 检测并监控 CC 引脚上的 vRd，以了解 VBUS 上的可用电流，并执行所需的任何方向 • DTS Source 监控两个 CC 引脚是否断开，当检测到任一引脚断开时，进入 UnattachedDeb.SRC • TS Sink 监控 VBUS 是否断开，当检测到断开时，进入 Unattached.SNK

B.2.5.1.2 DTS 源到 TS DRP 行为

下面描述了 DTS 源连接到 TS DRP 时的行为。

1. DTS Source 和 TS DRP 处于未连接状态 • TS DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替 2. DTS Source 通过 AttachWaitDeb.SRC 从 UnattachedDeb.SRC 转换为 AttachedDeb.SRC • DTS Source 检测到两个 CC 引脚上的 TS DRP 下拉并进入 AttachWaitDeb.SRC。tCCDebounce 之后，它进入 AttachedDeb.SRC • DTS Source 打开 VBUS

3. TS DRP 通过 AttachWait.SNK 从 Unattached.SNK 转换为 DebugAccessory.SNK

Unattached.SNK 中的 • TS DRP 检测到两个 CC 引脚上的 DTS 源上拉电阻并进入 AttachWait.SNK。该状态持续 tCCDebounce 后，检测到 VBUS，然后进入 DebugAccessory.SNK

4. 当 DTS Source 和 TS DRP 处于各自的连接状态时：

• DTS 源根据提供的电流需要调整两个 Rp 值 • TS DRP 检测并监控两个 CC 引脚上的 vRd，以了解 VBUS 上的可用电流并执行任何所需的定位 • DTS 源监控两个 CC 引脚是否分离，检测到分离后进入 UnattachedDeb.SRC • TS DRP 监控 VBUS 是否分离，检测到分离后进入 Unattached.SNK（并恢复在 Unattached.SNK 和 Unattached.SRC 之间切换）

B.2.5.1.3 DTS 接收器到 TS 源的行为

下面描述了 DTS Sink 连接到 TS Source 时的行为。

1. TS Source 和 DTS Sink 处于未连接状态

2. TS Source 通过 AttachWait.SRC 从 Unattached.SRC 过渡到 UnientedDebugAccessory.SRC

• TS Source 检测到 DTS Sink 在两个 CC 引脚上的下拉，并进入 AttachWait.SRC。tCCDebounce 之后，进入 UnientedDebugAccessory.SRC。• TS Source 打开 VBUS

3、DTS Sink 通过 AttachWaitDeb.SNK 从 UnattachedDeb.SNK 转换为 AttachedDeb.SNK。

UnattachedDeb.SNK 中的 • DTS Sink 检测到两个 CC 上的 TS Source 的上拉引脚并进入 AttachWaitDeb.SNK。AttachWaitDeb.SNK 中的 • DTS Sink 检测到两个 CC 引脚上的上拉电阻持续 tCCDebounce 并检测到 VBUS。它进入 AttachedDeb.SNK • DTS Sink 确定任一 CC 引脚上来自 vRd 的通告电流。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4. If orientation supported, DTS Sink adjusts Rd on the non-CC communication pin as needed for orientation detection.
5. If orientation supported, TS Source detects change in vRd of one of the CC pins and transitions from UnorientedDebugAccessory.SRC to OrientedDebugAccessory.SRC and performs any orientation required.
6. While the TS Source and DTS Sink are in the attached state:
   - If orientation is supported, DTS sink determines any change in advertised current from vRd of the CC pin that has been set as the CC communication pin.
   - TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC
   - DTS Sink monitors VBUS for detach and when detected, enters UnattachedDeb.SNK

B.2.5.1.4 DTS Sink to TS DRP Behavior

The following describes the behavior when a DTS Sink is connected to a TS DRP.

1. DTS Sink and TS DRP in the unattached state
   - TS DRP alternates between Unattached.SRC and Unattached.SNK
2. TS DRP transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC
   - TS DRP in Unattached.SRC detects both CC pull-downs of DTS Sink in UnattachedDeb.SNK and enters AttachWait.SRC
   - TS DRP in AttachWait.SRC detects that the pull-downs on both CC pins persist for tCCDebounce. It then enters UnorientedDebugAccessory.SRC and turns on VBUS
3. DTS Sink transitions from UnattachedDeb.SNK to AttachedDeb.SNK through AttachWaitDeb.SNK.
   - DTS Sink in UnattachedDeb.SNK detects the TS DRP's pull-ups on both CC pins and enters AttachWaitDeb.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters AttachedDeb.SNK
   - DTS sink determines advertised current from vRd on either CC pin.
7. If orientation is supported, DTS Sink adjusts Rd on the non-CC communication pin as needed for orientation detection.
8. If orientation supported, TS DRP detects change in vRd on one of the CC pins and transitions to OrientedDebugAccessory.SRC and performs the required orientation.
9. While the TS DRP and DTS Sink are in the attached state:
   - If orientation is supported, DTS sink determines any change in advertised current from vRd of the CC pin that has been set as the CC communication pin.
   - TS DRP monitors both CC pins for detach and when detected, enters Unattached.SNK
   - DTS Sink monitors VBUS for detach and when detected, enters UnattachedDeb.SNK

B.2.5.1.5 DTS DRP to TS Sink Behavior

The following describes the behavior when a DTS DRP is connected to a TS Sink.

1. DTS DRP and TS Sink in the unattached state

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

4. 如果支持方向，DTS Sink 会根据需要调整非 CC 通信引脚上的 Rd，以进行方向检测。5. 如果支持方向，TS Source 会检测其中一个 CC 引脚的 vRd 变化，并从 UnientedDebugAccessory.SRC 转换为 OrientedDebugAccessory.SRC，并执行所需的任何方向。6. 当 TS Source 和 DTS Sink 处于连接状态时：• 如果支持方向，DTS Sink 会确定已设置为 CC 通信引脚的 CC 引脚的 vRd 中公布的电流的任何变化。

• TS Source 监控两个 CC 引脚是否断开，检测到断开后进入 Unattached.SRC • DTS Sink 监控 VBUS 是否断开，检测到断开后进入 UnattachedDeb.SNK

B.2.5.1.4 DTS 接收器到 TS DRP 行为

下面描述了 DTS Sink 连接到 TS DRP 时的行为。

1. DTS Sink 和 TS DRP 处于未连接状态 • TS DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替 2. TS DRP 通过以下方式从 Unattached.SRC 转换为 Unientached.SRC

AttachWait.SRC

• Unattached.SRC 中的 TS DRP 检测到 UnattachedDeb.SNK 中 DTS Sink 的两个 CC 下拉，并进入 AttachWait.SRC • AttachWait.SRC 中的 TS DRP 检测到两个 CC 引脚上的下拉持续了 tCCDebounce。然后它进入 UnientedDebugAccessory.SRC 并打开 VBUS

3、DTS Sink 通过 AttachWaitDeb.SNK 从 UnattachedDeb.SNK 转换为 AttachedDeb.SNK。

UnattachedDeb.SNK 中的 • DTS Sink 检测两个 CC 引脚上的 TS DRP 上拉电阻并进入 AttachWaitDeb.SNK。该状态持续 tCCDebounce 后，检测到 VBUS，进入 AttachedDeb.SNK • DTS Sink 确定任一 CC 引脚上来自 vRd 的通告电流。

7. 如果支持方向，DTS Sink 会根据需要调整非 CC 通信引脚上的 Rd，以进行方向检测。8. 如果支持方向，TS DRP 会检测其中一个 CC 引脚上的 vRd 变化，然后转换到 OrientedDebugAccessory.SRC 并执行所需的方向。9. 当 TS DRP 和 DTS Sink 处于连接状态时：• 如果支持方向，DTS Sink 会确定已设置为 CC 通信引脚的 CC 引脚的 vRd 中公布电流的任何变化。• TS DRP 监控两个 CC 引脚是否断开，检测到断开后进入 Unattached.SNK • DTS Sink 监控 VBUS 是否断开，检测到断开后进入 UnattachedDeb.SNK

B.2.5.1.5 DTS DRP 到 TS 接收器行为

下面描述了 DTS DRP 连接到 TS Sink 时的行为。

1. 未连接状态下的DTS DRP和TS Sink

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK

2. DTS DRP transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS DRP in UnattachedDeb.SRC detects both of the CC pull-downs of TS Sink enters AttachWaitDeb.SRC
   - DTS DRP in AttachWaitDeb.SRC detects that the pull-downs on both CC pins persist for tCCDebounce. It then enters AttachedDeb.SRC
   - DTS DRP turns on VBUS
3. TS Sink transitions from Unattached.SNK to DebugAccessory.SNK through AttachWait.SNK
   - TS Sink in Unattached.SNK detects the DTS DRP's pull-ups on both CC pins and enters AttachWait.SNK
   - TS Sink in AttachWait.SNK detects that the pull-ups on both CC pins persist for tCCDebounce and it detects VBUS. It enters DebugAccessory.SNK
4. While the DTS DRP and TS Sink are in their respective attached states:
   - DTS DRP adjusts Rp as needed for offered current
   - TS Sink detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required
   - DTS DRP monitors both CC pins for detach and when detected, enters UnattachedDeb.SNK
   - TS Sink monitors VBUS for detach and when detected, enters Unattached.SNK

B.2.5.1.6 DTS DRP to TS DRP Behavior

The following describes the behavior when a DTS DRP is connected to TS DRP.

Case #1:

1. Both DRPs in the unattached state
   - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
   - TS DRP alternate between Unattached.SRC and Unattached.SNK
2. DTS DRP transitions from UnattachedDeb.SRC to AttachWaitDeb.SRC
   - DTS DRP in UnattachedDeb.SRC detects both CC pull-downs of TS DRP in Unattached.SNK and enters AttachWaitDeb.SRC
3. TS DRP transitions from Unattached.SNK to AttachWait.SNK
   - TS DRP in Unattached.SNK detects both CC pull-ups of DTS DRP and enters AttachWait.SNK
4. DTS DRP transitions from AttachWaitDeb.SRC to AttachedDeb.SRC
   - DTS DRP in AttachWaitDeb.SRC continues to see both CC pull-downs of TS DRP for tCCDebounce, enters AttachedDeb.SRC and turns on VBUS
5. TS DRP transitions from AttachWait.SNK to DebugAccessory.SNK
   - TS DRP detects DTS DRP's pull-ups on both CC pins for tCCDebounce and detects VBUS and enters DebugAccessory.SNK
   - TS DRP detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required
6. While the TS DRP and DTS DRP are in the attached state:

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• DTS DRP 在 UnattachedDeb.SRC 和 UnattachedDeb.SNK 之间交替

2.DTS DRP通过AttachWaitDeb.SRC从UnattachedDeb.SRC过渡到AttachedDeb.SRC

• UnattachedDeb.SRC 中的 DTS DRP 检测到 TS Sink 的两个 CC 下拉都进入 AttachWait Deb.SRC • AttachWaitDeb.SRC 中的 DTS DRP 检测到两个 CC 引脚上的下拉都持续了 t CCDebounce。然后进入 AttachedDeb.SRC • DTS DRP 打开 VBUS

3. TS Sink 通过 AttachWait.SNK 从 Unattached.SNK 过渡到 DebugAccessory.SNK

• Unattached.SNK 中的 TS Sink 检测到两个 CC 引脚上的 DTS DRP 上拉电阻，并进入 Att achWait.SNK • AttachWait.SNK 中的 TS Sink 检测到两个 CC 引脚上的上拉电阻持续 tCC Debounce，并检测到 VBUS。它进入 DebugAccessory.SNK

4.当DTS DRP和TS Sink处于各自的连接状态时：

• DTS DRP 根据提供的电流调整 Rp • TS Sink 检测并监控 CC 引脚上的 vRd，以了解 VB US 上的可用电流，并执行所需的任何定位 • DTS DRP 监控两个 CC 引脚是否分离，检测到分离后进入 UnattachedDeb.SNK • TS Sink 监控 VBUS 是否分离，检测到分离后进入 Unattached.SNK

B.2.5.1.6 DTS DRP 到 TS DRP 行为

下面描述了 DTS DRP 连接到 TS DRP 时的行为。

案例 #1：

1. 两个 DRP 都处于未连接状态 • DTS DRP 在 UnattachedDeb.SRC 和 UnattachedDeb.SNK 之间交替 • TS DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替 2. DTS DRP 从 UnattachedDeb. SRC 转换为 AttachWaitDeb.SRC • UnattachedDeb.SRC 中的 DTS DRP 检测到 Unattached.SNK 中 TS DRP 的两个 CC 下拉并进入 AttachWaitDeb.SRC 3. TS DRP 从 Unattached.SNK 转换为 A ttachWait.SNK • Unattached.SNK 中的 TS DRP 检测到 DTS DRP 的两个 CC 上拉并进入 Attach Wait.SNK 4. DTS DRP 从 AttachWaitDeb.SRC 转换为AttachedDeb.SRC • AttachWaitDeb.SRC 中的 DTS DRP 继续看到 TS DR 的两个 CC 下拉

磷

对于 tCCDebounce，进入 AttachedDeb.SRC 并打开 VBUS 5. TS DRP 从 AttachWait.S NK 转换到 DebugAccessory.SNK • TS DRP 检测 DTS DRP 在两个 CC 引脚上的上拉电阻，以进行 tCCDebounce 并检测 VBUS 并进入 DebugAccessory.SNK • TS DRP 检测并监控 CC 引脚上的 vRd，以了解 VBUS 上的可用电流

并执行任何所需的定位 6. 当 TS DRP 和 DTS DRP 处于
连接状态时：

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- TS DRP monitors VBUS for detach and when detected, enters Unattached.SNK
- DTS DRP monitors both CC pins for detach and when detected, enters UnattachedDeb.SNK

Case #2:

1. Both DRPs in the unattached state
   - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
   - TS DRP alternate between Unattached.SRC and Unattached.SNK
2. DTS DRP transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK
   - DTS DRP in UnattachedDeb.SNK detects both CC pull-ups of TS DRP in Unattached.SRC and enters AttachWaitDeb.SNK
3. TS DRP transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC
   - TS DRP in Unattached.SRC detects both CC pull-downs of DTS DRP and enters AttachWait.SRC
   - TS DRP in AttachWait.SRC continues to see both CC pull-downs of TS DRP for tCCDebounce, enters UnorientedDebugAccessory.SRC and turns on VBUS
4. DTS DRP transitions from AttachWaitDeb.SNK to TryDeb.SRC
   - DTS DRP in AttachWaitDeb.SNK continues to see both CC pull-ups of TS DRP for tCCDebounce and detects VBUS, enters TryDeb.SRC
5. TS DRP transitions from UnorientedDebugAccessory.SRC to Unattached.SNK
   - TS DRP in UnorientedDebugAccessory.SRC detects the removal of both CC pull-downs of DTS DRP and enters Unattached.SNK
6. TS DRP transitions from Unattached.SNK to AttachWait.SNK
   - TS DRP in Unattached.SNK detects both CC pull-ups of DTS DRP and enters AttachWait.SNK
7. DTS DRP transitions from TryDeb.SRC to AttachedDeb.SRC
   - DTS DRP in TryDeb.SRC detects both CC pull-downs of TS DRP for tTryCCDebounce and enters AttachedDeb.SRC
   - DTS DRP turns on VBUS
8. TS DRP transitions from AttachWait.SNK to DebugAccessory.SNK
   - TS DRP detects DTS DRP's pull-ups on both CC pins for tCCDebounce and detects VBUS and enters DebugAccessory.SNK
9. While the DTS DRP and TS DRP are in their respective attached states:
   - DTS DRP adjusts Rp as needed for offered current
   - TS DRP detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required
   - DTS DRP monitors both CC pins for detach and when detected, enters UnattachedDeb.SNK
   - TS DRP monitors VBUS for detach and when detected, enters Unattached.SNK

B.2.5.1.7 DTS DRP to TS Source Behavior

The following describes the behavior when a DTS DRP is connected to TS Source.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• TS DRP 监控 VBUS 是否断开，检测到断开后进入 Unattached.SNK • DTS DRP 监控两个 CC 引脚是否断开，检测到断开后进入 UnattachedDeb.SNK

案例 #2：

1. 两个 DRP 都处于未连接状态 • DTS DRP 在 UnattachedDeb.SRC 和 UnattachedDeb.SNK 之间交替 • TS DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替 2. DTS DRP 从 UnattachedDeb.SNK 转换为 AttachWaitDeb.SNK • UnattachedDeb.SNK 中的 DTS DRP 检测到 Unattached.SRC 中 TS DRP 的两个 CC 上拉并进入 AttachWaitDeb.SNK 3. TS DRP 通过 AttachWait.SRC 从 Unattached.SRC 转换为 UnientedDebugAccessory.SRC • Unattached.SRC 中的 TS DRP 检测到 DTS DRP 的两个 CC 下拉并进入 AttachWait.SRC • AttachWait.SRC 中的 TS DRP 继续看到两者tCCDebounce 时 TS DRP 的 CC 下拉，进入 Unientached.SRC 并打开 VBUS 4. DTS DRP 从 AttachWaitDeb.SNK 转换到 TryDeb.SRC • AttachWaitDeb.SNK 中的 DTS DRP 继续看到 tCCDebounce 时 TS DRP 的两个 CC 上拉并检测 VBUS，进入 TryDeb.SRC 5. TS DRP 从 Unientached.SRC 转换到 Unattached.SNK • Unientached.SNK 中的 TS DRP 检测到 DTS DRP 的两个 CC 下拉均被移除，并进入 Unattached.SNK 6. TS DRP 从 Unattached.SNK 转换到 AttachWait.SNK • Unattached.SNK 中的 TS DRP 检测到 DTS DRP 的两个 CC 上拉并进入AttachWait.SNK 7. DTS DRP 从 TryDeb.SRC 转换到 AttachedDeb.SRC • TryDeb.SRC 中的 DTS DRP 检测到 tTryCCDebounce 时 TS DRP 的两个 CC 下拉，并进入 AttachedDeb.SRC • DTS DRP 打开 VBUS 8. TS DRP 从 AttachWait.SNK 转换到 DebugAccessory.SNK • TS DRP 检测到 tCCDebounce 时 DTS DRP 在两个 CC 引脚上的上拉，并检测 VBUS 并进入 DebugAccessory.SNK 9. 当 DTS DRP 和 TS DRP 处于各自的连接状态时：• DTS DRP 根据需要调整 Rp 以获得提供的电流 • TS DRP 检测并监控 CC 引脚上的 vRd 以获取 VBUS 上的可用电流并执行任何所需的方向 • DTS DRP 监控两个 CC 引脚是否断开，检测到断开后进入 UnattachedDeb.SNK • TS DRP 监控 VBUS 是否断开，检测到断开后进入 Unattached.SNK

B.2.5.1.7 DTS DRP 到 TS 源行为

下面描述了 DTS DRP 连接到 TS Source 时的行为。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

1. DTS DRP and TS Source in the unattached state
   - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
   - TS Source in Unattached.SRC
2. DTS DRP transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK
   - DTS DRP in UnattachedDeb.SNK detects pull-ups on both CC pins and enters AttachWaitDeb.SNK
3. TS Source transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC
   - TS Source in Unattached.SRC detects both CC pull-downs of DTS DRP and enters AttachWait.SRC
   - TS Source in AttachWait.SRC continues to see both CC pull-downs of DTS DRP for tCCDebounce, enters UnorientedDebugAccessory.SRC and turns on VBUS
4. DTS DRP transitions from AttachWaitDeb.SNK to TryDeb.SRC
   - DTS DRP in AttachWaitDeb.SNK continues to see both CC pull-ups of TS DRP for tCCDebounce and detects VBUS, enters TryDeb.SRC
5. TS Source transitions from UnorientedDebugAccessory.SRC to Unattached.SRC
   - TS Source in UnorientedDebugAccessory.SRC detects the removal of both CC pull-downs of DTS DRP and enters Unattached.SRC
6. DTS DRP transitions from TryDeb.SRC to TryWaitDeb.SNK
   - After tDRPTry, DTS DRP does not see pull-downs on both CC pin and enters TryWaitDeb.SNK
7. TS Source transitions from Unattached.SRC to UnorientedDebugAccessory.SRC
   - TS Source in Unattached.SRC detects pull-downs on both CC pins and enters AttachWait.SRC
   - TS Source continues to detect pull-downs on both CC pins for tCCDebounce and enters UnorientedDebugAccessory.SRC and outputs VBUS
8. DTS DRP transitions from TryWaitDeb.SNK to AttachedDeb.SNK
   - DTS DRP sees pull-ups on both CC pins for tCCDebounce and detects VBUS and enters AttachedDeb.SNK
   - If orientation required, DTS DRP adjusts Rd on the non-CC communication pin as needed for orientation detection
9. If orientation supported, TS Source detects change in vRd on one of the CC pins and transitions to OrientedDebugAccessory.SRC and performs the required orientation.
10. While the TS Source and DTS DRP are in the attached state:
    - If orientation is supported, DTS DRP determines any change in advertised current from vRd of the CC pin that has been set as the CC communication pin.
    - TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC
    - DTS DRP monitors VBUS for detach and when detected, enters UnattachedDeb.SNK

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

1. DTS DRP 和 TS Source 处于未连接状态

   • DTS DRP 在 UnattachedDeb.SRC 和 UnattachedDeb.SNK 之间交替 • Unattached.SRC 中的 TS 源

2. DTS DRP 从 UnattachedDeb.SNK 转换为 AttachWaitDeb.SNK

   UnattachedDeb.SNK 中的 • DTS DRP 检测到两个 CC 引脚上的上拉电阻并进入 AttachWaitDeb.SNK

3. TS Source 通过 AttachWait.SRC 从 Unattached.SRC 转换为 UnientedDebugAccessory.SRC

   • Unattached.SRC 中的 TS Source 检测到 DTS DRP 的两个 CC 下拉并进入 AttachWait.SRC • AttachWait.SRC 中的 TS Source 继续看到 tCCDebounce 的 DTS DRP 的两个 CC 下拉，进入 UnientedDebugAccessory.SRC 并打开 VBUS

4. DTS DRP 从 AttachWaitDeb.SNK 转换为 TryDeb.SRC

   AttachWaitDeb.SNK 中的 • DTS DRP 继续看到 tCCDebounce 的 TS DRP 的两个 CC 上拉，并检测到 VBUS，进入 TryDeb.SRC

5. TS 源从 UnientedDebugAccessory.SRC 转换为 Unattached.SRC

   UnientedDebugAccessory.SRC 中的 • TS Source 检测到 DTS DRP 的两个 CC 下拉都被删除，并进入 Unattached.SRC

6. DTS DRP 从 TryDeb.SRC 转换为 TryWaitDeb.SNK

   • tDRPTry 之后，DTS DRP 未在两个 CC 引脚上看到下拉，因此进入 TryWaitDeb.SNK

7. TS 源从 Unattached.SRC 转换为 UnientedDebugAccessory.SRC

   • TS Source 在 Unattached.SRC 中检测到两个 CC 引脚上的下拉并进入 AttachWait.SRC • TS Source 继续检测两个 CC 引脚上的下拉并持续 tCCDebounce，然后进入 UnientedDebugAccessory.SRC 并输出 VBUS

8. DTS DRP 从 TryWaitDeb.SNK 转换为 AttachedDeb.SNK

   • DTS DRP 看到两个 CC 引脚上的 tCCDebounce 上拉电阻，并检测 VBUS 并进入 AttachedDeb.SNK • 如果需要方向，DTS DRP 会根据需要调整非 CC 通信引脚上的 Rd 以进行方向检测

9. 如果支持方向，TS Source 会检测其中一个 CC 引脚上的 vRd 变化，然后转换到 OrientedDebugAccessory.SRC 并执行所需的方向。

10. 当 TS Source 和 DTS DRP 处于连接状态时：

    • 如果支持方向，DTS DRP 将从已设置为 CC 通信引脚的 CC 引脚的 vRd 确定公布电流的任何变化。

    • TS 源监控两个 CC 引脚是否断开，检测到断开后进入 Unattached.SRC • DTS DRP 监控 VBUS 是否断开，检测到断开后进入 UnattachedDeb.SNK

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B.2.5.2 DTS Port to non-DAM TS Port Interoperability Behaviors

The following sub-sections describe the non-functional port-to-port interoperability behaviors for the various combinations of DTS and TS Sources, Sinks, and DRPs that do not support DAM.

B.2.5.2.1 DTS Source to non-DAM TS Sink Behavior

The following describes the behavior when a DTS Source is connected to a non-DAM TS Sink.

1. DTS Source and TS Sink in the unattached state
2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS Source detects the non-DAM TS Sink's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC
   - DTS Source turns on VBUS
3. Non-DAM TS Sink transitions from Unattached.SNK to AttachWait.SNK.
   - Non-DAM TS Sink in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK.
   - Non-DAM TS Sink continues to detect pull-ups on both CC pins and stays in AttachWait.SNK because it does not support DAM (will not enter Attached.SNK because it does not detect SNK.Open on either pin)
4. While the DTS Source and non-DAM TS Sink are in their final state:
   - DTS Source adjusts Rp as needed for offered current
   - Non-DAM TS Sink may draw USB default current from DTS Source as permitted by Section 4.5.2.2 but will not enter DAM
   - DTS Source monitors both CC pins for detach and when detected, enters UnattachedDeb.SRC
   - Non-DAM TS Sink monitors both CC pins for detach and when detected, enters Unattached.SNK

B.2.5.2.2 DTS Source to non-DAM TS DRP Behavior

The following describes the behavior when a DTS Source is connected to a non-DAM TS DRP.

1. DTS Source and non-DAM TS DRP in the unattached state
   - Non-DAM TS DRP alternates between Unattached.SRC and Unattached.SNK
2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS Source detects the non-DAM TS Sink's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC
   - DTS Source turns on VBUS
3. Non-DAM TS DRP transitions from Unattached.SNK to AttachWait.SNK.
   - Non-DAM TS DRP in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK.
   - Non-DAM TS DRP continues to detect pull-downs on both CC pins and stays in AttachWait.SNK because it does not support DAM (will not enter Attached.SNK because it does not detect SNK.Open on either pin)
4. While the DTS Source and non-DAM TS DRP are in their final state:

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

B.2.5.2 DTS 端口到非 DAM TS 端口互操作性行为

以下小节描述了不支持 DAM 的 DTS 和 TS 源、接收器和 DRP 的各种组合的非功能性端口到端口互操作性行为。

B.2.5.2.1 DTS 源到非 DAM TS 接收器行为

下面描述了 DTS 源连接到非 DAM TS 接收器时的行为。

1. DTS Source 和 TS Sink 处于未连接状态
2. DTS Source 通过 AttachWaitDeb.SRC 从 UnattachedDeb.SRC 过渡到 AttachedDeb.SRC

   • DTS Source 检测到两个 CC 引脚上的非 DAM TS Sink 下拉，并进入 AttachWaitDeb.SRC。tCCDebounce 之后，它进入 AttachedDeb.SRC • DTS Source 打开 VBUS

3.非DAM TS Sink从Unattached.SNK转换为AttachWait.SNK。

   • Unattached.SNK 中的非 DAM TS Sink 检测到两个 CC 引脚上的 DTS Source 上拉电阻并进入 AttachWait.SNK。• 非 DAM TS Sink 继续检测两个 CC 引脚上的上拉电阻并停留在 AttachWait.SNK 中，因为它不支持 DAM（不会进入 Attached.SNK，因为它未检测到任何引脚上的 SNK.Open）

4. 当 DTS 源和非 DAM TS 接收器处于最终状态时：

   • DTS 源根据提供的电流调整 Rp • 非 DAM TS 接收器可以从 DTS 源吸取 USB 默认电流，如第 4.5.2.2 节所允许，但不会进入 DAM • DTS 源监控两个 CC 引脚是否断开，检测到断开后进入 UnattachedDeb.SRC • 非 DAM TS 接收器监控两个 CC 引脚是否断开，检测到断开后进入 Unattached.SNK

B.2.5.2.2 DTS 源到非 DAM TS DRP 行为 下面描述了 DTS 源连接到非 DAM TS DRP 时的行为。

1. DTS 源和非 DAM TS DRP 处于未连接状态 • 非 DAM TS DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替
2. DTS Source 通过 AttachWaitDeb.SRC 从 UnattachedDeb.SRC 过渡到 AttachedDeb.SRC

   • DTS Source 检测到两个 CC 引脚上的非 DAM TS Sink 下拉，并进入 AttachWaitDeb.SRC。tCCDebounce 之后，它进入 AttachedDeb.SRC • DTS Source 打开 VBUS

3. 非 DAM TS DRP 从 Unattached.SNK 转换到 AttachWait.SNK。• Unattached.SNK 中的非 DAM TS DRP 检测到两个 CC 引脚上的 DTS 源上拉并进入 AttachWait.SNK。• 非 DAM TS DRP 继续检测两个 CC 引脚上的下拉并停留在 AttachWait.SNK 中，因为它不支持 DAM（不会进入 Attached.SNK，因为它没有检测到任何引脚上的 SNK.Open）4. 当 DTS 源和非 DAM TS DRP 处于其最终状态时：

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- DTS Source adjusts Rp as needed for offered current
- Non-DAM TS DRP may draw USB default current from DTS Source as permitted by Section 4.5.2.2 but will not enter DAM
- DTS Source monitors both CC pins for detach and when detected, enters UnattachedDeb.SRC
- Non-DAM TS DRP monitors both CC pins for detach and when detected, enters Unattached.SRC

B.2.5.2.3 DTS Sink to non-DAM TS Source Behavior

The following describes the behavior when a DTS Sink is connected to a non-DAM TS Source.

1. Non-DAM TS Source and DTS Sink in the unattached state
2. Non-DAM TS Source transitions from Unattached.SRC to AttachWait.SRC
   - Non-DAM TS Source detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.SRC.
   - Non-DAM TS Source continues to detect pull-downs on both CC pins and stays in AttachWait.SRC because it does not support DAM (will not enter Attached.SRC because it does not detect SRC.Rd on only one CC pin)
3. DTS Sink transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK.
   - DTS Sink in UnattachedDeb.SNK detects the non-DAM TS Source's pull-ups on both CC pins and enters AttachWaitDeb.SNK
   - DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS
4. While the non-DAM TS Source and DTS Sink are in their final state:
   - Non-DAM TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC
   - DTS Sink monitors VBUS for attach and both CC pins for detach and enters UnattachedDeb.SNK when both CC pins go to SNK.Open

B.2.5.2.4 DTS Sink to non-DAM TS DRP Behavior

The following describes the behavior when a DTS Sink is connected to a non-DAM TS DRP.

1. DTS Sink and non-DAM TS DRP in the unattached state
   - Non-DAM TS DRP alternates between Unattached.SRC and Unattached.SNK
   - DTS Sink in UnattachedDeb.SNK
2. Non-DAM TS DRP transitions from Unattached.SRC to AttachWait.SRC
   - Non-DAM TS DRP detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.SRC.
   - Non-DAM TS DRP continues to detect pull-downs on both CC pins and stays in AttachWait.SRC because it does not support DAM (will not enter Attached.SRC because it does not detect SRC.Rd on only one CC pin)
3. DTS Sink transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK.
   - DTS Sink in UnattachedDeb.SNK detects the non-DAM TS DRP's pull-ups on both CC pins and enters AttachWaitDeb.SNK
   - DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS
4. While the non-DAM TS DRP and DTS Sink are in their final state:

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• DTS 源根据提供的电流调整 Rp • 非 DAM TS DRP 可以从 DTS 源吸取 USB 默认电流，如第 4.5.2.2 节所允许，但不会进入 DAM • DTS 源监控两个 CC 引脚是否断开，检测到断开后进入 UnattachedDeb.SRC • 非 DAM TS DRP 监控两个 CC 引脚是否断开，检测到断开后进入 Unattached.SRC

B.2.5.2.3 DTS 接收器至非 DAM TS 源行为

下面描述了 DTS Sink 连接到非 DAM TS Source 时的行为。

1. 非DAM TS Source和DTS Sink处于未连接状态
2. 非 DAM TS 源从 Unattached.SRC 转换为 AttachWait.SRC

   • 非 DAM TS 源检测到 DTS 接收器在两个 CC 引脚上的下拉，并进入 AttachWait.SRC。• 非 DAM TS 源继续检测两个 CC 引脚上的下拉，并保持

   在 AttachWait.SRC 中，因为它不支持 DAM（不会进入 Attached.SRC，因为它仅在一个 CC 引脚上检测不到 SRC.Rd）
3. DTS Sink 从 UnattachedDeb.SNK 转换为 AttachWaitDeb.SNK。

   • UnattachedDeb.SNK 中的 DTS Sink 检测到两个 CC 引脚上的非 DAM TS Source 上拉电阻，并进入 AttachWaitDeb.SNK • DTS Sink 仍处于 AttachWaitDeb.SNK 中，因为它未检测到 VBUS
4. 当非 DAM TS 源和 DTS 接收器处于最终状态时：

   • 非 DAM TS 源监控两个 CC 引脚是否断开，检测到断开后进入未连接状态。SRC
   • DTS 接收器监控 VBUS 是否连接，监控两个 CC 引脚是否断开，然后进入

   当两个 CC 引脚都转到 SNK.Open 时，UnattachedDeb.SNK

B.2.5.2.4 DTS 接收器至非 DAM TS DRP 行为

下面描述了当 DTS Sink 连接到非 -DAM TS DRP 时的行为。

1. DTS Sink 和非 DAM TS DRP 处于未连接状态

   • 非 DAM TS DRP 在 Unattached.SRC 和 Unattached.SNK 之间交替 • UnattachedDeb.SNK 中的 DTS Sink
2. 非 DAM TS DRP 从 Unattached.SRC 转换为 AttachWait.SRC

   • 非 DAM TS DRP 检测两个 CC 引脚上的 DTS Sink 下拉并进入 AttachWait.SRC。• 非 DAM TS DRP 继续检测两个 CC 引脚上的下拉并停留在 AttachWait.SRC，因为它不支持 DAM（不会进入 Attached.SRC，因为它仅在一个 CC 引脚上未检测到 SRC.Rd）
3. DTS Sink 从 UnattachedDeb.SNK 转换为 AttachWaitDeb.SNK。

   UnattachedDeb.SNK 中的 • DTS Sink 检测到非 DAM TS DRP 的上拉 CC 引脚并进入 AttachWaitDeb.SNK • DTS Sink 保持在 AttachWaitDeb.SNK 中，因为它没有检测到 VBUS
4. 当非 DAM TS DRP 和 DTS Sink 处于最终状态时：

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- Non-DAM TS DRP monitors both CC pins for detach and when detected, enters Unattached.SNK
- DTS Sink monitors VBUS for attach and both CC pins for detach and enters UnattachedDeb.SNK when both CC pin go to SNK.Open

B.2.5.2.5 DTS DRP to non-DAM TS Sink Behavior

The DTS DRP to non-DAM TS Sink behavior follows the flow in Section B.2.5.2.1.

B.2.5.2.6 DTS DRP to non-DAM TS DRP Behavior

The DTS DRP to non-DAM TS DRP behavior follows the flows in Section B.2.5.2.2 and Section B.2.5.2.4 depending on the role forced by the non-DAM TS DRP

B.2.5.2.7 DTS DRP to non-DAM TS Source Behavior

The following describes the behavior when a DTS DRP is connected to non-DAM TS Source.

1. DTS DRP and non-DAM TS Source in the unattached state
   - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
   - Non-DAM TS Source in Unattached.SRC
2. DTS DRP transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK
   - DTS DRP in UnattachedDeb.SNK detects pull-ups on both CC pins and enters AttachWaitDeb.SNK
3. Non-DAM TS Source transitions from Unattached.SRC to AttachWait.SRC
   - Non-DAM TS Source in Unattached.SRC detects pull-downs on both CC pins and enters AttachWait.SRC
   - Non-DAM TS Source continues to detect pull-downs on both CC pins and stays in AttachWait.SRC because it does not support DAM (will not enter Attached.SRC because it does not detect SRC.Rd on only one CC pin)
   - DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS
5. While the non-DAM TS Source and DTS DRP are in their final state:
   - Non-DAM TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC
   - DTS DRP monitors VBUS for attach and both CC pins for detach and enters UnattachedDeb.SRC when both CC pin go to SNK.Open

B.2.5.2.8 DTS Sink to non-DAM TS Sink with Accessory Support Behavior

The following describes the behavior when a DTS Sink is connected to a non-DAM USB Type-C TS Sink with Accessory Support.

1. DTS Sink and non-DAM TS Sink with Accessory Support ("non-DAM TS Sink" for the remainder of this flow) in the unattached state
   - Non-DAM TS Sink alternates between Unattached.SNK and Unattached.Accessory
   - DTS Sink in UnattachedDeb.SNK
2. Non-DAM TS Sink transitions from Unattached.Accessory to AttachWait.Accessory
   - Non-DAM TS Sink detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.Accessory

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• 非 DAM TS DRP 监控两个 CC 引脚是否分离，检测到分离后进入 Unattached.SNK • DTS Sink 监控 VBUS 是否连接，监控两个 CC 引脚是否分离，当两个 CC 引脚都进入 SNK.Open 时进入 UnattachedDeb.SNK

B.2.5.2.5 DTS DRP 到非 DAM TS Sink 行为 DTS DRP 到非 DAM TS Sink 行为遵循第 B.2.5.2.1 节中的流程。

B.2.5.2.6 DTS DRP 到非 DAM TS DRP 行为

DTS DRP 到非 DAM TS DRP 行为遵循第 B.2.5.2.2 节和第 B.2.5.2.4 节中的流程，具体取决于非 DAM TS DRP 强制的角色

B.2.5.2.7 DTS DRP 到非 DAM TS 源行为

下面描述了 DTS DRP 连接到非 DAM TS 源时的行为。

1. DTS DRP 和非 DAM TS 源处于未连接状态

   • DTS DRP 在 UnattachedDeb.SRC 和 UnattachedDeb.SNK 之间交替 • Unattached.SRC 中的非 DAM TS 源

2. DTS DRP 从 UnattachedDeb.SNK 转换为 AttachWaitDeb.SNK

   UnattachedDeb.SNK 中的 • DTS DRP 检测到两个 CC 引脚上的上拉电阻，并进入 AttachWaitDeb.SNK

3. 非 DAM TS 源从 Unattached.SRC 转换为 AttachWait.SRC

   • 未连接的非 DAM TS 源。SRC 检测 CC 引脚上的下拉和
   进入 AttachWait.SRC • 非 DAM TS 源继续检测两个 CC 引脚上的下拉，并停留在 AttachWait.SRC 中，因为它不支持 DAM（不会进入 Attached.SRC，因为它没有检测到只有一个 CC 引脚上的 SRC.Rd）• DTS 接收器停留在 AttachWaitDeb.SNK 中，因为它没有检测到 VBUS

5. 当非 DAM TS 源和 DTS DRP 处于最终状态时：

   • 非 DAM TS 源监控两个 CC 引脚是否分离，检测到分离后进入 Unattached.SRC • DTS DRP 监控 VBUS 是否连接，监控两个 CC 引脚是否分离，当两个 CC 引脚都转至 SNK.Open 时进入 UnattachedDeb.SRC

B.2.5.2.8 DTS 接收器到具有附件支持行为的非 DAM TS 接收器

下面描述了当 DTS Sink 连接到具有配件支持的非 DAM USB Type-C TS Sink 时的行为。

1. 未连接状态下的 DTS 接收器和具有附件支持的非 DAM TS 接收器（本流程的其余部分称为“非 DAM TS 接收器”）

   • 非 DAM TS Sink 在 Unattached.SNK 和 Unattached.Accessory 之间
   交替 • UnattachedDeb.SNK 中的 DTS Sink

2. 非 DAM TS Sink 从 Unattached.Accessory 转换为 AttachWait.Accessory

   • 非 DAM TS Sink 检测到两个 CC 引脚上的 DTS Sink 下拉并进入 AttachWait.Accessory

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- Non-DAM TS Sink continues to detect pull-downs on both CC pins and enters USB Type-C Debug Accessory Mode

3. DTS Sink transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK.
   - DTS Sink in UnattachedDeb.SNK detects the non-DAM TS Sinks pull-ups on both CC pins and enters AttachWaitDeb.SNK
   - DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS
4. While the non-DAM TS DRP and DTS Sink are in their final state:
   - Non-DAM TS Sink monitors both CC pins for detach and when detected, enters Unattached.SNK
   - DTS Sink monitors both CC pins for detach and enters UnattachedDeb.SNK when both CC pins go to SNK.Open

B.2.6 Orientation Detection

Orientation detection is optional normative. A USB Type-C port supporting Debug Accessory Mode is not required to perform orientation detection. If orientation detection is required, this method shall be followed.

B.2.6.1 Orientation Detection using Rd and/or Rp Values

In this optional normative flow, the DTS shall always initiate an orientation detection sequence, independent of its role as Source, Sink, or DRP. This means that the TS must detect this orientation sequence and perform multiplexing to orient and connect the port signals to the proper channels as well as determine the proper CC pin for *USB-PD* communication.

B.2.6.1.1 Orientation Detection with DTS as a Source

When the DTS is presenting an Rp, it shall present asymmetric Rp values (Rp1/Rp2) on CC1/CC2 to indicate orientation to the TS. The DTS as a source shall indicate a weaker resistive value on CC2. Table B-2 shows the values of Rp resistance on each CC pin to indicate orientation and advertise the USB Type-C current available on VBUS. See Table 4-24 for the Rp resistance ranges.

Once the TS sink enters the DebugAccessory.SNK state, after the vRd on both CC pins is stable for tRpValueChange, it will orient its signal multiplexor based on the detected orientation indicated by the relative voltages of the CC pins. The CC pin with the greater voltage is the plug CC pin, which establishes the orientation of the DTS plug in the TS receptacle and also indicates the *USB-PD* CC communication wire. The TS Sink cannot perform *USB-PD* communication or connect any orientation-sensitive debug signals until orientation is determined.

B.2.6.1.2 Orientation Detection with DTS as a Sink

When the DTS is a sink, it shall follow a two-step approach.

1. The DTS sink shall present Rd/Rd on the CC pins of the debug accessory plug. This will put the system into debug accessory mode
2. Once the DTS sink enters AttachedDeb.SNK state, it shall present a resistance to GND of ≤ Ra on B5 (CC2)

The asymmetric signaling is detected by the TS Source in the UnorientedDebugAccessory.SRC state. Once Detected, the TS Source will move to the OrientedDebugAccessory.SRC. Once the TS source enters the OrientedDebugAccessory.SRC state, after the SRC.Ra level is detected on one of the CC pins, it will orient its signal

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- 非 DAM TS 接收器继续检测两个 CC 引脚上的下拉电阻并进入 USB Type-C 调试附件模式

3. DTS Sink 从 UnattachedDeb.SNK 转换为 AttachWaitDeb.SNK。

   UnattachedDeb.SNK 中的 • DTS Sink 检测到非 DAM TS Sinks 上拉
   CC 引脚并进入 AttachWaitDeb.SNK • DTS Sink 保持在 AttachWaitDeb.SNK 中
   ，因为它没有检测到 VBUS

4. 当非 DAM TS DRP 和 DTS Sink 处于最终状态时：

   - 非 DAM TS Sink 监控两个 CC 引脚是否断开，当检测到断开时，进入
     Unattached.SNK • DTS Sink 监控两个 CC 引脚是否分离，当两个 CC 引脚都转到
   SNK.Open 时进入 UnattachedDeb.SNK

B.2.6 方向检测

方向检测是可选规范。支持调试附件模式的 USB Type-C 端口不需要执行方向检测。如果需要方向检测，则应遵循此方法。

B.2.6.1 使用 Rd 和/或 Rp 值进行方向检测

在此可选规范流程中，DTS 应始终启动方向检测序列，无论其角色是源、接收器还是 DRP。这意味着 TS 必须检测此方向序列并执行多路复用以定位和连接端口信号到适当的通道，以及确定用于 *USB-PD* 通信的正确 CC 引脚。

B.2.6.1.1 以 DTS 为源的方向检测

当 DTS 呈现 Rp 时，它应在 CC1/CC2 上呈现不对称 Rp 值 (Rp1/Rp2)，以指示 TS 的方向。作为源的 DTS 应在 CC2 上指示较弱的电阻值。表 B-2 显示了每个 CC 引脚上的 Rp 电阻值，用于指示方向并通告 VBUS 上可用的 USB Type-C 电流。有关 Rp 电阻范围，请参阅表 4-24。

一旦 TS 接收器进入 DebugAccessory.SNK 状态，在两个 CC 引脚上的 vRd 稳定 tRpValueChange 后，它将根据 CC 引脚相对电压指示的检测到的方向调整其信号多路复用器的方向。电压较高的 CC 引脚是插头 CC 引脚，它确定了 DTS 插头在 TS 插座中的方向，并指示 *USB-PD* CC 通信线。在确定方向之前，TS 接收器无法执行 *USB-PD* 通信或连接任何方向敏感的调试信号。

B.2.6.1.2 使用 DTS 作为接收器进行方向检测

当DTS为接收器时，它应遵循两步方法。

1. DTS 接收器应在调试附件插头的 CC 引脚上显示 Rd/Rd。这将使系统进入调试附件模式

2. 一旦DTS接收器进入AttachedDeb.SNK状态，它应呈现对GND的电阻
   ≤ Ra 在 B5 (CC2) 上的分布

非对称信号由 TS 源在
UnientedDebugAccessory.SRC 状态。一旦检测到，TS 源将移至 OrientedDebugAccessory.SRC。一旦 TS 源进入 OrientedDebugAccessory.SRC 状态，在其中一个 CC 引脚上检测到 SRC.Ra 电平后，它将调整其信号

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

multiplexor based on the detected orientation indicated by the relative voltages of the CC pins. The CC pin with the greater voltage is the plug CC pin, which establishes the orientation of the DTS plug in the TS receptacle and also indicates the *USB-PD* CC communication wire. The TS Source cannot perform *USB-PD* communication or connect any orientation-sensitive debug signals until orientation is determined.

B.3 Security/Privacy Requirements:

Debug port(s) typically provide system access beyond the normal operation of USB hardware and protocol. Additional protection against unintended use is needed. The design must incorporate appropriate measures to prohibit unauthorized access or modification of the unit under test and to prevent exposure of private user data on the unit under test. The method of protection is not explicitly defined in this specification.

The vendor shall assert as part of USB compliance certification that:

- The device has met the requirement to protect the system's security and user's privacy in its vendor-specific implementation of the port, and
- The device requires the user to take an explicit action to authorize access to or modification of the unit.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

多路复用器根据 CC 引脚相对电压指示的检测方向来确定 DTS 插头的方向。电压较大的 CC 引脚是插头 CC 引脚，它确定了 DTS 插头在 TS 插座中的方向，并指示了 *USB-PD* CC 通信线。TS 源无法执行 *USB-PD* 通信或连接任何

方向敏感的调试信号，直到确定方向。

B.3 安全/隐私要求：

调试端口通常提供超出 USB 硬件和协议正常运行的系统访问。需要额外的保护措施以防止意外使用。设计必须包含适当的措施，以禁止未经授权的访问或修改被测单元，并防止被测单元上的私人用户数据泄露。本规范未明确定义保护方法。

贩卖 或者应作为 USB 合规认证的一部分进行声明 那 ：

- 该设备在其供应商特定的端口实现中满足了保护系统安全和用户隐私的要求，并且
- 该设备要求用户采取明确的操作来授权访问或修改该设备。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

C USB Type-C Digital Audio

C.1 Overview

One of the goals of USB Type-C® is to help reduce the number of I/O connectors on a host platform. One connector type that could be eliminated is the legacy 3.5 mm audio device jack. While USB Type-C does include definition of an analog audio adapter accessory (see Appendix A), that solution requires a separate adapter that can be readily lost and the host implementation in support of analog audio is technically challenging. To best serve the user experience, a simplified USB Type-C digital audio solution based on native USB protocol is simpler/more interoperable with both the host platform and audio device being connected directly without the need for adapters and operates seamlessly through existing USB topologies (e.g. through hubs and docks).

This appendix is for the optional normative definition of digital audio support on USB Type-C-based products. Any USB Audio Class product, having either a USB Type-C plug or receptacle, and whether it is a host system, typically an audio source, and an audio device, typically an audio sink, shall meet the requirements of this appendix in addition to all other applicable USB specification requirements.

C.2 USB Type-C Digital Audio Specifications

USB Type-C Digital Audio (TCDA), when implemented per this specification, shall be compliant with either the USB Audio Device Class 1.0, 2.0 or 3.0 specifications as listed below. While allowed, basing a TCDA on USB Audio Device Class 1.0 is not recommended. Given the number of benefits in terms of audio profile support, simplified enumeration and configuration, and improved low-power operation, use of the USB Audio Device Class 3.0 is *strongly recommended*.

USB Audio Device Class 1.0 including:

- USB Device Class Definition for Audio Devices, Release 1.0
- USB Device Class Definition for Audio Data Formats, Release 1.0
- USB Device Class Definition for Audio Terminal Types, Release 1.0

USB Audio Device Class 2.0 including:

- USB Device Class Definition for Audio Devices, Release 2.0
- USB Device Class Definition for Audio Data Formats, Release 2.0
- USB Device Class Definition for Audio Terminal Types, Release 2.0

USB Audio Device Class 3.0 including:

- USB Device Class Definition for Audio Devices, Revision 3.0
- USB Device Class Definition for Audio Data Formats, Release 3.0
- USB Device Class Definition for Audio Terminal Types, Release 3.0
- USB Device Class Definition for Basic Audio Functions, Release 3.0

USB Audio Device Class 3.0 specifications now include the definition of basic audio function profiles (Basic Audio Device Definition, BADD). TCDA devices based on USB Audio Device Class 3.0 will implement one of the defined profiles. TCDA-capable hosts based on USB Audio Device Class 3.0 will recognize and typically implement all of the profiles that are relevant to the capabilities and usage models for the host.

TCDA devices shall fall into one of the following two configurations:

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

碳 USB Type-C 数字音频

C.1 概述

USB Type-C v2 的目标之一是帮助减少主机平台上的 I/O 连接器数量。可以消除的一种连接器类型是传统的 3.5 毫米音频设备插孔。虽然 USB Type-C 确实包括模拟音频适配器附件的定义（参见附录 A），但该解决方案需要一个容易丢失的单独适配器，并且支持模拟音频的主机实现在技术上具有挑战性。为了更好地服务用户

经验表明，基于原生 USB 协议的简化 USB Type-C 数字音频解决方案更简单/更具互操作性，主机平台和音频设备均可直接连接，无需适配器，并可通过现有 USB 拓扑（例如通过集线器和基座）无缝运行。

本附录用于对基于 USB Type-C 的产品的数字音频支持的可选规范性定义。任何具有 USB Type-C 插头或插座的 USB 音频类产品，无论是主机系统（通常是音频源）还是音频设备（通常是音频接收器），除了所有其他适用的 USB 规范要求外，还应满足本附录的要求。

C.2 USB Type-C 数字音频规格

USB Type-C 数字音频 (TCDA) 按照本规范实施时，应符合下列 USB 音频设备类 1.0、2.0 或 3.0 规范。虽然允许，但不建议将 TCDA 基于 USB 音频设备类 1.0。鉴于在音频配置文件支持、简化枚举和配置以及改进的低功耗操作方面具有诸多优势，使用 USB 音频设备类 3.0 是 *strongly recommended*。

USB 音频设备类 1.0 包括：

- USB 设备类定义（针对音频设备），版本 1.0
- USB 设备类定义（针对音频数据格式），版本 1.0
- USB 设备类定义（针对音频终端类型），版本 1.0

USB 音频设备类 2.0 包括：

- USB 设备类定义（针对音频设备），版本 2.0
- USB 设备类定义（针对音频数据格式），版本 2.0
- USB 设备类定义（针对音频终端类型），版本 2.0

USB 音频设备类 3.0 包括：

- USB 设备类定义，用于音频设备，修订版 3.0
- USB 设备类定义，用于音频数据格式，版本 3.0
- USB 设备类定义，用于音频终端类型，版本 3.0
- USB 设备类定义，用于基本音频功能，版本 3.0

USB 音频设备类 3.0 规范现在包括基本音频功能配置文件 (Basic Audio Device Definition, BADD) 的定义。基于 USB 音频设备类 3.0 的 TCDA 设备将实现已定义的配置文件之一。基于 USB 音频设备类 3.0 的支持 TCDA 的主机将识别并通常实现与主机功能和使用模型相关的所有配置文件。

TCDA 设备应属于以下两种配置之一：

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- a traditional VBUS-powered USB device that has a USB Type-C receptacle for use with a standard USB Type-C cable, or
- a VCONN-Powered USB Device (VPD) that has a captive cable with a USB Type-C plug (including thumb drive style products).

USB Type-C plug-based TCDA devices shall not be implemented as a variant of the USB Type-C Analog Audio Adapter Accessory (Appendix A).

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- 传统的 VBUS 供电 USB 设备，具有 USB Type-C 插座，可与
  标准 USB Type-C 电缆，或 • 带有带 USB Type-C 插头的固定电缆的 VCONN 供电 USB 设备 (VPD)（包括拇指驱动器样式产品）。

基于 USB Type-C 插头的 TCDA 设备不得作为 USB Type-C 模拟音频适配器配件（附录 A）的变体来实现。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

D Thermal Design Considerations for Active Cables

D.1 Introduction

USB Type C® active cables use active circuitry to realize a longer link than passive cables and to maintain the electrical performance at high speed data transmission (*USB 3.2* Gen2 single-lane or *USB 3.2* Gen1 or Gen2 dual-lane). The additional power dissipation due to active components in the plug over-mold, creates a thermal challenge to passively dissipate power from its active components off limited outer surface area of cable over-mold. Furthermore, the VBUS current, up to 5 A for power delivery, generates joule heat from the conductors along VBUS and GND lines, including copper wires, solder joints, contact pins insides connectors and copper traces on paddle board.

This appendix provides some case studies to show the thermal impacts of certain factors affecting the maximum over-mold surface temperature TS such as IC power inside over-mold (PO), thermal boundary, VBUS current level, and port to port spacing. The case study provided is for a specific mechanical design of the cable. When a different mechanical design (geometry or material, etc.) are used, these impacts need further investigation. The methodology of the study is thermal modelling. The modeling results has been validated for some cases (1.5 W PO and 5A VBUS) with lab test results within ± 3 °C, but not for all cases. Note that this appendix is not a full factorial or complete Design of Experiment (DOE) study and whether there is interaction among any of these factors are not covered here.

To meet thermal requirements specified in Section 5.2.4.1, as well as the junction temperature T_J requirement of any active components, an active cable should be carefully designed to facilitate the desired heat flow paths. A desirable thermal resistance between powered IC to over-mold surface is achieved when neither T_S nor T_J exceeds their specifications. This appendix focuses solely on T_S as output of the study, as the T_J requirement varies depending on the IC requirements.

It is recommended that system integrator such as host or device designer should take into consideration the heat transferred to or from an active cable in the system level thermal analysis.

Nomenclature used in this appendix:

T_A = ambient temperature (°C)

T_J = junction temperature (°C)

T_S = plug over-mold outer surface maximum temperature (°C)

T_{MB} = motherboard/thermal boundary temperature (°C)

P_O = active component power (W) inside the over-mold that directly plugged in the host or device at each end of cable.

D.2 Model

D.2.1 Assumptions

A system model was built which includes a half active cable with one over-mold on the end, a mated pair of connectors (plug and receptacle) and a motherboard as its host or device side thermal boundary. The model assumes the cable is symmetric with VCONN power to be equally divided and each end of cable consumes half of VCONN power for the active components.

It is a Computational Fluid Dynamics (CFD) model with heat transfer of conduction, natural convection and radiation. Emissivity of the plug over-mold and cable jacket is assumed to be 0.92 and the connector metal surfaces is assumed to be 0.05.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

D 有源电缆的热设计考虑因素

D.1 简介

USB Type C® 有源电缆使用有源电路来实现比无源电缆更长的链路，并在高速数据传输（*USB 3.2* Gen2 单通道或 *USB 3.2* Gen1 或 Gen2 双通道）时保持电气性能。插头包覆成型中的~~有源组~~件会产生额外的功耗，~~这带来~~了热挑战，需要将其有源组件的功率从电缆包覆成型的有限外表面区域被动地耗散。此外，VBUS 电流（高达 5 A 的功率传输）会从 VBUS 和 GND 线路沿线的导体产生焦耳热，包括铜线、焊点、连接器内的接触针和桨板上的铜迹线。

本附录提供了一些案例研究，以显示某些因素对最大包覆模制表面温度 TS 的热影响，例如包覆模制内部 IC 电源 (PO)、热边界、VBUS 电流水平和端口到端口间距。提供的案例研究针对电缆的特定机械设计。当使用不同的机械设计（几何形状或材料等）时，需要进一步研究这些影响。研究的方法是热建模。建模结果已针对某些情况（1.5 W PO 和 5A VBUS）进行了验证，实验室测试结果在 ± 3 °C 以内，但并非适用于所有情况。请注意，本附录不是全因子或完整的实验设计 (DOE) 研究，本文未介绍这些因素之间是否存在相互作用。

为了满足第 5.2.4.1 节中规定的热要求以及任何有源元件的结温 T_J 要求，应精心设计有源电缆以促进所需的热流路径。当 T_S 和 T_J 均未超过其规格时，即可实现供电 IC 到包覆成型表面之间的理想热阻。本附录仅关注 T_S 作为研究的输出，因为 T_J 要求因 IC 要求而异。

建议系统集成商（例如主机或设备设计人员）在系统级热分析中考虑往返于有源电缆的热量。

本附录中使用的术语：

T_A = 环境温度（°C） T_J = 结温（°C） T_S = 插头包覆成型外表面最高温度（°C） T_{MB} = 主板/热边界温度（°C） P_O = 直接插入电缆两端主机或设备的包覆成型内的有源元件功率（W）。

D.2 模型

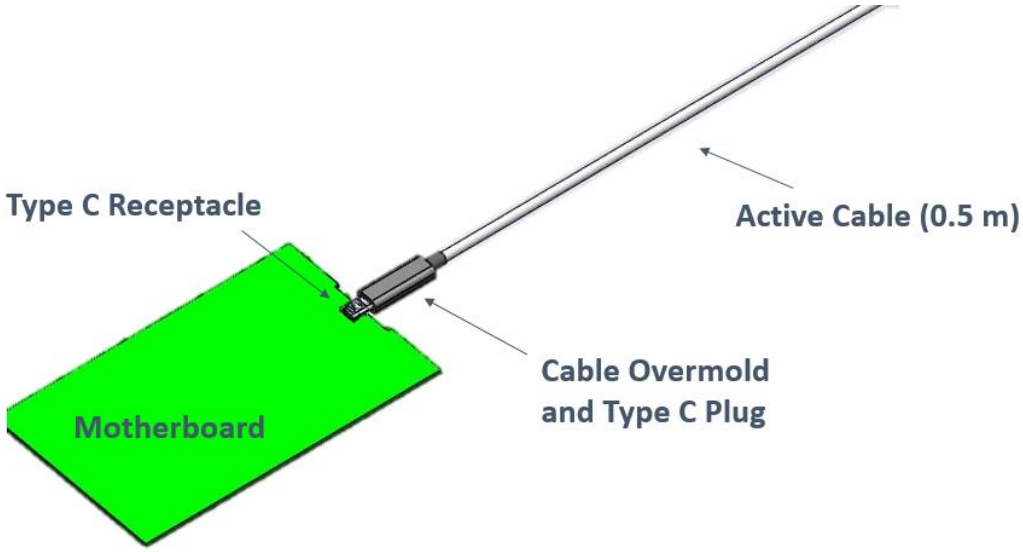
D.2.1 假设

我们建立了一个系统模型，其中包括一根半主动电缆，电缆末端有一个包覆成型件，一对配对的连接器（插头和插座）以及一个主板作为其主机或设备侧热边界。该模型假设电缆是对称的，V CONN 功率被均等分配，并且电缆的每一端为主动组件消耗一半的 V CONN 功率。

这是一种计算流体力学 (CFD) 模型，具有传导、自然对流和辐射传热。插头包覆成型件和电缆护套的辐射率假设为 0.92，连接器金属表面的辐射率假设为 0.05。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

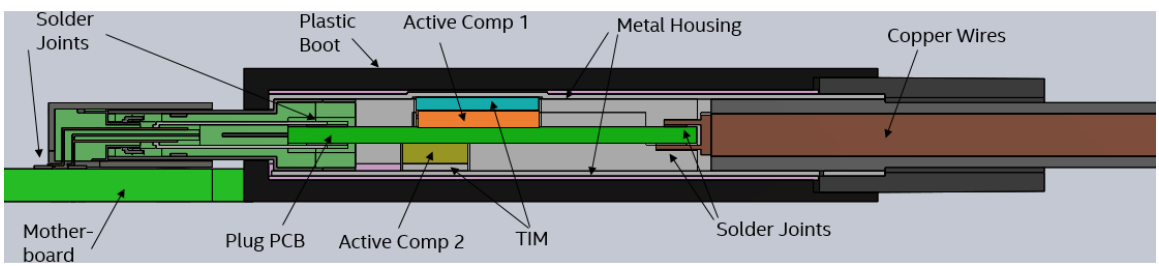
Figure D-1 Active Cable Model (Single Port, Top Mount Receptacle)



D.2.2 Model Architecture

The specific system and cable architecture used in the model is shown below.

Figure D-2 Model Architecture



The simplified cable model uses a pure copper cable, representing a typical short active cable, with total cross section of the copper conductors being about 3.8 mm^2.

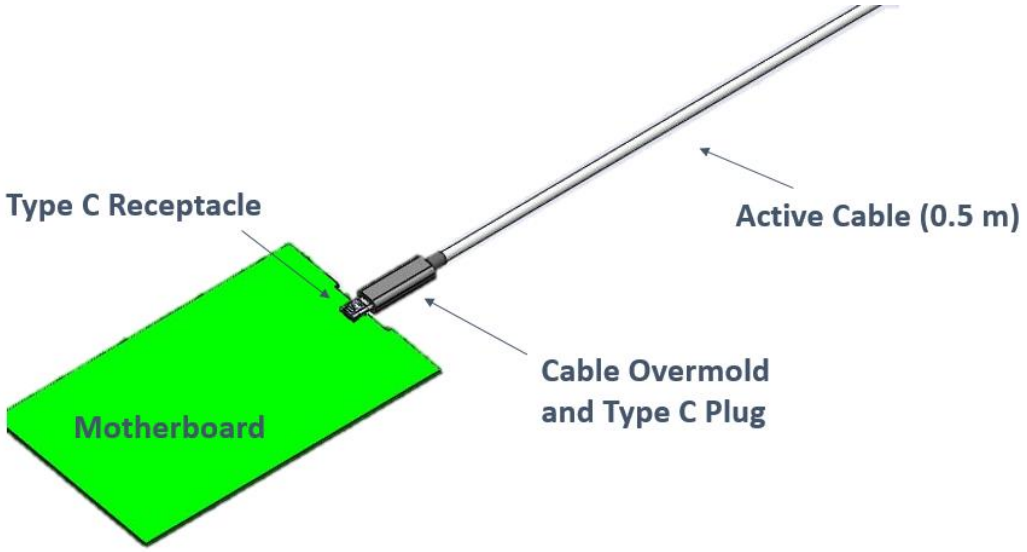
The cable model incorporates a plastic boot for the over-mold which allows a higher surface temperature threshold than some other materials such as metal or glass. The over-mold length in the study was 35 mm.

In this specific cable design, two active components are surface mounted on plug PCB (or paddle board). Thermal Interface Material (TIM) are placed between "hot components" and "heat spreading material" such as metal housings to reduce thermal resistance between component junctions to ambient. Metal shells help to reduce T_S by spreading heat across the over-mold surface and avoid hot spots.

The plug PCB and motherboard are assumed to be FR4 based material. The motherboard is a bulk model assumed to be at a constant temperature without a point heat source on it. The receptacle is top mounted on the motherboard in single port and horizontal stacked cases, Figure D-6; and is vertically mounted in vertical stack up cases, Figure D-4 and Figure D-5.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

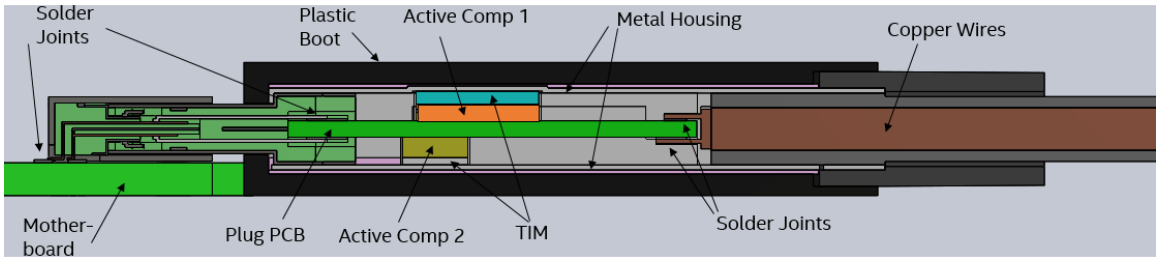
图 D-1 有源电缆模型（单端口，顶部安装插座）



D.2.2 模型架构

该模型所使用的具体系统和电缆架构如下所示。

图 D-2 模型架构



简化的电缆模型采用纯铜电缆，代表典型的短有源电缆，铜导体的总横截面积约为 3.8 毫米^2
。

电缆模型包含一个塑料套管作为包覆成型件，与其他材料（如金属或玻璃）相比，该塑料套管允许更高的表面温度阈值。研究中的包覆成型件长度为 35 毫米。

在这个特定的电缆设计中，两个有源元件表面贴装在插头 PCB（或桨板）上。热界面材料 (TIM) 放置在“ 热元件 ”和“ 散热材料 ”（如金属外壳）之间，以降低元件接头与周围环境之间的热阻。金属外壳有助于通过将热量分散到包覆成型表面来降低 T_S 并避免热点。

插头 PCB 和主板假定为基于 FR4 的材料。主板是一个块体模型，假定处于恒定温度，上面没有点热源。插座在单端口和水平堆叠盒中安装在主板顶部，如图 D-6 所示；在垂直堆叠盒中垂直安装，如图 D-4 和图 D-5 所示。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

D.2.3 Heat Sources

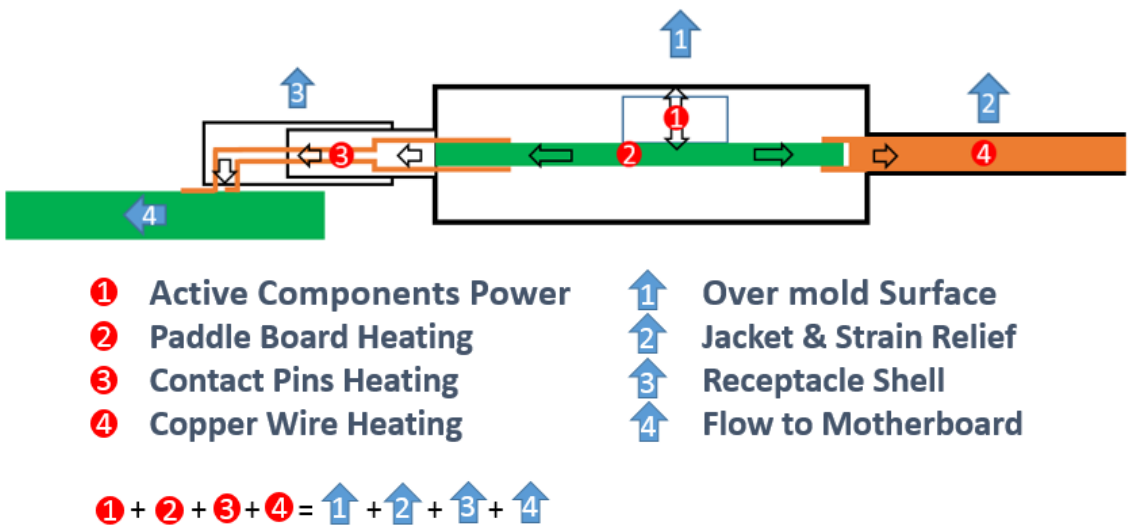
Main heat sources include:

- Active component power such as re-timer, voltage regulator, etc.; the overall power inside over-mold is P_O, which is about half of V_{CONN} power consumed by the full cable;
- Joule heat from the any conductor that carries high current, e.g. raw cable V_{BUS} and GND copper wire, the plug PCB copper traces, contact pins of connectors, etc.

D.2.4 Heat Flow

The main power sources and heat flow paths are illustrated in Figure D-3. The overall heat generated from the cable is mainly dissipated from over-mold surfaces, cable jacket and path to motherboard. The higher thermal resistance of one heat path, the more heat it will "push off" to other heat paths and the more risk that active component junction is overheated. Since heat flow to motherboard is not a desired path from the perspective of system design, cable and over-mold design are critical to achieve balanced heat dissipation paths so not to violate either T_S or T_J requirements.

Figure D-3 Heat Sources and Heat Flow Paths



The overall heat generated from the cable should be consistent with the overall power dissipated by the cable. An example of half a 1.0 m active cable consuming 1.5 W and sourcing 5 A V_{BUS} is shown below:

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

D.2.3 热源

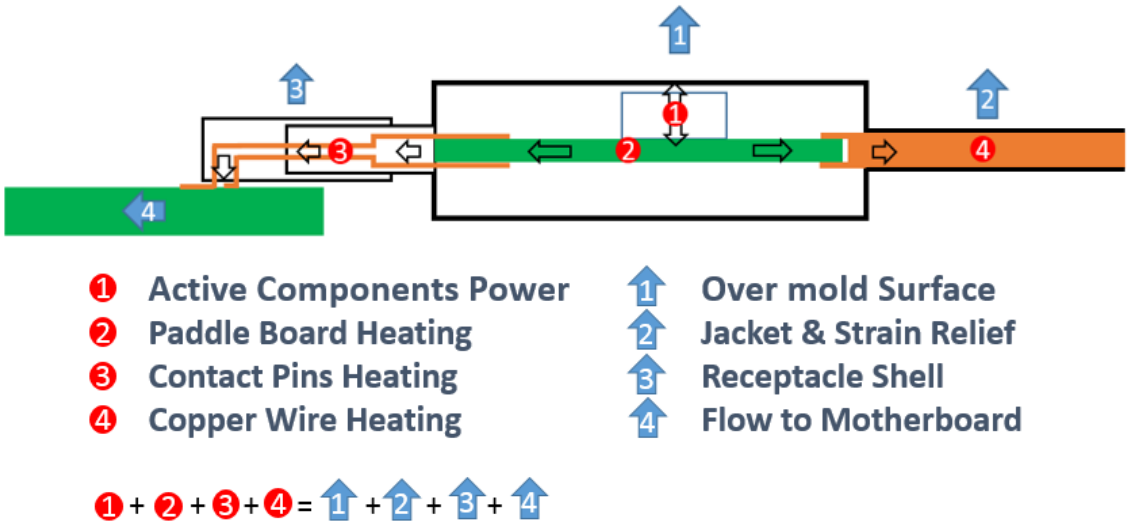
主要热源包括：

•有源元件功率，如重定时器、稳压器等；包覆成型内部的总功率为 P_0，约为整条电缆消耗的 VCONN 功率的一半；•来自任何承载大电流的导体的焦耳热，例如原始电缆 V BUS 和 GND 铜线、插头 PCB 铜线、连接器的接触针等。

D.2.4 热流

图 D-3 显示了主要电源和热流路径。电缆产生的总热量主要通过包覆成型表面、电缆护套和路径散发。
到主板。一条热路径的热阻越高，它“推向”其他热路径的热量就越多，有源元件结点过热的风险就越大。由于从系统设计的角度来看，热流到主板并不是理想的路径，因此电缆和包覆成型设计对于实现平衡的散热路径至关重要，这样才不会违反 T_S 或 T_J 要求。

图 D-3 热源和热流路径



电缆产生的总热量应与电缆耗散的总功率一致。下面显示了半根 1.0 米有源电缆的示例，其功耗为 1.5 W，提供 5 A VBUS：

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table D-1 Heat Sources and Heat Dissipation Example (1.5 W cable and 5 A)

(a) Heat Sources

Index	Heat Source	Power (W)
1	Active Components	0.750
2	Pin Heating	0.330
3	PCB Heating	0.135
4	Cable Heating	0.805
	Total Power Generation:	2.020

(b) Heat Dissipation

Index	Heat Source	Power (W)
1	Plug Surface	0.500
2	Cable & SR	1.120
3	Receptacle	0.050
4	Flow to Motherboard	0.350
	Total Power Dissipation:	2.020

D.3 USB 3.2 Single Lane Active Cable

Based on the assumption that VCONN power consumption is equally split between two ends of the cable and the 1 W maximum VCONN power dissipation in the USB Type-C active cable (See Table 4-5), active component power in each end or over-mold power (P_O) can go up to 0.5 W in a *USB 3.2* active cable.

D.3.1 USB 3.2 Single-Lane Active Cable Design Considerations

The active cable designer should design for T_S less than 30 °C above T_A in the condition where thermal boundary T_{MB} is of 25 °C above T_A per Section 5.5.4.

D.3.1.1 USB 3.2 Single-Lane Active Cable in a Single Port Configuration

An active cable connected to a single port in a host or device can take full advantage of the overall plug surface area for heat dissipation. Table D-2 shows that when P_O is 0.5 W, it is achievable to keep the plug over-mold surface temperature T_S of a single cable below the requirement, at both 3 A and 5 A VBUS, assuming the motherboard temperature is no higher than (T_A +25) °C.

Table D-2 USB 3.2 Active Cable Design Single Port Case Study at 35 °C Ambient and 60 °C Thermal Boundary (Single Lane)

	3 A VBUS	5 A VBUS
T_S (°C)	57	60

D.3.1.2 USB 3.2 Single-Lane Active Cable in a Multiple Port Configuration

When multi-port connector spacing is small, there is heat transfer between cables resulting in heat dissipation through natural convection being less effective than in the single port case. Radiation is also less effective due to the proximity of hot surfaces. This section lists a few typical 3-port configuration to show the impacts of receptacle spacing to the thermal

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 D-1 热源和散热示例（1.5 W 电缆和 5 A）

（一）热源

Index	Heat Source	Power (W)
1	Active Components	0.750
2	Pin Heating	0.330
3	PCB Heating	0.135
4	Cable Heating	0.805
	Total Power Generation:	2.020

(b)散热

Index	Heat Source	Power (W)
1	Plug Surface	0.500
2	Cable & SR	1.120
3	Receptacle	0.050
4	Flow to Motherboard	0.350
	Total Power Dissipation:	2.020

D.3 USB 3.2 单通道有源电缆

假设 VCONN 功耗在电缆两端均等分配，且 USB Type-C 有源电缆中 VCONN 最大功耗为 1W（见表 4-5），则 *USB 3.2* 有源电缆中每端的有源元件功率或包覆成型功率（P_O）可高达 0.5 W。

D.3.1 USB 3.2 单通道有源电缆设计注意事项

有源电缆设计人员应在以下条件下将 T_S 设计为比 T_A 高出 30 °C 以下
其中，根据第 5.5.4 节，热边界 T_{MB} 比 T_A 高 25 °C。

D.3.1.1 单端口配置中的 USB 3.2 单通道有源电缆

连接到主机或设备中单个端口的有源电缆可以充分利用整个插头表面积进行散热。表 D-2 显示，当 P_O 为 0.5 W 时，假设主板温度不高于 (T_A +25) °C，则可以将单个电缆的插头包覆成型表面温度 T_S 保持在要求以下，无论是 3 A 还是 5 A VBUS。

表 D-2 35 °C 环境温度下 USB 3.2 有源电缆设计单端口案例研究
和 60 °C 热边界条件（单通道）

	3 A VBUS	5 A VBUS
T_S (°C)	57	60

D.3.1.2 多端口配置中的 USB 3.2 单通道有源电缆

当多端口连接器间距较小时，电缆之间会发生热传递，导致通过自然对流散热的效果不如单端口情况。由于热表面的接近性，辐射效果也较差。本节列出了一些典型的 3 端口配置，以显示插座间距对热的影响

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

performance of an active cable. For Figure D-4 and Figure D-5 minimum spacing center to center is 7 mm; for Figure D-6 it is 12.85 mm.

Figure D-4 Vertically Stacked Horizontal Connectors 3x1 Configuration (VERT)

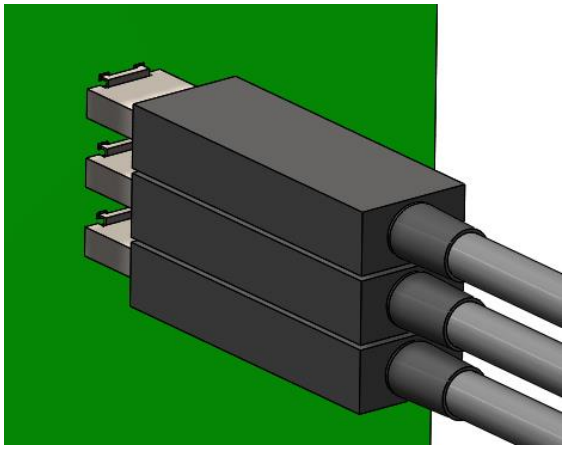


Figure D-5 Horizontally Stacked Vertical Connectors 1x3 Configuration (HZ90)

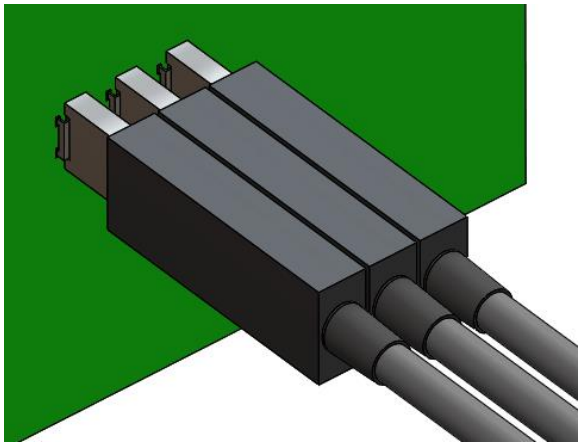
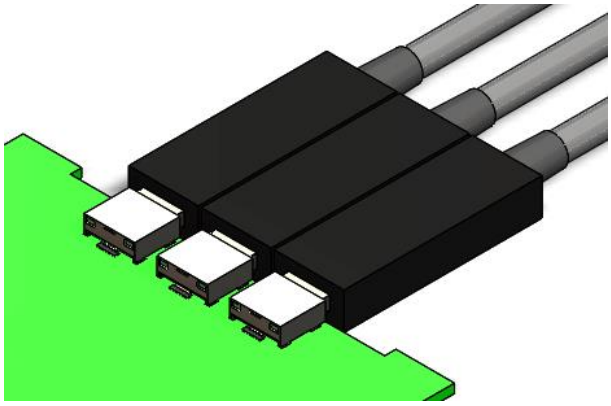


Figure D-6 Horizontally Stacked Horizontal Connector 1x3 Configuration (HORZ)



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

有源电缆的性能。对于图 D-4 和图 D-5，中心到中心的最小间距为 7 毫米；对于图 D-6，中心到中心的最小间距为 12.85 毫米。

图 D-4 垂直堆叠水平连接器 3x1 配置 (VERT)

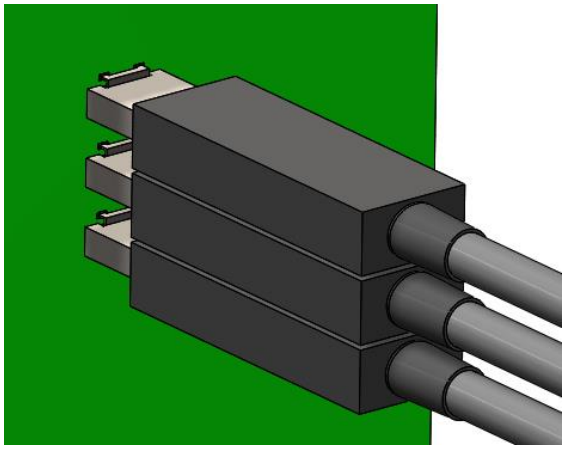


图 D-5 水平堆叠垂直连接器 1x3 配置 (HZ90)

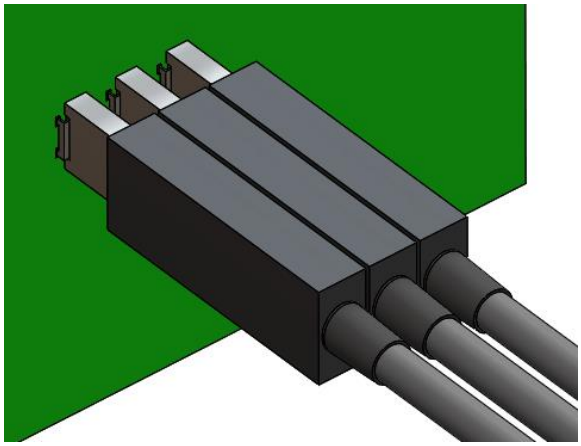
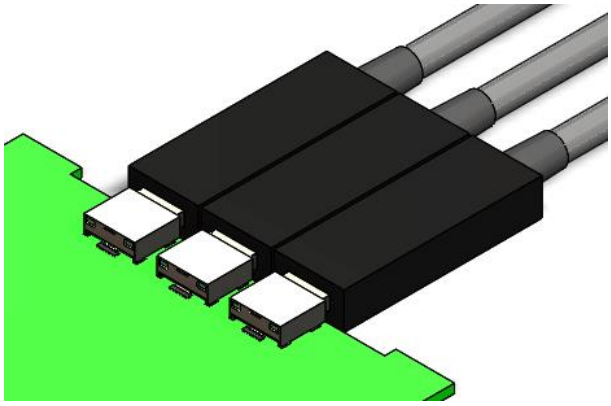


图 D-6 水平堆叠水平连接器 1x3 配置 (HORZ)



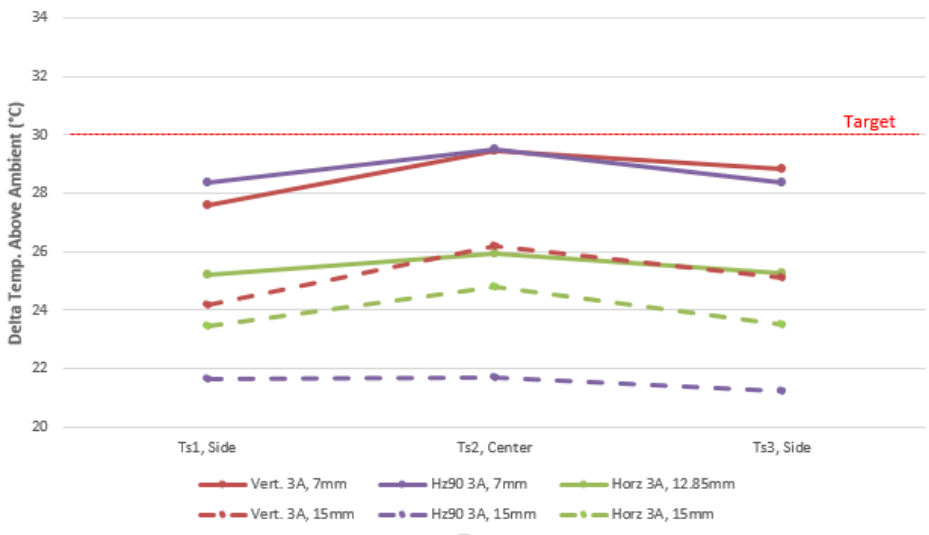
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

D.3.1.2.1 USB 3.2 Single-Lane 3A Active Cable in a 3-Port Configuration

When three active cables are stacked up, the port in the center position is usually in the worst situation for heat transfer. Figure D-7 shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three *USB 3.2* 3A cables are plugged on a 60 °C motherboard in 35°C ambient.

In all 3-port configurations shown in Figure D-4, Figure D-5, and Figure D-6, it is achievable to keep the all three plug over-mold surface temperature T_S below the requirement, at 3 A V_{BUS}, assuming the motherboard temperature is no higher than (T_A +25) °C. Specific cable design should be tested and validated because the margin of center port in VERT and HZ90 is less than 1 °C at minimum port spacing in thermal modeling.

Figure D-7 USB 3.2 Single-Lane 3A Active Cable in a 3-Port Configuration



D.3.1.2.2 USB 3.2 Single-Lane 5A Active Cable in a 3-Port Configuration

Figure D-8 shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three *USB 3.2* 5A cables are plugged on a 60 °C motherboard in 35 °C ambient.

All solid lines indicate the minimum spacing cases and dash lines the enlarged spacing cases. Center port is the worst case in all configurations. Three 5A cables at VERT and HZ90 configurations at minimum spacing could exceed the (T_A +30 °C) specification by up to 5 °C. HORZ configuration marginally meet spec on side ports but failed on center port.

Enlarging spacing between ports greatly reduce T_S. Especially in HZ90 configuration, spacing from 7 mm to 15 mm reduced T_S by about 8 °C.

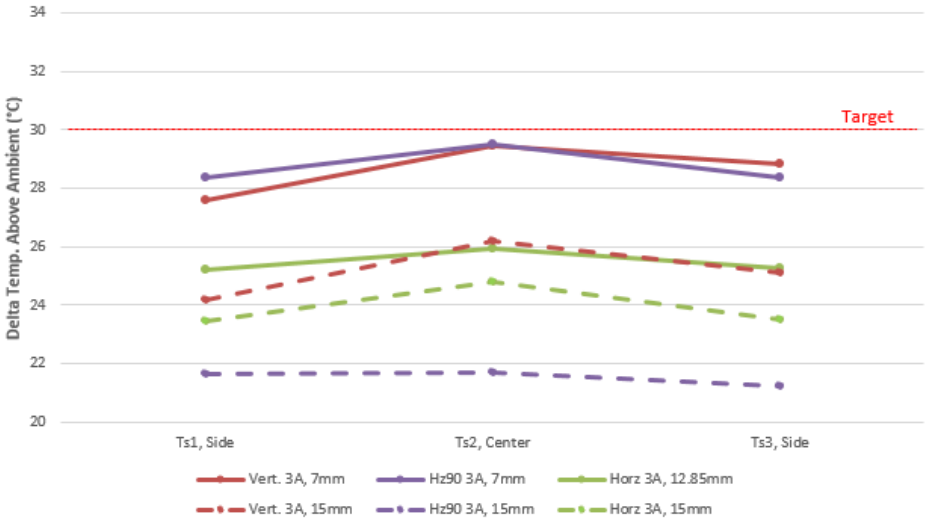
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

3.1.2.1 3 端口配置中的 USB 3.2 单通道 3A 有源电缆

当三条有源线缆堆叠在一起时，中心位置的端口通常处于最差的热传递情况。图 D-7 显示了当三条 *USB 3.2* 3A 线缆插在 60 °C 主板上且环境温度为 35°C 时，三个端口的最大包覆模表面温度 T_S 与环境温度 T_A 之间的温差。

在图 D-4、图 D-5 和图 D-6 所示的所有 3 端口配置中，假设主板温度不高于 (T_A +25) °C，则可将所有三个插头的模制表面温度 T_S 保持在要求以下。应测试和验证特定的电缆设计，因为在热建模中，VERT 和 HZ90 中的中心端口的裕度在最小端口间距处小于 1 °C。

图 D-7 3 端口配置中的 USB 3.2 单通道 3A 有源线缆



D.3.1.2.2 3 端口配置中的 USB 3.2 单通道 5A 有源电缆 配给

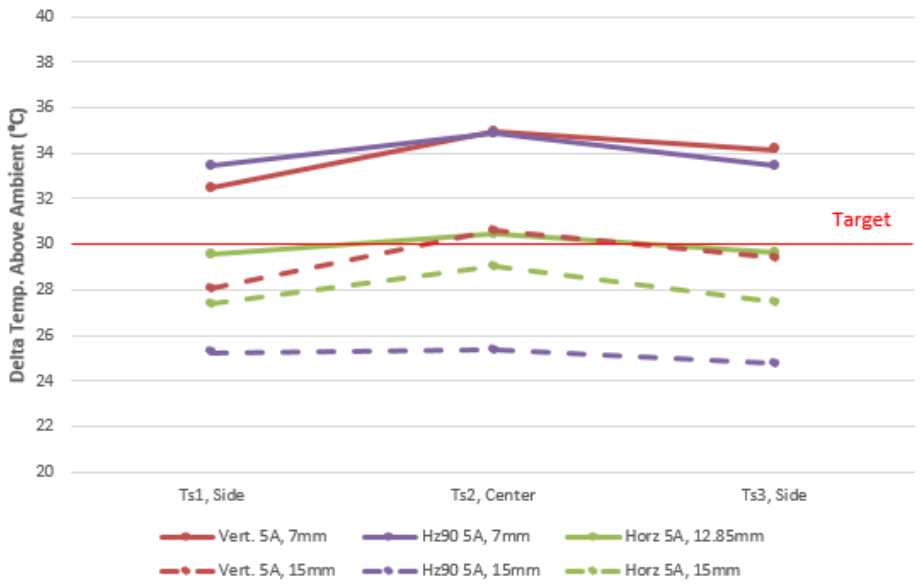
图 D-8 显示了在 35 °C 环境下，将三根 *USB 3.2* 5A 线缆插在 60 °C 的主板上时，三个端口的最大包覆成型表面温度 T_S 与环境温度 T_A 之间的温差。

所有实线表示最小间距情况，虚线表示扩大间距情况。
中心端口是所有配置中最糟糕的情况。VERT 和 HZ90 配置中最小间距的三根 5A 电缆可能会超过 (T_A +30 °C) 规格最高 5 °C。HORZ 配置在侧面端口上勉强符合规格，但在中心端口上不符合规格。

扩大端口间距可大大降低 T_S。特别是在 HZ90 配置中，间距从 7 毫米到 15 毫米可使 T_S 降低约 8 °C。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure D-8 USB 3.2 Single-Lane 5A Active Cable in a 3-Port Configuration



D.4 Dual-Lane Active Cables

USB 3.2 defines two lanes of SuperSpeed USB data and in dual-lane operation typically has higher active component power consumption than *USB 3.2* single-lane Gen2 active cables. Higher power could heat up the over-mold and raise T_S above user comfort zone when plugging or unplugging the cable.

USB 3.2 dual-lane active cable may consume up to 1.5 W of power from V_{CONN}. This compares with the 1 W allowed for *USB 3.2* single-lane active cables.

Section D.4.1 shows T_S resulting from 0.75 W over-mold power P_O in a 1.5 W dual-lane *USB 3.2* active cable for a certain design, in both single-port and multiple-port configurations. Results reveals that thermal solution is necessary to meeting cable design requirements especially in multiple-port configuration.

Both over-mold power P_O and thermal boundary of the cable T_{MB} have impacts on T_S. The correlation of three are studied in Section D.4.1.2 which helps system and cable designer to take both factors into consideration.

D.4.1 USB 3.2 Dual-Lane Active Cable Design Considerations

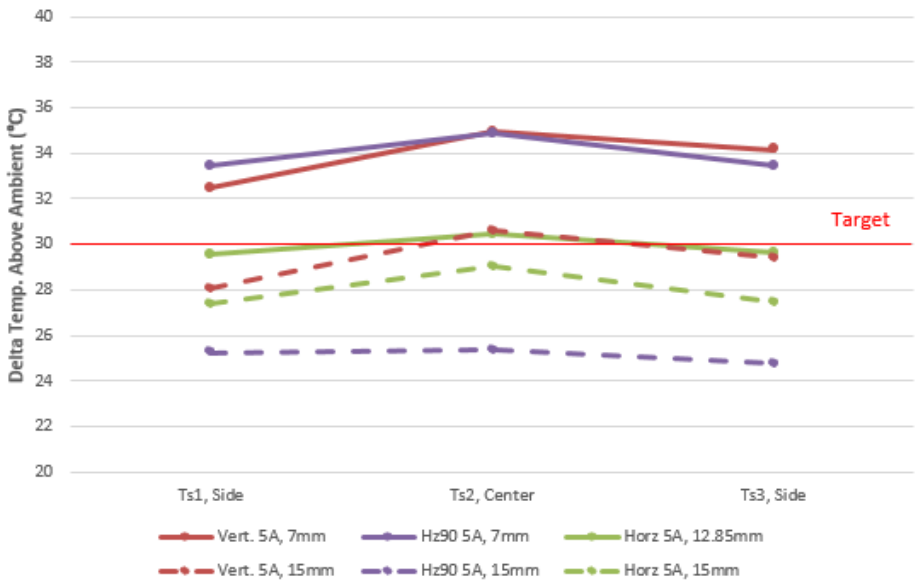
The cable designer should design for T_S of the over-mold less than 30 °C above T_A in the condition where thermal boundary T_{MB} is of 25 °C above T_A per Section 5.5.4.

D.4.1.1 USB 3.2 Dual-Lane Active Cable in a Single Port Configuration

An active cable connected to a single port in a host or device can take full advantage of the overall plug surface area for heat dissipation. Table D-3 shows that when P_O is 0.75 W, it is achievable to keep the plug over-mold surface temperature T_S of a single cable below (T_A +30) °C at both 3 A and 5 A V_{BUS}, assuming the motherboard temperature is no higher than (T_A +25) °C.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 D-8 3 端口配置中的 USB 3.2 单通道 5A 有源线缆



D.4 双通道有源电缆

USB 3.2 定义了两个 SuperSpeed USB 数据通道，在双通道操作中，有源组件功耗通常高于 *USB 3.2* 单通道 Gen2 有源电缆。更高的功率可能会加热包覆成型件，并在插入或拔出电缆时使 T_S 高于用户舒适区。

USB 3.2 双通道有源电缆可能从 V CONN 消耗高达 1.5 W 的功率。相比之下，*USB 3.2* 单通道有源电缆允许的功率为 1 W。

D.4.1 节显示了在单端口和多端口配置中，1.5 W 双通道 *USB 3.2* 有源电缆中 0.75 W 包覆成型功率 P_O 产生的 T_S。结果表明，热解决方案对于满足电缆设计要求是必要的，尤其是在多端口配置中。

包覆成型功率 P_O 和电缆热边界 T_{MB} 都会对 T_S 产生影响。第 D.4.1.2 节研究了三者的相关性，这有助于系统和电缆设计人员同时考虑这两个因素。

D.4.1 USB 3.2 双通道有源电缆设计注意事项

电缆设计人员应根据第 5.5.4 节的规定，在热边界 T_{MB} 高出 T_A 25°C 的条件下，将包覆成型的 T_S 设计为高出 T_A 不超过 30°C。

D.4.1.1 单端口配置中的 USB 3.2 双通道有源电缆

连接到主机或设备中单个端口的有源电缆可以充分利用整个插头表面积进行散热。表 D-3 显示，当 P_O 为 0.75 W 时，假设主板温度不高于 (T_A +25) °C，则在 3 A 和 5 A VBUS 下，都可以将单根电缆的插头包覆成型表面温度 T_S 保持在 (T_A +30) °C 以下。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table D-3 USB 3.2 Active Cable Design Single Port Case Study at 35 °C Ambient and 60 °C Thermal Boundary (Dual Lane)

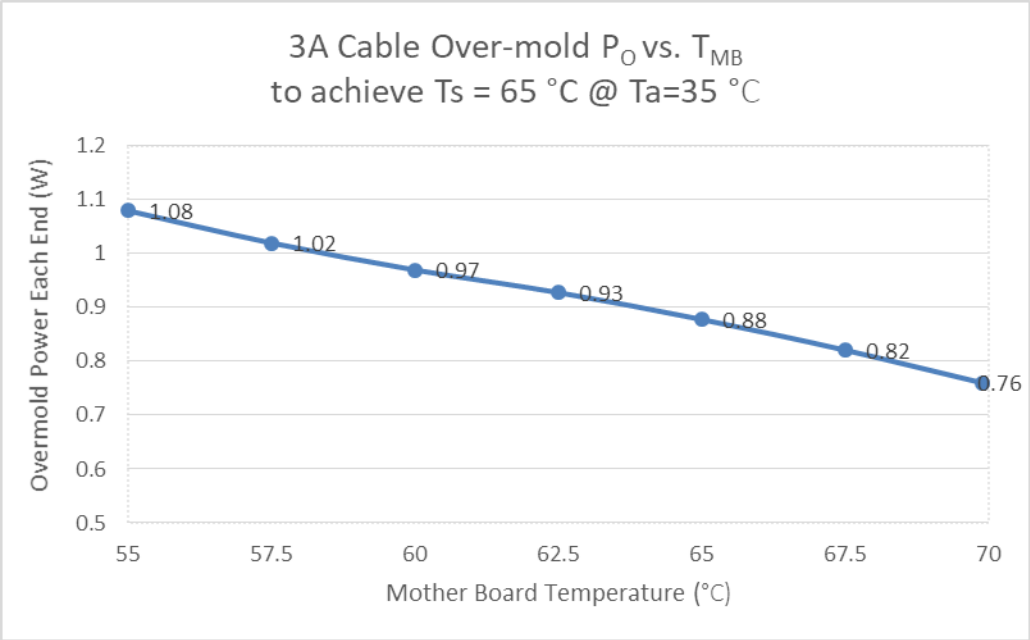
	3 A VBUS	5 A VBUS
T_S (°C)	61	64

In 5 A VBUS case, T_S is much closer to specified limit than 3 A VBUS case (Section D.3.1.1), so test and verification of thermal design is highly recommended.

D.4.1.2 Impact of Over-mold Power P_O and Thermal Boundary Temperature T_{MB}

In Figure D-9, the area under graph indicate the combination of over-mold power P_O and thermal boundary temperature T_{MB} that can achieve $T_S < (T_A + 30)$ °C in a single port configuration in a 3 A VBUS application.

Figure D-9 Impact of Over-mold Power P_O and Thermal Boundary Temperature T_{MB} at 3 A VBUS in a Single Port Configuration



In Figure D-10, the area under graph indicate the combination of over-mold power P_O and thermal boundary temperature T_{MB} that can achieve $T_S < (T_A + 30)$ °C in a single port configuration in a 5 A VBUS application.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 D-3 35 °C 环境温度下 USB 3.2 有源电缆设计单端口案例研究
和 60 °C 热边界（双通道）

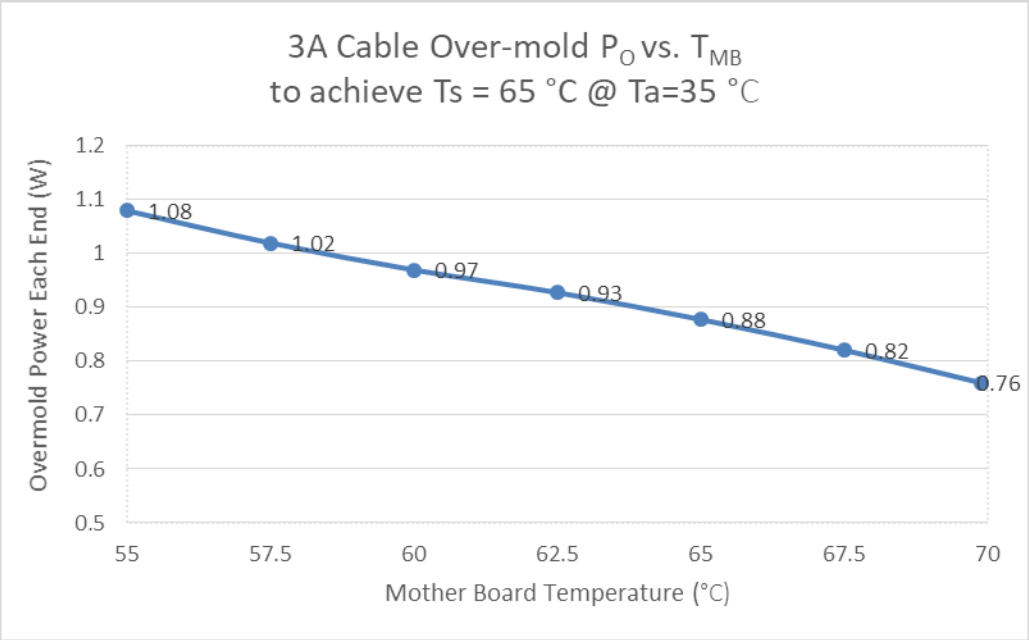
	3 A VBUS	5 A VBUS
T_S (°C)	61	64

在 5 A VBUS 情况下，T_S 比 3 A VBUS 情况（第 D.3.1.1 节）更接近规定限值，因此强烈建议进行热设计测试和验证。

D.4.1.2 影响 包覆成型功率 P_O 和热边界温度 重新 T_{MB}

在图 D-9 中，图形下方的区域表示在 3 A VBUS 应用中的单端口配置中可以实现 $T_S < (T_A + 30)$ °C 的包覆成型功率 P_O 和热边界温度 T_{MB} 的组合。

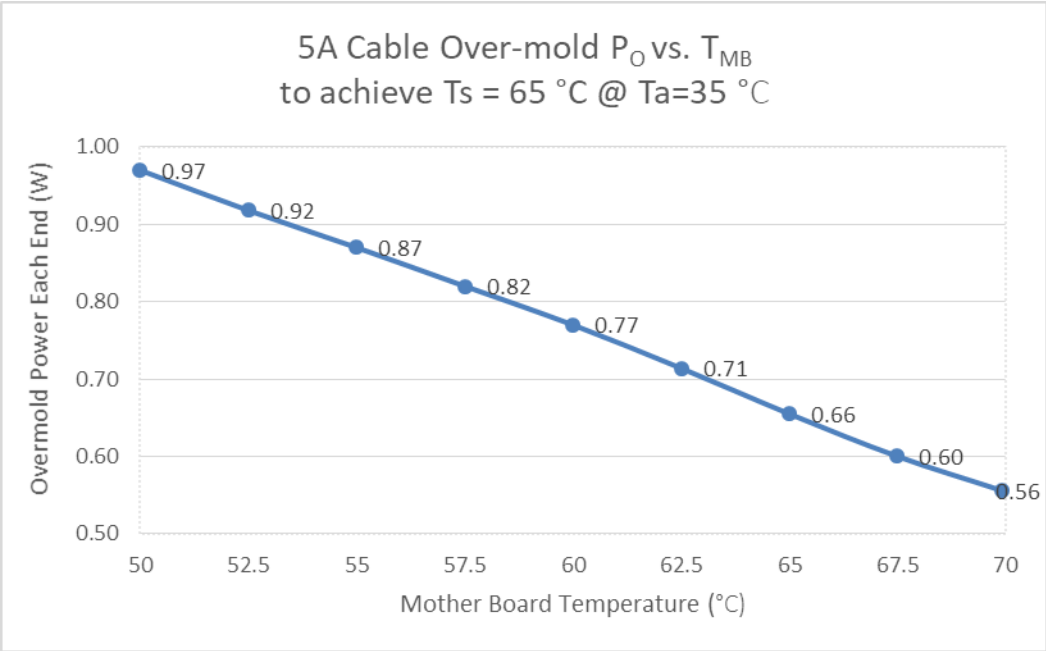
图 D-9 单端口配置中 3 A VBUS 下包覆成型功率 P_O 和热边界温度 T_{MB} 的影响



在图 D-10 中，图形下方的区域表示在 5 A VBUS 应用中的单端口配置中可以达到 $T_S < (T_A + 30)$ °C 的包覆成型功率 P_O 和热边界温度 T_{MB} 的组合。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure D-10 Impact of Over-mold Power P_O and Thermal Boundary Temperature T_{MB} at 5 A V_{BUS} in a Single Port Configuration



D.4.1.3 Dongle Cable

When overall active component power is higher than the maximum over-mold power P_O that could meet T_S requirement, cable may be re-designed to move the thermal load away from the USB Type-C plug over-mold such as in a dongle cable as illustrated in Figure D-11.

Figure D-11 USB 3.2 Active Cable Dongle Design (One End Shown)

The cable should be designed so that the over-mold directly plugged in the host or device dissipates no more than maximum P_O and extra heat is migrated to another part of the cable such as a dongle, so neither extra heat will flow into host and device, nor over-mold surface temperature is too hot for users to touch.

D.4.2 USB 3.2 Dual-Lane Active Cable in a Multi-Port Configuration

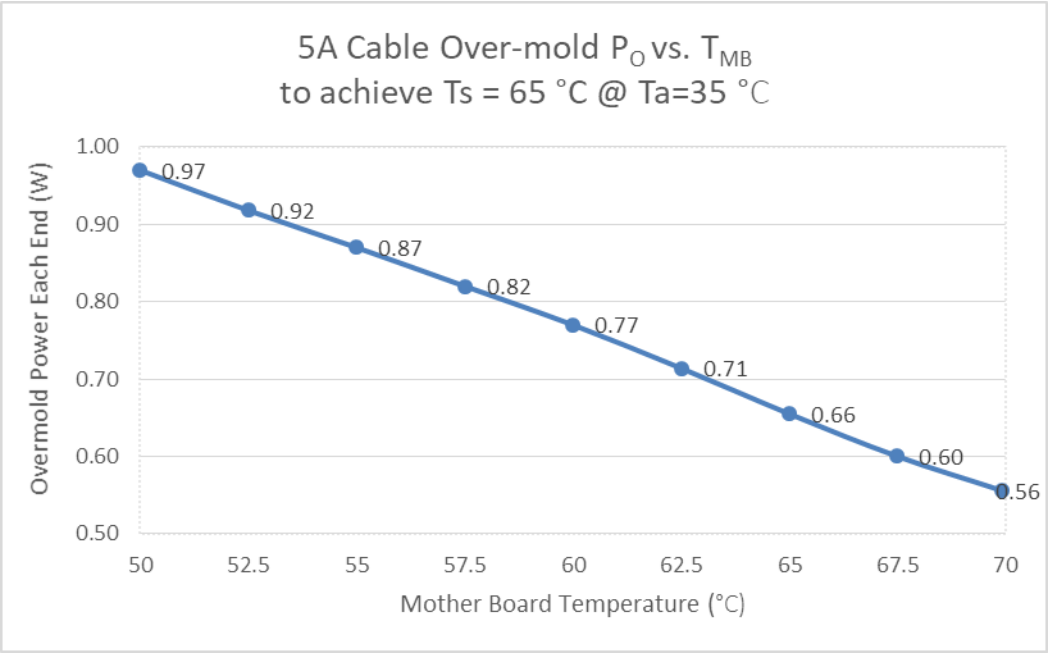
Multi-port connector spacing results in less effective heat dissipation by natural convection and radiation. This section lists a few typical 3-port configuration to show the impacts of receptacle spacing to the thermal performance of *USB 3.2* active cables. Naming of configurations used in this section are the same as in Section D.3.1.2.

D.4.2.1 USB 3.2 Dual-Lane 3A Active Cable in a 3-Port Configuration

Figure D-12 shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three *USB 3.2* dual-lane 3A V_{BUS} and 1.5 W cables are plugged on a 60 °C motherboard in 35 °C ambient. The port in the center position is usually in the worst situation for heat transfer.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 D-10 单端口配置中 5 A VBUS 下包覆成型功率 P_O 和热边界温度 T_{MB} 的影响



D.4.1.3 加密狗电缆

当整体有源组件功率高于可满足 T_S 要求的最大包覆功率 P_O 时，可以重新设计电缆，以将热负荷从 USB Type-C 插头包覆成型移开，例如加密狗电缆，如图 D-11 所示。

图 D-11 USB 3.2 有源电缆适配器设计（显示一端）

电缆的设计应使得直接插入主机或设备的包覆成型件散发的热量不超过最大 P_O，并且多余的热量被迁移到电缆的另一部分（例如加密狗），因此多余的热量既不会流入主机和设备，包覆成型件的表面温度也不会太高而导致用户无法触摸。

D.4.2 多端口配置中的 USB 3.2 双通道有源电缆

多端口连接器间距会导致自然对流和辐射散热效果较差。本节列出了几种典型的 3 端口配置，以显示插座间距对 *USB 3.2* 有源电缆热性能的影响。本节中使用的配置命名与第 D.3.1.2 节中的相同。

D.4.2.1 3 端口配置中的 USB 3.2 双通道 3A 有源电缆

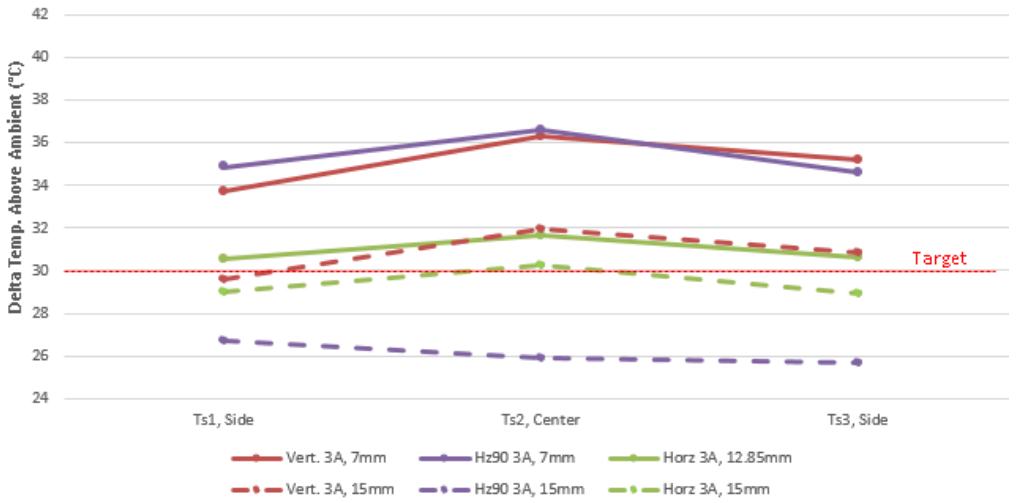
图 D-12 显示了当三条 *USB 3.2* 双通道 3A VBUS 和 1.5 W 电缆在 35 °C 环境下插入 60 °C 主板时，三个端口的最大包覆模表面温度 T_S 与环境温度 T_A 之间的温差。中心位置的端口通常处于最差的热传递情况。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

All solid lines indicate the minimum spacing cases and dash lines the enlarged spacing cases. Center port is the worst case in all configurations. T_S of center port in VERT and HZ90 configurations at minimum spacing could be more than 6 °C over the (T_A +30 °C) specification and in HORZ configuration about 2 °C over specification.

Enlarging spacing between ports could greatly reduce T_S. Especially in HZ90 configuration, spacing from 7 mm to 15 mm reduced T_S by about 11 °C, which help to reduce T_S to meet specification.

Figure D-12 USB 3.2 Dual-Lane 3A Active Cable in a 3-Port Configuration



D.4.2.2 USB 3.2 Dual-Lane 5A Active Cable in a 3-Port Configuration

Figure D-13 shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three USB 3.2 dual-lane 5 A V_{BUS} and 1.5 W cables are plugged on a 60 °C motherboard in 35 °C ambient. The T_S port in the center position is still the highest of all three in all cases.

In all 3-port configurations listed in Figure D-4, Figure D-5, and Figure D-6, plug over-mold surface temperature T_S of all three ports have exceeded the requirement, at 5 A V_{BUS}, assuming the motherboard temperature is at (T_A +25) °C. T_S of center port in VERT and HZ90 configurations at minimum spacing are the highest, near 12 °C over the (T_A +30 °C) specification and in HORZ configuration about 6 °C over specification.

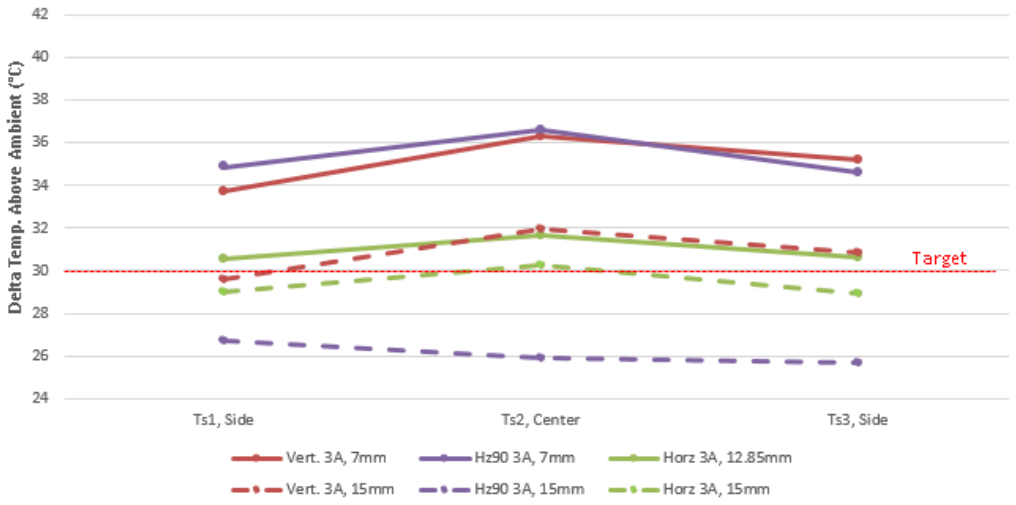
Enlarging spacing between ports could help reduce T_S. The largest reduction is seen in HZ90 configuration, which is near 12 °C and it brings T_S back close to target, when spacing is enlarged from 7 mm to 15 mm. However, when port spacing is not sufficient to bring T_S down to desired range, further design options in cable and host/device should be investigated.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

所有实线表示最小间距情况，虚线表示扩大间距情况。
中心端口是所有配置中最差的情况。在最小间距下，VERT 和 HZ90 配置中的中心端口 T_S 可能比 (T_A +30 °C) 规格高出 6 °C 以上，而在 HORZ 配置中则比规格高出约 2 °C。

扩大端口间距可以大大降低 T_S。特别是在 HZ90 配置中，间距从 7 毫米到 15 毫米可使 T_S 降低约 11 °C，这有助于降低 T_S 以满足规格。

图 D-12 3 端口配置中的 USB 3.2 双通道 3A 有源线缆



D.4.2.2 3 端口配置中的 USB 3.2 双通道 5A 有源线缆

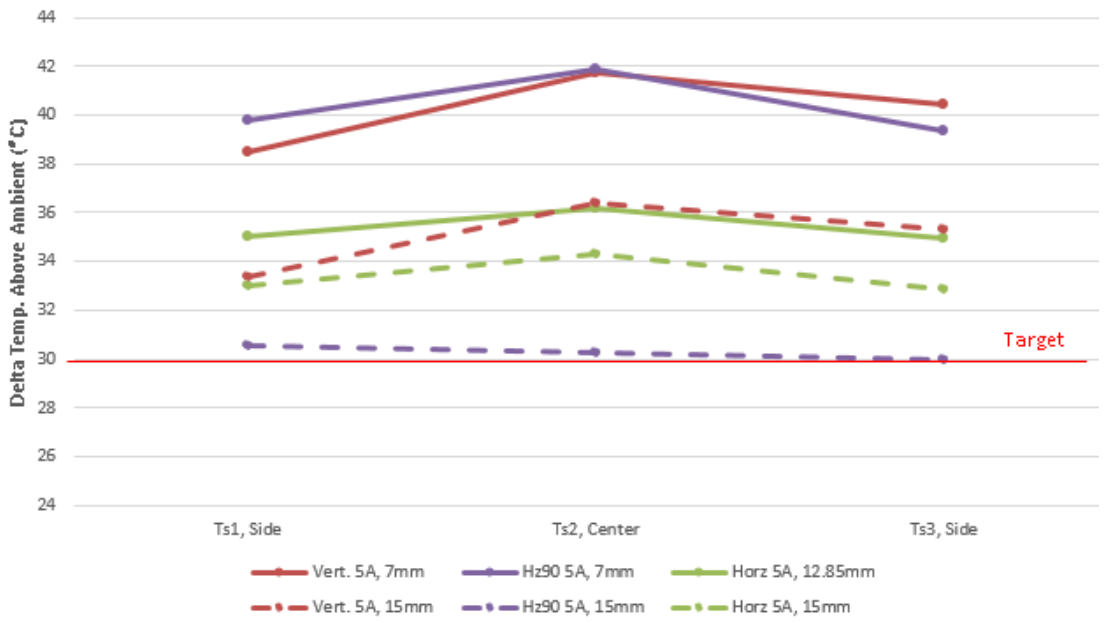
图 D-13 显示了在 35 °C 环境温度下将三条 USB 3.2 双通道 5 A VBUS 和 1.5 W 线缆插入 60 °C 主板时，三个端口的最大包覆成型表面温度 T_S 与环境温度 T_A 之间的温差。在所有情况下，中间位置的 T_S 端口仍然是三个端口中温度最高的。

在图 D-4、图 D-5 和图 D-6 列出的所有 3 端口配置中，所有三个端口的插头包覆成型表面温度 T_S 都已超过要求，在 5 A V BUS 时，假设主板温度为 (T_A +25) °C。最小间距的 VERT 和 HZ90 配置中的中心端口的 T_S 最高，比 (T_A +30 °C) 规格高出近 12 °C，而 HORZ 配置中的中心端口的 T_S 比规格高出约 6 °C。

扩大端口间距有助于降低 T_S。最大降幅出现在 HZ90 配置中，接近 12 °C，当间距从 7 毫米扩大到 15 毫米时，它使 T_S 回到接近目标值。但是，当端口间距不足以将 T_S 降至所需范围时，应研究电缆和主机/设备的进一步设计选项。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure D-13 USB 3.2 Dual-Lane 5A Active Cable in a 3-Port Configuration



D.5 USB 3.2 Host and Device Design Considerations

Multi-port *USB 3.2* systems should follow the connector minimum spacing requirement defined in Section 3.10.2.

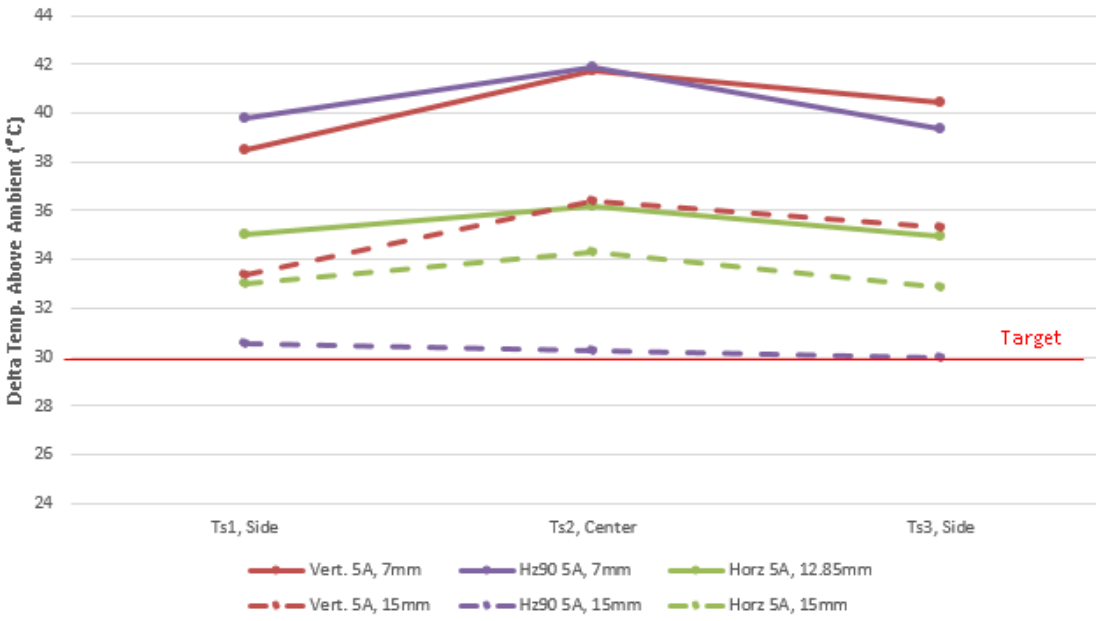
From heat flow schematics (Section D.2.4), when flow path 1 (over-mold surface dissipation) is less effective due to the limited spacing between cables, more heat would flow to motherboard and cable. It is recommended that system designer evaluate the heat flow to the system in a system level thermal analysis and provide a heat solution at the system level to reduce the motherboard temperature at these ports if necessary.

D.5.1 Heat Spreading or Heat Sinking from Host or Device

Proper thermal solutions may be needed on host or device to meet cable thermal requirements. Below are examples of placement of thermal interface material on host or device USB Type-C receptacle connector to spread heat or conduct heat away from chassis. This is to help either direct heat away from active components inside cable plug or limit amount of heat from flowing from host or device into the cable plug. Both would prevent the increased junction temperature of active components and increased cable plug surface temperature over the finger touch temperature limit. The heat management solution shown below are not limited to certain type or size.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 D-13 3 端口配置中的 USB 3.2 双通道 5A 有源线缆



D.5 USB 3.2 主机和设备设计注意事项

多端口 *USB 3.2 系统*应遵循第 3.10.2 节中定义的连接器最小间距要求。

从热流示意图（第 D.2.4 节）可知，当流道 1（过模表面耗散）
由于电缆之间的间距有限，效率会降低，更多的热量会流向主板和电缆。建议系统设计师在系统级热分析中评估系统的热流，并在系统级提供散热解决方案，以降低这些端口处的主板温度（如有必要）。

D.5.1 主机或设备的散热或散热

主机或设备可能需要适当的散热解决方案来满足电缆散热要求。以下是在主机或设备 USB Type-C 插座连接器上放置热界面材料的示例，用于散热或将热量传导出底盘。这有助于将热量从电缆插头内的有源组件中导出，或限制从主机或设备流入电缆插头的热量。两者都可以防止有源组件的结温升高和电缆插头表面温度升高超过手指触摸温度限制。下面显示的散热管理解决方案不限于特定类型或尺寸。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure D-14 Example: Additional Heat Spreader on Receptacle in Host or Device

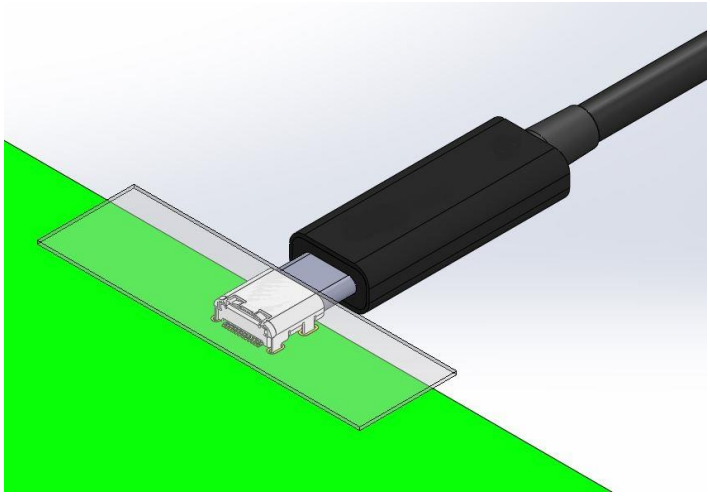
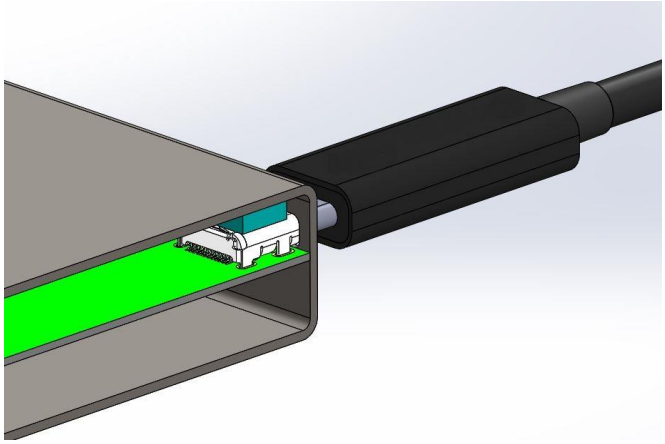


Figure D-15 Example: Heat Sinking by Chassis of Host or Device



D.5.2 Motherboard Temperature Control

Motherboard as a thermal boundary for the cable, could impact the thermal performance of cable greatly. Lowered mother temperature especially the area local around the receptacles could help reduce plug surface temperature T_S and component junction temperature T_J. See more discussion in Section D.4.1.1.

D.5.3 Wider Port Spacing for Multi-Port Applications

Wider spacing between receptacle connectors, especially when no additional heat sinking is available, is recommended for multiport application. Section D.3.1.2.1 and section D.3.1.2.2 show the impact from adjustment of port spacing.

D.5.4 Power Policies

To be added in a future update.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 D-14 示例：主机或设备插座上的附加散热器

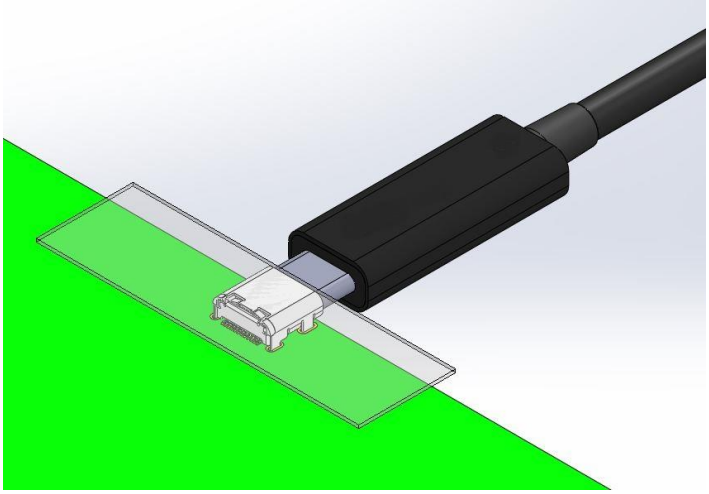
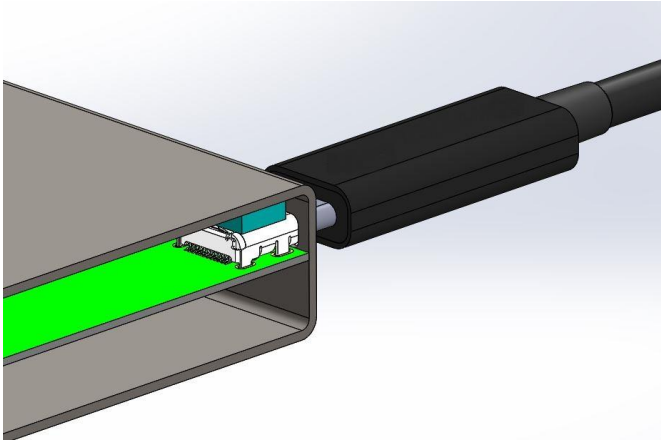


图 D-15 示例：主机或设备底盘散热



D.5.2 主板温度控制

主板作为电缆的热边界，会极大地影响电缆的热性能。降低主板温度，尤其是插座周围局部区域的温度，有助于降低插头表面温度 T_S 和组件结温 T_J。请参阅第 D.4.1.1 节中的更多讨论。

D.5.3 更宽的端口间距，适用于多端口应用

对于多端口应用，建议插座连接器之间的间距更大，尤其是在没有额外散热器的情况下。第 D.3.1.2.1 节和第 D.3.1.2.2 节显示了调整端口间距的影响。

D.5.4 电源策略

将在未来的更新中添加。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

E Alternate Modes

All hosts and devices (except chargers and clearly marked charge-through ports) using a USB Type-C® receptacle shall expose a USB interface (minimally *USB 2.0*). In the case where the host or device optionally supports Alternate Modes:

- The host and device shall use *USB Power Delivery* Structured Vendor Defined Messages (Structured VDMs) to discover, configure and enter/exit modes to enable Alternate Modes.
- The device is strongly encouraged to provide equivalent USB functionality where such exists for best user experience.
- Where no equivalent USB functionality is implemented, the device shall provide a USB interface exposing a *USB Billboard Device Class* used to provide information needed to identify the device. A device is not required to provide a USB interface exposing a *USB Billboard Device Class* for non-user facing modes (e.g., diagnostic modes).

As Alternate Modes do not traverse the USB hub topology, they shall only be used between a host connected directly to a device.

There are Alternate Mode devices that look like a USB hub – the downstream facing ports of such devices are USB Type-C receptacles that support Alternate Modes. These devices are referred to as Alternate Mode expanders:

- The Alternate Mode port expander's downstream facing USB Type-C receptacles shall expose a USB 2.0 interface.

An Alternate Mode port expander with the capability to pass SuperSpeed USB through its upstream facing port should expose SuperSpeed USB on its downstream facing USB Type-C receptacles.

E.1 Alternate Mode Architecture

The *USB Power Delivery* Structured VDMs are defined to extend the functionality a device exposes. Only Structured VDMs shall be used to alter the USB functionality or reconfigure the pins the USB Type-C Connector exposes. Structured VDMs provide a standard method to identify the modes a device supports and to command the device to enter and exit a mode. The use of Structured VDMs are in addition to the normal *USB PD* messages used to manage power. Structured VDMs may be interspersed within the normal *USB PD* messaging stream, however they shall not be inserted in the middle of an ongoing PD power negotiation.

The Structured VDMs consist of a request followed by a response. The response is either a successful completion of the request (ACK), an indication that the device needs time before it can service a request (BUSY), or a rejection of the request (NAK). A host and device do not enter a mode when either a NAK or BUSY is returned.

Multiple modes may exist and/or function concurrently. For example, a Structured VDM may be used to manage an active cable at the same time that another Structured VDM is used to manage the device so that both the cable and device are operating in a compatible mode.

E.2 Alternate Mode Requirements

The host and device shall negotiate a *USB PD* Explicit Contract before Structured VDMs may be used to discover or enter an Alternate Mode.

The ACK shall be sent after switching to the Alternate Mode has been completed by the UFP for Enter Mode and Exit Mode requests. See Section 6.4.4 in the *USB Power Delivery Specification*.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

E 替代模式

所有使用 USB Type-C® 插座的主机和设备（充电器和明确标记的充电端口除外）都应暴露 USB 接口（最低为 *USB 2.0*）。如果主机或设备选择性地支持替代模式：

- 主机和设备应使用 *USB Power Delivery* 结构化供应商定义消息 (Structured VDMs) 来发现、配置和进入/退出模式，以启用
  替代模式。• 强烈建议设备提供等效的 USB 功能（如果存在），以获得最佳用户体验。
- 如果未实现等效的 USB 功能，设备应提供 USB 接口，以公开 *USB Billboard Device Class*，用于提供识别设备所需的信息。设备无需为非面向用户的模式（例如诊断模式）提供公开 *USB Billboard Device Class* 的 USB 接口。

由于备用模式不跨越 USB 集线器拓扑，因此它们只能在
主机直接连接到设备。

有些备用模式设备看起来像 USB 集线器 - 此类设备的下游端口是支持备用模式的 USB Type-C 插座。这些设备称为备用模式扩展器：

- 备用模式端口扩展器的下游 USB Type-C 插座应暴露 USB 2.0 接口。

具有通过其上游端口传输超高速 USB 功能的备用模式端口扩展器应该在其下游 USB Type-C 插座上暴露超高速 USB。

E.1 备用模式架构

USB Power Delivery 结构化 VDM 被定义为扩展设备公开的功能。只有结构化 VDM 才可用于更改 USB 功能或重新配置 USB Type-C 连接器公开的引脚。结构化 VDM 提供了一种标准方法来识别设备支持的模式并命令设备进入和退出模式。结构化 VDM 的使用是对用于管理电源的正常 *USB PD* 消息的补充。结构化 VDM 可以散布在正常的 *USB PD* 消息流中，但它们不得插入正在进行的 PD 电源协商的中间。

结构化 VDM 由请求和响应组成。响应要么是请求成功完成 (ACK)，要么是设备需要时间才能处理请求 (BUSY)，要么是拒绝请求 (NAK)。当返回 NAK 或 BUSY 时，主机和设备不会进入模式。

多种模式可能同时存在和/或起作用。例如，结构化 VDM 可用于管理活动电缆，同时另一个结构化 VDM 可用于管理设备，以便电缆和设备都以兼容模式运行。

E.2 替代模式要求

在使用结构化 VDM 发现或进入替代模式之前，主机和设备应协商 *USB PD* 显式合同。

对于进入模式和退出模式请求，UFP 完成切换到备用模式后应发送 ACK。请参阅
USB Power Delivery Specification 中的第 6.4.4 节。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

If a device fails to successfully enter an Alternate Mode within tAMETimeout then the device shall minimally expose a *USB 2.0* interface (*USB Billboard Device Class*) that is powered by VBUS. If the device additionally supports *USB4*, then the device should defer exposing a *USB 2.0* interface (*USB Billboard Device Class*) due to an Alternate Mode timeout until the *USB4* discovery and entry process has completed (See Section 5.2.2).

When a device offers multiple modes, especially where multiple Alternate Mode definitions are needed in order to be compatible with multiple host-side implementations, successfully entering an Alternate Mode may be predicated on only one of the available modes being successfully recognized by a host. In this case, the device is not required to expose but may still expose a *USB Billboard Device Class* interface to indicate to the host the availability and status of the modes it supports.

The host may send an Enter Mode after tAMETimeout. If the device enters the mode, it shall respond with an ACK and discontinue exposing the *USB Billboard Device Class* interface. The device may expose the *USB Billboard Device Class* interface again with updated capabilities.

The current supplied over VCONN may be redefined by a specific Alternate Mode but the power shall not exceed the current rating of the pin (See Section 3.7.8.4).

E.2.1 Alternate Mode Pin Reassignment

Figure E-1 illustrates the only pins that shall be available for functional reconfiguration in a full-featured cable. The pins highlighted in yellow are the only pins that shall be reconfigured.

Figure E-1 Pins Available for Reconfiguration over the Full-Featured Cable

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

Figure E-2 illustrates the only pins that shall be available for functional reconfiguration in direct connect applications such as a cradle dock, captive cable or a detachable notebook. The pins highlighted in yellow are the only pins that shall be reconfigured. Five additional pins are available because this configuration is not limited by the cable wiring.

Figure E-2 Pins Available for Reconfiguration for Direct Connect Applications

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

The *USB 2.0* data pins (A6, A7) shall remain connected to the USB host controller during entry, while in and during exit of an Alternate Mode except in the case of a direct connect application that remaps A6 and A7. Direct connect applications that remap A6 and A7 through the use of an Alternate Mode shall provide a USB Billboard Class device that is presented if the remapped Alternate Mode is not entered within tAMETimeout.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

如果设备未能在 tAMETimeout 内成功进入备用模式，则设备应至少公开由 VBUS 供电的 *USB 2.0* 接口 (*USB Billboard Device Class*)。如果设备还支持 *USB4*，则设备应由于备用模式超时而推迟公开 *USB 2.0* 接口 (*USB Billboard Device Class*)，直到 *USB4* 发现和进入过程完成（参见第 5.2.2 节）。

当设备提供多种模式时，尤其是需要多个备用模式定义才能与多个主机端实现兼容时，成功进入备用模式可能取决于主机成功识别出其中一种可用模式。在这种情况下，设备不需要公开但仍可以公开 *USB Billboard Device Class* 接口，以向主机指示其支持的模式的可用性和状态。

主机可以在 tAMETimeout 之后发送进入模式。如果设备进入该模式，它将以 ACK 做出响应并停止公开 *USB Billboard Device Class* 接口。设备可以再次公开具有更新功能的 *USB Billboard Device Class* 接口。

通过 VCONN 提供的电流可以通过特定的替代模式重新定义，但功率不得超过引脚的电流额定值（参见第 3.7.8.4 节）。

E.2.1 备用模式引脚重新分配

图 E-1 显示了全功能电缆中唯一可用于功能重新配置的引脚。黄色突出显示的引脚是唯一应重新配置的引脚。

图 E-1 可通过全功能电缆重新配置的引脚

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

图 E-2 显示了在直接连接应用（例如底座、固定电缆或可拆卸笔记本电脑）中唯一可用于功能重新配置的引脚。黄色突出显示的引脚是唯一应重新配置的引脚。由于此配置不受电缆布线的限制，因此还有五个额外的引脚可用。

图 E-2 可用于直接连接应用重新配置的引脚

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

在进入、处于和退出备用模式期间，*USB 2.0* 数据引脚（A6、A7）应保持与 USB 主机控制器的连接，但重新映射 A6 和 A7 的直接连接应用程序除外。通过使用备用模式重新映射 A6 和 A7 的直接连接应用程序应提供 USB Billboard Class 设备，如果未在 tAMETimeout 内进入重新映射的备用模式，则将显示该设备。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

E.2.2 Alternate Mode Electrical Requirements

Signaling during the use of Alternate Modes shall comply with all relevant cable assembly, adapter assembly and electrical requirements of Chapter 3.

Several requirements are specified in order to minimize risk of damage to the SuperSpeed USB transmitters and receivers in a USB host or device when operating in an Alternate Mode:

- If pin pairs B11, B10 (RX1) and A11, A10 (RX2) are used on a captive cable, they shall be AC coupled either before or in the USB Type-C plug.
- If pin pairs B11, B10 (RX1) and A11, A10 (RX2) are used on a USB Type-C receptacle, they may be AC coupled and discharged per *USB 3.2* before the receptacle.
- AC coupling on pin pairs A2, A3 (TX1) and B2, B3 (TX2) as defined for SuperSpeed USB signaling per *USB 3.2* shall be used for Alternate Mode signaling.
- Signals being received at the USB Type-C receptacle shall not exceed the value specified for $V_{TX\text{-}DIFF\text{-}PP}$ in Table 6-18 of the *USB 3.2* specification.
- Direct Connect applications that remap pins A6 and A7 shall place pins A6 and A7 in a hi-Z state before transmitting the *USB PD* Enter_Mode command to the Sink. The Source shall not enable the alternate use of the A6 and A7 pins until an ACK has been received by the Source. In the event of a failure to enter the Alternate Mode after transmission of the *USB PD* Enter_Mode command, the Source shall restore pins A6 and A7 to the normative *USB 2.0* operation.

Direct connect applications shall ensure that any stubs introduced by repurposing the extra D+/D− pair do not interfere with USB communication with compliant hosts that short the pairs of pins together on the receptacle. This can be ensured by placing the Alternate Mode switch close to the plug, by adding inductors to eliminate the stubs at *USB 2.0* frequencies, by AC-terminating the long stubs to remove reflections at the cost of attenuated signal, or by other means.

When in an Alternate Mode, activity on the SBU lines shall not interfere with *USB PD* BMC communications or interfere with detach detection.

The AC coupling requirement are the same as defined in the *USB 3.2* specification. The TX signals shall be AC coupled within the system before the physical connector. The RX signals may be DC coupled or AC coupled and discharged within the system.

It should be noted that the AC coupling capacitor is placed in the system next to the USB Type-C receptacle, so that the system components (the orientation switch, the Alternate Mode selection multiplexer, and other system components) operate within the common mode limits set by the local PHY. This applies, in the SuperSpeed USB operation, to both the transmit path and the receive path within the local system. The receive path is isolated from the common mode of the port partner by the AC coupling capacitors that are implemented on the TX path in the port partner.

Figure E-3 shows the key components in a typical Alternate Mode implementation using a USB Type-C to USB Type-C full featured cable. This implementation meets the AC coupling requirements, as the capacitors required to be in or before the USB Type-C plug are implemented behind the TX pins in the port partner.

It should be noted that the AC coupling capacitor is placed in the system next to the USB Type-C receptacle, so that the system components (the orientation switch, the Alternate Mode selection multiplexer, and other system components) operate within the common mode limits set by the local PHY. This applies, in the SuperSpeed USB operation, to both the

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

E.2.2 备用模式电气要求

使用替代模式期间的信号传输应符合第 3 章的所有相关电缆组件、适配器组件和电气要求。

为了最大限度地降低在备用模式下操作时对 USB 主机或设备中的超高速 USB 发送器和接收器造成损坏的风险，指定了几项要求：

• 如果在固定电缆上使用引脚对 B11、B10（RX1）和 A11、A10（RX2），则应在 USB Type -C 插头之前或之中进行交流耦合。• 如果在 USB Type -C 插座上使用引脚对 B11、B10（RX1）和 A11、A10（RX2），则可按照 *USB 3.2* 在插座之前进行交流耦合和放电。• 引脚对 A2、A3（TX1）和 B2、B3（TX2）上的交流耦合（按照 *USB 3.2* 为超高速 USB 信号定义）应用于备用模式信号。• USB Type-C 插座接收的信号不得超过 *USB 3.2* 规范表 6-18 中 $V_{TX\text{-}DIFF\text{-}PP}$ 规定的值。重新映射引脚 A6 和 A7 的 • 直接连接应用应在将 *USB PD* Enter_Mode 命令传输到接收器之前将引脚 A6 和 A7 置于高阻状态。在源收到 ACK 之前，源不得启用 A6 和 A7 引脚的交替使用。如果在传输 *USB PD* Enter_Mode 命令后无法进入备用模式，源应将引脚 A6 和 A7 恢复到标准的 *USB 2.0* 操作。

直接连接应用应确保通过重新利用额外的 D+/D− 对而引入的任何短截线不会干扰 USB 与兼容主机的通信，这些主机将插座上的引脚对短接在一起。可以通过将备用模式开关放置在靠近插头的位置、通过添加电感器以消除 *USB 2.0* 频率的短截线、通过 AC 端接长短截线以消除反射（以衰减信号为代价）或其他方式来确保这一点。

处于备用模式时，SBU 线路上的活动不得干扰 *USB PD* BMC 通信或干扰分离检测。

AC 耦合要求与 *USB 3.2* 规范中的定义相同。TX 信号应在物理连接器之前在系统内进行 AC 耦合。RX 信号可以进行 DC 耦合或 AC 耦合并在系统内放电。

需要注意的是，AC 耦合电容器放置在系统中 USB Type-C 插座旁边，以便系统组件（方向开关、备用模式选择多路复用器和其他系统组件）在本地 PHY 设置的共模限制内运行。在超高速 USB 操作中，这适用于本地系统内的发送路径和接收路径。接收路径通过端口伙伴中 TX 路径上实现的 AC 耦合电容器与端口伙伴的共模隔离。

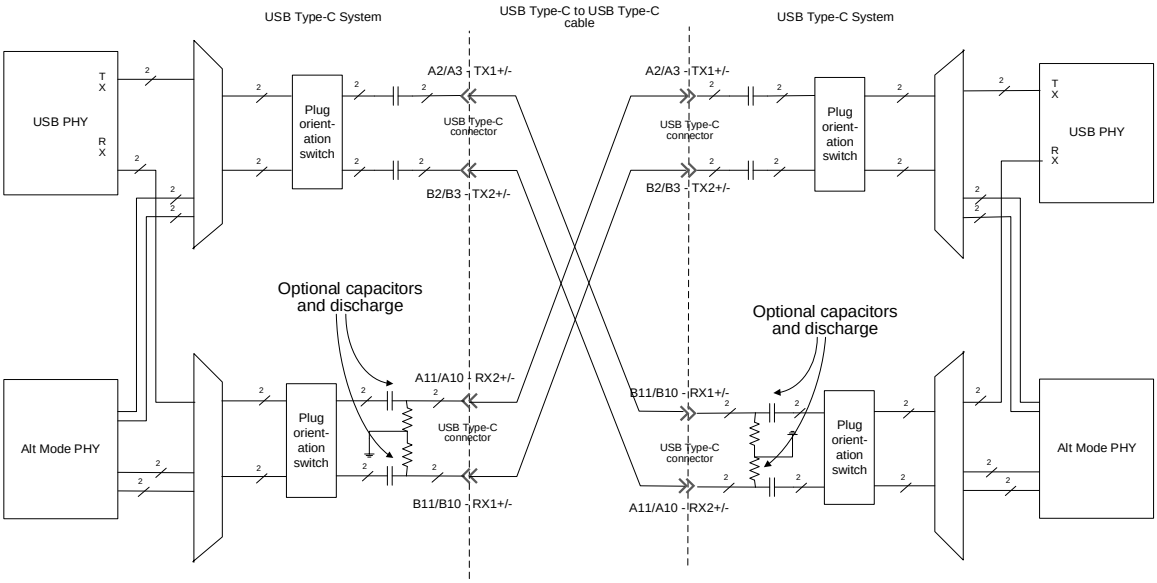
图 E-3 显示了使用 USB Type-C 转 USB Type-C 全功能电缆的典型备用模式实现中的关键组件。此实现满足交流耦合要求，因为需要在 USB Type-C 插头内或插头前的电容器在端口配对的 TX 引脚后面实现。

需要注意的是，交流耦合电容器放置在系统中 USB Type-C 插座旁边，以便系统组件（方向开关、备用模式选择多路复用器和其他系统组件）在本地 PHY 设置的共模限制内运行。在超高速 USB 操作中，这适用于

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

transmit path and the receive path within the local system. The receive path is isolated from the common mode of the port partner by the AC coupling capacitors that are implemented on the TX path in the port partner.

Figure E-3 Alternate Mode Implementation using a USB Type-C to USB Type-C Cable



In the case where the Alternate Mode System is required to implement DC blocking capacitors within the system between active system components and the Alternate Mode connector, then this provides the necessary isolation and further capacitors in the USB Type-C to Alternate Mode adapter cable are not necessary, and may indeed impair signal integrity.

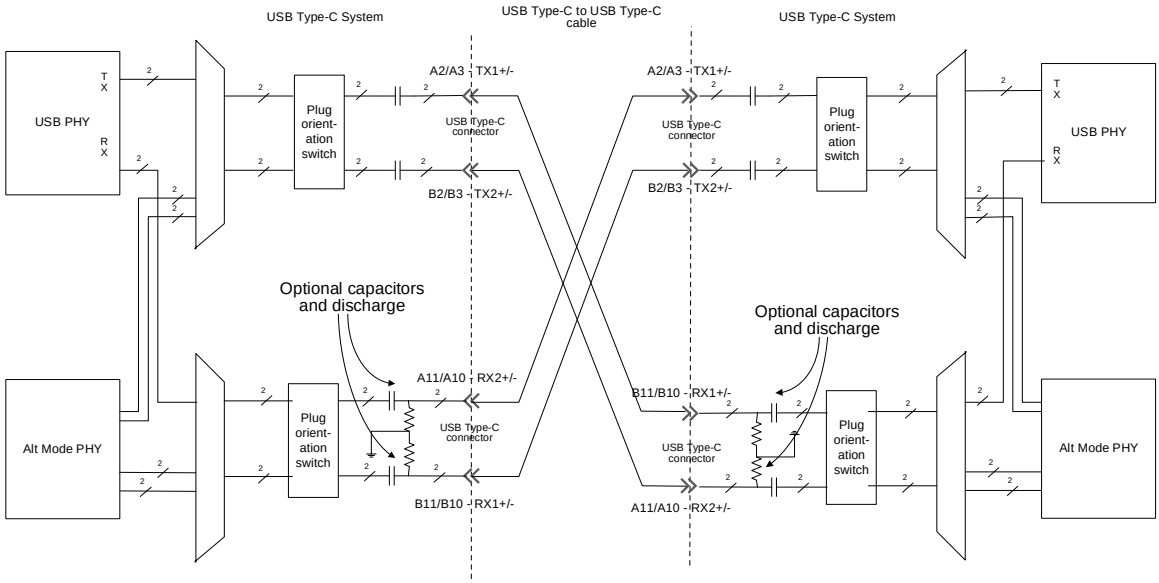
Figure E-4 shows the key components in a typical Alternate Mode implementation using either a USB Type-C to Alternate Mode connector cable, or a USB Type-C Alternate Mode Direct Attach device. In both cases it is necessary that the system path behind the RX pins on the USB receptacle be isolated from external common mode. This requirement is met by incorporating capacitors in or behind the USB Type-C plug on the Alternate Mode cable or Alternate Mode device.

In the case where the Alternate Mode System is required to implement DC blocking capacitors within the system between active system components and the Alternate Mode connector, then this provides the necessary isolation and further capacitors in the USB Type-C to Alternate Mode adapter cable are not necessary, and may indeed impair signal integrity.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

本地系统内的发送路径和接收路径。接收路径通过端口伙伴的 TX 路径上实现的 AC 耦合电容器与端口伙伴的共模隔离。

图 E-3 使用 USB Type-C 转 USB Type-C 线缆实现替代模式



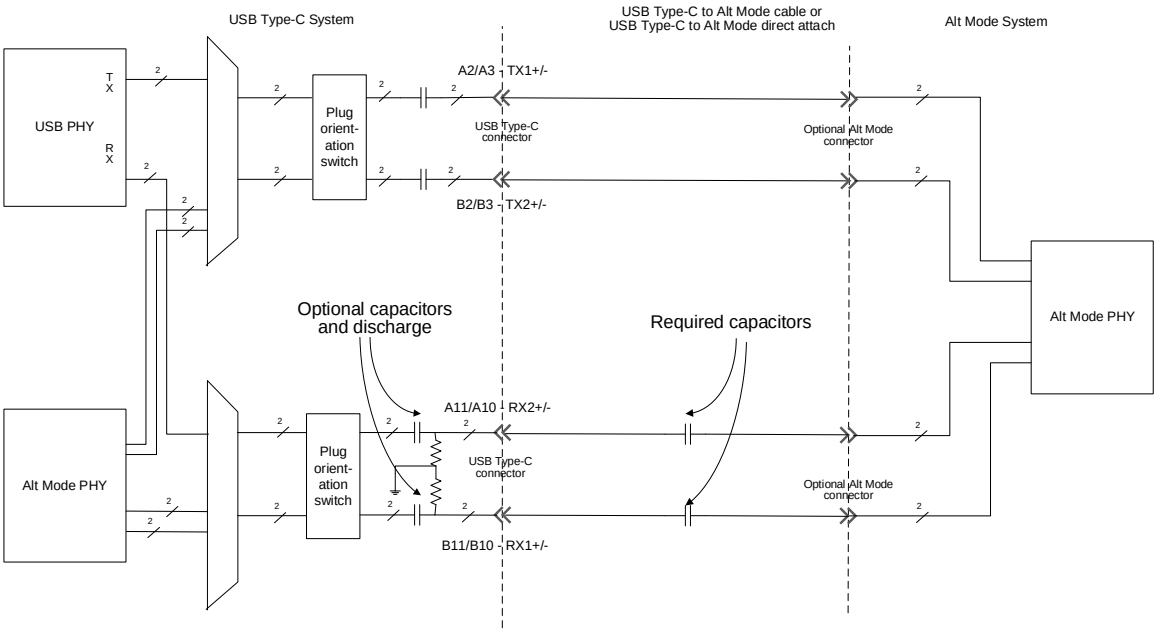
如果备用模式系统需要在有源系统组件和备用模式连接器之间的系统内实现直流阻断电容器，那么这将提供必要的隔离，而 USB Type-C 到备用模式适配器电缆中的其他电容器是没有必要的，并且可能确实会损害信号完整性。

图 E-4 显示了使用 USB Type-C 至备用模式连接器电缆或 USB Type-C 备用模式直接连接设备的典型备用模式实现中的关键组件。在这两种情况下，USB 插座上 RX 引脚后面的系统路径都必须与外部共模隔离。通过在备用模式电缆或备用模式设备上的 USB Type-C 插头内或后面加入电容器，可以满足此要求。

如果备用模式系统需要在有源系统组件和备用模式连接器之间的系统内实现直流阻断电容器，那么这将提供必要的隔离，而 USB Type-C 到备用模式适配器电缆中的其他电容器是没有必要的，并且可能确实会损害信号完整性。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure E-4 Alternate Mode Implementation using a USB Type-C to Alternate Mode Cable or Device



The USB Safe State is defined by the *USB PD* specification. The USB Safe State defines an electrical state for the SBU1/2 and TX/RX for DFPs, UFPs, and Active Cables when transitioning between USB and an Alternate Mode. SBU1/2 and TX/RX must transition to the USB Safe State before entering to or exiting from an Alternate Mode. Table E-1 defines the electrical requirements for the USB Safe State. See the *USB-PD* Specification for more detail on entry/exit mechanisms to the USB Safe State.

Table E-1 USB Safe State Electrical Requirements

	SBU1/2	TX[1,2]	RX[2]	A6/A7/B6/B7[4]
Common-mode voltage	0 to 1.5 V	0 to 1.5 V	0 to 1.5 V	0 to 1.5 V
Impedance to ground[3]	< 4 MΩ	< 4 MΩ	25 KΩ – 4 MΩ	< 4 MΩ

Notes:

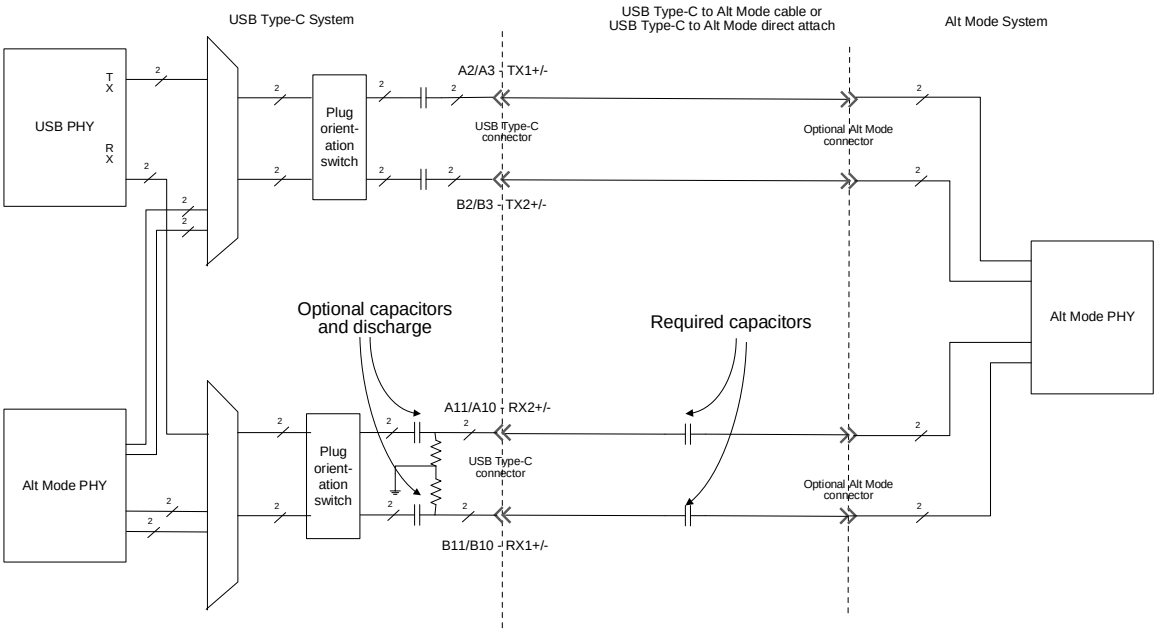
1. TX common-mode voltage is defined on the integrated circuit side of the AC coupling capacitors.
2. Unused TX and RX signals should transition to USB Safe State if wired to the connector but not used.
3. The DFP and UFP shall provide a discharge path to ground in USB Safe State when a connection to the USB Type-C receptacle is present.
4. Applies to docking solutions/direct connect applications that redefine pins A6, A7, B6 and B7.

E.3 Parameter Values

Table E-2 provides the timeout requirement for a device that supports Alternate Modes to enable a *USB Billboard Device Class* interface when none of the modes supported by the device are successfully recognized and configured by the DFP to which the device is attached.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 E-4 使用 USB Type-C 转备用模式电缆或设备实现备用模式



USB 安全状态由 *USB PD* 规范定义。USB 安全状态定义了在 USB 和备用模式之间转换时 DFP、UFP 和有源电缆的 SBU1/2 和 TX/RX 的电气状态。SBU1/2 和 TX/RX 必须先转换到 USB 安全状态，然后才能进入或退出备用模式。表 E-1 定义了 USB 安全状态的电气要求。有关进入/退出 USB 安全状态的更多详细信息，请参阅 *USB-PD* 规范。

表 E-1 USB 安全状态电气要求

	SBU1/2	**TX[1,2]**	**RX[2]**	**A6/A7/B6/B7[4]**
Common-mode voltage	0 to 1.5 V	0 to 1.5 V	0 to 1.5 V	0 to 1.5 V
Impedance to ground[3]	< 4 MΩ	< 4 MΩ	25 KΩ – 4 MΩ	< 4 MΩ

注释：1. TX 共模电压在交流耦合电容器的集成电路侧定义。2. 如果未使用的 TX 和 RX 信号连接到连接器但未使用，则应转换为 USB 安全状态。3. 当存在与 USB Type-C 插座的连接时，DFP 和 UFP 应在 USB 安全状态下提供接地放电路径。4. 适用于重新定义引脚 A6、A7、B6 和 B7 的对接解决方案/直接连接应用。

E.3 参数值

表 E-2 提供了当设备所连接的 DFP 无法成功识别和配置该设备支持的任何模式时，支持备用模式的设备启用 *USB Billboard Device Class* 接口的超时要求。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table E-2 USB Billboard Device Class Availability Following Alternate Mode Entry Failure

	Maximum	Description
tAMETimeout	1000 ms	The time between a Sink attach until a *USB Billboard Device Class* interface is exposed when an Alternate Mode is not successfully entered

While operating in an Alternate Mode, the signaling shall not cause noise ingression onto USB signals operating concurrently that exceeds the Vnoise parameters given in Table E-3.

Table E-3 Alternate Mode Signal Noise Ingression Requirements

	Limit	Bandwidth
Vnoise on BMC during BMC Active	30 mV	100 ns time constant filter
Vnoise on BMC during BMC Idle	100 mV	100 ns time constant filter
Vnoise on D+/D− (Single-ended)	40 mV	500 MHz
Vnoise on D+/D− (Differential)	10 mV	500 MHz

Note: Each Vnoise parameter is the max noise ingression level allowed onto the respective interface that is due to two SBU aggressors from the Alternate Mode signaling, under respective worse case scenarios. The coupling between SBU_A/SBU_B and CC within a USB Type-C cable shall meet the requirement described in Section 3.7.2.5.4. The coupling between SBU_A/SBU_B and USB D+/D− within a USB Type-C cable shall meet the requirement described in Section 3.7.2.5.5.

E.4 Example Alternate Mode – USB DisplayPort™ Dock

This example illustrates the use of Structured VDMs to expose and access functionality beyond the basic functionality defined by the USB Type-C Connector. The device uses its USB Type-C connector to make connection when placed in a cradle dock. This example only illustrates the functional connections.

E.4.1 USB DisplayPort™ Dock Example

- The cradle dock provides mechanical alignment and attachment in addition to those provided by the USB Type C connector allowing for only one orientation eliminating the need for an orientation MUX in the dock.
- The dock and system use *USB PD* to manage charging and power.
- The dock uses DisplayPort to drive a DisplayPort-to-HDMI adapter to support connecting an HDMI monitor.
- The dock has a USB hub that exposes two external USB ports and attached internal USB Devices, e.g. a USB audio Device (a 3.5 mm audio jack), and a USB Billboard Device.

Figure E-5 illustrates the USB DisplayPort Dock example in a block diagram form.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 E-2 备用模式进入失败后 USB 公告牌设备类别的可用性

	Maximum	Description
tAMETimeout	1000 ms	The time between a Sink attach until a *USB Billboard Device Class* interface is exposed when an Alternate Mode is not successfully entered

在替代模式下运行时，信号不得导致噪声进入同时操作的 USB 信号，且噪声不得超过表 E-3 中给出的 Vnoise 参数。

表 E-3 交替模式信号噪声侵入要求

	Limit	Bandwidth
Vnoise on BMC during BMC Active	30 mV	100 ns time constant filter
Vnoise on BMC during BMC Idle	100 mV	100 ns time constant filter
Vnoise on D+/D− (Single-ended)	40 mV	500 MHz
Vnoise on D+/D− (Differential)	10 mV	500 MHz

注意：每个 Vnoise 参数都是在各自最坏情况下，由于来自备用模式信号的两个 SBU 干扰源而允许进入相应接口的最大噪声侵入水平。USB Type-C 电缆中 SBU_A/SBU_B 和 CC 之间的耦合应满足第 3.7.2.5.4 节中所述的要求。USB Type-C 电缆中 SBU_A/SBU_B 和 USB D+/D− 之间的耦合应满足第 3.7.2.5.5 节中所述的要求。

E.4 示例替代模式 – USB DisplayPort™ 基座

此示例说明了如何使用结构化 VDM 来公开和访问 USB Type-C 连接器定义的基本功能以外的功能。设备在放置在底座中时使用其 USB Type-C 连接器进行连接。此示例仅说明了功能连接。

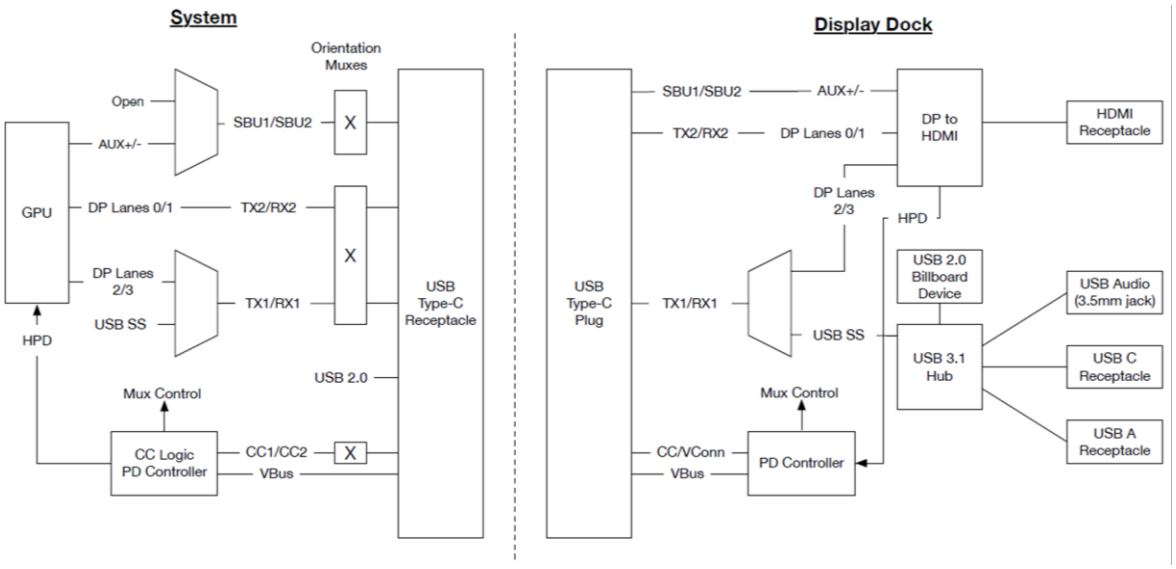
E.4.1 USB DisplayPort™ 基座示例

- 除了上述功能外，支架底座还提供机械对准和连接功能
  由 USB Type C 连接器提供，仅允许一个方向消除
  需要在基座中使用方向 MUX。• 基座和系统使用 *USB PD* 来管理充电和电源。• 基座使用 DisplayPort 来驱动 DisplayPort 转 HDMI 适配器，以支持连接 HDMI 显示器。• 基座有一个 USB 集线器，可公开两个外部 USB 端口和连接的内部 USB 设备，例如 USB 音频设备（3.5 毫米音频插孔）和 USB 广告牌设备。

图 E-5 以框图形式说明了 USB DisplayPort Dock 示例。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure E-5 USB DisplayPort Dock Example



The system uses *USB PD* Structured VDMs to communicate with the dock to discover that it supports a compatible Alternate Mode. The system then uses a Structured VDM to enter the dock mode. Since *USB PD* is used, it may also be used to negotiate power for the system and dock. In this example, the SuperSpeed USB signals allow the dock to work as a USB-only dock when attached to a system that does not fully support the dock or even *USB PD*.

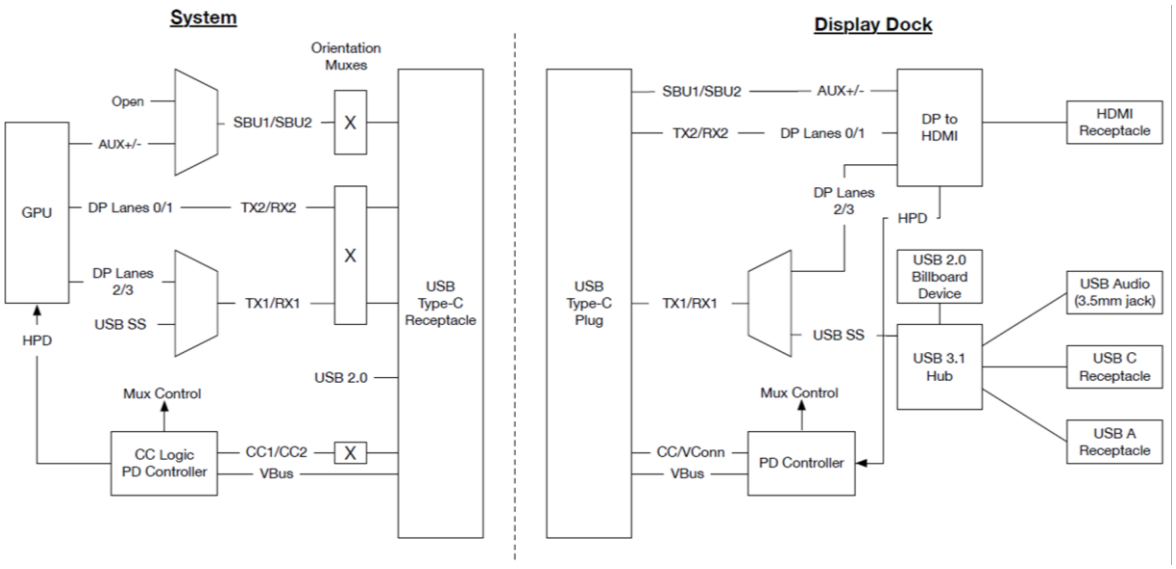
E.4.2 Functional Overview

The following summarizes the behavior resulting from attaching the example USB DisplayPort Dock for three likely host system cases.

1. Host system does not support *USB PD* or supports *USB PD* without Structured VDMs
    - The host does not support *USB PD*, or supports *USB PD* but not Structured VDMs, so it will not look for SVIDs using the Structured VDM method.
    - The host will discover the USB hub and operates as it would when connected to any USB hub.
    - Since the host will not send an Enter Mode command, after tAMETimeout the dock will expose a *USB Billboard Device Class* interface that the host will enumerate. The host then reports to the user that an unsupported Device has been connected, identifying the type of Device from the *USB Billboard Device Class* information.
2. Host system supports *USB PD* and Structured VDMs but does not support this specific USB DisplayPort Dock
    - The host discovers the USB hub and operates as it would when connected to any USB hub.
    - The Host looks for SVIDs that it recognizes. The VID associated with this USB DisplayPort Dock may or may not be recognized by the Host.
    - If that VID is recognized by the Host, the Host then requests the modes associated with this VID. The mode associated with this USB DisplayPort Dock is not recognized by the Host.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 E-5 USB DisplayPort 基座示例



系统使用 *USB PD* 结构化 VDM 与底座通信，以发现它支持兼容的备用模式。然后系统使用结构化 VDM 进入底座模式。由于使用了 *USB PD*，因此它还可用于协商系统和底座的电源。在此示例中，当连接到不完全支持底座甚至 *USB PD* 的系统时，超高速 USB 信号允许底座作为仅支持 USB 的底座工作。

E.4.2 功能概述

下面总结了在三种可能的主机系统情况下连接示例 USB DisplayPort Dock 所产生的行为

。

1. 主机系统不支持 *USB PD* 或不支持没有结构化 VDM 的 *USB PD*

   o 主机不支持 *USB PD*，或者支持 *USB PD* 但不支持结构化 VDM，因此它不会使用结构化 VDM 方法查找 SVID。o 主机将发现 USB 集线器并像连接时一样运行

   到任何 USB 集线器。o 由于主机不会发送进入模式命令，因此在 tAMETimeout 之后

   dock 将公开一个主机将枚举的 *USB Billboard Device Class* 接口。然后主机向用户报告已连接不受支持的设备，并从 *USB Billboard Device Class* 信息中识别设备类型。

2. 主机系统支持 *USB PD* 和 Structured VDM，但不支持此特定的 USB DisplayPort Dock

   o 主机发现 USB 集线器并像连接到任何 USB 集线器时一样运行。 o 主机查找它识别的 SVID。主机可能会识别或可能不会识别与此 USB DisplayPort Dock 关联的 VID。 o 如果主机识别该 VID，则主机会请求与此 VID 关联的模式。主机无法识别与此 USB DisplayPort Dock 关联的模式。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- Since the host does not recognize the mode as being supported hence will not send the Enter Mode command, after tAMETimeout the dock will expose a *USB Billboard Device Class* interface that the host will enumerate. The host then reports to the user that an unsupported Device has been connected, identifying the type of Device from the *USB Billboard Device Class* information.

3. Host system supports this specific USB DisplayPort Dock
   - The Host looks for SVIDs that it recognizes. The VID associated with this USB DisplayPort Dock is recognized by the Host.
   - The Host then requests the modes associated with this VID. The mode associated with this USB/Display Dock is recognized by the Host.
   - Since this mode is recognized as supported, the Host uses the Enter Mode command to reconfigure the USB Type-C receptacle and enter the USB DisplayPort Dock mode.
   - The USB DisplayPort Dock may optionally expose the *USB Billboard Device Class* interface to provide additional information to the OS.

E.4.3 Operational Summary

The following summarizes the basic process of discovery through configuration when the USB DisplayPort Dock is attached to the Host.

1. Host detects presence of a device (CC pins) and connector orientation
2. Host applies default VBUS
3. Host applies VCONN because the dock presents Ra
4. Host uses *USB PD* to make power contract with the USB DisplayPort Dock
5. Host runs the Discover Identify process
   a. Sends Discover Identity message
   b. Receives an ACK message with information identifying the cable
6. Host runs the Discover SVIDs process
   a. Sends Discover SVID message
   b. Receives an ACK message with list of SVIDs for which the Dock device has modes
7. Host runs the Discover Modes process
   a. Sends Discover Modes VDM for the VIDs previously discovered
   b. Receives an ACK message with a list of modes associated with each VID
   c. If USB DisplayPort Dock mode not found, dock will timeout and present the *USB Billboard Device Class* interface and the OS will inform the user of the error - done
   d. Else
8. Host runs the Enter Mode process
   a. Sends Enter Mode VDM with VID and USB DisplayPort Dock mode
   b. Receives an ACK message – Host is now attached to the USB DisplayPort Dock and supports DisplayPort signaling to interface additional functions in combination with USB signaling

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

o 由于主机无法识别受支持的模式，因此不会发送“进入模式”命令，在 tAMETimeout 之后，扩展坞将公开主机将枚举的 *USB Billboard Device Class* 接口。然后，主机向用户报告已连接不受支持的设备，并从 *USB Billboard Device Class* 信息中识别设备类型。

3. 主机系统支持此特定的 USB DisplayPort 底座

o 主机查找其识别的 SVID。与此 USB 关联的 VID DisplayPort Dock 被主机识别。o 然后主机请求与此 VID 关联的模式。主机识别与此 USB/Display Dock 关联的模式。o 由于此模式被识别为受支持，主机使用 Enter Mode 命令重新配置 USB Type-C 插座并进入 USB DisplayPort Dock 模式。o USB DisplayPort Dock 可以选择性地公开 *USB Billboard Device Class* 接口以向操作系统提供更多信息。

E.4.3 操作概要

下面总结了当 USB DisplayPort Dock 连接到 Host 时，通过配置进行发现的基本过程。

1. 主机检测设备的存在（CC 引脚）和连接器方向 2. 主机应用默认 VBUS 3. 主机应用 VCONN，因为底座提供 Ra 4. 主机使用 *USB PD* 与 USB DisplayPort 底座建立电源协议 5. 主机运行发现识别过程 a. 发送发现识别消息 b. 接收带有识别电缆信息的 ACK 消息

6. 主机运行 Discover SVID 进程

a. 发送 Discover SVID 消息 b. 接收 ACK 消息，其中包含 Dock 设备具有模式的 SVID 列表

7. 主机运行发现模式进程

a. 发送先前发现的 VID 的发现模式 VDM b. 接收带有与每个 VID 关联的模式列表的 ACK 消息 c. 如果未找到 USB DisplayPort Dock 模式，则 dock 将超时并显示 *USB Billboard Device Class* 接口，操作系统将通知用户错误 - 完成 d. 否则

8.主机运行进入模式进程

a. 发送带有 VID 和 USB DisplayPort 基座模式的进入模式 VDM b. 接收 ACK 消息 – 主机现已连接到 USB DisplayPort 基座，并支持 DisplayPort 信号传输，以便结合 USB 信号传输实现附加功能

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

9. Host stays in the USB DisplayPort Dock mode until
    a. Explicitly exited by an Exit Mode VDM
    b. System physically disconnected from the USB DisplayPort Dock
    c. Hard Reset on *USB PD*
    d. V_{BUS} is removed

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

9. 主机保持 USB DisplayPort Dock 模式，直到

a. 通过退出模式 VDM 明确退出 b. 系统与 USB DisplayPort 基座物理断开连接 c. 在 *USB PD* 上进行硬重置 d. VBUS 被移除

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F Thunderbolt 3 Compatibility Discovery and Entry

The *USB4™* specification includes defined support for compatibility between *USB4* products that are designed to interoperate with existing Thunderbolt™ 3 (TBT3) products. This appendix documents the normative methodology to discover and enter into TBT3 between two port partners – this methodology relys on Alternate Mode protocol as defined in Appendix E of this specification and the USB Power Delivery specification.

Thunderbolt 3 technology is organized into two primary product categories; hosts and devices. Most TBT3 devices include at least one upstream and one downstream port although a TBT3 device may include more than one downstream port in a manner similar to a hub or no downstream ports in a manner similar to a peripheral.

F.1 TBT3 Compatibility Mode Functional Requirements

In order to successfully interoperate with existing TBT3 products, the functional requirements in the following subsections must be met.

F.1.1 TBT3-Compatible Power Requirements

Before two TBT3-compatible port partners can enter TBT3 mode, a *USB PD* explicit power contract shall be established.

F.1.2 TBT3-Compatible Host Requirements

All TBT3-compatible host ports shall meet the following requirements.

- Support DRP operation
- If resolved to a UFP, use *USB PD* DR_Swap to attempt to switch into the DFP data role when DFP is preferred
- If resolved to a DFP, do not accept *USB PD* DR_Swap to remain in the DFP data role when DFP is preferred

F.1.3 TBT3-Compatible Device Upstream Requirements

F.1.3.1 Self-Powered Device

The TBT3-compatible upstream port of a self-powered device shall meet the following requirements.

- Support DRP operation
- Prefer Sink/UFP through the implementation and use of Try.SNK as needed
- If resolved to a DFP, accept *USB PD* DR_Swap to switch into the UFP data role

F.1.3.2 Bus-Powered Device

The TBT3-compatible upstream port of a bus-powered device shall meet the following requirements.

- Support Sink/UFP operation
- Reject *USB PD* DR_Swap to remain in the UFP data role

F.1.4 TBT3-Compatible Device Downstream Requirements

F.1.4.1 Self-Powered Device

The TBT3-compatible downstream stream port of a self-powered device shall meet the following requirements.

- Support DRP operation

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F Thunderbolt 3 兼容性发现和输入

USB4™ 规范包括对 *USB4* 产品之间兼容性的定义支持，这些产品旨在与现有的 Thunde rbolt™ 3 (T BT3) 产品进行互操作。本附录记录了在两个端口合作伙伴之间发现和进入 TBT3 的规范方法 - 该方法依赖于本规范附录 E 中定义的备用模式协议和 USB 电源传输规范。

Thunderbolt 3 技术分为两个主要产品类别：主机和设备。大多数 TBT3 设备至少包含一个上行端口和一个下行端口，但 TBT3 设备可能包含多个下行端口（类似于集线器）或不包含下行端口（类似于外围设备）。

F.1 TBT3兼容模式功能要求

为了成功地与现有的 T BT3 产品互操作，必须满足以下小节中的功能要求。

F.1.1 TBT3 兼容电源要求

在两个兼容 TBT3 的端口伙伴进入 TBT3 模式之前，必须建立 *USB PD* 显式电源合同。

F.1.2 TBT3 兼容主机要求

所有兼容TBT3的主机端口都应满足以下要求。

- 支持 DRP 操作 • 如果解析为 UFP，则使用 *USB PD* DR_Swap 尝试切换到 DFP 数据角色

  当 DFP 为首选时 • 如果解析为 DFP，则不接受 *USB PD* DR_Swap，以便在 DFP 为首选时保留 DFP 数据角色

F.1.3 TBT3 兼容设备上行要求

F.1.3.1 自供电设备

自供电设备的TBT3兼容上行端口应满足以下要求。

- 支持 DRP 操作 • 根据需要通过实施和使用 Try.SNK 来优先选择 Sink/UFP • 如果解析为 DFP，则接受 *USB PD* DR_Swap 以切换到 UFP 数据角色

F.1.3.2 总线供电设备

总线供电设备的TBT3兼容上行端口应满足以下要求。

- 支持 Sink/UFP 操作 • 拒绝 *USB PD* DR_Swap 以保留 UFP 数据角色

F.1.4 TBT3 兼容设备下游要求

F.1.4.1 自供电设备

自供电设备的兼容TBT3的下行流端口应满足以下要求。

- 支持DRP操作

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- Prefer Source/DFP through the implementation and use of Try.SRC as needed
- If resolved to a DFP, do not accept *USB PD* DR_Swap and remain in the DFP data role

F.1.4.2 Bus-Powered Device

The TBT3-compatible downstream port of a bus-powered device shall meet the following requirements.

- Support Sink

F.1.5 TBT3-Compatible Self-Powered Device Without Predefined Upstream Port Rules

A TBT3-compatible device port may behave as either a downstream or upstream port based on its connection state to a TBT3-compatible host as described below.

- When no TBT3-compatible host is connected, the USB Type-C® ports shall:
  - Prefer to be configured as a UFP
  - Implement and use Try.SNK as needed to get into the UFP state
  - If resolved to a DFP, initiate or accept *USB PD* DR_Swap to switch to the UFP data role
  - Accept *USB PD* DR_Swap to switch to the DFP data role
  - When resolved to a UFP, identify this port as being connected to the host
- When a TBT3-compatible host is initially connected, the remaining downstream USB Type-C ports shall:
  - Implement and use Try.SRC as needed to get into the DFP state
  - Issue a Hard Reset if a *USB PD* DR_Swap is received when both a connection is present and an Alternate Mode is in place
  - Issue a *USB PD* DR_Swap to switch to the DFP data role if a connection is present but no Alternate Mode has been entered (this includes performing a disconnect/reconnect on the port)
  - Accept *USB PD* DR_Swap to switch to the DFP data role if a connection is present but no Alternate Mode has been entered (this includes performing a disconnect/reconnect on the port)
- When a TBT3-compatible host is disconnected, the downstream USB Type-C ports shall:
  - Perform a disconnect/reconnect on the port
  - Behave as if no host is connected

F.1.6 TBT3-Compatible Devices with a Captive Cable

TBT3-compatible devices with a captive cable shall respond to *USB PD* messages both SOP and SOP'.

F.2 TBT3 Discovery and Entry Flow

Figure F-1 describes the flow for a TBT3-compatible DFP port to discover and enter into the TBT3 Compatibility Mode of USB4 with a connected UFP. For each functional block, refer to the sub-sections identified for additional details.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• 根据需要通过实施和使用 Try.SRC 来首选 Source/DFP • 如果解析为 DFP，则不接受 *USB PD* DR_Swap 并保留在 DFP 数据角色中

F.1.4.2 总线供电设备

总线供电设备的TBT3兼容下行端口应满足以下要求。

• 支撑水槽

F.1.5 无预定义上行端口规则的 TBT3 兼容自供电设备

TBT3 兼容设备端口可以根据其与 TBT3 兼容主机的连接状态表现为下游端口或上游端口，如下所述。

• 当未连接任何兼容 TBT3 的主机时，USB Type-C® 端口应：o 优先配置为 UFP o 根据需要实现并使用 Try.SNK 进入 UFP 状态 o 如果解析为 DFP，则启动或接受 *USB PD* DR_Swap 以切换到 UFP 数据角色 o 接受 *USB PD* DR_Swap 以切换到 DFP 数据角色 o 解析为 UFP 时，将此端口标识为已连接到主机 • 首次连接兼容 TBT3 的主机时，其余下游 USB

Type-C 端口应： o 根据需要实现并使用 Try.SRC 以进入 DFP 状态 o 如果在存在连接且备用模式就绪的情况下收到 *USB PD* DR_Swap，则发出硬重置 o 如果存在连接但未进入备用模式（这包括在端口上执行断开连接/重新连接），则发出 *USB PD* DR_Swap 以切换到 DFP 数据角色 o 如果存在连接但未进入备用模式（这包括在端口上执行断开连接/重新连接），则接受 *USB PD* DR_Swap 以切换到 DFP 数据角色 • 当 TBT3 兼容主机断开连接时，下游 USB Type-C 端口应： o 在端口上执行断开连接/重新连接 o 表现得好像没有主机连接

F.1.6 具有固定电缆的 TBT3 兼容设备

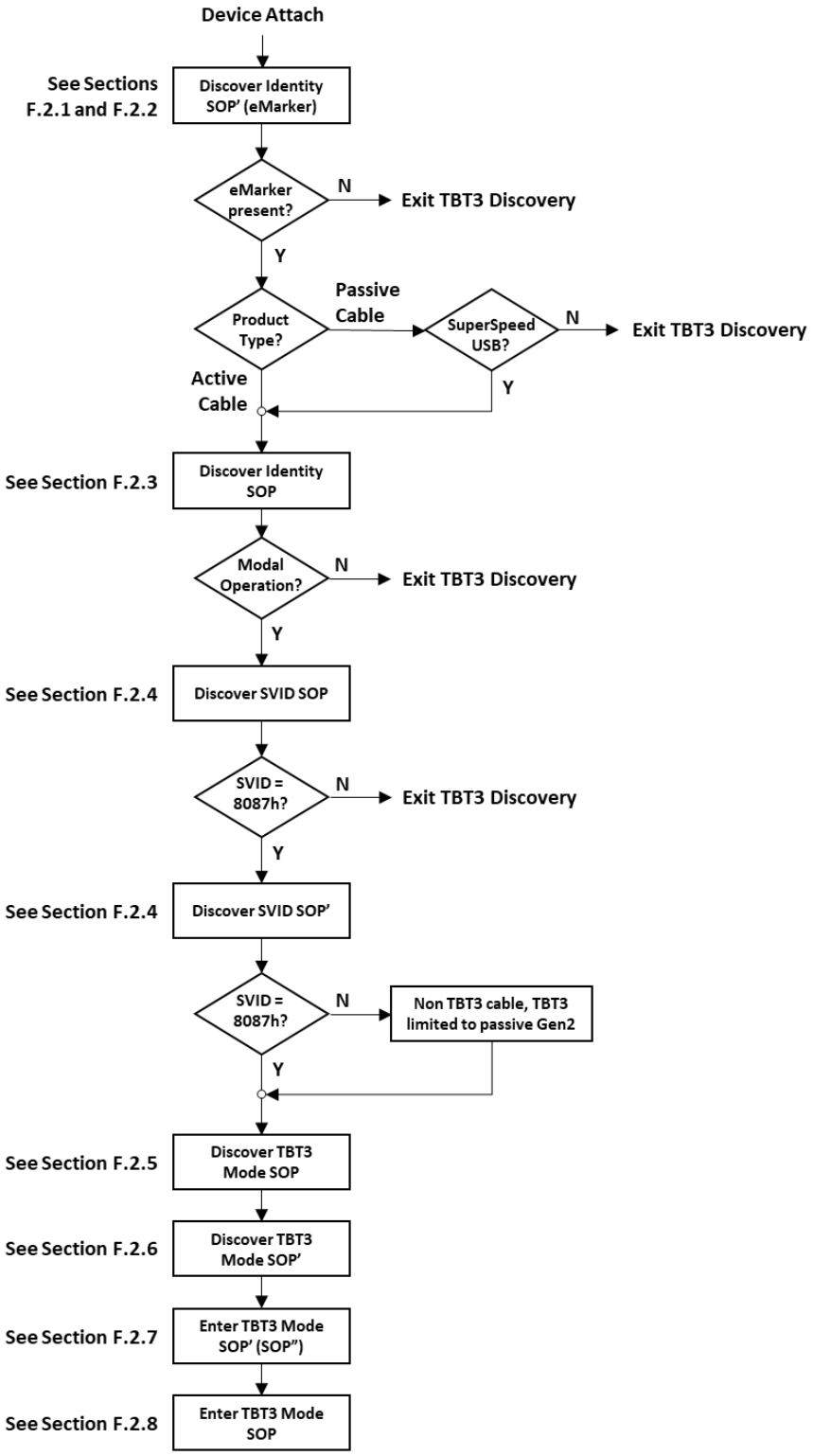
带有固定电缆的 TBT3 兼容设备应对 *USB PD* 消息 SOP 和 SOP ’ 做出响应。

F.2 TBT3 发现和进入流程

图 F-1 描述了兼容 TBT3 的 DFP 端口发现并进入 USB4 的 TBT3 兼容模式（已连接 UFP）的流程。有关每个功能块的更多详细信息，请参阅所标识的子部分。

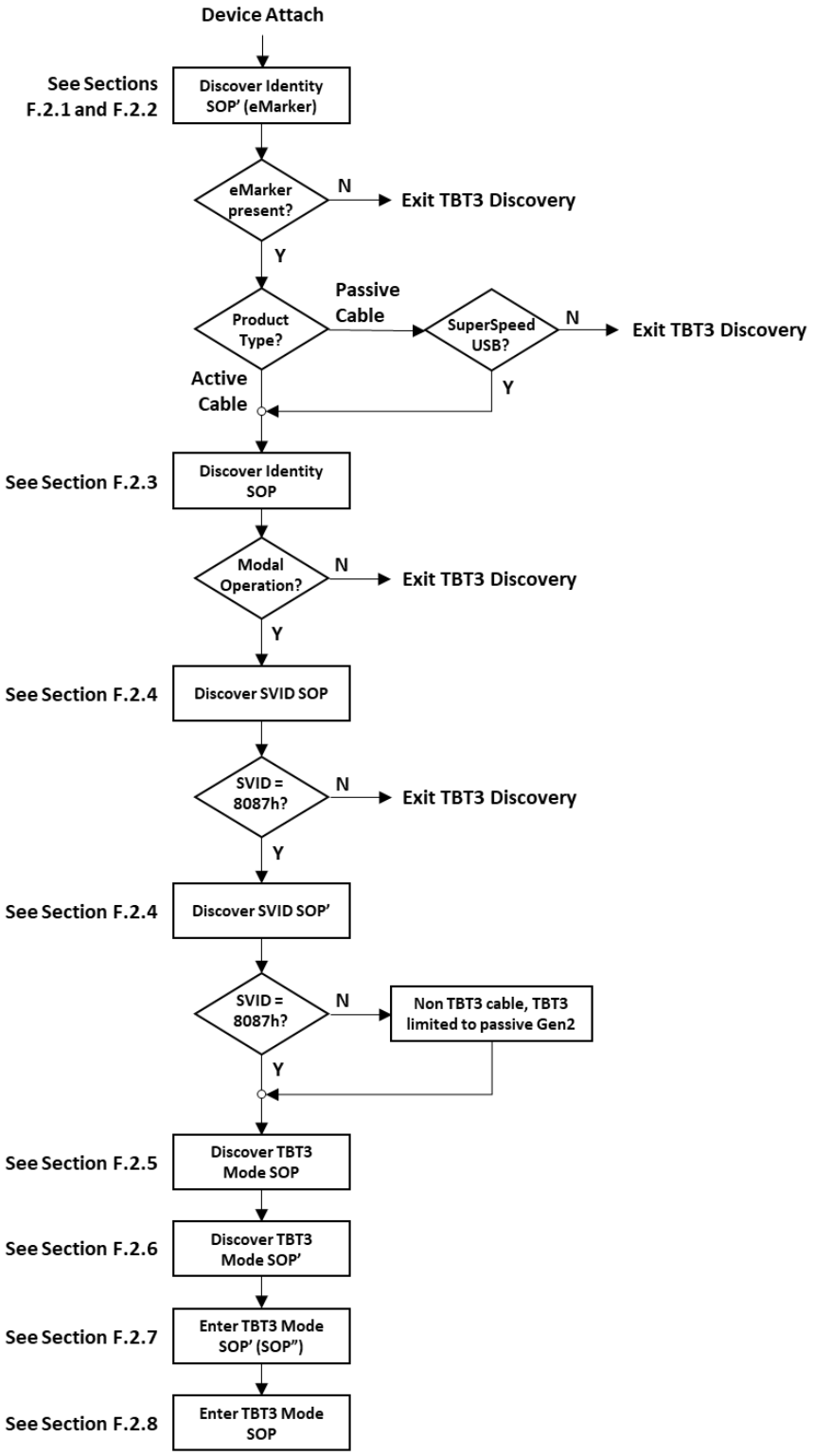
Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Figure F-1 TBT3 Discovery Flow



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

图 F-1 TBT3 发现流程



Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.1 TBT3 Passive Cable Discover Identity Responses

Table F-1, along with Table F-2 and Table F-3, defines the expected Discover Identity VDO responses for a TBT3 passive cable. In fields where multiple values are listed, cable responses may vary to match the specific connected cable's capabilities.

Table F-1 TBT3 Passive Cable Discover Identity VDO Responses

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	5…6	0…7	1 = Cable Plug		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00001b

Bit(s)	Value	Parameter
ID Header VDO		
B31	0	USB Communications Capable as USB Host
B30	0	USB Communications Capable as a USB Device
B29…27	011b = Passive Cable	Product Type (Cable Plug)
B26	1 = Modal Operation	Modal Operation Supported
B25…23	000b	Product Type (DFP)
B22…16	0	***Reserved***
B15…0	Per vendor	USB Vendor ID
Cert Stat VDO		
B31…0	0x00000000…0xFFFFFFFF	XID assigned by USB-IF
Product VDO		
B31…16	0x0000…0xFFFF	USB Product ID
B15…0	0x0000…0xFFFF	bcdDevice
Passive Cable VDO		
Depending on USB PD Specification Revision: See Table F-2 for USB PD Revision 2.0 or Table F-3 for USB PD Revision 3.0		

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.1 TBT3 无源电缆发现身份响应

表 F-1 以及表 F-2 和表 F-3 定义了 TBT3 无源电缆的预期 Discover Identity VDO 响应。在列出多个值的字段中，电缆响应可能会有所不同，以匹配特定连接电缆的功能。

表 F-1 TBT3 无源电缆发现身份 VDO 响应

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	5…6	0…7	1 = Cable Plug		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00001b

Bit(s)	Value	Parameter
ID Header VDO		
B31	0	USB Communications Capable as USB Host
B30	0	USB Communications Capable as a USB Device
B29…27	011b = Passive Cable	Product Type (Cable Plug)
B26	1 = Modal Operation	Modal Operation Supported
B25…23	000b	Product Type (DFP)
B22…16	0	***Reserved***
B15…0	Per vendor	USB Vendor ID
Cert Stat VDO		
B31…0	0x00000000…0xFFFFFFFF	XID assigned by USB-IF
Product VDO		
B31…16	0x0000…0xFFFF	USB Product ID
B15…0	0x0000…0xFFFF	bcdDevice
Passive Cable VDO		
Depending on USB PD Specification Revision: See Table F-2 for USB PD Revision 2.0 or Table F-3 for USB PD Revision 3.0		

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table F-2 TBT3 Passive Cable VDO for USB PD Revision 2.0, Version 1.3

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	0001b – <10ns (~1m) 0010b – 10ns to 20ns (~2m)	Cable Latency
B12…11	00b = VCONN not required	Cable Termination Type
B10	0 = Fixed	SSTX1 Directionality Support
B9	0 = Fixed	SSTX2 Directionality Support
B8	0 = Fixed	SSRX1 Directionality Support
B7	0 = Fixed	SSRX2 Directionality Support
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4	1 = Yes	VBUS through cable
B3	0 = No	SOP" controller present
B2…0	010b = [USB 3.1] Gen1 and Gen2	SuperSpeed USB Signaling Support

Table F-3 TBT3 Passive Cable VDO for USB PD Revision 3.0, Version 1.2

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…21	000b = Version 1.0	VDO Version
B20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	0001b – <10ns (~1m) 0010b – 10ns to 20ns (~2m)	Cable Latency
B12…11	00b = VCONN not required	Cable Termination Type
B10…9	00b = 20V	Maximum VBUS Voltage
B8…7	00b	***Reserved***
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4…3	00b	***Reserved***
B2…0	010b = [USB 3.2] Gen1 and Gen2	SuperSpeed USB Signaling Support

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 F-2 USB PD 修订版 2.0、版本 1.3 的 TBT3 无源电缆 VDO

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	0001b – <10ns (~1m) 0010b – 10ns to 20ns (~2m)	Cable Latency
B12…11	00b = VCONN not required	Cable Termination Type
B10	0 = Fixed	SSTX1 Directionality Support
B9	0 = Fixed	SSTX2 Directionality Support
B8	0 = Fixed	SSRX1 Directionality Support
B7	0 = Fixed	SSRX2 Directionality Support
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4	1 = Yes	VBUS through cable
B3	0 = No	SOP" controller present
B2…0	010b = [USB 3.1] Gen1 and Gen2	SuperSpeed USB Signaling Support

表 F-3 USB PD 修订版 3.0、版本 1.2 的 TBT3 无源电缆 VDO

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…21	000b = Version 1.0	VDO Version
B20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	0001b – <10ns (~1m) 0010b – 10ns to 20ns (~2m)	Cable Latency
B12…11	00b = VCONN not required	Cable Termination Type
B10…9	00b = 20V	Maximum VBUS Voltage
B8…7	00b	***Reserved***
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4…3	00b	***Reserved***
B2…0	010b = [USB 3.2] Gen1 and Gen2	SuperSpeed USB Signaling Support

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.2 TBT3 Active Cable Discover Identity Responses

Table F-4, along with Table F-5, Table F-6 and Table F-7, defines the expected Discover Identity VDO responses for a TBT3 active cable. In fields where multiple values are listed, cable responses may vary to match the specific connected cable's capabilities.

Table F-4 TBT3 Active Cable Discover Identity VDO Responses

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	5…6	0…7	1 = Cable Plug		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00001b

Bit(s)	Value	Parameter
ID Header VDO		
B31	0	USB Communications Capable as USB Host
B30	0	USB Communications Capable as a USB Device
B29…27	100b = Active Cable	Product Type (Cable Plug)
B26	1 = Modal Operation Supported	Modal Operation Supported
B25…23	000b	Product Type (DFP)
B22…16	0	***Reserved***
B15…0	Per vendor	USB Vendor ID
Cert Stat VDO		
B31…0	0x00000000…0xFFFFFFFF	XID assigned by USB-IF
Product VDO		
B31…16	0x0000…0xFFFF	USB Product ID
B15…0	0x0000…0xFFFF	bcdDevice
Active Cable VDO 1		
Depending on USB PD Specification Revision: See Table F-5 for USB PD Revision 2.0 or Table F-6 for USB PD Revision 3.0		
Active Cable VDO 2		
Applicable only for USB PD Revision 3.0 – See Table F-7		

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.2 TBT3 主动电缆发现身份响应

表 F-4 以及表 F-5、表 F-6 和表 F-7 定义了 TBT3 有源电缆的预期 Discover Identity VDO 响应。在列出多个值的字段中，电缆响应可能会有所不同，以匹配特定连接电缆的功能。

表 F-4 TBT3 主动电缆发现身份 VDO 响应

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	5…6	0…7	1 = Cable Plug		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00001b

Bit(s)	Value	Parameter
ID Header VDO		
B31	0	USB Communications Capable as USB Host
B30	0	USB Communications Capable as a USB Device
B29…27	100b = Active Cable	Product Type (Cable Plug)
B26	1 = Modal Operation Supported	Modal Operation Supported
B25…23	000b	Product Type (DFP)
B22…16	0	***Reserved***
B15…0	Per vendor	USB Vendor ID
Cert Stat VDO		
B31…0	0x00000000…0xFFFFFFFF	XID assigned by USB-IF
Product VDO		
B31…16	0x0000…0xFFFF	USB Product ID
B15…0	0x0000…0xFFFF	bcdDevice
Active Cable VDO 1		
Depending on USB PD Specification Revision: See Table F-5 for USB PD Revision 2.0 or Table F-6 for USB PD Revision 3.0		
Active Cable VDO 2		
Applicable only for USB PD Revision 3.0 – See Table F-7		

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table F-5 TBT3 Active Cable VDO for USB PD Revision 2.0, Version 1.3

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	0001b – <10ns (~1m)	Cable Latency
B12…11	11b = Both ends Active, VCONN required	Cable Termination Type
B10	0 = Fixed	SSTX1 Directionality Support
B9	0 = Fixed 1= Configurable	SSTX2 Directionality Support
B8	0 = Fixed 1 = Configurable	SSRX1 Directionality Support
B7	0 = Fixed 1 = Configurable	SSRX2 Directionality Support
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4	1 = Yes	VBUS through cable
B3	0 = No 1 = Yes	SOP' controller present
B2…0	010b = [USB 3.1] Gen1 and Gen2	SuperSpeed USB Signaling Support

Table F-6 TBT3 Active Cable VDO 1 for USB PD Revision 3.0, Version 1.2

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…21	010b = Version 1.2	VDO Version
B20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	xxxxb (e.g., 0010b – 10ns to 20ns (~2m))	Cable Latency
B12…11	11b = Both ends Active, VCONN required	Cable Termination Type
B10…9	00b = 20V	Maximum VBUS Voltage
B8	1 = Yes	SBU Supported
B7	0 = Passive 1 = Active	SBU Type
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4	0 = No 1 = Yes	VBUS through cable
B3	0 = No 1= Yes	SOP' controller present
B2…0	010b = [USB 3.2] Gen1 and Gen2	SuperSpeed USB Signaling Support

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 F-5 USB PD 修订版 2.0、版本 1.3 的 TBT3 有源电缆 VDO

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	0001b – <10ns (~1m)	Cable Latency
B12…11	11b = Both ends Active, VCONN required	Cable Termination Type
B10	0 = Fixed	SSTX1 Directionality Support
B9	0 = Fixed 1= Configurable	SSTX2 Directionality Support
B8	0 = Fixed 1 = Configurable	SSRX1 Directionality Support
B7	0 = Fixed 1 = Configurable	SSRX2 Directionality Support
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4	1 = Yes	VBUS through cable
B3	0 = No 1 = Yes	SOP' controller present
B2…0	010b = [USB 3.1] Gen1 and Gen2	SuperSpeed USB Signaling Support

表 F-6 USB PD 修订版 3.0、版本 1.2 的 TBT3 有源电缆 VDO 1

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…21	010b = Version 1.2	VDO Version
B20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	xxxxb (e.g., 0010b – 10ns to 20ns (~2m))	Cable Latency
B12…11	11b = Both ends Active, VCONN required	Cable Termination Type
B10…9	00b = 20V	Maximum VBUS Voltage
B8	1 = Yes	SBU Supported
B7	0 = Passive 1 = Active	SBU Type
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4	0 = No 1 = Yes	VBUS through cable
B3	0 = No 1= Yes	SOP' controller present
B2…0	010b = [USB 3.2] Gen1 and Gen2	SuperSpeed USB Signaling Support

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

Table F-7 TBT3 Active Cable VDO 2 for USB PD Revision 3.0, Version 1.2

Bit(s)	Value	Parameter
B31…24	xxxxxxxxb (e.g., 10101010b = 170 °C)	Maximum Operating Temperature
B23…16	xxxxxxxxb (e.g., 11010010b = 210 °C)	Shutdown Temperature
B15	0	***Reserved***
B14…12	000b ≥ 10 mW	U3 Power
B11	0	U3 to U0 Transition mode
B10…8	000b	***Reserved***
B7…6	00b	USB 2.0 Hub Hops Consumed
B5	0 = Supported	USB 2.0 Supported
B4	0 = Supported	SuperSpeed Supported
B3	1 = two lanes	SuperSpeed Lanes Supported
B2	0	***Reserved***
B1…0	00b = Gen1 01b = Gen2	SuperSpeed Signaling

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

表 F-7 适用于 USB PD 修订版 3.0、版本 1.2 的 TBT3 有源电缆 VDO 2

Bit(s)	Value	Parameter
B31…24	xxxxxxxxb (e.g., 10101010b = 170 °C)	Maximum Operating Temperature
B23…16	xxxxxxxxb (e.g., 11010010b = 210 °C)	Shutdown Temperature
B15	0	***Reserved***
B14…12	000b ≥ 10 mW	U3 Power
B11	0	U3 to U0 Transition mode
B10…8	000b	***Reserved***
B7…6	00b	USB 2.0 Hub Hops Consumed
B5	0 = Supported	USB 2.0 Supported
B4	0 = Supported	SuperSpeed Supported
B3	1 = two lanes	SuperSpeed Lanes Supported
B2	0	***Reserved***
B1…0	00b = Gen1 01b = Gen2	SuperSpeed Signaling

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.3 TBT3 Device Discover Identity Responses

Table F-8 defines the expected Discover Identity VDO responses for a TBT3 device. In fields where multiple values are listed, device responses may vary to match the specific connected device's capabilities.

Table F-8 TBT3 Device Discover Identity VDO Responses

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	4	0…7	0 = UFP		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00001b

Bit(s)	Value	Parameter
ID Header VDO		
B31	0 or 1	USB Communications Capable as USB Host
B30	0 or 1	USB Communications Capable as a USB Device
B29…27	001b = PDUSB Hub 010b = PDUSB Peripheral 101b = Alternate Mode Adapter (AMA) 110b = VCONN-Powered USB Device (VPD)	Product Type (UFP)
B26	1 = Modal Operation Supported	Modal Operation Supported
B25…23	001b = PDUSB Hub 010b = PDUSB Host 100b = Alternate Mode Controller (AMC)	Product Type (DFP)
B22…16	0	***Reserved***
B15…0	Per vendor	USB Vendor ID
Cert Stat VDO		
B31…0	0x00000000…0xFFFFFFFF	XID assigned by USB-IF
Product VDO		
B31…16	0x0000…0xFFFF	USB Product ID
B15…0	0x0000…0xFFFF	bcdDevice

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.3 TBT3 设备发现身份响应

表 F-8 定义了 TBT3 设备的预期 Discover Identity VDO 响应。在列出多个值的字段中，设备响应可能会有所不同，以匹配特定连接设备的功能。

表 F-8 TBT3 设备发现身份 VDO 响应

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	4	0…7	0 = UFP		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00001b

Bit(s)	Value	Parameter
ID Header VDO		
B31	0 or 1	USB Communications Capable as USB Host
B30	0 or 1	USB Communications Capable as a USB Device
B29…27	001b = PDUSB Hub 010b = PDUSB Peripheral 101b = Alternate Mode Adapter (AMA) 110b = VCONN-Powered USB Device (VPD)	Product Type (UFP)
B26	1 = Modal Operation Supported	Modal Operation Supported
B25…23	001b = PDUSB Hub 010b = PDUSB Host 100b = Alternate Mode Controller (AMC)	Product Type (DFP)
B22…16	0	***Reserved***
B15…0	Per vendor	USB Vendor ID
Cert Stat VDO		
B31…0	0x00000000…0xFFFFFFFF	XID assigned by USB-IF
Product VDO		
B31…16	0x0000…0xFFFF	USB Product ID
B15…0	0x0000…0xFFFF	bcdDevice

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.4 TBT3 Discover SVID Responses

Table F-9 defines the expected Discover SVID VDO responses for a TBT3 device or cable.

Table F-9 TBT3 Discover SVID VDO Responses

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	3	0…7	0 = UFP		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00010b

Bit(s)	Value	Parameter
VDO 1		
B31…16	0x8087 = Intel/TBT3	SVID 0
B15…0	0xFF01 = VESA DP (if supported)	SVID 1
VDO 2		
B31…16	0x0000 – 0xFFFF (normally the cable manufacturer VID)	SVID 2
B15…0	0x0000 (normally)	SVID 3

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.4 TBT3 发现 SVID 响应

表 F-9 定义了 TBT3 设备或电缆的预期 Discover SVID VDO 响应。

表 F-9 TBT3 发现 SVID VDO 响应

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	3	0…7	0 = UFP		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00010b

Bit(s)	Value	Parameter
VDO 1		
B31…16	0x8087 = Intel/TBT3	SVID 0
B15…0	0xFF01 = VESA DP (if supported)	SVID 1
VDO 2		
B31…16	0x0000 – 0xFFFF (normally the cable manufacturer VID)	SVID 2
B15…0	0x0000 (normally)	SVID 3

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.5 TBT3 Device Discover Mode Responses

Table F-10 defines the expected Discover Mode VDO responses for a TBT3 device. In fields where multiple values are listed, device responses may vary to match the specific connected device's capabilities.

Table F-10 TBT3 Device Discover Mode VDO Responses

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	2	0…7	0 = UFP		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	001b	0	00011b

Bit(s)	Value	Parameter
TBT3 SOP VDO		
B31	0 = Not supported 1 = Supported	Vendor specific B1
B30	0 = Not supported 1 = Supported	Vendor specific B0
B29…27	000b	***Reserved***
B26	0 = Not supported 1 = Supported	Intel specific B0
B25…17	000000000b	***Reserved***
B16	0b = TBT2 Legacy Adapter 1b = TBT3 Adapter	TBT Adapter
B15…0	0x0001 = TBT Mode	TBT Alternate Mode

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.5 TBT3 设备发现模式响应

表 F-10 定义了 TBT3 设备的预期发现模式 VDO 响应。在列出多个值的字段中，设备响应可能会有所不同，以匹配特定连接设备的功能。

表 F-10 TBT3 设备发现模式 VDO 响应

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	2	0…7	0 = UFP		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	001b	0	00011b

Bit(s)	Value	Parameter
TBT3 SOP VDO		
B31	0 = Not supported 1 = Supported	Vendor specific B1
B30	0 = Not supported 1 = Supported	Vendor specific B0
B29…27	000b	***Reserved***
B26	0 = Not supported 1 = Supported	Intel specific B0
B25…17	000000000b	***Reserved***
B16	0b = TBT2 Legacy Adapter 1b = TBT3 Adapter	TBT Adapter
B15…0	0x0001 = TBT Mode	TBT Alternate Mode

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.6 TBT3 Cable Discover Mode Responses

Table F-11 defines the expected Discover Mode VDO responses for a TBT3 cable. In fields where multiple values are listed, cable responses may vary to match the specific connected cable's capabilities.

Table F-11 TBT3 Cable Discover Mode VDO Responses

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	2	0…7	1 = Cable Plug		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	001b	0	00011b

Bit(s)	Value	Parameter
TBT3 SOP' VDO		
B31…24	00000000b	***Reserved***
B23	0 = Active with bi-directional LSRX[1] communication or when Passive 1 = Active with uni-directional LSRX[1] communication	Active Cable Plug Link Training
B22	0 = Not re-timer 1 = Re-timer	Re-timer
B21	0b = Non-Optical 1b = Optical	Cable Type
B20…19	00b = 3rd Gen Non-Rounded TBT 01b = 3rd & 4th Gen Rounded and Non-Rounded TBT 10b…11b = Reserved	TBT_Rounded_Support
B18…16	000b = Reserved 001b = USB3.1 Gen1 Cable (10 Gbps TBT support) 010b = 10 Gbps (USB 3.2 Gen1 and Gen2 passive cables) 011b = 10 Gbps and 20 Gbps (TBT 3rd Gen active cables and 20 Gbps passive cables) 100b…111b = Reserved	Cable Speed
B15…0	0x0001 = TBT Mode	TBT Alternate Mode

Notes:
1. LSRX in TBT3 is the same communication channel as SBRX in USB4.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.6 TBT3 电缆发现模式响应

表 F-11 定义了 TBT3 电缆的预期发现模式 VDO 响应。在列出多个值的字段中，电缆响应可能会有所不同，以匹配特定连接电缆的功能。

表 F-11 TBT3 电缆发现模式 VDO 响应

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	2	0…7	1 = Cable Plug		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	001b	0	00011b

Bit(s)	Value	Parameter
TBT3 SOP' VDO		
B31…24	00000000b	***Reserved***
B23	0 = Active with bi-directional LSRX[1] communication or when Passive 1 = Active with uni-directional LSRX[1] communication	Active Cable Plug Link Training
B22	0 = Not re-timer 1 = Re-timer	Re-timer
B21	0b = Non-Optical 1b = Optical	Cable Type
B20…19	00b = 3rd Gen Non-Rounded TBT 01b = 3rd & 4th Gen Rounded and Non-Rounded TBT 10b…11b = Reserved	TBT_Rounded_Support
B18…16	000b = Reserved 001b = USB3.1 Gen1 Cable (10 Gbps TBT support) 010b = 10 Gbps (USB 3.2 Gen1 and Gen2 passive cables) 011b = 10 Gbps and 20 Gbps (TBT 3rd Gen active cables and 20 Gbps passive cables) 100b…111b = Reserved	Cable Speed
B15…0	0x0001 = TBT Mode	TBT Alternate Mode

注意：1. TBT3 中的 LSRX 与 USB4 中的 SBRX 是相同的通信通道。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.7 TBT3 Cable Enter Mode Command

Table F-12 defines the Enter Mode Command that shall be sent to the SOP' (and if needed the SOP") of an active TBT3 cable to enable the cable for TBT3 operation.

Table F-12 TBT3 Cable Enter Mode Command

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	1	0…7	1 = Cable Plug		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	000b	0	00100b

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.7 TBT3 电缆进入模式命令

表 F-12 定义了应发送到活动 TBT3 电缆的 SOP ’（如果需要，还有 SOP ”）的进入模式命令，以使电缆能够进行 TBT3 操作。

表 F-12 TBT3 电缆进入模式命令

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	1	0…7	1 = Cable Plug		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	000b	0	00100b

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.8 TBT3 Device Enter Mode Command

Table F-13 defines the Enter Mode Command that shall be sent to the SOP of a TBT3 device to enable the device for TBT3 operation.

Table F-13 TBT3 Device Enter Mode Command

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	2	0…7	0 = UFP		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	000b	0	00100b

Bit(s)	Value	Parameter
TBT3 SOP VDO		
B31	0 = Not supported 1 = Supported	Vendor specific B1
B30	0 = Not supported 1 = Supported	Vendor specific B0
B29…27	000b	***Reserved***
B26	0 = Not supported 1 = Supported	Intel specific B0
B25	0b	***Reserved***
B24	0 = Passive cable 1= Active cable	Active_Passive
B23	0 = Active with bi-directional LSRX[1] communication or when Passive 1 = Active with uni-directional LSRX[1] communication	Active Cable Link Training
B22	0 = Not re-timer 1 = Re-timer	Re-timer
B21	0b = Non-Optical 1b = Optical	Cable Type
B20…19	00b = 3rd Gen Non-Rounded TBT 01b = 3rd & 4th Gen Rounded and Non-Rounded TBT 10b…11b = Reserved	TBT_Rounded_Support
B18…16	000b = Reserved 001b = USB3.1 Gen1 Cable (10 Gbps TBT support) 010b = 10 Gbps (USB 3.2 Gen1 and Gen2 passive cables) 011b = 10 Gbps and 20 Gbps (TBT 3rd Gen active cables and 20 Gbps passive cables) 100b…111b = Reserved	Cable Speed
B15…0	0x0001 = TBT Mode	TBT Alternate Mode

Notes:
1. LSRX in TBT3 is the same communication channel as SBRX in USB4.

The values to be used when sending the TBT3 Device Enter Mode command to the SOP of a TBT3 device are determined based on information retained from earlier in the discovery flow as follows:

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

F.2.8 TBT3 设备进入模式命令

表 F-13 定义了应发送到 TBT3 设备的 SOP 的进入模式命令，以启用该设备进行 TBT3 操作。

表 F-13 TBT3 设备进入模式命令

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	2	0…7	0 = UFP		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	000b	0	00100b

Bit(s)	Value	Parameter
TBT3 SOP VDO		
B31	0 = Not supported 1 = Supported	Vendor specific B1
B30	0 = Not supported 1 = Supported	Vendor specific B0
B29…27	000b	***Reserved***
B26	0 = Not supported 1 = Supported	Intel specific B0
B25	0b	***Reserved***
B24	0 = Passive cable 1= Active cable	Active_Passive
B23	0 = Active with bi-directional LSRX[1] communication or when Passive 1 = Active with uni-directional LSRX[1] communication	Active Cable Link Training
B22	0 = Not re-timer 1 = Re-timer	Re-timer
B21	0b = Non-Optical 1b = Optical	Cable Type
B20…19	00b = 3rd Gen Non-Rounded TBT 01b = 3rd & 4th Gen Rounded and Non-Rounded TBT 10b…11b = Reserved	TBT_Rounded_Support
B18…16	000b = Reserved 001b = USB3.1 Gen1 Cable (10 Gbps TBT support) 010b = 10 Gbps (USB 3.2 Gen1 and Gen2 passive cables) 011b = 10 Gbps and 20 Gbps (TBT 3rd Gen active cables and 20 Gbps passive cables) 100b…111b = Reserved	Cable Speed
B15…0	0x0001 = TBT Mode	TBT Alternate Mode

注意：1. TBT3 中的 LSRX 与 USB4 中的 SBRX 是相同的通信通道。

向 TBT3 设备的 SOP 发送 TBT3 设备进入模式命令时使用的值是根据发现流程中先前保留的信息确定的，如下所示：

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

- B31 and B30: return the values received in the B31 and B30 fields of the TBT3 Device Discover Mode Response.
- B26: return the value received in the B26 field of the TBT3 Device Discover Mode Response.
- B23: if using a TBT3 cable, return the value received in the B23 field of the TBT3 Cable Discover Mode Response, otherwise set to 0.
- B22: if using a TBT3 cable, return the value received in the B22 field of the TBT3 Cable Discover Mode Response, otherwise set to 0.
- B21: if using a TBT3 cable, return the value received in the B21 field of the TBT3 Cable Discover Mode Response, otherwise set to 0.
- B20…19: if using a TBT3 cable, return the value received in the B20…19 field of the TBT3 Cable Discover Mode Response, otherwise set to 00b.
- B18…16: if using a TBT3 cable, return the value received in the B18…16 field of the TBT3 Cable Discover Mode Response, otherwise set to 010b.

F.2.9 TBT3 Cable Functional Difference Summary

Table F-14 provides a summary of existing TBT3 cables and the unique functional differences between them.

Table F-14 TBT3 Cable Functional Difference Summary

Cable	Function					SOP' Configuration				
						ID Header VDO	Discover Mode (8087)			
	USB2	USB3	TBT3-Limit	USB4	DP	Passive/ Active B29…27	Re-timer B22	Uni/Bi Directional LSRX[1] B23	Rounded /none B20…19	Optical /none B21
Passive	Yes	Yes	Yes	Yes	Yes	011	0	N/A (0)	N/A (0)	0
TBT3 Re-timer	Yes	No	Legacy	No	No	100	1	0	00	0
Re-Timer	Yes	Yes	Yes	Yes	Yes	100	1	1	01	0
Re-Driver	Yes	Yes	Yes	Yes	Yes	100	0	1	01	0
Limit Optical	No	No	Yes No CLx No CC	No	No	100	0	1	00	1
Linear Optical Re-Driver	No	Yes	Yes	Yes	No	100	0	1	01	1

Notes:
1. LSRX in TBT3 is the same communication channel as SBRX in USB4.

Notes:

1. TBT3 Re-timer cables only supports TBT3 and does not support USB4 operation.
2. All other re-timer cables are as defined in Chapter 6.
3. Limit Optical cables are as defined in Chapter 6 as optically-isolated active cables.

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.

• B31 和 B30：返回在 TBT3 设备发现模式响应的 B31 和 B30 字段中收到的值。• B26：返回在 TBT3 设备发现模式响应的 B26 字段中收到的值。• B23：如果使用 TBT3 电缆，则返回在 TBT3 电缆发现模式响应的 B23 字段中收到的值，否则设置为 0。• B22：如果使用 TBT3 电缆，则返回在 TBT3 电缆发现模式响应的 B22 字段中收到的值，否则设置为 0。• B21：如果使用 TBT3 电缆，则返回在 TBT3 电缆发现模式响应的 B21 字段中收到的值，否则设置为 0。• B20…19：如果使用 TBT3 电缆，则返回在 TBT3 电缆发现模式响应的 B20…19 字段中收到的值，否则设置为 00b。 • B18…16：如果使用 TBT3 电缆，则返回 B18…16 字段中收到的值

TBT3 电缆发现模式响应，否则设置为 010b。

F.2.9 TBT3 电缆功能差异汇总

表 F-14 提供了现有 TBT3 电缆的摘要及其之间独特的功能差异。

表 F-14 TBT3 电缆功能差异汇总

Cable	Function					SOP' Configuration				
						ID Header VDO	Discover Mode (8087)			
	USB2	USB3	TBT3-Limit	USB4	DP	Passive/ Active B29…27	Re-timer B22	Uni/Bi Directional LSRX[1] B23	Rounded /none B20…19	Optical /none B21
Passive	Yes	Yes	Yes	Yes	Yes	011	0	N/A (0)	N/A (0)	0
TBT3 Re-timer	Yes	No	Legacy	No	No	100	1	0	00	0
Re-Timer	Yes	Yes	Yes	Yes	Yes	100	1	1	01	0
Re-Driver	Yes	Yes	Yes	Yes	Yes	100	0	1	01	0
Limit Optical	No	No	Yes No CLx No CC	No	No	100	0	1	00	1
Linear Optical Re-Driver	No	Yes	Yes	Yes	No	100	0	1	01	1

注意：1. TBT3 中的 LSRX 与 USB4 中的 SBRX 是相同的通信通道。

笔记：

1. TBT3 重定时器电缆仅支持 TBT3，不支持 USB4 操作。2. 所有其他重定时器电缆均如第 6 章中定义。3. 限制光缆如第 6 章中定义，为光隔离有源电缆。

Copyright © 2019 USB 3.0 Promoter Group. All rights reserved.