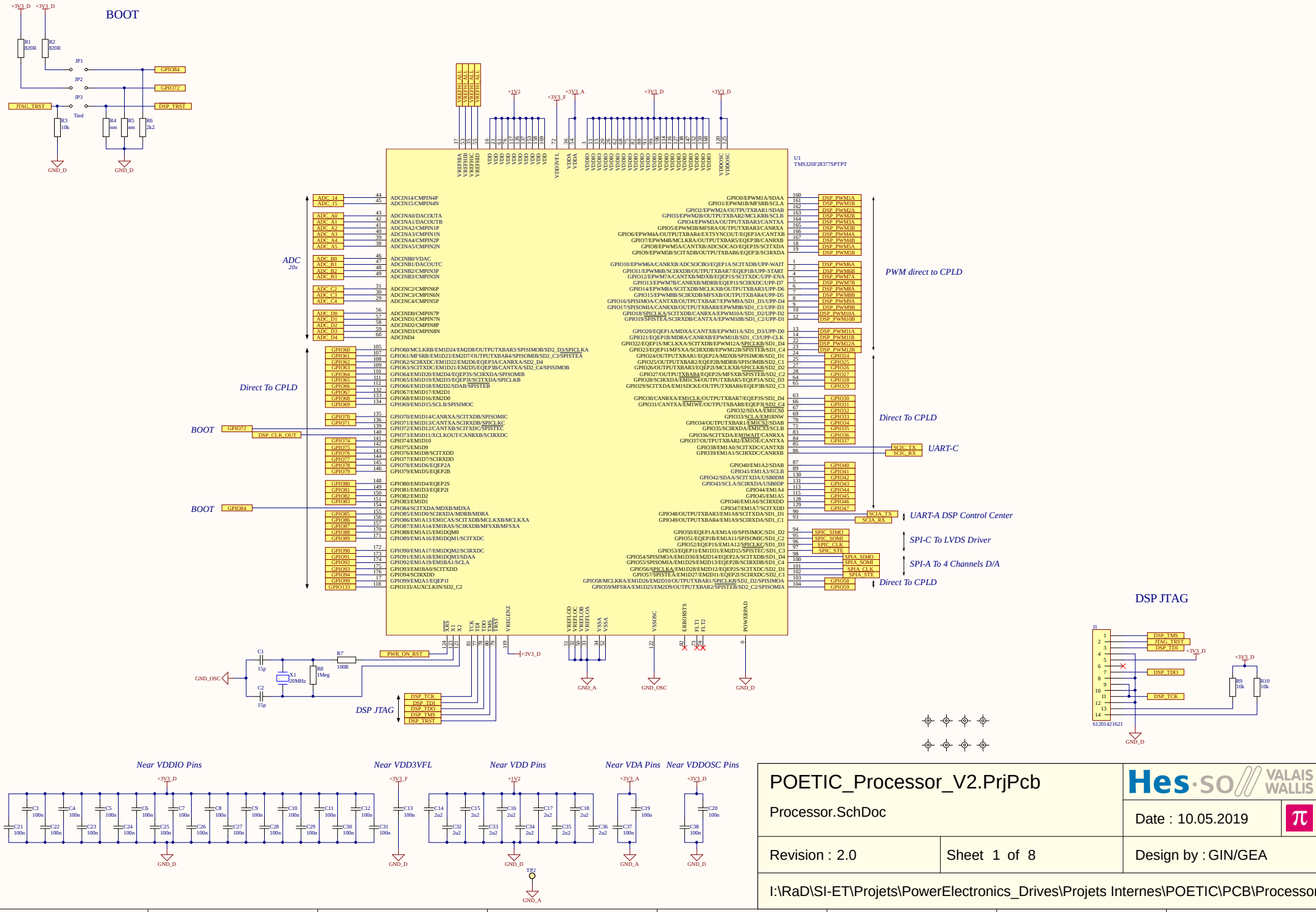

POETIC_Processor_V2.PrjPcb		Hes·SO VALAIS WALLIS
Processor.SchDoc		Date : 10.05.2019
Revision : 2.0	Sheet 1 of 8	Design by : GIN/GEA
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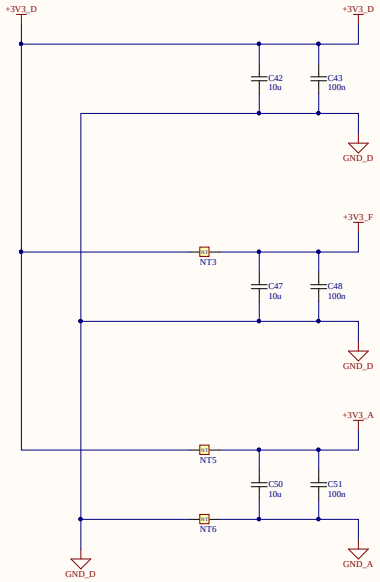
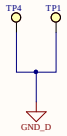
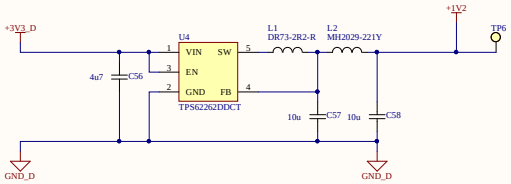
3V3 BackPlane ---------->3V3_D, 3V3_F, 3V3_A





3V3 D ---------->1V2

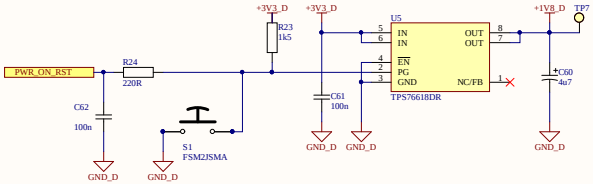
for F28 core



3V3 D ---------->1V8

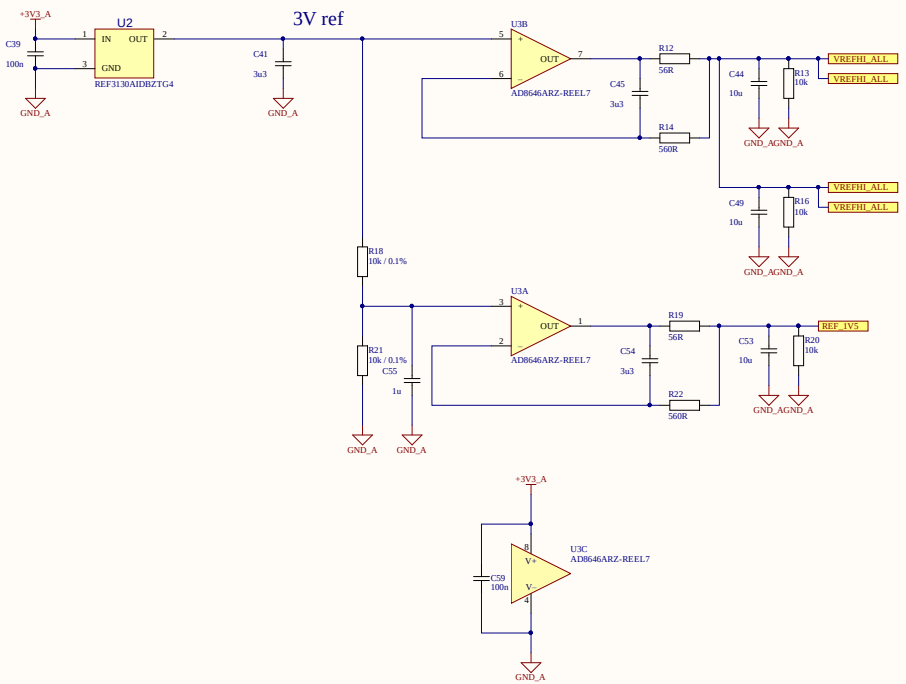
for XC2C core

3V3 / 1V8



3V AD Analog Voltage

fc = 100Hz



POETIC_Processor_V2.PrjPcb Supply.SchDoc		Hes·SO VALAIS WALLIS Date : 10.05.2019
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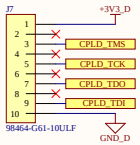
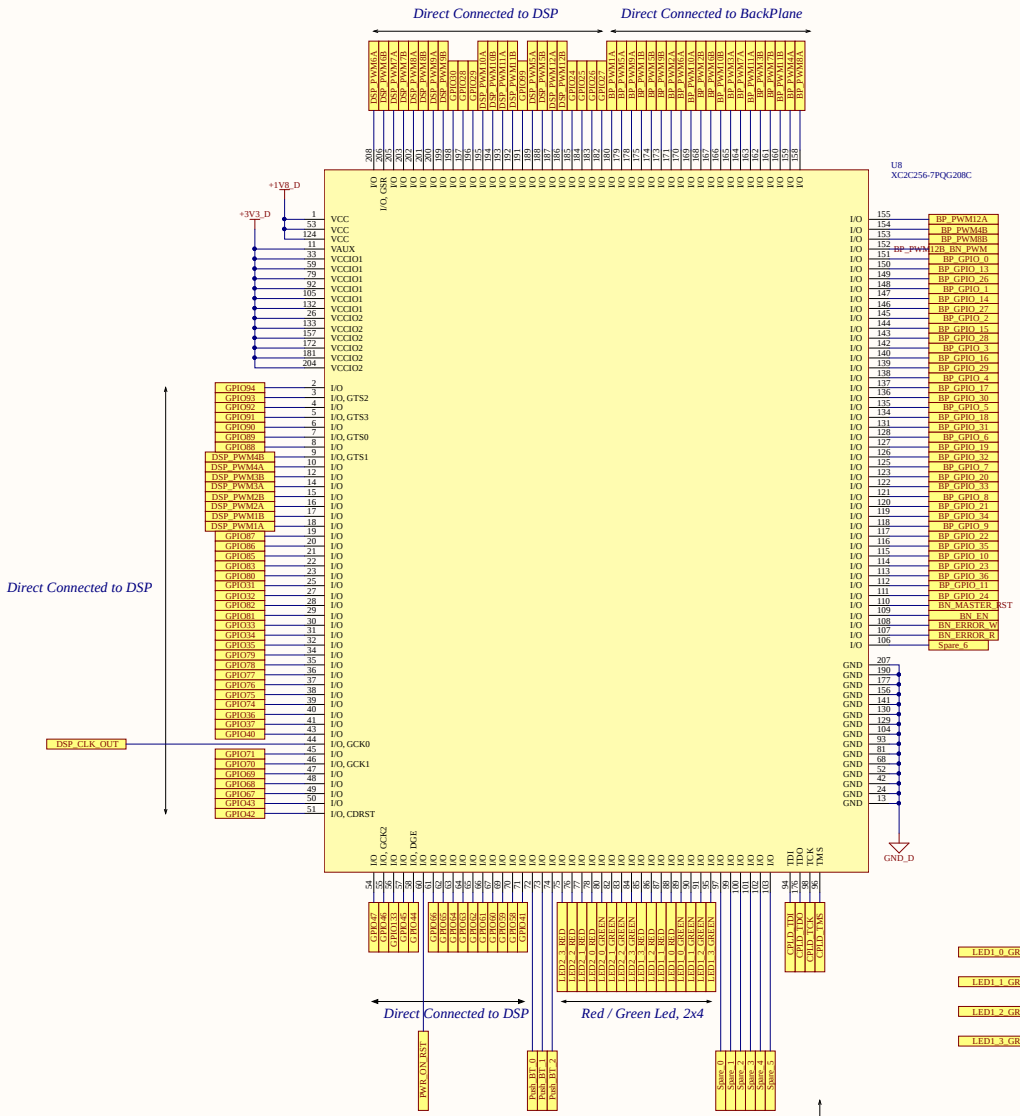
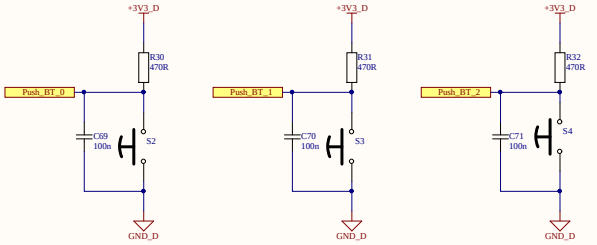
I:\RaD\SI-ET\Projets\PowerElectronics_Drives\Projets Internes\POETIC\PCB\Processor\POE		

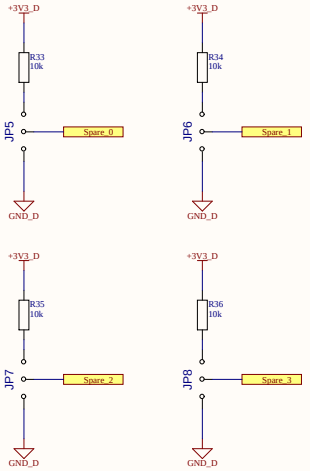
CPLD JTAG



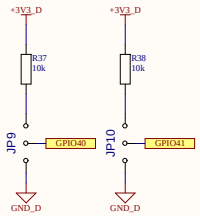




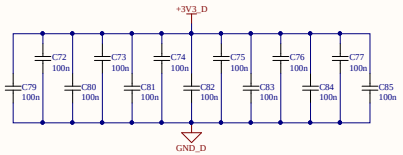
Jumper CPLD



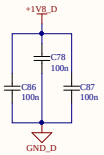
Jumper DSP---CPLD



Near VCCIO1, VCCIO2, VAUX Pins



Near VCC Pins



POETIC_Processor_V2.PrjPcb		Hes·SO VALAIS WALLIS
CPLD.SchDoc		Date : 10.05.2019
Revision : 2.0	Sheet 3 of 8	Design by : GIN/GEA
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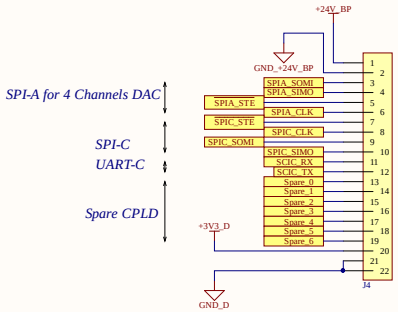
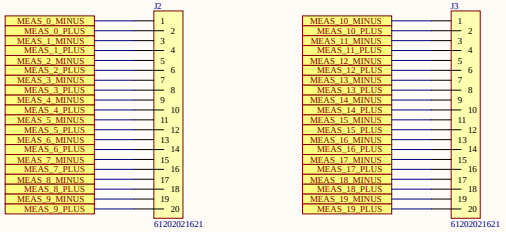
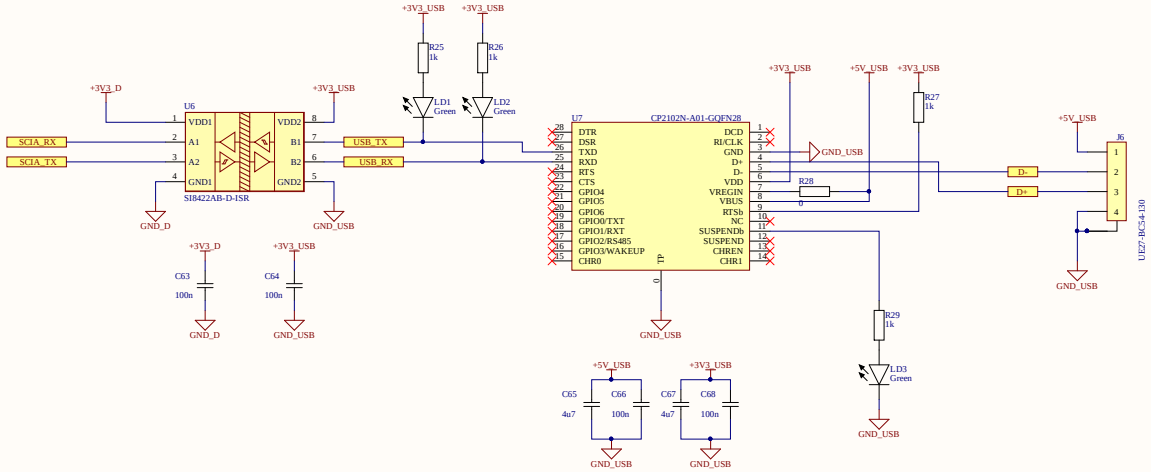
DSP to Mezzazzine board



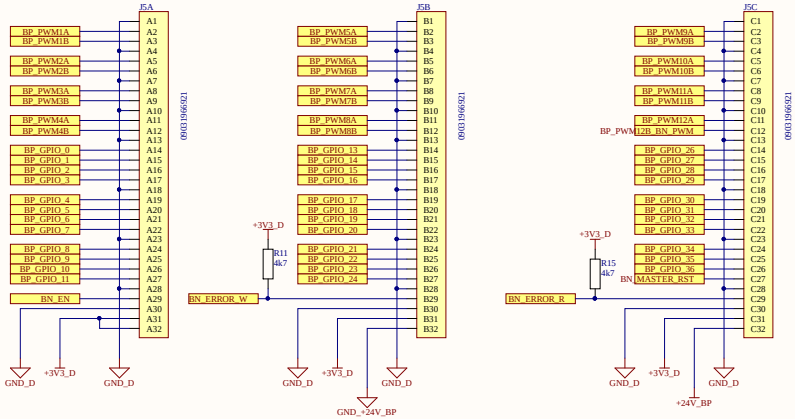
Connector for Analog Input Board



UART-A DSP Control Center



BackPlane Connector



POETIC_Processor_V2.PrjPcb Connector_0.SchDoc		Hes·SO VALAIS WALLIS Date : 10.05.2019
Revision : 2.0	Sheet 4 of 8	Design by : GIN/GEA
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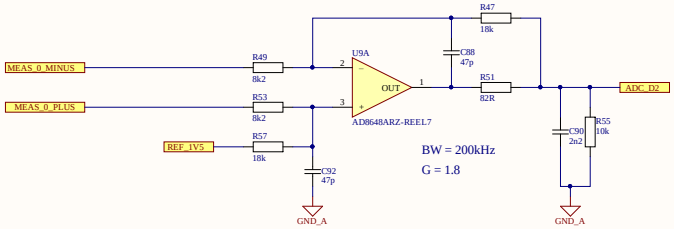

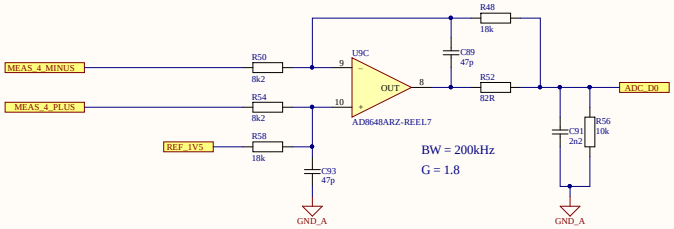

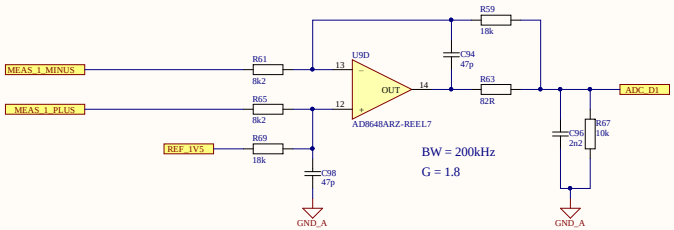

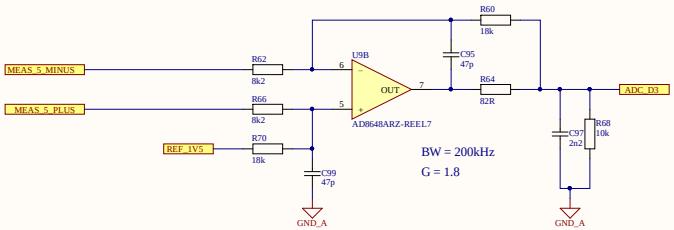

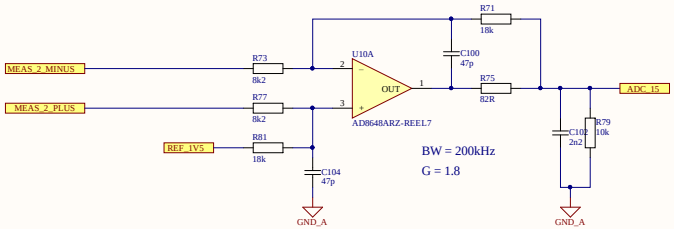

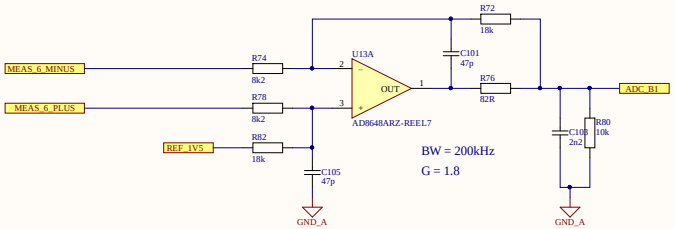

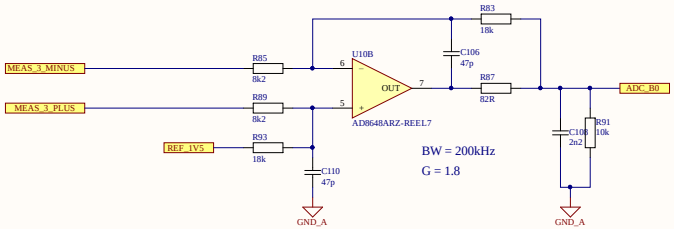

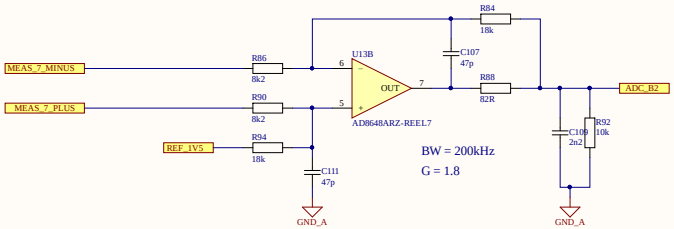

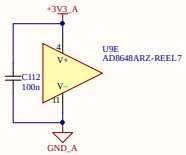

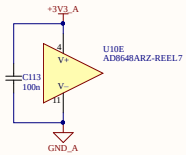

POETIC_Processor_V2.PrjPcb AD_0.SchDoc		Hes·SO VALAIS WALLIS Date : 10.05.2019
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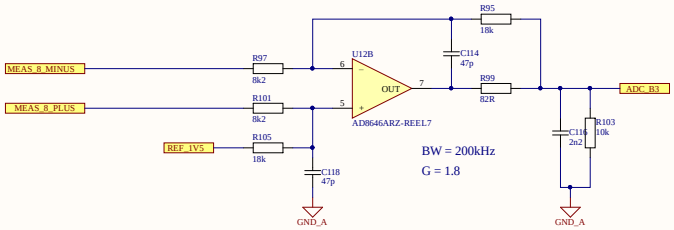
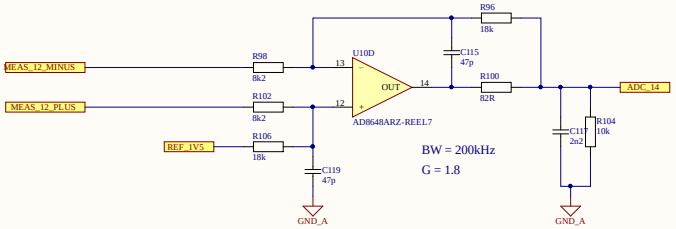
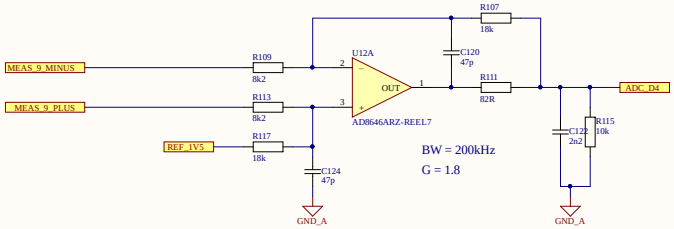
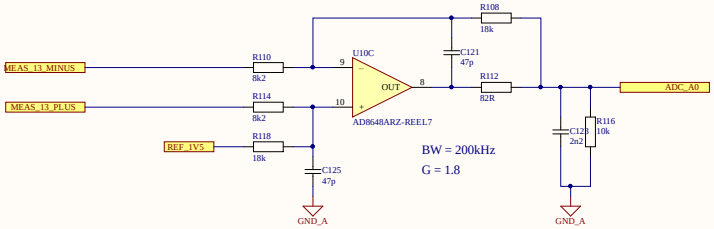
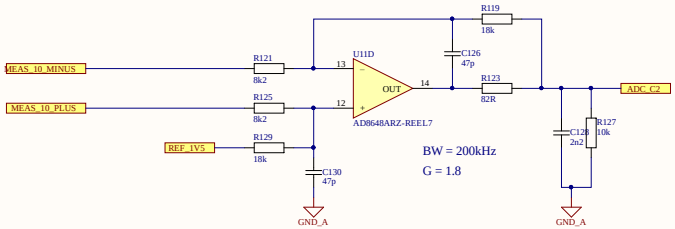
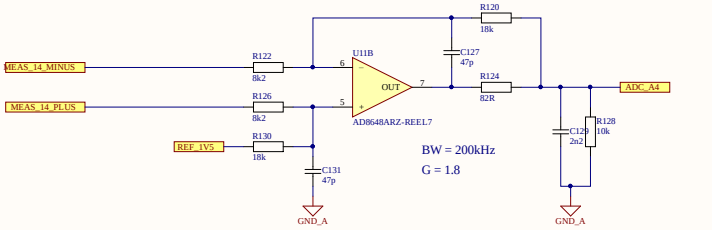


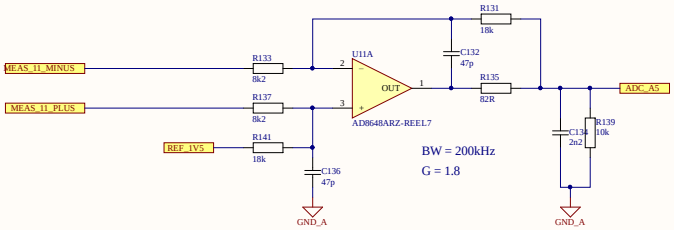


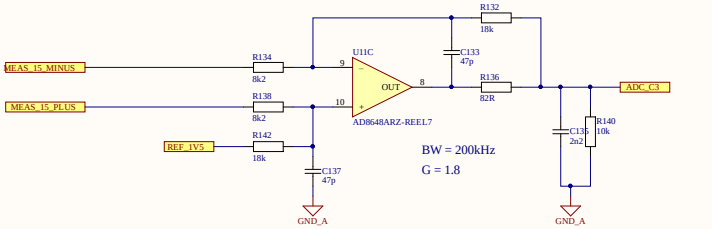


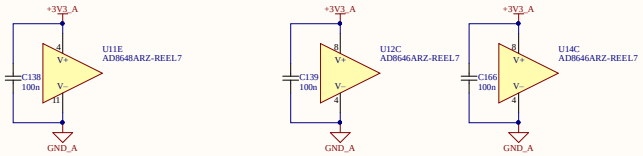




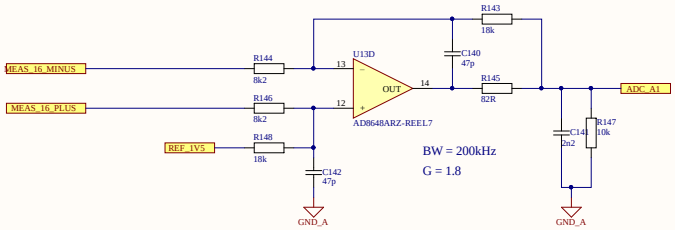


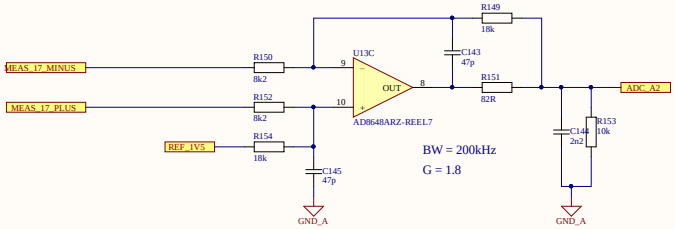


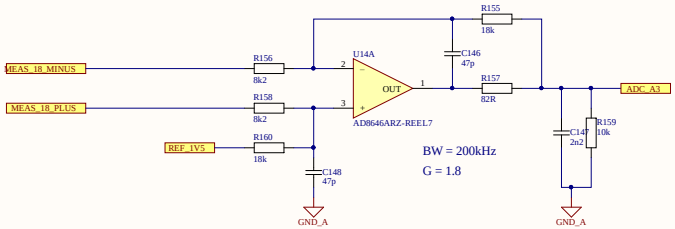


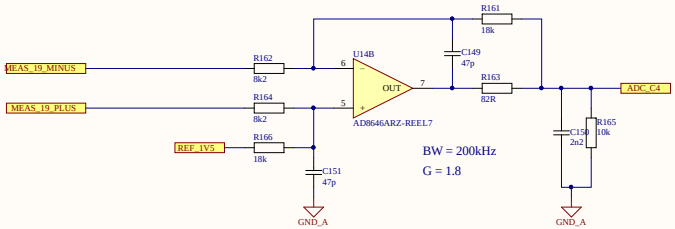


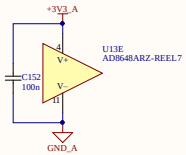
POETIC_Processor_V2.PrjPcb AD_1.SchDoc		Hes·SO VALAIS WALLIS Date : 10.05.2019
Revision : 2.0	Sheet 6 of 8	Design by : GIN/GEA
I:\RaD\SI-ET\Projets\PowerElectronics_Drives\Projets Internes\POETIC\PCB\Processor\POE		











POETIC_Processor_V2.PrjPcb AD_2.SchDoc		Hes·SO VALAIS WALLIS Date : 10.05.2019
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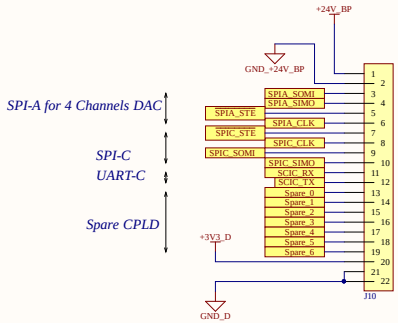
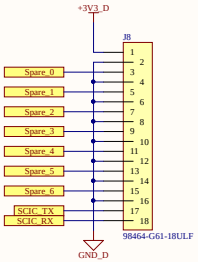
I:\RaD\SI-ET\Projets\PowerElectronics_Drives\Projets Internes\POETIC\PCB\Processor\POE		

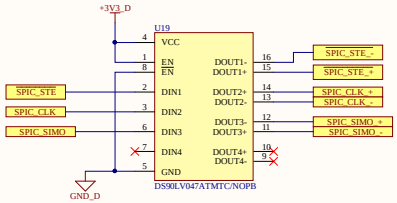
From DSP Board

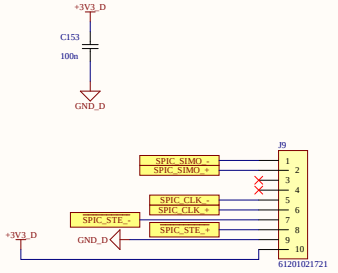


Spare connector



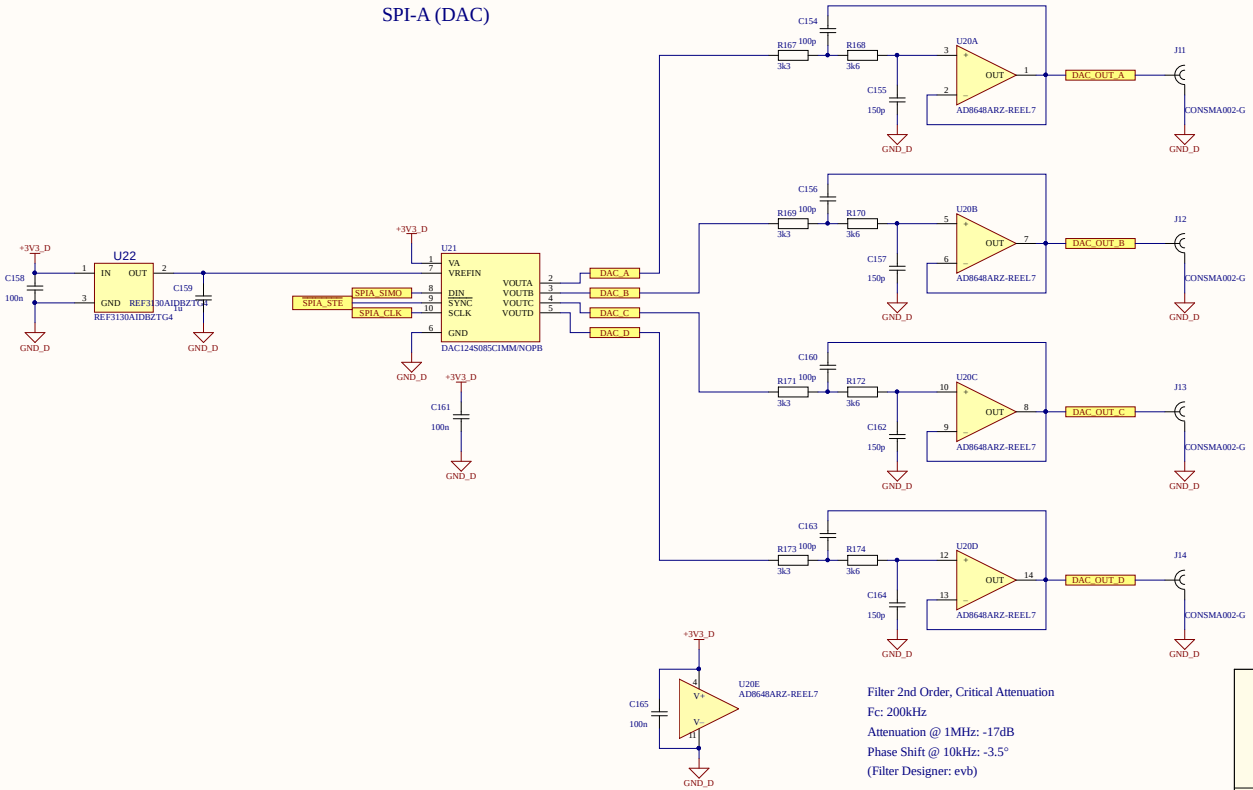
SPI-C with LVDS Driver





SPIOSOMI and LDAC not used for this application but already reserved

SPI-A (DAC)



POETIC_Processor_V2.PrjPcb Mezz_Board.SchDoc		Hes·SO VALAIS WALLIS Date : 10.05.2019
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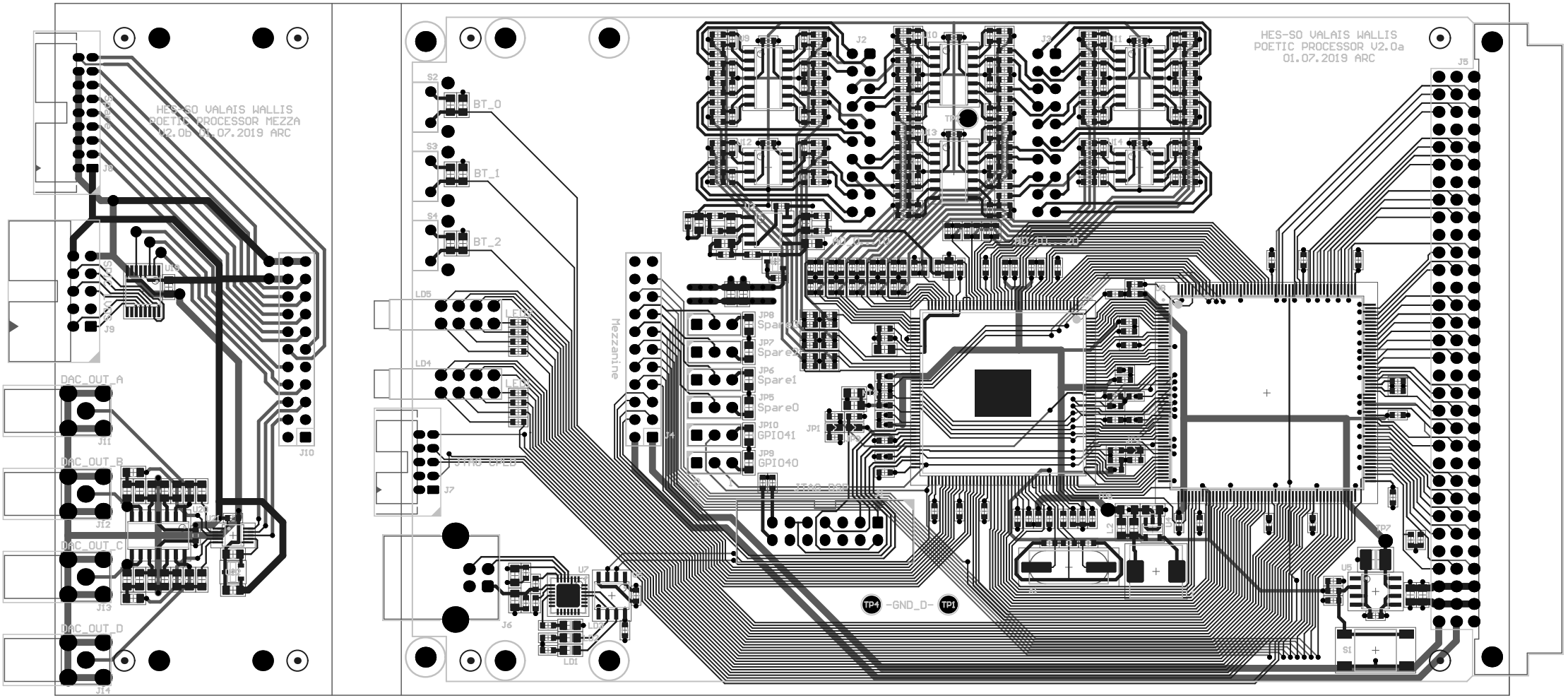
HES-SO VALAIS WALLIS
POETIC PROCESSOR MEZZA
V2.0b 01.07.2019 ARC
DAC_OUT_A
DAC_OUT_B
DAC_OUT_C
DAC_OUT_D
HES-SO VALAIS WALLIS
POETIC PROCESSOR V2.0a
01.07.2019 ARC
BT_0
BT_1
BT_2
Mezzanine
Spare2
Spare1
Spare0
GPIO41
GPIO40
-GND_D-

HES-SO VALAIS WALLIS
POETIC PROCESSOR U2.0a
01.07.2019 ARC
Mezzanine
GND_D
BT_2
BT_1
BT_0
GPIO40
GPIO41
SparE0
SparE1