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HEVs
Route du Rawyl 47
1950 Sion 2
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Zahno Silvan
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or
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FPGA_Rack Board : Rack-mounted Development FPGA platform

Page	Title	Description
1	Cover	This first page
2	Board	Shows Board connectivity
3	Power	3.3V 2.5V 1.8V 1.2V Regulation
4	FPGA Power	Xilinx Spartan 6 Power and Decoupling
5	FPGA 1	Xilinx Spartan 6 Bank 0 and 2 !!!!! Pay Attention on differences between LX45 and LX100
6	FPGA 2	Xilinx Spartan 6 Bank 1 and 3
7	FPGA Config	JTAG Connector / Reset Circuit / Done / Button / Leds
8	Memory	FLASH / SDRAM / Decoupling capacitors
9	Mezzanine	Mezza A and Mezza B Connectors (mezzanine support)
10	VME	VME Compatible Connector 96Pin
11	Ethernet	2 Ethernet Ports
12	UART	FTDI USB UART / UART

FPGA Rack
HES-SO // Valais Wallis
HAUTE ECOLE VALAISANNE

DES
REV
1/25

{Date}

V1.0

{Path}
FPGA_Rack_v1_0.sch

zas

Cover

1

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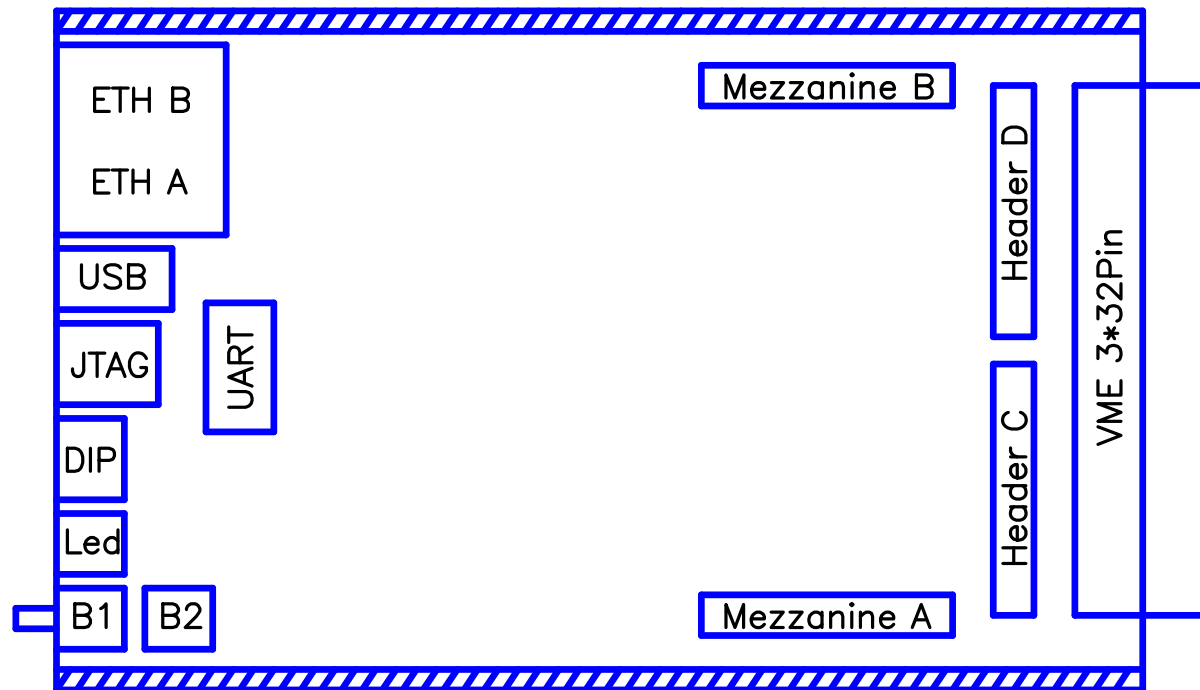
8

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FPGA Rack Connectivity

 = min. 3mm with no components for Rack insertion



FPGA Rack	DES	{Date}	zas
HES-SO // Valais Wallis	REV	V1.0	
HAUTE ECOLE VALAISANNE	2/25	{Path}	FPGA_Rack_v1_0.sch

Power supply

5V → From VME or USB
3.3V → From LTM4615 (1)
1.2V → From LTM4615 (2)
1.8V → From LTM4615 LDO
2.5V → From LDO

Layout Hints

- THERMAL_SW1 and THERMAL_SW2 Floating on separate copper planes
- Decoupling capacitors close to pins

LDO VOUT

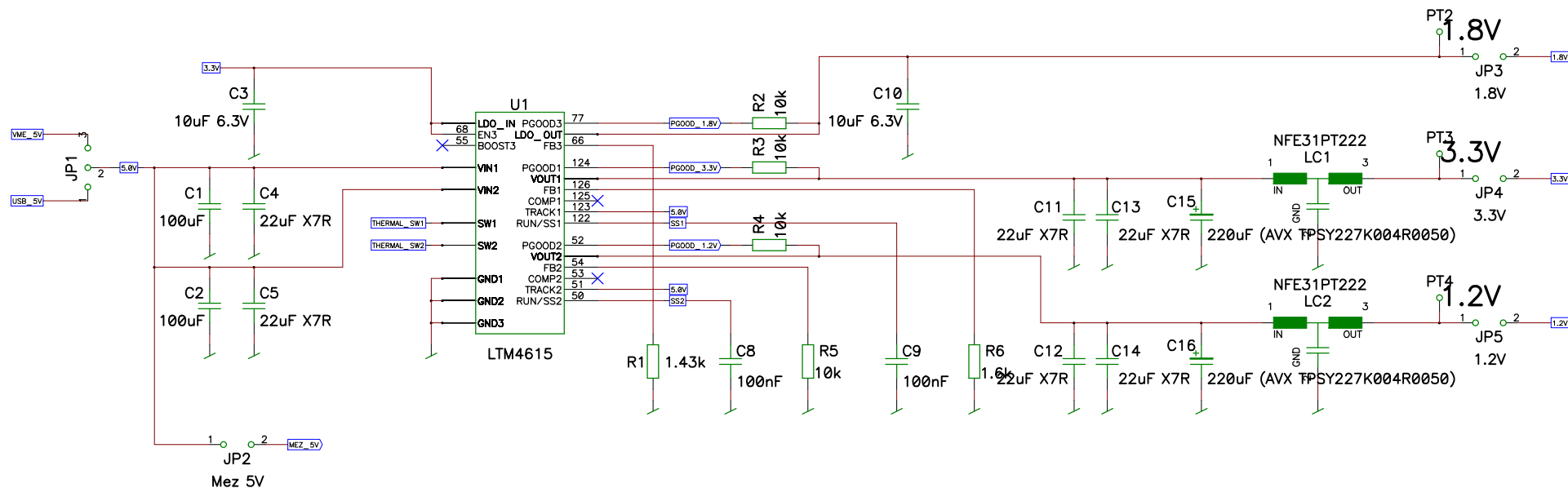
$$VLDO_OUT = 0.4V * (4.99k + RFB_LDO) / RFB_LDO$$

$$\rightarrow RFB_LDO = 1.996k / (VLDO_OUT - 0.4V)$$

$$RFB_LDO (Vout = 1.8V) = 1.996k / (1.8 - 0.4) = 1.42571k \rightarrow 1.43k \ 1\% \rightarrow 1.80563V$$

$$V_{OUT} = 0.8V * (4.99k + R_{FB}) / R_{FB}$$
$$\rightarrow R_{FB} = 3.992k / (V_{out} - 0.8)$$
$$\text{RFB (Vout = 3.3V)} = 3.992\text{k} / (3.3 - 0.8) = 1.5968\text{k} \rightarrow 1.6\text{k } 1\% \rightarrow 3.295\text{ V}$$
$$\text{RFB (Vout} = 1.2\text{V)} = 3.992\text{k} / (1.2 - 0.8) = 9.98\text{k} \rightarrow 10\text{k } 1\% \rightarrow 1.1992\text{ V}$$

3.3V @ 4A / 1.2V @ 4A / 1.8V @ 1.5A



2.5V @950mA



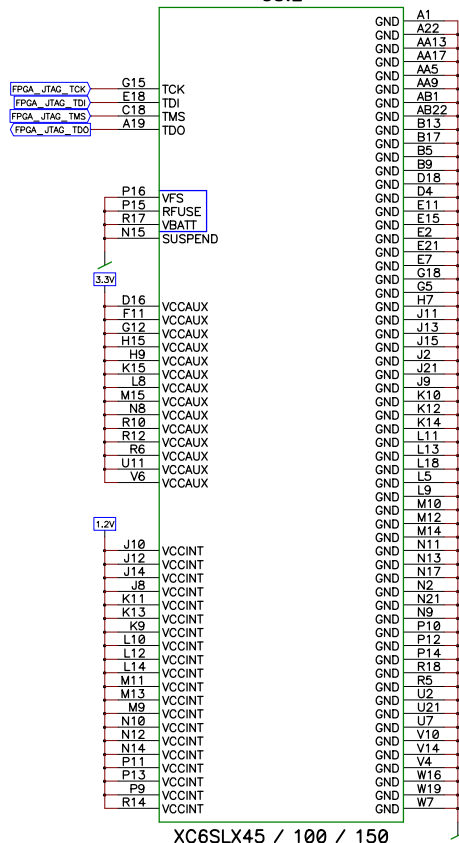
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HES—SO // Valais Wallis	REV	v1.0	
HAUTE ECOLE VALAISANNE	3/25	{Path}	FPGA_Rack_v1_0.sch

FPGA Power

Pins NOT AVAILABLE ON LX45
ONLY AVAILABLE ON LX100 / 150

- VFS
- RFUSE
- VBATT

U3:E



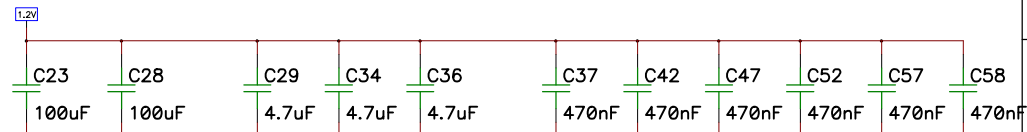
XC6SLX45 / 100 / 150

VCC0 Bank 3 Decoupling
LX45, LX100, LX150 -> 1x100uF / 1x4.7uF / 3x0.47uF

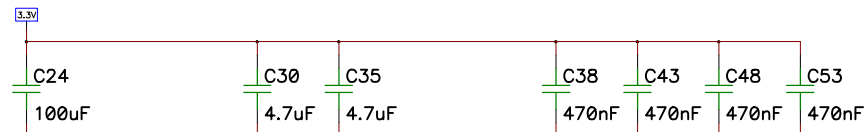


FPGA Decoupling

VCCINT Decoupling
LX45 -> 1x100uF / 1x4.7uF / 2x0.47uF
LX100 -> 1x100uF / 2x4.7uF / 4x0.47uF
LX150 -> 2x100uF / 3x4.7uF / 6x0.47uF



VCCAUX Decoupling
LX45, LX100, LX150 -> 1x100uF / 2x4.7uF / 4x0.47uF



VCC0 Bank 0 Decoupling
LX45, LX100, LX150 -> 1x100uF / 1x4.7uF / 2x0.47uF



VCC0 Bank 1 Decoupling
LX45, LX100, LX150 -> 1x100uF / 1x4.7uF / 3x0.47uF



VCC0 Bank 2 Decoupling
LX45 -> 1x100uF / 1x4.7uF / 4x0.47uF
LX100, LX150 -> 1x100uF / 1x4.7uF / 3x0.47uF



FPGA Rack
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HAUTE ECOLE VALAISANNE

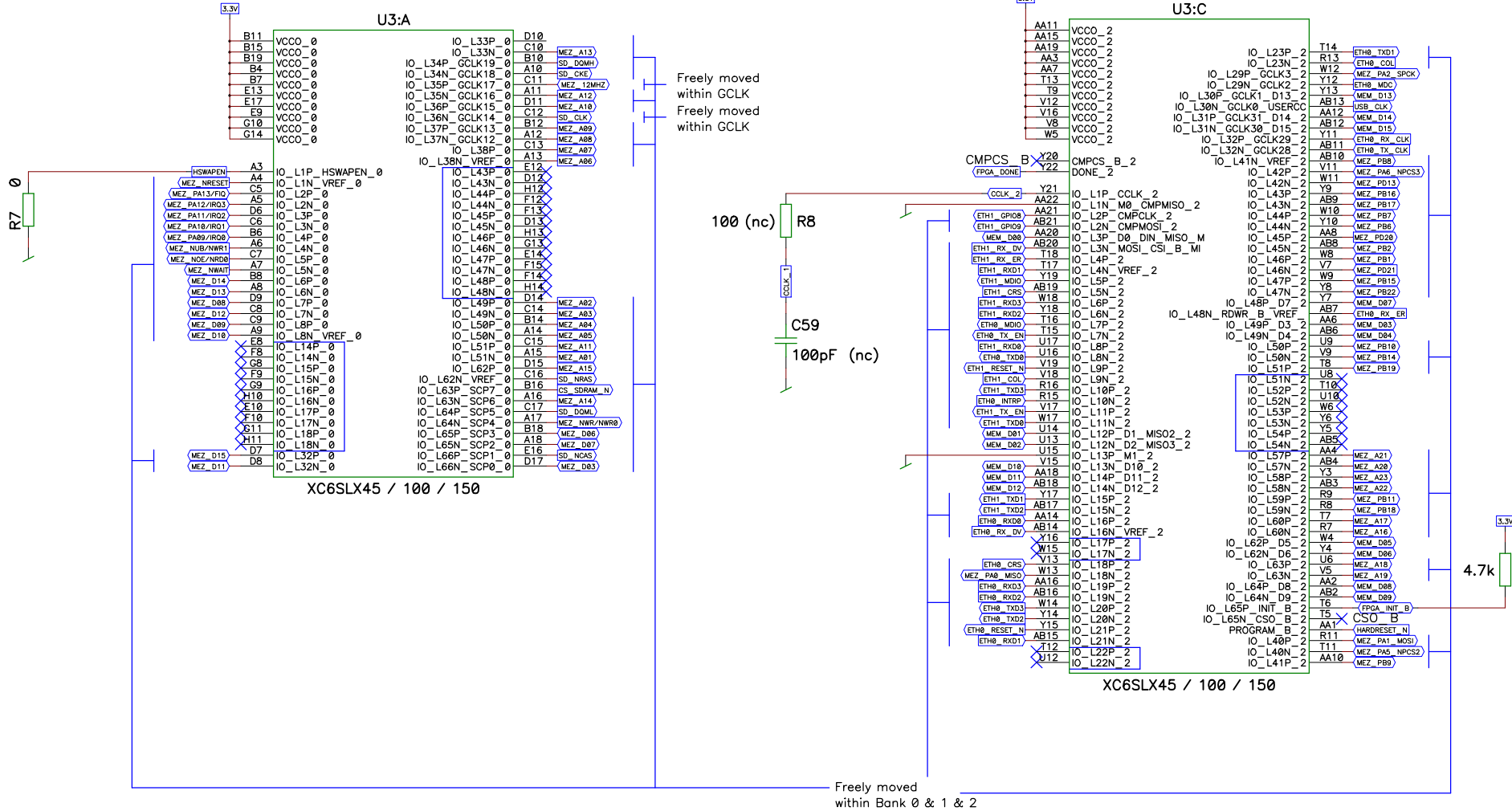
DES	{Date}	zas
REV	V1.0	
4/25	{Path}	FPGA_Rack_v1_0.sch

FPGA Bank 0 & 2

Pins NOT AVAILABLE ON LX45
ONLY AVAILABLE ON LX100 / 150
- IO_L14P_0, IO_L14N_0, IO_L15P_0,
IO_L15N_0, IO_L16P_0, IO_L16N_0,
IO_L17P_0, IO_L17N_0, IO_L18P_0

BPI Programming mode
M0 = 0
M1 = 0

Pins NOT AVAILABLE ON LX100
ONLY AVAILABLE ON LX45 / 150
- IO_L17P_2, IO_L17N_2
- IO_L22P_2, IO_L22N_2
- IO_L51P_2, IO_L51N_2, IO_L52P_2,
IO_L52N_2, IO_L53P_2, IO_L53N_2,
IO_L54P_2, IO_L54N_2



FPGA Rack	DES	{Date}	zas
HES-SO // Valais Wallis	REV	V1.0	
HAUTE ECOLE VALAISANNE	5/25	{Path}	FPGA_Rack_v1_0.sch

FPGA 1

FPGA Bank 1 & 3

The diagram illustrates the internal connections of FPGA Bank 1 & 3, specifically focusing on the U3:B and U3:D components. The layout is organized into columns representing different FPGA banks (1 to 10) and rows representing different components or connections (A to F).

U3:B Component:

- Inputs/Outputs:** Includes signals like CLK_25M, ETH1_PWR_DOWN_INT, ETH1_CLK_OUT, ETH1_MDC, MEZ_24MHz, CLK_186_25M, ETH1_RX_CLK, ETH1_TX_CLK, MEM_A83, MEM_A82, MEM_A81, MEM_A80, FLASH_OE_N, FLASH_WE_N, LDC, HDC, USER_DIL_1, JTAG_GPI00, JTAG_GPI01, JTAG_GPI02, JTAG_GPI03, JTAG_GPI04, JTAG_GPI05, JTAG_GPI06, JTAG_GPI07, JTAG_GPI08, JTAG_GPI09, JTAG_GPI10, JTAG_GPI11, JTAG_GPI12, JTAG_GPI13, JTAG_GPI14, JTAG_GPI15, JTAG_GPI16, JTAG_GPI17, JTAG_GPI18, JTAG_GPI19, JTAG_GPI20, JTAG_GPI21, JTAG_GPI22, JTAG_GPI23, JTAG_GPI24, JTAG_GPI25, JTAG_GPI26, JTAG_GPI27, JTAG_GPI28, JTAG_GPI29, JTAG_GPI30, JTAG_GPI31, JTAG_GPI32, JTAG_GPI33, JTAG_GPI34, JTAG_GPI35, JTAG_GPI36, JTAG_GPI37, JTAG_GPI38, JTAG_GPI39, JTAG_GPI40, JTAG_GPI41, JTAG_GPI42, JTAG_GPI43, JTAG_GPI44, JTAG_GPI45, JTAG_GPI46, JTAG_GPI47, JTAG_GPI48, JTAG_GPI49, JTAG_GPI50, JTAG_GPI51, JTAG_GPI52, JTAG_GPI53, JTAG_GPI54, JTAG_GPI55, JTAG_GPI56, JTAG_GPI57, JTAG_GPI58, JTAG_GPI59, JTAG_GPI60, JTAG_GPI61, JTAG_GPI62, JTAG_GPI63, JTAG_GPI64, JTAG_GPI65, JTAG_GPI66, JTAG_GPI67, JTAG_GPI68, JTAG_GPI69, JTAG_GPI70, JTAG_GPI71, JTAG_GPI72, JTAG_GPI73, JTAG_GPI74, JTAG_GPI75, JTAG_GPI76, JTAG_GPI77, JTAG_GPI78, JTAG_GPI79, JTAG_GPI80, JTAG_GPI81, JTAG_GPI82, JTAG_GPI83, JTAG_GPI84, JTAG_GPI85, JTAG_GPI86, JTAG_GPI87, JTAG_GPI88, JTAG_GPI89, JTAG_GPI90, JTAG_GPI91, JTAG_GPI92, JTAG_GPI93, JTAG_GPI94, JTAG_GPI95, JTAG_GPI96, JTAG_GPI97, JTAG_GPI98, JTAG_GPI99, JTAG_GPI100.
- Power/Reset:** Includes signals like VREF, FCS_B, FCS_A, FWE_B, FWE_A, LDC, HDC, USER_DIL_1, JTAG_GPI00, JTAG_GPI01, JTAG_GPI02, JTAG_GPI03, JTAG_GPI04, JTAG_GPI05, JTAG_GPI06, JTAG_GPI07, JTAG_GPI08, JTAG_GPI09, JTAG_GPI10, JTAG_GPI11, JTAG_GPI12, JTAG_GPI13, JTAG_GPI14, JTAG_GPI15, JTAG_GPI16, JTAG_GPI17, JTAG_GPI18, JTAG_GPI19, JTAG_GPI20, JTAG_GPI21, JTAG_GPI22, JTAG_GPI23, JTAG_GPI24, JTAG_GPI25, JTAG_GPI26, JTAG_GPI27, JTAG_GPI28, JTAG_GPI29, JTAG_GPI30, JTAG_GPI31, JTAG_GPI32, JTAG_GPI33, JTAG_GPI34, JTAG_GPI35, JTAG_GPI36, JTAG_GPI37, JTAG_GPI38, JTAG_GPI39, JTAG_GPI40, JTAG_GPI41, JTAG_GPI42, JTAG_GPI43, JTAG_GPI44, JTAG_GPI45, JTAG_GPI46, JTAG_GPI47, JTAG_GPI48, JTAG_GPI49, JTAG_GPI50, JTAG_GPI51, JTAG_GPI52, JTAG_GPI53, JTAG_GPI54, JTAG_GPI55, JTAG_GPI56, JTAG_GPI57, JTAG_GPI58, JTAG_GPI59, JTAG_GPI60, JTAG_GPI61, JTAG_GPI62, JTAG_GPI63, JTAG_GPI64, JTAG_GPI65, JTAG_GPI66, JTAG_GPI67, JTAG_GPI68, JTAG_GPI69, JTAG_GPI70, JTAG_GPI71, JTAG_GPI72, JTAG_GPI73, JTAG_GPI74, JTAG_GPI75, JTAG_GPI76, JTAG_GPI77, JTAG_GPI78, JTAG_GPI79, JTAG_GPI80, JTAG_GPI81, JTAG_GPI82, JTAG_GPI83, JTAG_GPI84, JTAG_GPI85, JTAG_GPI86, JTAG_GPI87, JTAG_GPI88, JTAG_GPI89, JTAG_GPI90, JTAG_GPI91, JTAG_GPI92, JTAG_GPI93, JTAG_GPI94, JTAG_GPI95, JTAG_GPI96, JTAG_GPI97, JTAG_GPI98, JTAG_GPI99, JTAG_GPI100.

U3:D Component:

- Inputs/Outputs:** Includes signals like L39P_M3LDOS_3, L39N_M3LDOSN_3, L40P_M3DQ6_3, L40N_M3DQ7_3, L41P_GCLK27_M3DQ4_3, L41N_GCLK26_M3DQ5_3, L42P_GCLK25_IRDY2_3, L42N_GCLK24_M3DQ4_3, L43P_GCLK23_M3RAS_3, L43N_GCLK22_IRDY2_3, L44P_GCLK21_M3A5_3, L44N_GCLK20_M3A6_3, L45P_M3A3_3, L45N_M3DQ1_3, L46P_M3C0L_3, L46N_M3CLKN_3, L47P_M3A0_3, L47N_M3A1_3, L48P_M3BA0_3, L48N_M3BA1_3, L49P_M3A7_3, L49N_M3A2_3, L50P_M3WE_3, L50N_M3BA2_3, L51P_M3A10_3, L51N_M3A4_3, L52P_M3A8_3, L52N_M3A9_3, L53P_M3CKE_3, L53N_M3A12_3, L54P_M3RESET_3, L54N_M3A11_3, L55P_M3A13_3, L55N_M3A14_3, L57P_3, L57N_VREF_3, L32P_M3DQ14_3, L32N_M3DQ15_3, L33P_M3DQ12_3, L33N_M3DQ13_3, L34P_M3UDQS_3, L34N_M3UDQSN_3, L35P_M3DQ10_3, L35N_M3DQ11_3, L36P_M3DQ8_3, L36N_M3DQ9_3, L37P_M3DQ0_3, L37N_M3DQ1_3, L38P_M3DQ2_3, L38N_M3DQ3_3, L39N_M3DQ3_3, L39N_M3DQ3_3.
- Power/Reset:** Includes signals like VREF, FCS_B, FCS_A, FWE_B, FWE_A, LDC, HDC, USER_DIL_1, JTAG_GPI00, JTAG_GPI01, JTAG_GPI02, JTAG_GPI03, JTAG_GPI04, JTAG_GPI05, JTAG_GPI06, JTAG_GPI07, JTAG_GPI08, JTAG_GPI09, JTAG_GPI10, JTAG_GPI11, JTAG_GPI12, JTAG_GPI13, JTAG_GPI14, JTAG_GPI15, JTAG_GPI16, JTAG_GPI17, JTAG_GPI18, JTAG_GPI19, JTAG_GPI20, JTAG_GPI21, JTAG_GPI22, JTAG_GPI23, JTAG_GPI24, JTAG_GPI25, JTAG_GPI26, JTAG_GPI27, JTAG_GPI28, JTAG_GPI29, JTAG_GPI30, JTAG_GPI31, JTAG_GPI32, JTAG_GPI33, JTAG_GPI34, JTAG_GPI35, JTAG_GPI36, JTAG_GPI37, JTAG_GPI38, JTAG_GPI39, JTAG_GPI40, JTAG_GPI41, JTAG_GPI42, JTAG_GPI43, JTAG_GPI44, JTAG_GPI45, JTAG_GPI46, JTAG_GPI47, JTAG_GPI48, JTAG_GPI49, JTAG_GPI50, JTAG_GPI51, JTAG_GPI52, JTAG_GPI53, JTAG_GPI54, JTAG_GPI55, JTAG_GPI56, JTAG_GPI57, JTAG_GPI58, JTAG_GPI59, JTAG_GPI60, JTAG_GPI61, JTAG_GPI62, JTAG_GPI63, JTAG_GPI64, JTAG_GPI65, JTAG_GPI66, JTAG_GPI67, JTAG_GPI68, JTAG_GPI69, JTAG_GPI70, JTAG_GPI71, JTAG_GPI72, JTAG_GPI73, JTAG_GPI74, JTAG_GPI75, JTAG_GPI76, JTAG_GPI77, JTAG_GPI78, JTAG_GPI79, JTAG_GPI80, JTAG_GPI81, JTAG_GPI82, JTAG_GPI83, JTAG_GPI84, JTAG_GPI85, JTAG_GPI86, JTAG_GPI87, JTAG_GPI88, JTAG_GPI89, JTAG_GPI90, JTAG_GPI91, JTAG_GPI92, JTAG_GPI93, JTAG_GPI94, JTAG_GPI95, JTAG_GPI96, JTAG_GPI97, JTAG_GPI98, JTAG_GPI99, JTAG_GPI100.

Annotations:

- Freely moved within GCLK:** Indicated for certain components in the U3:B section.
- Freely moved within Bank 0 & 1 & 2:** Indicated for components in the U3:B section.
- Freely moved within Bank 3:** Indicated for components in the U3:D section.
- But try to keep Differential Pairs together on connector:** A note for the U3:D section.
- Try to use all GCLK:** A note for the U3:D section.

Legend:

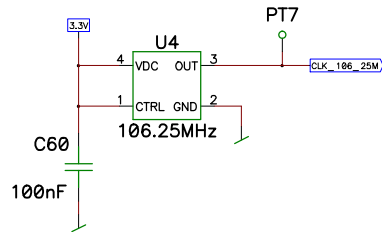
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- REV:** V1.0
- 6/25:** {Path} FPGA_Rack_v1_0.sch

FPGA 2

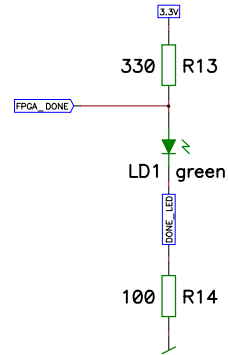
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6/25	{Path} FPGA Rack v1	0.sch

FPGA Config

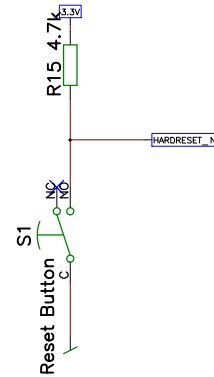
Main Oscillator



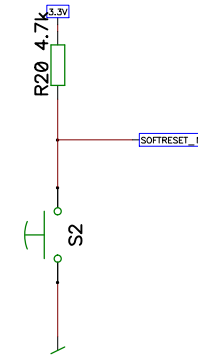
FPGA Done LED



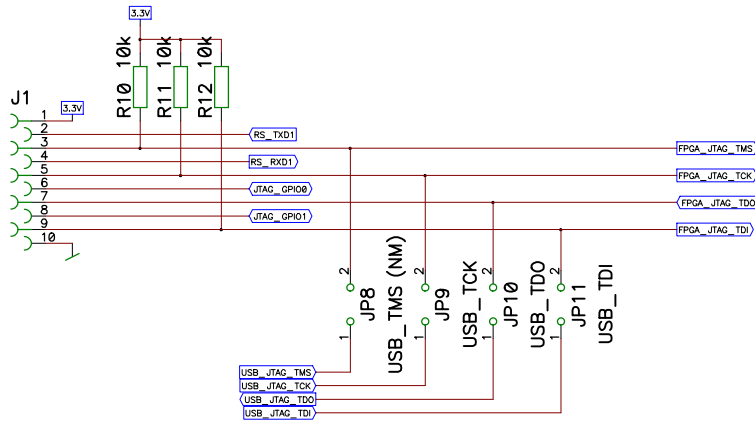
FPGA Hardreset Reprogram



FPGA Softreset

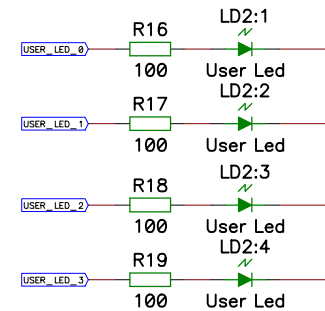


JTAG connector

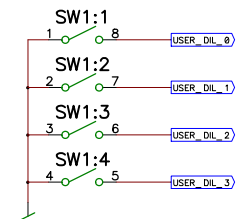


USER LED's

$$R = (3.3V - 2V) / 20mA = 65$$



USER DIP Switches

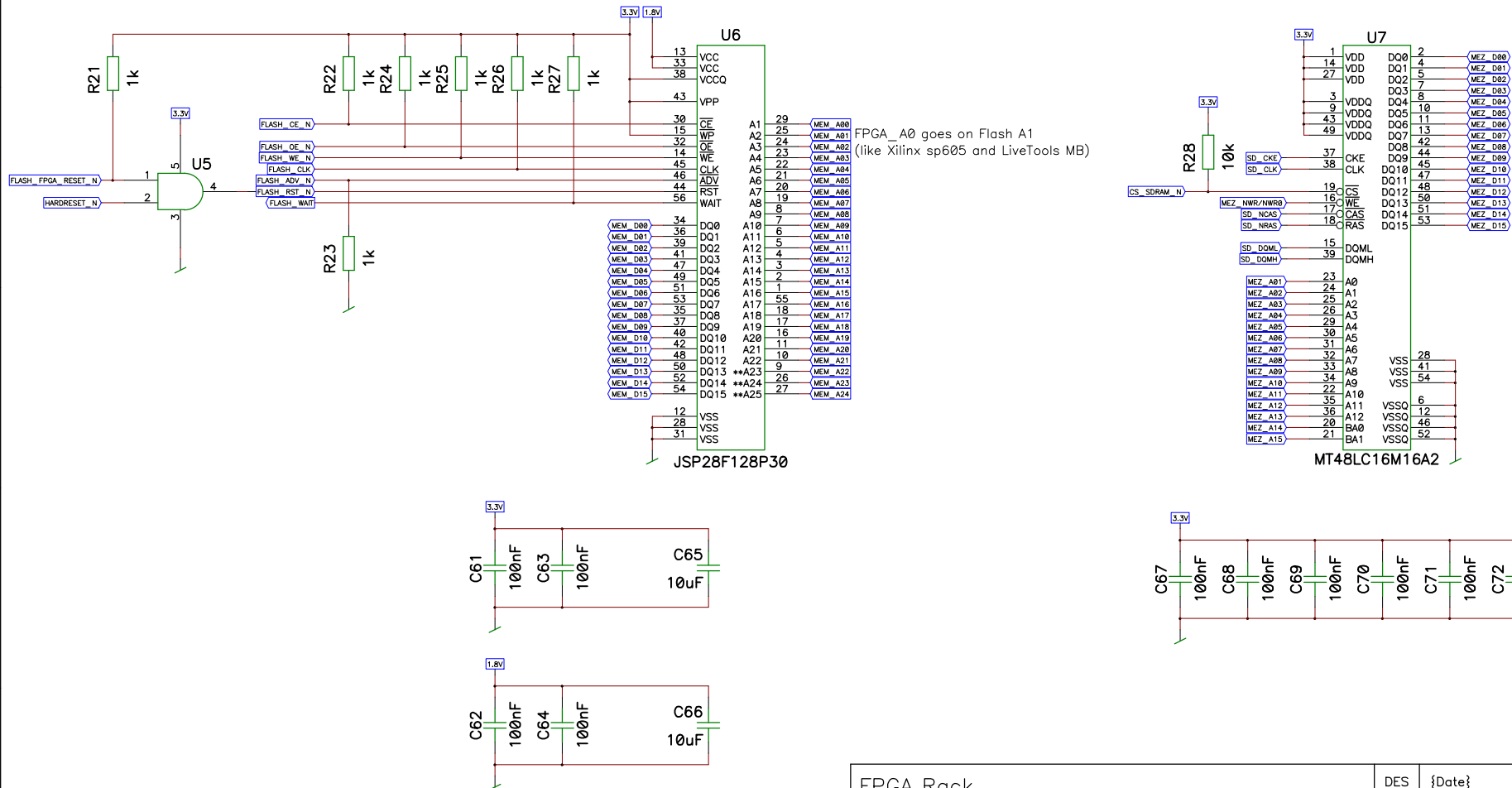


FPGA Rack
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FPGA Config

DES	{Date}	zas
REV	V1.0	
7/25	{Path}	FPGA_Rack_v1_0.sch

Memory Flash RAM



FPGA Rack	DES	{Date} zas
HES-SO // Valais Wallis	REV	V1.0
HAUTE ECOLE VALAISANNE	8/25	{Path} FPGA_Rack_v1_0.sch

Mezzanine

Mezza A

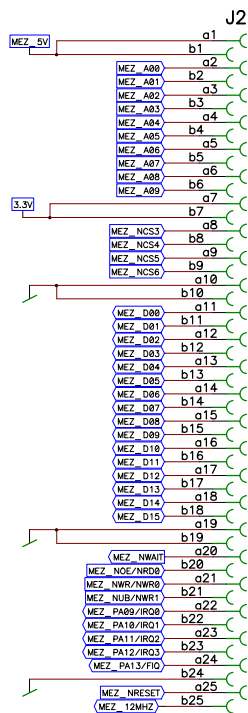
Mezza B

TOP SIDE

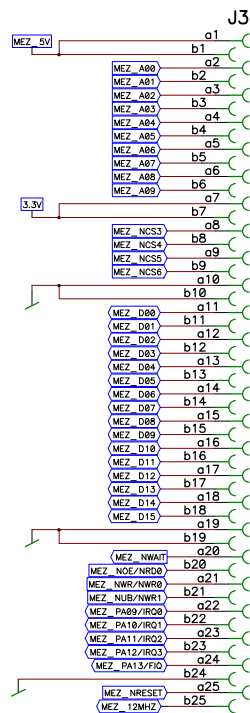
BOTTOM SIDE

TOP SIDE

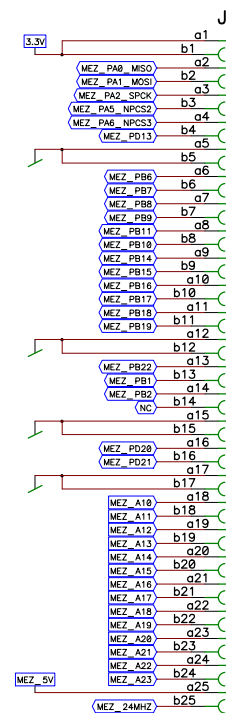
BOTTOM SIDE



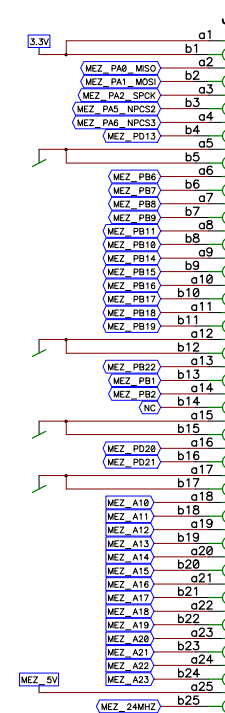
39 point-to-point I/Os
+ 1 global reset
+ 1 global clock (CLOCK)



39 point-to-point I/Os
+ 1 global reset
+ 1 global clock (CLOCK)



37 point-to-point I/Os
+ 1 global clock (MCK0)



37 point-to-point I/Os
+ 1 global clock (MCK0)

FPGA Rack

HES-SO // Valais Wallis

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Mezzanine

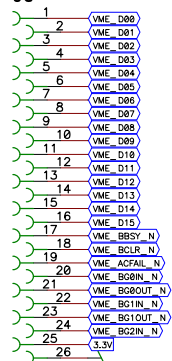
DES {Date} zas

REV V1.0

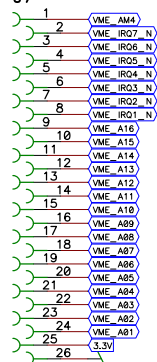
9/25 {Path}
FPGA_Rack_v1_0.sch

VME 96Pin

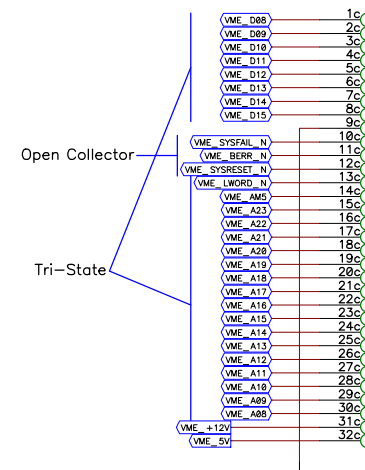
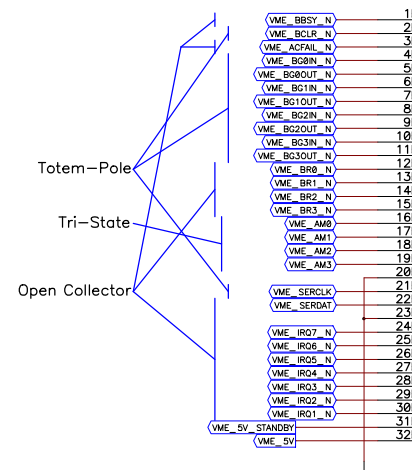
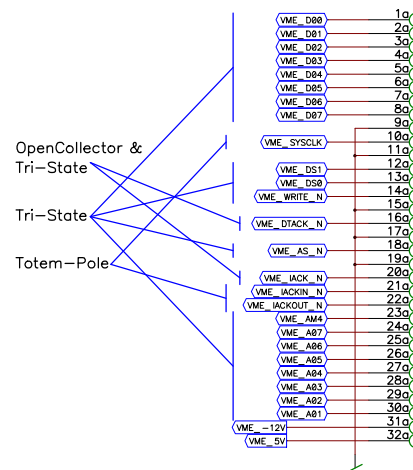
J6



J7



Pins on J10 and J11
can be freely moved except power



FPGA Rack

HES-SO // Valais Wallis

HAUTE ECOLE VALAISANNE

VME

DES {Date} zas

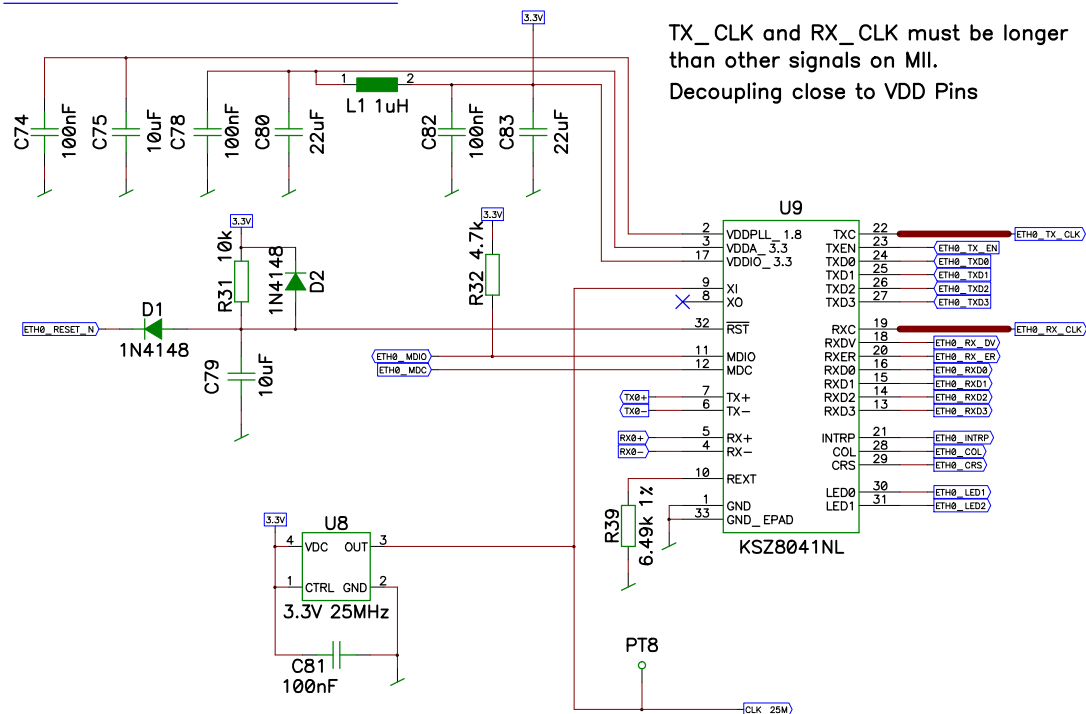
REV V1.0

10/25 {Path} FPGA_Rack_v1_0.sch

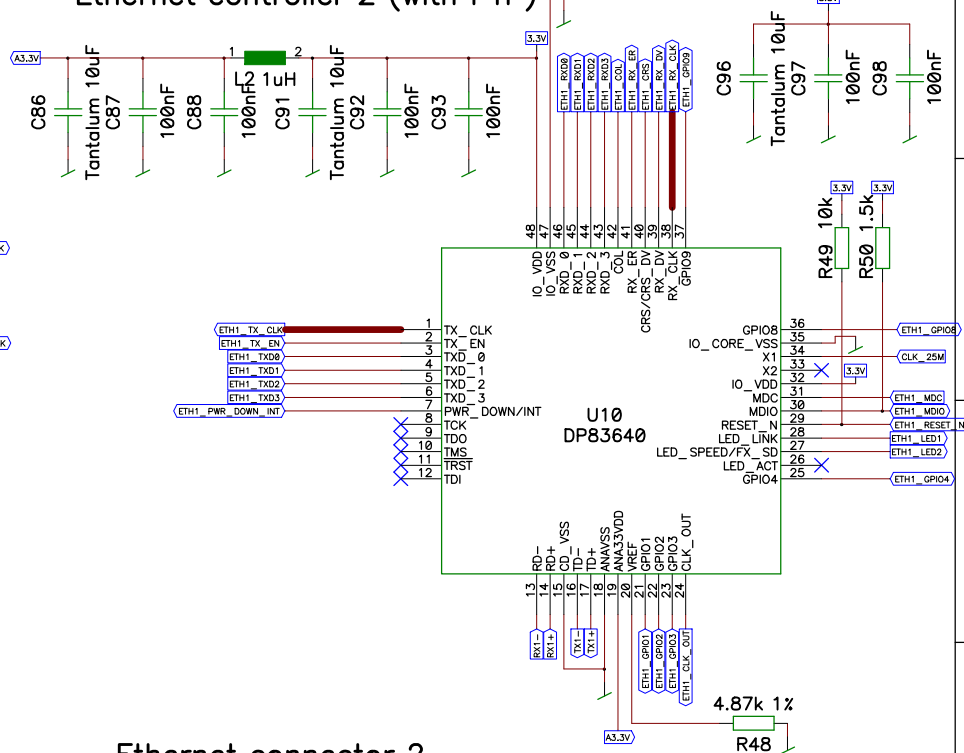
2 x Ethernet

Ethernet controller 1

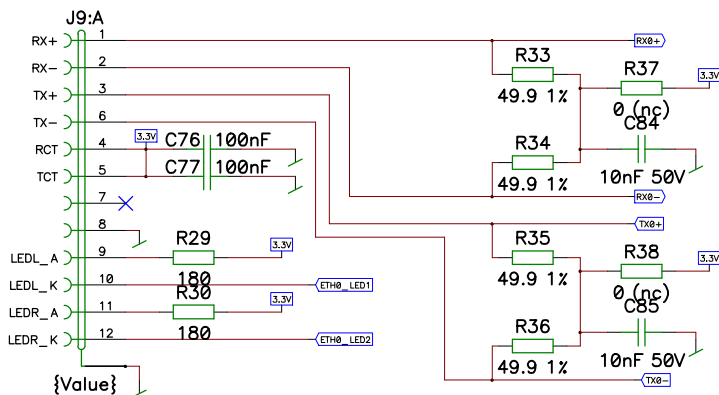
TX_CLK and RX_CLK must be longer than other signals on MII.
Decoupling close to VDD Pins



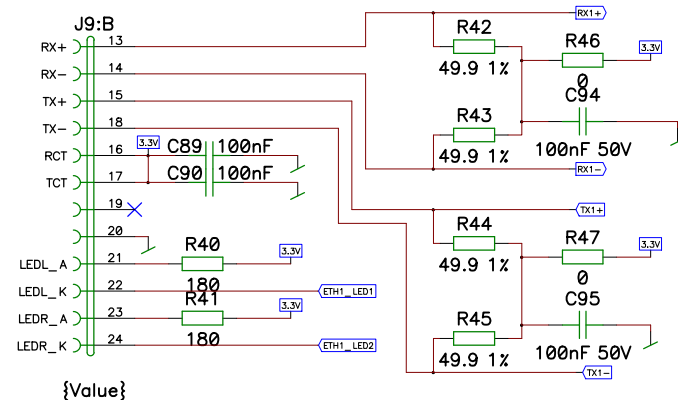
Ethernet controller 2 (with PTP)



Ethernet connector 1

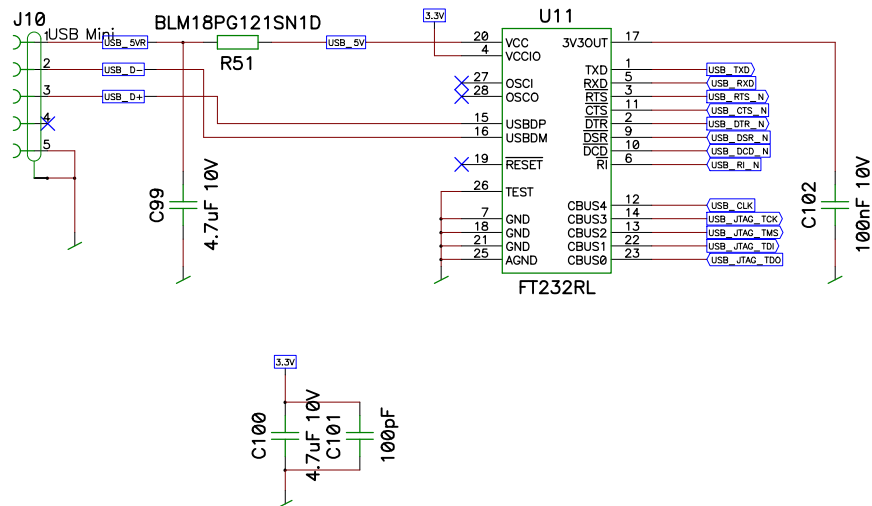


Ethernet connector 2



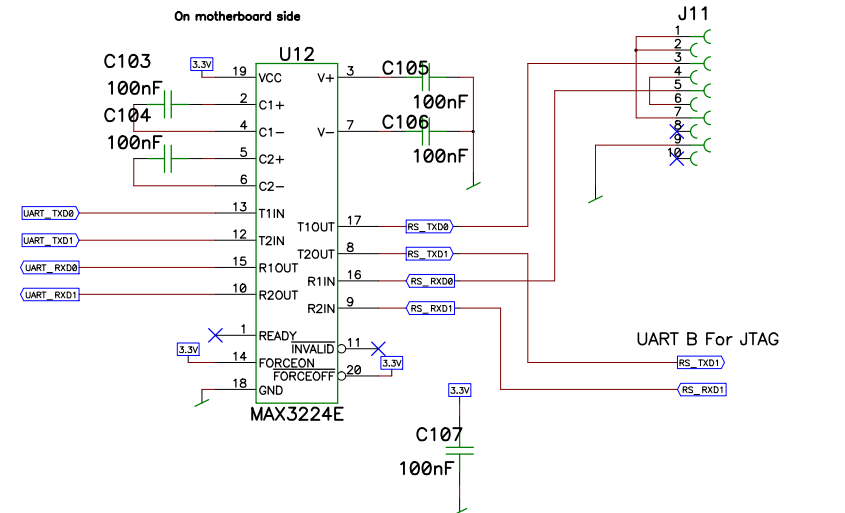
FPGA Rack	DES	{Date}	zas
HES-SO // Valais Wallis	REV	V1.0	
HAUTE ECOLE VALAISANNE	11/25	{Path}	FPGA_Rack_v1_0.sch

UART & FTDI



RS 232 Serial ports

UART A for Ribboncable conn



FPGA Rack	DES	{Date} zas
HES–SO // Valais Wallis	REV	V1.0
HAUTE ECOLE VALAISANNE	12/25	{Path} FPGA_Rack_v1_0.sch