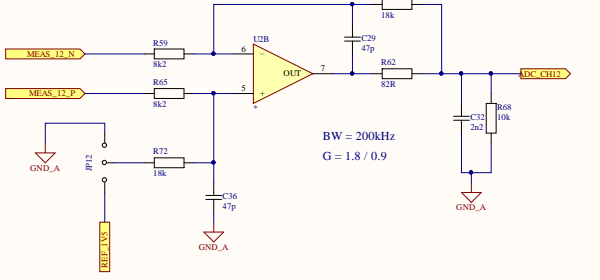
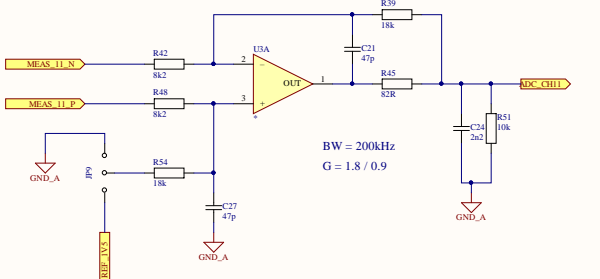
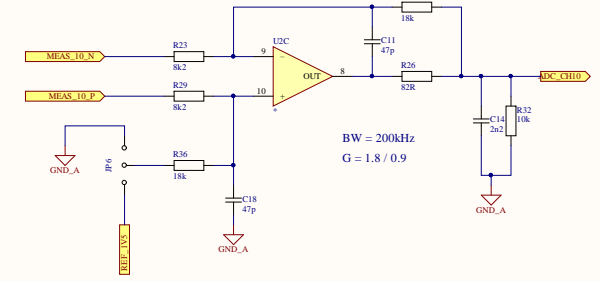
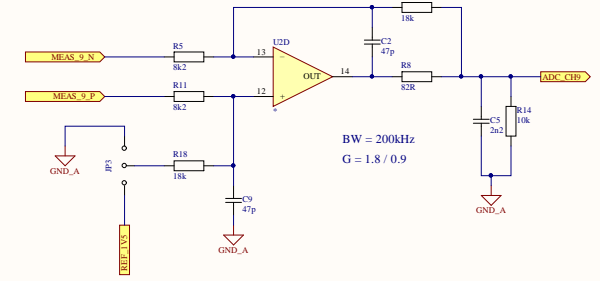
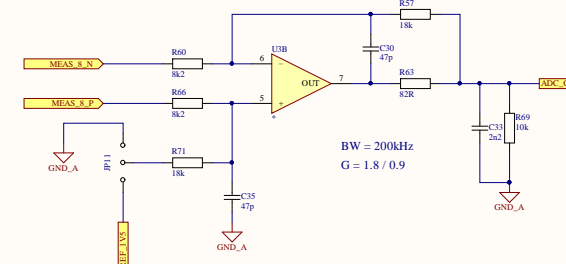
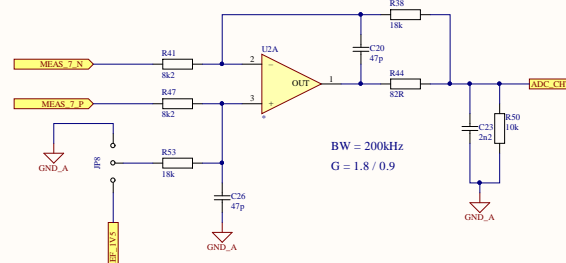
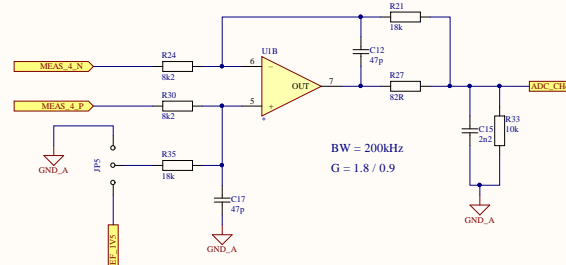
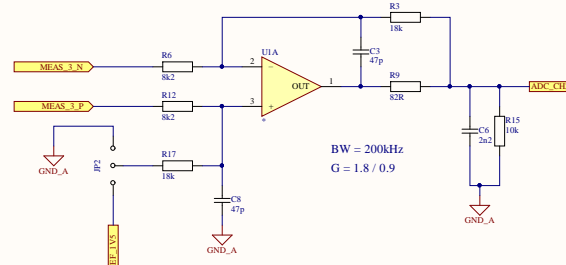
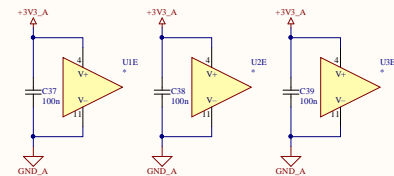
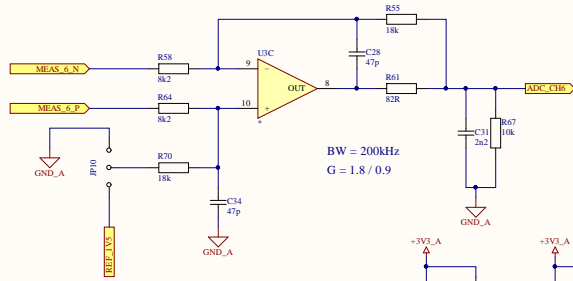
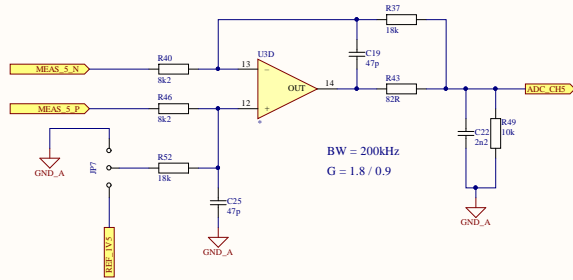
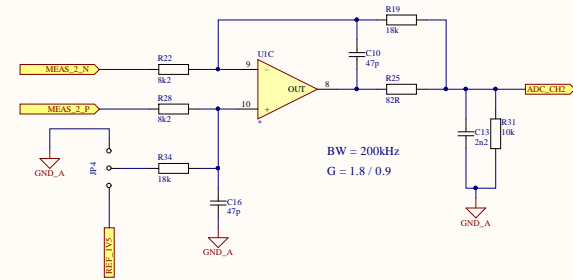
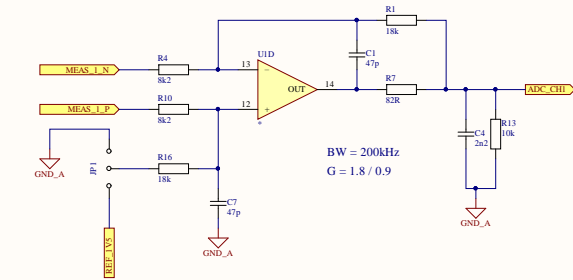


# Differential to single end conversion



ANAI0G\_MEZZANINE.PrjPcb

AD\_0.SchDoc

Revision : 1.0

Sheet 1 of 6

R:\Diploma\TD2021\SYND\jean.nanchen\Hardware\Mezzanine\_Board\AD\_0.SchDoc

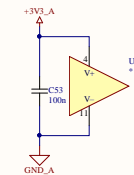
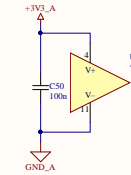
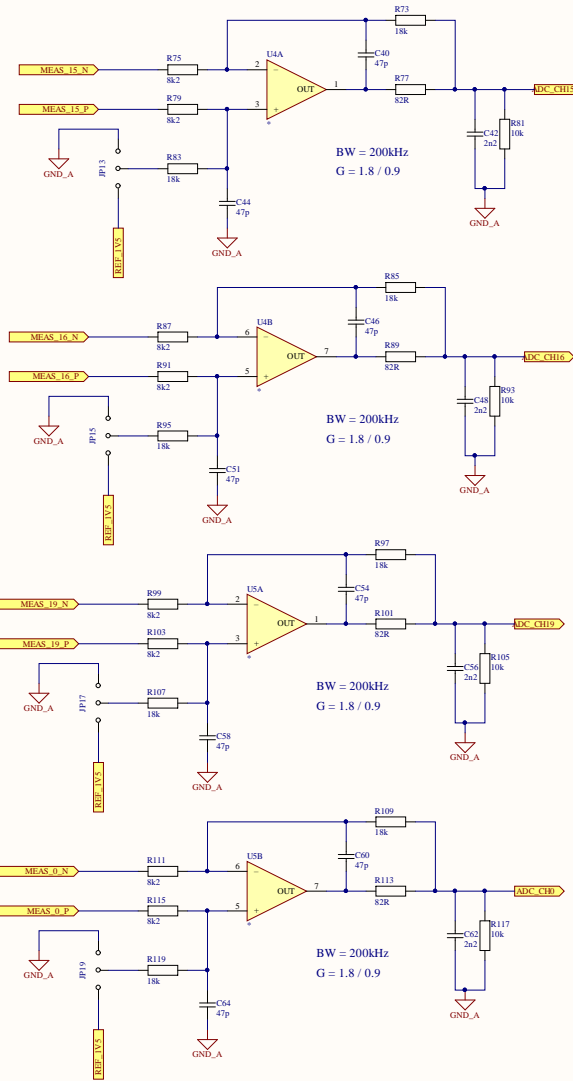
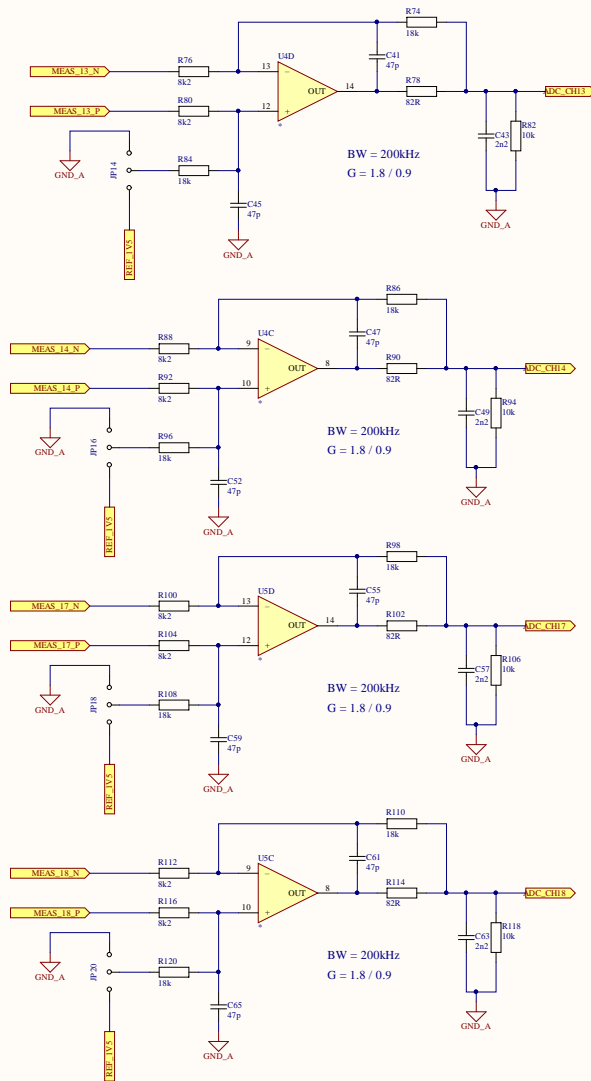
Hes·so VALAIS WALLIS

Date : 09.06.2021



Design by : Jean Nanchen

# Differential to single end conversion



ANAI0G\_MEZZANINE.PrjPcb

AD\_1.SchDoc

Revision : 1.0

Sheet 2 of 6

Date : 09.06.2021

Design by : Jean Nanchen

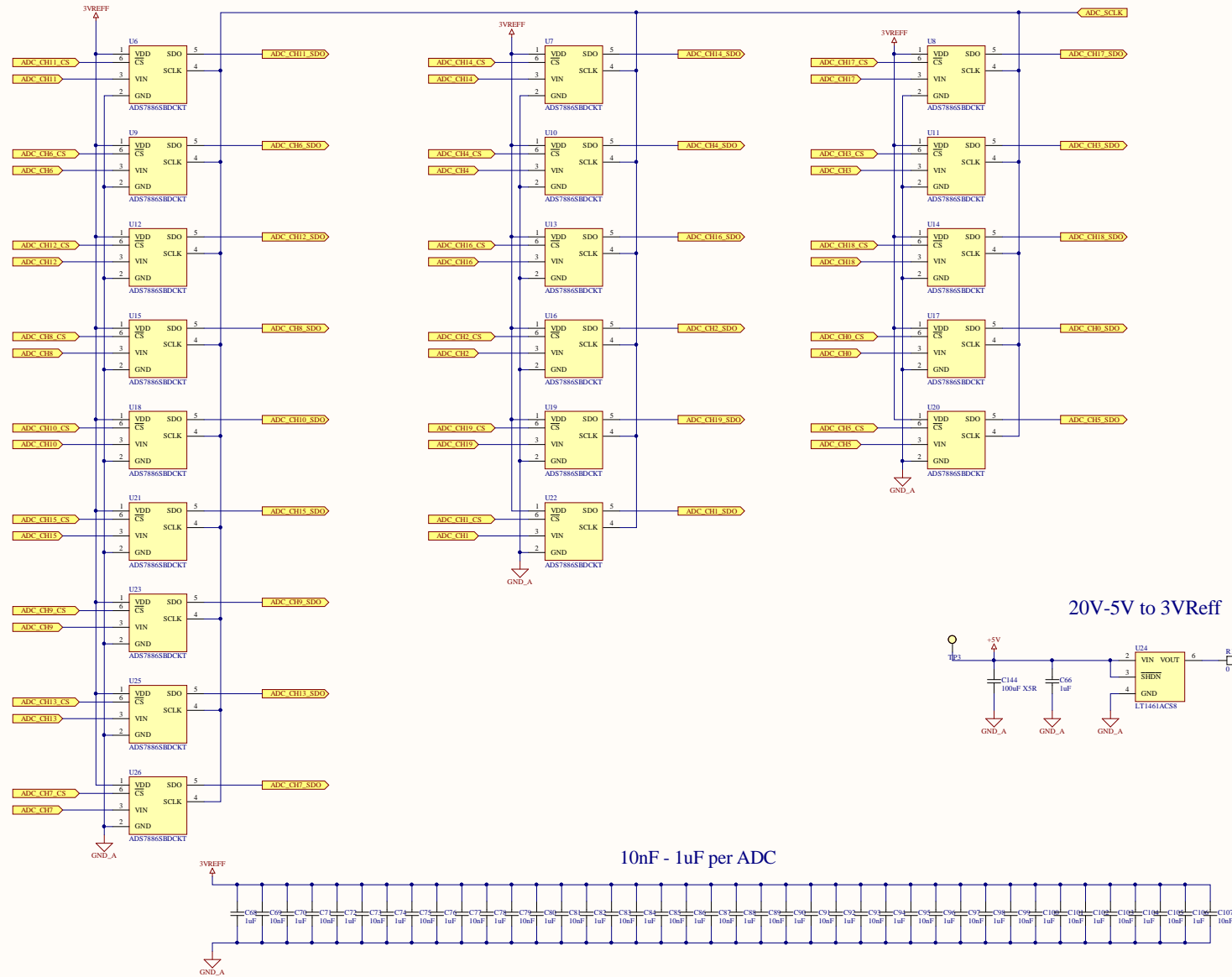
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# 20 CHANNELS ADC @ 1MSPS

ITOT = 30mA



ANAI0G\_MEZZANINE.PrjPcb

AD\_3.SchDoc

Revision : 1.0

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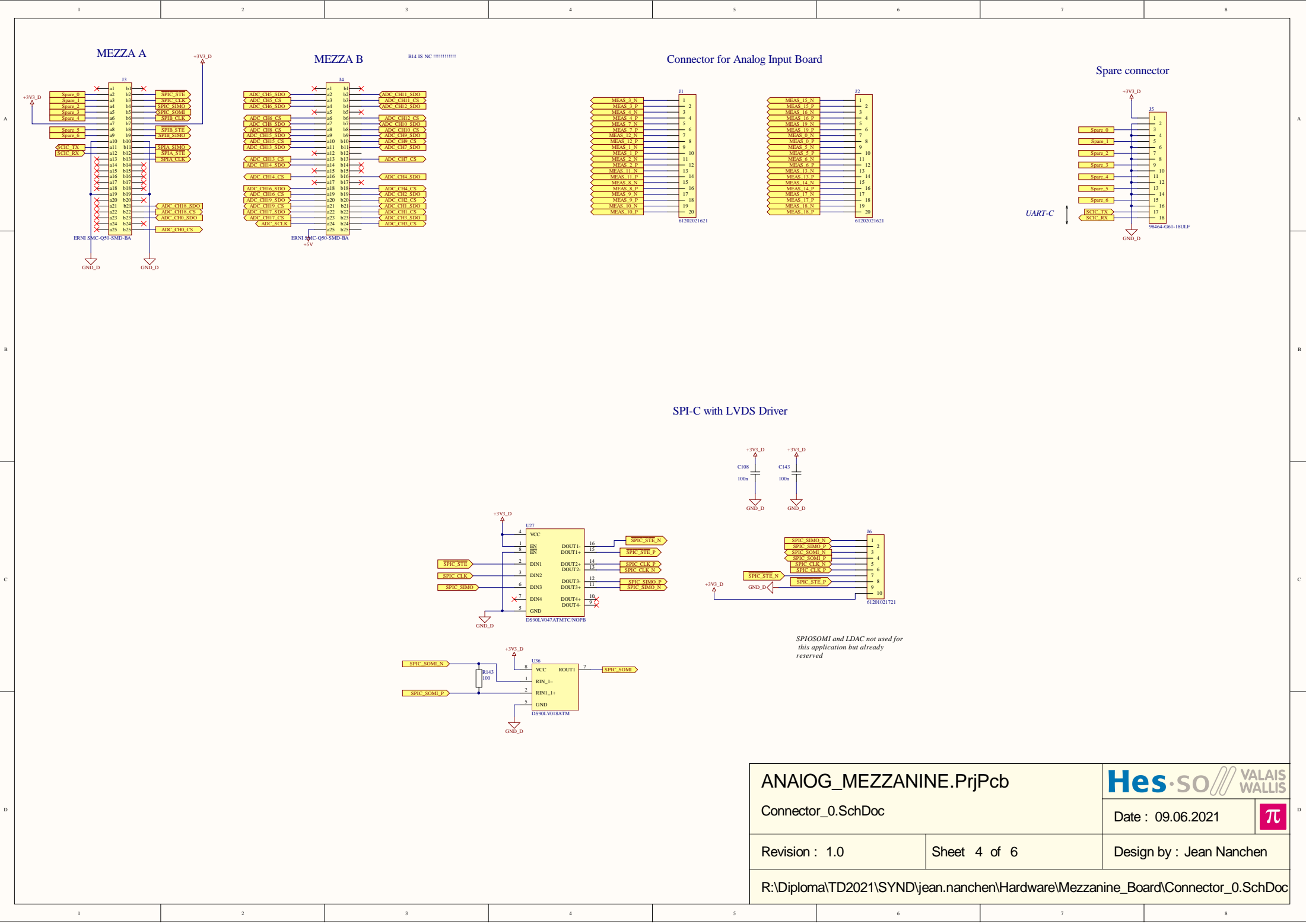
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Hes·SO VALAIS WALLIS

Date : 09.06.2021

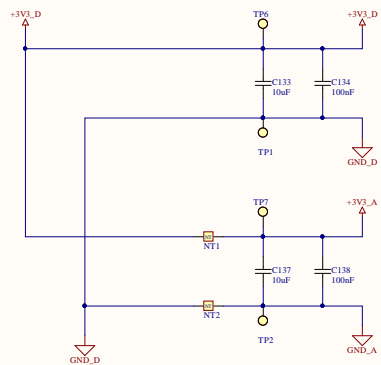


Design by : Jean Nanchen

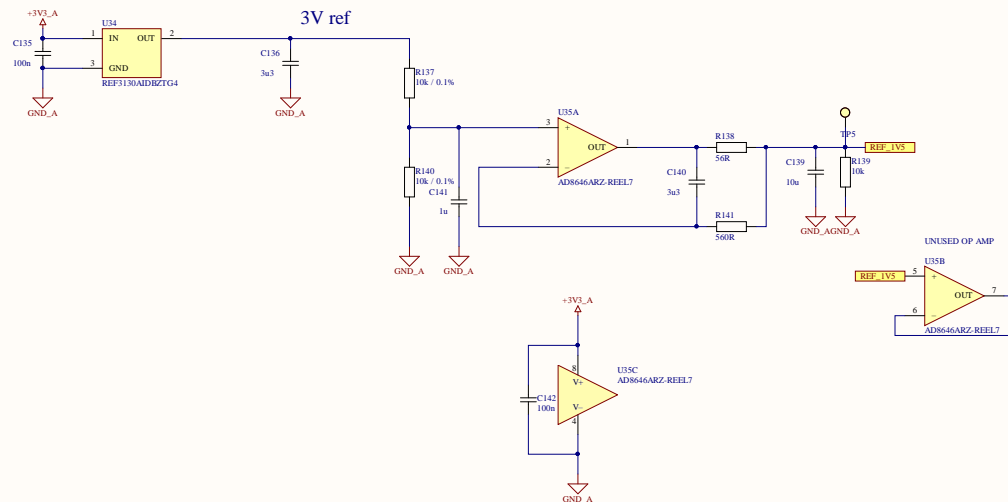


ANAIOG_MEZZANINE.PrjPcb		<div>Hes·SO VALAIS WALLIS</div>	
Connector_0.SchDoc		Date : 09.06.2021	<div>π</div>
Revision : 1.0	Sheet 4 of 6	Design by : Jean Nanchen	
R:\Diploma\TD2021\SYND\jean.nanchen\Hardware\Mezzanine_Board\Connector_0.SchDoc			

3V3 BackPlane ----->3V3\_D, 3V3\_A



1.5V Reference



ANAI0G\_MEZZANINE.PrjPcb

Supply\_0.SchDoc

Revision : 1.0

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Date : 09.06.2021

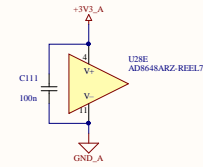
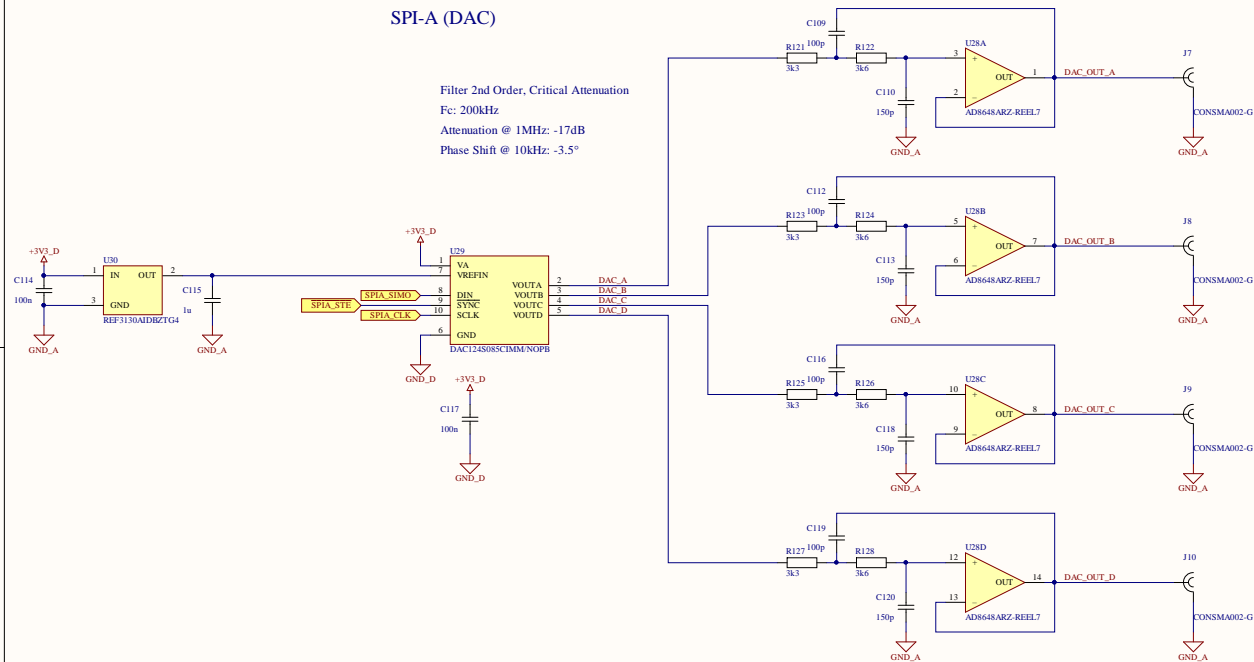


Design by : Jean Nanchen

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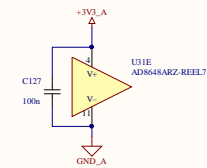
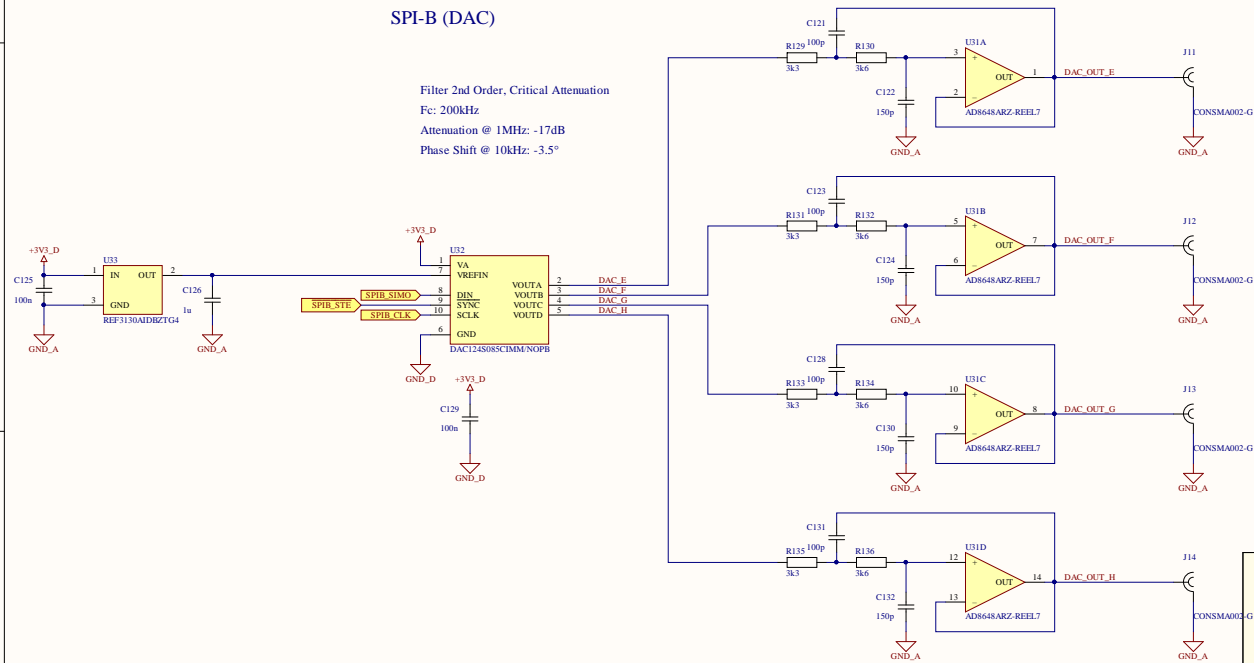
# SPI-A (DAC)

Filter 2nd Order, Critical Attenuation  
Fc: 200kHz  
Attenuation @ 1MHz: -17dB  
Phase Shift @ 10kHz: -3.5°



# SPI-B (DAC)

Filter 2nd Order, Critical Attenuation  
Fc: 200kHz  
Attenuation @ 1MHz: -17dB  
Phase Shift @ 10kHz: -3.5°



ANAI0G\_MEZZANINE.PrjPcb

DAC\_0.SchDoc

Revision : 1.0

Sheet 6 of 6

Hes·so VALAIS WALLIS

Date : 09.06.2021



Design by : Jean Nanchen

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