HEVs
Route du Rawyl 47
1950 Sion 2
www.hevs.ch

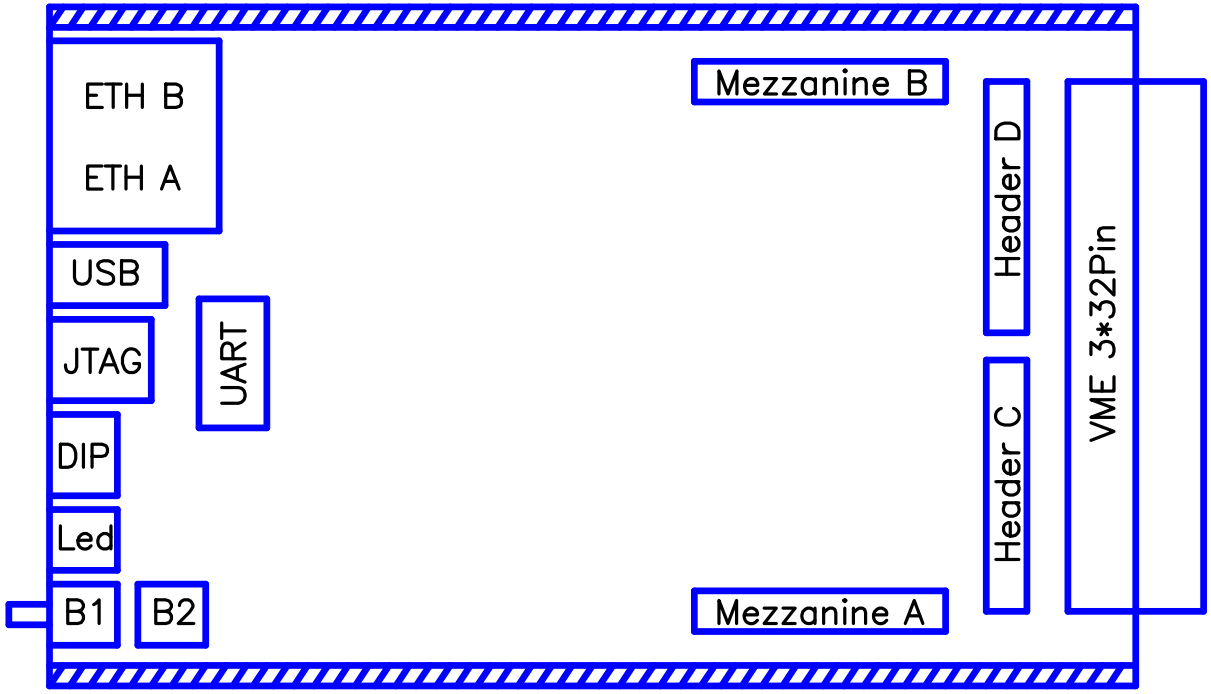
Designer:
Zahno Silvan
silvan.zahno@hevs.ch
or
zahno.silvan@gmail.com

FPGA_Rack Board : Rack-mounted Development FPGA platform

Page	Title	Description
1	Cover	This first page
2	Board	Shows Board connectivity
3	Power	3.3V 2.5V 1.8V 1.2V Regulation
4	FPGA Power	Xilinx Spartan 6 Power and Decoupling
5	FPGA 1	Xilinx Spartan 6 Bank 0 and 2 !!!!! Pay Attention on differences between LX45 and LX100
6	FPGA 2	Xilinx Spartan 6 Bank 1 and 3
7	FPGA Config	JTAG Connector / Reset Circuit / Done / Button / Leds
8	Memory	FLASH / SDRAM / Decoupling capacitors
9	Mezzanine	Mezza A and Mezza B Connectors (mezzanine support)
10	VME	VME Compatible Connector 96Pin
11	Ethernet	2 Ethernet Ports
12	UART	FTDI USB UART / UART

FPGA Rack Connectivity

= min. 3mm with no components for Rack insertion



FPGA Rack HES–SO // Valais Wallis Board		DES	{Date} zas
		REV	V1.0
HAUTE ECOLE VALAISANNE		2/25	{Path} FPGA_Rack_v1_0.sch

Power supply

5V –> From VME or USB
3.3V –> From LTM4615 (1)
1.2V –> From LTM4615 (2)
1.8V –> From LTM4615 LDO
2.5V –> From LDO

Layout Hints
– THERMAL_SW1 and THERMAL_SW2 Floating on seperate copper planes
– Decoupling capacitors close to pins

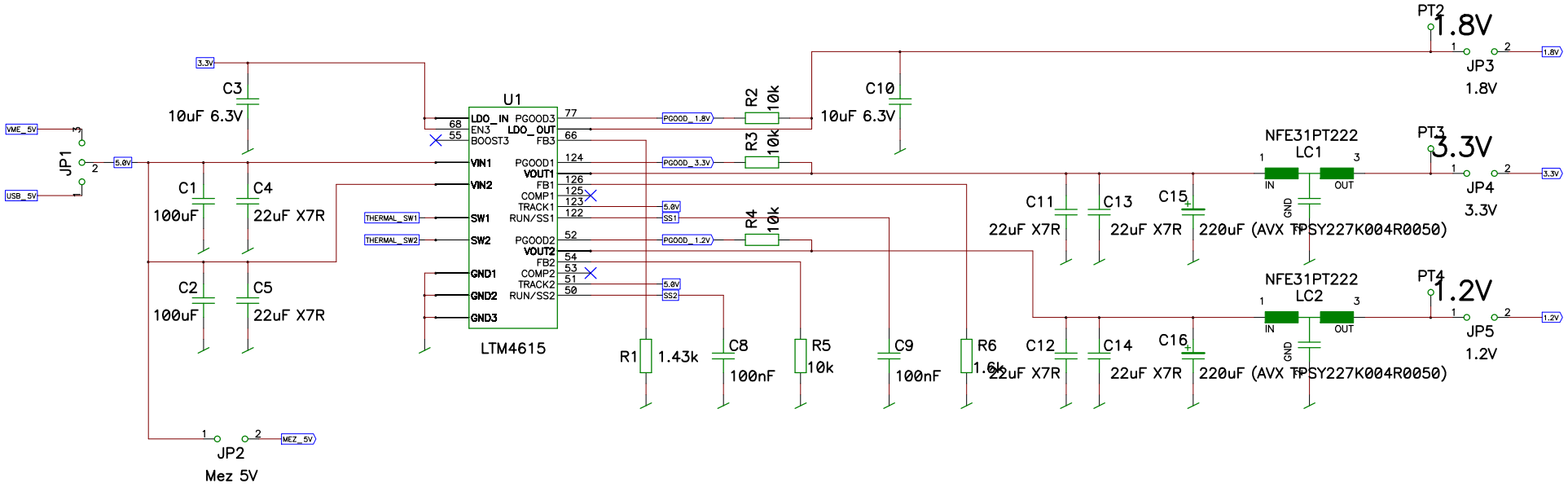
LDO VOUT
VLDO_OUT = 0.4V*(4.99k+RFB_LDO)/RFB_LDO
–> RFB_LDO = 1.996k / (VLDO_OUT – 0.4V)
RFB_LDO (Vout = 1.8V) = 1.996k / (1.8 – 0.4) = 1.42571k –> 1.43k 1% –> 1.80563V

VOUT = 0.8V * (4.99k + RFB) / RFB
–> RFB = 3.992k / (Vout – 0.8)

RFB (Vout = 3.3V) = 3.992k / (3.3 – 0.8) = 1.5968k –> 1.6k 1% –> 3.295 V

RFB (Vout = 1.2V) = 3.992k / (1.2 – 0.8) = 9.98k –> 10k 1%–> 1.1992 V

3.3V @ 4A / 1.2V @ 4A / 1.8V @ 1.5A

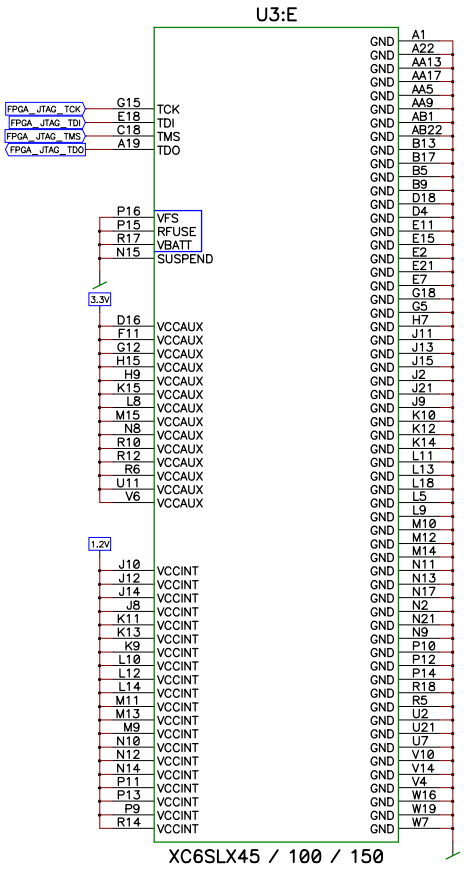


2.5V @950mA

FPGA Rack HES–SO // Valais Wallis	Power	DES	{Date} zas
		REV	V1.0
HAUTE ECOLE VALAISANNE		3/25	{Path} FPGA_Rack_v1_0.sch

FPGA Power

Pins NOT AVAILABLE ON LX45
ONLY AVAILABLE ON LX100 / 150
– VFS
– RFUSE
– VBATT

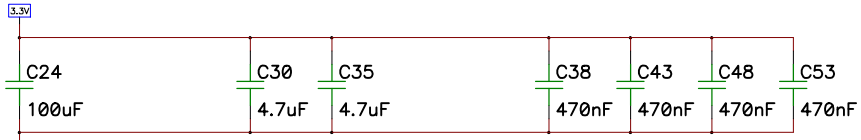


VCC0 Bank 3 Decoupling
LX45, LX100, LX150 –> 1x100uF / 1x4.7uF / 3x0.47uF

FPGA Decoupling

VCCINT Decoupling
LX45 –> 1x100uF / 1x4.7uF / 2x0.47uF
LX100 –> 1x100uF / 2x4.7uF / 4x0.47uF
LX150 –> 2x100uF / 3x4.7uF / 6x0.47uF

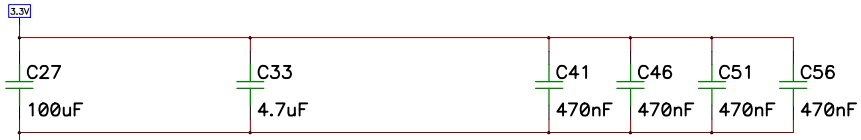
VCCAUX Decoupling
LX45, LX100, LX150 –> 1x100uF / 2x4.7uF / 4x0.47uF



VCC0 Bank 0 Decoupling
LX45, LX100, LX150 –> 1x100uF / 1x4.7uF / 2x0.47uF

VCC0 Bank 1 Decoupling
LX45, LX100, LX150 –> 1x100uF / 1x4.7uF / 3x0.47uF

VCC0 Bank 2 Decoupling
LX45 –> 1x100uF / 1x4.7uF / 4x0.47uF
LX100, LX150 –> 1x100uF / 1x4.7uF / 3x0.47uF



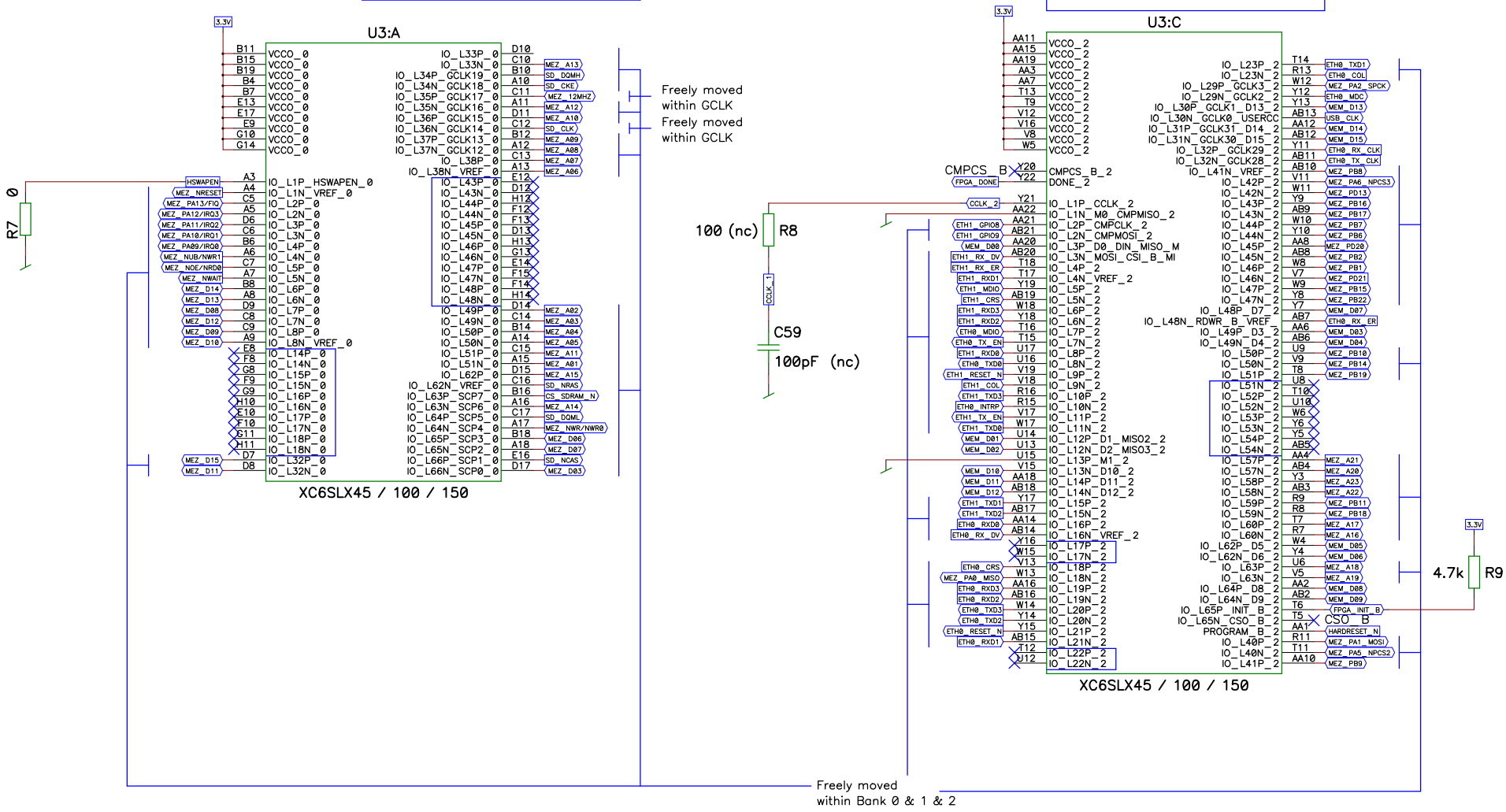
FPGA Rack HES–SO // Valais Wallis FPGA Power	DES	{Date} zas
	REV	V1.0
HAUTE ECOLE VALAISANNE	4/25	{Path} FPGA_Rack_v1_0.sch

FPGA Bank 0 & 2

Pins NOT AVAILABLE ON LX45
ONLY AVAILABLE ON LX100 / 150
– IO_L14P_0, IO_L14N_0, IO_L15P_0,
IO_L15N_0, IO_L16P_0, IO_L16N_0,
IO_L17P_0, IO_L17N_0, IO_L18P_0

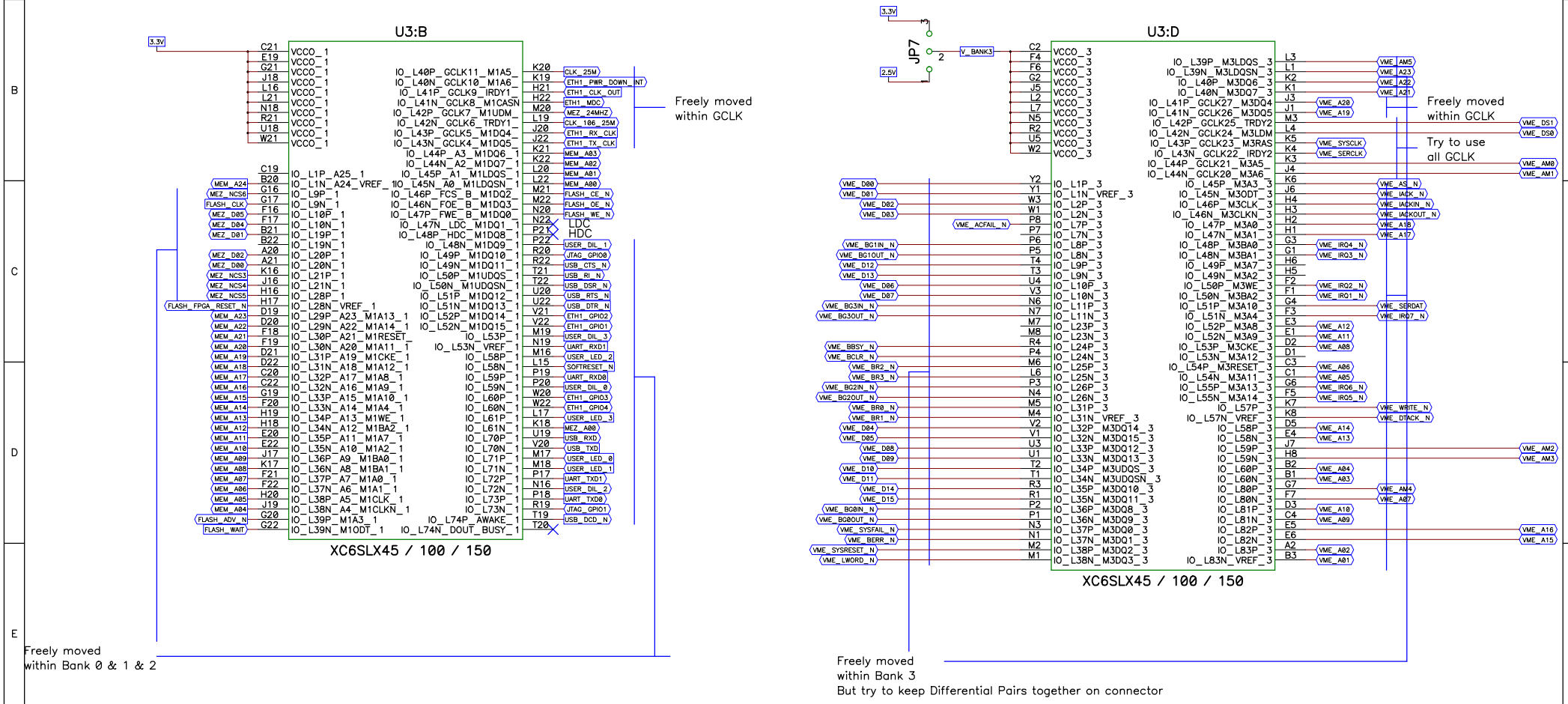
BPI Programming mode
M0 = 0
M1 = 0

Pins NOT AVAILABLE ON LX100
ONLY AVAILABLE ON LX45 / 150
– IO_L17P_2, IO_L17N_2
– IO_L22P_2, IO_L22N_2
– IO_L51P_2, IO_L51N_2, IO_L52P_2,
IO_L52N_2, IO_L53P_2, IO_L53N_2,
IO_L54P_2, IO_L54N_2



FPGA Rack HES–SO // Valais Wallis FPGA 1 HAUTE ECOLE VALAISANNE	DES	{Date} zas
	REV	V1.0
	5/25	{Path} FPGA_Rack_v1_0.sch

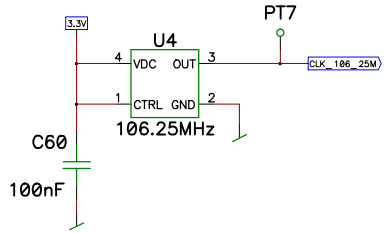
FPGA Bank 1 & 3



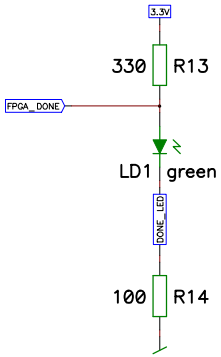
FPGA Rack		DES	{Date} zas
HES–SO // Valais Wallis	FPGA 2	REV	V1.0
HAUTE ECOLE VALAISANNE		6/25	{Path} FPGA_Rack_v1_0.sch

FPGA Config

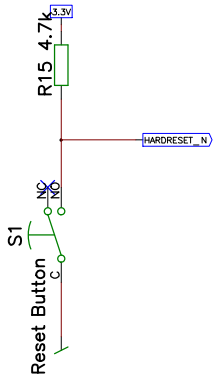
Main Oscillator



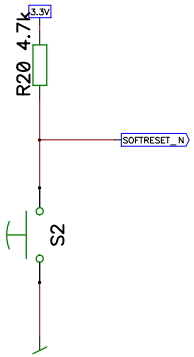
FPGA Done LED



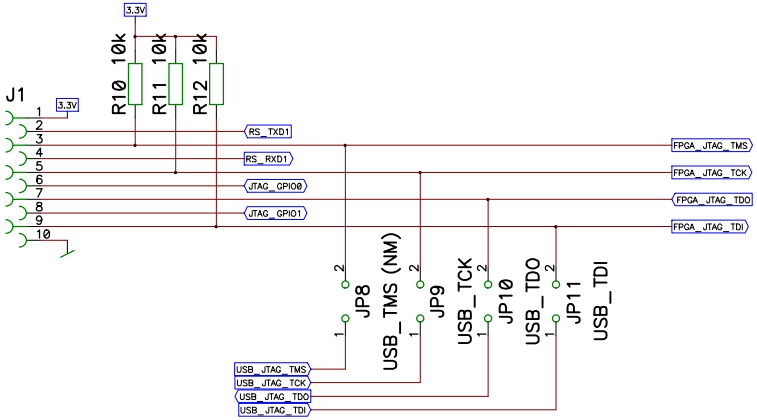
FPGA Hardreset Reprogram



FPGA Softreset

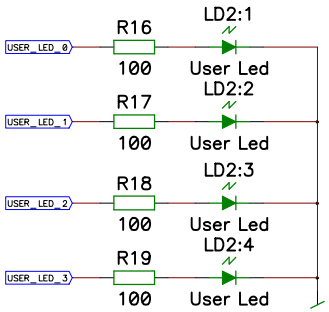


JTAG connector

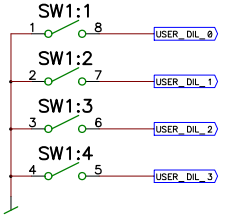


USER LED's

R = (3.3V – 2V) / 20mA = 65

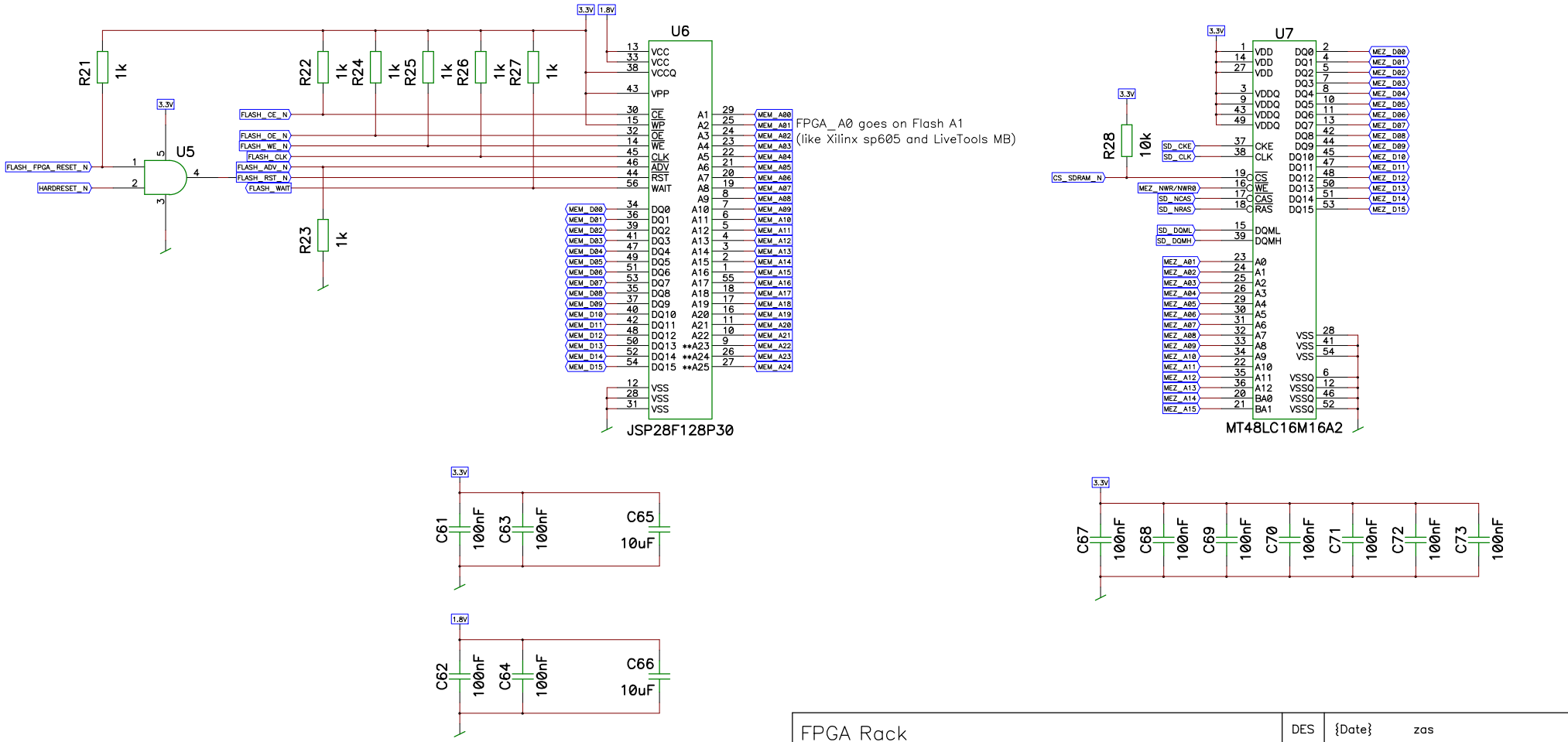


USER DIP Switches



FPGA Rack HES–SO // Valais Wallis FPGA Config		DES	{Date} zas
		REV	V1.0
HAUTE ECOLE VALAISANNE		7/25	{Path} FPGA_Rack_v1_0.sch

Memory Flash RAM

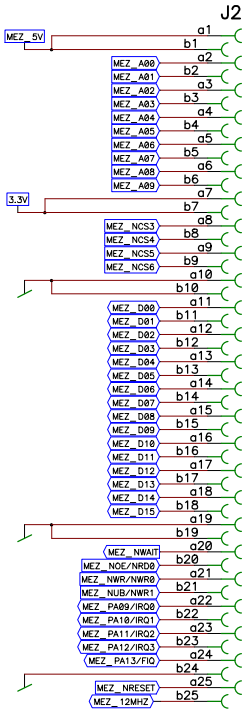


FPGA Rack	DES {Date} zas
HES-SO // Valais Wallis — Memory	REV V1.0
HAUTE ECOLE VALAISANNE	8/25 {Path} FPGA_Rack_v1_0.sch

Mezzanine

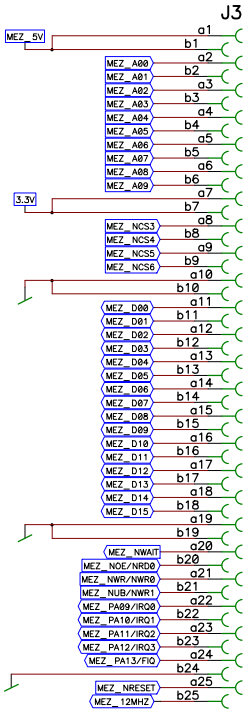
Mezza A

TOP SIDE



39 point-to-point IOs
+ 1 global reset
+ 1 global clock (CLOCK)

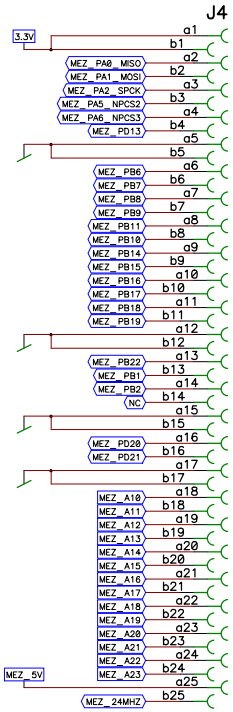
BOTTOM SIDE



39 point-to-point IOs
+ 1 global reset
+ 1 global clock (CLOCK)

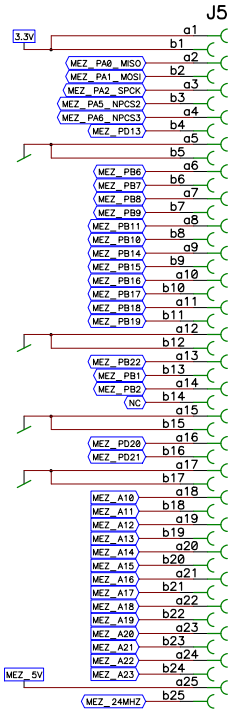
Mezza B

TOP SIDE



37 point-to-point IOs
+ 1 global clock (MCK0)

BOTTOM SIDE



37 point-to-point IOs
+ 1 global clock (MCK0)

FPGA Rack HES-SO // Valais Wallis — Mezzanine	DES	{Date} zas
	REV	V1.0
HAUTE ECOLE VALAISANNE	9/25	{Path} FPGA_Rack_v1_0.sch

VME 96Pin

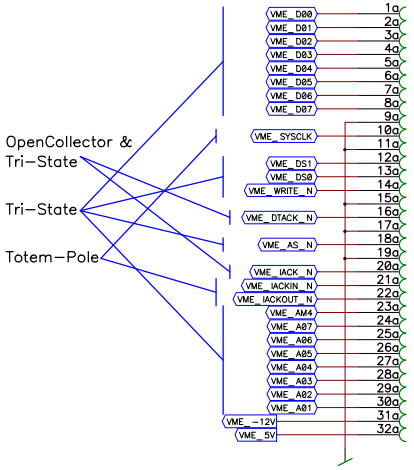
J6

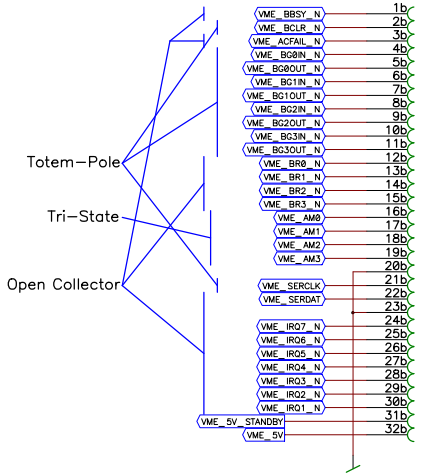
1	VME_D00
2	VME_D01
3	VME_D02
4	VME_D03
5	VME_D04
6	VME_D05
7	VME_D06
8	VME_D07
9	VME_D08
10	VME_D09
11	VME_D10
12	VME_D11
13	VME_D12
14	VME_D13
15	VME_D14
16	VME_D15
17	VME_BBSY_N
18	VME_BCLR_N
19	VME_ACFAIL_N
20	VME_BG0IN_N
21	VME_BG0OUT_N
22	VME_BG1IN_N
23	VME_BG1OUT_N
24	VME_BG2IN_N
25	3.3V
26	

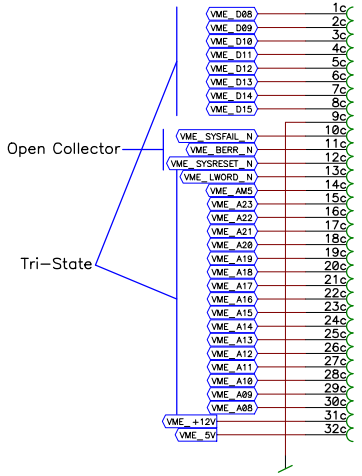
J7

1	VME_AM4
2	VME_IRQ7_N
3	VME_IRQ6_N
4	VME_IRQ5_N
5	VME_IRQ4_N
6	VME_IRQ3_N
7	VME_IRQ2_N
8	VME_IRQ1_N
9	VME_A16
10	VME_A15
11	VME_A14
12	VME_A13
13	VME_A12
14	VME_A11
15	VME_A10
16	VME_A09
17	VME_A08
18	VME_A07
19	VME_A06
20	VME_A05
21	VME_A04
22	VME_A03
23	VME_A02
24	VME_A01
25	3.3V
26	

Pins on J10 and J11
can be freely moved except power



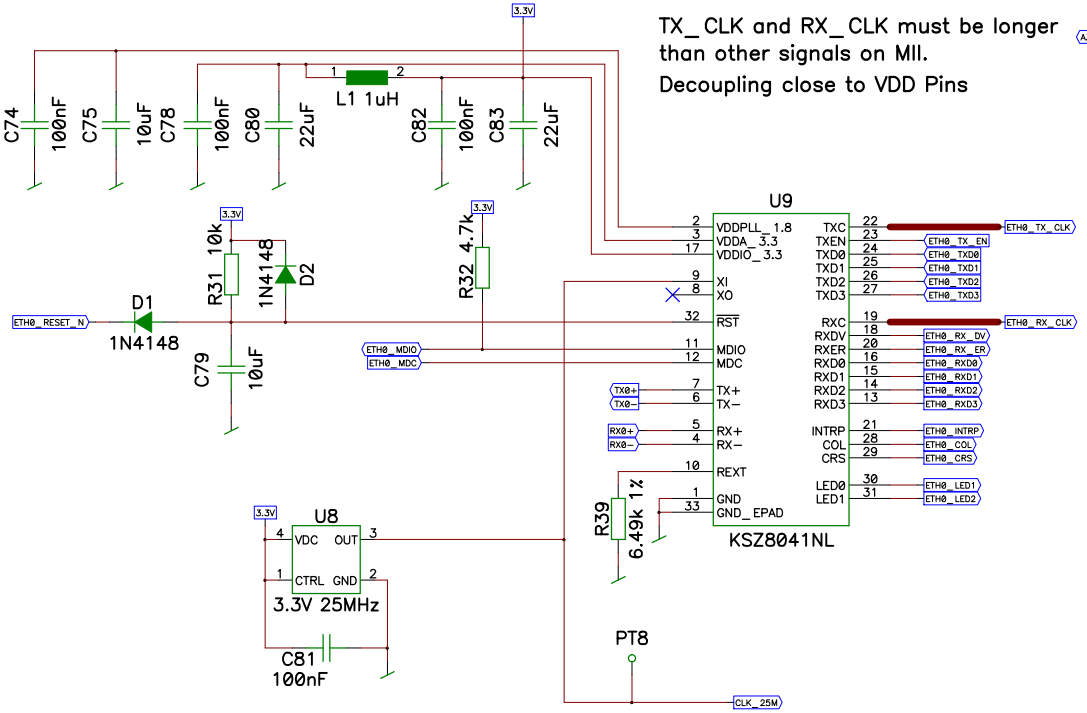




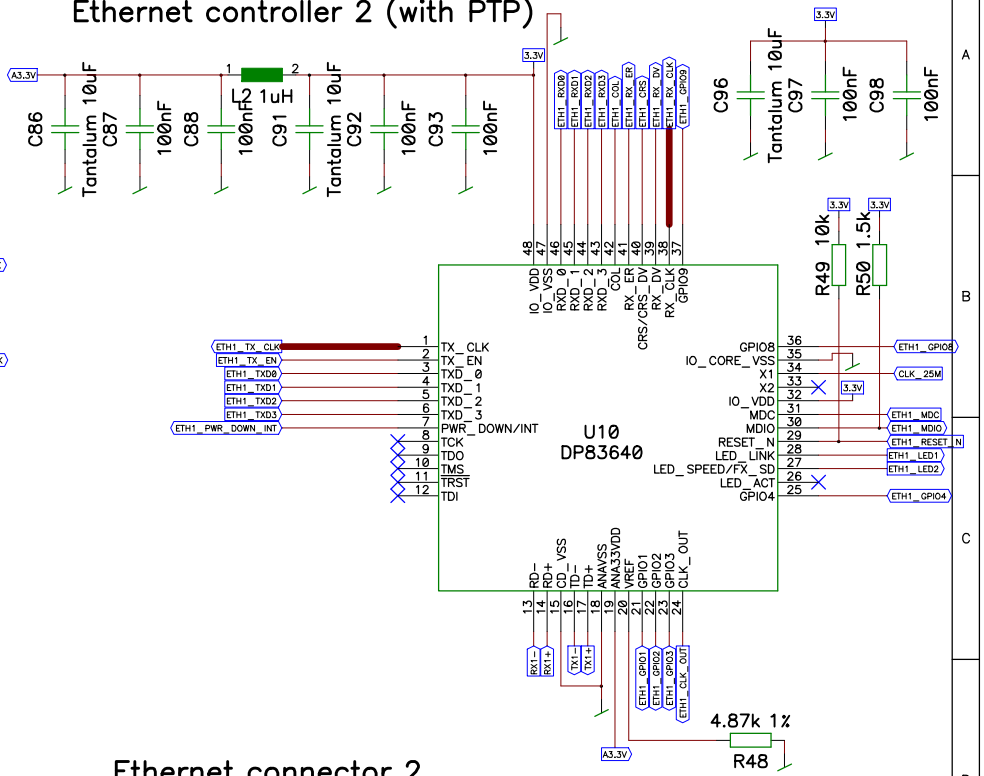
FPGA Rack		DES	{Date} zas
HES-SO // Valais Wallis	VME	REV	V1.0
HAUTE ECOLE VALAISANNE		10/25	{Path} FPGA_Rack_v1_0.sch

2 x Ethernet

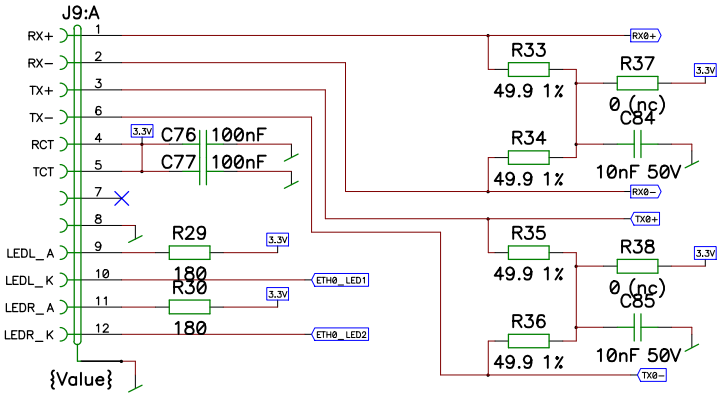
Ethernet controller 1



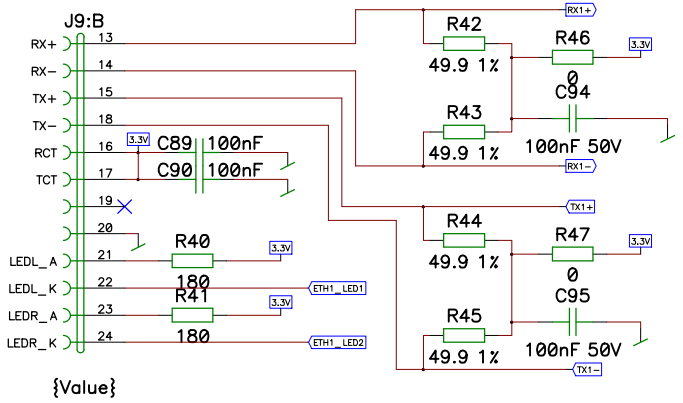
Ethernet controller 2 (with PTP)



Ethernet connector 1

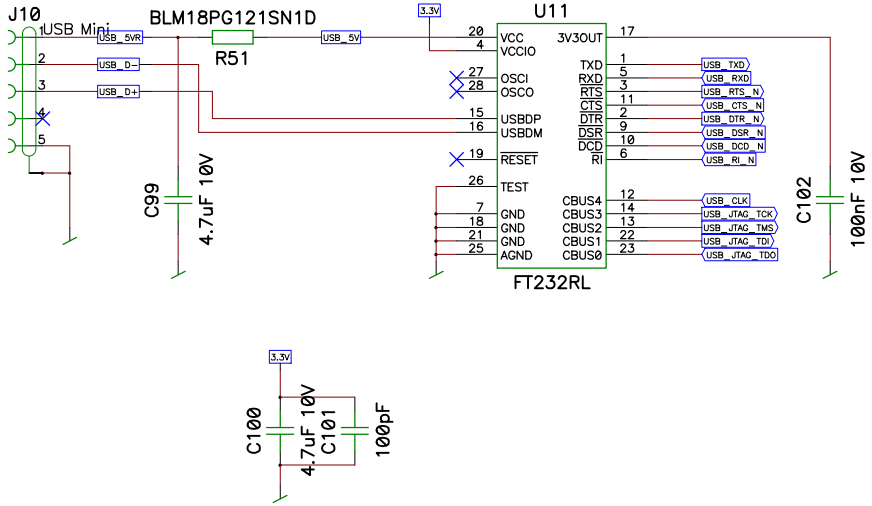


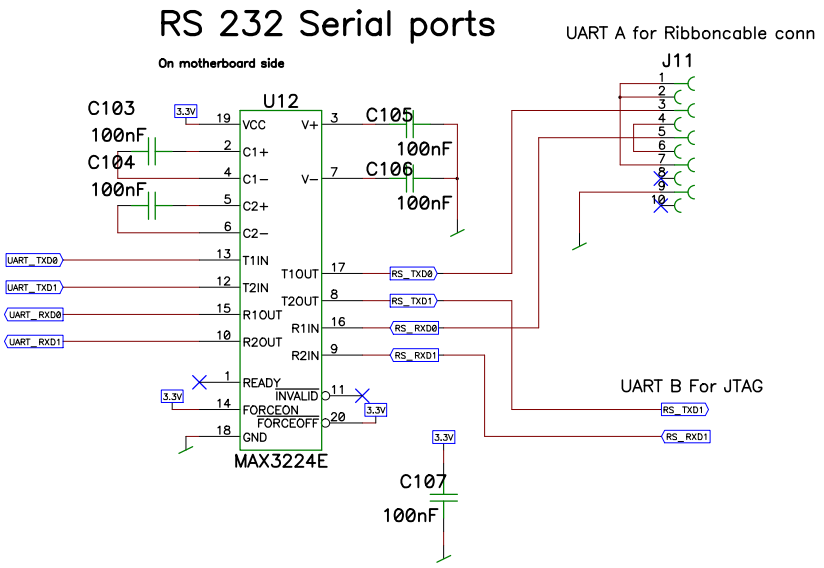
Ethernet connector 2



FPGA Rack HES–SO // Valais Wallis Ethernet	DES	{Date} zas
	REV	V1.0
HAUTE ECOLE VALAISANNE	11/25	{Path} FPGA_Rack_v1_0.sch

UART & FTDI





FPGA Rack HES-SO // Valais Wallis	UART	DES	{Date} zas
		REV	V1.0
HAUTE ECOLE VALAISANNE		12/25	{Path} FPGA_Rack_v1_0.sch