

TO/FROM MEZZANINE BOARD

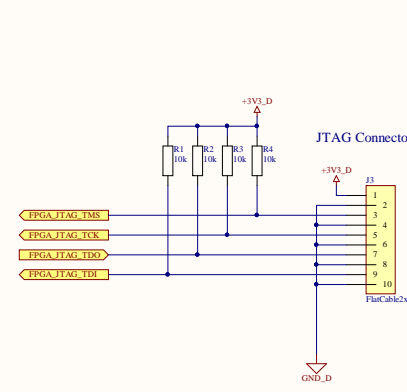
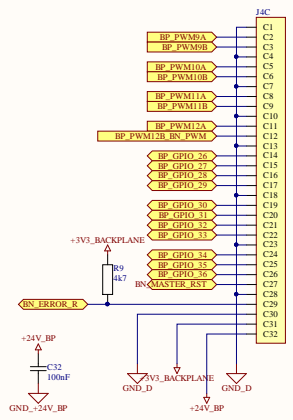
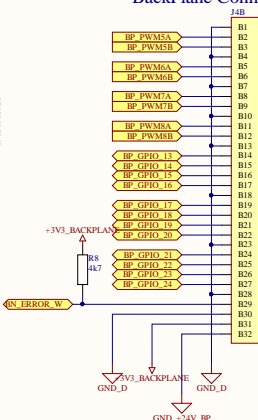
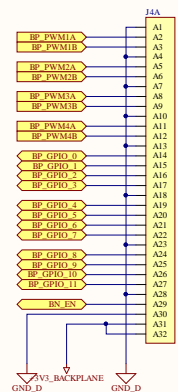
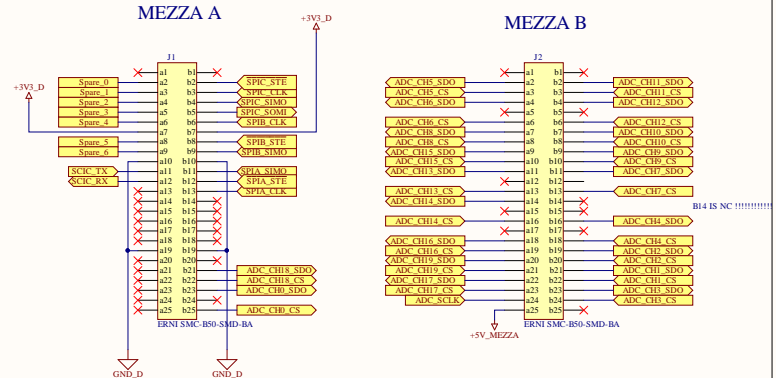
TO/FROM BACKPLANE

BackPlane Connector

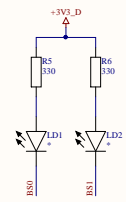
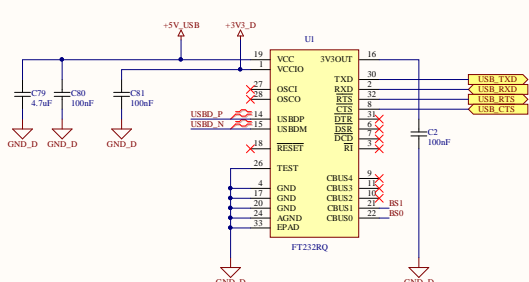
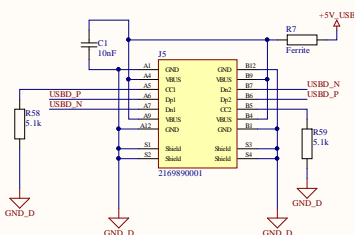
FPGA JTAG

MEZZA A

MEZZA B



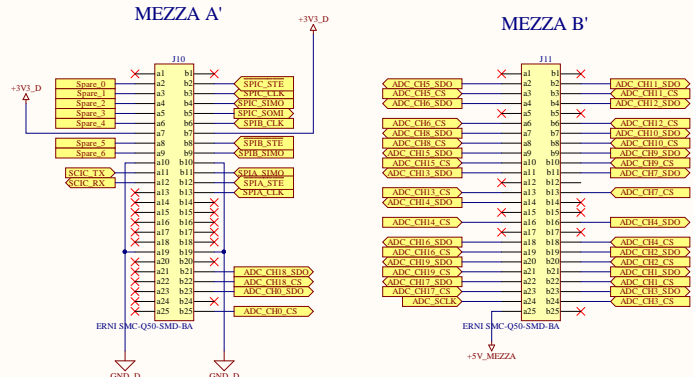
USB TO SERIAL UART



TO/FROM MEZZANINE BOARD (BOTTOM)

MEZZA A'

MEZZA B'



FPGA_POETIC.PrjPcb

Connector_0.SchDoc

Revision : SchematicRevisiorSheet * of *

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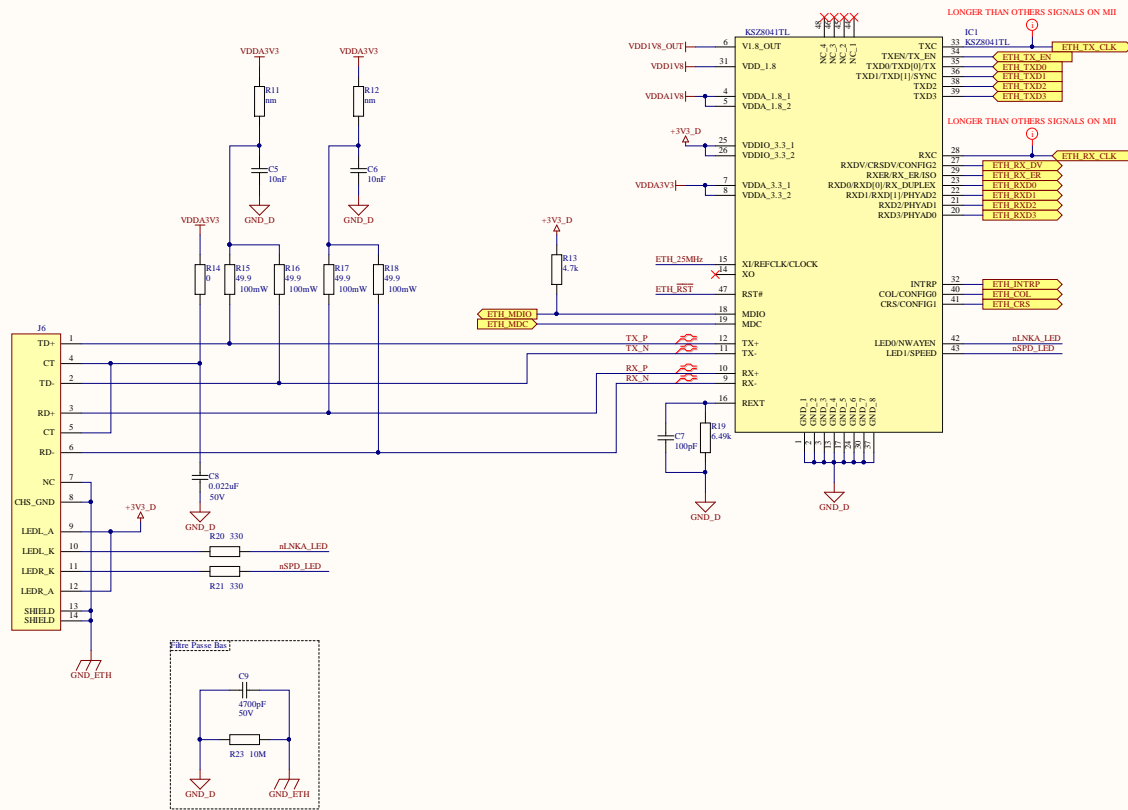
Hes·so VALAIS WALLIS

Date : SchematicDate

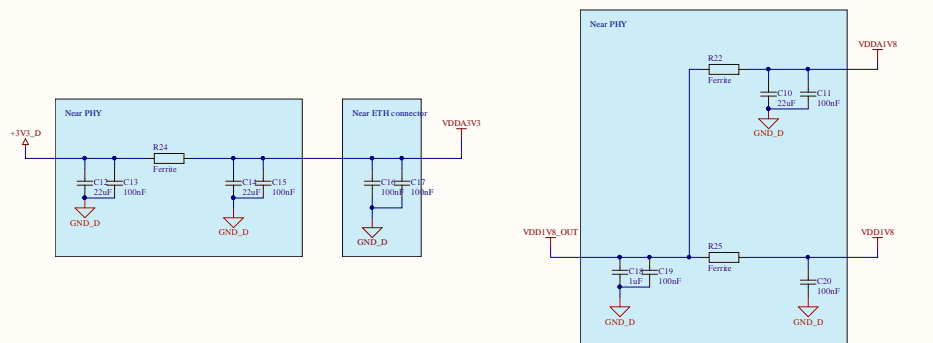


Design by : SchematicDesigner

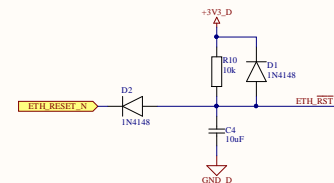
RJ45 & ETHERNET PHY KSZ8041TL



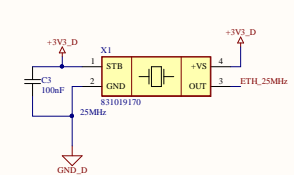
DECOUPLING & SUPPLY SPLIT



PHY RESET



PHY OSCILLATOR



FPGA_POETIC.PrjPcb

Ethernet_0.SchDoc

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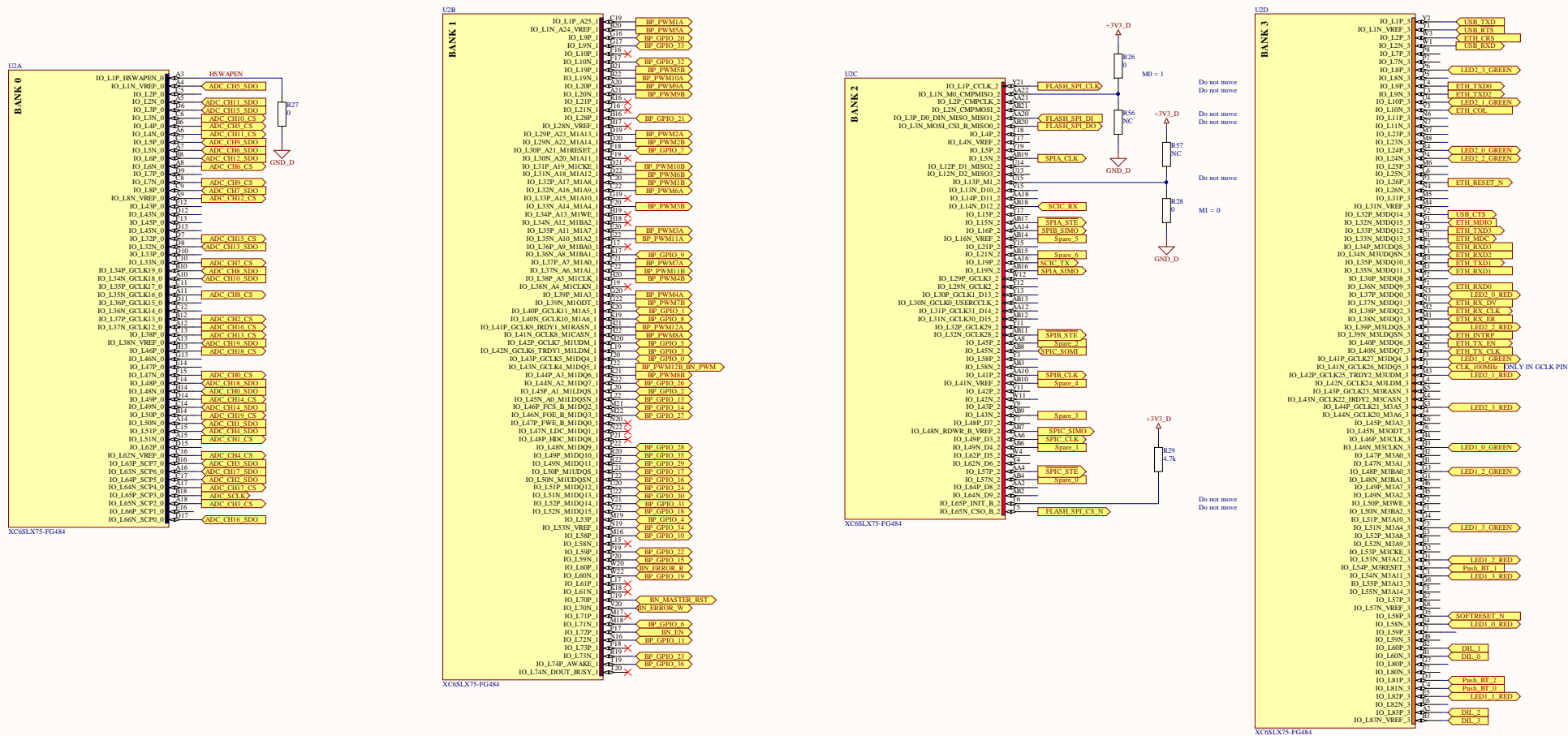
Date : SchematicDate

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Revision : SchematicRevisionSheet * of *

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FPGA_POETIC.PrjPcb

FPGA_0.SchDoc

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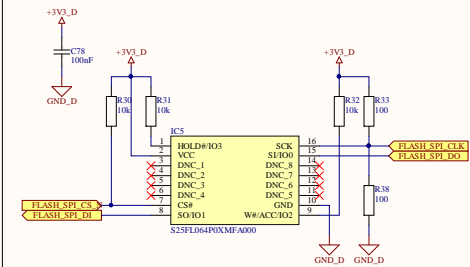
Hes·so VALAIS WALLIS

Date : SchematicDate

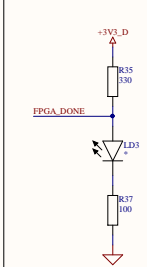


Design by : SchematicDesigner

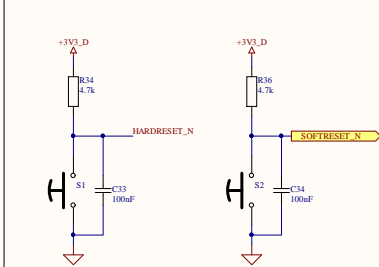
FPGA FLASH



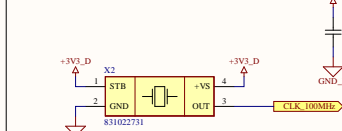
FPGA DONE LED



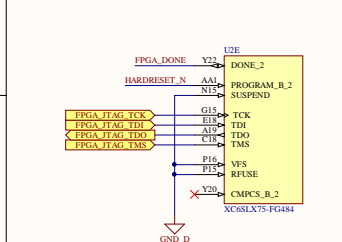
RESET BUTTONS



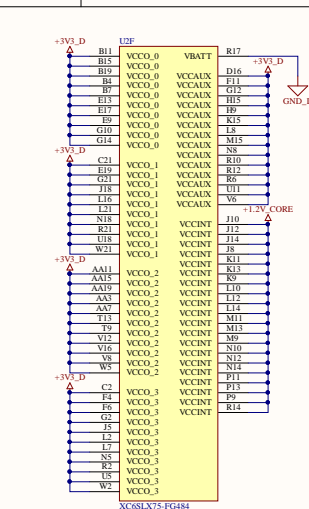
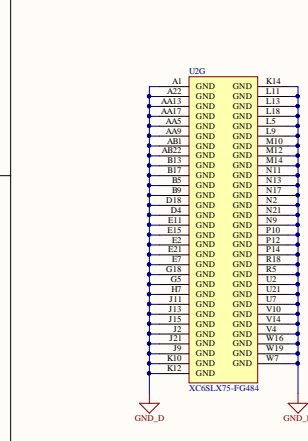
FPGA OSCILLATOR



FPGA CONFIGURATION PINS



FPGA SUPPLY PINS



FPGA DECOUPLING

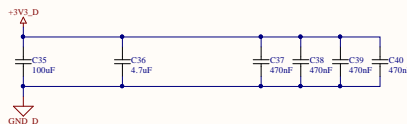
Table 2-2: PCB Capacitor Specifications

Ideal Value	Value Range ⁽¹⁾	Body Size ⁽²⁾	Type	ESL Maximum	ESR Range ⁽³⁾	Voltage Rating ⁽⁴⁾	Suggested Part Number
100 µF	C > 100 µF	1210	2-Terminal Ceramic X7R or X5R	5 nH	10 mΩ < ESR < 60 mΩ	6.3V	GRM32ER60J107ME20L
4.7 µF	C > 4.7 µF	0805	2-Terminal Ceramic X7R or X5R	2 nH	10 mΩ < ESR < 60 mΩ	6.3V	
0.47 µF	C > 0.47 µF	0204 or 0402	2-Terminal Ceramic X7R or X5R	1.5 nH	10 mΩ < ESR < 60 mΩ	6.3V	

PCB Capacitor Substitution Rules:

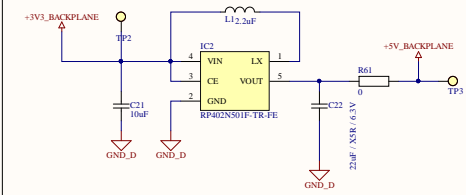
1. Values can be larger than specified.
2. Body size can be smaller than specified.
3. ESR must be within the specified range.
4. Voltage rating can be higher than specified.

VCC0 Bank 0 Decoupling
LX75, LX100, LX150 -> 1x100nF / 1x4.7uF / 2x470nF

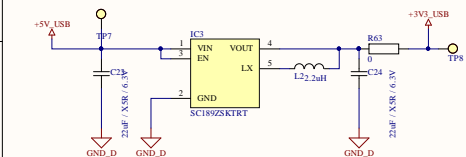


VCC0 Bank 1 Decoupling
LX75, LX

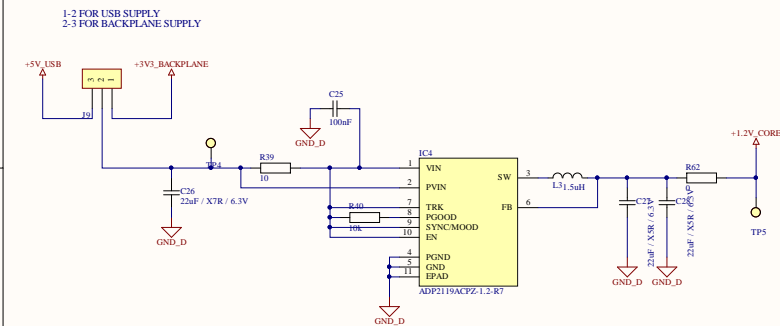
5V FROM 3V3 BACKPLANE



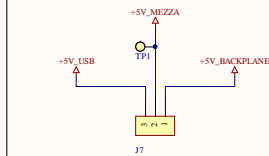
3V3 FROM 5V USB



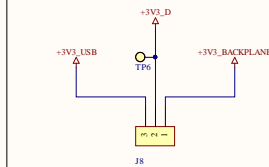
1V2 FPGA CORE SUPPLY



5V SUPPLY SELECTOR



3V3 SUPPLY SELECTOR



FPGA_POETIC.PrjPcb

Supply_0.SchDoc

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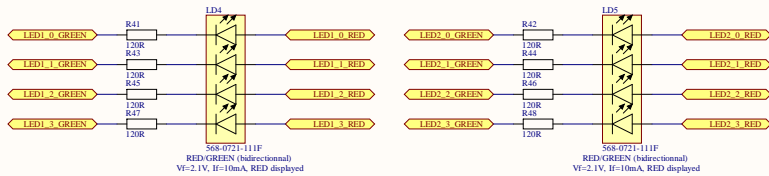
Hes·SO VALAIS WALLIS

Date : SchematicDate

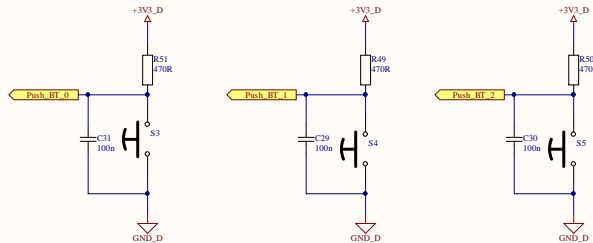


Design by : SchematicDesigner

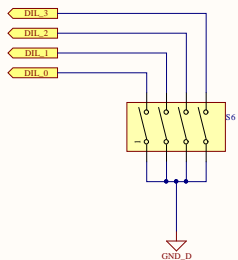
BI-COLOR LED



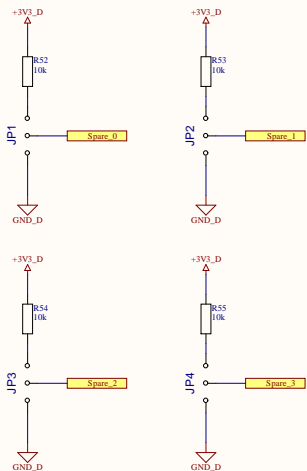
PUSH BUTTONS



DIL SWITCH 4 POS



SPARE PULL UP/DOWN HEADER



FPGA_POETIC.PrjPcb

UserInterface_0.SchDoc

Revision : 1.0

Sheet * of *

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Hes·SO VALAIS WALLIS

Date : 02.06.2021

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Design by : Jean Nanchen