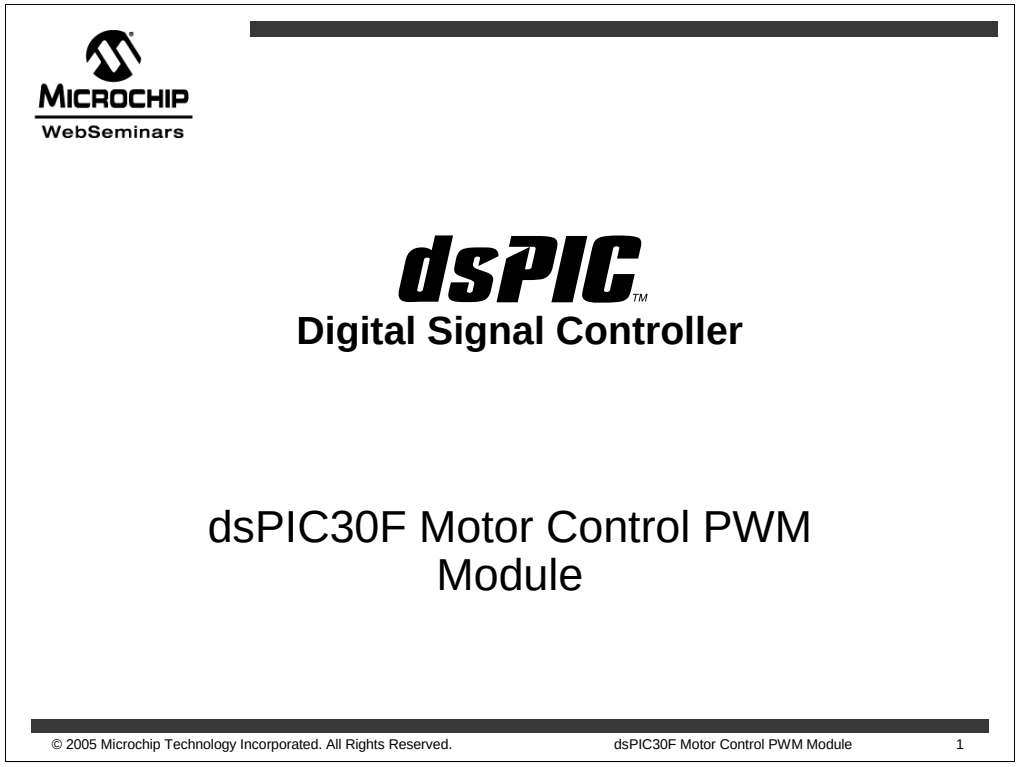
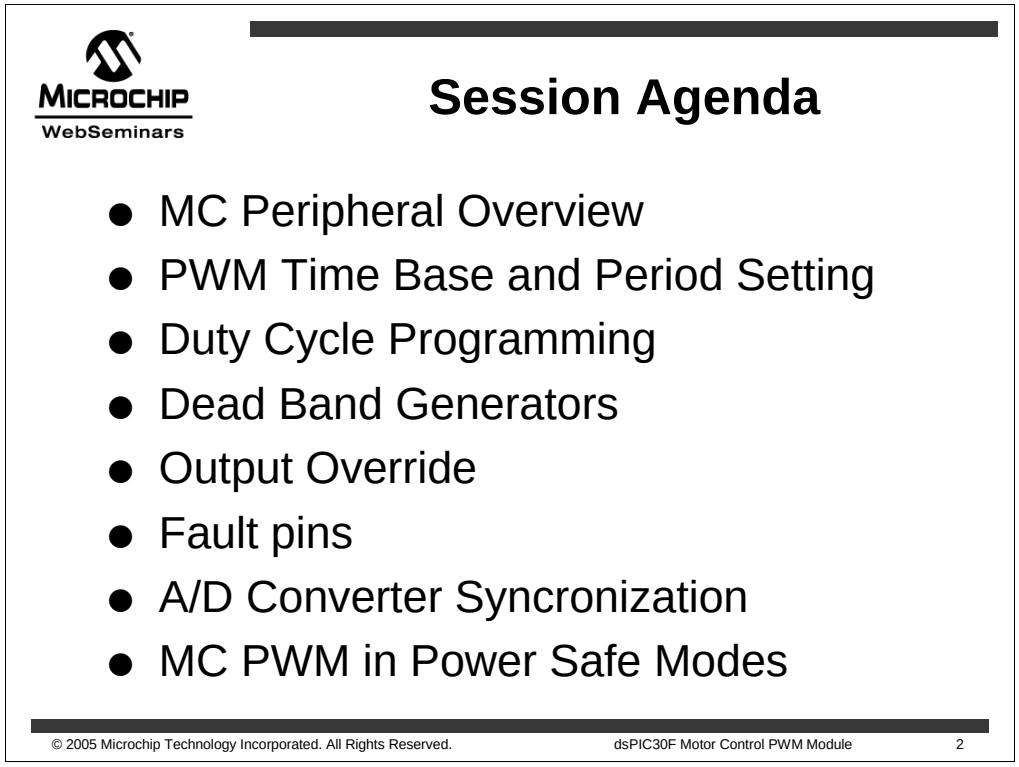


Welcome to the dsPIC30F Motor Control PWM Module web seminar.

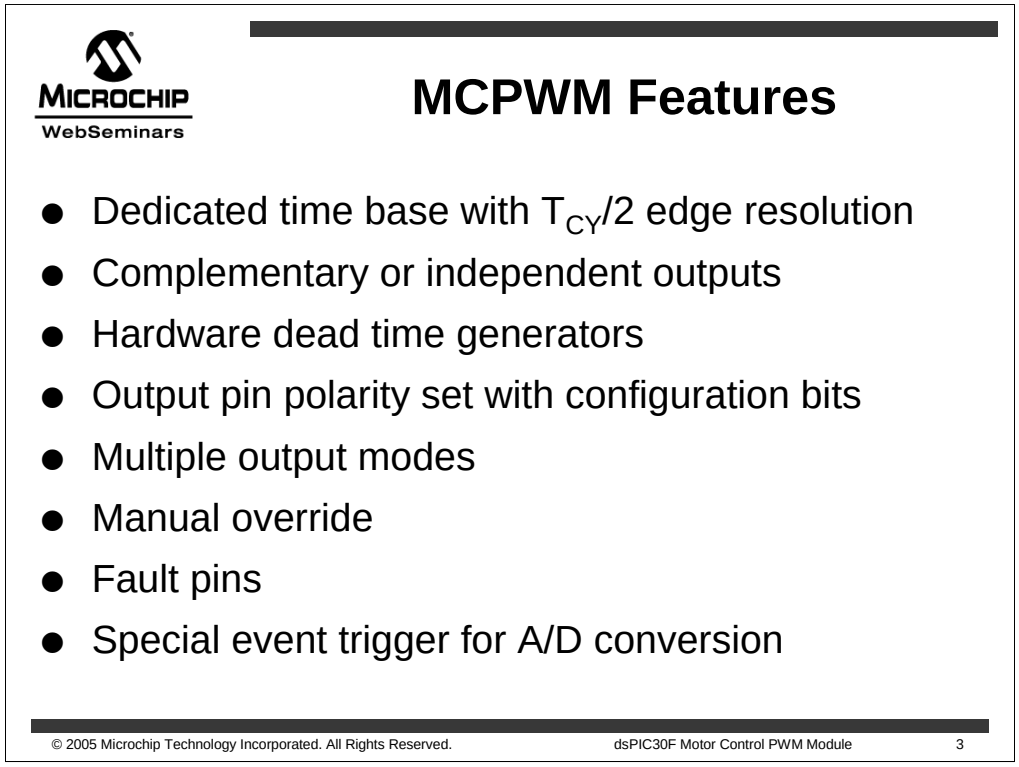


Here is the agenda for today's seminar.

We will talk about the general structure of the peripheral and then we will have some details on the period generator and the duty cycle generators. The different drive capabilities of the output pins will be targeted and we will see how dead bands help in preventing damages or even the destruction of the external power stages. The fault pins can help us in this as well.

The A/D syncronization capability permits us to select the exact timing for starting the conversion.

At the end we will see how the peripheral behaves in the idle and sleep modes, that is in the power save modes.



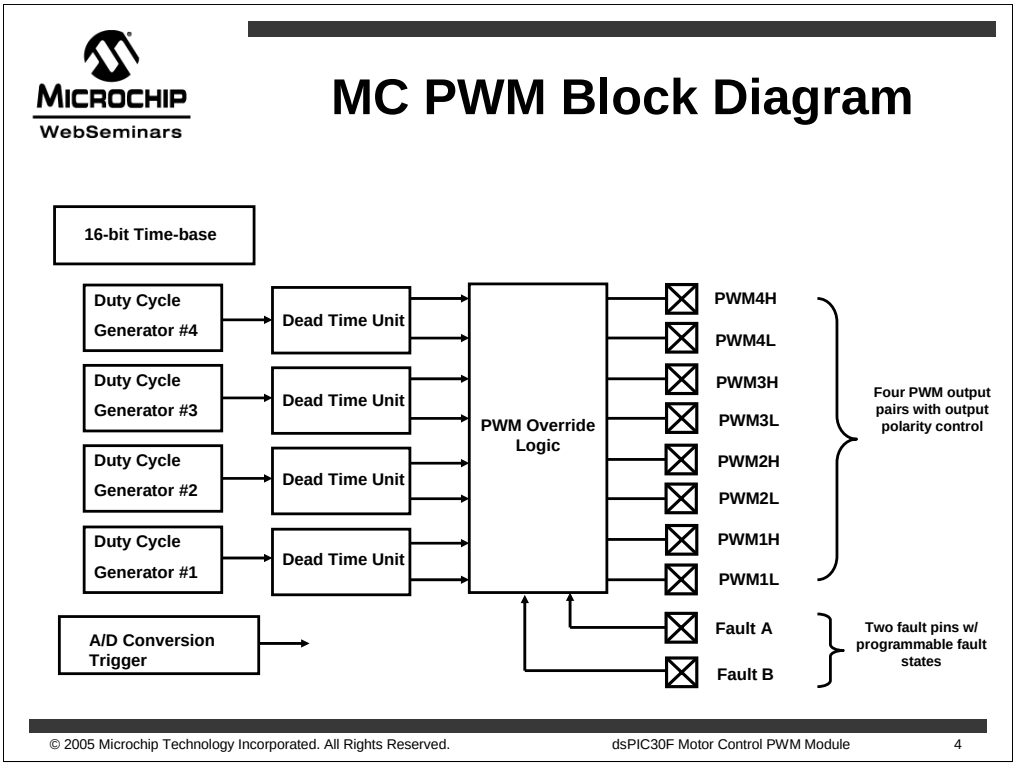
The peripheral uses a dedicated timer for the generation of the PWM frequency. Its maximum input frequency is the instruction cycle frequency Fcy, but the duty cycle edge resolution can be enhanced half an instruction cycle for improved performances.

The peripheral pins can be coupled to give complementary outputs or used as single ended pins. In both cases the polarity (active high or active low) can be set as part of the configuration bits.

The implementation of external bridge power circuits requires that the peripheral should be capable of adding dead times between the commutations of the two complementary outputs in order to avoid short circuits through the power transistors. An added safety feature are the fault pins that are capable of disabling in a very short time the PWM outputs so that “fault” conditions in the power section of the board are not destructive to the circuitry.

In many motor control applications, like BLDC motors, it is required that the firmware be able to replace the PWM output with a constant low or high output signal: the manual override function is what helps in these situations.

For sensorless control of BLDC motors, the necessity of synchronizing the PWM output to the A/D converter arises. This allows the designer to select the correct timing for sampling the back emf to determine the run-time position of the rotor.



The high level block diagram of the Motor Control PWM module is shown.

We can see the PWM period generator at the top left, the 16-bit Time Base.

The dsPIC is capable of generating up to four output PWM signals, with the same period but different duty cycles. There are four such units in devices with 64 or more pins.

The Duty cycle generators are followed by the dead time units. The outputs from these units go through the PWM Override Logic and finally to the output pins. The output pins are grouped in pairs, to facilitate driving the low side and high side of a power half-bridge.

The safety fault feature is directly connected to the output stages of the peripheral in order to have the smallest possible response time.

At the bottom left we can also find the A/D Conversion trigger block.

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MC-PWM Timebase

- Dedicated 15-bit time-base, period register
  - Up count (edge align), up/down count (center align)
- PWM resolution : Tcy/2 For Example:
  - At 20 MIPS: 19.5 KHz @ 11 bit
    i.e. 11 bit resolution above audible frequencies
  - PWM interrupt every 1-16 periods
- 1:1, 1:4, 1:16, or 1:64 prescaler options

PTCON Register

PTEN	-	PTSIDL	-	-	-	-	-
bit15	14	13	12	11	10	9	bit8

PTOPS3	PTOPS2	PTOPS1	PTOPS0	PTCKPS1	PTCKPS0	PTMOD1	PTMOD0
bit7	6	5	4	3	2	1	bit0

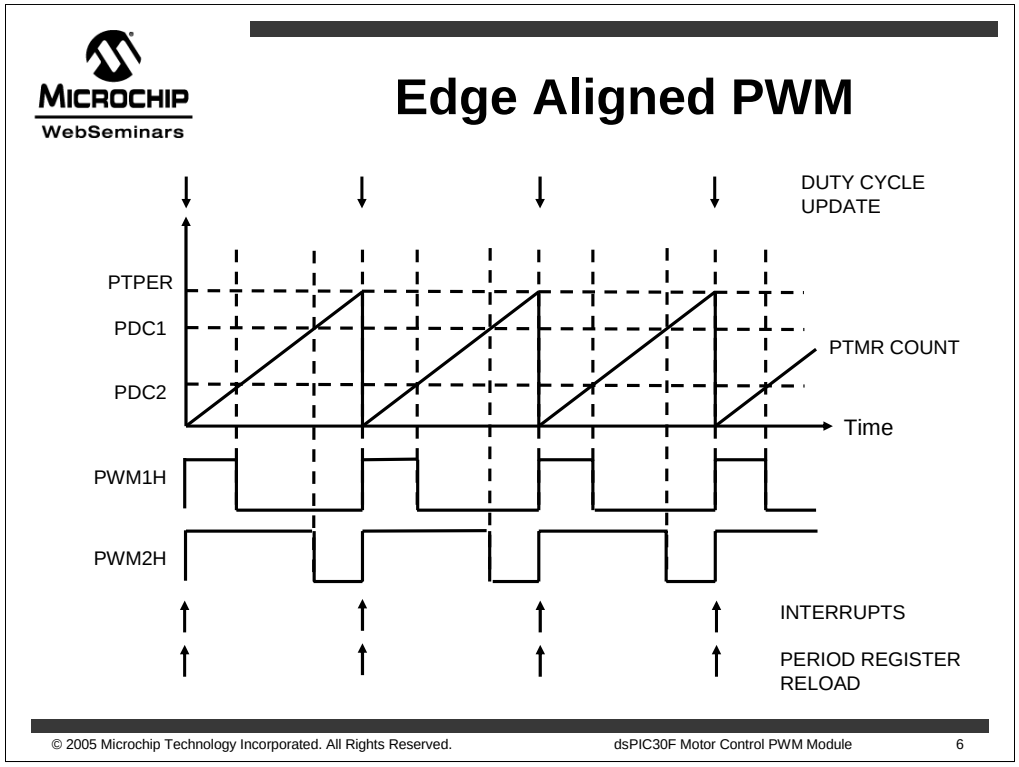
 dsPIC30F Motor Control PWM Module 5

The time base is generated by a 15 bit timer called PTMR with a prescaler which divides the timebase frequency by 1, 4, 16 or 64. Bit 15 of the PTMR register indicates the count direction: 0 indicates an upward count and 1 indicates a downward count. This feature allows the unit to generate edge aligned and center aligned PWM waveforms, as we will see shortly.

The timer content is continuosly compared with the value of the preset period register. When a period match occurs, an interrupt to the CPU is generated. The module can be configured to generate an interrupt after up to 16 period match events. This feature reduces the CPU overhead, since in many applications the duty cyle value need not be changed one every PWM cycle.

Though the clock to the time base timer is Tcy, the duty cycle resolution is Tcy/2; this feature can be utlized to obtain finer PWM resolution at lower device operating speeds, e.g., 11 bits of resolution at 19.5 Khz using a 20 MHz clock.

The PTCON register is used to switch the timer on and off, to halt it in IDLE mode, to set the prescaler and postscaler value and to select one of the four operating modes of the peripheral: free running mode, single event mode, continuos up/down mode, countinuos up/down with double PWM update. We will discuss these modes in the following foils.



The edge aligned PWM is generated when the time base is operating in Free Running mode

At the beginning of each period the outputs are driven active (high in this example). As soon as the timer value, while counting up, matches the value in any duty cycle register (PDC1, PDC2, and so on), the output is driven inactive (low here).

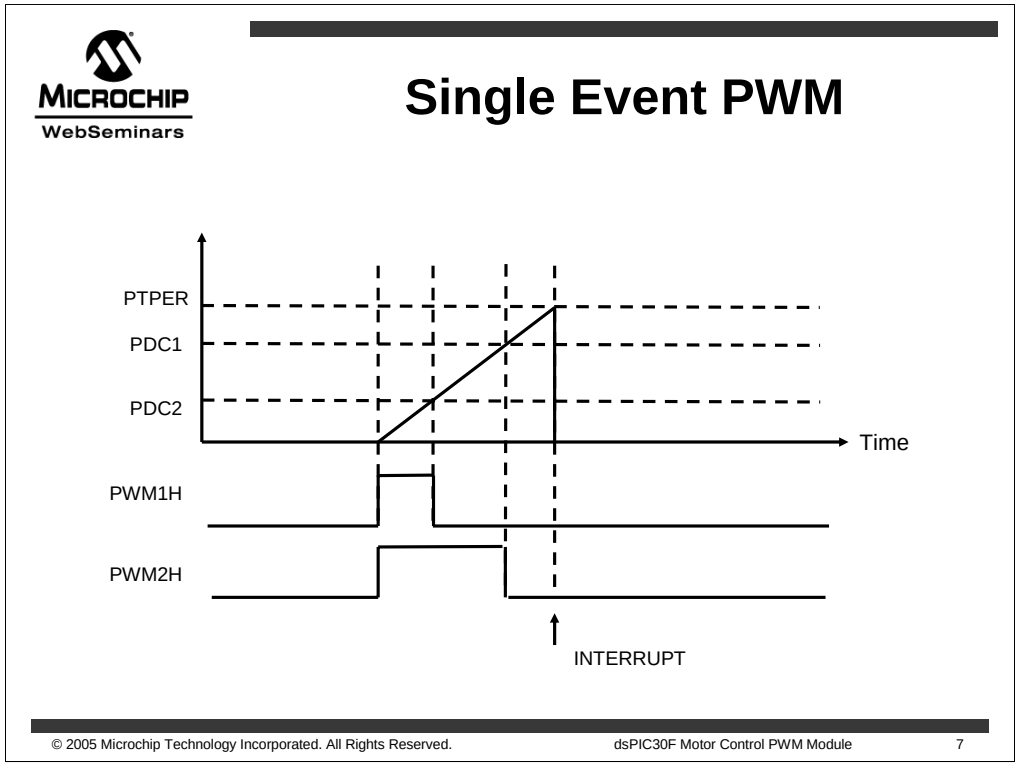
The duty cycle registers are updated when the timer register is reset to zero and start counting up again. The application software can update the duty cycle value at any time during the period.

Duty cycles from 0% to 100% are allowed.

An interrupt is generated, if enabled, when the timer resets, due to a match with the PTPER register.

In order to avoid glitches the duty cycle registers are double buffered.

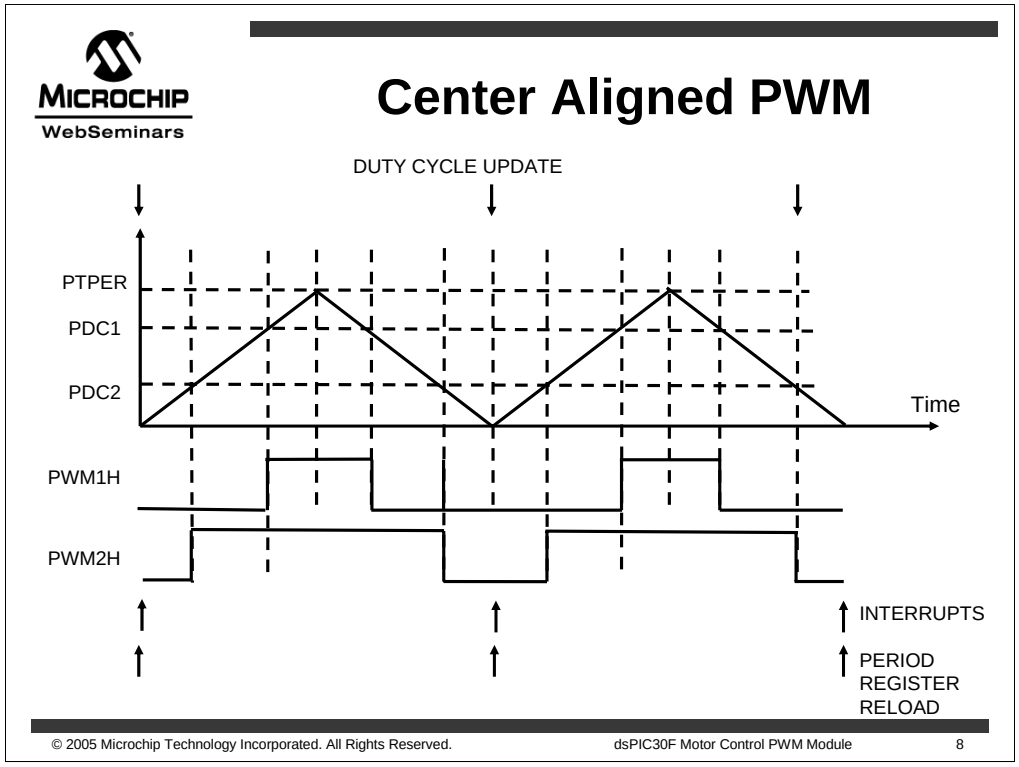
In the figure only two out of four duty cycle registers and outputs are shown.



The Single Event feature alllows to generate a single output pulse. Setting the PTEN enable bit in the PTCON register the timer starts counting up; the bit will be automatically reset when the timer resets and stops counting.

An interrupt is generated, if enabled, when the timers resets.

When the PTEN bit is set, the I/O pins are driven to their active state: they will be driven to the inactive state again when a match with a duty cycle register occurs.

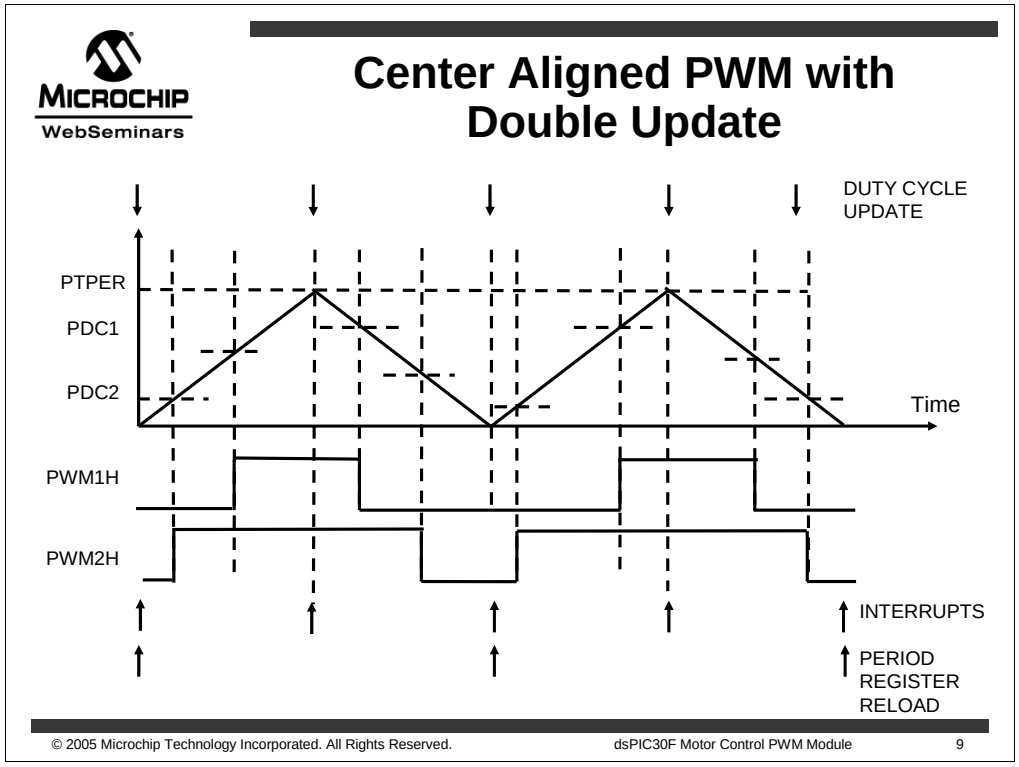


In the center aligned mode, the time base is an up-down counter: it starts from zero, counts up to the value in the period register and then counts down to zero and so on. Bit 15 in the timer register indicates the counting direction. In this mode, the PWM period is twice the time base period.

The duty cycle buffers are updated when the timer is reset to zero; the interrupt flag is set at the same time.

As you can see from the figure, the PWM waveform is centered around the instant in time when the timer reaches its maximum value and start counting back: from this the name “center aligned”.

Although the PWM frequency is half the edge aligned PWM, this mode is very useful because it avoids the simultaneous switching of all the PWM outputs at the same time. This is not a problem for the device itself, but since power switches are connected to these outputs, the switching current can be quite high and may require an oversized power supply.



This mode is quite similar to the previous one. The time base operates in a continuous up/down count mode.The main difference is that the duty cycle buffer update is done twice per period: when the timer reaches zero and when it counts to the upper limit.

The advantage is that the output PWM waveform is no more symmetrical.

Again the interrupt flags are set when the timer reaches zero.

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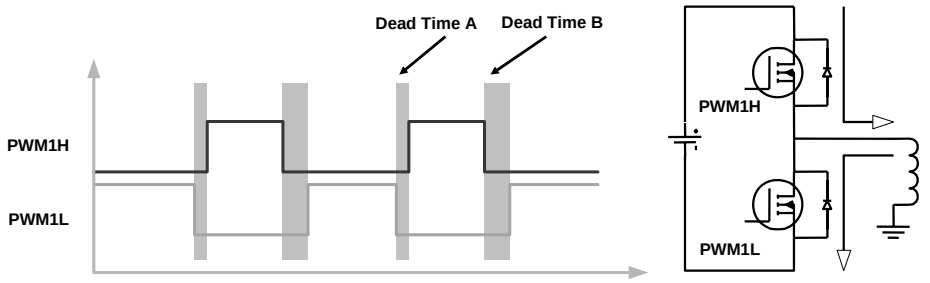
Dead Time Control

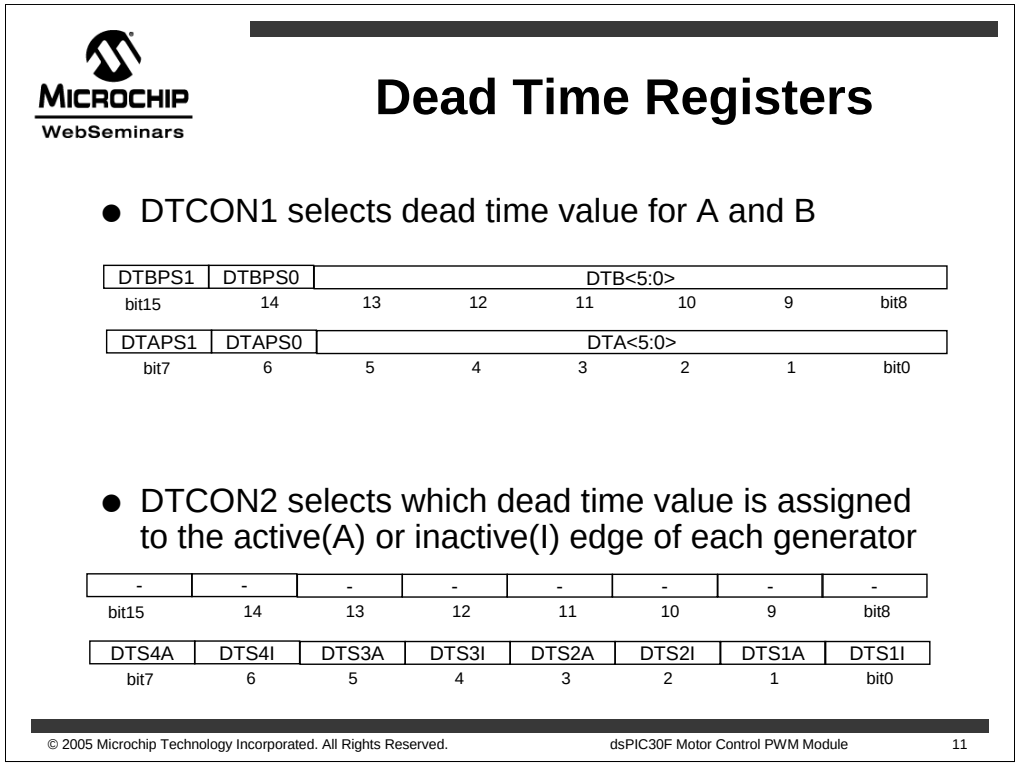
- Applies only to pin pairs in complementary mode
- Two programmable dead times
- One dead time per pair for multiple inverters OR
- Two dead times per pair for distortion optimization
- Tcy minimum resolution with four pre-scale options



The dead time unit immediately follows the duty cycle generators and applies only in complementary mode. Since power switches in the high and low sides usually have different on and off times, if both were operated at the same time it is possible that the two transistors in a complementary pin-pair are switched on simultaneously for a short duration: this causes a short circuit betweeen the supply rails and a huge amount of current flows through the devices, potentially causing damage to the system.

The solution is to delay the switching of the two transistors by adding a small amount of time between the falling edge of one pin and the rising edge of the other.

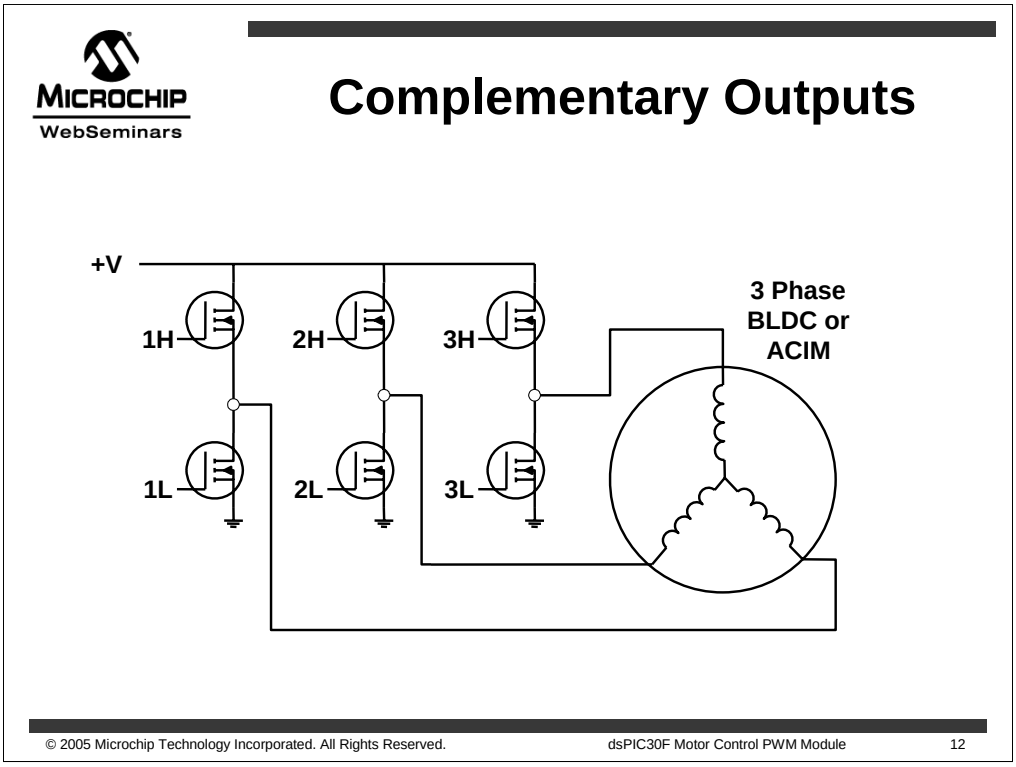
You can select one or two different dead times; the devices with 6 output pins provide one dead time whereas those with 8 outputs have two. Having 2 dead time units is useful in 2 ways. First, to compensate for the difference in the switching times of the 2 transistors in the same complementary pair. Second, to enable control of different motor drive circuits using different complementary pin-pairs.



Two registers are used to enable and program the dead band generator. It is based on a 6 bit down counter with a maximum clock frequency of Fcy optionally divided by a 1:2, 1:4 or 1:8 prescaler.

Register DTCON1 selects the period match value and the prescaler for both dead time generators, called A and B.

Register DTCON2 allows selection of the dead time unit (A or B) for each output pin (low and high) and for each edge (rising an falling). Thus, the designer has full control over dead time insertion.



Each output pin pair can be programmed in the independent mode or in the complementary mode.

In the independent mode the dead time generators are disabled and there is no restriction in the state of the pins for any output pin pair.

The complementary mode is very useful in driving loads such as the inverter in this figure, that could be used for any three phase load, for example: Brushless DC Motors and Induction Motors. As we have seen, dead time insertion helps preventing short circuits between the two rails through each couple of transistors.

Through device configuration bits, the reset-state polarity of the output pins can be selected.

The HPOL bits in the BOR/POR configuration register determines whether the high-side output pins must have an active high or low output polarity. The LPOL bits in the same register set the low-side active high or low polarity.

Moreover, at reset the peripheral output pins can be controlled by PORT registers, that is, they are normal input-output pins initilized as inputs, or they can be directly controlled by the Motor Control PWM module as output pins.

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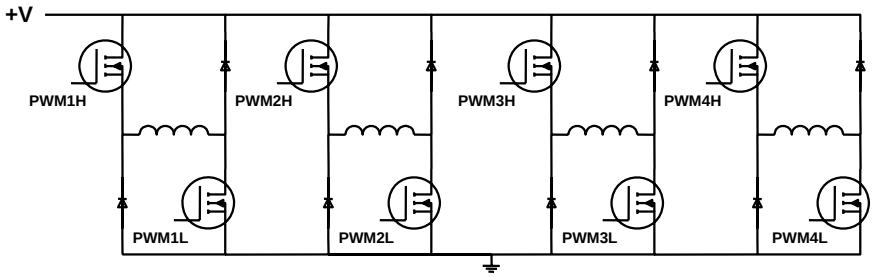
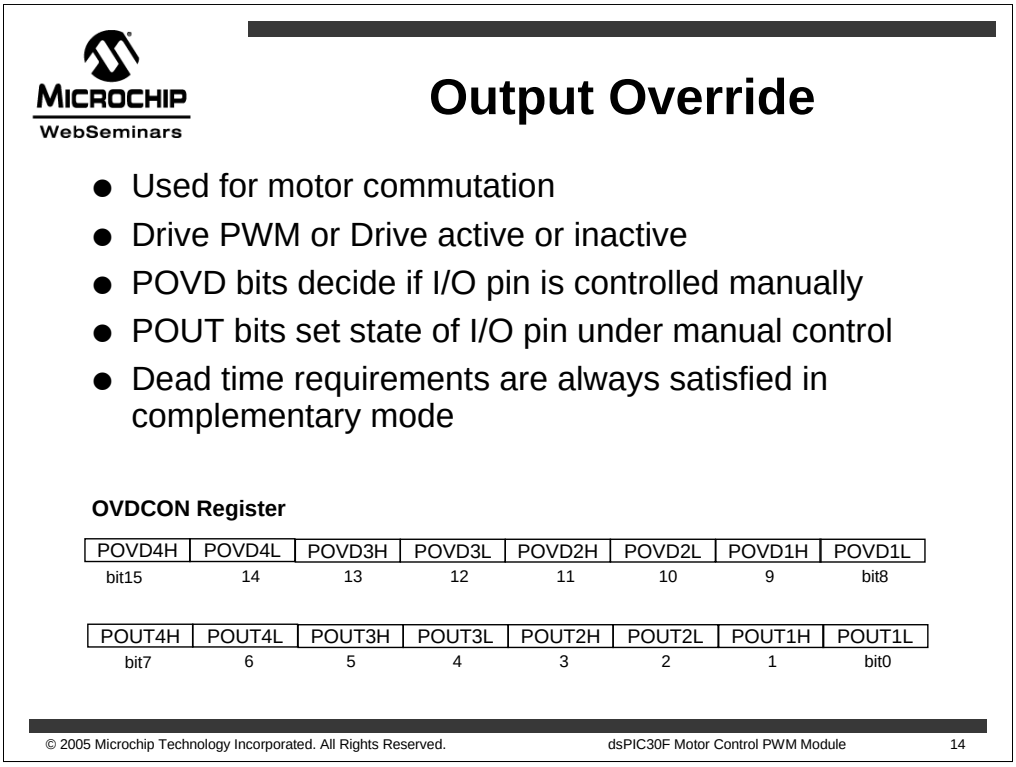
Independent Outputs

- Independent mode is used for switched reluctance motors
- Special inverter circuit to control current in SR motors
- Independent mode enables both devices to turn on



This is an example where all the four PWM outputs are used in independent mode to drive a Switched Reluctance motor, where each pair of outputs drives one phase of the stator.



The manual override control bits allow the user to implement motor commutation. Through the control bits, a particular output pin may be programmed to receive the PWM signal from the duty cycle generator, driven active, or driven inactive. There is a POVD control bit for each PWM output pin. If this bit is cleared, the pin will output a PWM signal. If the POVD bit is set, the pin will be controlled manually. There is a POUT bit for each PWM pin that sets the state of the pin when the output is manually controlled.

Restrictions for complementary outputs cannot be violated through manual PWM control. When the module is operating in the complementary mode, the signals on each high-side ouput pin will take priority and the proper dead time will always be inserted.

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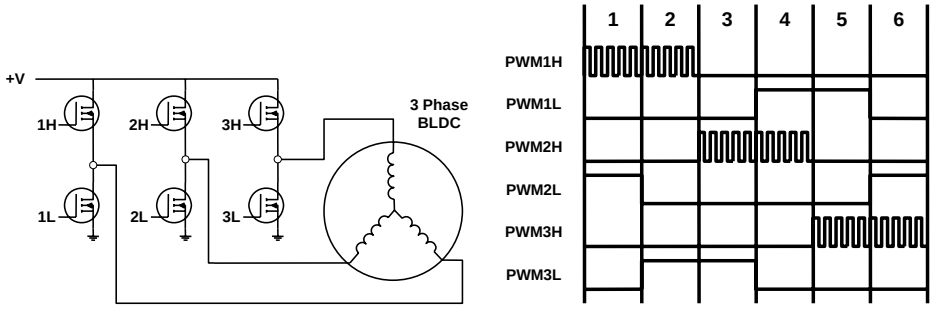
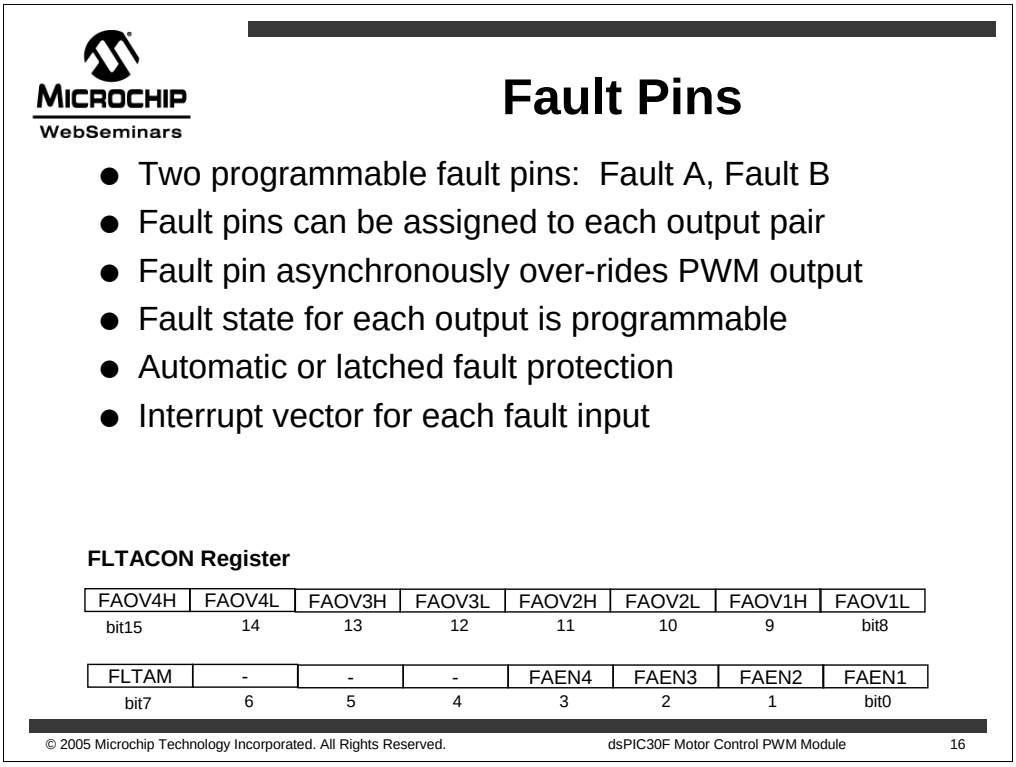
Output Override

- Using PWM for 6-step modulation
  - Energize BLDC motor coils based on measured rotor position
  - PWM override register used to control active transistors -- duty cycle sets current



This is a typical application of the override capability. In order to be able to control the rotor speed, the PWM is output on the high side transistors: its duty cycle will determine the medium voltage applied to the motor and hence its speed. The required software overhead is really minimum.



The fault pins are safety features: if asserted, they will drive the PWM I/O pins to a defined state. The action takes place without software intervention, thus allowing fast and safe response to system failures.

In the smallest devices you can find one fault pin (FLTA), the bigger ones have them all (FLTA and FLTB). They are active low inputs so that you can easily wire-OR many different sources.

The FAEN bits allows you to select if any output pin-pair will be controlled by the fault pins when a fault occurs.

If the functionality is enabled, as soon any fault pin is asserted, the PWM output pins will go active or inactive according to the content of the upper part of the FLTACON (or FLTBCON) register.

Each fault pin has its own interrupt vector, flag and interrupt priority register.

There are two different operating modes. In the latched mode as soon as the fault pin is asserted, the PWM output will get the value defined in the FLTxCON register. The outputs will remain in this state until the fault pin is deasserted and the corresponding interrupt flag is cleared.

In the automatic mode, the outputs will keep the fault value as long as the fault pin is asserted. When released, at the beginning of the following PWM period, the output will return to normal PWM operation.

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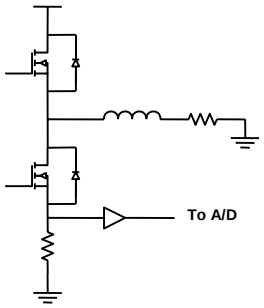
A/D Synchonization

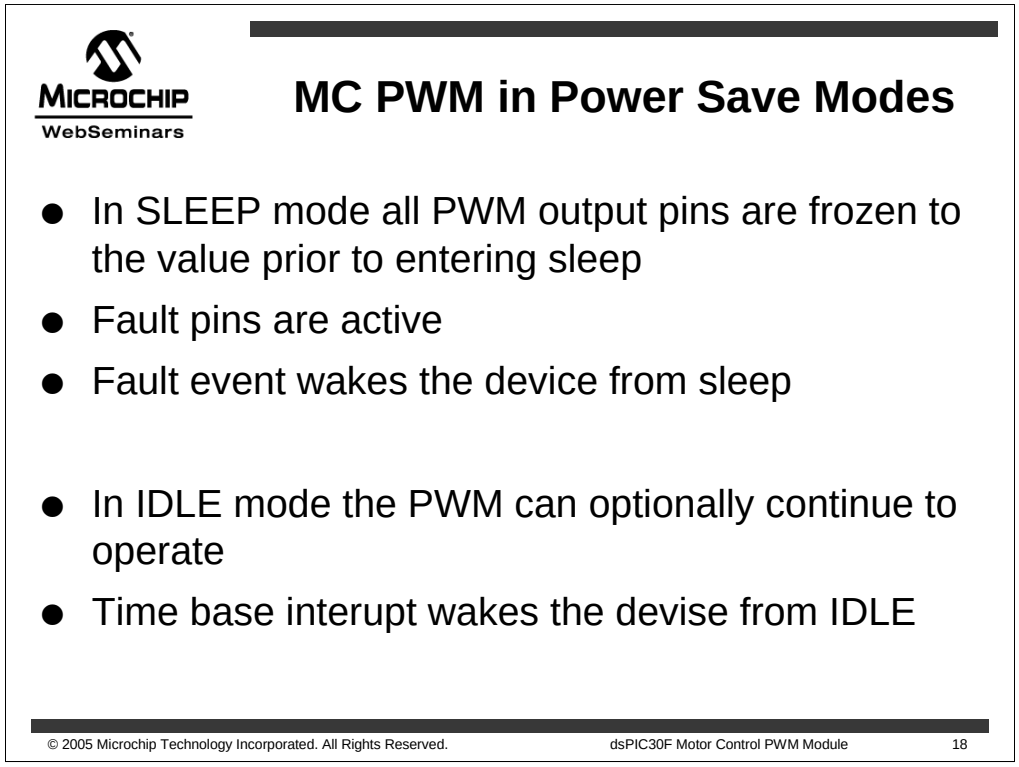
- SEVTCMP register sets A/D conversion start time
- SEVTDIR bit sets direction of PTMR
- Ensure A/D properly captures shunt current
- Minimize control loop update delay



The PWM module has a special trigger that allows the A/D converter to be synchronized to the PWM time base. This trigger will start the conversion phase of the A/D block, in order to minimize the delay between getting the A/D conversion result and updating the duty cycle value.

The Special Event Compare Register is loaded with a number which is compared to the content of the time base timer, while this one is counting up or down. The counting direction is set by the Special Event Direction bit. As soon as there is a match between the two registers, the trigger is generated and the A/D conversion is started.

This feature is very useful for synchronizing with the phase drive signals the reading of the shunt currents or the reading of the back emf in a sensorless BLDC motor control.



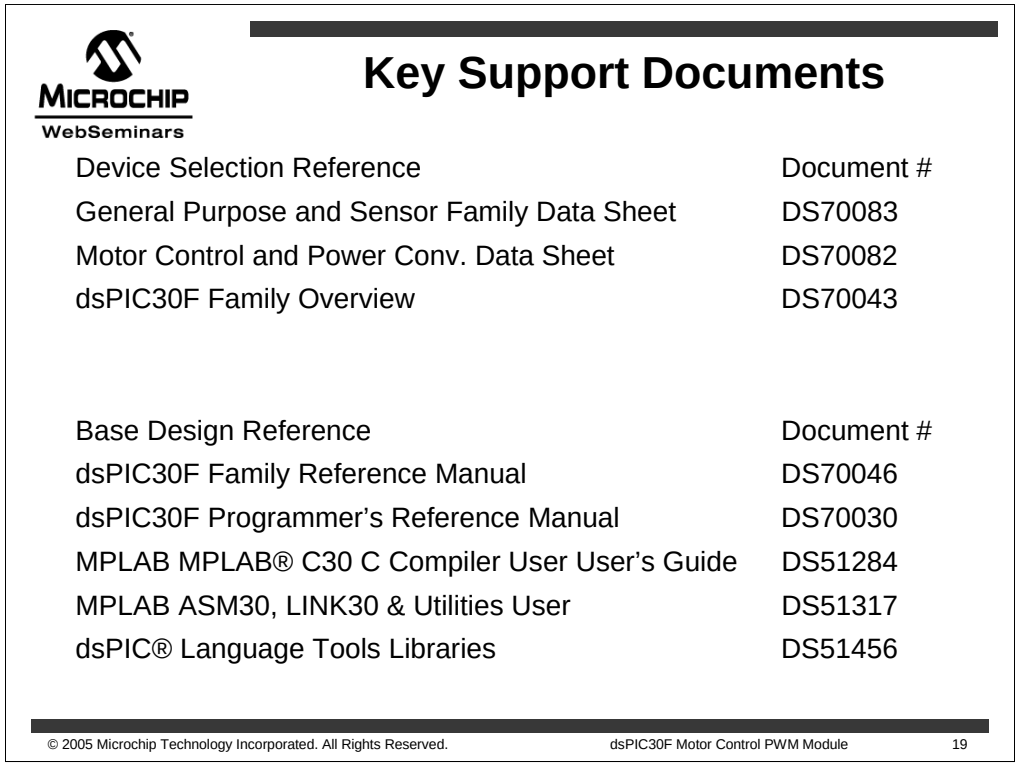
Finally, let us study the oepration of the peripheral in device power save modes.

In sleep mode the PWM output pins will retain the value that they had when entering sleep. It is your responsability to put the output pins in a known state before entering power save: this can be very important for some kind of loads.

During sleep the fault pins, if enabled, will continue to control the outputs, so that if any fault input is asserted the output PWM pins will be driven to the state programmed into the Fault Control register. If the fault interrupt enable pin is set, the device will be waken up from sleep when the fault pin is asserted. If the interrupt priority is higher than the current CPU priority the ISR will be served, otherwise the code execution will continue from the next instruction following the PWRSAV instruction.

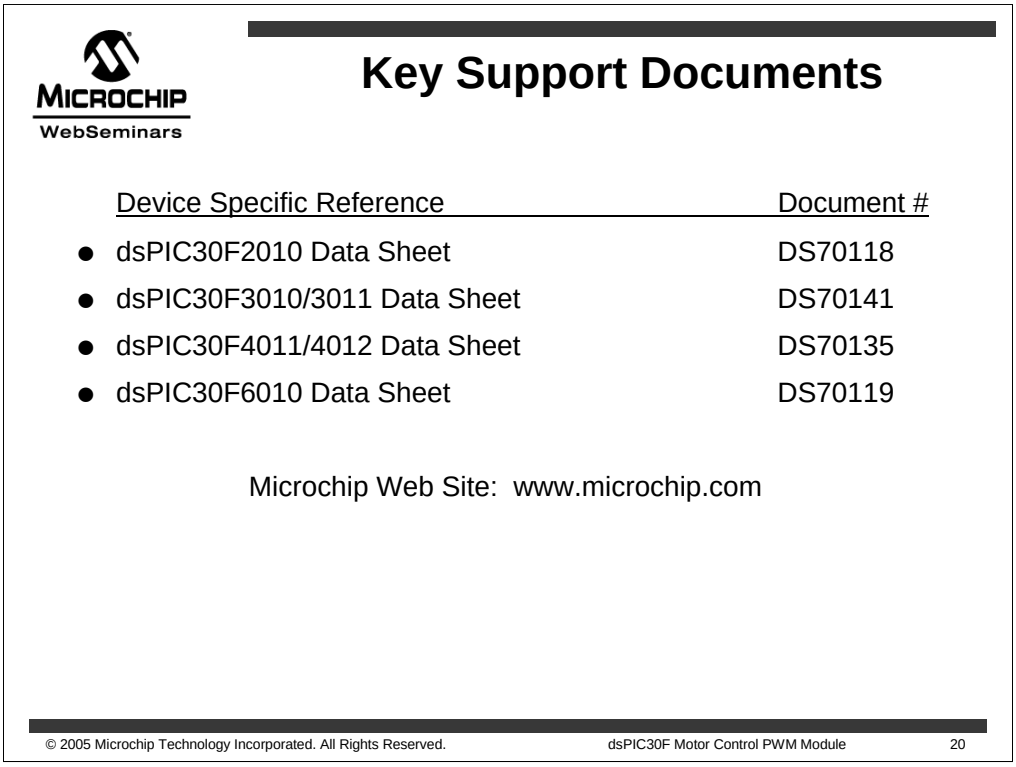
In IDLE mode the PWM peripheral can be completely functional, according to the value of the PWM Time Base Stop in IDLE Mode Bit. If reset, the unit will operate normally. The time base interrupt, if enabled, will wake the unit. Code execution will continue with the ISR if the priority is higher than the CPU priority or with the next instruction after the PWRSAV instruction.

A last feature is worth mentioning, which is extremely useful during code debugging. The PWM pins can be optionally tri-stated when the emulator or the debugger is halted. You should install pull-up or pull-down resistor in order to ensure that the PWM outputs are diven to the correct state so that external hardware is not damaged.

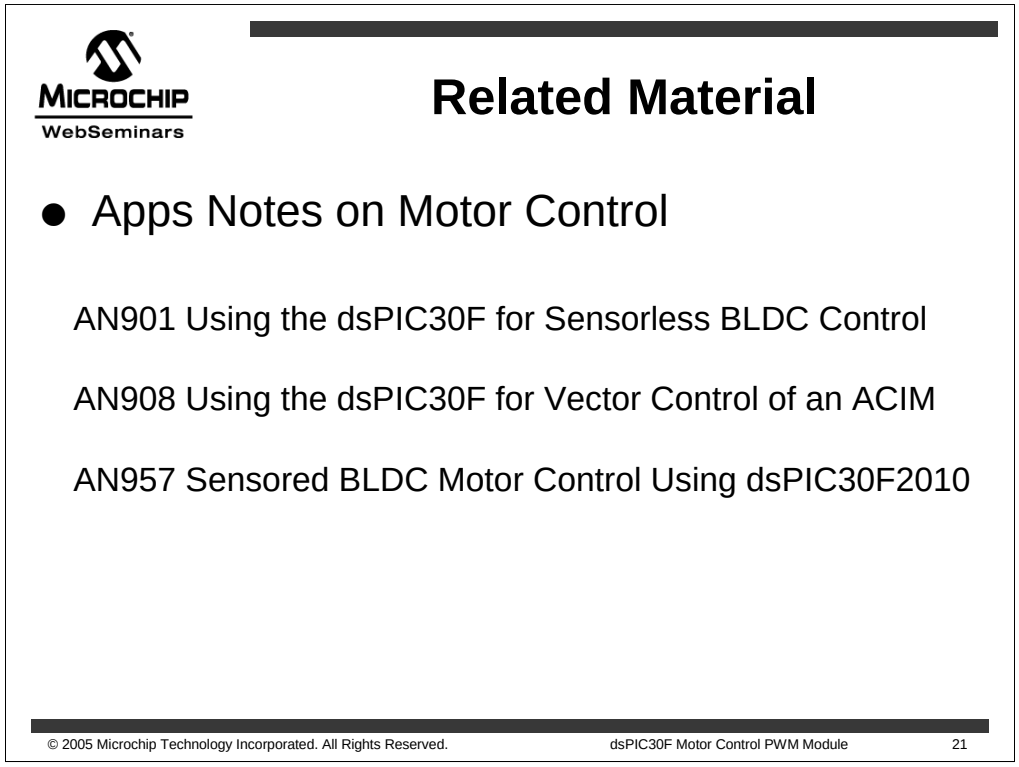


For more information, here are references to some important documents that contain a lot of information about the dsPIC30F family of devices.

The Family Reference Manual contains detailed information about the architecture and peripherals, whereas the Programmer's Reference Manual contains a thorough description of the instruction set.



For device-specific information such as pinout diagrams, packaging and electrical characteristics, the device datasheets listed here are the best source of information.



We also have some application notes on motor control, in which the peripheral is extensively used.

All these documents can be obtained from the Microchip web site, by clicking on the “dsPIC® Digital Signal Controllers” or “Technical Documentation” link.

This wraps up the seminar on dsPIC30F Motor Control Peripheral. Thank you for your interest in the dsPIC30F Family of Digital Signal Controllers.