Overview of UVM P6

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UVM Project – Serial Peripheral Interface (SPI) Master Controller

The SPI Master is a synchronous digital circuit that implements SPI protocol in Master mode.

Supports full-duplex communication (simultaneous transmit/receive).

Uses an 8-bit data width (MSB-first by default).

Configurable clock divider (CLK_DIV) for sclk generation.

Implements a simple state machine with IDLE and TRANSFER states.

Simple handshaking (start, busy, done) for controller interaction.

Fixed SPI Mode 0 (CPOL=0, CPHA=0).

Single-slave support (one cs_n line).

Continuous sclk during transfer, gated to idle-low when inactive.

UVM Project

Objective: Develop a complete DV on a DUT using UVM, including the test plan.

Please copy spi.tar.gz to your local area.

Perform the steps at the right.

Enable detailed debug logging by setting simulation verbosity to +UVM_VERBOSITY=UVM_HIGH

1. cd <your_local_area>
2. cp ~seanooi/F/dv/uvm/spi.tar.gz .
3. gtar -zxvf spi.tar.gz
4. cd spi
5. vim README.txt
6. source spi.setup
7. cd sim
8. Perform the steps in TASKS.txt

UVM Classes

```
.
├── spi_agt.sv
├── spi_cov.sv
├── spi_drv.sv
├── spi_env.sv
├── spi.f
├── spi_if.sv
├── spi_mon.sv
├── spi_scb.sv
├── spi_seq.sv
├── spi_sqr.sv
├── spi.sv
├── spi_tb.sv
├── spi_test.sv
└── spi_tran.sv
```

```
class spi_agt extends uvm_agent;
class spi_cov extends uvm_component;
class spi_drv extends uvm_driver #(spi_tran);
class spi_env extends uvm_env;
class spi_mon extends uvm_monitor;
class spi_scb extends uvm_scoreboard;
class spi_seq extends uvm_sequence #(spi_tran);
class spi_sqr extends uvm_sequencer #(spi_tran);
class spi_test extends uvm_test;
class spi_tran extends uvm_sequence_item;
```

THANK YOU

For more information, contact Corporate Training Team at ext 595/517/512 or email corptraining@psdc.org.my