1. DESCRIPTION

MT5727H is a SoC based wireless power receiver which is designed for application withs up to 20W power delivery and can be configured as a wireless charging transmitter to provide power to other receiver. It is fully compliant with WPC Qi Specification (Version 1.2.4).

The AC input can be converted to fully programmable DC output voltage due to the magnetic induction charging technology.

Designed with ARM Cortex M0 processor, integrated with optimized and adaptive full synchronous rectifier control and special LDO, the chip achieves high efficiency, ultra-low bias current and very small power MOSFET R_{DSON}.

MT5727H is embedded with various protection features, such as FOD, over-voltage, over-current and over-temperature protection which guarantee the system reliability.

2. APPLICATIONS

- Smartphones and wearable devices
- TRx function for phones or power banks
- Other wireless power applications

3. FEATURES

- Power delivery: up to 20W
- Fully programmable output voltage and current limit
- Embedded with ARM Cortex M0 processor with 8KB SRAM and 16KB MTP
- AC input to DC output efficiency: up to 97%
- Reverse charging mode with integrated dual channel T_X demodulation
- Fully integrated bi-directional current sensing
- Embedded with various protection features: over-voltage, over-current, over-temperature protection, FOD
- Innovative output LDO with output clamping and fast response to line and load transient
- Qi 1.2.4 compliant and proprietary communication protocols support with hardware ASK and FSK modulation and demodulation
- Independent I^2C slave interface with additional configurable GPIOs
- Halogen free and RoHS compliant
- 2.82mm x 3.98mm 52-WLCSP

4. TYPICAL APPLICATION CIRCUIT

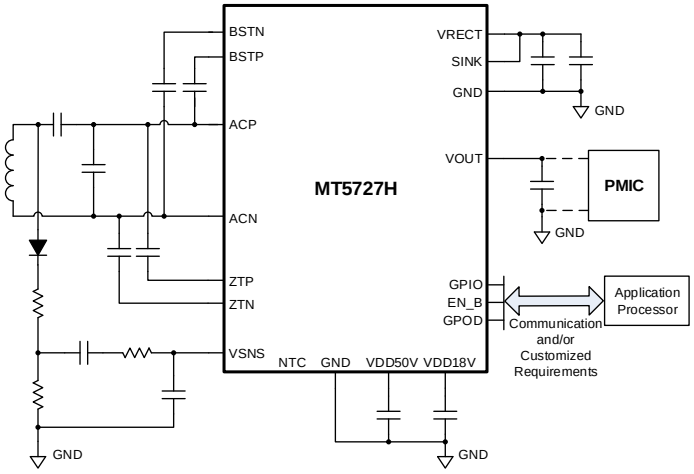

Figure 1 Typical Application Circuit

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5. PIN CONFIGURATIONS AND FUNCTIONS

5.1. Pin Configurations

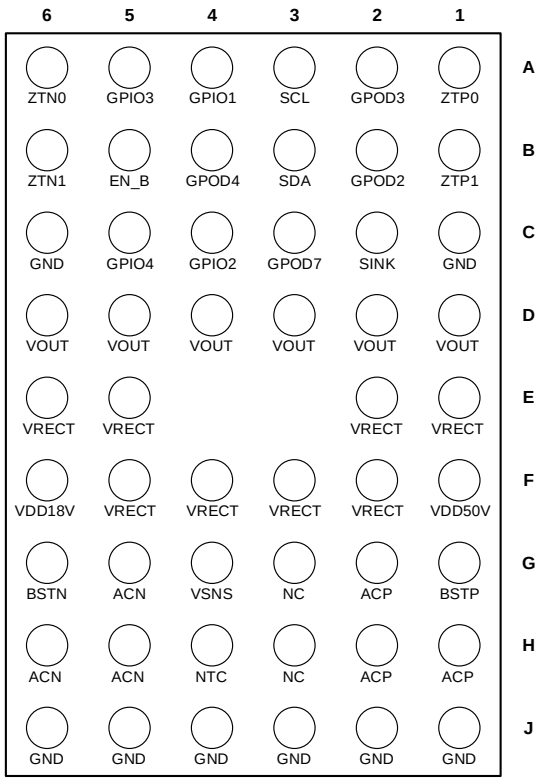


Figure 2 Bottom View (pin/ball side)

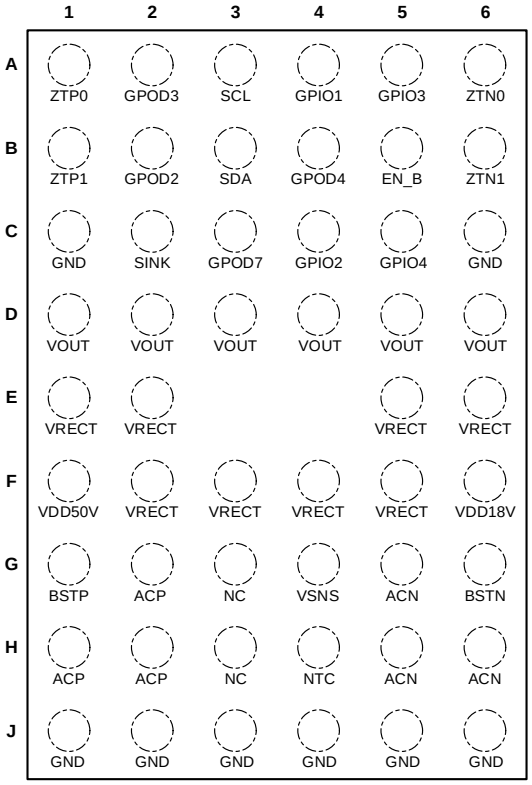


Figure 3 Top View (marking side)

5.2. Pin Functions

Table 1 Pin Functions

Pin Name	Pin No.	Description
ACN	G5,H5,H6	AC negative input.
ACP	G2,H1,H2	AC positive input.
GND	J1,J2,J3,J4,J5,J6, C1,C6	Power Ground.
VRECT	F2,F3,F4,F5, E1,E2,E5,E6	Output of Synchronous Rectifier. Recommend to connect three parallel 10μF capacitors between this pin and GND.
VOUT	D1,D2,D3,D4,D5, D6	Output of LDO. Connect a 10μF capacitor between this pin and GND.
SINK	C2	Providing sinking current. Recommend to connect a 50Ω resistor between this pin and VRECT.
BSTP	G1	Boost Capacitor for internal driver for synchronous bridge rectifier at ACP. Recommend to connect a 22nF capacitor between this pin and ACP.
BSTN	G6	Boost Capacitor for internal driver for synchronous bridge rectifier at ACN. Recommend to connect a 22nF capacitor between this pin and ACN.
ZTP0	A1	ASK Modulation FET at ACP. Recommend to connect a 22nF capacitor between this pin and ACP.
ZTN0	A6	ASK Modulation FET at ACN. Recommend to connect a 22nF capacitor between this pin and ACN.
ZTP1	B1	ASK Modulation FET at ACP. Recommend to connect a 22nF capacitor between this pin and ACP.
ZTN1	B6	ASK Modulation FET at ACN. Recommend to connect a 22nF capacitor between this pin and ACN.
NTC	H4	Input of ADC, users can connect external thermistor as temperature sensor.
EN_B	B5	Disable Pin. Connect this pin to logic HIGH can disable whole chip, while to logic LOW or floating can enable the chip.
VSNS	G4	Coil's voltage sense for Tx demodulation.
VDD50V	F1	Internal 5V power supply for internal analog circuit. Recommend to connect a 10μF capacitor between this pin and GND.
VDD18V	F6	Internal 1.8V power supply for internal digital circuit. Recommend to connect a 4.7μF capacitor between this pin and GND.
SCL	A3	I^2C slave SCL.
SDA	B3	I^2C slave SDA.
GPOD2~4,7	B2,A2, B4,C3	General Purpose I/O. Type: Open Drain. For more details, see Section 5.3.
GPIO1~4	A4,C4, A5,C5	General Purpose I/O. Type: Push/Pull. For more details, see Section 5.3.

5.3. I/O Pin Default Configurations

Table 2 GPOD Default Configurations

GPOD2~4, 7	
GPOD2	General GPIO, ADC.
GPOD3	General GPIO, ADC.
GPOD4	General GPIO, ADC.
GPOD7	General GPIO, ADC.
Note: GPOD2~4, 7 can be reconfigured upon customers' request.	

Table 3 GPIO Default Configurations

GPIO1~4	
GPIO1	General GPIO, ADC.
GPIO2	General GPIO, ADC.
GPIO3	General GPIO, ADC.
GPIO4	General GPIO, ADC.
Note: GPIO1~4 can be reconfigured upon customers' request.	

6. SPECIFICATIONS

6.1. Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

Pin Name	Absolute Maximum Ratings
ACN, ACP, ZTP0, ZTN0, ZTP1, ZTN1	-0.3V to 30V
BSTP with respect to ACP	-0.3V to 6V
BSTN with respect to ACN	-0.3V to 6V
VRECT, SINK	-0.3V to 30V
VOUT	-0.3V to 22V
VDD50V	-0.3V to 6V
GPOD2~4,7, GPIO1~4	-0.3V to 6V
EN_B, VSNS, NTC	-0.3V to 6V
SCL, SDA	-0.3V to 6V
VDD18V	-0.3V to 2V
Storage Temperature (T_{STG})	-55°C to 150°C
Maximum Soldering Temperature (Reflow, Pb-Free)	260°C

Note:

- *Stresses greater than those listed as Absolute Maximum Ratings could cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods might affect reliability.*
- *All voltages are referred to ground unless otherwise stated.*

6.2. ESD Ratings

Table 5 ESD Ratings

Test Model	Pins	Ratings
HBM	All pins	2000V
CDM	All pins	1000V
LU	All pins	250mA

Note:

Design target for now.

6.3. Recommended Operating Conditions

Table 6 Recommended Operating Conditions

Operating Temperature (Environment)	-40°C ~ 85°C
Operating Current (I_{OUT})	0A ~ 1.25A
Operating Voltage (V_{OUT})	3V ~ 16V

6.4. Package Thermal Information

Table 7 Package Thermal Information

Junction to Ambient ($R_{\theta JA}$)	50°C/W

6.5. Electrical Characteristics

Test conditions: V_{RECT}=12V, T_A=25°C, unless otherwise stated.

Table 8 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Startup (VDD pin)						
V_{UVLO}	Under voltage lockout	V_{RECT} rising from 0V		2.95		V
V_{UVLO_HYS}	Under voltage lockout hysteresis	V_{RECT} falling		200		mV
Supply Current						
I_Q	Quiescent Current in normal operation mode			6		mA
ENB Pin						
V_{IH}②	Input threshold for logic HIGH		1.4			V
V_{IL}②	Input threshold for logic LOW				0.4	V
I_{ENB}	Quiescent current when ENB is logic HIGH				200	μA
Bridge Rectifier						
R_{DSON}	R_{DSON} of power MOSFETs			40		mΩ
Over-Voltage Protection						
V_{OVP-DC}	DC over-voltage protection (programmable)	Rising voltage			20	V
V_{LSB_OVP}②	Least significant Bit at OVP			550		mV
LDO						
V_{OUT}	Output voltage regulation	V_{RECT} = 8V I_{OUT} = 0A		5		V
V_{LSB_VOUT}②	Least Significant Bit when programming output voltage			25		mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PRO}②	Output programmable voltage			3~16		V
I_{LIMIT_MAX}	Output current limit				1.3	A
I_{LSB_ILIMIT}②	Least Significant Bit when programming output current limit			25		mA
ADC						
N	Resolution			12		Bit
f_{SAMPLE}②	Sampling rate			100		kS/s
Channel	Number of channels			8		
Miscellaneous						
VDD50V	VDD50V output voltage			5		V
VDD18V	VDD18V output voltage			1.8		V
Digital I/O Pins						
GPOD2~4, 7 SCL, SDA	high level input voltage V_{IH}②		1.26			V
	low level input voltage V_{IL}②				0.54	V
	Low level output voltage V_{OL}	I_{SOURCE}=4mA		0		V
	Low level output current I_{OL}②		2/8①			mA
	Analog input range②			0~5		V
GPIO2~4	High level input voltage V_{IH}②		1.26			V
	Low level input voltage V_{IL}②				0.54	V
	High level output voltage V_{OH}	I_{SINK}=0.5mA		1.8		V
	Low level output voltage V_{OL}	I_{SOURCE}=4mA		0		V
	High level output current I_{OH}②		2/8①			mA
	Low level output current I_{OL}②		2/8①			mA
	Analog input range②			0~5		V
GPIO1	High level input voltage V_{IH}②		1.26			V
	Low level input voltage V_{IL}②				0.54	V
	High level output voltage V_{OH}	I_{SINK}=0.5mA		5		V
	Low level output voltage V_{OL}	I_{SOURCE}=4mA		0		V
	High level output current I_{OH}②		2/8①			mA
	Low level output current I_{OL}②		2/8①			mA
	Analog input range②			0~5		V

Note

① *: Digital I/O pin output current can be programmed.*

② *Guaranteed by design.*

6.6. Typical Operating Characteristics

The following performance characteristics were taken using MT5815 wireless power transmitter at T_A=25°C, unless otherwise noted.

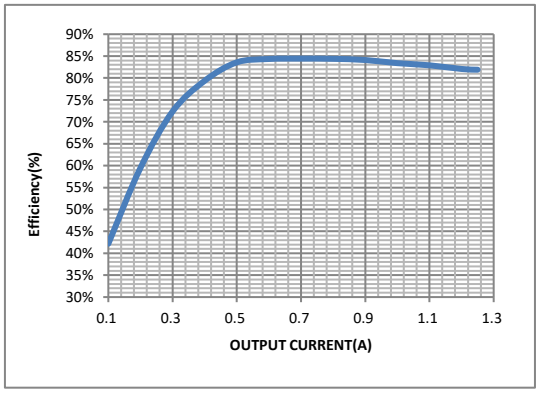


Figure 4 Efficiency vs. Output Load: V_{OUT}=5V

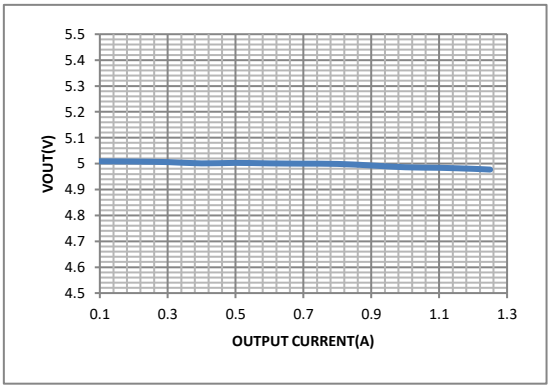


Figure 5 Load Reg. vs. Output Load: V_{OUT}=5V

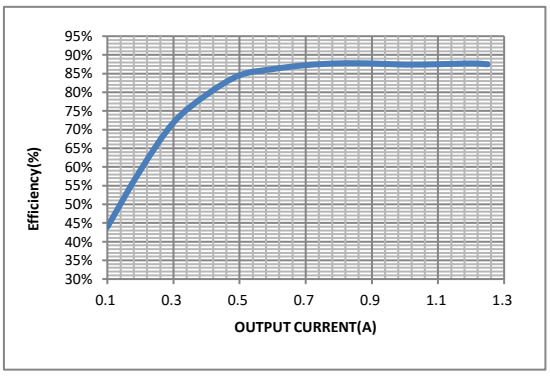


Figure 6 Efficiency vs. Output Load: V_{OUT}=9V

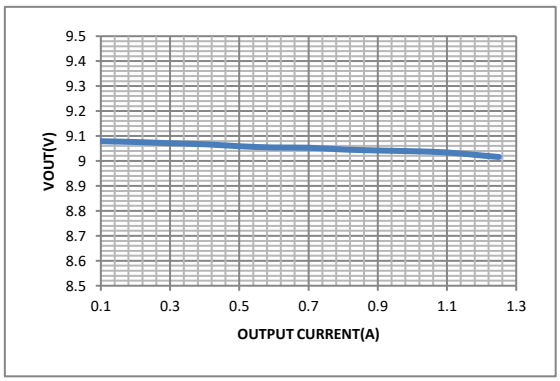


Figure 7 Load Reg. vs. Output Load: V_{OUT}=9V

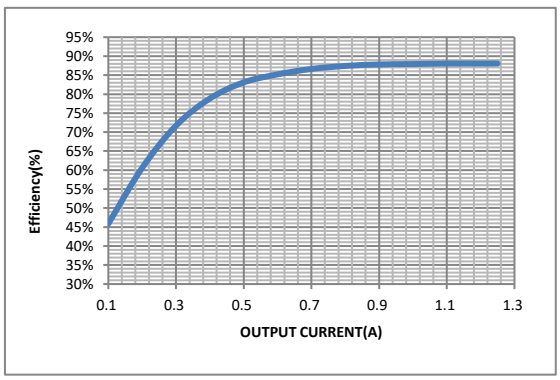


Figure 8 Efficiency vs. Output Load: V_{OUT}=12V

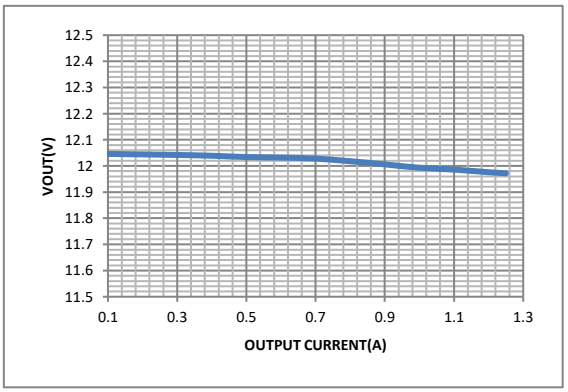


Figure 9 Load Reg. vs. Output Load: V_{OUT}=12V

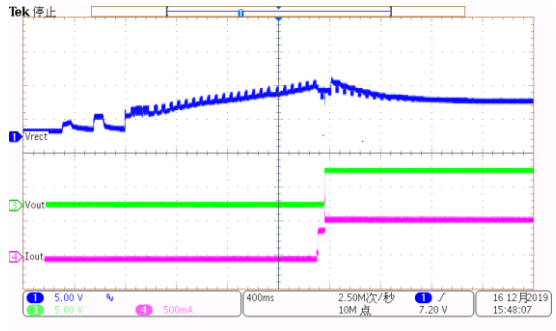


Figure 10 Enable Startup: V_{OUT}=5V; I_{OUT}=0.6A

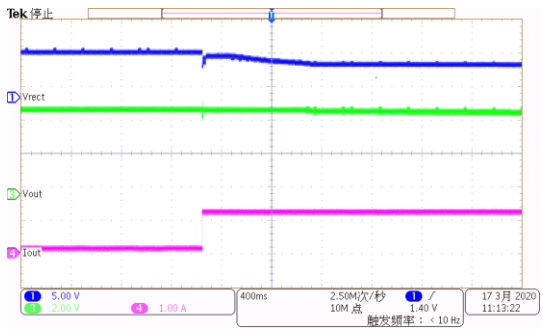


Figure 11 Transient Resp: V_{OUT}=5V; I_{OUT}=0 to 1.25A

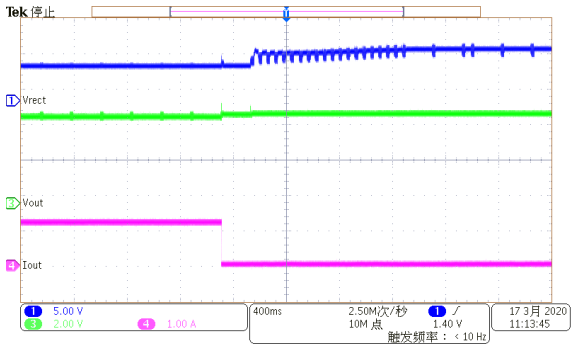


Figure 12 Transient Resp: V_{OUT}=5V; I_{OUT}=1.25 to 0A

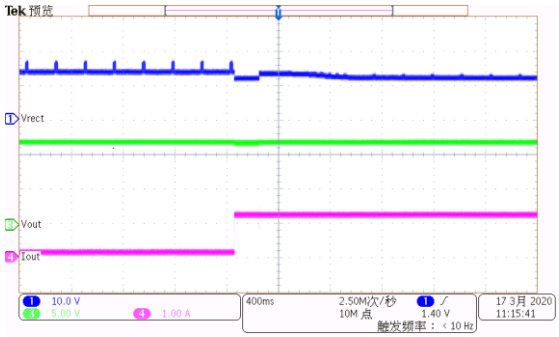


Figure 13 Transient Resp: V_{OUT}=12V; I_{OUT}=0 to 1.25A

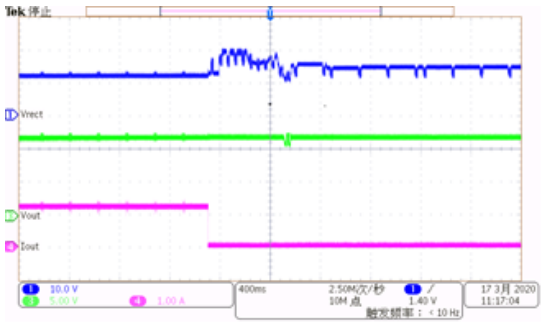


Figure 14 Transient Resp: V_{OUT}=12V; I_{OUT}=1.25 to 0A

7. DETAILED DESCRIPTIONS

7.1. Functional Block Diagram

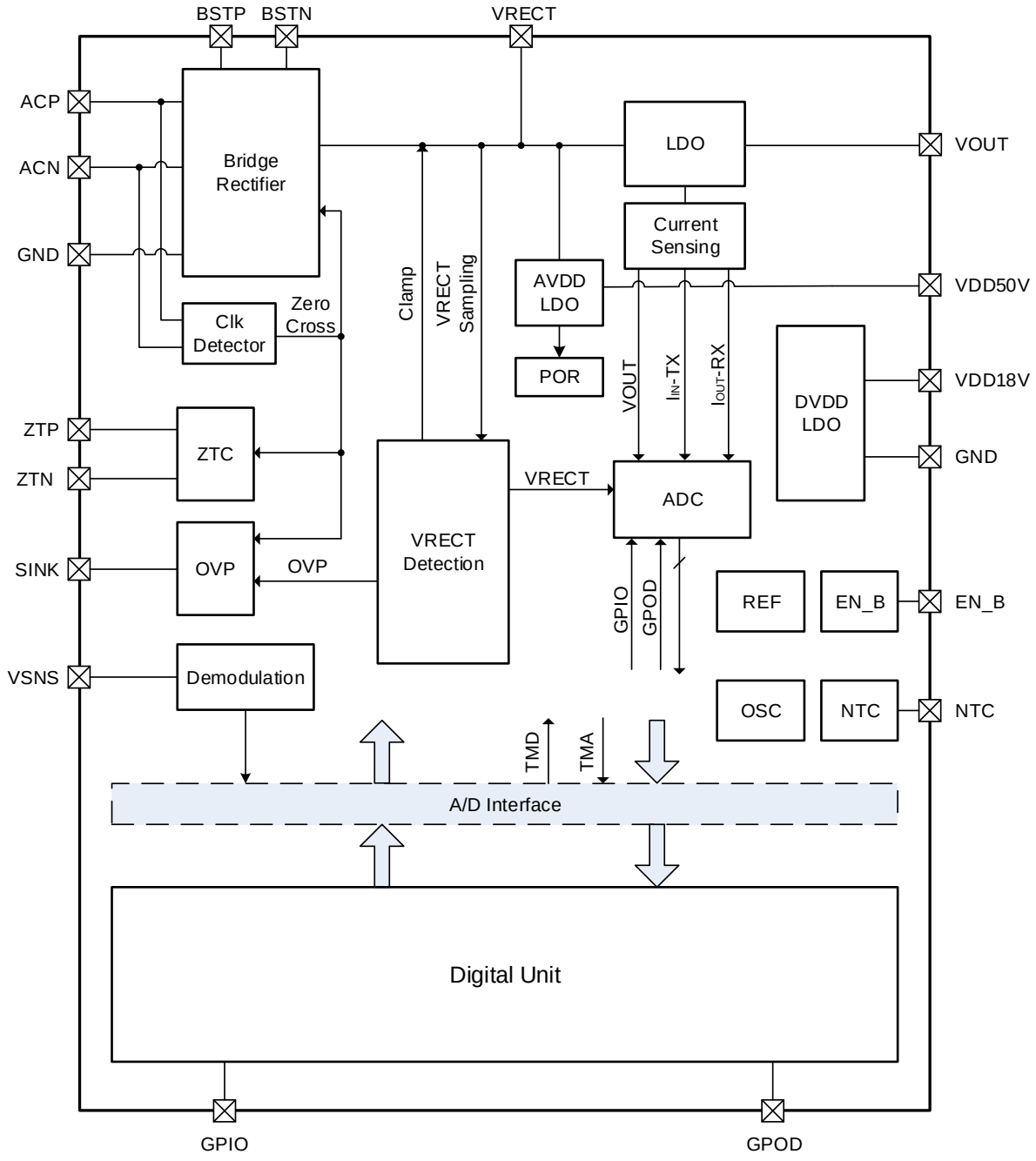


Figure 15 Functional Block Diagram

7.2. Theory of Operation

MT5727H is a SoC based wireless power receiver which is designed for application with up to 20W power delivery. It only requires several passive components like power receiving coils, resonant tank capacitors, decoupling capacitors and pull-up/down resistors to build a complete wireless power receiver system. When coupled with a wireless power transmitter, this system can provide all the functions for wireless power transfer, including power receiving and rectification, output regulation, communication for power control and data exchange, and protections from abnormal conditions (FOD, over-voltage over-current, over-temperature, etc.).

MT5727H is by default programmed to be fully compliant with WPC Qi Specification (Version 1.2.4) with support of both BPP and EPP. It can also be programmed to be compliant with major smartphone vendors' proprietary fast wireless charging protocols.

7.2.1. Bridge Rectifier

MT5727H integrates a high-efficiency full-wave synchronous bridge rectifier to convert AC signal from the resonant tank to DC signal on the VRECT pin. VRECT Detection block is used to monitor the VRECT pin voltage. During startup, the bridge rectifier operates as a passive diode bridge, and it goes into bridge rectifier mode as VRECT pin voltage, detected by VRECT Detection block, exceeds V_{UVLO}. If VRECT pin voltage is too high, over-voltage protection is triggered.

7.2.2. LDO Regulator

MT5727H integrates three LDO regulators,

- The main regulator function as a load switch (connecting and disconnecting the external load), output voltage and current regulation and output clamping when fast load/line transient happens.
- VDD50V LDO and VDD18V LDO, provide necessary regulated power supplies from rectifier output for the operation of the chip.

7.2.3. ADC Converter

ADC Converter is one of the key blocks converts various measured analog variables (voltages, currents, temperature, external analog inputs, etc.) to digital domain such that the embedded microcontroller can use the information for follow-up actions.

7.2.4. Digital Unit

This block contains all the digital circuits, which include embedded microcontroller, volatile and non-volatile memories, I^2C interface, peripherals, Direct Memory Access (DMA), internal buses, and other digital functional blocks. This block is the brain of whole chip which dynamically configures chip for different functions in different state, communicate with the outside world (power transmitter and receiver side external host), and perform necessary data processing for proper operation (like FOD calculation, target VRECT and VOUT calculation, etc.).

7.2.5. Others

- ZTC and CLK Detector. These blocks are for the bi-directional communication for power control and data exchange.
- OSC and REF. These blocks provide the timing reference and voltage reference for the whole chip.

7.2.6. Foreign Object Detection

In the selection phase (Qi V1.2.4), MT5727H tries to figure out the load property, which can be achieved by measuring the damping voltage of coil. If there is foreign object on the surface of the Tx coil, eddy currents generated, causing significant unexplained power dissipation, then the damping voltage drops dramatically. Under this condition, the transmitter stops power delivery because a foreign object may exist. With Pre-FOD circuit, MT5727H can identify whether foreign object (FO) exists.

During power transfer phase, the receiver periodically communicates with the transmitter for the amount of power received, the transmitter compares this power with the power transmitted at the same time. By comparing the power difference, the chip can confirm whether foreign object exists.

8. APPLICATIONS AND IMPLEMENTATIONS

8.1. Reference Schematic

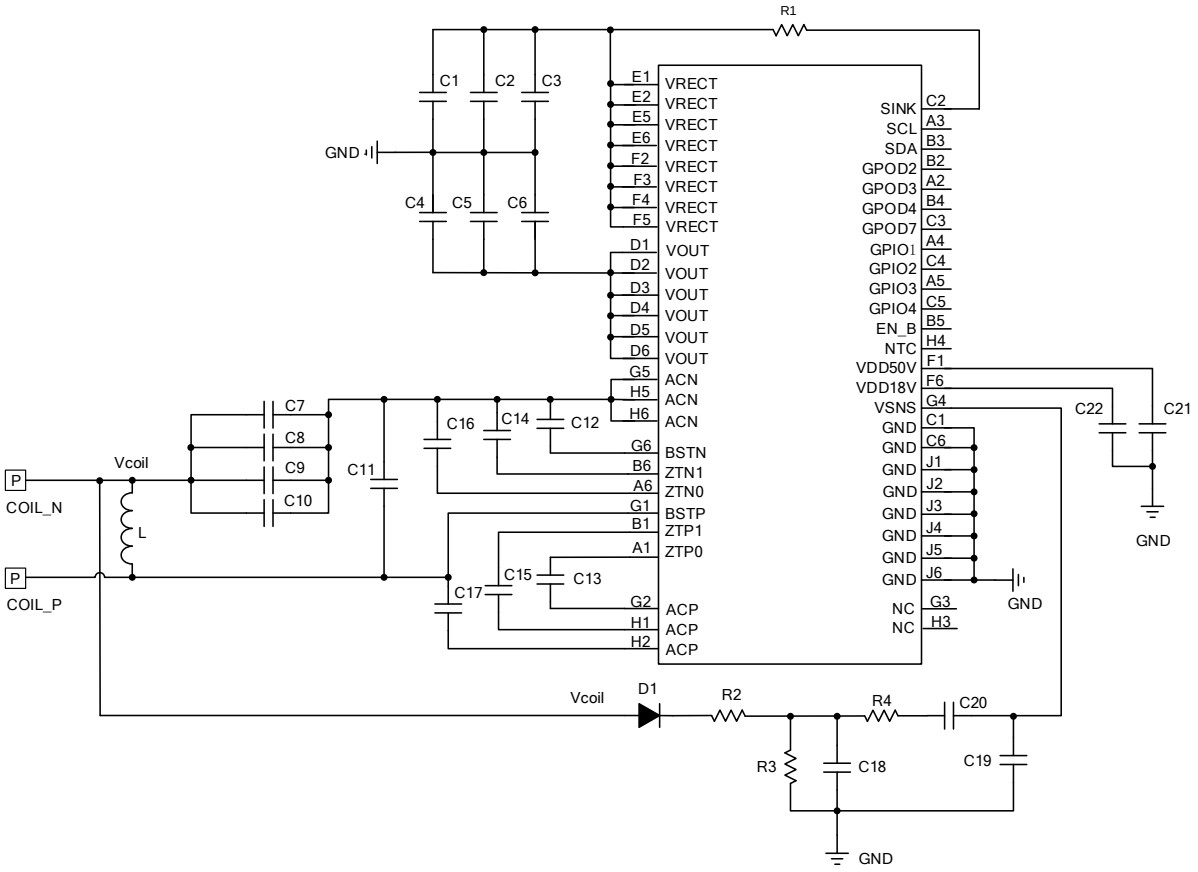


Figure 16 Reference Schematic

8.2. BILL OF MATERIAL (BOM)

Table 9 Bill of Material

#	Reference	Value	Description	Footprint	Quantity
1	R1	50R	RES SMD 50R 5% 1/8W	0805	1
2	R2	5.1K	RES SMD 5.1K 5% 1/20W	0201	1
3	R3	220K	RES SMD 220K 5% 1/20W	0201	1
4	R4	10K	RES SMD 10K 5% 1/20W	0201	1
5	C2,C3, C4,C6	10μF	CAP CER 10μF 25V X7R	0603	4
6	C1,C5,	100nF	CAP CER 100nF 25V X7R	0603	2
7	C7,C8,C9,C10	100nF	CAP CER 0.1μF 50V X7R	0603	4
8	C11	3.3nF	CAP CER 3.3nF 50V X7R	0402	1
9	C12,C13,C14, C15,C16,C17	22nF	CAP CER 22nF 50V X7R	0402	6
10	C18	5nF	CAP CER 5nF 50V X7R	0201	1
11	C19	680pF	CAP CER 680pF 50V X7R	0201	1
12	C20	22nF	CAP CER 22nF 6.3V X7R	0201	1
13	C21	10μF	CAP CER 10μF 6.3V X7R	0201	1
14	C22	4.7μF	CAP CER 4.7μF 6.3V X7R	0201	1
15	D1	MBR0540	Diode	SOD-323	1
16	U1	MT5727H	Wireless power receiver IC	CSP52	1
			Notes		27

8.3. PCB Layout Guidelines

- The heat management of the MT5727H design is critical to performance, and from the thermal perspective. The copper shape with more than 10 thermal vias is an important connection and layout improvement because it assists with current conduction and dramatically improves the MT5727H thermal performance.
- ACN, ACP, GND, VRECT, Crect and Cs must form a minimum AC current loop as shown in the figure below

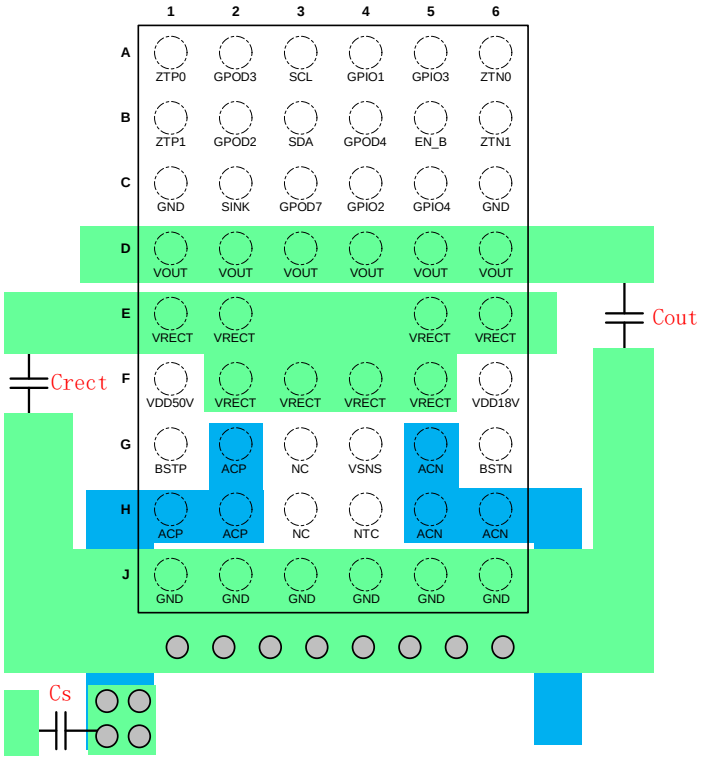


Figure 17 PCB Layout Guidelines

The VRECT capacitors and OUT bypass capacitors should be placed as close as possible to associated pins. It is important to keep the area of the current loop that conducts the AC current from the synchronous bridge rectifier to the VRECT capacitors and GND to minimum to avoid noise. The copper planes should be as wide as possible for the connections for VRECT from MT5727H to the capacitors and back to GND.

- The VDD50V and VDD18V pin capacitors are used to stabilize the internal linear regulators. The capacitors must be close to MT5727H.
- ZTP and ZTN capacitors should be placed as close as possible to MT5727H.
- C1 and C6 are connected to analog ground, which should be connected to the power ground with symmetric traces on the PCB.
- J1, J2, J3, J4, J5 and J6 are connected to power ground. More via holes are needed around these pins. Ground should be completely laid on at least one floor, it's better to have no other traces.

9. REGISTER MAP

The default I²C slave address is 0101011X, where the X indicates read and write privileges, can be configured as:

- 0: read, equals to 0x56 in HEX.
- 1: write, equals to 0x57 in HEX.

Unless otherwise stated, the parameter values are got under the condition of:

- base address: 0x0000
- byte order: little endian

9.1. System Control

Table 10 System Control

Name	R/W	Offset	Bit Field		
Chip ID	RO	0x0000	**Bit**	**Label**	**Description**
			15:0	ID	Chip ID Register
Cust Code	RO	0x0002	**Bit**	**Label**	**Description**
			7:0	Code	Customer code
SYSMODE	RO	0x0005	**Bit**	**Label**	**Description**
			3	ACMISSING	Whether the system can detect missing AC signal. ● 0: Yes ● 1: No
			2	TX	MT572x work in transmitter mode
			0	RX	MT572x work in receiver mode
CMD	RW	0x0006	**Bit**	**Label**	**Description**
			10	VOUT_CHANGE	VOUT change cmd
			9	OCP_CHANGE	OCP change cmd
			8	OVP_CHANGE	OVP change cmd
			7	FAST_CHARGE	Fast charge cmd
			5	CLEAR_INT	Clear the interrupt flag bits
			0	SEND_PPP	Send Proprietary Packet cmd
INTEN	RW	0x0010	Bit	**Label**	**Description**
			15	INT POWER ON	Rx power on interrupt enable
			11	INT FSK SUCCESS	When the FSK is successfully received, this bit will be set up
			10	INT FSK TIMEOUT	After sending a private ASK message, this bit will be set up after a period of time when no FSK is received.
			7	INT LDO OFF	LDO off interrupt enable.

Name	R/W	Offset	Bit Field		
			6	INT LDO_ON	LDO on interrupt enable.
			4	INT FSK RECV	Any FSK message from the transmitter that is successfully received and is not 0x1E 0xFF data, will set up this bit.
			3	INT RX READY	Receiver ready interrupt enable.
			1	INT OVP FLAG	OVP interrupt enable.
			0	INT OCP FLAG	OCP interrupt enable.
INTFLAG	RO	0x0014	**Bit**	**Label**	**Description**
			15	INT POWER ON	Rx power on interrupt flag
			11	INT FSK SUCCESS	When the FSK is successfully received, this bit will be set up
			10	INT FSK TIMEOUT	After sending a private ASK message, this bit will be set up after a period of time when no FSK is received.
			7	INT LDO OFF	LDO off interrupt flag
			6	INT LDO_ON	LDO on interrupt flag
			4	INT FSK RECV	Any FSK message from the transmitter that is successfully received and is not 0x1E 0xFF data, will set up this bit.
			3	INT RX READY	Receiver ready interrupt flag
			1	INT OVP FLAG	OVP interrupt flag
			0	INT OCP FLAG	OCP interrupt flag
INTCLR	RW	0x0018	**Bit**	**Label**	**Description**
			15	INT POWER ON	Clear Rx power on interrupt flag
			11	INT FSK SUCCESS	Clear INT FSK SUCCESS interrupt flag
			10	INT FSK TIMEOUT	Clear INT FSK TIMEOUT interrupt flag
			7	INT LDO OFF	Clear LDO off interrupt flag
			6	INT LDO_ON	Clear LDO on interrupt flag
			4	INT FSK RECV	Clear INT FSK RECV interrupt flag
			3	INT RX READY	Clear Receiver ready interrupt flag
			1	INT OVP FLAG	Clear OVP interrupt flag
			0	INT OCP FLAG	Clear OCP interrupt flag

9.2. System Setting

Table 11 System Setting

Name	R/W	Offset	Bit Field		
Frequency	RO	0x0020	**Bit**	**Label**	**Description**
			15:0	KHz	Operating Frequency
Fping	RO	0x0022	**Bit**	**Label**	**Description**
			15:0	KHz	Ping Frequency
Prx	RO	0x0024	**Bit**	**Label**	**Description**
			15:0	value	RPP values in the WPC protocol
Vdiff	RO	0x0026	**Bit**	**Label**	**Description**
			15:0	mV	Threshold for fast-charge
IOUT	RO	0x0028	**Bit**	**Label**	**Description**
			15:0	mA	LDO output current
VOUT	RO	0x002a	**Bit**	**Label**	**Description**
			15:0	mV	LDO Output voltage
VRECT	RO	0x002c	**Bit**	**Label**	**Description**
			15:0	mV	Rectifier output voltage
VOUTSET	RW	0x002e	**Bit**	**Label**	**Description**
			15:0	mV	LDO output voltage
VRECTADJ	RW	0x0030	**Bit**	**Label**	**Description**
			15:0	mV	VRECT adjust
VFC	RW	0x0032	**Bit**	**Label**	**Description**
			15:0	mV	fast charge voltage
ILIM	RW	0x0034	**Bit**	**Label**	**Description**
			15:0	mA	I_{OUT} limit
Vlim	RW	0x0036	**Bit**	**Label**	**Description**
			15:0	mV	VRECT limit
PLDO	RW	0x0038	**Bit**	**Label**	**Description**
			15:0	mW	LDO power protection threshold
REC_Hysteresis	RW	0x003a	**Bit**	**Label**	**Description**
			15:0	mA	Hysteresis for switching bridge rectifier mode
REC_Ihalf	RW	0x003c	**Bit**	**Label**	**Description**
			15:0	mA	Threshold for switching bridge between diode mode and half mode
REC_Ifull	RW	0x003e	**Bit**	**Label**	**Description**
			15:0	mA	Threshold for switching bridge between diode mode and half mode
VrectX1			**Bit**	**Label**	**Description**

Name	R/W	Offset	Bit Field		
	RW	0x0040	15:0	value	Target VRECT curve parameter
VrectX2	RW	0x0042	Bit	Label	Description
			15:0	value	Target VRECT curve parameter
VrectY1	RW	0x0044	Bit	Label	Description
			15:0	value	Target VRECT curve parameter
VrectY2	RW	0x0046	Bit	Label	Description
			15:0	value	Target VRECT curve parameter
Manufacturer Code	RW	0x0048	Bit	Label	Description
			15:0	value	Manufacturer Code
RECMode	RO	0x0071	Bit	Label	Description
			7:0	value	Bridge Rectifier mode 0xF0: diode mode 0x50: half-bridge mode 0x00: full-bridge mode
SS	RO	0x0070	Bit	Label	Description
			7:0	value	Signal Strength value
CEPCNT	RW	0x00C0	Bit	Label	Description
			31:0	value	CEP counter

9.3. ASK

Table 12 ASK

Name	R/W	Offset	Bit Field		
ASKHEADER	RW	0x0050	Bit	Label	Description
			7:0	value	Proprietary packet header
ASKMSG0	RW	0x0051	Bit	Label	Description
			7:0	value	Proprietary packet msg[0]
ASKMSG1	RW	0x0052	Bit	Label	Description
			7:0	value	Proprietary packet msg[1]
ASKMSG2	RW	0x0053	Bit	Label	Description
			7:0	value	Proprietary packet msg[2]
ASKMSG3	RW	0x0054	Bit	Label	Description
			7:0	value	Proprietary packet msg[3]
ASKMSG4	RW	0x0055	Bit	Label	Description
			7:0	value	Proprietary packet msg[4]
ASKMSG5	RW	0x0056	Bit	Label	Description
			7:0	value	Proprietary packet msg[5]
ASKMSG6	RW	0x0057	Bit	Label	Description

Name	R/W	Offset	Bit Field		
			7:0	value	Proprietary packet msg[6]
ASKMSG7	RW	0x0058	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[7]
ASKMSG8	RW	0x0059	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[8]
ASKMSG9	RW	0x005A	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[9]
ASKMSG10	RW	0x005B	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[10]
ASKMSG11	RW	0x005C	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[11]
ASKMSG12	RW	0x005D	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[12]
ASKMSG13	RW	0x005E	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[13]
ASKMSG14	RW	0x005F	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[14]
ASKMSG15	RW	0x0060	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[15]
ASKMSG16	RW	0x0061	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[16]
ASKMSG17	RW	0x0062	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[17]
ASKMSG18	RW	0x0063	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[18]
ASKMSG19	RW	0x0064	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[19]
ASKMSG20	RW	0x0065	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[20]
ASKMSG21	RW	0x0066	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[21]
ASKMSG22	RW	0x0067	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[22]
ASKMSG23	RW	0x0068	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[23]
ASKMSG24	RW	0x0069	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[24]
ASKMSG25	RW	0x006A	**Bit**	**Label**	**Description**
			7:0	value	Proprietary packet msg[25]

Name	R/W	Offset	Bit Field		
ASKMSG26	RW	0x006B	Bit	Label	Description
			7:0	value	Proprietary packet msg[26]
ASKMSG27	RW	0x006C	Bit	Label	Description
			7:0	value	Proprietary packet msg[27]
ASKMSG28	RW	0x006D	Bit	Label	Description
			7:0	value	Proprietary packet msg[28]
ASKMSG29	RW	0x006E	Bit	Label	Description
			7:0	value	Proprietary packet msg[29]
ASKMSG30	RW	0x006F	Bit	Label	Description
			7:0	value	Proprietary packet msg[30]
ASKMSG31	RW	0x0070	Bit	Label	Description
			7:0	value	Proprietary packet msg[31]

9.4. FSK

Table 13 FSK

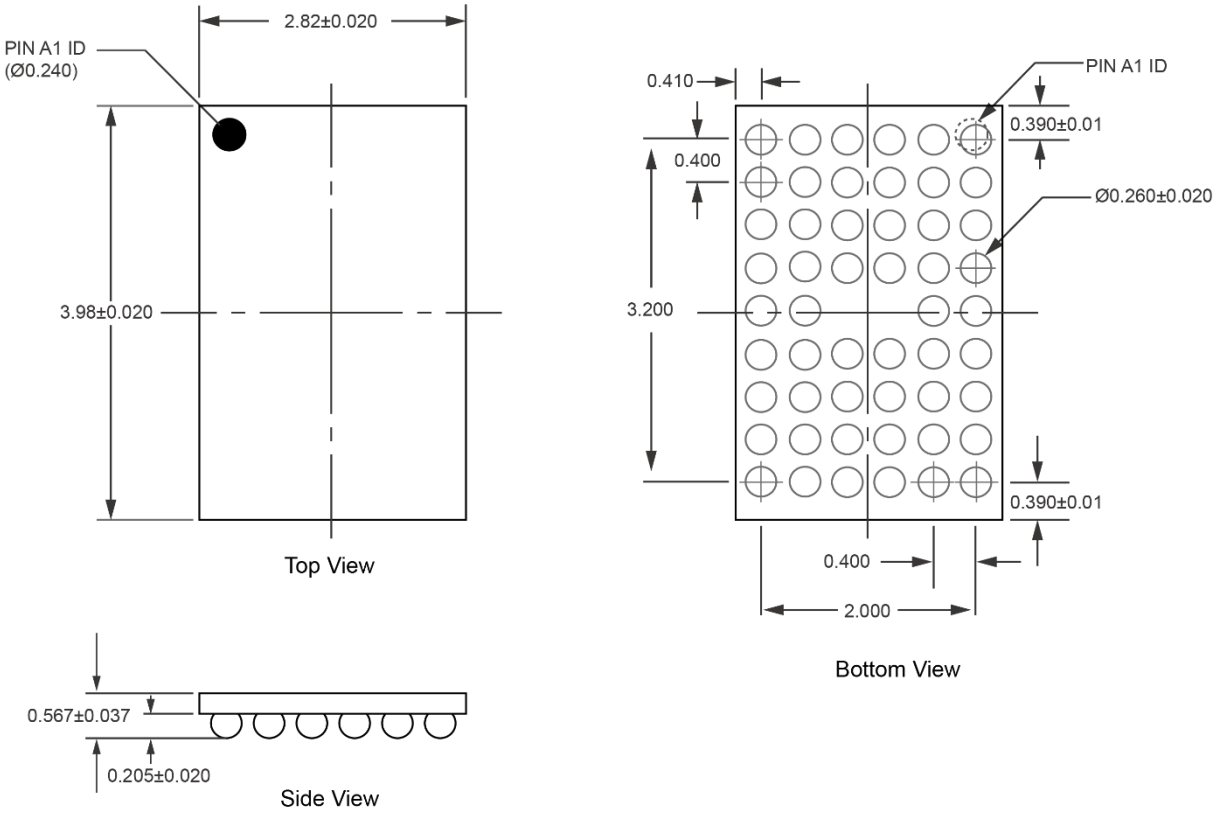
Name	R/W	Offset	Bit Field		
FSK Header	RO	0x0066	Bit	Label	Description
			7:0	value	FSK Proprietary packet header
FSKMSG0	RO	0x0067	Bit	Label	Description
			7:0	value	FSK Proprietary packet msg[0]
FSKMSG1	RO	0x0068	Bit	Label	Description
			7:0	value	FSK Proprietary packet msg[1]
FSKMSG2	RO	0x0069	Bit	Label	Description
			7:0	value	FSK Proprietary packet msg[2]
iFSKMSG3	RO	0x006A	Bit	Label	Description
			7:0	value	FSK Proprietary packet msg[3]
FSKMSG4	RO	0x006B	Bit	Label	Description
			7:0	value	FSK Proprietary packet msg[4]
FSKMSG5	RO	0x006C	Bit	Label	Description
			7:0	value	FSK Proprietary packet msg[5]
FSKMSG6	RO	0x006D	Bit	Label	Description
			7:0	value	FSK Proprietary packet msg[6]
FSKMSG7	RO	0x006E	Bit	Label	Description
			7:0	value	FSK Proprietary packet msg[7]

9.5. FOD

Table 14 FOD

Name	R/W	Offset	Bit Field		
FOD0	RW	0x0078	**Bit**	**Label**	**Description**
			15:8	Offset	FOD section 0 offset
			7:0	Gain	FOD section 0 gain
FOD1	RW	0x007A	**Bit**	**Label**	**Description**
			15:8	Offset	FOD section 1 offset
			7:0	Gain	FOD section 1 gain
FOD2	RW	0x007C	**Bit**	**Label**	**Description**
			15:8	Offset	FOD section 2 offset
			7:0	Gain	FOD section 2 gain
FOD3	RW	0x007E	**Bit**	**Label**	**Description**
			15:8	Offset	FOD section 3 offset
			7:0	Gain	FOD section 3 gain
FOD4	RW	0x0080	**Bit**	**Label**	**Description**
			15:8	Offset	FOD section 4 offset
			7:0	Gain	FOD section 4 gain
FOD5	RW	0x0082	**Bit**	**Label**	**Description**
			15:8	Offset	FOD section 5 offset
			7:0	Gain	FOD section 5 gain
FOD6	RW	0x0084	**Bit**	**Label**	**Description**
			15:8	Offset	FOD section 6 offset
			7:0	Gain	FOD section 6 gain
FOD7	RW	0x0086	**Bit**	**Label**	**Description**
			15:8	Offset	FOD section 7 offset
			7:0	Gain	FOD section 7 gain

10. DETAILED PACKAGING INFORMATION



NOTES:

1. ALL DIMENSIONS AND TOLERANCES ARE PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 18 Detailed Packaging Information

11. ORDERING INFORMATION

Table 15 Ordering information

Part No.	Package Information	Package Quantity	Moisture Sensitivity Level	Chip Mark
MT5727H	2.82mmx 3.98mm 52-WLCSP	3000/Tape & Reel	MSL I	POWER27 ZZZZZ YWWZZ ZZZZ ZZZZ
MT5727H-XXXXXX①	2.82mm x 3.98mm 52-WLCSP	3000/Tape & Reel	MSL I	POWER27② ZZZZZ YWWZZ ZZZZ ZZZZ

12. REVISION HISTORY

Table 16 Revision History

Revision	Date	Description
0.1	2019-12-13	Preliminary version.
0.2	2020-04-14	Add Register Map.
0.3	2020-06-06	Add Halogen and RoHS test results.
0.4	2020-08-17	Update POD diagram.
0.5	2020-09-24	Change the chip mark and POD diagram.
0.6	2021-05-11	Update the chip mark.
1.00	2021-08-06	Update the register map and upgrade the file for formal release.
1.10	2022-04-19	Upgrade the MSL.
1.20	2022-11-30	Update in operating temperature (Environment).