General Description

SIP1221LR1S is a high performance but small footprint ambient light sensor which also called ALS. ALS is used to measure the illuminance of ambient light; the response values will be output via an I2C communication port.

There are two ALS channels and a flicker channel in SIP1221LR1S. Two group of ultra-high sensitivity, low dark current photodiodes which have specific optical filters on them are key elements of ALS, they simulate the human eye response appropriately, and respond to various of light sources accurately. Precise timing control block and independent gain setting for different channels help to measure wide range of illuminance.

SIP1221LR1S has a 512 bytes FIFO in it, which acts as data buffer. SIP1221LR1S also can be used to detect the flicker frequency of light source by the flicker channel.

SIP1221LR1S supports synchronized working mode with SYNC pin externally triggered.

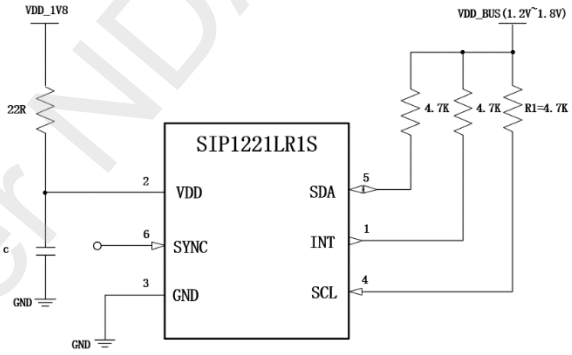
Key Features

- Sensor uses 1.8V power supply, IO voltage is compatible to 1.2V and 1.8V
- ALS:
  - Photopic + wideband two channels design
  - Ultra-high sensitivity, low noise, low dark current
  - Integration time is configurable, gain setting is independently for ALS channels
  - Integration can be synchronized with external signal
- 1MHz I2C communication frequency
- Build-in 512 bytes FIFO, supports light source flicker frequency detection
- Support external SYNC function
- Low power consumption design:
  - IDLE mode
  - Sleep mode
- Operation temperature range: -40℃~85℃
- Moisture Sensitivity Level 3
- 6-pin WB LGA packaging, 2.0mm x 1.0mm x 0.5mm

Application

- Wearable devices display management
- Mobile phone, PAD display management
- Notebook PC, TV display management
- Light source flicker detection

Application Diagram



Content

1 System Description

Device overview

SIP1221LR1S includes three group of PD and three Readout circuits design, support ambient light illuminance measurement and flicker frequency detection. VDD is the supply to sensor die, INT pin is used to output the internal interrupt events, such like data beyond thresholds event, I2C communication port is used for configuration as well as data output, and SYNC can be configured to synchronized with external signal, and trigger the ALS integration.

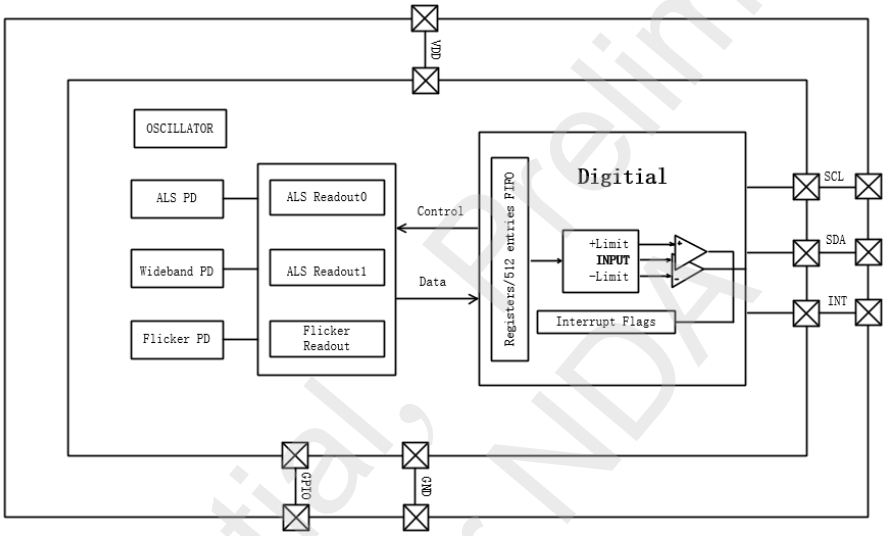


Figure 1-1 Block diagram

Pin configuration and functions

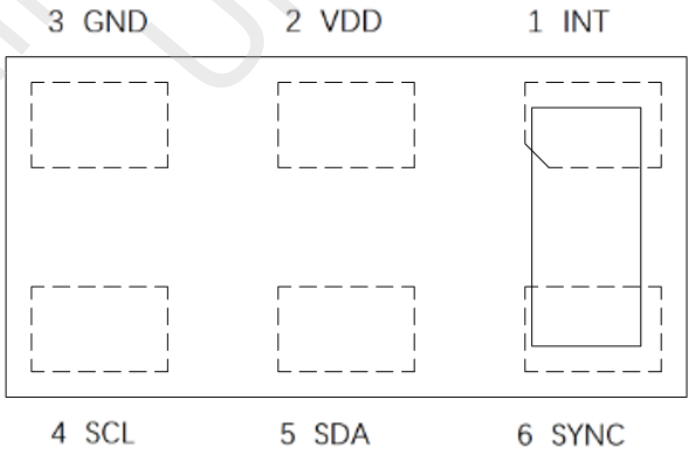


Figure 1-2 Pin configuration (top view)

Table 1-1Pins functions

#	Name	Direction	Type	Comments

1	INT	O	Analog	Interrupt output pin, open drain, default active low
2	VDD	PWR	Supply	1.8V power supply
3	GND	GND	Ground	Ground
4	SCL	I	Digital	I²C serial clock input
5	SDA	I/O	Digital	I²C serial data input/output, open drain.
6	SYNC	I/O	Analog	Connect to external SYNC trigger signal or connect to ground or connect to supply or NC

Typical Application

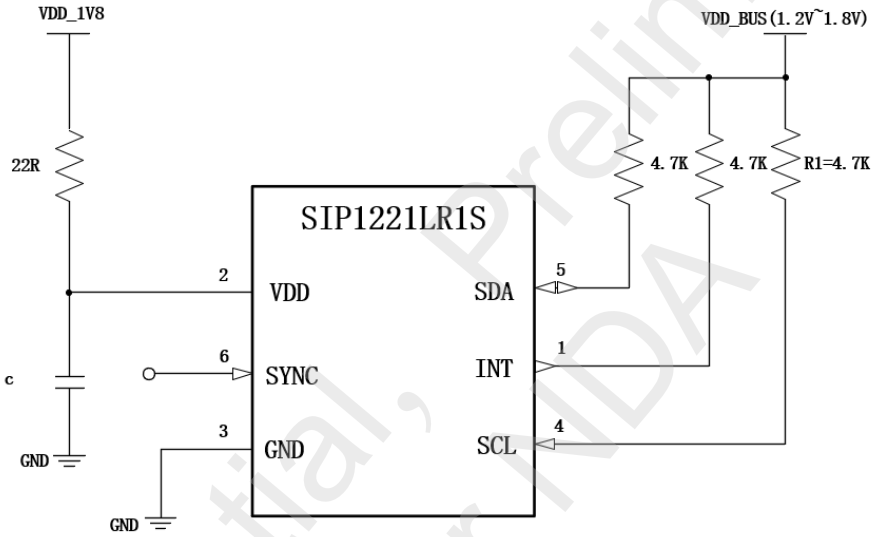


Figure 1-3 SIP1221LR1S application circuits

2 Electrical Characteristics

Absolute Maximum Rating

Table 2-1 Absolute Maximum Rating

Parameters	Symbol	Min.	Typ.	Max.	Units
Supply voltage	VDD	-0.3		1.98	V
Digital Input/Output voltage	SCL, SDA, INT	-0.3		1.98	V
Storage Temperature Range	T_{STG}	-40		85	℃
Moisture Sensitivity Level	MSL		3		
Lead Temperature (Soldering 10 seconds)			260		℃

ESD Rating

Table 2-2 ESD Rating

Stress Test	Value	Units
Human-body mode (HBM), per ESDA/JEDEC JS-001-2017	±2000	V
Charged-device mode (CDM)， per ESDA/JEDEC JS-002-2018	±500	V
Latch-up	±100	mA

Recommended Operating Conditions

Parameters	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage	VDD		1.62	1.8	1.98	V
Operating Ambient Temperature	T_A		-40		85	℃
I2C Com Frequency	f_{I2C}				1M	KHz

Electrical Specifications

Table 2-3 Operating Characteristics with VDD=1.8V, T_A=25℃ (unless otherwise noted)

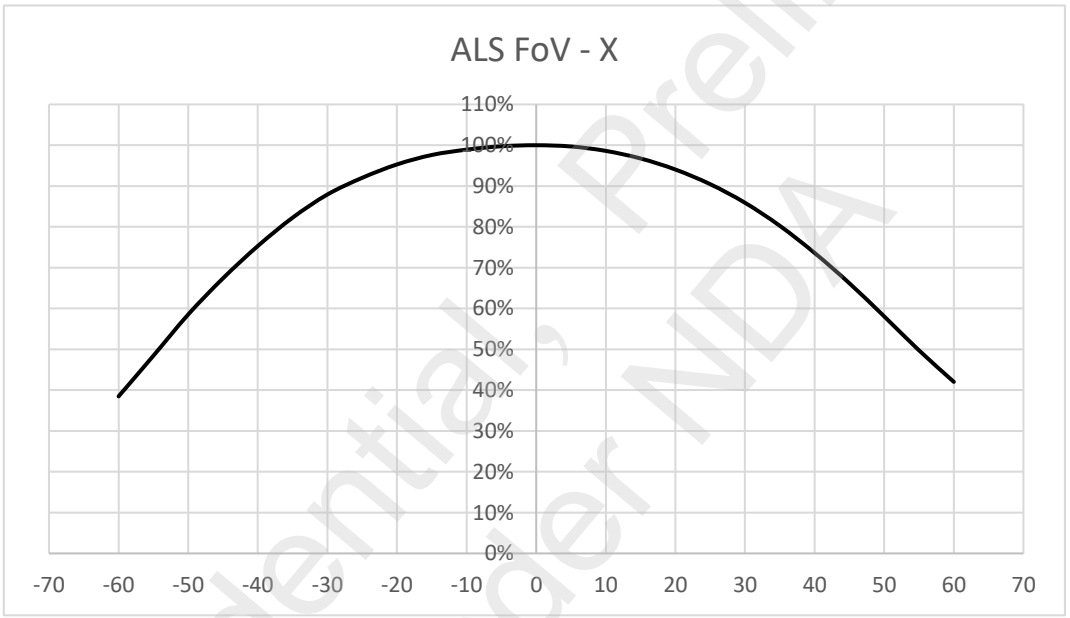
Parameters	Symbol	Condition	Min.	Typ.	Max.	Units
SDA, SCL input high voltage	V_{IH}		0.71			V
SDA, SCL input low voltage	V_{IL}				0.44	V
SDA, INT output low voltage	V_{OL}				0.12	V
Oscillator Frequency	f_{OSC}			8.1		MHz
Supply Current	I_{Sleep}	Sleep		0.75		μA
	I_{Idle}	Idle		41		μA
	I_{ALS}	ALS Active		190		μA
ALS characteristics						
CH0 WB sensitivity			-12%	TBD	+12%	counts
CH1 ALS sensitivity			-12%	TBD	+12%	counts
ALS Integration Time	T_{ALS_inte}		1.358μ		356m	s

ALS Output Full Range					65535	counts
ALS Dark Current	DCR	Max gain, 100ms integration time @dark environment		0	3	
ALS Noise		ALS_GAIN = 512x T_{ALS_inte} = 100ms		0.2		%(σ)

*Note1: T_{ALS_inte} = ALS_INTE_TIME * 1.358μs; time step is 1.358μs

*Note2: $I_{ALS\_LowPower}$: 10ms in active mode, 190ms in sleep mode

Optical Characteristics



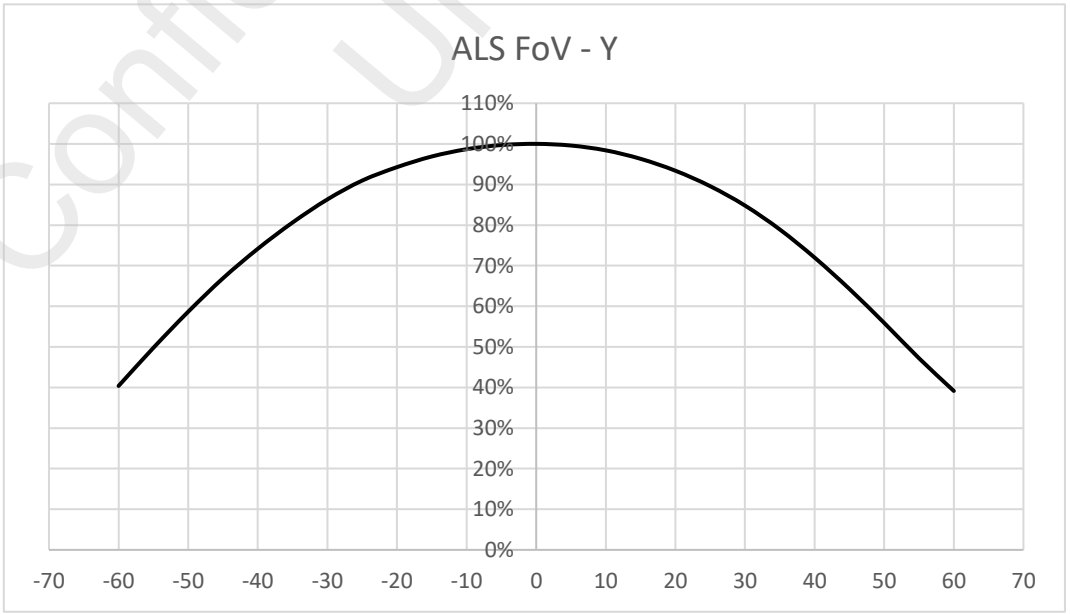


Figure 2-1 SIP1221LR1S ALS Angular Response

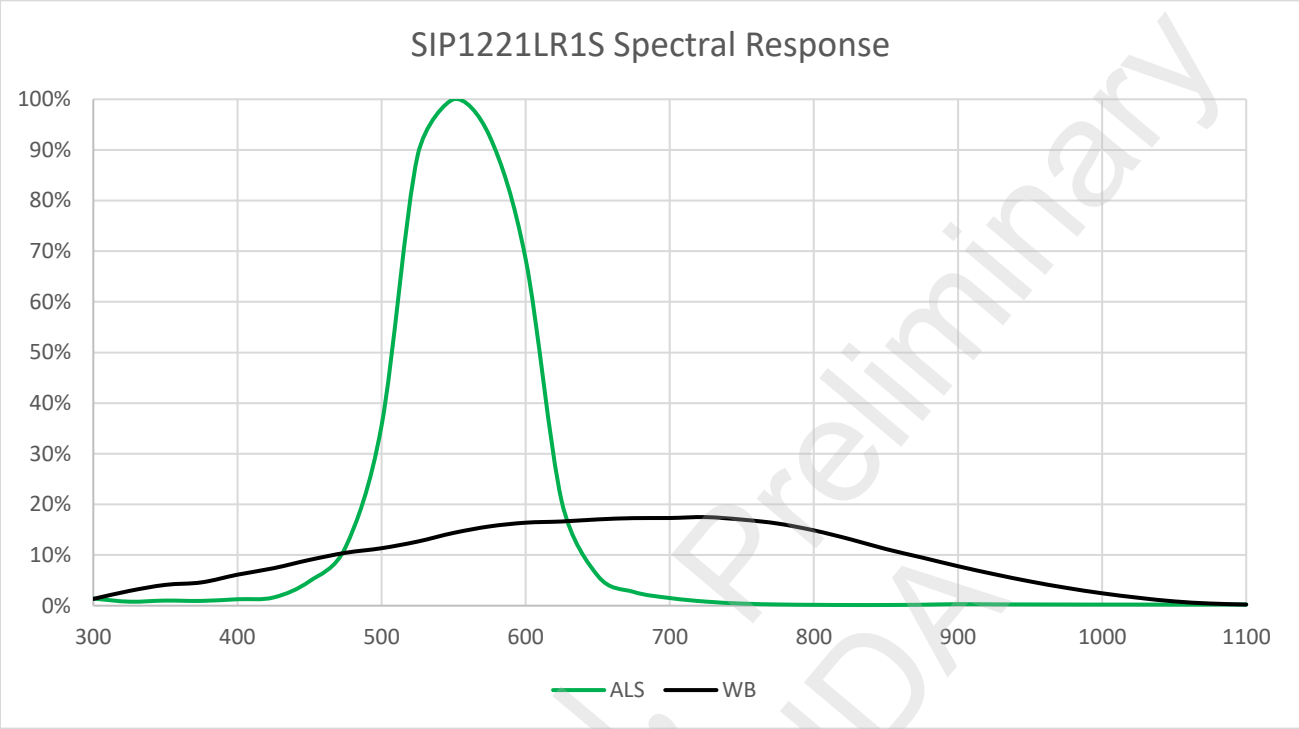


Figure 2-2 SIP1221LR1S Spectral Responsivity

General I²C Operation

The SIP1221LR1S operates as an I²C slave, use 7-bit slave address 0x58.

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The corresponding pins on the SIP1221LR1S for the two signals are SDA and SCL. The bus transfers data serially, one bit at a time. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection. Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Use pull-up resistors between 660 Ω and 4.7 kΩ. Do not allow the SDA and SCL voltages to exceed the device digital interface supply voltage, V_{DD}.

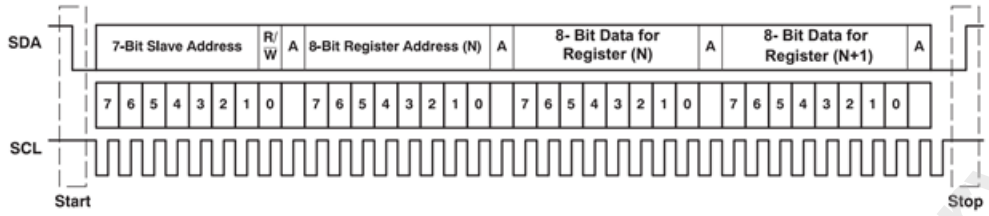


Figure 2-3 Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. Figure 2-3 shows a generic data transfer sequence.

2.1.1 Single-Byte and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the SIP1221LR1S responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges. The SIP1221LR1S supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has taken place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

2.1.2 Single-Byte Write

As shown in Figure 2-4, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the SIP1221LR1S responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the device internal memory address being accessed. After receiving the register byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

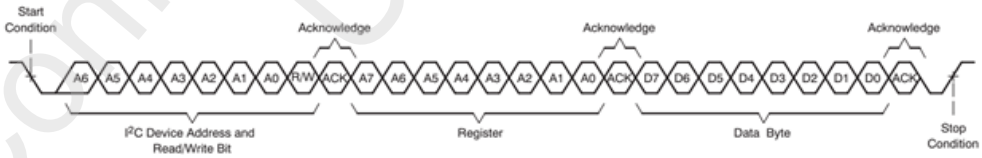


Figure 2-4 Single Byte Write transfer

2.1.3 Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the SIP1221LR1S as shown in Figure 2-5. After receiving each data byte, the device responds with an acknowledge bit.

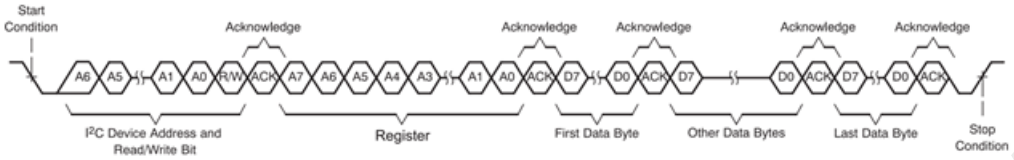


Figure 2-5 Multiple-Byte Write transfer

2.1.4 Single-Byte Read

As shown in Figure 2-6, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0. After receiving the SIP1221LR1S address and the read/write bit, the device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the SIP1221LR1S address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the SIP1221LR1S transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

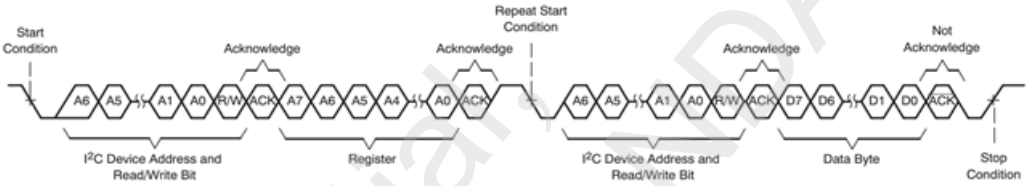


Figure 2-6 Single-Byte Read transfer

2.1.5 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the SIP1221LR1S to the master device as shown in Figure 2-7. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

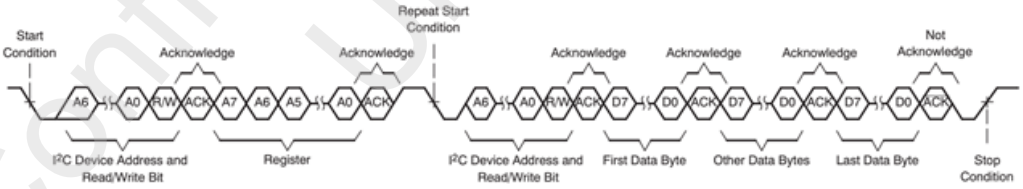


Figure 2-7 Multiple-Byte Read transfer

2.1.6 Timing Chart

Parameters	Symbol	Standard-Mode		Fast-Mode		Fast-Mode Plus		Units
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{scl}	0	100	0	400	0	1000	kHz
Hold time (repeated) START condition. After this	T_s_hd	4.0		0.6		0.26		us

period, the first clock pulse is generated.								
LOW period of the SCL clock	T_low_scl	4.7		1.3		0.5		us
HIGH period of the SCL clock	T_high_scl	4.0		0.6		0.26		us
Setup time for a repeated START condition	T_rep_s_su	4.7		0.6		0.26		us
Data hold time: For I2C bus devices	T_s_hd	0	3.45	0	0.9	0		us
Data set-up time	T_s_su	250		100		50		ns
SDA and SCL Rise Time	Tr_scl		1000	20+0.1x Cb	300		120	ns
SDA and SCL Fall Time	Tf_scl		300	20+0.1x Cb	300	20+0.1 xCb	120	ns
Set-up time for STOP condition	T_t_su	4		0.6		0.26		us
Bus free time between a STOP and START condition	T_t_buf	4.7		1.3		0.5		us
Capacitive load for each bus line	Cb		400		400		550	pF

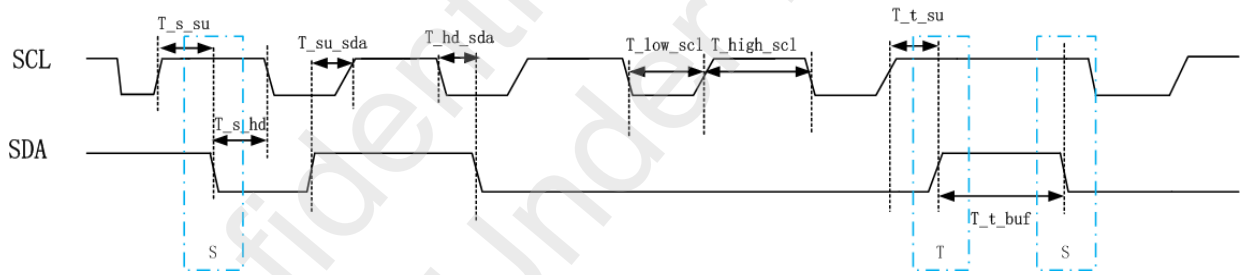


Figure 2-8 Timing diagrams

3 Function Description

ALS Operation

ALS is used to measure the illuminance of light. The response value is directly proportional to ambient light illuminance, ALS integration time (from 1.356μs to 356ms) and ALS gain setting (from 0.25x to 1024x). Once ALS is enabled, two ALS channels are doing accumulation simultaneously and periodically, but can have independent gain setting. Host gets two 16-bit ALS channel data from single integration time, and do calculation to generate illuminance result. The range of ALS channel data depends on the ALS integration time, its maximum output will be the value of ALS_INTE_TIME[17:0] + 1. It's recommended that once ALS integration

time or ALS gain setting is changed, the ALS should be re-enabled to avoid mess data.

SIP1221LR1S supports various of ALS interrupts (status bits in REG 0x81), including

ALS saturation interrupts, ALS_ANA_SAT_INT represents ALS data is saturated corresponding to the integration time which can not reach to full range (65535), and ALS_DIG_SAT_INT represents ALS data is up to 65535.

ALS timing error interrupt indicates that configured ALS period time (REG 0x5B and 0x5C) is shorter than ALS integration time (REG 0x58, 0x59 and 0x5A).

ALS data beyond thresholds interrupt, and a debounce filter designed for ALS data interrupt. If ALS data is greater than high threshold or lower than low threshold consecutively, and reach the number which is configured to the debounce filter (ALS_PERSIST_NUM in REG 0x52), ALS_INT will be asserted. And please note that ALS data equal to high threshold or low threshold won't trigger thresholds interrupt.

All the ALS interrupt status bits can be cleared by reading REG 0x81 if INT_CLR_MODE = 0, or by writing 1 to REG 0x81 if INT_CLR_MODE = 1. Enable the INT pin (REG 0x06) and ALS interrupt switches (0x53), the enabled interrupts will output to INT pin once they are asserted. INT pin polarity can be inverted by setting INT_POLARITY in REG 0x06.

State machine diagram

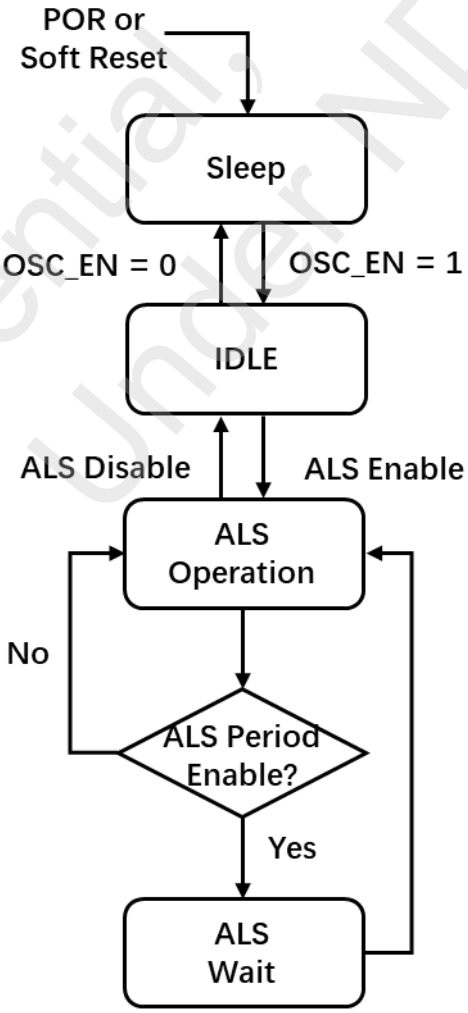


Figure 3-1 SIP1221LR1S operation state diagram

FIFO

SIP1221LR1S has build-in 512 bytes FIFO, it supports high sample rate for ALS measurement (e.g., up to ~7000Hz when ALS_INTE_TIME[17:0] = 99 and ALS_RST_NUM =0 , ~5028Hz when ALS_INTE_TIME[17:0] = 99 and ALS_RST_NUM = 1).

FIFO is enabled to store ALS channel data when FIFO_MODE in REG 0xA3 and 0xA4 is set, data will be put in FIFO in order of ALS CH0 data, ALS CH1 data, ALS CH0 data …, and then will be read bytes by bytes with same order from REG 0x9F. REG 0xA0 & 0xA1 shows the current bytes number of available ALS data in FIFO (the 3 LSB bits are in REG 0xA0 FSTATUS[7:5]), please note that 0xA0 must be read first then 0xA1 to get 10bit width FIFO level data. REG 0xA0 help to get the current status of FIFO, such as FIFO empty, FIFO full, FIFO almost empty and FIFO almost full, and the threshold of almost empty and almost full can be configured via REG 0xA2. All data will be cleared after writing “1” to FIFO_CLEAR(in REG 0xA3).

It is always recommended to read data from FIFO by the length of times of (2 x enabled ALS channels) to avoid chaotic situation. For example, when both ALS CH0 & CH1 are enabled, FIFO mode is enabled too, it is better to read data by times of 4, then can always easily be sure the sequence of reading data is ALS CH0 high, ALS CH0 low, ALS CH1 high, ALS CH1 low …

External SYNC function

ALS integration can be triggered with SYNC pin and the delay time from external SYNC trigger to real ALS integration can be configured. Detailed settings are under REG 0x52, 0xE2 and 0xE3. SIP1221LR1S can also be configured to respond every certain number of SYNC pulses with REG 0xE4. SYNC signal lost and period change will be monitored and once happened triggers SYNC interrupt (REG 0xE8 ~ 0xEB 0xE0, 0x81). The period of SYNC can also be calculated with the data in REG 0xEC~0xEE. SYNC active polarity can also be configured if needed (REG 0xE0).

4 Register Mapping

All communication with the device shall be performed by reading from and writing to the registers. Any reading or writing operation to this device can activate I2C communication mode.

Addr	Register name	R/W	Default	Description
0x02	CLKCTRL	RW	0x33	Functions clock enable
0x03	ID	R	0x06	Chip ID register
0x05	CTRL	RW	0x01	OSC enable and reset control
0x06	INTCTRL	RW	0x00	Working mode and INT control
0x50	ALSENABLE	RW	0x00	ALS enables
0x51	ALS_CTRL0	RW	0xA0	ALS control register 0
0x52	ALS_CTRL1	RW	0x1C	ALS control register 1
0x53	ALSINT_EN	RW	0x0F	ALS interrupts enables
0x54	ALS_THLOW_H	RW	0x00	High data of ALS interrupt low threshold
0x55	ALS_THLOW_L	RW	0x20	Low data of ALS interrupt low threshold

0x56	ALS_THHIGH_H	RW	0xFF	High data of ALS interrupt high threshold
0x57	ALS_THHIGH_L	RW	0xD0	Low data of ALS interrupt high threshold
0x58	ALSINTE_TIME_H	RW	0x00	High data of ALS integration time
0x59	ALSINTE_TIME_M	RW	0x00	Middle data of ALS integration time
0x5A	ALSINTE_TIME_L	RW	0x00	Low data of ALS integration time
0x5B	ALSPERIOD_STEP	RW	0x00	ALS period step configuration
0x5C	ALSPERIOD_TIME	RW	0x00	ALS period time configuration
0x5D	ALS_RST_NUM	RW	0x01	ALS initialization control
0x5E	ALSAZ_CTRL	RW	0xFF	ALS auto zero control
0x5F	ALSAZ_EN	RW	0xC0	ALS auto zero enables
0x60	RESERVE1	RW	0x05	Reserved registers, must be configured to 0x05
0x62	ALS_GAIN	RW	0x00	Gain setting for ALS channel 0 and channel 1
0x63	ALS_GAIN	RW	0x00	Gain setting for Flicker channel
0x71	FLK_CTRL	RW	0x01	FLK control register
0x73	FLKINTE_TIME_H	RW	0x00	High data of FLK integration time
0x74	FLKINTE_TIME_M	RW	0x00	Middle data of FLK integration time
0x75	ALSINTE_TIME_L	RW	0x00	Low data of FLK integration time
0x81	ALSINT_STATUS	RW	0x00	ALS interrupts status
0x84	DATA_VALID	R	0x00	Data valid status of ALS
0x94	ALSDATA_HIGH	R	0x00	High data of photopic channel
0x95	ALSDATA_LOW	R	0x00	Low data of photopic channel
0x96	WBDATA_HIGH	R	0x00	High data of wideband channel
0x97	WBDATA_LOW	R	0x00	Low data of wideband channel
0x9F	FDATA	R	0x00	The register for FIFO data reading
0xA0	FSTATUS	R	0x0A	High data of FIFO lvel and status of FIFO
0xA1	FLVL	R	0x00	Low data of FIFO level
0xA2	F_THRESH	RW	0x58	FIFO almost empty & full threshold
0xA3	FMODE0	RW	0x00	FIFO mode,FIFO clear
0XA4	FMODE1	RW	0x00	Select which channel's data to send to FIFO
0xE0	SYNC_CTRL	RW	0x00	Control register of external SYNC
0xE2	SYNCDLY_CNT_H	RW	0x00	Delay time from external SYNC trigger to real ALS integration
0xE3	SYNCDLY_CNT_L	RW	0x00	Delay time from external SYNC trigger to real ALS integration
0xE4	SYNCTRIG_CNT	RW	0x00	ALS trigger frequency on external SYNC
0xE8	SYNCWDT_CNT_H	RW	0x00	Watchdog trigger time for external SYNC trigger
0xE9	SYNCWDT_CNT_L	RW	0x00	Watchdog trigger time for external SYNC trigger
0xEA	SYNC_FRQCHG_THRESH_H	RW	0x00	SYNC period time change threshold
0xEB	SYNC_FRQCHG_THRESH_L	RW	0x00	SYNC period time change threshold
0xEC	SYNCPERIOD_H	R	0x00	SYNC period counter high byte
0xED	SYNCPERIOD_M	R	0x00	SYNC period counter middle byte
0xEE	SYNCPERIOD_L	R	0x00	SYNC period counter low byte

CLKCTRL (0x02) (default:0x33)

Bit	Name	R/W	default	Description
7	---	---	0	Reserved and Unused
6	LOWPOWER_EN	RW	0	When write"1", will enable low power mode which can

				help to save more power when sensor is in wait state
5	CLK_FLK_EN	RW	1	Clock enable for flicker detection channel “0”: disable “1”: enable
4	CLK_ALS_EN	RW	1	Clock enable for ALS function “0”: disable “1”: enable
3:2	---	---	00	Reserved and Unused
1	CLK_EFUSE_EN	RW	1	Clock enable for efuse clock “0”: disable “1”: enable
0	CLK_DIG_EN	RW	1	Clock enable for digital; it is always required to be enabled unless sensor is in sleep or idle state “0”: disable “1”: enable

ID (0x03) (default:0x06)

Bit	Name	R/W	default	Description
7:0	ID	R	00000110	SIP1221LR1S ID value, 0x06.

CTRL(0x05) (default:0x01)

Bit	Name	R/W	default	Description
7:2	---	---	000000	Reserved and Unused
1	OSC_EN	RW	0	Oscillator enable “0”: disable “1”: enable
0	SOFT_RST_N	RW	1	Soft reset trigger, this bit will be set to “1” after soft reset is completed. “0”: trigger soft reset “1”: normal operation

INTCTRL (0x06) (default:0x00)

Bit	Name	R/W	default	Description
7:4	---	---	0000	Reserved and Unused
3	Reserved	RW	0	Must be set to “0” for normal operation
2	INT_EN	RW	0	INT pin output enable, it must be enabled if want to output internal interrupts to external “0”: disable “1”: enable
1	INT_POLARITY	RW	0	Output level polarity configuration “0”: output active low “1”: output active high

0	INT_CLR_MODE	RW	0	Interrupt clear mode, for REG 0x81 "0": interrupts will be cleared after reading related status registers "1": interrupts will be cleared after writing "1" to related status bit

ALSENABLE (0x50) (default:0x00)

Bit	Name	R/W	default	Description
7:6	---	---	00	Reserved and Unused
5	AL2_EN	RW	0	ambient light channel2(flicker)
4	AL1_EN	RW	0	ambient light channel1(wideband)
3	AL0_EN	RW	0	ambient light channe0(ALS)
2:1	---	---	00	Must be set to "00" for normal operation
0	ALS_EN	RW	0	ALS general switch enable "0": ALS general switch disable "1": ALS general switch enable

ALS_CTRL0 (0x51) (default:0xA0)

Bit	Name	R/W	default	Description
7:1	RESERVED	RW	1010000	Must be set to "1010000" for normal operation
0	ALSPERIOD_EN	RW	0	ALS period control enable, it will only be used when required ALS sample rate is low and lower power consumption requirement. "0": disable ALS period control "1": enable ALS period control

ALS_CTRL1 (0x52) (default:0x1C)

Bit	Name	R/W	default	Description
7:4	ALS_PERSIST_NUM	RW	0001	Debounce filter setting for ALS interrupt. ALS_INT will be asserted only when ALS data beyond the thresholds for number of consecutive times. "0": 0 time, ALS_INT will be asserted every ALS cycle no matter the ALS data beyond the thresholds or not; "1": 1 time, ALS_INT will be asserted once ALS data beyond the thresholds; "2": 2 times, ALS_INT will be asserted when ALS data beyond the thresholds for 2 consecutive times; … "15": 15 times, ALS_INT will be asserted when ALS data beyond the thresholds for 15 consecutive times;
3:2	RESERVED	RW	11	Must be set to "11" for normal operation
1:0	ALS_TRIG_MODE	RW	00	Defines the ambient light work trigger mode. "0": Automatic trigger mode; "1": Manually triggered mode;

				“2”: In the vsync trigger mode , the initial(AZ) and integration are after ADTIME; “3”: In the vsync trigger mode , the initial(AZ) is in the ADTIME process, and the integration is performed after ADTIME.

ALSINT_EN (0x53) (default:0x0F)

Bit	Name	R/W	default	Description
7:6	ALS_CH_INT_SEL	---	00	“10”: Select ALS channel 0 (ALS) data for threshold comparison “11”: Select ALS channel 1 (Wideband) data for threshold comparison
5:4	---	---	00	Reserved and Unused
3	ALS_ERR_INT_EN	RW	1	Enable control of the interrupt status to indicate ALS timing error. e.g., ALS period time is too short for ALS integration.
2	ALS_ANA_SAT_INT_EN	RW	1	Enable control of the interrupt status to indicate ALS analog saturation.
1	ALS_DIG_SAT_INT_EN	RW	1	Enable control of the interrupt status to indicate ALS digital saturation.
0	ALS_INT_EN	RW	1	Enable control of the interrupt status to indicate ALS data beyond thresholds event

ALS_THLOW_H (0x54) (default:0x00)

Bit	Name	R/W	default	Description
7:0	ALS_TH_LOW_H	RW	00000000	Upper byte of ALS low data threshold

ALS_THLOW_L (0x55) (default:0x20)

Bit	Name	R/W	default	Description
7:0	ALS_TH_LOW_L	RW	00100000	Lower byte of ALS low data threshold

ALS_THHIGH_H (0x56) (default:0xFF)

Bit	Name	R/W	default	Description
7:0	ALS_TH_HIGH_H	RW	11111111	Upper byte of ALS high data threshold

ALS_THHIGH_L (0x57) (default:0xD0)

Bit	Name	R/W	default	Description
7:0	ALS_TH_HIGH_L	RW	11010000	Lower byte of ALS high data threshold

ALSINTE_TIME_H (0x58) (default:0x00)

Bit	Name	R/W	default	Description
7:2	---	---	000000	Reserved and Unused
1:0	ALS_INTE_TIME_H	RW	00	ALS integration time setting, ALS_INTE_TIME[17:16]

ALSINTE_TIME_M (0x59) (default:0x00)

Bit	Name	R/W	default	Description
7:0	ALS_INTE_TIME_M	RW	00000000	ALS integration time setting, ALS_INTE_TIME[15:8]

ALSINTE_TIME_L (0x5A) (default:0x00)

Bit	Name	R/W	default	Description
7:0	ALS_INTE_TIME_L	RW	00000000	ALS integration time setting, ALS_INTE_TIME[7:0] als_integration_time = (ALS_INTE_TIME + 1) * 1.358μs

ALSPERIOD_STEP (0x5B) (default:0x00)

Bit	Name	R/W	default	Description
7:0	ALS_PERIOD_STEP	RW	00000000	ALS period time step setting. als_period_step = ALS_PERIOD_STEP * 189.6μs

ALSPERIOD_TIME (0x5C) (default:0x00)

Bit	Name	R/W	default	Description
7:0	ALSPERIOD_TIME	RW	00000000	ALS period time setting. als_period_time = ALSPERIOD_TIME * als_period_step

ALS_RST_NUM (0x5D) (default:0x01)

Bit	Name	R/W	default	Description
7:0	RST_NUM	RW	00000001	“0”: Never do internal ALS initialization “1”: Internal ALS initialization will be done every ALS integration “2~255”: Internal ALS initialization will be done every N times ALS integration

ALSAZ_CTRL (0x5E) (default:0xFF)

Bit	Name	R/W	default	Description
7:0	ALS_AZ_NUM	RW	11111111	ALS auto zero setting. “0”: ALS auto zero is disabled “1”: ALS auto zero will be done once every ALS cycle “2”: ALS auto zero will be done once every two ALS cycles … “255”: ALS auto zero will be done only one time after ALS is enabled

ALSAZ_EN (0x5F) (default:0xC0)

Bit	Name	R/W	default	Description
7:1	RESERVED	RW	1100000	Must be set to “1100000” for normal operation
0	ALS_AZ_EN	RW	0	ALS auto zero enable control. “0”: disable ALS auto zero “1”: enable ALS auto zero

RESERVE (0x60) (default:0x05)

Bit	Name	R/W	default	Description
7:0	RESERVED	RW	00000101	Must be set to “00000101” for normal operation

ALS_GAIN (0x62) (default:0x00)

Bit	Name	R/W	default	Description
7:4	ALS1_GAIN	RW	0000	Gain setting for ALS channel1 “0000”: 0.25x “0001”: 0.5x “0010”: 1x … “1100”: 1024x
3:0	ALS0_GAIN	RW	0000	Gain setting for ALS channel0 “0000”: 0.25x “0001”: 0.5x “0010”: 1x … “1100”: 1024x

ALS_GAIN (0x63) (default:0x00)

Bit	Name	R/W	default	Description
7:4	---	---	0000	Reserved and Unused
3:0	ALS2_GAIN	RW	0000	Gain setting for ALS channel2 “0000”: 0.25x “0001”: 0.5x “0010”: 1x … “1100”: 1024x

FLK_CTRL (0x71) (default:0x01)

Bit	Name	R/W	default	Description
7:1	---	---	0000000	Reserved and Unused
0	RESERVED	RW	1	Must be set to “0” for normal operation

FLKINTE_TIME_H (0x73) (default:0x00)

Bit	Name	R/W	default	Description
7:2	---	---	000000	Reserved and Unused
1:0	FLK_INTE_TIME_H	RW	00	FLK integration time setting, FLK_INTE_TIME[17:16]

FLKINTE_TIME_M (0x74) (default:0x00)

Bit	Name	R/W	default	Description
7:0	FLK_INTE_TIME_M	RW	00000000	FLK integration time setting, FLK_INTE_TIME[15:8]

FLKINTE_TIME_L (0x75) (default:0x00)

Bit	Name	R/W	default	Description
7:0	FLK_INTE_TIME_L	RW	00000000	FLK integration time setting, FLK_INTE_TIME[7:0] flk_integration_time = (FLK_INTE_TIME + 1) * 1.358μs

ALSINT_STATUS (0x81) (default:0x00)

Bit	Name	R/W	default	Description
7	FIFO_INT	R	0	Interrupt status to indicate FIFO almost full or empty.
6	SYNC_CHG_INT	R	0	Interrupt status to indicate the difference of two successive external SYNC period exceed the SYNC change time threshold.
5	SYNC_LOST_INT	R	0	Interrupt status to indicate the external SYNC signal detection exceed SYNC watchdog time.
4	FLK_SAT_INT	R	0	Interrupt status to indicate flicker channel saturation.
3	ALS_ERR_INT	R	0	Interrupt status to indicate ALS timing error.
2	ALS_ANS_SAT_INT	R	0	Interrupt status to indicate ALS analog saturation.
1	ALS_DIG_SAT_INT	R	0	Interrupt status to indicate ALS digital saturation.
0	ALS_INT	R	0	Interrupt status to indicate ALS data beyond thresholds event

DATA_VALID (0x84) (default:0x00)

Bit	Name	R/W	default	Description
7:3	---	---	00000	Reserved and Unused
2	ALS_DATA_VALID	R	0	Indicates new ALS data is refreshed after last reading, it will be cleared automatically after the new ALS data is read out.
1:0	---	---	00	Reserved and Unused

ALSDATA_HIGH (0x94) (default:0x00)

Bit	Name	R/W	default	Description
7:0	ALS_DATA_HIGH	R	00000000	High 8 bit of photopic channel data.

ALSDATA_LOW (0x95) (default:0x00)

Bit	Name	R/W	default	Description
7:0	ALS_DATA_LOW	R	00000000	Low 8 bit of photopic channel data.

WBDATA_HIGH (0x96) (default:0x00)

Bit	Name	R/W	default	Description
7:0	WB_DATA_HIGH	R	00000000	High 8 bit of wideband channel data.

WBDATA_LOW (0x97) (default:0x00)

Bit	Name	R/W	default	Description
7:0	WB_DATA_LOW	R	00000000	Low 8 bit of wideband channel data.

FDATA (0x9F) (default:0x00)

Bit	Name	R/W	default	Description
7:0	ALS_DATA	R	00000000	The address of FIFO for ALS data reading. If SAVE_DATA_TO_FIFO=0，the Flicker data is stored in the FIFO. The sequence of data will be **Flicker channel high 8bits, Flicker channel low 8bits**. If SAVE_DATA_TO_FIFO=1，the ALS data is stored in the FIFO.And if ALS_FIFO_DATA_SRC_SEL[3:2]=11, the sequence of data will be ALS channel 0 high 8bits, ALS channel 0 low 8bits, ALS channel 1 high 8bits, ALS channel 1 low 8bits. If ALS_FIFO_DATA_SRC_SEL[3:2]=01, the sequence of data will be ALS channel 0 high 8bits, ALS channel 0 low 8bits. If ALS_FIFO_DATA_SRC_SEL[3:2]=10, the sequence of data will be ALS channel 1 high 8bits, ALS channel 1 low 8bits.

FSTATUS (0xA0) (default:0x0A)

Bit	Name	R/W	default	Description
7:5	FIFO_LVL_L	R	101	2 LSB bits of FIFO level, FIFO_lvl[2:0]
4	FIFO_FULL_INT	R	0	FIFO full status
3	FIFO_EMPTY_INT	R	0	FIFO empty status
2	FIFO_AF_INT	R	0	FIFO almost full status
1	FIFO_AE_INT	R	0	FIFO almost empty status
0	---	---	0	Reserved and Unused

FLVL (0xA1) (default:0x00)

Bit	Name	R/W	default	Description
7	---	---	0	Reserved and Unused
6:0	FIFO_LVL_H	R	00000000	7 MSB bits of FIFO level, FIFO_lvl[9:3]

F_THRESH (0xA2) (default:0x58)

Bit	Name	R/W	default	Description
7:5	FIFO_FULL_TH	RW	010	3 bits of FIFO almost full threshold
4:2	FIFO_EMPTY_TH	RW	110	3 bits of FIFO almost empty threshold
1	FIFO_INTE_ALMOST_FULL_VALID	RW	0	“0”: FIFO almost full as FIFO int invalid “1”: FIFO almost full as FIFO int valid
0	FIFO_INTE_ALMOST_EMPTY_VALID	RW	0	“0”: FIFO almost empty as FIFO int invalid “1”: FIFO almost empty as FIFO int valid

FMODE0 (0xA3) (default:0x00)

Bit	Name	R/W	default	Description
7	---	---	0	Reserved and Unused
6	FIFO_AL_FLAG_STICKY_EN	RW	0	Control Al FIFO flag “0”: FIFO_almost_empty and FIFO_almost_full are non-sticky, vary according to FIFO size. “1”: FIFO_almost_empty and FIFO_almost_full are sticky and hold after an assert until the interrupt is cleared.
5	FIFO_INT_EN	RW	0	FIFO interruption enable

4	FIFO_CLEAR	RW	0	FIFO clear “0”: no clear FIFO “1”: clear FIFO, Write “1” to clear FIFO, all data will be cleared from FIFO.
3	FIFO_MODE	RW	0	“0”: Disable FIFO mode “1”: Enable FIFO mode
2:0	---	---	000	Reserved and Unused

FMODE1 (0xA4) (default:0x00)

Bit	Name	R/W	default	Description
7:5	---	---	000	Reserved and Unused
4	SAVE_DATA_TO_FIFO	RW	0	Control data into the FIFO . “0”: save Flicker data to FIFO. “1”: save ALS data to FIFO.
3:0	ALS_FIFO_DATA_SRC_SEL	RW	0000	“1100”: save ALS channel1 and channel 0 data to FIFO. “1000”: save ALS channel1 data to FIFO. “0100”: save ALS channel0 data to FIFO.

SYNC_CTRL (0xE0) (default:0x00)

Bit	Name	R/W	Default	Description
7:5	---	---	0000	Reserved and Unused
4	SYNC_LOST_FSM_EN	RW	0	1: when vsync_lost_int,als state break 0: when vsync_lost_int,als state keep
3	SYNC_FREQ_INT_EN	RW	0	External SYNC frequency change interrupt enable bit “0”: Disable “1”: Enable When the time difference between two external SYNC periods is greater than SYNC_FRQ_CHG_TH, SYNC_CHG is valid
2	SYNC_LOST_INT_EN	RW	0	SYNC lost interrupt enable bit “0”: Disable “1”: Enable SYNC_LOST is judged when there is no external SYNC signal detection during SYNC_WDT time
1	SYNC_POL	RW	0	SYNC trigger polarity “0”: external SYNC voltage high active “1”: external SYNC voltage low active
0	WDT_EN	RW	0	SYNC lost and frequency change WDT enable “0”: Disable “1”: Enable

SYNCDLY_CNT_H (0xE2) (default:0x00)

Bit	Name	R/W	default	Description

7:0	SYNC_DLY_CNT_H	RW	00000000	Delay time from external SYNC trigger to real ALS integration. It is 16bit width, {SYNC_DLY_CNT_H, SYNC_DLY_CNT_L} * 1.975μs

SYNCDLY_CNT_L (0xE3) (default:0x00)

Bit	Name	R/W	default	Description
7:0	SYNC_DLY_CNT_L	RW	00000000	Delay time from external SYNC trigger to real ALS integration. It is 16bit width, {SYNC_DLY_CNT_H, SYNC_DLY_CNT_L} * 1.975μs

SYNCTRIG_CNT (0xE4) (default:0x00)

Bit	Name	R/W	Default	Description
7:0	SYNC_TRIG_CNT	RW	00000000	It defines the frequency of external SYNC trigger: 0: ALS integration will be triggered by every external SYNC signal; 1~255: ALS integration will be triggered by (SYNC_TRIG_CNT + 1) external SYNC signal pulses, e.g., 1 means every 2 SYNC signal… It is recommended to enable ALS first, then enable external SYNC function

SYNCWDT_CNT_H (0xE8) (default:0x00)

Bit	Name	R/W	Default	Description
7	---	---	0	Reserved and Unused
6:0	SYNC_WDT_CNT_H	RW	0000000	Watchdog trigger time for external SYNC detection, cycle will be 15bit width, {SYNC_WDT_CNT_H, SYNC_WDT_CNT_L }*2^4* 1.975μs.

SYNCWDT_CNT_L (0xE9) (default:0x00)

Bit	Name	R/W	default	Description

7:0	SYNC_WDT_CNT_L	RW	00000000	Watchdog trigger time for external SYNC detection, cycle will be 15bit width, {SYNC_WDT_CNT_H, SYNC_WDT_CNT_L} *2^4* 1.975μs. It defines the maximum time for external SYNC detection. The watch dog timer will be reset once SYNC is detected, otherwise SYNC_LOST will be triggered when SYNC detection won't be happened during the time.

SYNC_FRQCHG_THRESH_H (0xEA) (default:0x00)

Bit	Name	R/W	Default	Description
7:0	SYNC_FRQ_CHG_TH_H	RW	00000000	The threshold of external SYNC period change detection, it is 16bit width, {SYNC_FRQ_CHG_TH_H, SYNC_FRQ_CHG_TH_L] * 2^4 * 1.975μs

SYNC_FRQCHG_THRESH_L (0xEB) (default:0x00)

Bit	Name	R/W	Default	Description
7:0	SYNC_FRQ_CHG_TH_L	RW	00000000	The threshold of external SYNC period change detection, it is 16bit width, {SYNC_FRQ_CHG_TH_H, SYNC_FRQ_CHG_TH_L] * 2^4 * 1.975μs It defines the maximum time difference of successive 2 SYNC period. When the difference is greater than the configured SYNC_FRQ_CHG time the SYNC_CHG will be triggered.

SYNCPERIOD_H (0xEC) (default:0x00)

Bit	Name	R/W	default	Description
3:0	SYNC_PERIOD_H	R	0000	SYNC period counter high byte The counter for external SYNC period is 20 bit width. SYNC period = {SYNC_PERIOD_H, SYNC_PERIOD_M, SYNC_PERIOD_L} * 1.975μs
7:4	---	---	0000	Reserved and Unused

SYNCPERIOD_M (0xED) (default:0x00)

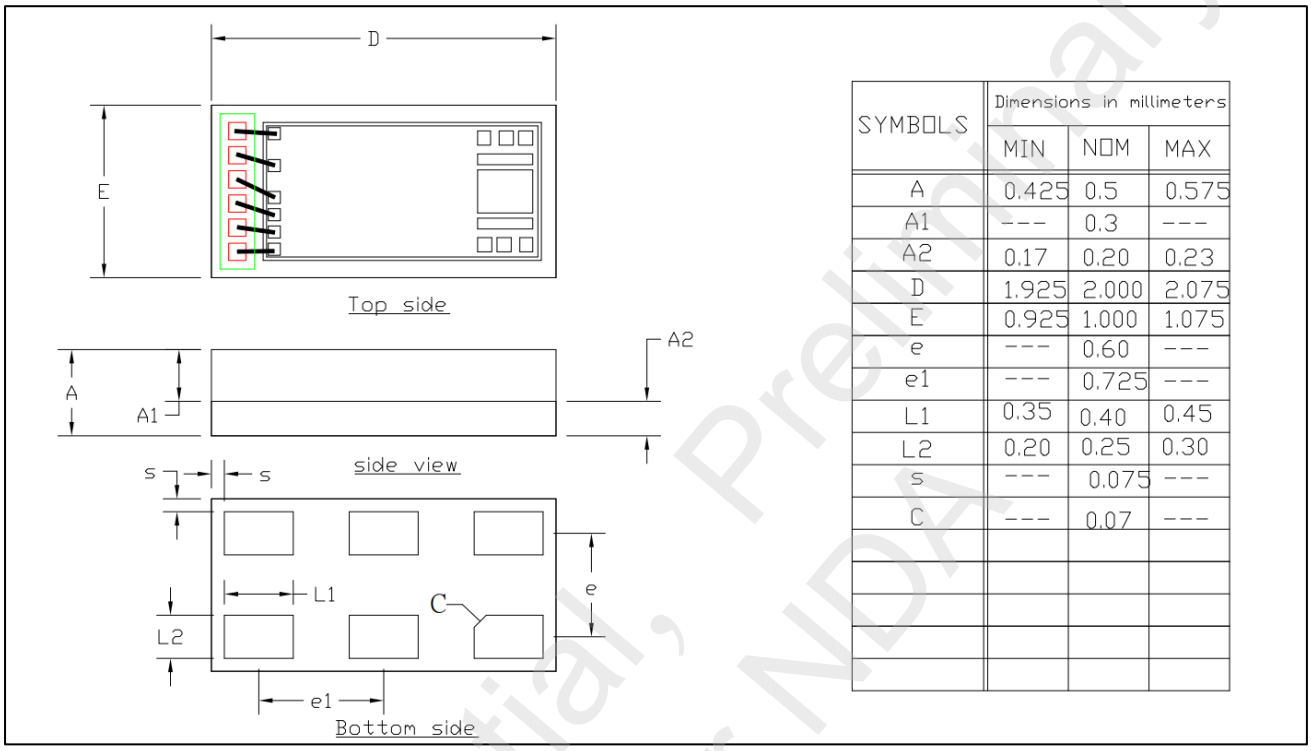
Bit	Name	R/W	default	Description
7:0	SYNC_PERIOD_M	R	00000000	SYNC period counter middle byte The counter for external SYNC period is 20 bit width. SYNC period = {SYNC_PERIOD_H, SYNC_PERIOD_M, SYNC_PERIOD_L} * 1.975μs

SYNCPERIOD_L (0xEE) (default:0x00)

Bit	Name	R/W	default	Description
7:0	SYNC_PERIOD_L	R	00000000	SYNC period counter low byte The counter for external SYNC period is 20 bit width. SYNC period = {SYNC_PERIOD_H, SYNC_PERIOD_M, SYNC_PERIOD_L} * 1.975μs

5 Packaging Information

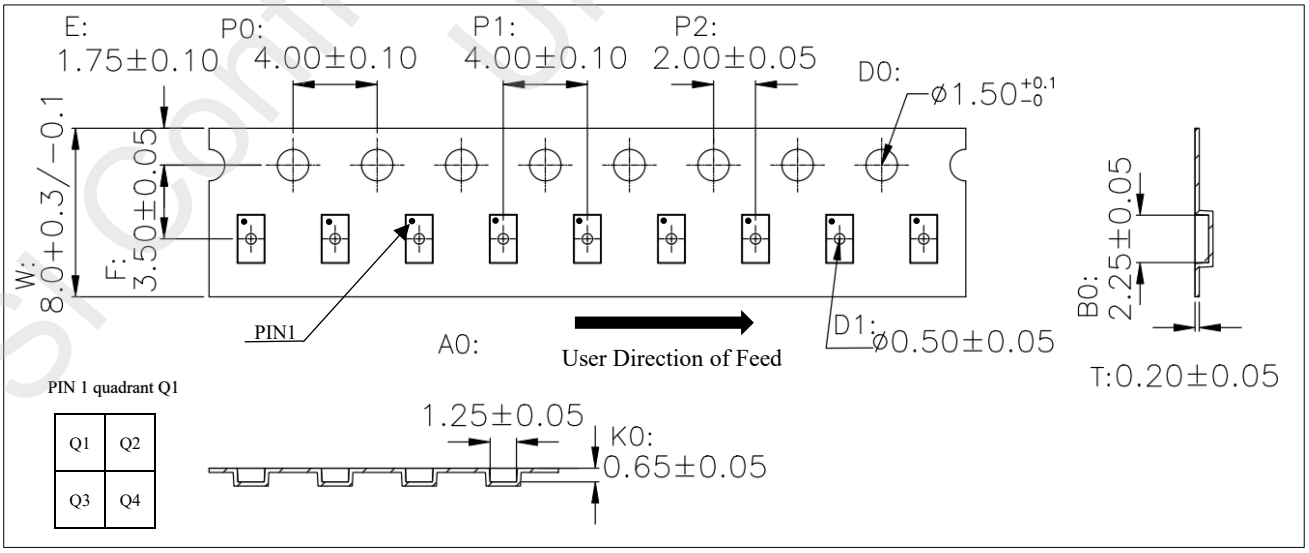
Package Dimension



SYMBOLS	Dimensions in millimeters		
	MIN	NOM	MAX
A	0.425	0.5	0.575
A1	---	0.3	---
A2	0.17	0.20	0.23
D	1.925	2.000	2.075
E	0.925	1.000	1.075
e	---	0.60	---
e1	---	0.725	---
L1	0.35	0.40	0.45
L2	0.20	0.25	0.30
s	---	0.075	---
C	---	0.07	---

Figure 5-1 Package dimension

Tape Reel Information



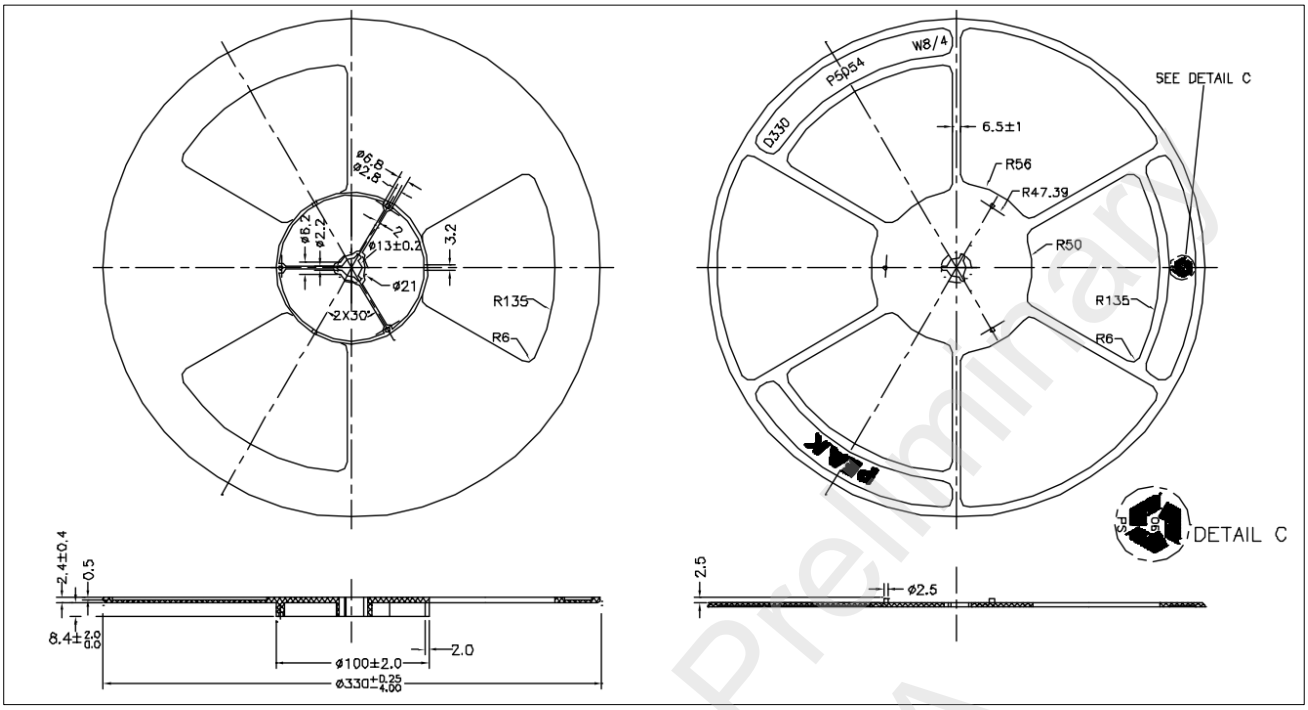


Figure 5-2 Tape reel information

6 Solder Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Solder Flow Profile Graph

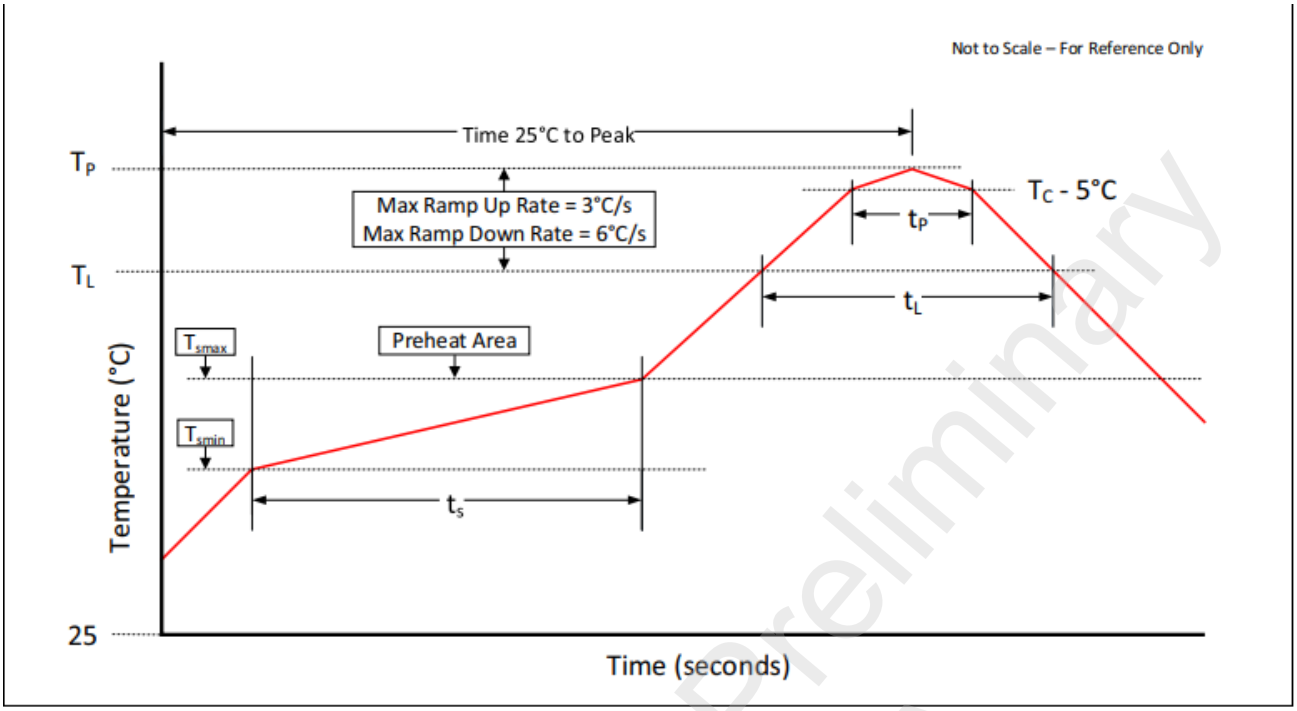


Table 6-1 Solder Reflow Profile

Profile Feature Preheat/Soak	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Temperature Min (T_{smin})	100°C	150°C
Temperature Max (T_{smax})	150°C	200°C
Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds	60-120 seconds
Ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp of 235°C For suppliers T_P must equal or exceed the Classification temp of 235°C	For users T_P must not exceed the Classification temp of 260°C For suppliers T_P must equal or exceed the Classification temp of 260°C
Time (t_P)[(1)] within 5°C of the specified classification temperature (T_c)	20[(1)]seconds	30[(1)]seconds
Ramp-down rate (T_P to T_L)	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

7 Order Information

Table 7-1 Order Information

Product Part	Temp Range	Moisture Sensitivity Level	Package	Delivery Form
SIP1221LR1S	-40 ºC ~ +85ºC	MSL3	WB LGA	10000 pcs/reel

8 Reversion History

Table 8-1Reversion History

Version	Status	Date	Change Notice
0.1	Draft	Feb., 2023	Initial draft
0.2	Preliminary	Feb., 2023	Preliminary version
0.3	Preliminary	Feb., 2023	Preliminary version
0.4	Preliminary	Apr., 2023	Preliminary version