SYNOPSYS®

Sentaurus Technology Template: IGBT Characterization

Abstract

This TCAD Sentaurus™ simulation project provides a template setup for IGBT device characterization.

I_c–V_{ge} curves and a family of I_c–V_{ce} curves are simulated for an IGBT at different device temperatures. In addition, the off-state breakdown as well as the time-dependent switching characteristics are simulated.

Introduction

This project provides standard templates for the device simulator Sentaurus Device that can be used to perform the most common types of simulation used in IGBT device characterization and performance assessment. It contains device simulation setups for I_c–V_{ge} simulation, setups for the simulation of a family of I_c–V_{ce} curves, setups for off-state breakdown simulations, and setups for the simulation of transient switching characteristics.

The IGBT device is defined by using the Sentaurus Structure Editor. The geometric dimensions as well as doping profile parameters, such as peak concentration and junction depth, can be adjusted to specific needs.

The template setup can also be used to investigate the electrical properties of device structures created by the process simulator Sentaurus Process (or others). In this case, Sentaurus Process must be added to the tool flow and the input file of the Sentaurus Structure Editor would need to be adapted to remesh the simulated structure.

It is assumed that users are familiar with the Sentaurus tool suite, in particular, Sentaurus Workbench, Sentaurus Structure Editor, Sentaurus Device, and Sentaurus Visual. For an introduction and tutorials, see the TCAD Sentaurus Tutorial.

The focus of this project is to provide a setup that can be used as is or adapted to specific needs. The documentation focuses on aspects of the setups. For details about tool uses and specific tool syntax, refer to the respective manuals.

General Simulation Setup

This section describes the tool flow of the Sentaurus Workbench project. For each tool, the associated Sentaurus Workbench input parameters and the extracted parameters are discussed.

Sentaurus Structure Editor

Sentaurus Structure Editor defines the analytic IGBT structures.

Sentaurus Device: IcVg

The first instance of Sentaurus Device is `IcVg`. It performs an I_c–V_{ge} sweep at a fixed collector bias for the given devices.

The device temperature, the collector bias V_{ce}, and final gate voltage V_{ge} are defined by the following Sentaurus Workbench parameters:

- `Temp` [K] defines the device temperature. Here, it assumes the values `300` and `425`. You can add or remove values as required.
- `Vg` [V] defines the gate voltage at the end of the I_c–V_{ge} sweep. Here, it is set to `5`.
- `Vc` [V] defines the collector bias. Here, it is set to `5`.
- `IcVg= 0 | 1` is a logical flag. The I_c–V_{ge} sweep is performed only if the flag is `1`.

Sentaurus Visual: PlotIcVg

The subsequent instance of the visualization tool Sentaurus Visual is `PlotIcVg`. It plots the I_c–V_{ge} characteristics and extracts:

- `IcMax` [A/µm]: I_c at V_{ce} = `Vc` and V_{ge} = `Vg`.

Sentaurus Device: IcVc

The following instance of Sentaurus Device is `IcVc`. It simulates a family of I_c–V_{ce} curves. The gate biases are defined by Sentaurus Workbench parameters:

- `Vgmin` [V] defines the gate bias for the first collector voltage sweep. It is set to `3.0`.
- `Vgmax` [V] defines the gate bias for the last collector voltage sweep. It is set to `5.0`.
- `NVg` [1] defines the number of sweeps. It is set to `3`. The gate biases are distributed linearly between the minimum and maximum values.
- `IcVc= 0 | 1` is a logical flag. The I_c–V_{ce} sweep is performed only if the flag is `1`.

Sentaurus Visual: PlotIcVc

The subsequent Sentaurus Visual instance is `PlotIcVc`. It plots the family of I_c–V_{ce} curves.

Sentaurus Device: BV

The next instance of Sentaurus Device is `BV`. It performs the simulation of the off-state breakdown characteristics. The following Sentaurus Workbench parameters are used:

- `Rc` [Ωµm] defines the value of the external resistor, which is attached to the collector (see Device Simulation Using Sentaurus Device on page 5). Here, a value of `1e10` is used.
- `Vcmax` [V] defines the maximum applied (outer) collector voltage. Here, a value of `1e6` is used.

- `BV= 0 | 1` is a logical flag. The off-state breakdown simulation is performed only if the flag is `1`.

Sentaurus Visual: PlotBV

The subsequent Sentaurus Visual instance is `PlotBV`. It plots collector current as a function of the collector voltage and extracts:

- `BVi` [V]: Breakdown voltage defined as the (inner) collector voltage at which a certain collector current level is reached. The value used here is 10^{-7} A/µm. (The current level used for the extraction is set in the Sentaurus Visual input file.)

Sentaurus Device: Transient

The final instance of Sentaurus Device is `Transient`. It simulates the switching characteristics of the IGBT in response to a voltage pulse on the gate:

- `VcT` [V] defines the (outer) collector bias. Here, a value of `200` is used.
- `Transient= 0 | 1` is a logical flag. The transient simulation is performed only if the flag is `1`.

Sentaurus Visual: PlotTransient

The subsequent Sentaurus Visual instance is `PlotTransient`. It plots the gate voltage pulse, the collector current response, the collector voltage response ('inner voltage') as well as the power dissipation as a function of time.

Tool-Specific Setups

This section discusses tool-specific setups.

Device Generation Using Sentaurus Structure Editor

The analytic IGBT structures are defined by Sentaurus Structure Editor. The gate is formed by a 3-µm deep trench with slanted sidewalls filled with polysilicon. The various regions of the device are defined as polygons. For example, the polysilicon gate is defined with:

```
(sdegeo:create-polygon (list
  (position 2.0 0.0 0) (position 2.1 3.13 0)
  (position 2.7 3.13 0) (position 2.8 0.0 0)
  (position 2.0 0.0 0)) "PolySi" "R.PolyGate")
```

The bottom trench corners are rounded with:

```
(sdegeo:fillet-2d (find-vertex-id
  (position 2.1 3.13 0)) 0.2)
(sdegeo:fillet-2d (find-vertex-id
  (position 2.7 3.13 0)) 0.2)
```

The sidewall oxide thickness is 20 nm.

Figure 1 shows the top portion of the IGBT.

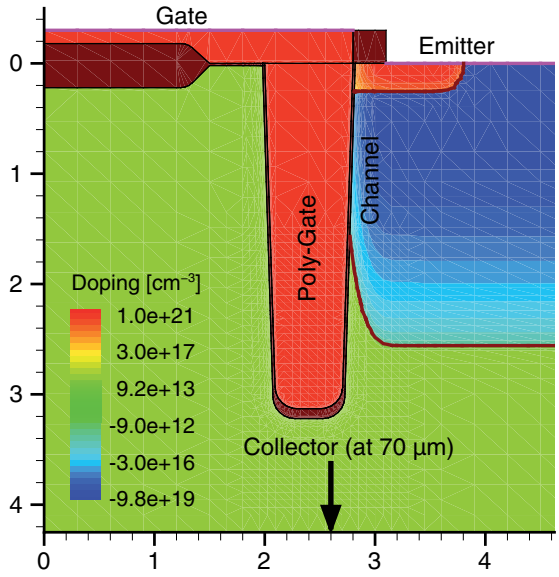

Figure 1 Top portion of IGBT device generated by Sentaurus Structure Editor; concentrations of dopants in various regions are shown

Mesh Generation

The most critical channel area of the IGBT is formed by the slanted trench sidewall. Using the offset feature of Sentaurus Mesh, you can create boundary-conforming meshes. The offset meshing strategy is defined in the command file of Sentaurus Structure Editor.

For example, the specifications for the boundary-conforming mesh at the channel–oxide interface are given by:

```
(sdedr:offset-block "material" "Silicon"
  "maxedgelength" 0.1 "maxlevel" 10)

(sdedr:offset-interface "region" "R.Si" "R.Gox"
  "hlocal" 0.0015 "factor" 1.5)

(sdedr:offset-interface "region" "R.Gox" "R.PolyGate"
  "hlocal" 0.01 "factor" 1.5)

(sdedr:offset-interface "region" "R.Gox" "R.Si"
  "hlocal" 0.003 "factor" 1.5)
```

In the first command, the keyword `maxlevel` specifies that 10 boundary-conforming layers should be created in the silicon region. In the second command, the keyword `hlocal` specifies that the grid spacing at the silicon–oxide interface is 1.5 nm. In the third and fourth commands, the grid spacing values in the gate oxide region at the oxide–polysilicon and oxide–silicon interfaces are set to 10 nm and 3 nm, respectively. The keyword `factor` specifies that the grid spacing increases by a factor of 1.5 for each consecutive layer.

Figure 2 shows a magnified view of the boundary-conforming mesh at the silicon–oxide interface near the bottom of the trench.

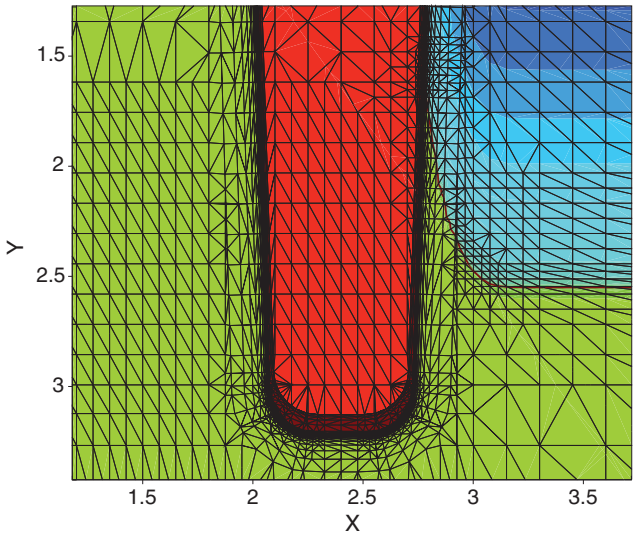

Figure 2 Detail of mesh at bottom of trench; boundary-conforming mesh is generated using the offset feature of Sentaurus Mesh

Device Simulation Using Sentaurus Device

Sentaurus Device simulates the collector current as a function of the gate voltage (I_c–V_{ge}) as well as a family of collector current curves as a function of the collector voltage (I_c–V_{ce}) for different values of the gate bias. Furthermore, the off-state breakdown characteristics and the time-dependent switching characteristics are simulated.

All simulations are performed using the drift-diffusion transport model and the inversion and accumulation layer mobility model (`IALMob`). High-field saturation effects and avalanche generation effects are accounted for.

The `Physics` section of the Sentaurus Device command file is given here:

```
Physics {
  Temperature= @Temp@
  EffectiveIntrinsicDensity(BandGapNarrowing
    (Slotboom))
  Thermodynamic
  AnalyticTEP
}

Physics(Material="Silicon"){
  Mobility (
    Enormal(IALMob)
    HighFieldSaturation
  )
  Recombination (
    SRH(DopingDependence TempDependence)
    Auger
    Avalanche (Lackner)
  )
}
```

The high-field saturation model is activated for both electrons and holes. Since the simulation is performed using the drift-diffusion transport model for both electrons and holes, Sentaurus Device automatically selects `GradQuasiFermi` as the driving-force model for both electrons and holes.

The Lackner impact ionization model is activated. Similar to the case of the high-field saturation model, Sentaurus Device automatically selects `GradQuasiFermi` as the driving force.

Figure 3 shows the I_c–V_{ge} curves for the IGBT for device temperatures of 300 K and 425 K.

For the I_c–V_{ce} simulation, the Tcl block preprocessing mode of Sentaurus Workbench is used to generate input for Sentaurus Device that defines the family of curves. In this mode, any text enclosed in:

```
!( <Tcl-block> )!
```

is treated as a Tcl script block, which is executed at preprocessing time. The text itself is removed during preprocessing, with the exception of the output of the Tcl `puts` commands.

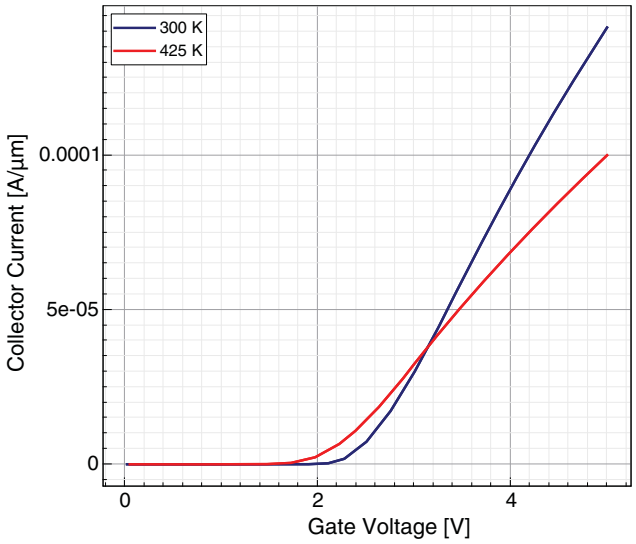

Figure 3 Collector current as a function of gate voltage for IGBT at device temperature of 300 K and 425 K simulated with Sentaurus Device

The first Tcl block generates the `Time` string, which determines at which values of the gate voltage a solution is saved:

```
Quasistationary( ...
      Goal { Name="Gate" Voltage=@Vgmax@ }
   ){ Coupled { Poisson Electron Hole }
      Save( FilePrefix="IcVc_n@node@" NoOverWrite
!(
  set TIMES "Time=("
  for { set i 1 } { $i < @NVg@ } { incr i } {
    set dV [expr (@Vgmax@-@Vgmin@)/(@NVg@-1.0)]
    set Time [expr (@Vgmin@ + ($i-1)*$dV)/@Vgmax@]
    append TIMES "[format %.3f ${Time}];"
```

```
  }
  set Time 1.0
  append TIMES "[format %.3f ${Time}]) )"
  puts $TIMES
)!
   }
```

The Sentaurus Workbench parameters `Vgmin` and `Vgmax` define the first and last gate bias, respectively, and `NVg` defines the number of gate biases for which I_c–V_{ce} sweeps are performed.

The Tcl block of the input file given above is translated during Sentaurus Workbench preprocessing to:

```
Quasistationary( ...
    Goal { Name="Gate" Voltage=5.0 }
   ){ Coupled { Poisson Electron Hole }
    Save( FilePrefix="IcVc_n22" NoOverWrite
    Time=(0.600;0.800;1.000) )
}
```

The next Tcl block generates the input file segments, which reload the previously saved solution for a given gate bias and perform the collector voltage sweep:

```
!(
  for { set i 0 } { $i < @NVg@ } { incr i } {
    set Number [format "%04d" $i]
    puts  "
      NewCurrentFile=\"IcVc_${i}_\"
      Load(FilePrefix=\"IcVc_n@node@_$Number\")
      Quasistationary( ...
         Goal \{Name=\"Collector\" Voltage=@Vc@"\}
      )\{"Coupled \{"Poisson Electron Hole"\}"...
     \}"
  }
)!
```

After preprocessing, the Tcl block is expanded to:

```
      NewCurrentFile="IcVc_0_"
      Load(FilePrefix="IcVc_n22_0000")
      Quasistationary( ...
         Goal { Name="Collector" Voltage=5.0 }
      ){ Coupled { Poisson Electron Hole } ...
      }

      NewCurrentFile="IcVc_1_"
      Load(FilePrefix="IcVc_n22_0001")
      Quasistationary( ...
         MinStep=1e-5 MaxStep=0.05
         Goal { Name="Collector" Voltage=5.0 }
      ){ Coupled { Poisson Electron Hole }...
      }
      ...
```

Figure 4 shows the I_c–V_{ce} curves for the IGBT devices at V_{ce} = 3, 4, and 5 V.

The robust numerics of Sentaurus Device allow simple breakdown simulations to be performed by attaching a large resistor to one of the electrodes and, then, sweeping the bias of this electrode to very large values. After the onset of impact ionization, most of the voltage drop occurs across this resistor if the value chosen is sufficiently large. Therefore, this simple technique achieves an automatic switching from a voltage-controlled prebreakdown regime to a current-controlled postbreakdown regime.

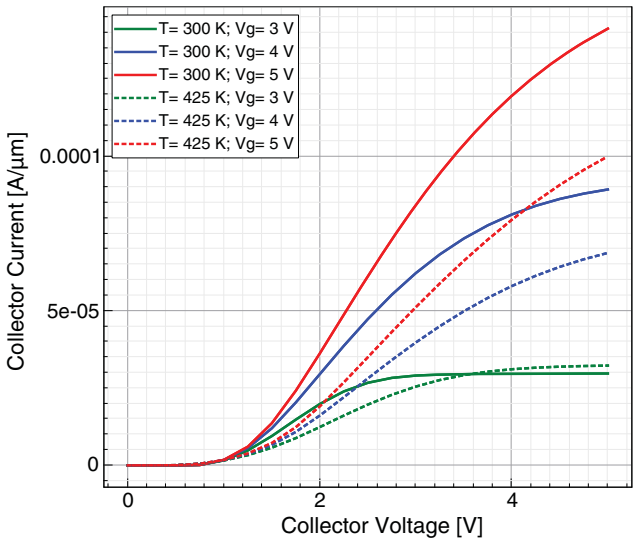

Figure 4 Collector current as a function of collector voltage for IGBT devices simulated with Sentaurus Device; gate bias for curves is 3 V, 4 V, and 5 V; results for device temperature of 300 K (solid lines) and 425 K (dashed lines) are shown

The breakdown characteristics can be seen by plotting the terminal current versus the inner contact voltage instead of the outer. The appropriate value for the attached resistor is of the order of $R = V/I$ at the onset of impact ionization.

This technique is used here for the off-state breakdown simulations. The values of the external resistor are defined by the Sentaurus Workbench parameter `Rc`. The external resistor is declared in the `Electrode` section of Sentaurus Device with:

```
Electrode {...
  { Name="collector" Voltage=0.0 Resistance=@Rc@ }
}
```

The final voltage for the collector bias sweep is defined by the Sentaurus Workbench parameter `Vcmax`. Here, a value of 1 MV is used. Note that the applied (outer) voltage includes the voltage drop across the external resistor; therefore, the maximum collector voltage experienced by the IGBT (‘inner voltage’) is considerably less.

Figure 5 on page 7 shows the off-state breakdown characteristics for the IGBT.

The simulation of the transient switching characteristics is performed here in a mixed-mode environment. That is, instead of simulating an isolated IGBT, the IGBT is embedded in an external circuit. Therefore, it is necessary to specify the width of the device such that the terminal current is given in ampere instead of ampere per micrometer.

The area factor is specified in the general `Physics` section with:

```
Physics {...
  AreaFactor = 1e5 }
```

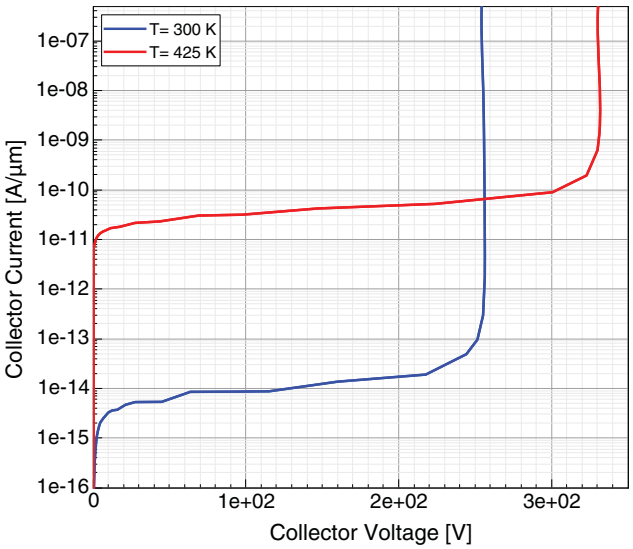

Figure 5 Off-state breakdown characteristics: collector current as a function of the collector voltage at zero gate bias for IGBT; device temperature is 300 K and 425 K

Here, a device width of 100000 µm or 10 cm is specified. The circuit connections to the IGBT and the voltages and currents to be plotted are defined in the `System` section:

```
System {
  IGBT IGBT (Emitter=0 Gate=2 Collector=3)
  Vsource_pset vc (4 0) { dc = 0 }
  Vsource_pset vg (2 0) { pwl = (0 0 2e-7 0 2.01e-7
    15 1e-6 15 1.2e-6 -15 1 -15) }
  Resistor_pset rc (4 3) { resistance = 100 }
  Plot "n@node@_1" (time() v(2) v(3) v(4) i(rc 3))
}
```

The collector is connected to the DC voltage source `vc` by a 100 Ω resistor (`rc`). The gate is connected to a time-dependent voltage source `vg`. The pulse profile is defined as 'piecewise linear,' that is, by a list of time-voltage values. Here, the gate voltage is 0 V for the first 0.2 µs; over the next 1 ns, it rises to 15 V. It remains at 15 V until 1 µs, then it drops to –15 V during an interval of 0.2 µs. It remains at this value for the remainder of the simulation. The emitter is grounded (node `0`). The `Plot` statement directs the voltages at all non-grounded nodes as well as the current through the external resistor `rc` at node `3` to the output file.

In the `Solve` section, first the DC voltage source `vc` is ramped to a value given by the Sentaurus Workbench parameter `VcT`. Here, a value of 400 V is used. Then, the transient simulation of the first 3 µs is performed with:

```
Transient (
    InitialTime=0 FinalTime=3e-6
    InitialStep=1e-12 Increment=1.35
    MinStep=1e-14 MaxStep=1e-7
  ){ Coupled { Poisson Electron Hole }
  }
```

Figure 6 shows the power dissipation as a function of time in the IGBT during a switching event.

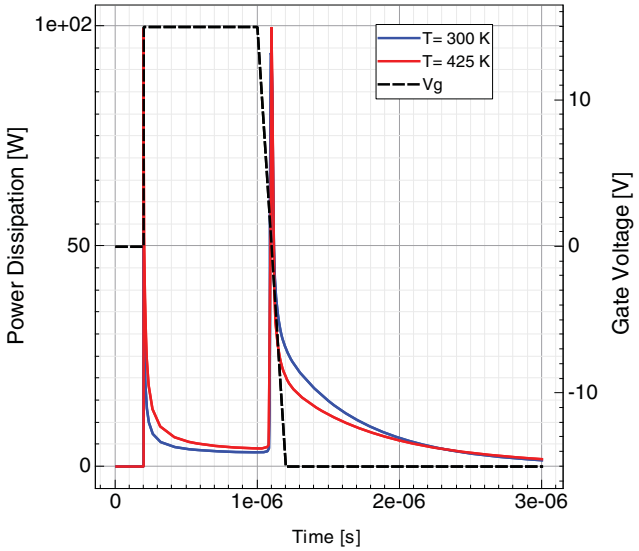

Figure 6 IGBT power dissipation as a function of time in response to a voltage pulse at gate simulated with Sentaurus Device; device temperature is 300 K and 425 K; dashed line shows gate voltage as a function of time

Extraction and Visualization Using Sentaurus Visual

In the Sentaurus Workbench tool flow, each instance of Sentaurus Device is followed by an instance of Sentaurus Visual, which plots the corresponding I–V or switching characteristics, and extracts relevant electrical parameters as discussed in General Simulation Setup on page 3.

See the "Visualizing Simulation Results Using Sentaurus Visual" section of *Process and Device Simulation of Partially Depleted SOI MOSFET* [1], for an example that illustrates the Sentaurus Visual commands for:

- Plotting a curve
- Visualizing curves from multiple Sentaurus Visual nodes in a single Sentaurus Visual tool instance

The extractions are performed using the extraction library of Sentaurus Visual. The extraction library is loaded automatically when Sentaurus Visual starts. However, if you have disabled the automatic loading of extension libraries, you can load the extraction library explicitly with the command:

```
load_library extract
```

See the *Sentaurus™ Visual User Guide* for details about the Sentaurus Visual commands and the procedures of the extraction library. For an introduction to the extraction library, see the "Extraction Using Extraction Library of Sentaurus Visual" section [1].

The breakdown voltage is extracted from the collector current–collector voltage curve using the extraction library procedure `ext::ExtractBVi`:

```
set Vcs [get_variable_data "Collector InnerVoltage" \
  -dataset PLT($N)]
set Ics [get_variable_data "Collector TotalCurrent" \
  -dataset PLT($N)]
ext::ExtractBVi -out BVi -name "out" -v $Vcs -i $Ics \
  -io 1e-7
```

The collector current–collector voltage curve is represented by two Tcl lists: `Vcs` and `Ics`. The `Vcs` list contains the collector inner voltage points, and the `Ics` list contains the corresponding collector current values. The keywords `-v` and `-i` of the procedure are set to `Vcs` and `Ics`, respectively (`-v $Vcs -i $Ics`).

The breakdown voltage is extracted at the current level of `1e-7` A/µm (`-io 1e-7`).

The extracted breakdown voltage value is stored in the Tcl variable `BVi` (specified using the `-out` keyword). It also is displayed as the Sentaurus Workbench variable `BVi` (`-name "out"`).

`IcMax` is extracted using the `ext::ExtractExtremum` procedure, which extracts the maximum of a curve if the keyword `type` is set to `max`:

```
ext::ExtractExtremum -out Icmax -name "Ic" \
  -x $Vgs -y $Ics -type "max"
```

References

[1] *Process and Device Simulation of Partially Depleted SOI MOSFET*, available from TCAD Sentaurus Version V-2024.03 installation, go to `Applications_Library/CMOS/PDSOI`.