
STM32
CubeMX

1. Description

1.1. Project

Project Name	WEACT_743_V2
Board Name	custom
Generated with:	STM32CubeMX 6.15.0
Date	07/25/2025

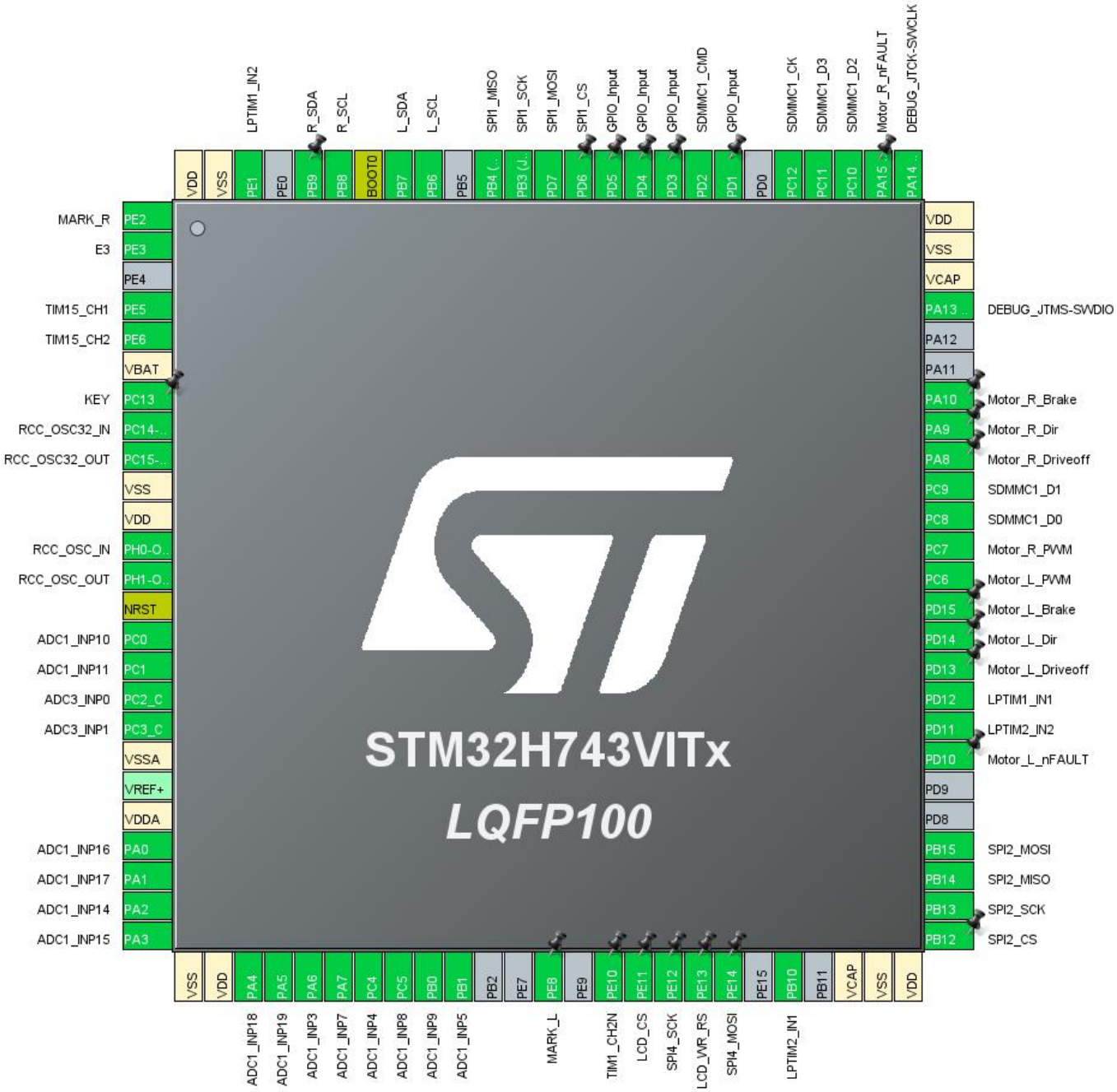
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743VITx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	ARM Cortex-M7

2. Pinout Configuration



3. Pins Configuration

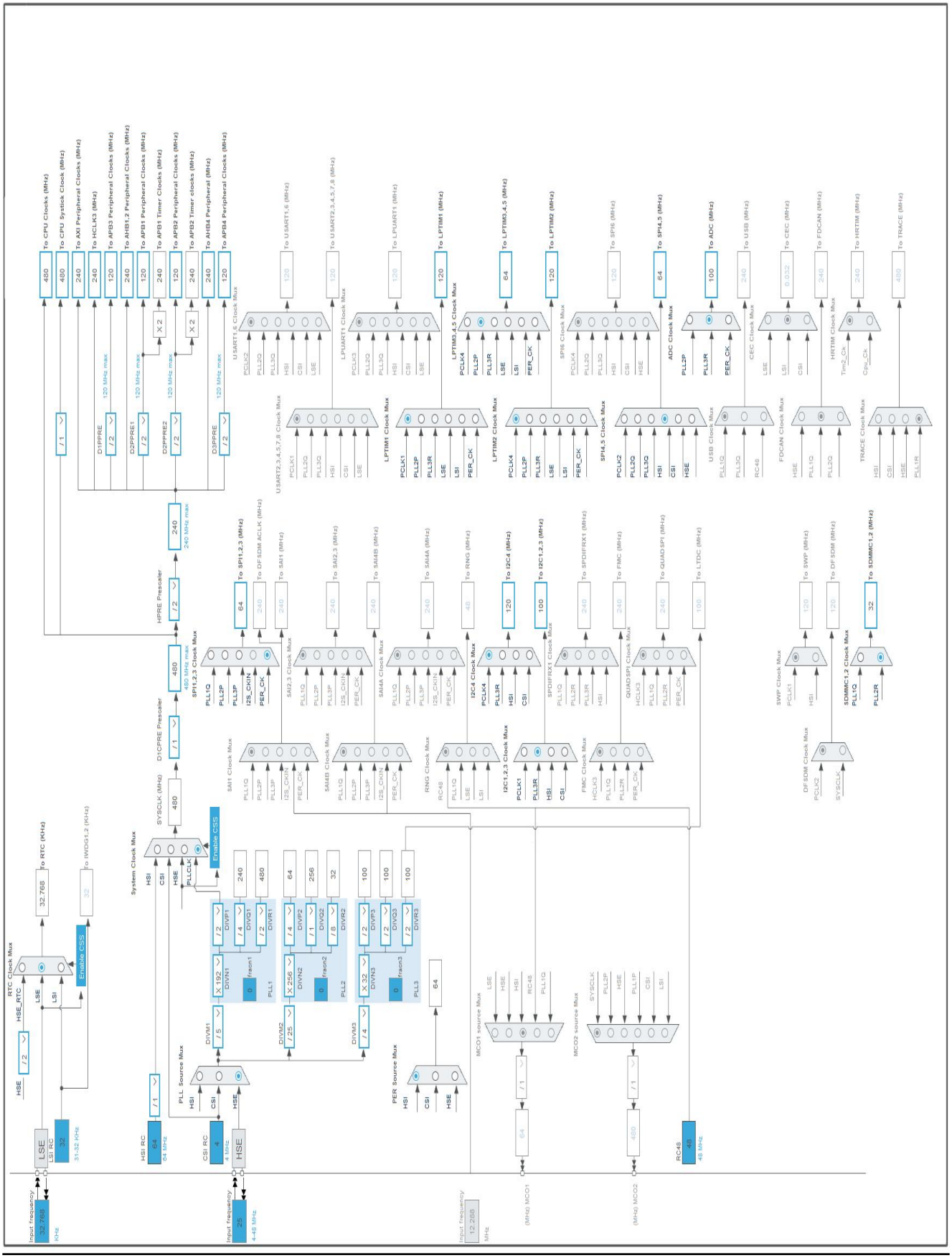
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	MARK_R
2	PE3 *	I/O	GPIO_Output	E3
4	PE5	I/O	TIM15_CH1	
5	PE6	I/O	TIM15_CH2	
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	KEY
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	ADC1_INP10	
16	PC1	I/O	ADC1_INP11	
17	PC2_C	I/O	ADC3_INP0	
18	PC3_C	I/O	ADC3_INP1	
19	VSSA	Power		
21	VDDA	Power		
22	PA0	I/O	ADC1_INP16	
23	PA1	I/O	ADC1_INP17	
24	PA2	I/O	ADC1_INP14	
25	PA3	I/O	ADC1_INP15	
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	ADC1_INP18	
29	PA5	I/O	ADC1_INP19	
30	PA6	I/O	ADC1_INP3	
31	PA7	I/O	ADC1_INP7	
32	PC4	I/O	ADC1_INP4	
33	PC5	I/O	ADC1_INP8	
34	PB0	I/O	ADC1_INP9	
35	PB1	I/O	ADC1_INP5	
38	PE8 *	I/O	GPIO_Output	MARK_L

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
40	PE10	I/O	TIM1_CH2N	
41	PE11 *	I/O	GPIO_Output	LCD_CS
42	PE12	I/O	SPI4_SCK	
43	PE13 *	I/O	GPIO_Output	LCD_WR_RS
44	PE14	I/O	SPI4_MOSI	
46	PB10	I/O	LPTIM2_IN1	
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	SPI2_CS
52	PB13	I/O	SPI2_SCK	
53	PB14	I/O	SPI2_MISO	
54	PB15	I/O	SPI2_MOSI	
57	PD10 *	I/O	GPIO_Input	Motor_L_nFAULT
58	PD11	I/O	LPTIM2_IN2	
59	PD12	I/O	LPTIM1_IN1	
60	PD13 *	I/O	GPIO_Output	Motor_L_Driveoff
61	PD14 *	I/O	GPIO_Output	Motor_L_Dir
62	PD15 *	I/O	GPIO_Output	Motor_L_Brake
63	PC6	I/O	TIM8_CH1	Motor_L_PWM
64	PC7	I/O	TIM8_CH2	Motor_R_PWM
65	PC8	I/O	SDMMC1_D0	
66	PC9	I/O	SDMMC1_D1	
67	PA8 *	I/O	GPIO_Output	Motor_R_Driveoff
68	PA9 *	I/O	GPIO_Output	Motor_R_Dir
69	PA10 *	I/O	GPIO_Output	Motor_R_Brake
72	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
77	PA15 (JTDI) *	I/O	GPIO_Input	Motor_R_nFAULT
78	PC10	I/O	SDMMC1_D2	
79	PC11	I/O	SDMMC1_D3	
80	PC12	I/O	SDMMC1_CK	
82	PD1 *	I/O	GPIO_Input	
83	PD2	I/O	SDMMC1_CMD	
84	PD3 *	I/O	GPIO_Input	
85	PD4 *	I/O	GPIO_Input	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
86	PD5 *	I/O	GPIO_Input	
87	PD6 *	I/O	GPIO_Output	SPI1_CS
88	PD7	I/O	SPI1_MOSI	
89	PB3 (JTDO/TRACESWO)	I/O	SPI1_SCK	
90	PB4 (NJTRST)	I/O	SPI1_MISO	
92	PB6	I/O	I2C1_SCL	L_SCL
93	PB7	I/O	I2C1_SDA	L_SDA
94	BOOT0	Boot		
95	PB8	I/O	I2C4_SCL	R_SCL
96	PB9	I/O	I2C4_SDA	R_SDA
98	PE1	I/O	LPTIM1_IN2	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743VITx
Datasheet	DS12110_Rev8

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

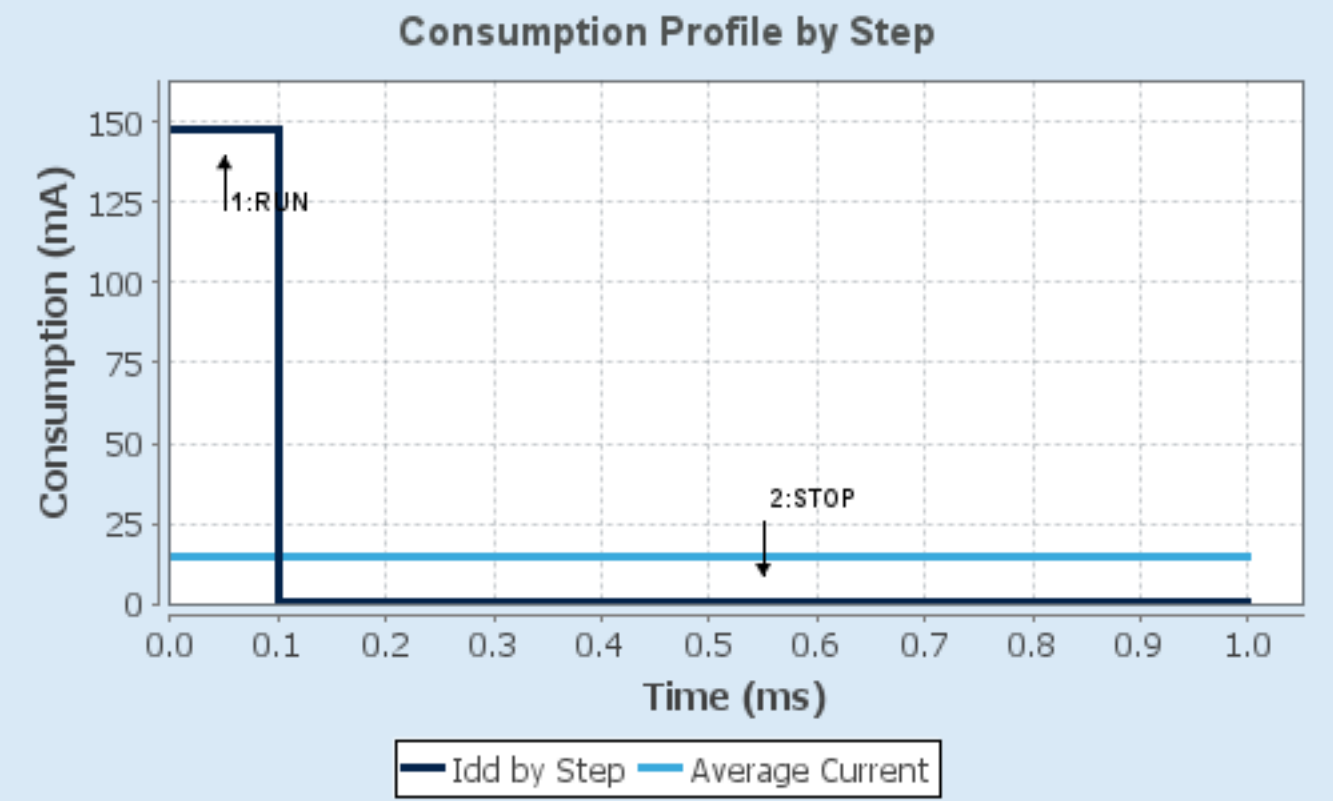
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	ITCM	NA
CPU Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL	Flash-OFF
Clock Source Frequency	24 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	148 mA	150 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Ta Max	105.02	124.98
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Software Project

2.1. Project Settings

Name	Value
Project Name	WEACT_743_V2
Project Folder	C:\Users\kth59\OneDrive\Desktop\WEACT\WEACT 743 V2
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.12.1
Application Structure	Basic
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	No
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_RTC_Init	RTC
4	MX_SPI4_Init	SPI4
5	MX_TIM1_Init	TIM1
6	MX_ADC1_Init	ADC1
7	MX_LPTIM1_Init	LPTIM1
8	MX_LPTIM2_Init	LPTIM2
9	MX_SPI1_Init	SPI1
10	MX_SPI2_Init	SPI2
11	MX_TIM8_Init	TIM8

Rank	Function Name	Peripheral Instance Name
12	MX_LPTIM3_Init	LPTIM3
13	MX_I2C1_Init	I2C1
14	MX_LPTIM4_Init	LPTIM4
15	MX_LPTIM5_Init	LPTIM5
16	MX_I2C4_Init	I2C4
17	MX_SDMMC1_SD_Init	SDMMC1
18	MX_TIM15_Init	TIM15
19	MX_ADC2_Init	ADC2
20	MX_FATFS_Init	FATFS
21	MX_ADC3_Init	ADC3

3. Peripherals and Middlewares Configuration

3.1. ADC1

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN5: IN5 Single-ended

mode: IN7

mode: IN8

mode: IN9

IN10: IN10 Single-ended

mode: IN11

mode: IN14

mode: IN15

IN16: IN16 Single-ended

mode: IN17

IN18: IN18 Single-ended

mode: IN19

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 2 ***
Resolution	**ADC 12-bit optimized resolution ***
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	**Enabled ***
Number Of Discontinuous Conversions	1
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Oversampling Ratio	1
Number Of Conversion	**14 ***

External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 5 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**2 ***
Channel	**Channel 9 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**3 ***
Channel	**Channel 8 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**4 ***
Channel	**Channel 4 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**5 ***
Channel	**Channel 7 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**6 ***
Channel	Channel 3
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**7 ***
Channel	**Channel 19 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**8 ***
Channel	**Channel 18 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**9 ***
Channel	**Channel 15 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset

Rank	**10 ***
Channel	**Channel 14 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**11 ***
Channel	**Channel 17 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**12 ***
Channel	**Channel 16 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**13 ***
Channel	**Channel 11 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
Rank	**14 ***
Channel	**Channel 10 ***
Sampling Time	**32.5 Cycles ***
Offset Number	No offset
ADC_Injected_ConversionMode:	
Enable Injected Conversions	Disable
Analog Watchdog 1:	
Enable Analog WatchDog1 Mode	false
Analog Watchdog 2:	
Enable Analog WatchDog2 Mode	false
Analog Watchdog 3:	
Enable Analog WatchDog3 Mode	false

3.2. ADC2

IN16: Vbat/4 Channel

3.2.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Clock Prescaler	

	Asynchronous clock mode divided by 2 *
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Oversampling Ratio	1
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel Vbat
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
ADC_Injected_ConversionMode:	
Enable Injected Conversions	Disable
Analog Watchdog 1:	
Enable Analog WatchDog1 Mode	false
Analog Watchdog 2:	
Enable Analog WatchDog2 Mode	false
Analog Watchdog 3:	
Enable Analog WatchDog3 Mode	false

3.3. ADC3
mode: IN0
IN1: IN1 Single-ended

3.3.1. Parameter Settings:

ADC_Settings:	
Clock Prescaler	**Asynchronous clock mode divided by 2 ***
Resolution	**ADC 12-bit resolution ***

Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	**Enabled ***
Number Of Discontinuous Conversions	1
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Oversampling Ratio	1
Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	**16.5 Cycles ***
Offset Number	No offset
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	**16.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

3.4. DEBUG

Debug: Serial Wire

3.5. I2C1

I2C: I2C

3.5.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	**Disabled ***
Timing	**0x10C0F1FF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

3.6. I2C4

I2C: I2C

3.6.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x307075B1 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

3.7. LPTIM1

Mode: Encoder mode from IN1 IN2

3.7.1. Parameter Settings:

Clock:

ULP Clock Polarity	Rising Edge
ULP Clock Sample Time	**2 Transitions ***

Preload:

Update Mode	Update Immediate

Trigger:

Trigger Source	Software Trigger

3.8. LPTIM2

Mode: Encoder mode from IN1 IN2

3.8.1. Parameter Settings:

Clock:

ULP Clock Polarity	Rising Edge
ULP Clock Sample Time	**2 Transitions ***

Preload:

Update Mode	Update Immediate

Trigger:

Trigger Source	Software Trigger

3.9. LPTIM3

Mode: Counts internal clock events

3.9.1. Parameter Settings:

Clock:

Clock Prescaler	**Prescaler Div32 ***

Preload:

Update Mode	Update Immediate

Trigger:

Trigger Source	Software Trigger

3.10. LPTIM4

mode: Mode

3.10.1. Parameter Settings:

Clock:

Clock Prescaler	**Prescaler Div32 ***

Preload:

Update Mode	Update Immediate

Trigger:

Trigger Source	Software Trigger

3.11. LPTIM5

mode: Mode

3.11.1. Parameter Settings:

Clock:

Clock Prescaler	**Prescaler Div32 ***

Preload:

Update Mode	Update Immediate

Trigger:

Trigger Source	Software Trigger

3.12. MEMORYMAP

mode: Activated

3.13. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

3.13.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY

Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability
CSI Calibration Value	32
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)
Product revision	rev.V

PLL range Parameters:

PLL1 clock Input range	Between 4 and 8 MHz
PLL2 input frequency range	Between 1 and 2 MHz
PLL3 input frequency range	Between 4 and 8 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range
PLL3 clock Output range	Wide VCO range

3.14. RTC

mode: Activate Clock Source

mode: Activate Calendar

3.14.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	**12 ***
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	**June ***

Date	1
Year	**20 ***

3.15. SDMMC1

Mode: SD 4 bits Wide bus

3.15.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMC clock divide factor	0
Is external transceiver present ?	no

3.16. SPI1

Mode: Full-Duplex Master

3.16.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**32.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle

Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

3.17. SPI2

Mode: Full-Duplex Master

3.17.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**2.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

3.18. SPI4

Mode: Half-Duplex Master

3.18.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola

Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**8.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

3.19. SYS

Timebase Source: SysTick

3.20. TIM1

Clock Source : Internal Clock

Channel2: PWM Generation CH2N

3.20.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**11 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 2N:

Mode	**PWM mode 2 ***
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CHN Polarity	High
CHN Idle State	Reset

3.21. TIM8

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

3.21.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**9599 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	**Enable ***
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

3.22. TIM15

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

3.22.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**249 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**319 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable

Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

3.23. FATFS

mode: SD Card

3.23.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8

FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
FS_LOCK (Number of files opened simultaneously)	2

3.23.2. Advanced Settings:

SDIO/SDMMC:

SDMMC instance	SDMMC1
Use dma template	Disabled
BSP code for SD	Generic

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_INP10	Analog mode	No pull-up and no pull-down	n/a	
	PC1	ADC1_INP11	Analog mode	No pull-up and no pull-down	n/a	
	PA0	ADC1_INP16	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_INP17	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_INP14	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_INP15	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_INP18	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_INP19	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC1_INP7	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_INP4	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_INP8	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_INP9	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PC2_C	ADC3_INP0	Analog mode	No pull-up and no pull-down	n/a	
	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	L_SCL
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	L_SDA
I2C4	PB8	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	R_SCL
	PB9	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	R_SDA
LPTIM1	PD12	LPTIM1_IN1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE1	LPTIM1_IN2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
LPTIM2	PB10	LPTIM2_IN1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD11	LPTIM2_IN2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-	RCC_OSC32_O	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC32_OUT	UT				
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3 (JTDO/TRACESWO)	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4 (NJTRST)	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI4	PE12	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PE14	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
TIM1	PE10	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	Motor_L_PWM
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	Motor_R_PWM
TIM15	PE5	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	TIM15_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MARK_R
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E3
	PC13	GPIO_Input	Input mode	**Pull-down ***	n/a	KEY
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MARK_L
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LCD_CS
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LCD_WR_RS
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2_CS
	PD10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Motor_L_nFAULT
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Motor_L_Driveoff

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Motor_L_Dir
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Motor_L_Brake
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Motor_R_Driveoff
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Motor_R_Dir
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Motor_R_Brake
	PA15 (JTDI)	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Motor_R_nFAULT
	PD1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_CS

4.2. DMA configuration

nothing configured in DMA service

4.3. BDMA configuration

nothing configured in DMA service

4.4. MDMA configuration

nothing configured in DMA service

4.5. NVIC configuration

4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
LPTIM3 global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
SDMMC1 global interrupt	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		
LPTIM1 global interrupt	unused		
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		
TIM15 global interrupt	unused		
HSEM1 global interrupt	unused		
ADC3 global interrupt	unused		
LPTIM2 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
LPTIM4 global interrupt	unused		
LPTIM5 global interrupt	unused		

4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
LPTIM3 global interrupt	false	true	true

*** User modified value**

5. System Views

5.1. Category view

5.1.1. Current

5.1.2. Without filters

5.2. Power Domain view

6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Flyers	https://www.st.com/resource/en/flyer/flpowerstbd.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32h7rs.pdf
Security Bulletin	https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf
Security Bulletin	https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-stmicroelectronics.pdf

Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4539-hrtim-cookbook-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4839-level-1-cache-on-stm32f7-series-and-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4891-stm32h72x-stm32h73x-and-singlecore-stm32h74x75x-system-architecture-and-performance-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4936-migration-of-

	microcontroller-applications-from-stm32f7-series-to-stm32h743753-line-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4990-getting-started-with-sigmadelta-digital-interface-on-applicable-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5027-interfacing-pdm-digital-microphones-using-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5033-stm32cube-mcu-package-examples-for-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5073-receiving-spdif-audio-stream-with-the-stm32f4f7h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5312-migration-from-revy-to-revv-for-stm32h743753-and-stm32h750-value-line-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5354-getting-started-with-the-stm32h7-series-mcu-16bit-adc-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4760-quadspi-interface-on-stm32-microcontrollers-and-microprocessors--stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4899-stm32-microcontroller-gpio-hardware-settings-and-lowpower-consumption-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5612-esd-protection-of-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5293-migration-guide-from-stm32f7-series-to-stmh74x75x-stm32h72x73x-and-stmh7a37bx-devices-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4991-how-to-wake-up-an-stm32-microcontroller-from-lowpower-mode-with-the-usart-or-the-lpuart-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4838-introduction-to-

	memory-protection-unit-management-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5927-i3c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4879-introduction-to-usb-hardware-and-pcb-guidelines-using-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5225-introduction-to-usb-typec-power-delivery-for-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5342--how-to-use-error-correction-code-ecc-management-for-internal-memories-protection-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4938-getting-started-with-stm32h74xig-and-stm32h75xig-mcu-hardware-development-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5537-how-to-use-adc-oversampling-techniques-to-improve-signaltonoise-ratio-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5036-guidelines-for-thermal-management-on-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5405-how-to-use-fdcan-bootloader-protocol-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5690-how-to-use-vrefbuf-peripheral-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4230-introduction-to-random-number-generation-validation-using-the-nist-statistical-test-suite-for-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2867-guidelines-for-oscillator-design-on-stm8afals-and-stm32-mcusmpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4013-introduction-to-timers-for-stm32-mcus-stmicroelectronics.pdf

Application Notes	https://www.st.com/resource/en/application_note/an4277-how-to-use-pwm-shutdown-for-motor-control-and-digital-power-conversion-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4635-how-to-optimize-lpuart-power-consumption-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4759-introduction-to-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4861-introduction-to-lcdtft-display-controller-ltdc-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4908-getting-started-with-usart-automatic-baud-rater-detection-for-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4943-how-to-use-chromart-accelerator-to-refresh-an-lcdtft-display-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5156-introduction-to-security-for-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5200-getting-started-with-stm32h7-mcus-sdmmc-host-controller-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5224-introduction-to-dmamux-for-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5507-how-to-use-crc-to-check-the-integrity-of-the-internal-flash-memory-on-stm32h7-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5543-guidelines-for-enhanced-spi-communication-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5337-guidelines-for-estimating-stm32h7-mcus-lifetime-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4996-how-to-use-the-jpeg-codec-peripheral-on-stm32-mcus-stmicroelectronics.pdf

Application Notes	https://www.st.com/resource/en/application_note/an5348-introduction-to-fdcan-peripherals-for-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/cd00211314-how-to-optimize-the-adc-accuracy-in-the-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack2-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5020-introduction-to-digital-camera-interface-dcmi-for-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4566-how-to-extend-the-dac-performance-on-stm32-mcus-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4323-getting-started-with-stemwin-library-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4435-guidelines-for-obtaining-ulcsaiec-607301603351-class-b-certification-in-any-stm32-application-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4657-stm32-inapplication-programming-iap-using-the-usart-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4841-digital-signal-processing-for-stm32-microcontrollers-using-cmsis-stmicroelectronics.pdf
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