```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                      2 ************************************************************************
                                                      3 *
                                                      4 *            CLC, CLCL, MVCIN and TRT instruction tests
                                                      5 *
                                                      6 ************************************************************************
                                                      7 *
                                                      8 *  This program tests proper functioning of the CLCL, MVCIN and TRT
                                                      9 *  instructions.  It also optionally times them.
                                                     10 *
                                                     11 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                     12 *  obvious coding errors.  None of the tests are thorough.  They are
                                                     13 *  NOT designed to test all aspects of any of the instructions.
                                                     14 *
                                                     15 ************************************************************************
                                                     16 *
                                                     17 *  Example Hercules Testcase:
                                                     18 *
                                                     19 *
                                                     20 *     *Testcase CLCL-et-al (Test CLCL, MVCIN and TRT instructions)
                                                     21 *
                                                     22 *     archlvl     390
                                                     23 *     mainsize    2
                                                     24 *     numcpu      1
                                                     25 *     sysclear
                                                     26 *
                                                     27 *     loadcore    "$(testpath)/CLCL-et-al.core"
                                                     28 *
                                                     29 *     runtest     2         # (NON-timing test duration)
                                                     30 *     ##r           21fd=ff   # (enable timing tests too!)
                                                     31 *     ##runtest     150       # (TIMING too test duration)
                                                     32 *
                                                     33 *     *Compare
                                                     34 *     r 21fe.2
                                                     35 *
                                                     36 *     *Want  "Ending test/subtest number"   9510
                                                     37 *
                                                     38 *     *Done
                                                     39 *
                                                     40 *
                                                     41 ************************************************************************
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                    43          PRINT OFF
                                                  3424          PRINT ON

                                                  3426 ********************************************************************************
                                                  3427 *        SATK prolog stuff...
                                                  3428 ********************************************************************************

                                                  3430          ARCHLVL  ZARCH=NO,MNOTE=NO
                                                  3432+$AL      OPSYN AL
                                                  3433+$ALR     OPSYN ALR
                                                  3434+$B       OPSYN B
                                                  3435+$BAS     OPSYN BAS
                                                  3436+$BASR    OPSYN BASR
                                                  3437+$BC      OPSYN BC
                                                  3438+$BCTR    OPSYN BCTR
                                                  3439+$BE      OPSYN BE
                                                  3440+$BH      OPSYN BH
                                                  3441+$BL      OPSYN BL
                                                  3442+$BM      OPSYN BM
                                                  3443+$BNE     OPSYN BNE
                                                  3444+$BNH     OPSYN BNH
                                                  3445+$BNL     OPSYN BNL
                                                  3446+$BNM     OPSYN BNM
                                                  3447+$BNO     OPSYN BNO
                                                  3448+$BNP     OPSYN BNP
                                                  3449+$BNZ     OPSYN BNZ
                                                  3450+$BO      OPSYN BO
                                                  3451+$BP      OPSYN BP
                                                  3452+$BXLE    OPSYN BXLE
                                                  3453+$BZ      OPSYN BZ
                                                  3454+$CH      OPSYN CH
                                                  3455+$L       OPSYN L
                                                  3456+$LH      OPSYN LH
                                                  3457+$LM      OPSYN LM
                                                  3458+$LPSW    OPSYN LPSW
                                                  3459+$LR      OPSYN LR
                                                  3460+$LTR     OPSYN LTR
                                                  3461+$NR      OPSYN NR
                                                  3462+$SL      OPSYN SL
                                                  3463+$SLR     OPSYN SLR
                                                  3464+$SR      OPSYN SR
                                                  3465+$ST      OPSYN ST
                                                  3466+$STM     OPSYN STM
                                                  3467+$X       OPSYN X
                                                  3468+$AHI     OPSYN AHI
                                                  3469+$B       OPSYN J
                                                  3470+$BC      OPSYN BRC
                                                  3471+$BE      OPSYN JE
                                                  3472+$BH      OPSYN JH
                                                  3473+$BL      OPSYN JL
                                                  3474+$BM      OPSYN JM
                                                  3475+$BNE     OPSYN JNE
```

```
 LOC         OBJECT CODE        ADDR1     ADDR2     STMT

                                                    3476+$BNH     OPSYN JNH
                                                    3477+$BNL     OPSYN JNL
                                                    3478+$BNM     OPSYN JNM
                                                    3479+$BNO     OPSYN JNO
                                                    3480+$BNP     OPSYN JNP
                                                    3481+$BNZ     OPSYN JNZ
                                                    3482+$BO      OPSYN JO
                                                    3483+$BP      OPSYN JP
                                                    3484+$BXLE    OPSYN JXLE
                                                    3485+$BZ      OPSYN JZ
                                                    3486+$CHI     OPSYN CHI
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  3488 ********************************************************************************
                                                  3489 *        Initiate the CLCLetal CSECT in the CODE region
                                                  3490 *        with the location counter at 0
                                                  3491 ********************************************************************************

                                                  3493 CLCLetal ASALOAD  REGION=CODE
                                00000000  00003000  3494+CLCLetal START 0,CODE
00000000  000A0000 00000008                       3496+         PSW   0,0,2,0,X'008'      64-bit Restart ISR Trap New PSW
00000008                      00000008  00000058  3497+         ORG   CLCLetal+X'058'
00000058  000A0000 00000018                       3499+         PSW   0,0,2,0,X'018'      64-bit External ISR Trap New PSW
00000060  000A0000 00000020                       3500+         PSW   0,0,2,0,X'020'      64-bit Supervisor Call ISR Trap New PSW
00000068  000A0000 00000028                       3501+         PSW   0,0,2,0,X'028'      64-bit Program ISR Trap New PSW
00000070  000A0000 00000030                       3502+         PSW   0,0,2,0,X'030'      64-bit Machine Check Trap New PSW
00000078  000A0000 00000038                       3503+         PSW   0,0,2,0,X'038'      64-bit Input/Output Trap New PSW
00000080                      00000080  00000200  3504+         ORG   CLCLetal+512



                                                  3506 ********************************************************************************
                                                  3507 *        Create IPL (restart) PSW
                                                  3508 ********************************************************************************


                                                  3510          ASAIPL   IA=BEGIN
00000200                      00000200  00000000  3511+         ORG   CLCLetal
00000000  00080000 00000200                       3512+         PSW   0,0,0,0,BEGIN,24
00000008                      00000008  00000200  3513+         ORG   CLCLetal+512     Reset CSECT to end of assigned storage area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    3515 ********************************************************************************
                                                    3516 *                The actual "CLCLetal" program itself...
                                                    3517 ********************************************************************************
                                                    3518 *
                                                    3519 *  Architecture Mode: 390
                                                    3520 *  Addressing Mode:   31-bit
                                                    3521 *  Register Usage:
                                                    3522 *
                                                    3523 *   R0       (work)
                                                    3524 *   R1       I/O device used by ENADEV and RAWIO macros
                                                    3525 *   R2       First base register
                                                    3526 *   R3       IOCB pointer for ENADEV and RAWIO macros
                                                    3527 *   R4       IO work register used by ENADEV and RAWIO
                                                    3528 *   R5-R7    (work)
                                                    3529 *   R8       ORB pointer
                                                    3530 *   R9       Second base register
                                                    3531 *   R10-R13  (work)
                                                    3532 *   R14      Subroutine call
                                                    3533 *   R15      Secondary Subroutine call or work
                                                    3534 *
                                                    3535 ********************************************************************************


00000200                    00000000                3537          USING  ASA,R0          Low core addressability
00000200                    00000200                3538          USING  BEGIN,R2        FIRST Base Register
00000200                    00001200                3539          USING  BEGIN+4096,R9   SECOND Base Register
00000200                    00000000                3540          USING  IOCB,R3         SATK Device I/O Control Block
00000200                    00000000                3541          USING  ORB,R8          ESA/390 Operation Request Block


00000200  0520                                      3543 BEGIN    BALR  R2,0             Initalize FIRST base register
00000202  0620                                      3544          BCTR  R2,0             Initalize FIRST base register
00000204  0620                                      3545          BCTR  R2,0             Initalize FIRST base register

00000206  4190 2800                      00000800   3547          LA    R9,2048(,R2)     Initalize SECOND base register
0000020A  4190 9800                      00000800   3548          LA    R9,2048(,R9)     Initalize SECOND base register

0000020E  45E0 91B8                      000013B8   3550          BAL   R14,INIT         Initalize Program
                                                    3551 *
                                                    3552 **       Run the tests...
                                                    3553 *
00000212  45E0 203A                      0000023A   3554          BAL   R14,TEST01       Test CLC   instruction
00000216  45E0 20F0                      000002F0   3555          BAL   R14,TEST02       Test CLCL  instruction
0000021A  45E0 21CA                      000003CA   3556          BAL   R14,TEST03       Test MVCIN instruction
0000021E  45E0 2210                      00000410   3557          BAL   R14,TEST04       Test TRT   instruction
                                                    3558 *
00000222  45E0 22B8                      000004B8   3559          BAL   R14,TEST91       Time CLC   instruction  (speed test)
00000226  45E0 2594                      00000794   3560          BAL   R14,TEST92       Time CLCL  instruction  (speed test)
0000022A  45E0 29C0                      00000BC0   3561          BAL   R14,TEST93       Time MVCIN instruction  (speed test)
0000022E  45E0 2C66                      00000E66   3562          BAL   R14,TEST94       Time TRT   instruction  (speed test)
                                                    3563 *
00000232  45E0 2F16                      00001116   3564          BAL   R14,TEST95       Test CLCL page fault handling
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                    3565 *
00000236  47F0 9208                       00001408  3566          B     EOJ               Normal completion
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3568 ********************************************************************************
                                                  3569 *        TEST01                  Test CLC instruction
                                                  3570 ********************************************************************************

0000023A  9201 9FFE                      000021FE  3572 TEST01   MVI   TESTNUM,X'01'
                                                  3573 *
                                                  3574 **       Initialize test parameters...
                                                  3575 *
0000023E  5850 9428                      00001628  3576          L      R5,CLC4          Operand-1 address
00000242  92FF 5003                      00000003  3577          MVI    3(R5),X'FF'      Force unequal compare (op1 high)
00000246  5850 9438                      00001638  3578          L      R5,CLC256        (same thing for CLC256)
0000024A  92FF 50FF                      000000FF  3579          MVI    255(R5),X'FF'    (same thing for CLC256)
0000024E  5850 9440                      00001640  3580          L      R5,CLCOP1        (same thing for CLCOP1)
00000252  92FF 50FF                      000000FF  3581          MVI    255(R5),X'FF'    (same thing for CLCOP1)
00000256  5860 9434                      00001634  3582          L      R6,CLC8+4        OPERAND-2(!) address
0000025A  92FF 6007                      00000007  3583          MVI    7(R6),X'FF'      Force OPERAND-2 to be high! (op1 LOW!)
                                                  3584 *
                                                  3585 **       Neither cross (one byte)
                                                  3586 *
0000025E  9201 9FFF                      000021FF  3587          MVI   SUBTEST,X'01'
00000262  9856 9408                      00001608  3588          LM    R5,R6,CLC1
00000266  D500 5000 6000      00000000   00000000  3589          CLC   0(1,R5),0(R6)
0000026C  4770 9238                      00001438  3590          BNE   FAILTEST
                                                  3591 *
                                                  3592 **       Neither cross (two bytes)
                                                  3593 *
00000270  9202 9FFF                      000021FF  3594          MVI   SUBTEST,X'02'
00000274  9856 9410                      00001610  3595          LM    R5,R6,CLC2
00000278  D501 5000 6000      00000000   00000000  3596          CLC   0(2,R5),0(R6)
0000027E  4770 9238                      00001438  3597          BNE   FAILTEST
                                                  3598 *
                                                  3599 **       Neither cross (four bytes)
                                                  3600 *
00000282  9204 9FFF                      000021FF  3601          MVI   SUBTEST,X'04'
00000286  9856 9428                      00001628  3602          LM    R5,R6,CLC4
0000028A  D503 5000 6000      00000000   00000000  3603          CLC   0(4,R5),0(R6)
00000290  47D0 9238                      00001438  3604          BNH   FAILTEST                 (see INIT; CLC4:    op1 > op2)
                                                  3605 *
                                                  3606 **       Neither cross (eight bytes)
                                                  3607 *
00000294  9208 9FFF                      000021FF  3608          MVI   SUBTEST,X'08'
00000298  9856 9430                      00001630  3609          LM    R5,R6,CLC8
0000029C  D507 5000 6000      00000000   00000000  3610          CLC   0(8,R5),0(R6)
000002A2  47B0 9238                      00001438  3611          BNL   FAILTEST                 (see INIT; CLC8:    op1 < op2)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3613 *
                                                  3614 **       Neither cross (256 bytes)
                                                  3615 *
000002A6  92FF 9FFF                     000021FF  3616          MVI   SUBTEST,X'FF'
000002AA  9856 9438                     00001638  3617          LM    R5,R6,CLC256
000002AE  D5FF 5000 6000      00000000  00000000  3618          CLC   0(256,R5),0(R6)
000002B4  47D0 9238                     00001438  3619          BNH   FAILTEST                (see INIT; CLC256:  op1 > op2)
                                                  3620 *
                                                  3621 **       Both cross
                                                  3622 *
000002B8  9222 9FFF                     000021FF  3623          MVI   SUBTEST,X'22'
000002BC  9856 9418                     00001618  3624          LM    R5,R6,CLCBOTH
000002C0  D5FF 5000 6000      00000000  00000000  3625          CLC   0(256,R5),0(R6)
000002C6  4770 9238                     00001438  3626          BNE   FAILTEST
                                                  3627 *
                                                  3628 **       Only op1 crosses
                                                  3629 *
000002CA  9210 9FFF                     000021FF  3630          MVI   SUBTEST,X'10'
000002CE  9856 9440                     00001640  3631          LM    R5,R6,CLCOP1
000002D2  D5FF 5000 6000      00000000  00000000  3632          CLC   0(256,R5),0(R6)
000002D8  47D0 9238                     00001438  3633          BNH   FAILTEST                (see INIT; CLCOP1:  op1 > op2)
                                                  3634 *
                                                  3635 **       Only op2 crosses
                                                  3636 *
000002DC  9220 9FFF                     000021FF  3637          MVI   SUBTEST,X'20'
000002E0  9856 9420                     00001620  3638          LM    R5,R6,CLCOP2
000002E4  D5FF 5000 6000      00000000  00000000  3639          CLC   0(256,R5),0(R6)
000002EA  4770 9238                     00001438  3640          BNE   FAILTEST
                                                  3641 *
000002EE  07FE                                    3642          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          3644 ********************************************************************************
                                          3645 *        TEST02                    Test CLCL instruction
                                          3646 ********************************************************************************

000002F0  9202 9FFE                     000021FE  3648 TEST02   MVI   TESTNUM,X'02'
                                          3649 *
                                          3650 **       Initialize test parameters...
                                          3651 *
000002F4  9856 9E6C                     0000206C  3652          LM    R5,R6,CLCL4     CLCL4 test Op1 address and length
000002F8  1E56                                    3653          ALR   R5,R6           Point past last byte
000002FA  0650                                    3654          BCTR  R5,0            Backup to last byte
000002FC  92FF 5000                     00000000  3655          MVI   0(R5),X'FF'     Force unequal compare (op1 high)
                                          3656 *
00000300  9856 9E8C                     0000208C  3657          LM    R5,R6,CLCLOP1   (same thing for CLCLOP1 test)
00000304  1E56                                    3658          ALR   R5,R6                    "
00000306  0650                                    3659          BCTR  R5,0                     "
00000308  92FF 5000                     00000000  3660          MVI   0(R5),X'FF'              "
                                          3661 *
0000030C  9856 9E84                     00002084  3662          LM    R5,R6,CLCL8+8   CLCL8 test ===> OP2 <===
00000310  1E56                                    3663          ALR   R5,R6
00000312  0650                                    3664          BCTR  R5,0
00000314  92FF 5000                     00000000  3665          MVI   0(R5),X'FF'     ===> OPERAND-2 high (OP1 LOW) <===
                                          3666 *
                                          3667 **       Neither cross (one byte)
                                          3668 *
00000318  9201 9FFF                     000021FF  3669          MVI   SUBTEST,X'01'
0000031C  98AD 9E0C                     0000200C  3670          LM    R10,R13,CLCL1
00000320  0FAC                                    3671          CLCL  R10,R12
00000322  4770 9238                     00001438  3672          BNE   FAILTEST
00000326  4150 9EAC                     000020AC  3673          LA    R5,ECLCL1
0000032A  45F0 91CA                     000013CA  3674          BAL   R15,ENDCLCL
                                          3675 *
                                          3676 **       Neither cross (two bytes)
                                          3677 *
0000032E  9202 9FFF                     000021FF  3678          MVI   SUBTEST,X'02'
00000332  98AD 9E1C                     0000201C  3679          LM    R10,R13,CLCL2
00000336  0FAC                                    3680          CLCL  R10,R12
00000338  4770 9238                     00001438  3681          BNE   FAILTEST
0000033C  4150 9EBC                     000020BC  3682          LA    R5,ECLCL2
00000340  45F0 91CA                     000013CA  3683          BAL   R15,ENDCLCL
                                          3684 *
                                          3685 **       Neither cross (four bytes)
                                          3686 **       (inequality on last byte of op1)
                                          3687 *
00000344  9204 9FFF                     000021FF  3688          MVI   SUBTEST,X'04'
00000348  98AD 9E6C                     0000206C  3689          LM    R10,R13,CLCL4
0000034C  0FAC                                    3690          CLCL  R10,R12
0000034E  47D0 9238                     00001438  3691          BNH   FAILTEST                (see INIT; CLCL4:   op1 > op2)
00000352  4150 9F0C                     0000210C  3692          LA    R5,ECLCL4
00000356  45F0 91CA                     000013CA  3693          BAL   R15,ENDCLCL
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3695 *
                                                  3696 **       Neither cross (eight bytes)
                                                  3697 **       (inequality on last byte of op2)
                                                  3698 *
0000035A  9208 9FFF                     000021FF  3699          MVI   SUBTEST,X'08'
0000035E  98AD 9E7C                     0000207C  3700          LM    R10,R13,CLCL8
00000362  0FAC                                    3701          CLCL  R10,R12
00000364  47B0 9238                     00001438  3702          BNL   FAILTEST                  (see INIT; CLCL8:   op1 < op2)
00000368  4150 9F1C                     0000211C  3703          LA    R5,ECLCL8
0000036C  45F0 91CA                     000013CA  3704          BAL   R15,ENDCLCL
                                                  3705 *
                                                  3706 **       Neither cross (1K bytes)
                                                  3707 *
00000370  9200 9FFF                     000021FF  3708          MVI   SUBTEST,X'00'
00000374  98AD 9E3C                     0000203C  3709          LM    R10,R13,CLCL1K
00000378  0FAC                                    3710          CLCL  R10,R12
0000037A  4770 9238                     00001438  3711          BNE   FAILTEST
0000037E  4150 9EDC                     000020DC  3712          LA    R5,ECLCL1K
00000382  45F0 91CA                     000013CA  3713          BAL   R15,ENDCLCL
                                                  3714 *
                                                  3715 **       Both cross
                                                  3716 *
00000386  9222 9FFF                     000021FF  3717          MVI   SUBTEST,X'22'
0000038A  98AD 9E4C                     0000204C  3718          LM    R10,R13,CLCLBOTH
0000038E  0FAC                                    3719          CLCL  R10,R12
00000390  4770 9238                     00001438  3720          BNE   FAILTEST
00000394  4150 9EEC                     000020EC  3721          LA    R5,ECLCLBTH
00000398  45F0 91CA                     000013CA  3722          BAL   R15,ENDCLCL
                                                  3723 *
                                                  3724 **       Only op1 crosses
                                                  3725 **       (inequality on last byte of op1)
                                                  3726 *
0000039C  9210 9FFF                     000021FF  3727          MVI   SUBTEST,X'10'
000003A0  98AD 9E8C                     0000208C  3728          LM    R10,R13,CLCLOP1
000003A4  0FAC                                    3729          CLCL  R10,R12
000003A6  47D0 9238                     00001438  3730          BNH   FAILTEST                  (see INIT; CLCLOP1: op1 > op2)
000003AA  4150 9F2C                     0000212C  3731          LA    R5,ECLCLOP1
000003AE  45F0 91CA                     000013CA  3732          BAL   R15,ENDCLCL
                                                  3733 *
                                                  3734 **       Only op2 crosses
                                                  3735 *
000003B2  9220 9FFF                     000021FF  3736          MVI   SUBTEST,X'20'
000003B6  98AD 9E5C                     0000205C  3737          LM    R10,R13,CLCLOP2
000003BA  0FAC                                    3738          CLCL  R10,R12
000003BC  4770 9238                     00001438  3739          BNE   FAILTEST
000003C0  4150 9EFC                     000020FC  3740          LA    R5,ECLCLOP2
000003C4  45F0 91CA                     000013CA  3741          BAL   R15,ENDCLCL
                                                  3742 *
000003C8  07FE                                    3743          BR    R14
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                    3745 ********************************************************************************
                                                    3746 *        TEST03                    Test MVCIN instruction
                                                    3747 ********************************************************************************

000003CA  9203 9FFE                        000021FE  3749 TEST03   MVI   TESTNUM,X'03'
                                                    3750 *
                                                    3751 **       Neither cross (one byte)
                                                    3752 *
000003CE  4150 9448                        00001648  3753          LA    R5,INV1
000003D2  45F0 91DA                        000013DA  3754          BAL   R15,MVCINTST
                                                    3755 *
                                                    3756 **       Neither cross (two bytes)
                                                    3757 *
000003D6  4150 9458                        00001658  3758          LA    R5,INV2
000003DA  45F0 91DA                        000013DA  3759          BAL   R15,MVCINTST
                                                    3760 *
                                                    3761 **       Neither cross (four bytes)
                                                    3762 *
000003DE  4150 9468                        00001668  3763          LA    R5,INV4
000003E2  45F0 91DA                        000013DA  3764          BAL   R15,MVCINTST
                                                    3765 *
                                                    3766 **       Neither cross (eight bytes)
                                                    3767 *
000003E6  4150 9478                        00001678  3768          LA    R5,INV8
000003EA  45F0 91DA                        000013DA  3769          BAL   R15,MVCINTST
                                                    3770 *
                                                    3771 **       Neither cross (256 bytes)
                                                    3772 *
000003EE  4150 9488                        00001688  3773          LA    R5,INV256
000003F2  45F0 91DA                        000013DA  3774          BAL   R15,MVCINTST
                                                    3775 *
                                                    3776 **       Both cross
                                                    3777 *
000003F6  4150 9498                        00001698  3778          LA    R5,INVBOTH
000003FA  45F0 91DA                        000013DA  3779          BAL   R15,MVCINTST
                                                    3780 *
                                                    3781 **       Only op1 crosses
                                                    3782 *
000003FE  4150 94A8                        000016A8  3783          LA    R5,INVOP1
00000402  45F0 91DA                        000013DA  3784          BAL   R15,MVCINTST
                                                    3785 *
                                                    3786 **       Only op2 crosses
                                                    3787 *
00000406  4150 94B8                        000016B8  3788          LA    R5,INVOP2
0000040A  45F0 91DA                        000013DA  3789          BAL   R15,MVCINTST
                                                    3790 *
0000040E  07FE                                      3791          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3793 ********************************************************************************
                                                  3794 *        TEST04                    Test TRT instruction
                                                  3795 ********************************************************************************
00000410  9204 9FFE                      000021FE  3797 TEST04   MVI   TESTNUM,X'04'
                                                  3798
00000414  5010 22A8                      000004A8  3799          ST    R1,SAVER1          Save register 1
00000418  18F2                                     3800          LR    R15,R2             Save first base register
                                                  3801
0000041A                                          3802          DROP  R2                 Temporarily drop addressability
0000041A                  00000200                3803          USING BEGIN,R15          Establish temporary addressability
                                                  3804
0000041A  4150 96C8                      000018C8  3805          LA    R5,TRTCTL          Point R5 --> testing control table
0000041E                  00000000                3806          USING TRTTEST,R5         What each table entry looks like
                                                  3807
                          0000041E  00000001      3808 TST4LOOP EQU   *
                                                  3809 *
                                                  3810 **       Initialize operand data  (move data to testing address)
                                                  3811 *
0000041E  58A0 5008                      00000008  3812          L     R10,OP1WHERE       Where to move operand-1 data to
00000422  58C0 5014                      00000014  3813          L     R12,OP2WHERE       Where to move operand-2 data to
                                                  3814
00000426  5860 5000                      00000000  3815          L     R6,OP1DATA         Where op1 data is right now
0000042A  5870 5004                      00000004  3816          L     R7,OP1LEN          How much of it there is
0000042E  4470 F292                      00000492  3817          EX    R7,TRTMVC1         Move op1 data to testing location
                                                  3818
00000432  5860 500C                      0000000C  3819          L     R6,OP2DATA         Where op1 data is right now
00000436  5870 5010                      00000010  3820          L     R7,OP2LEN          How much of it there is
0000043A  4470 F298                      00000498  3821          EX    R7,TRTMVC2         Move op1 data to testing location
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3823 *
                                                  3824 **       Initialize R1/R2...      (TRT non-zero CC updates R1/R2!)
                                                  3825 *
0000043E  1F11                                    3826          SLR   R1,R1               (known value)
00000440  5820 9324                     00001524  3827          L     R2,=A(REG2PATT)    (known value)
                                                  3828 *
                                                  3829 **       Execute TRT instruction and check for expected condition code
                                                  3830 *
00000444  5870 5018                     00000018  3831          L     R7,EXLEN           (len-1)
00000448  58B0 501C                     0000001C  3832          L     R11,FAILMASK       (failure CC)
                                                  3833
0000044C  9200 9FFF                     000021FF  3834          MVI   SUBTEST,X'00'      (primary TRT)
00000450  4470 F29E                     0000049E  3835          EX    R7,TRT             TRT...
00000454  9012 F2B0                     000004B0  3836          STM   R1,R2,SAVETRT      (save R1/R2 results)
00000458  44B0 F2A4                     000004A4  3837          EX    R11,TRTBC          fail if...
                                                  3838 *
                                                  3839 **       Verify R1/R2 now contain (or still contain!) expected values
                                                  3840 *
0000045C  9867 5020                     00000020  3841          LM    R6,R7,ENDREGS
                                                  3842
00000460  9201 9FFF                     000021FF  3843          MVI   SUBTEST,X'01'      (R1 result)
00000464  1516                                    3844          CLR   R1,R6              R1 correct?
00000466  4770 F286                     00000486  3845          BNE   TRTFAIL            No, FAILTEST!
                                                  3846
0000046A  9202 9FFF                     000021FF  3847          MVI   SUBTEST,X'02'      (R2 result)
0000046E  1527                                    3848          CLR   R2,R7              R2 correct?
00000470  4770 F286                     00000486  3849          BNE   TRTFAIL            No, FAILTEST!
                                                  3850
00000474  4150 5028                     00000028  3851          LA    R5,TRTNEXT         Go on to next table entry
00000478  D503 9328 5000      00001528  00000000  3852          CLC   =F'0',0(R5)        End of table?
0000047E  4770 F21E                     0000041E  3853          BNE   TST4LOOP           No, loop...
00000482  47F0 F28A                     0000048A  3854          B     TRTDONE            Done! (success!)
                                                  3855
00000486  41E0 9238                     00001438  3856 TRTFAIL  LA    R14,FAILTEST       Unexpected results!
0000048A  5810 F2A8                     000004A8  3857 TRTDONE  L     R1,SAVER1          Restore register 1
0000048E  182F                                    3858          LR    R2,R15             Restore first base register
00000490  07FE                                    3859          BR    R14                Return to caller or FAILTEST
                                                  3860
00000492  D200 A000 6000      00000000  00000000  3861 TRTMVC1  MVC   0(0,R10),0(R6)      (move op1 to where it should be)
00000498  D200 C000 6000      00000000  00000000  3862 TRTMVC2  MVC   0(0,R12),0(R6)      (move op2 to where it should be)
                                                  3863
0000049E  DD00 A000 C000      00000000  00000000  3864 TRT      TRT   0(0,R10),0(R12)    (TRT op1,op2)
000004A4  4700 F286                     00000486  3865 TRTBC    BC    0,TRTFAIL          (fail if unexpected condition code)
                                                  3866
000004A8  00000000                                3867 SAVER1   DC    F'0'
000004B0  00000000 00000000                       3868 SAVETRT  DC    D'0'               (saved R1/R2 from TRT results)
                                                  3869
000004B8                                          3870          DROP  R5
000004B8                                          3871          DROP  R15
000004B8                      00000200            3872          USING BEGIN,R2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    3874 ********************************************************************************
                                                    3875 *        TEST91                  Time CLC instruction  (speed test)
                                                    3876 ********************************************************************************

000004B8  91FF 9FFD                      000021FD  3878 TEST91   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
000004BC  078E                                     3879          BZR   R14              No, skip timing tests

000004BE  9291 9FFE                      000021FE  3881          MVI   TESTNUM,X'91'
000004C2  9201 9FFF                      000021FF  3882          MVI   SUBTEST,X'01'
                                                    3883 *
                                                    3884 **       First, time the overhead...
                                                    3885 *
000004C6  5850 9370                      00001570  3886          L     R5,NUMLOOPS
000004CA  B205 9378                      00001578  3887          STCK  BEGCLOCK
000004CE  0560                                     3888          BALR  R6,0
000004D0  0656                                     3889          BCTR  R5,R6
000004D2  B205 9380                      00001580  3890          STCK  ENDCLOCK
000004D6  45F0 912C                      0000132C  3891          BAL   R15,CALCDUR
000004DA  D207 9390 9388      00001590  00001588  3892          MVC   OVERHEAD,DURATION
                                                    3893 *
                                                    3894 **       Now do the actual timing run...
                                                    3895 *
000004E0  5850 9370                      00001570  3896          L     R5,NUMLOOPS
000004E4  98AD 9E2C                      0000202C  3897          LM    R10,R13,CLCL256
000004E8  B205 9378                      00001578  3898          STCK  BEGCLOCK
000004EC  0560                                     3899          BALR  R6,0
000004EE  D5FF A000 C000      00000000  00000000  3900          CLC   0(256,R10),0(R12)
000004F4  D5FF A000 C000      00000000  00000000  3901          CLC   0(256,R10),0(R12)
                                                    3902 *        ..........ETC..........
                                                    3903          PRINT OFF
                                                    4009          PRINT ON
00000770  D5FF A000 C000      00000000  00000000  4010          CLC   0(256,R10),0(R12)
00000776  D5FF A000 C000      00000000  00000000  4011          CLC   0(256,R10),0(R12)
0000077C  D5FF A000 C000      00000000  00000000  4012          CLC   0(256,R10),0(R12)
00000782  0656                                     4013          BCTR  R5,R6
00000784  B205 9380                      00001580  4014          STCK  ENDCLOCK
                                                    4015 *
00000788  D204 93D9 934C      000015D9  0000154C  4016          MVC   PRTLINE+33(5),=CL5'CLC'
0000078E  45F0 9052                      00001252  4017          BAL   R15,RPTSPEED
00000792  07FE                                     4018          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                          4020 ********************************************************************************
                                          4021 *        TEST92                  Time CLCL instruction  (speed test)
                                          4022 ********************************************************************************

00000794  91FF 9FFD                 000021FD  4024 TEST92   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
00000798  078E                              4025          BZR   R14              No, skip timing tests

0000079A  9292 9FFE                 000021FE  4027          MVI   TESTNUM,X'92'
0000079E  9201 9FFF                 000021FF  4028          MVI   SUBTEST,X'01'
                                          4029 *
                                          4030 **       First, time the overhead...
                                          4031 *
000007A2  5850 9370                 00001570  4032          L     R5,NUMLOOPS
000007A6  B205 9378                 00001578  4033          STCK  BEGCLOCK
000007AA  0560                              4034          BALR  R6,0
000007AC  98AD 9E2C                 0000202C  4035          LM    R10,R13,CLCL256
000007B0  98AD 9E2C                 0000202C  4036          LM    R10,R13,CLCL256
000007B4  98AD 9E2C                 0000202C  4037          LM    R10,R13,CLCL256
                                          4038 *        .........ETC.........
                                          4039          PRINT OFF
                                          4135          PRINT ON
00000934  98AD 9E2C                 0000202C  4136          LM    R10,R13,CLCL256
00000938  98AD 9E2C                 0000202C  4137          LM    R10,R13,CLCL256
0000093C  0656                              4138          BCTR  R5,R6
0000093E  B205 9380                 00001580  4139          STCK  ENDCLOCK
00000942  45F0 912C                 0000132C  4140          BAL   R15,CALCDUR
00000946  D207 9390 9388      00001590  00001588  4141          MVC   OVERHEAD,DURATION
                                          4142 *
                                          4143 **       Now do the actual timing run...
                                          4144 *
0000094C  5850 9370                 00001570  4145          L     R5,NUMLOOPS
00000950  B205 9378                 00001578  4146          STCK  BEGCLOCK
00000954  0560                              4147          BALR  R6,0
00000956  98AD 9E2C                 0000202C  4148          LM    R10,R13,CLCL256
0000095A  0FAC                              4149          CLCL  R10,R12
0000095C  98AD 9E2C                 0000202C  4150          LM    R10,R13,CLCL256
00000960  0FAC                              4151          CLCL  R10,R12
00000962  98AD 9E2C                 0000202C  4152          LM    R10,R13,CLCL256
00000966  0FAC                              4153          CLCL  R10,R12
                                          4154 *        .........ETC.........
                                          4155          PRINT OFF
                                          4346          PRINT ON
00000BA2  98AD 9E2C                 0000202C  4347          LM    R10,R13,CLCL256
00000BA6  0FAC                              4348          CLCL  R10,R12
00000BA8  98AD 9E2C                 0000202C  4349          LM    R10,R13,CLCL256
00000BAC  0FAC                              4350          CLCL  R10,R12
00000BAE  0656                              4351          BCTR  R5,R6
00000BB0  B205 9380                 00001580  4352          STCK  ENDCLOCK
                                          4353 *
00000BB4  D204 93D9 9351      000015D9  00001551  4354          MVC   PRTLINE+33(5),=CL5'CLCL'
00000BBA  45F0 9052                 00001252  4355          BAL   R15,RPTSPEED
00000BBE  07FE                              4356          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4358 ********************************************************************************
                                                  4359 *        TEST93                  Time MVCIN instruction  (speed test)
                                                  4360 ********************************************************************************

00000BC0  91FF 9FFD                     000021FD  4362 TEST93   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
00000BC4  078E                                    4363          BZR   R14              No, skip timing tests

00000BC6  9293 9FFE                     000021FE  4365          MVI   TESTNUM,X'93'
00000BCA  9201 9FFF                     000021FF  4366          MVI   SUBTEST,X'01'
                                                  4367 *
                                                  4368 **       First, time the overhead...
                                                  4369 *
00000BCE  5850 9370                     00001570  4370          L     R5,NUMLOOPS
00000BD2  B205 9378                     00001578  4371          STCK  BEGCLOCK
00000BD6  0560                                    4372          BALR  R6,0
00000BD8  0656                                    4373          BCTR  R5,R6
00000BDA  B205 9380                     00001580  4374          STCK  ENDCLOCK
00000BDE  45F0 912C                     0000132C  4375          BAL   R15,CALCDUR
00000BE2  D207 9390 9388      00001590  00001588  4376          MVC   OVERHEAD,DURATION
                                                  4377 *
                                                  4378 **       Now do the actual timing run...
                                                  4379 *
00000BE8  98AD 9488                     00001688  4380          LM    R10,R13,INV256
00000BEC  D2FF D000 94C8      00000000  000016C8  4381          MVC   0(256,R13),MVCININ
00000BF2  5850 9370                     00001570  4382          L     R5,NUMLOOPS
00000BF6  B205 9378                     00001578  4383          STCK  BEGCLOCK
00000BFA  0560                                    4384          BALR  R6,0
00000BFC  E8FF A000 B000      00000000  00000000  4385          MVCIN 0(256,R10),0(R11)
00000C02  E8FF A000 B000      00000000  00000000  4386          MVCIN 0(256,R10),0(R11)
00000C08  E8FF A000 B000      00000000  00000000  4387          MVCIN 0(256,R10),0(R11)
                                                  4388 *        .........ETC.........
                                                  4389          PRINT OFF
                                                  4484          PRINT ON
00000E42  E8FF A000 B000      00000000  00000000  4485          MVCIN 0(256,R10),0(R11)
00000E48  E8FF A000 B000      00000000  00000000  4486          MVCIN 0(256,R10),0(R11)
00000E4E  E8FF A000 B000      00000000  00000000  4487          MVCIN 0(256,R10),0(R11)
00000E54  0656                                    4488          BCTR  R5,R6
00000E56  B205 9380                     00001580  4489          STCK  ENDCLOCK
                                                  4490 *
00000E5A  D204 93D9 9356      000015D9  00001556  4491          MVC   PRTLINE+33(5),=CL5'MVCIN'
00000E60  45F0 9052                     00001252  4492          BAL   R15,RPTSPEED
00000E64  07FE                                    4493          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4495 ********************************************************************************
                                                  4496 *        TEST94                  Time TRT instruction  (speed test)
                                                  4497 ********************************************************************************

00000E66  91FF 9FFD                     000021FD  4499 TEST94   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
00000E6A  078E                                    4500          BZR   R14              No, skip timing tests

00000E6C  9294 9FFE                     000021FE  4502          MVI   TESTNUM,X'94'
00000E70  9201 9FFF                     000021FF  4503          MVI   SUBTEST,X'01'
                                                  4504 *
                                                  4505 **       First, time the overhead...
                                                  4506 *
00000E74  5850 9370                     00001570  4507          L     R5,NUMLOOPS
00000E78  B205 9378                     00001578  4508          STCK  BEGCLOCK
00000E7C  0560                                    4509          BALR  R6,0
00000E7E  0656                                    4510          BCTR  R5,R6
00000E80  B205 9380                     00001580  4511          STCK  ENDCLOCK
00000E84  45F0 912C                     0000132C  4512          BAL   R15,CALCDUR
00000E88  D207 9390 9388      00001590  00001588  4513          MVC   OVERHEAD,DURATION
                                                  4514 *
                                                  4515 **       Now do the actual timing run...
                                                  4516 *
00000E8E  58A0 932C                     0000152C  4517          L     R10,=A(00+(5*K64))
00000E92  D2FF A000 980C      00000000  00001A0C  4518          MVC   0(256,R10),TRTOP10
00000E98  58C0 9330                     00001530  4519          L     R12,=A(MB+(5*K64))
00000E9C  D2FF C000 9B0C      00000000  00001D0C  4520          MVC   0(256,R12),TRTOP20
00000EA2  5850 9370                     00001570  4521          L     R5,NUMLOOPS
00000EA6  B205 9378                     00001578  4522          STCK  BEGCLOCK
00000EAA  0560                                    4523          BALR  R6,0
00000EAC  DDFF A000 C000      00000000  00000000  4524          TRT   0(256,R10),0(R12)
00000EB2  DDFF A000 C000      00000000  00000000  4525          TRT   0(256,R10),0(R12)
00000EB8  DDFF A000 C000      00000000  00000000  4526          TRT   0(256,R10),0(R12)
                                                  4527 *        .........ETC.........
                                                  4528          PRINT OFF
                                                  4623          PRINT ON
000010F2  DDFF A000 C000      00000000  00000000  4624          TRT   0(256,R10),0(R12)
000010F8  DDFF A000 C000      00000000  00000000  4625          TRT   0(256,R10),0(R12)
000010FE  DDFF A000 C000      00000000  00000000  4626          TRT   0(256,R10),0(R12)
00001104  0656                                    4627          BCTR  R5,R6
00001106  B205 9380                     00001580  4628          STCK  ENDCLOCK
                                                  4629 *
0000110A  D204 93D9 935B      000015D9  0000155B  4630          MVC   PRTLINE+33(5),=CL5'TRT'
00001110  45F0 9052                     00001252  4631          BAL   R15,RPTSPEED
00001114  07FE                                    4632          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4634 ********************************************************************************
                                                  4635 *        TEST95                    Test CLCL page fault handling
                                                  4636 ********************************************************************************

00001116  9295 9FFE                      000021FE  4638 TEST95   MVI   TESTNUM,X'95'
0000111A  9200 9FFF                      000021FF  4639          MVI   SUBTEST,X'00'
                                                  4640 *
                                                  4641 **       Initialize Dynamic Address Translation tables...
                                                  4642 *
0000111E  58A0 9334                      00001534  4643          L     R10,=A(SEGTABLS)   Segment Tables Origin
00001122  41B0 0020                      00000020  4644          LA    R11,NUMPGTBS       Number of Segment Table Entries
00001126  58C0 9338                      00001538  4645          L     R12,=A(PAGETABS)   Page Tables Origin
0000112A  1F00                                     4646          SLR   R0,R0              First Page Frame Address
0000112C  4160 0004                      00000004  4647          LA    R6,4               Size of one table entry
00001130  5870 933C                      0000153C  4648          L     R7,=A(PAGE)        Size of one Page Frame

00001134  50C0 A000                      00000000  4650 SEGLOOP  ST    R12,0(,R10)        Seg Table Entry <= Page Table Origin
00001138  960F A003                      00000003  4651          OI    3(R10),X'0F'       Seg Table Entry <= Page Table Length
0000113C  1EA6                                     4652          ALR   R10,R6             Bump to next Segment Table Entry

0000113E  41D0 0010                      00000010  4654          LA    R13,16             Page Table Entries per Page Table
00001142  5000 C000                      00000000  4655 PAGELOOP ST    R0,0(,R12)         Page Table Entry = Page Frame Address
00001146  1E07                                     4656          ALR   R0,R7              Increment to next Page Frame Address
00001148  1EC6                                     4657          ALR   R12,R6             Bump to next Page Table Entry
0000114A  46D0 2F42                      00001142  4658          BCT   R13,PAGELOOP       Loop until Page table is complete

0000114E  46B0 2F34                      00001134  4660          BCT   R11,SEGLOOP        Loop until all Segment Table Entries built
                                                  4661 *
                                                  4662 **       Update desired page table entry to cause page fault
                                                  4663 *
00001152  98AD 9E9C                      0000209C  4664          LM    R10,R13,CLCLPF     Retrieve CLCL PF test parameters
00001156  185A                                     4665          LR    R5,R10             R5 --> Operand-1
00001158  5E50 9340                      00001540  4666          AL    R5,=A(PFPGBYTS)    R5 --> Operand-1 Page Fault address
0000115C  1865                                     4667          LR    R6,R5              R6 --> Address where PF should occur
0000115E  8850 000C                      0000000C  4668          SRL   R5,12              R5 = Page Frame number
00001162  8950 0002                      00000002  4669          SLL   R5,2               R5 = Page Table Entry number

00001166  9204 9FFF                      000021FF  4671          MVI   SUBTEST,X'04'
0000116A  5E50 9338                      00001538  4672          AL    R5,=A(PAGETABS)    R5 --> Page Table Entry
0000116E  9604 5002                      00000002  4673          OI    2(R5),X'04'        Mark this page invalid
                                                  4674 *
                                                  4675 **       Install program check routine to catch the page fault
                                                  4676 *
00001172  9202 9FFF                      000021FF  4677          MVI   SUBTEST,X'02'
00001176  D207 2FB0 0068      000011B0  00000068  4678          MVC   SVPGMNEW,PGMNPSW   Save original Program New PSW
0000117C  4100 2FC0                      000011C0  4679          LA    R0,MYPGMNEW        Point to temporary Pgm New routine
00001180  5000 006C                      0000006C  4680          ST    R0,PGMNPSW+4       Point Program New PSW to our routine
00001184  9208 0069                      00000069  4681          MVI   PGMNPSW+1,X'08'    Make it a non-disabled-wait PSW!
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   4683 *
                                                   4684 **       Run the test: should cause a page fault
                                                   4685 *
00001188  920F 9FFF                     000021FF  4686          MVI   SUBTEST,X'0F'
0000118C  B700 9368                     00001568  4687          LCTL  R0,R0,CRLREG0      Switch to DAT mode
00001190  B711 936C                     0000156C  4688          LCTL  R1,R1,CTLREG1      Switch to DAT mode
00001194  8200 2FB8                     000011B8  4689          LPSW  DATONPSW           Switch to DAT mode
00001198  4700 2F98                     00001198  4690 BEGDATON NOP   *                  (pad)
0000119C  4700 2F9C                     0000119C  4691          NOP   *                  (pad)
000011A0  B20D 0000                     00000000  4692          PTLB  ,                  Purge Translation Lookaside Buffer
000011A4  0FAC                                    4693 PFINSADR CLCL  R10,R12            Page Fault should occur on this instr
000011A6  0700                                    4694          CNOP  0,8                  (align to doubleword)
000011A8  00000000 00000000                       4695 LOGICERR DC    D'0'                 We should never reach here!
000011B0  00000000 00000000                       4696 SVPGMNEW DC    D'0'                 Original Program New PSW
000011B8  04080000 00001198                       4697 DATONPSW DC    XL4'04080000',A(BEGDATON)  Enable DAT PSW
                                                   4698 *
                                                   4699 **       Temporary Program New routine:
                                                   4700 **       Restore original Program New PSW
                                                   4701 *
000011C0  D207 0068 2FB0  00000068  000011B0      4702 MYPGMNEW MVC   PGMNPSW,SVPGMNEW   Restore original Program New PSW
                                                   4703 *
                                                   4704 **       Verify Program Check occurred on expected instruction
                                                   4705 *
000011C6  9268 9FFF                     000021FF  4706          MVI   SUBTEST,X'68'
000011CA  D503 9344 002C  00001544      0000002C  4707          CLC   =A(PFINSADR),PGMOPSW+4   Program Check where expected?
000011D0  4770 9238                     00001438  4708          BNE   FAILTEST                 No?! Something is VERY WRONG!
                                                   4709 *
                                                   4710 **       Verify Program Check was indeed a page fault
                                                   4711 *
000011D4  9211 9FFF                     000021FF  4712          MVI   SUBTEST,X'11'
000011D8  9511 008F                     0000008F  4713          CLI   PGMICODE+1,X'11'   Verify it's a Page Fault interrupt
000011DC  4770 9238                     00001438  4714          BNE   FAILTEST          If not then something is VERY WRONG!
                                                   4715 *
                                                   4716 **       Verify Page Fault occurred on expected Page
                                                   4717 *
000011E0  9205 9FFF                     000021FF  4718          MVI   SUBTEST,X'05'
000011E4  5800 0090                     00000090  4719          L     R0,PGMTRX          Get where Page Fault occurred
000011E8  8800 000C                     0000000C  4720          SRL   R0,12
000011EC  8900 000C                     0000000C  4721          SLL   R0,12

000011F0  8860 000C                     0000000C  4723          SRL   R6,12              Where Page Fault is expected
000011F4  8960 000C                     0000000C  4724          SLL   R6,12

000011F8  1506                                    4726          CLR   R0,R6              Page Fault occur on expected Page?
000011FA  4770 9238                     00001438  4727          BNE   FAILTEST           No? Then something is very wrong!
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4729 *
                                                  4730 **       Verify CLCL instruction registers were updated as expected
                                                  4731 *
000011FE  9206 9FFF                     000021FF  4732          MVI   SUBTEST,X'06'
00001202  55A0 9E9C                     0000209C  4733          CL    R10,CLCLPF          (op1 greater than starting value?)
00001206  47D0 9238                     00001438  4734          BNH   FAILTEST
0000120A  55C0 9EA4                     000020A4  4735          CL    R12,CLCLPF+4+4      (op2 greater than starting value?)
0000120E  47D0 9238                     00001438  4736          BNH   FAILTEST

00001212  9207 9FFF                     000021FF  4738          MVI   SUBTEST,X'07'
00001216  15BD                                    4739          CLR   R11,R13             (same remaining lengths?)
00001218  4770 9238                     00001438  4740          BNE   FAILTEST
0000121C  55B0 9EA0                     000020A0  4741          CL    R11,CLCLPF+4        (op1 len less than starting value?)
00001220  47B0 9238                     00001438  4742          BNL   FAILTEST
00001224  55D0 9EA8                     000020A8  4743          CL    R13,CLCLPF+4+4+4    (op2 len less than starting value?)
00001228  47B0 9238                     00001438  4744          BNL   FAILTEST

0000122C  9208 9FFF                     000021FF  4746          MVI   SUBTEST,X'08'
00001230  55A0 9F3C                     0000213C  4747          CL    R10,ECLCLPF         (stop before end?)
00001234  47B0 9238                     00001438  4748          BNL   FAILTEST

00001238  9209 9FFF                     000021FF  4750          MVI   SUBTEST,X'09'
0000123C  15A6                                    4751          CLR   R10,R6              (stop at or before expected page?)
0000123E  4720 9238                     00001438  4752          BH    FAILTEST

00001242  9210 9FFF                     000021FF  4754          MVI   SUBTEST,X'10'
00001246  187A                                    4755          LR    R7,R10              (op1 stopped address)
00001248  1E7B                                    4756          ALR   R7,R11              (add remaining length)
0000124A  1576                                    4757          CLR   R7,R6               (would remainder reach PF page?)
0000124C  47D0 9238                     00001438  4758          BNH   FAILTEST

00001250  07FE                                    4760          BR    R14                 Success!
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4762 ********************************************************************************
                                          4763 *        RPTSPEED                  Report instruction speed
                                          4764 ********************************************************************************

00001252  50F0 9128                 00001328  4766 RPTSPEED ST    R15,RPTSAVE        Save return address
00001256  45F0 912C                 0000132C  4767          BAL   R15,CALCDUR        Calculate duration
                                          4768 *
0000125A  4150 9390                 00001590  4769          LA    R5,OVERHEAD        Subtract overhead
0000125E  4160 9388                 00001588  4770          LA    R6,DURATION        From raw timing
00001262  4170 9388                 00001588  4771          LA    R7,DURATION        Yielding true instruction timing
00001266  45F0 9180                 00001380  4772          BAL   R15,SUBDWORD       Do it
                                          4773 *
0000126A  98CD 9388                 00001588  4774          LM    R12,R13,DURATION   Convert to...
0000126E  8CC0 000C                 0000000C  4775          SRDL  R12,12             ... microseconds
                                          4776 *
00001272  4EC0 9398                 00001598  4777          CVD   R12,TICKSAAA       convert HIGH part to decimal
00001276  4ED0 93A0                 000015A0  4778          CVD   R13,TICKSBBB       convert LOW  part to decimal
                                          4779 *
0000127A  F877 93A8 9398      000015A8  00001598  4780          ZAP   TICKSTOT,TICKSAAA            Calculate...
00001280  FC75 93A8 9360      000015A8  00001560  4781          MP    TICKSTOT,=P'4294967296'      ...decimal...
00001286  FA77 93A8 93A0      000015A8  000015A0  4782          AP    TICKSTOT,TICKSBBB            ...microseconds
                                          4783 *
0000128C  D20B 93E3 93FC      000015E3  000015FC  4784          MVC   PRTLINE+43(L'EDIT),EDIT          (edit into...
00001292  DE0B 93E3 93AB      000015E3  000015AB  4785          ED    PRTLINE+43(L'EDIT),TICKSTOT+3     ...print line)
```

```
                                          4787          RAWIO 4,FAIL=FAILIO      Print elapsed time on console
00001298  9200 300E                 0000000E  4788+         MVI   IOCBSC,X'00'           Clear SC information
0000129C  D201 300A 3006      0000000A  00000006  4789+         MVC   IOCBST,IOCBZERO       Clear accumulated status
000012A2  5810 3000                 00000000  4790+         L     1,IOCBDID            Remember the device ID with which I am working
                                          4791+* Initiate Subchannel-based input/output operation
000012A6  5840 3018                 00000018  4792+         $L    4,IOCBORB            Locate the ORB for the channel subsystem
000012AA  B233 4000                 00000000  4793+         SSCH  0(4)                 Initiate the I/O operation
000012AE  A774 00BD                 00001428  4794+         $BC   B'0111',FAILIO       ..Start function failed, report/handle the error
000012B2  5840 3020                 00000020  4795+         $L    4,IOCBIRB            Locate the IRB storage area
000012B6                      00000000  4796+         USING IRB,4                Make it addressable

                                          4798+* Wait for I/O operation to present status via an interruption
000012B6                                  4799+IOWT0007 DS    0H  Wait for I/O to complete
000012B6  D207 90D8 0078      000012D8  00000078  4801+         MVC   IOS0008(8),120(0)               Save Input/Output new PSW
000012BC  D207 0078 90D0      00000078  000012D0  4802+         MVC   120(8,0),ION0008               Establish Input/Ouput new PSW
000012C2  8200 90C8                 000012C8  4803+         $LPSW WPSW0008                Wait for event
000012C8  020A0000 00000000                 4804+WPSW0008 PSW   2,0,2,0,0                 Wait for event
000012D0  00082000 000012E0                 4805+ION0008  PSW   0,0,0,32,IRST0008,24           I/O New PSW: cc==2
000012D8  00000000 00000000                 4806+IOS0008  DC    XL8'00'
                                          4807+* Handle input/output interruption
000012E0                                  4808+IRST0008 DS    0H
000012E0  D207 0078 90D8      00000078  000012D8  4809+         MVC   120(8,0),IOS0008            Restore input/output new PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                         4810+* Process the interruption...
                                         4811+* Validate interruption is for the expected subchannel
000012E6  5510 00B8                      000000B8 4812+         CL    1,IOSSID              Is this the device for which I am waiting?
000012EA  A774 FFE6                      000012B6 4813+         $BNE  IOWT0007              ..No, continue waiting for it
                                         4814+* Accumulate interruption information from IRB
000012EE  B235 4000                      00000000 4815+         TSCH  0(4)                  Retrive interrupt information
000012F2  A744 FFE2                      000012B6 4816+         $BC   B'0100',IOWT0007      CC1 (not status pending), wait for it to arriv
000012F6  A714 0099                      00001428 4817+         $BC   B'0001',FAILIO        CC3 (not operational), an error then
                                         4818+*                                           CC0 (status was pending), accumulate the status
000012FA  D600 300E 4003      0000000E   00000003 4819+         OC    IOCBSC,IRBSCSW+SCSW2  Accumulate status control
00001300  D601 300A 4008      0000000A   00000008 4820+         OC    IOCBST,IRBSCSW+SCSWUS Accumulate device and channel status
00001306  9104 300E                      0000000E 4821+         TM    IOCBSC,SCSWSPRI       Primary subchannel status?
0000130A  A7E4 FFD6                      000012B6 4822+         $BNO  IOWT0007              ..No, wait for primary status
0000130E  D203 3010 4004      00000010   00000004 4823+         MVC   IOCBSCCW,IRBSCSW+SCSWCCW  CCW address
00001314  D201 3016 400A      00000016   0000000A 4824+         MVC   IOCBRCNT,IRBSCSW+SCSWCNT  Residual count
                                         4825+* Test for errors as specified in the IOCB
0000131A  910C 300A                      0000000A 4826+         TM    IOCBUS,CSWCE+CSWDE    Channel end and device end both accumulated?
0000131E  A7E4 0085                      00001428 4827+         $BNO  FAILIO                Hunh? No CE and DE but do have primary status!
                                         4828+* Input/Output operation successful


00001322  58F0 9128                      00001328 4830          L     R15,RPTSAVE           Restore return address
00001326  07FF                                    4831          BR    R15                   Return to caller

00001328  00000000                                4833 RPTSAVE  DC    F'0'                  R15 save area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4835 ********************************************************************************
                                          4836 *        CALCDUR                  Calculate DURATION
                                          4837 ********************************************************************************

0000132C  50F0 9170                  00001370  4839 CALCDUR  ST    R15,CALCRET        Save return address
00001330  9057 9174                  00001374  4840          STM   R5,R7,CALCWORK     Save work registers
                                          4841 *
00001334  9867 9378                  00001578  4842          LM    R6,R7,BEGCLOCK     Remove CPU number from clock value
00001338  8C60 0006                  00000006  4843          SRDL  R6,6                       "
0000133C  8D60 0006                  00000006  4844          SLDL  R6,6                       "
00001340  9067 9378                  00001578  4845          STM   R6,R7,BEGCLOCK             "
                                          4846 *
00001344  9867 9380                  00001580  4847          LM    R6,R7,ENDCLOCK     Remove CPU number from clock value
00001348  8C60 0006                  00000006  4848          SRDL  R6,6                       "
0000134C  8D60 0006                  00000006  4849          SLDL  R6,6                       "
00001350  9067 9380                  00001580  4850          STM   R6,R7,ENDCLOCK             "
                                          4851 *
00001354  4150 9378                  00001578  4852          LA    R5,BEGCLOCK        Starting time
00001358  4160 9380                  00001580  4853          LA    R6,ENDCLOCK        Ending time
0000135C  4170 9388                  00001588  4854          LA    R7,DURATION        Difference
00001360  45F0 9180                  00001380  4855          BAL   R15,SUBDWORD       Calculate duration
                                          4856 *
00001364  9857 9174                  00001374  4857          LM    R5,R7,CALCWORK     Restore work registers
00001368  58F0 9170                  00001370  4858          L     R15,CALCRET        Restore return address
0000136C  07FF                               4859          BR    R15                Return to caller

00001370  00000000                           4861 CALCRET  DC    F'0'               R15 save area
00001374  00000000 00000000                  4862 CALCWORK DC    3F'0'              R5-R7 save area



                                          4864 ********************************************************************************
                                          4865 *        SUBDWORD                 Subtract two doublewords
                                          4866 *        R5 --> subtrahend, R6 --> minuend, R7 --> result
                                          4867 ********************************************************************************

00001380  90AD 91A8                  000013A8  4869 SUBDWORD STM   R10,R13,SUBDWSAV   Save registers
                                          4870 *
00001384  98AB 5000                  00000000  4871          LM    R10,R11,0(R5)      Subtrahend  (value to subtract)
00001388  98CD 6000                  00000000  4872          LM    R12,R13,0(R6)      Minuend     (what to subtract FROM)
0000138C  1FDB                               4873          SLR   R13,R11            Subtract LOW part
0000138E  47B0 9196                  00001396  4874          BNM   *+4+4              (branch if no borrow)
00001392  5FC0 9348                  00001548  4875          SL    R12,=F'1'          (otherwise do borrow)
00001396  1FCA                               4876          SLR   R12,R10            Subtract HIGH part
00001398  90CD 7000                  00000000  4877          STM   R12,R13,0(R7)      Store results
                                          4878 *
0000139C  98AD 91A8                  000013A8  4879          LM    R10,R13,SUBDWSAV   Restore registers
000013A0  07FF                               4880          BR    R15                Return to caller

000013A8  00000000 00000000                  4882 SUBDWSAV DC    2D'0'              R10-R13 save area
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                           4884 ********************************************************************************
                                           4885 *        Program Initialization
                                           4886 ********************************************************************************

000013B8                                   4888 INIT     DS     0H               Program Initialization

000013B8  4130 92A8                 000014A8  4890          LA     R3,IOCB_009      Point to IOCB
000013BC  5880 3018                 00000018  4891          L      R8,IOCBORB       Point to ORB

000013C0  45F0 9248                 00001448  4893          BAL    R15,IOINIT       Initialize the CPU for I/O operations
000013C4  45F0 9256                 00001456  4894          BAL    R15,ENADEV       Enable our device making ready for use
000013C8  07FE                              4895          BR     R14              Return to caller




                                           4897 ********************************************************************************
                                           4898 *        Verify CLCL ending register values
                                           4899 * R10-R12 = actual ending values, R5 --> expected ending values
                                           4900 ********************************************************************************

000013CA  90AD 9F4C                 0000214C  4902 ENDCLCL  STM    R10,R13,CLCLEND      Save actual ending register values
000013CE  D50F 5000 9F4C  00000000  0000214C  4903          CLC    0(4*4,R5),CLCLEND    Do they have the expected values?
000013D4  4770 9238                 00001438  4904          BNE    FAILTEST             If not then the test has failed
000013D8  07FF                              4905          BR     R15                  Otherwise return to caller




                                           4907 ********************************************************************************
                                           4908 *        MVCINTST
                                           4909 ********************************************************************************

000013DA  98AD 5000                 00000000  4911 MVCINTST LM    R10,R13,0(R5)        a(dst),a(src+(len-1)),a(len-1),a(src)
000013DE  4160 95C7                 000017C7  4912          LA     R6,MVCININ+256-1     Point to end of source
000013E2  1F6C                              4913          SLR    R6,R12               Backup by length amount
000013E4  44C0 91F6                 000013F6  4914          EX     R12,MVCINSRC         Initialize source data
000013E8  44C0 91FC                 000013FC  4915          EX     R12,MVCINMVC         Do the Move Inverse
000013EC  44C0 9202                 00001402  4916          EX     R12,MVCINCLC         Compare with expected results
000013F0  4770 9238                 00001438  4917          BNE    FAILTEST             FAIL if not the expected value
000013F4  07FF                              4918          BR     R15                  Otherwise return to caller


000013F6  D200 D000 6000  00000000  00000000  4920 MVCINSRC MVC    0(0,R13),0(R6)       Executed Instruction
000013FC  E800 A000 B000  00000000  00000000  4921 MVCINMVC MVCIN  0(0,R10),0(R11)       Executed Instruction
00001402  D500 A000 95C8  00000000  000017C8  4922 MVCINCLC CLC    0(0,R10),MVCINOUT    Executed Instruction
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4924 ************************************************************************
                                                  4925 *        Normal completion or Abnormal termination PSWs
                                                  4926 ************************************************************************


                                                  4928 EOJ      DWAITEND LOAD=YES          Normal completion
00001408                                          4930+EOJ      DS    0H
00001408  8200 9210                     00001410  4931+         LPSW  DWAT0010
00001410  000A0000 00000000                       4932+DWAT0010 PSW   0,0,2,0,X'000000'


                                                  4934 FAILDEV  DWAIT LOAD=YES,CODE=01     ENADEV failed
00001418                                          4935+FAILDEV  DS    0H
00001418  8200 9220                     00001420  4936+         LPSW  DWAT0011
00001420  000A0000 00010001                       4937+DWAT0011 PSW   0,0,2,0,X'010001'


                                                  4939 FAILIO   DWAIT LOAD=YES,CODE=02     RAWIO failed
00001428                                          4940+FAILIO   DS    0H
00001428  8200 9230                     00001430  4941+         LPSW  DWAT0012
00001430  000A0000 00010002                       4942+DWAT0012 PSW   0,0,2,0,X'010002'


                                                  4944 FAILTEST DWAIT LOAD=YES,CODE=BAD    Abnormal termination
00001438                                          4945+FAILTEST DS    0H
00001438  8200 9240                     00001440  4946+         LPSW  DWAT0013
00001440  000A0000 00010BAD                       4947+DWAT0013 PSW   0,0,2,0,X'010BAD'
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                 4949 ************************************************************************
                                                 4950 *        Initialize the CPU for I/O operations
                                                 4951 ************************************************************************

                                                 4953 IOINIT   IOINIT ,
00001448  B766 9250                   00001450  4954+IOINIT   LCTL  6,6,IOMK0014       Enable subchannel subclasses for interruptions
0000144C  47F0 9254                   00001454  4955+         B     IOMK0014+4
00001450                                        4956+IOMK0014 DS    0F
00001450  FF000000                              4957+         DC    XL4'FF000000'         All subchannel subclasses enabled

00001454  07FF                                  4959          BR    R15                   Return to caller

                                                 4961 ************************************************************************
                                                 4962 *        Enable the device, making it ready for use
                                                 4963 ************************************************************************

                                                 4965 ENADEV   ENADEV ENAOKAY,FAILDEV,REG=4
00001456  5810 929C                   0000149C  4966+ENADEV   L     1,FIND0015
0000145A  5840 3028                   00000028  4967+         $L    4,IOCBSIB             Locate where the SCHIB is to be stored
0000145E                    00000000            4968+         USING SCHIB,4
0000145E                                        4969+FINL0015 DS    0H   Retrieve Subchannel Information Block for desired device number
0000145E  B234 4000                   00000000  4970+         STSCH 0(4)                  Store the SCHIB for first subchannel
00001462  A774 FFDB                   00001418  4971+         $BC   B'0111',FAILDEV       Subchannel does not exist and device number not found
00001466  9101 4005                   00000005  4972+         TM    PMCW1_8,PMCWV         Is the subchannel device number valid?
0000146A  A784 0011                   0000148C  4973+         $BZ   FINN0015              ..No, check the next subchannel
0000146E  D501 4006 3004      00000006  00000004  4974+         CLC   PMCWDNUM,IOCBDEV      Is this the device number being sought?
00001474  A774 000C                   0000148C  4975+         $BNE  FINN0015              ..No, check the next subchannel
                                                 4976+* Subchannel found!
00001478  5010 3000                   00000000  4977+         ST    1,IOCBDID             Remember the subchannel so I/O can be done to it.
0000147C  9680 4005                   00000005  4978+         OI    PMCW1_8,PMCWE         Make sure it is enabled so I/O requests accepted
00001480  B232 4000                   00000000  4979+         MSCH  0(4)                  Enable the subchannel to the channel sub-system
00001484  A784 0010                   000014A4  4980+         $BC   B'1000',ENAOKAY       CC0 (SCHIB updated), device is ready.
00001488  A7F4 FFC8                   00001418  4981+         $B    FAILDEV               CC1,CC2,CC3 (SCHIB update failed), quit
0000148C                                        4982+FINN0015 DS    0H  Advance to next subchannel
0000148C  4110 1001                   00000001  4983+         LA    1,1(0,1)              Advance to next subchannel
00001490  5510 92A0                   000014A0  4984+         CL    1,FINM0015            Beyond maximum subchannel
00001494  A7D4 FFE5                   0000145E  4985+         $BNH  FINL0015              ..No, examine the next subchannel
00001498  A724 FFC0                   00001418  4986+         $BH   FAILDEV               ..Yes, failed to enable the device
0000149C                                        4987+         DROP  4                     Forget SCHIB addressing
0000149C  00010000                              4988+FIND0015 DC    A(X'00010000')        First subchannel subsystem ID
000014A0  0001FFFF                              4989+FINM0015 DC    A(X'0001FFFF')        Last subchannel subsystem ID

000014A4  07FF                                  4991 ENAOKAY  BR    R15                   Return to caller
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    4993 ********************************************************************************
                                                    4994 *         Structure used by RAWIO identifying
                                                    4995 *         the device and operation being performed
                                                    4996 ********************************************************************************


                                                    4998 IOCB_009 IOCB  X'009',CCW=CONPGM
000014A8  00000000                                  4999+IOCB_009 DC    A(0)            +0 Device Identifier (supplied by ENADEV macro)
000014AC  0009                                      5000+         DC    AL2(X'009')     +4 Device address or device number
000014AE  0000                                      5001+         DC    H'0'            +6 Must be zeros
000014B0  D3                                        5002+         DC    AL1(X'D3')      +8 Default detected unit errors
000014B1  3F                                        5003+         DC    AL1(X'3F')      +9 Default detected channel errors
000014B2  0000                                      5004+         DC    HL2'0'          +10 Accumulated unit and channel errors
000014B4  0000                                      5005+         DC    HL2'0'          +12 Tested unit and channel status
000014B6  00                                        5006+         DC    XL1'00'         +14 Accumulated subchannel status control from SCSW
000014B7  80                                        5007+         DC    XL1'80'         +15 Default unsoliticed wait condition
000014B8  00000000                                  5008+         DC    F'0'            +16 I/O status CCW address
000014BC  00000000                                  5009+         DC    F'0'            +20 residual count
000014C0  00001518                                  5010+         DC    A(IORB0016)     +24  Address where ORB is located
000014C4  00000000                                  5011+         DC    A(0)            +28  reserved
000014C8  000014D8                                  5012+         DC    A(IIRB0016)     +32 Address where IRB stored
000014CC  00000000                                  5013+         DC    A(0)            +36 reserved
000014D0  000014D8                                  5014+         DC    A(IIRB0016)     +40 Address where SCHIB stored
000014D4  00000000                                  5015+         DC    A(0)            +44 reserved
000014D8  00000000 00000000                         5016+IIRB0016 DC    16F'0'              Embedded shared IRB and SCHIB area
00001518                                            5018+IORB0016 DS    0XL12
00001518  00000000                                  5019+         DC    A(0)            Word 0 - Interruption Parameter
0000151C  00                                        5020+         DC    AL1((0)*16+B'0000')  Word 1, bits 0-7
0000151D  80                                        5021+         DC    BL1'10000000'   Word 1, bits 8-15
0000151E  FF                                        5022+         DC    AL1(255)        Word 1, bits 16-23
0000151F  00                                        5023+         DC    BL1'00000000'    Word 1, bits 24-31
00001520  000015B0                                  5024+         DC    AL4(CONPGM)     Word 2 - CCW address
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5026 ********************************************************************************
                                                    5027 *        Working Storage
                                                    5028 ********************************************************************************


00001524                                            5030          LTORG ,                  Literals pool
00001524  AABBCCDD                                  5031                =A(REG2PATT)
00001528  00000000                                  5032                =F'0'
0000152C  00050000                                  5033                =A(00+(5*K64))
00001530  00150000                                  5034                =A(MB+(5*K64))
00001534  00003000                                  5035                =A(SEGTABLS)
00001538  00003080                                  5036                =A(PAGETABS)
0000153C  00001000                                  5037                =A(PAGE)
00001540  00005000                                  5038                =A(PFPGBYTS)
00001544  000011A4                                  5039                =A(PFINSADR)
00001548  00000001                                  5040                =F'1'
0000154C  C3D3C340 40                               5041                =CL5'CLC'
00001551  C3D3C3D3 40                               5042                =CL5'CLCL'
00001556  D4E5C3C9 D5                               5043                =CL5'MVCIN'
0000155B  E3D9E340 40                               5044                =CL5'TRT'
00001560  04294967 296C                             5045                =P'4294967296'

                            00000400  00000001  5047 K        EQU   1024             One KB
                            00001000  00000001  5048 PAGE     EQU   (4*K)            Size of one page
                            00010000  00000001  5049 K64      EQU   (64*K)           64 KB
                            00100000  00000001  5050 MB       EQU   (K*K)             1 MB

                            000021FE  00000001  5052 TESTADDR EQU   (2*PAGE+X'200'-2)  Where test/subtest numbers will go
                            000021FD  00000001  5053 TIMEADDR EQU   (TESTADDR-1)       Address of timing tests option flag

                            00200000  00000001  5055 MAINSIZE EQU   (2*MB)                   Minimum required storage size
                            00000020  00000001  5056 NUMPGTBS EQU   ((MAINSIZE+K64-1)/K64)   Number of Page Tables needed
                            00000002  00000001  5057 NUMSEGTB EQU   ((NUMPGTBS*4)/(16*4))    Number of Segment Tables
                            00003000  00000001  5058 SEGTABLS EQU   (3*PAGE)                 Segment Tables Origin
                            00003080  00000001  5059 PAGETABS EQU   (SEGTABLS+(NUMPGTBS*4))  Page Tables Origin
00001568  00B00060                                  5060 CRLREG0  DC    0A(0),XL4'00B00060'      Control Register 0
0000156C  00003002                                  5061 CTLREG1  DC    A(SEGTABLS+NUMSEGTB)     Control Register 1

00001570  00002710                                  5063 NUMLOOPS DC    F'10000'         10,000 * 100 = 1,000,000

00001578  BBBBBBBB BBBBBBBB                         5065 BEGCLOCK DC    0D'0',8X'BB'     Begin
00001580  EEEEEEEE EEEEEEEE                         5066 ENDCLOCK DC    0D'0',8X'EE'     End
00001588  DDDDDDDD DDDDDDDD                         5067 DURATION DC    0D'0',8X'DD'     Diff
00001590  FFFFFFFF FFFFFFFF                         5068 OVERHEAD DC    0D'0',8X'FF'     Overhead

00001598  00000000 0000000C                         5070 TICKSAAA DC    PL8'0'           Clock ticks high part
000015A0  00000000 0000000C                         5071 TICKSBBB DC    PL8'0'           Clock ticks low part
000015A8  00000000 0000000C                         5072 TICKSTOT DC    PL8'0'           Total clock ticks

000015B0  09000044 000015B8                         5074 CONPGM   CCW1  X'09',PRTLINE,0,L'PRTLINE
000015B8  40404040 40404040                         5075 PRTLINE  DC    C'         1,000,000 iterations of XXXXX took 999,999,999 microseconds'
000015FC  40202020 6B202020                         5076 EDIT     DC    X'402020206B2020206B202120'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5078 ************************************************************************
                                                    5079 *        CLC Test Parameters:   A(operand-1),A(operand-2)
                                                    5080 ************************************************************************

00001608  00010000 00110000                         5082 CLC1     DC    A(1*K64),A(MB+(1*K64))                          both equal
00001610  00010000 00110000                         5083 CLC2     DC    A(1*K64),A(MB+(1*K64))                          both equal
00001618  0000FFF4 0010FFDE                         5084 CLCBOTH  DC    A(1*K64-12),A(MB+(1*K64)-34)                    both equal
00001620  00010000 0010FFDE                         5085 CLCOP2   DC    A(1*K64),A(MB+(1*K64)-34)                       both equal

00001628  00020000 00120000                         5087 CLC4     DC    A(2*K64),A(MB+(2*K64))                            op1 HIGH
00001630  00030000 00130000                         5088 CLC8     DC    A(3*K64),A(MB+(3*K64))                            op1 LOW!
00001638  00040000 00140000                         5089 CLC256   DC    A(4*K64),A(MB+(4*K64))                            op1 HIGH
00001640  0004FFF4 00150000                         5090 CLCOP1   DC    A(5*K64-12),A(MB+(5*K64))                         op1 HIGH


                                                    5092 ************************************************************************
                                                    5093 *        MVCIN Test Parameters
                                                    5094 ************************************************************************
                                                    5095          PRINT DATA
00001648  00010000 00110000                         5096 INV1     DC    A(1*K64),A(MB+(1*K64)+1-1),A(1-1),A(MB+(1*K64))
00001650  00000000 00110000
00001658  00020000 00120001                         5097 INV2     DC    A(2*K64),A(MB+(2*K64)+2-1),A(2-1),A(MB+(2*K64))
00001660  00000001 00120000
00001668  00030000 00130003                         5098 INV4     DC    A(3*K64),A(MB+(3*K64)+4-1),A(4-1),A(MB+(3*K64))
00001670  00000003 00130000
00001678  00040000 00140007                         5099 INV8     DC    A(4*K64),A(MB+(4*K64)+8-1),A(8-1),A(MB+(4*K64))
00001680  00000007 00140000
00001688  00050000 001500FF                         5100 INV256   DC    A(5*K64),A(MB+(5*K64)+256-1),A(256-1),A(MB+(5*K64))
00001690  000000FF 00150000

00001698  0005FFF4 001600DD                         5102 INVBOTH  DC    A(6*K64-12),A(MB+(6*K64)-34+256-1),A(256-1),A(MB+(6*K64)-34)
000016A0  000000FF 0015FFDE
000016A8  0006FFF4 001700FF                         5103 INVOP1   DC    A(7*K64-12),A(MB+(7*K64)+256-1),A(256-1),A(MB+(7*K64))
000016B0  000000FF 00170000
000016B8  00080000 001800DD                         5104 INVOP2   DC    A(8*K64),A(MB+(8*K64)-34+256-1),A(256-1),A(MB+(8*K64)-34)
000016C0  000000FF 0017FFDE
                                                    5105          PRINT NODATA
000016C8                                            5106 MVCININ  DC    0XL256'00'
000016C8  00010203 04050607                         5107          DC    XL16'000102030405060708090A0B0C0D0E0F'
000016D8  10111213 14151617                         5108          DC    XL16'101112131415161718191A1B1C1D1E1F'
000016E8  20212223 24252627                         5109          DC    XL16'202122232425262728292A2B2C2D2E2F'
000016F8  30313233 34353637                         5110          DC    XL16'303132333435363738393A3B3C3D3E3F'
                                                    5111          PRINT OFF
                                                    5124          PRINT ON
000017C8                                            5125 MVCINOUT DC    0XL256'00'
000017C8  FFFEFDFC FBFAF9F8                         5126          DC    XL16'FFFEFDFCFBFAF9F8F7F6F5F4F3F2F1F0'
000017D8  EFEEEDEC EBEAE9E8                         5127          DC    XL16'EFEEEDECEBEAE9E8E7E6E5E4E3E2E1E0'
000017E8  DFDEDDDC DBDAD9D8                         5128          DC    XL16'DFDEDDDCDBDAD9D8D7D6D5D4D3D2D1D0'
000017F8  CFCECDCC CBCAC9C8                         5129          DC    XL16'CFCECDCCCBCAC9C8C7C6C5C4C3C2C1C0'
                                                    5130          PRINT OFF
                                                    5143          PRINT ON
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    5145 ********************************************************************************
                                                    5146 *        TRTTEST DSECT
                                                    5147 ********************************************************************************


                                                    5149 TRTTEST  DSECT ,


00000000  00000000                                  5151 OP1DATA  DC    A(0)           Pointer to Operand-1 data
00000004  00000000                                  5152 OP1LEN   DC    F'0'           How much data is there - 1
00000008  00000000                                  5153 OP1WHERE DC    A(0)           Where Operand-1 data should be placed


0000000C  00000000                                  5155 OP2DATA  DC    A(0)           Pointer to Operand-2 data
00000010  00000000                                  5156 OP2LEN   DC    F'0'           How much data is there - 1
00000014  00000000                                  5157 OP2WHERE DC    A(0)           Where Operand-2 data should be placed


00000018  00000000                                  5159 EXLEN    DC    F'0'           Operand-1 test length (EX instruction)
0000001C  00000000                                  5160 FAILMASK DC    A(0)           Failure Branch on Condition mask


00000020  00000000 00000000                         5162 ENDREGS  DC    A(0),XL4'00'   Ending R1/R2 register values


                                                    5164 TRTNEXT  EQU   *              Start of next table entry...


                                                    5166 REG2PATT EQU   X'AABBCCDD'    Register 2 starting/ending CC0 value
                                                    5167 REG2LOW  EQU         X'DD'    (last byte above)


                                                    5169 CLCLetal CSECT ,
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    5171 ************************************************************************
                                                    5172 *        TRT Testing Control tables   (ref: TRTDSECT)
                                                    5173 ************************************************************************
                                                    5174          PRINT DATA
000018C8                                            5175 TRTCTL   DC    0A(0)    start of table




000018C8  00001A0C 00000000                         5177 TRT1     DC    A(TRTOP10),A(001-1),A(00+(1*K64))
000018D0  00010000
000018D4  00001D0C 000000FF                         5178          DC    A(TRTOP20),A(256-1),A(MB+(1*K64))
000018DC  00110000
000018E0  00000000 00000007                         5179          DC               A(001-1),A(7) CC0
000018E8  00000000 AABBCCDD                         5180          DC                        A(0),A(REG2PATT)



000018F0  00001A0C 00000000                         5182 TRT2     DC    A(TRTOP10),A(002-2),A(00+(2*K64))
000018F8  00020000
000018FC  00001D0C 000000FF                         5183          DC    A(TRTOP20),A(256-1),A(MB+(2*K64))
00001904  00120000
00001908  00000001 00000007                         5184          DC               A(002-1),A(7) CC0
00001910  00000000 AABBCCDD                         5185          DC                        A(0),A(REG2PATT)



00001918  00001A0C 00000003                         5187 TRT4     DC    A(TRTOP10),A(004-1),A(00+(3*K64))
00001920  00030000
00001924  00001D0C 000000FF                         5188          DC    A(TRTOP20),A(256-1),A(MB+(3*K64))
0000192C  00130000
00001930  00000003 00000007                         5189          DC               A(004-1),A(7) CC0
00001938  00000000 AABBCCDD                         5190          DC                        A(0),A(REG2PATT)



00001940  00001A0C 00000007                         5192 TRT8     DC    A(TRTOP10),A(008-1),A(00+(4*K64))
00001948  00040000
0000194C  00001D0C 000000FF                         5193          DC    A(TRTOP20),A(256-1),A(MB+(4*K64))
00001954  00140000
00001958  00000007 00000007                         5194          DC               A(008-1),A(7) CC0
00001960  00000000 AABBCCDD                         5195          DC                        A(0),A(REG2PATT)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001968  00001A0C 000000FF                        5197 TRT256   DC    A(TRTOP10),A(256-1),A(00+(5*K64))
00001970  00050000
00001974  00001D0C 000000FF                        5198          DC    A(TRTOP20),A(256-1),A(MB+(5*K64))
0000197C  00150000
00001980  000000FF 00000007                        5199          DC               A(256-1),A(7) CC0
00001988  00000000 AABBCCDD                        5200          DC                    A(0),A(REG2PATT)



00001990  00001B0C 000000FF                        5202 TRTBTH   DC    A(TRTOP111),A(256-1),A(00+(6*K64)-12)  both cross page
00001998  0005FFF4
0000199C  00001E0C 000000FF                        5203          DC    A(TRTOP211),A(256-1),A(MB+(6*K64)-34)  both cross page
000019A4  0015FFDE
000019A8  000000FF 0000000B                        5204          DC                A(256-1),A(11) CC1 = stop, scan incomplete
000019B0  00060005 AABBCC11                        5205          DC                     A(00+(6*K64)-12+X'11'),A(REG2PATT-REG2LOW+X'11')



000019B8  00001C0C 000000FF                        5207 TRTOP1   DC    A(TRTOP1F0),A(256-1),A(00+(7*K64)-12)  only op1 crosses
000019C0  0006FFF4
000019C4  00001F0C 000000FF                        5208          DC    A(TRTOP2F0),A(256-1),A(MB+(7*K64))
000019CC  00170000
000019D0  000000FF 0000000D                        5209          DC                A(256-1),A(13) CC2 = stopped on last byte
000019D8  000700F3 AABBCCF0                        5210          DC                     A(00+(7*K64)-12+255),A(REG2PATT-REG2LOW+X'F0')



000019E0  00001B0C 000000FF                        5212 TRTOP2   DC    A(TRTOP111),A(256-1),A(00+(8*K64))
000019E8  00080000
000019EC  00001E0C 000000FF                        5213          DC    A(TRTOP211),A(256-1),A(MB+(8*K64)-34)  only op2 crosses
000019F4  0017FFDE
000019F8  000000FF 0000000B                        5214          DC                A(256-1),A(11) CC1 = stop, scan incomplete
00001A00  00080011 AABBCC11                        5215          DC                     A(00+(8*K64)+X'11'),A(REG2PATT-REG2LOW+X'11')



00001A08  00000000                                 5217          DC    A(0)     end of table
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   5219 ********************************************************************************
                                                   5220 *        TRT op1 scan data...
                                                   5221 ********************************************************************************

00001A0C  78125634 78125634                        5223 TRTOP10  DC    64XL4'78125634'    (CC0)
00001A14  78125634 78125634
00001A1C  78125634 78125634
00001A24  78125634 78125634
00001A2C  78125634 78125634
00001A34  78125634 78125634
00001A3C  78125634 78125634
00001A44  78125634 78125634
00001A4C  78125634 78125634
00001A54  78125634 78125634
00001A5C  78125634 78125634
00001A64  78125634 78125634
00001A6C  78125634 78125634
00001A74  78125634 78125634
00001A7C  78125634 78125634
00001A84  78125634 78125634
00001A8C  78125634 78125634
00001A94  78125634 78125634
00001A9C  78125634 78125634
00001AA4  78125634 78125634
00001AAC  78125634 78125634
00001AB4  78125634 78125634
00001ABC  78125634 78125634
00001AC4  78125634 78125634
00001ACC  78125634 78125634
00001AD4  78125634 78125634
00001ADC  78125634 78125634
00001AE4  78125634 78125634
00001AEC  78125634 78125634
00001AF4  78125634 78125634
00001AFC  78125634 78125634
00001B04  78125634 78125634

00001B0C  78125634 78125634                        5225 TRTOP111 DC    04XL4'78125634',X'00110000',59XL4'78125634'    (CC1)
00001B14  78125634 78125634
00001B1C  00110000 78125634
00001B24  78125634 78125634
00001B2C  78125634 78125634
00001B34  78125634 78125634
00001B3C  78125634 78125634
00001B44  78125634 78125634
00001B4C  78125634 78125634
00001B54  78125634 78125634
00001B5C  78125634 78125634
00001B64  78125634 78125634
00001B6C  78125634 78125634
00001B74  78125634 78125634
00001B7C  78125634 78125634
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00001B84  78125634 78125634
00001B8C  78125634 78125634
00001B94  78125634 78125634
00001B9C  78125634 78125634
00001BA4  78125634 78125634
00001BAC  78125634 78125634
00001BB4  78125634 78125634
00001BBC  78125634 78125634
00001BC4  78125634 78125634
00001BCC  78125634 78125634
00001BD4  78125634 78125634
00001BDC  78125634 78125634
00001BE4  78125634 78125634
00001BEC  78125634 78125634
00001BF4  78125634 78125634
00001BFC  78125634 78125634
00001C04  78125634 78125634

00001C0C  78125634 78125634                    5227 TRTOP1F0 DC    63XL4'78125634',X'000000F0'    (CC2)
00001C14  78125634 78125634
00001C1C  78125634 78125634
00001C24  78125634 78125634
00001C2C  78125634 78125634
00001C34  78125634 78125634
00001C3C  78125634 78125634
00001C44  78125634 78125634
00001C4C  78125634 78125634
00001C54  78125634 78125634
00001C5C  78125634 78125634
00001C64  78125634 78125634
00001C6C  78125634 78125634
00001C74  78125634 78125634
00001C7C  78125634 78125634
00001C84  78125634 78125634
00001C8C  78125634 78125634
00001C94  78125634 78125634
00001C9C  78125634 78125634
00001CA4  78125634 78125634
00001CAC  78125634 78125634
00001CB4  78125634 78125634
00001CBC  78125634 78125634
00001CC4  78125634 78125634
00001CCC  78125634 78125634
00001CD4  78125634 78125634
00001CDC  78125634 78125634
00001CE4  78125634 78125634
00001CEC  78125634 78125634
00001CF4  78125634 78125634
00001CFC  78125634 78125634
00001D04  78125634 000000F0
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5229 ********************************************************************************
                                                    5230 *        TRT op2 stop tables...
                                                    5231 ********************************************************************************

00001D0C  00000000 00000000                         5233 TRTOP20  DC    256X'00'     no stop
00001D14  00000000 00000000
00001D1C  00000000 00000000
00001D24  00000000 00000000
00001D2C  00000000 00000000
00001D34  00000000 00000000
00001D3C  00000000 00000000
00001D44  00000000 00000000
00001D4C  00000000 00000000
00001D54  00000000 00000000
00001D5C  00000000 00000000
00001D64  00000000 00000000
00001D6C  00000000 00000000
00001D74  00000000 00000000
00001D7C  00000000 00000000
00001D84  00000000 00000000
00001D8C  00000000 00000000
00001D94  00000000 00000000
00001D9C  00000000 00000000
00001DA4  00000000 00000000
00001DAC  00000000 00000000
00001DB4  00000000 00000000
00001DBC  00000000 00000000
00001DC4  00000000 00000000
00001DCC  00000000 00000000
00001DD4  00000000 00000000
00001DDC  00000000 00000000
00001DE4  00000000 00000000
00001DEC  00000000 00000000
00001DF4  00000000 00000000
00001DFC  00000000 00000000
00001E04  00000000 00000000

00001E0C  00000000 00000000                         5235 TRTOP211 DC    17X'00',X'11',238X'00'     stop on X'11'
00001E14  00000000 00000000
00001E1C  00110000 00000000
00001E24  00000000 00000000
00001E2C  00000000 00000000
00001E34  00000000 00000000
00001E3C  00000000 00000000
00001E44  00000000 00000000
00001E4C  00000000 00000000
00001E54  00000000 00000000
00001E5C  00000000 00000000
00001E64  00000000 00000000
00001E6C  00000000 00000000
00001E74  00000000 00000000
00001E7C  00000000 00000000
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00001E84  00000000 00000000
00001E8C  00000000 00000000
00001E94  00000000 00000000
00001E9C  00000000 00000000
00001EA4  00000000 00000000
00001EAC  00000000 00000000
00001EB4  00000000 00000000
00001EBC  00000000 00000000
00001EC4  00000000 00000000
00001ECC  00000000 00000000
00001ED4  00000000 00000000
00001EDC  00000000 00000000
00001EE4  00000000 00000000
00001EEC  00000000 00000000
00001EF4  00000000 00000000
00001EFC  00000000 00000000
00001F04  00000000 00000000

00001F0C  00000000 00000000                    5237 TRTOP2F0 DC    240X'00',X'F0',15X'00'     stop on X'F0'
00001F14  00000000 00000000
00001F1C  00000000 00000000
00001F24  00000000 00000000
00001F2C  00000000 00000000
00001F34  00000000 00000000
00001F3C  00000000 00000000
00001F44  00000000 00000000
00001F4C  00000000 00000000
00001F54  00000000 00000000
00001F5C  00000000 00000000
00001F64  00000000 00000000
00001F6C  00000000 00000000
00001F74  00000000 00000000
00001F7C  00000000 00000000
00001F84  00000000 00000000
00001F8C  00000000 00000000
00001F94  00000000 00000000
00001F9C  00000000 00000000
00001FA4  00000000 00000000
00001FAC  00000000 00000000
00001FB4  00000000 00000000
00001FBC  00000000 00000000
00001FC4  00000000 00000000
00001FCC  00000000 00000000
00001FD4  00000000 00000000
00001FDC  00000000 00000000
00001FE4  00000000 00000000
00001FEC  00000000 00000000
00001FF4  00000000 00000000
00001FFC  F0000000 00000000
00002004  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   5239 ************************************************************************
                                                   5240 *        CLCL Test Parameters
                                                   5241 ************************************************************************

0000200C  00060000 00000001                        5243 CLCL1    DC    A(6*K64),A(1),A(MB+(6*K64)),A(1)             both equal
00002014  00160000 00000001

0000201C  00060000 00000002                        5245 CLCL2    DC    A(6*K64),A(2),A(MB+(6*K64)),A(2)             both equal
00002024  00160000 00000002

0000202C  00060000 00000100                        5247 CLCL256  DC    A(6*K64),A(256),A(MB+(6*K64)),A(256)         both equal
00002034  00160000 00000100

0000203C  00060000 00000400                        5249 CLCL1K   DC    A(6*K64),A(K),A(MB+(6*K64)),A(K)             both equal
00002044  00160000 00000400

0000204C  0005FFF4 00010000                        5251 CLCLBOTH DC    A(6*K64-12),A(K64),A(MB+(6*K64)-34),A(K64)   both equal
00002054  0015FFDE 00010000

0000205C  00060000 00001000                        5253 CLCLOP2  DC    A(6*K64),A(PAGE),A(MB+(6*K64)-34),A(K64)     both equal
00002064  0015FFDE 00010000

0000206C  00070000 00000004                        5255 CLCL4    DC    A(7*K64),A(4),A(MB+(7*K64)),A(4)              op1 HIGH
00002074  00170000 00000004

0000207C  00080000 00000008                        5257 CLCL8    DC    A(8*K64),A(8),A(MB+(8*K64)),A(8)              op1 LOW!
00002084  00180000 00000008

0000208C  0008FFF4 00010000                        5259 CLCLOP1  DC    A(9*K64-12),A(K64),A(MB+(9*K64)),A(PAGE)      op1 HIGH
00002094  00190000 00001000

0000209C  000A0000 00010000                        5261 CLCLPF   DC    A(10*K64),A(K64),A(MB+(10*K64)),A(K64)      page fault
000020A4  001A0000 00010000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5263 ************************************************************************
                                                    5264 *        CLCL Expected Ending Register Values
                                                    5265 ************************************************************************

000020AC  00060001 00000000                         5267 ECLCL1   DC    A(6*K64+1),A(0),A(MB+(6*K64)+1),A(0)         both equal
000020B4  00160001 00000000

000020BC  00060002 00000000                         5269 ECLCL2   DC    A(6*K64+2),A(0),A(MB+(6*K64)+2),A(0)         both equal
000020C4  00160002 00000000

000020CC  00060100 00000000                         5271 ECLCL256 DC    A(6*K64+256),A(0),A(MB+(6*K64)+256),A(0)     both equal
000020D4  00160100 00000000

000020DC  00060400 00000000                         5273 ECLCL1K  DC    A(6*K64+K),A(0),A(MB+(6*K64)+K),A(0)         both equal
000020E4  00160400 00000000

000020EC  0006FFF4 00000000                         5275 ECLCLBTH DC    A(6*K64-12+K64),A(0),A(MB+(6*K64)-34+K64),A(0) bth equl
000020F4  0016FFDE 00000000

000020FC  00061000 00000000                         5277 ECLCLOP2 DC    A(6*K64+PAGE),A(0),A(MB+(6*K64)-34+K64),A(0) both equal
00002104  0016FFDE 00000000

0000210C  00070003 00000001                         5279 ECLCL4   DC    A(7*K64+4-1),A(1),A(MB+(7*K64)+4-1),A(1)       op1 HIGH
00002114  00170003 00000001

0000211C  00080007 00000001                         5281 ECLCL8   DC    A(8*K64+8-1),A(1),A(MB+(8*K64)+8-1),A(1)       op1 LOW!
00002124  00180007 00000001

0000212C  0009FFF3 00000001                         5283 ECLCLOP1 DC    A(9*K64-12+K64-1),A(1),A(MB+(9*K64)+PAGE),A(0) op1 HIGH
00002134  00191000 00000000

0000213C  000B0000 00000000                         5285 ECLCLPF  DC    A(10*K64+K64),A(0),A(MB+(10*K64)+K64),A(0)   page fault
00002144  001B0000 00000000

0000214C  00000000 00000000                         5287 CLCLEND  DC    4F'0'          (actual ending register values)
00002154  00000000 00000000
                            00000005  00000001    5288 PFPAGE   EQU   5              (page the Page Fault should occur on)
                            00005000  00000001    5289 PFPGBYTS EQU   (PFPAGE*PAGE)  (number of bytes into operand-1)
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                     5291 ********************************************************************************
                                                     5292 *        Fixed storage locations
                                                     5293 ********************************************************************************


0000215C                      0000215C  000021FD   5295          ORG   CLCLetal+TIMEADDR      (s/b @ X'21FD')

000021FD  00                                       5297 TIMEOPT  DC    X'00'      Set to non-zero to run timing tests




000021FE                      000021FE  000021FE   5299          ORG   CLCLetal+TESTADDR      (s/b @ X'21FE', X'21FF')

000021FE  00                                       5301 TESTNUM  DC    X'00'      Test number of active test
000021FF  00                                       5302 SUBTEST  DC    X'00'      Active test sub-test number


00002200                      00002200  00003000   5304          ORG   CLCLetal+SEGTABLS      (s/b @ X'3000')
00003000  00                                       5306 DATTABS  DC    X'00'      Segment and Page Tables will go here...
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5308 ********************************************************************************
                                                    5309 *        IOCB DSECT
                                                    5310 ********************************************************************************

                                                    5312          DSECTS NAME=IOCB
                                                    5314+IOCB     DSECT
                                                    5315+*     Field usage by: CH SC Description (R->program read-only, X->program read/write)
00000000                                            5316+IOCBDID  DS    0F  +0     R  Device Identifier - Subsystem ID for channel subsystem
00000000  0000                                      5317+         DS    H   +0  R      reserved - must be zeros
00000002  0000                                      5318+IOCBDV   DS    H   +2  R      Channel Unit Device address of I/O operation
00000004  0000                                      5319+IOCBDEV  DS    H   +4  X  X   Device address or device number (R after ENADEV)
00000006  0000                                      5320+IOCBZERO DS    H   +6  R  R   Must be zeros
00000008  00                                        5321+IOCBUM   DS    X   +8  X  X   Unit status test mask
00000009  00                                        5322+IOCBCM   DS    X   +9  X  X   Channel status test mask
0000000A                                            5323+IOCBST   DS    0H  +10 X  X   Input/Output unit and channel status accumulation
0000000A  00                                        5324+IOCBUS   DS    X   +10 R  R   Accumulated unit status
0000000B  00                                        5325+IOCBCS   DS    X   +11 R  R   Accumulated channel status
0000000C  00                                        5326+IOCBUT   DS    X   +14 R  R   Used to test unit status
0000000D  00                                        5327+IOCBCT   DS    X   +13 R  R   Used to test channel status
0000000E  00                                        5328+IOCBSC   DS    X   +14    R   Accumulted subchanel status control
0000000F  00                                        5329+IOCBWAIT DS    X   +15 X  X   Recognized unsolicited interruption unit status events
00000010  00000000                                  5330+IOCBSCCW DS    A   +16 R  R   I/O status CCW address
00000014                                            5331+IOCBSCNT DS    0F  +20 R  R   I/O status residual count as a positive full word
00000014  0000                                      5332+         DS    H   +20 R      reserved must be zeros
00000016  0000                                      5333+IOCBRCNT DS    H   +22 R      I/O status residual count as an unsigned halfword
00000018                                            5334+IOCBCAW  DS    0A  +24 X      Channel Address word
00000018  00000000 00000000                         5335+IOCBORB  DS    AD  +24    X   Address of the ORB for channel subsystem I/O
00000020  00000000 00000000                         5336+IOCBIRB  DS    AD  +32    X   Channel subsystem IRB address
00000028  00000000 00000000                         5337+IOCBSIB  DS    AD  +40    X   Channel subsystem SCHIB address
                            00000030  00000001      5338+IOCBL    EQU   *-IOCB  Length of IOCB control block (48) without embedded structures
```

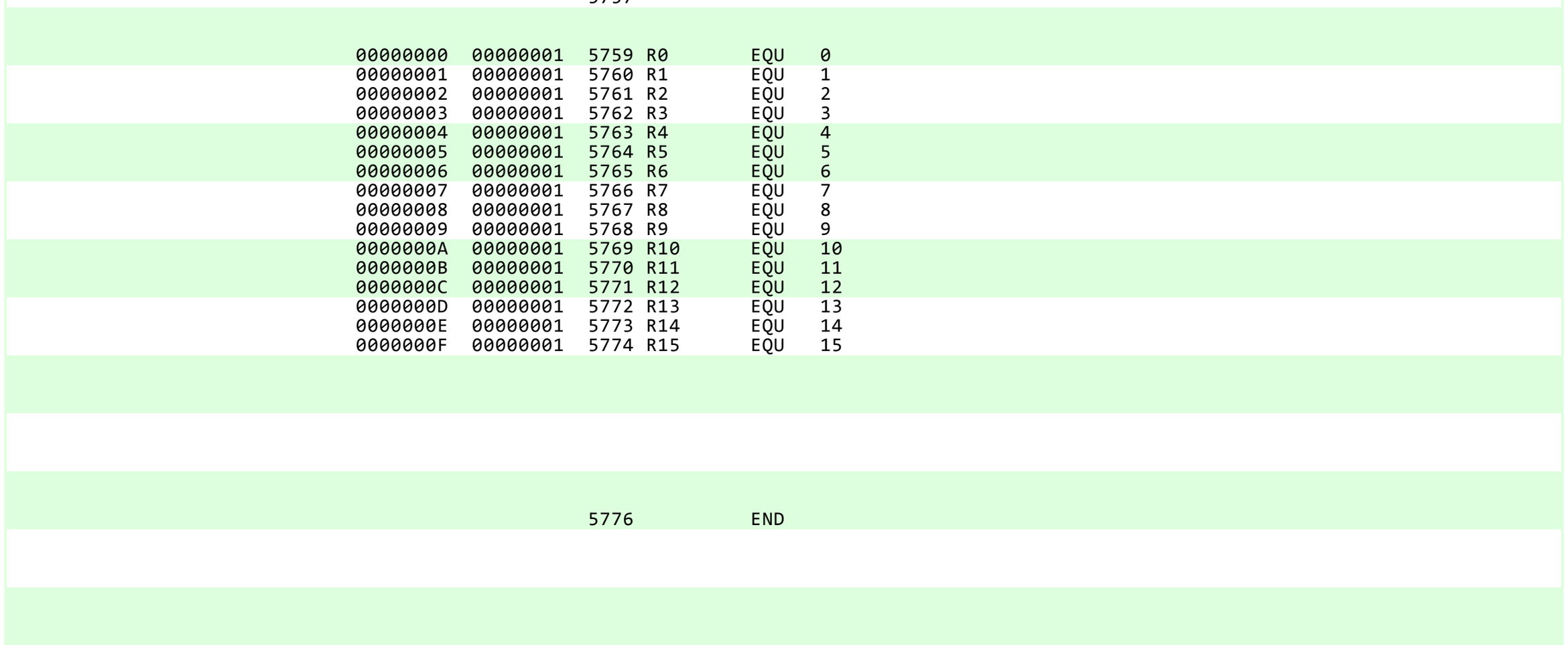
```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  5340 ********************************************************************************
                                                  5341 *        ORB DSECT
                                                  5342 ********************************************************************************

                                                  5344          DSECTS NAME=ORB
                                                  5346+ORB      DSECT
00000000  00000000                                5347+ORBPARM  DC    F'0'     Word 0, bits 0-31

00000004  00                                      5349+ORB1_0   DC    X'00'    Word 1, bits 0-7
                            000000F0  00000001    5350+ORBKEYM  EQU   X'F0'    Word 1, bits 0-3   - Storage Key Mask
                            00000008  00000001    5351+ORBS     EQU   X'08'    Word 1, bit 4      - Suspend Control
                            00000004  00000001    5352+ORBC     EQU   X'04'    Word 1, bit 5      - Streaming Mode Control
                            00000002  00000001    5353+ORBM     EQU   X'02'    Word 1, bit 6      - Modification Control
                            00000001  00000001    5354+ORBY     EQU   X'01'    Word 1, bit 7      - Synchronization Control

00000005  00                                      5356+ORB1_8   DC    X'00'    Word 1, bits 8-15
                            00000080  00000001    5357+ORBF     EQU   X'80'    Word 1, bit 8      - CCW Format-Control
                            00000040  00000001    5358+ORBP     EQU   X'40'    Word 1, bit 9      - Pre-fetch control
                            00000020  00000001    5359+ORBI     EQU   X'20'    Word 1, bit 10     - Initial-status Interruption Control
                            00000010  00000001    5360+ORBA     EQU   X'10'    Word 1, bit 11     - Address Limit Checking Control
                            00000008  00000001    5361+ORBU     EQU   X'08'    Word 1, bit 12     - Suppress-suspended-interruption control
                            00000004  00000001    5362+ORBB     EQU   X'04'    Word 1, bit 13     - Channel-Program-Type Control
                            00000002  00000001    5363+ORBH     EQU   X'02'    Word 1, bit 14     - Format 2-IDAW Control
                            00000001  00000001    5364+ORBT     EQU   X'01'    Word 1, bit 15     - 2K-IDAW control
00000006  00                                      5365+ORBLPM   DC    X'00'    Word 1, bits 16-23 - Logical Path Mask
00000007  00                                      5366+ORRB1_24 DC    X'00'    Word 1, bits 24-31
                            00000080  00000001    5367+ORBL     EQU   X'80'    Word 1, bit 24     - Incorrect Length Suppression Mode
                            0000007F  00000001    5368+ORBRSV3  EQU   X'7F'    Word 1, bits 25-31 - reserved must be zeros
                            00000040  00000001    5369+ORBD     EQU   X'40'    Word 1, bit 25     - MIDAW Addressing Control
                            0000003E  00000001    5370+ORBRSV26 EQU   X'3E'    Word 1, bits 26-30 - reserved must be zeros
                            0000007E  00000001    5371+ORBRSV25 EQU   X'7E'    Word 1, bits 25-30 - reserved must be zeros
                            00000001  00000001    5372+ORBX     EQU   X'01'    Word 1, bit 31     - ORB-extension control

00000008  00000000                                5374+ORBCCW   DC    A(0)     Word 2, bits 1-31  - Channel Program Address
                            00000080  00000001    5375+ORBRSV4  EQU   X'80'    Word 2, bit 0      - reserved must be zero
                            0000000C  00000001    5376+ORBLEN   EQU   *-ORB Length of standard ORB
                                                  5377+* Extended ORB fields
0000000C  00                                      5378+ORBCSS   DC    X'00'    Word 3, bits 0-7   - Channel Subsystem Priority
0000000D  00                                      5379+ORBRSV5  DC    X'00'    Word 3, bits 8-15  - reserved must be zeros
0000000E                                          5380+ORBPGM   DC    0X'00'   Word 3, bits 16-23 - Transport mode reserves for program us
0000000E  00                                      5381+ORBCU    DC    X'00'    Word 3, bits 16-23 - Control Unit Priority
0000000F  00                                      5382+ORBRSV6  DC    X'00'    Word 3, bits 24-31 - reserved must be zeros
00000010  00000000 00000000                       5383+ORBRSV7  DC    XL16'00' Words 4-7          - reserved must be zeros
00000018  00000000 00000000
                            00000020  00000001    5384+ORBXLEN  EQU   *-ORB Length of extended ORB
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  5387 ********************************************************************************
                                                  5388 *        IRB DSECT
                                                  5389 ********************************************************************************

                                                  5391          DSECTS NAME=IRB
                                                  5393+IRB      DSECT Interruption          Response Block
00000000  00000000 00000000                       5394+IRBSCSW  DC    XL12'00' Words 0-2 - Subchannel Status Word (Defined by DSECT SCSW)
00000008  00000000
0000000C  00000000 00000000                       5395+IRBESW   DC    XL20'00' Words 3-7 - Extended Status Word
00000014  00000000 00000000
0000001C  00000000
00000020  00000000 00000000                       5396+IRBECW   DC    XL32'00' Words 8-15 - Extended Control Word
00000028  00000000 00000000
00000030  00000000 00000000
00000038  00000000 00000000
                             00000040  00000001  5397+IRBL     EQU   *-IRB    IRB Length
00000040  00000000 00000000                       5398+IRBEMW   DC    XL32'00' Words 16-23 - Extended Measurement Word
00000048  00000000 00000000
00000050  00000000 00000000
00000058  00000000 00000000
                             00000060  00000001  5399+IRBXL    EQU   *-IRB    Extended IRB Length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5402 ********************************************************************************
                                                    5403 *        SCSW DSECT
                                                    5404 ********************************************************************************

                                                    5406          DSECTS NAME=SCSW
                                                    5408+SCSW     DSECT Subchannel          Status Word
00000000  00                                        5409+SCSWFLAG DC    X'00'    Flags
                                00000F0  00000001   5410+SCSWKEYM EQU   X'F0'    Storage Key Mask of subchannel storage key
                                00000008 00000001   5411+SCSWSUSC EQU   X'08'    Suspend Control
                                00000004 00000001   5412+SCSWESWF EQU   X'04'    Extended Status Word Format
                                00000003 00000001   5413+SCSWDCCM EQU   X'03'    Deferred condiont code mask
                                00000000 00000001   5414+SCSWDCC0 EQU   X'00'    Normal I/O interruption
                                00000001 00000001   5415+SCSWDCC1 EQU   X'01'    Deferred condition code is 1
                                00000003 00000001   5416+SCSWDCC3 EQU   X'03'    Deferred condition code is 3

00000001  00                                        5418+SCSWCTLS DC    X'00'    General Controls
                                00000080 00000001   5419+SCSWCCWF EQU   X'80'    CCW Format control when ...
                                00000040 00000001   5420+SCSWCCWP EQU   X'40'    CCW Prefetch Control
                                00000020 00000001   5421+SCSWISIC EQU   X'20'    Initial-Status-Interruption Control
                                00000010 00000001   5422+SCSWALKC EQU   X'10'    Address-Limit-Checking Control
                                00000008 00000001   5423+SCSWSSIC EQU   X'08'    Suppress suspended interruption
                                00000004 00000001   5424+SCSW0CC  EQU   X'04'    Zero-Condition Code
                                00000002 00000001   5425+SCSWECWC EQU   X'02'    Extended Control Word control
                                00000001 00000001   5426+SCSWPNOP EQU   X'01'    Path Not Operational

00000002  00                                        5428+SCSW1    DC    X'00'    Control Byte 1
                                00000070 00000001   5429+SCSWFM   EQU   X'70'    Functional Control Mask
                                00000040 00000001   5430+SCSWFS   EQU   X'40'    Function Control - Start Function
                                00000020 00000001   5431+SCSWFH   EQU   X'20'    Function Control - Halt Function
                                00000010 00000001   5432+SCSWFC   EQU   X'10'    Function Control - Clear Function
                                00000008 00000001   5433+SCSWARP  EQU   X'08'    Activity Control - Resume pending
                                00000004 00000001   5434+SCSWASP  EQU   X'04'    Activity Control - Start pending
                                00000002 00000001   5435+SCSWAHP  EQU   X'02'    Activity Control - Halt pending
                                00000001 00000001   5436+SCSWACP  EQU   X'01'    Activity Control - Clear pending
00000003  00                                        5437+SCSW2    DC    X'00'    Control Byte 2
                                00000080 00000001   5438+SCSWASA  EQU   X'80'    Activity Control - Subchannel Active
                                00000040 00000001   5439+SCSWADA  EQU   X'40'    Activity Control - Device Active
                                00000020 00000001   5440+SCSWASUS EQU   X'20'    Activity Control - Suspended
                                00000010 00000001   5441+SCSWSAS  EQU   X'10'    Status Control   - Alert Status
                                00000008 00000001   5442+SCSWSINT EQU   X'08'    Status Control   - Intermediate Status
                                00000004 00000001   5443+SCSWSPRI EQU   X'04'    Status Control   - Primary Status
                                00000002 00000001   5444+SCSWSSEC EQU   X'02'    Status Control   - Secondary Status
                                00000001 00000001   5445+SCSWSPEN EQU   X'01'    Status Control   - Status Pending

00000004  00000000                                  5447+SCSWCCW  DC    A(0)     CCW Address

00000008  00                                        5449+SCSWUS   DC    X'00'    Unit Status
                                00000080 00000001   5450+SCSWATTN EQU   X'80'    Attention
                                00000040 00000001   5451+SCSWSM   EQU   X'40'    Status modifier
                                00000020 00000001   5452+SCSWCUE  EQU   X'20'    Control-unit end
                                00000010 00000001   5453+SCSWBUSY EQU   X'10'    Busy
                                00000008 00000001   5454+SCSWCE   EQU   X'08'    Channel end
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                               00000004  00000001  5455+SCSWDE   EQU   X'04'    Device end
                               00000002  00000001  5456+SCSWUC   EQU   X'02'    Unit check
                               00000001  00000001  5457+SCSWUX   EQU   X'01'    Unit exception

00000009  00                                       5459+SCSWCS   DC    X'00'    Channel Status
                               00000080  00000001  5460+SCSWPCI  EQU   X'80'    Program-controlled interruption
                               00000040  00000001  5461+SCSWIL   EQU   X'40'    Incorrect length
                               00000020  00000001  5462+SCSWPRGM EQU   X'20'    Program check
                               00000010  00000001  5463+SCSWPROT EQU   X'10'    Protection Check
                               00000008  00000001  5464+SCSWCDAT EQU   X'08'    Channel-data check
                               00000004  00000001  5465+SCSWCCTL EQU   X'04'    Channel-control check
                               00000002  00000001  5466+SCSWICTL EQU   X'02'    Interface-control check
                               00000001  00000001  5467+SCSWCHNG EQU   X'01'    Chaining check

0000000A  0000                                     5469+SCSWCNT  DC    H'0'     Residual CCW count
                               0000000C  00000001  5470+SCSWL    EQU   *-SCSW
```

```
  LOC         OBJECT CODE        ADDR1     ADDR2     STMT

                                                     5473 ********************************************************************************
                                                     5474 *        (other DSECTS needed by SATK)
                                                     5475 ********************************************************************************

                                                     5477          DSECTS PRINT=OFF,NAME=(ASA,SCHIB,CCW0,CCW1,CSW)
```



```
                                                     5753          PRINT ON

                                                     5755 ********************************************************************************
                                                     5756 *        Register equates
                                                     5757 ********************************************************************************

                             00000000  00000001  5759 R0        EQU   0
                             00000001  00000001  5760 R1        EQU   1
                             00000002  00000001  5761 R2        EQU   2
                             00000003  00000001  5762 R3        EQU   3
                             00000004  00000001  5763 R4        EQU   4
                             00000005  00000001  5764 R5        EQU   5
                             00000006  00000001  5765 R6        EQU   6
                             00000007  00000001  5766 R7        EQU   7
                             00000008  00000001  5767 R8        EQU   8
                             00000009  00000001  5768 R9        EQU   9
                             0000000A  00000001  5769 R10       EQU   10
                             0000000B  00000001  5770 R11       EQU   11
                             0000000C  00000001  5771 R12       EQU   12
                             0000000D  00000001  5772 R13       EQU   13
                             0000000E  00000001  5773 R14       EQU   14
                             0000000F  00000001  5774 R15       EQU   15
```



```
                                                     5776          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
ASA	4	00000000	512	5481	3537
ASBEGIN	U	00000000	1	5482	5487 5529 5565 5574 5592 5599 5605 5609 5613 5619 5636
ASEND	U	00000200	1	5635	5636
ASLENGTH	U	00000200	1	5636	
BCEXTCOD	H	0000001A	2	5499	
BCIOCOD	H	0000003A	2	5507	
BCMCKCOD	H	00000032	2	5505	
BCPGMCOD	H	0000002A	2	5503	
BCSVCCOD	H	00000022	2	5501	
BEGCLOCK	D	00001578	8	5065	3887 3898 4033 4146 4371 4383 4508 4522 4842 4845 4852
BEGDATON	I	00001198	4	4690	4697
BEGIN	I	00000200	2	3543	3512 3538 3539 3803 3872
CALCDUR	I	0000132C	4	4839	3891 4140 4375 4512 4767
CALCRET	F	00001370	4	4861	4839 4858
CALCWORK	F	00001374	4	4862	4840 4857
CAW	F	00000048	4	5511	
CAWADDR	R	00000049	3	5514	
CAWKEY	X	00000048	1	5512	
CAWSUSP	U	00000008	1	5513	
CCW0	4	00000000	8	5640	5646
CCW0ADDR	R	00000001	3	5642	
CCW0CNT	H	00000006	2	5645	
CCW0CODE	X	00000000	1	5641	
CCW0FLGS	X	00000004	1	5643	
CCW0L	U	00000008	1	5646	
CCW1	4	00000000	8	5658	5663
CCW1ADDR	A	00000004	4	5662	
CCW1CNT	H	00000002	2	5661	
CCW1CODE	X	00000000	1	5659	
CCW1FLGS	X	00000001	1	5660	
CCW1L	U	00000008	1	5663	
CCWCC	U	00000040	1	5650	
CCWCD	U	00000080	1	5649	
CCWIDA	U	00000004	1	5654	
CCWPCI	U	00000008	1	5653	
CCWSKIP	U	00000010	1	5652	
CCWSLI	U	00000020	1	5651	
CCWSUSP	U	00000002	1	5655	
CHANID	F	000000A8	4	5566	
CLC1	A	00001608	4	5082	3588
CLC2	A	00001610	4	5083	3595
CLC256	A	00001638	4	5089	3578 3617
CLC4	A	00001628	4	5087	3576 3602
CLC8	A	00001630	4	5088	3582 3609
CLCBOTH	A	00001618	4	5084	3624
CLCL1	A	0000200C	4	5243	3670
CLCL1K	A	0000203C	4	5249	3709
CLCL2	A	0000201C	4	5245	3679
CLCL256	A	0000202C	4	5247	3897 4035 4036 4037 4040 4041 4042 4043 4044 4045 4046 4047 4048 4049 4050 4051 4052 4053 4054 4055 4056 4057 4058 4059 4060 4061 4062 4063 4064 4065 4066 4067 4068 4069 4070 4071 4072 4073 4074 4075 4076 4077 4078 4079 4080 4081 4082 4083 4084 4085 4086 4087

```
     SYMBOL         TYPE    VALUE      LENGTH    DEFN  REFERENCES

                                                      4088  4089  4090  4091  4092  4093  4094  4095  4096  4097  4098  4099  4100
                                                      4101  4102  4103  4104  4105  4106  4107  4108  4109  4110  4111  4112  4113
                                                      4114  4115  4116  4117  4118  4119  4120  4121  4122  4123  4124  4125  4126
                                                      4127  4128  4129  4130  4131  4132  4133  4134  4136  4137  4148  4150  4152
                                                      4156  4158  4160  4162  4164  4166  4168  4170  4172  4174  4176  4178  4180
                                                      4182  4184  4186  4188  4190  4192  4194  4196  4198  4200  4202  4204  4206
                                                      4208  4210  4212  4214  4216  4218  4220  4222  4224  4226  4228  4230  4232
                                                      4234  4236  4238  4240  4242  4244  4246  4248  4250  4252  4254  4256  4258
                                                      4260  4262  4264  4266  4268  4270  4272  4274  4276  4278  4280  4282  4284
                                                      4286  4288  4290  4292  4294  4296  4298  4300  4302  4304  4306  4308  4310
                                                      4312  4314  4316  4318  4320  4322  4324  4326  4328  4330  4332  4334  4336
                                                      4338  4340  4342  4344  4347  4349
CLCL4                A     0000206C           4  5255  3652  3689
CLCL8                A     0000207C           4  5257  3662  3700
CLCLBOTH             A     0000204C           4  5251  3718
CLCLEND              F     0000214C           4  5287  4902  4903
CLCLETAL             J     00000000       12289  3494  3497  3504  3511  3513  5295  5299  5304
CLCLOP1              A     0000208C           4  5259  3657  3728
CLCLOP2              A     0000205C           4  5253  3737
CLCLPF               A     0000209C           4  5261  4664  4733  4735  4741  4743
CLCOP1               A     00001640           4  5090  3580  3631
CLCOP2               A     00001620           4  5085  3638
CODE                 2     00000000       12289  3494
CONPGM               W     000015B0           8  5074  5024
CPUID                U     0000031B           1  5638
CRLREG0              A     00001568           4  5060  4687
CSW                  F     00000040           8  5510
CSWATTN              U     00000080           1  5680
CSWBUSY              U     00000010           1  5683
CSWCCTL              U     00000004           1  5695
CSWCCW               R     00000001           3  5677
CSWCDAT              U     00000008           1  5694
CSWCE                U     00000008           1  5684  4826
CSWCHNG              U     00000001           1  5697
CSWCNT               H     00000006           2  5699
CSWCS                X     00000005           1  5689
CSWCUE               U     00000020           1  5682
CSWDCC0              U     00000000           1  5673
CSWDCC1              U     00000001           1  5674
CSWDCC3              U     00000003           1  5675
CSWDCCM              U     00000003           1  5672
CSWDE                U     00000004           1  5685  4826
CSWFLAG              X     00000000           1  5667
CSWFMT               4     00000000           8  5666  5700
CSWFMTL              U     00000008           1  5700
CSWICTL              U     00000002           1  5696
CSWIL                U     00000040           1  5691
CSWKEYM              U     000000F0           1  5668
CSWLOG               U     00000004           1  5671
CSWPCI               U     00000080           1  5690
CSWPRGM              U     00000020           1  5692
CSWPROT              U     00000010           1  5693
```

```
     SYMBOL         TYPE    VALUE      LENGTH    DEFN  REFERENCES

CSWSM                U    00000040          1  5681
CSWSUSP              U    00000008          1  5670
CSWUC                U    00000002          1  5686
CSWUS                X    00000004          1  5679
CSWUX                U    00000001          1  5687
CTLREG1              A    0000156C          4  5061  4688
DATONPSW             X    000011B8          4  4697  4689
DATTABS              X    00003000          1  5306
DURATION             D    00001588          8  5067  3892  4141  4376  4513  4770  4771  4774  4854
DWAT0010             3    00001410          8  4932  4931
DWAT0011             3    00001420          8  4937  4936
DWAT0012             3    00001430          8  4942  4941
DWAT0013             3    00001440          8  4947  4946
ECLCL1               A    000020AC          4  5267  3673
ECLCL1K              A    000020DC          4  5273  3712
ECLCL2               A    000020BC          4  5269  3682
ECLCL256             A    000020CC          4  5271
ECLCL4               A    0000210C          4  5279  3692
ECLCL8               A    0000211C          4  5281  3703
ECLCLBTH             A    000020EC          4  5275  3721
ECLCLOP1             A    0000212C          4  5283  3731
ECLCLOP2             A    000020FC          4  5277  3740
ECLCLPF              A    0000213C          4  5285  4747
EDIT                 X    000015FC         12  5076  4784  4785
ENADEV               I    00001456          4  4966  4894
ENAOKAY              I    000014A4          2  4991  4980
ENDCLCL              I    000013CA          4  4902  3674  3683  3693  3704  3713  3722  3732  3741
ENDCLOCK             D    00001580          8  5066  3890  4014  4139  4352  4374  4489  4511  4628  4847  4850  4853
ENDREGS              A    00000020          4  5162  3841
EOJ                  H    00001408          2  4930  3566
EXLEN                F    00000018          4  5159  3831
EXTCPUAD             H    00000084          2  5531
EXTICODE             H    00000086          2  5532
EXTIPARM             F    00000080          4  5530
EXTNPSW              F    00000058          8  5520
EXTOPSW              F    00000018          8  5492  5498
FAILDEV              H    00001418          2  4935  4971  4981  4986
FAILIO               H    00001428          2  4940  4794  4817  4827
FAILMASK             A    0000001C          4  5160  3832
FAILTEST             H    00001438          2  4945  3590  3597  3604  3611  3619  3626  3633  3640  3672  3681  3691  3702  3711
                                                  3720  3730  3739  3856  4708  4714  4727  4734  4736  4740  4742  4744  4748
                                                  4752  4758  4904  4917
FIND0015             A    0000149C          4  4988  4966
FINL0015             H    0000145E          2  4969  4985
FINM0015             A    000014A0          4  4989  4984
FINN0015             H    0000148C          2  4982  4973  4975
IIRB0016             F    000014D8          4  5016  5012  5014
IMAGE                1    00000000      12289     0
INIT                 H    000013B8          2  4888  3550
INV1                 A    00001648          4  5096  3753
INV2                 A    00001658          4  5097  3758
INV256               A    00001688          4  5100  3773  4380
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
INV4	A	00001668	4	5098	3763
INV8	A	00001678	4	5099	3768
INVBOTH	A	00001698	4	5102	3778
INVOP1	A	000016A8	4	5103	3783
INVOP2	A	000016B8	4	5104	3788
IOCB	4	00000000	48	5314	5338 3540
IOCBCAW	A	00000018	4	5334	
IOCBCM	X	00000009	1	5322	
IOCBCS	X	0000000B	1	5325	
IOCBCT	X	0000000D	1	5327	
IOCBDEV	H	00000004	2	5319	4974
IOCBDID	F	00000000	4	5316	4790 4977
IOCBDV	H	00000002	2	5318	
IOCBIRB	A	00000020	8	5336	4795
IOCBL	U	00000030	1	5338	
IOCBORB	A	00000018	8	5335	4792 4891
IOCBRCNT	H	00000016	2	5333	4824
IOCBSC	X	0000000E	1	5328	4788 4819 4821
IOCBSCCW	A	00000010	4	5330	4823
IOCBSCNT	F	00000014	4	5331	
IOCBSIB	A	00000028	8	5337	4967
IOCBST	H	0000000A	2	5323	4789 4820
IOCBUM	X	00000008	1	5321	
IOCBUS	X	0000000A	1	5324	4826
IOCBUT	X	0000000C	1	5326	
IOCBWAIT	X	0000000F	1	5329	
IOCBZERO	H	00000006	2	5320	4789
IOCB_009	A	000014A8	4	4999	4890
IOELADDR	F	000000AC	4	5567	
IOICODE	H	000000BA	2	5572	
IOIID	F	000000C0	4	5577	
IOINIT	I	00001448	4	4954	4893
IOIPARM	F	000000BC	4	5576	
IOMK0014	F	00001450	4	4956	4954 4955
ION0008	3	000012D0	8	4805	4802
IONPSW	F	00000078	8	5524	
IOOPSW	F	00000038	8	5496	5506
IORB0016	X	00001518	12	5018	5010
IOS0008	X	000012D8	8	4806	4801 4809
IOSSID	F	000000B8	4	5575	4812
IOWT0007	H	000012B6	2	4799	4813 4816 4822
IPLCCW1	F	00000008	8	5484	
IPLCCW2	F	00000010	8	5485	
IPLPSW	F	00000000	8	5483	
IRB	4	00000000	96	5393	5397 5399 4796
IRBECW	X	00000020	32	5396	
IRBEMW	X	00000040	32	5398	
IRBESW	X	0000000C	20	5395	
IRBL	U	00000040	1	5397	
IRBSCSW	X	00000000	12	5394	4819 4820 4823 4824
IRBXL	U	00000060	1	5399	
IRST0008	H	000012E0	2	4808	4805

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
K	U	00000400	1	5047	5048 5049 5050 5249 5273
K64	U	00010000	1	5049	5056 4517 4519 5082 5083 5084 5085 5087 5088 5089 5090 5096 5097
					5098 5099 5100 5102 5103 5104 5177 5178 5182 5183 5187 5188 5192
					5193 5197 5198 5202 5203 5205 5207 5208 5210 5212 5213 5215 5243
					5245 5247 5249 5251 5253 5255 5257 5259 5261 5267 5269 5271 5273
					5275 5277 5279 5281 5283 5285
LCHANLOG	F	000000B0	4	5568	
LOGICERR	D	000011A8	8	4695	
MAINSIZE	U	00200000	1	5055	5056
MB	U	00100000	1	5050	5055 4519 5082 5083 5084 5085 5087 5088 5089 5090 5096 5097 5098
					5099 5100 5102 5103 5104 5178 5183 5188 5193 5198 5203 5208 5213
					5243 5245 5247 5249 5251 5253 5255 5257 5259 5261 5267 5269 5271
					5273 5275 5277 5279 5281 5283 5285
MCKLOG	F	00000100	4	5600	
MCKNPSW	F	00000070	8	5523	
MCKOPSW	F	00000030	8	5495	5504
MEASUREB	X	000000B9	1	5571	
MKARCHMD	X	000000A3	1	5559	
MKARS	F	00000120	4	5598	
MKCLKCMP	F	000000E0	8	5584	
MKCPUTIM	F	000000D8	8	5583	
MKCRS	F	000001C0	4	5603	
MKDMGCOD	F	000000F4	4	5587	
MKFAILA	F	000000F8	4	5589	
MKFPRS	D	00000160	8	5601	
MKICODE	F	000000E8	4	5585	
MKLOGOUT	F	00000100	4	5591	
MKMODEL	F	000000FC	4	5590	
MKXSAA	F	000000D4	4	5582	
MONCLS	H	00000094	2	5547	
MONCODE	F	0000009C	4	5554	
MONNUMBR	X	00000095	1	5549	
MPGACCID	X	000000A2	1	5557	
MVCINCLC	I	00001402	6	4922	4916
MVCININ	X	000016C8	256	5106	4381 4912
MVCINMVC	I	000013FC	6	4921	4915
MVCINOUT	X	000017C8	256	5125	4922
MVCINSRC	I	000013F6	6	4920	4914
MVCINTST	I	000013DA	4	4911	3754 3759 3764 3769 3774 3779 3784 3789
MYPGMNEW	I	000011C0	6	4702	4679
NKGRS	F	00000180	4	5602	
NUMLOOPS	F	00001570	4	5063	3886 3896 4032 4145 4370 4382 4507 4521
NUMPGTBS	U	00000020	1	5056	5057 5059 4644
NUMSEGTB	U	00000002	1	5057	5061
OP1DATA	A	00000000	4	5151	3815
OP1LEN	F	00000004	4	5152	3816
OP1WHERE	A	00000008	4	5153	3812
OP2DATA	A	0000000C	4	5155	3819
OP2LEN	F	00000010	4	5156	3820
OP2WHERE	A	00000014	4	5157	3813
ORB	4	00000000	32	5346	5376 5384 3541
ORB1_0	X	00000004	1	5349	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
ORB1_8	X	00000005	1	5356	
ORBA	U	00000010	1	5360	
ORBB	U	00000004	1	5362	
ORBC	U	00000004	1	5352	
ORBCCW	A	00000008	4	5374	
ORBCSS	X	0000000C	1	5378	
ORBCU	X	0000000E	1	5381	
ORBD	U	00000040	1	5369	
ORBF	U	00000080	1	5357	
ORBH	U	00000002	1	5363	
ORBI	U	00000020	1	5359	
ORBKEYM	U	000000F0	1	5350	
ORBL	U	00000080	1	5367	
ORBLEN	U	0000000C	1	5376	
ORBLPM	X	00000006	1	5365	
ORBM	U	00000002	1	5353	
ORBP	U	00000040	1	5358	
ORBPARM	F	00000000	4	5347	
ORBPGM	X	0000000E	1	5380	
ORBRSV25	U	0000007E	1	5371	
ORBRSV26	U	0000003E	1	5370	
ORBRSV3	U	0000007F	1	5368	
ORBRSV4	U	00000080	1	5375	
ORBRSV5	X	0000000D	1	5379	
ORBRSV6	X	0000000F	1	5382	
ORBRSV7	X	00000010	16	5383	
ORBS	U	00000008	1	5351	
ORBT	U	00000001	1	5364	
ORBU	U	00000008	1	5361	
ORBX	U	00000001	1	5372	
ORBXLEN	U	00000020	1	5384	
ORBY	U	00000001	1	5354	
ORRB1_24	X	00000007	1	5366	
OVERHEAD	D	00001590	8	5068	3892 4141 4376 4513 4769
PAGE	U	00001000	1	5048	5052 5058 5289 4648 5253 5259 5277 5283
PAGELOOP	I	00001142	4	4655	4658
PAGETABS	U	00003080	1	5059	4645
PCFETO	A	000000C4	4	5578	
PERACCID	X	000000A1	1	5556	
PERADDR	F	00000098	4	5553	
PERCODE	X	00000096	1	5550	
PERCODMK	U	000000F0	1	5551	
PFINSADR	I	000011A4	2	4693	4707
PFPAGE	U	00000005	1	5288	5289
PFPGBYTS	U	00005000	1	5289	4666
PGMACCID	X	000000A0	1	5555	
PGMDXC	F	00000090	4	5545	
PGMICODE	H	0000008E	2	5544	4713
PGMIID	F	0000008C	4	5540	
PGMIILC	X	0000008D	1	5542	
PGMIILCM	U	0000000C	1	5543	
PGMNPSW	F	00000068	8	5522	4678 4680 4681 4702

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
PGMOPSW	F	00000028	8	5494	5502 4707
PGMTRX	F	00000090	4	5546	4719
PMCW1_0	X	00000004	1	5707	
PMCW1_8	X	00000005	1	5710	4972 4978
PMCWB	U	00000004	1	5742	
PMCWCHP0	X	00000010	1	5731	
PMCWCHP1	X	00000011	1	5732	
PMCWCHP2	X	00000012	1	5733	
PMCWCHP3	X	00000013	1	5734	
PMCWCHP4	X	00000014	1	5735	
PMCWCHP5	X	00000015	1	5736	
PMCWCHP6	X	00000016	1	5737	
PMCWCHP7	X	00000017	1	5738	
PMCWDNUM	H	00000006	2	5722	4974
PMCWE	U	00000080	1	5711	4978
PMCWEXC	X	0000001B	1	5741	
PMCWIP	F	00000000	4	5706	
PMCWISCM	U	00000038	1	5708	
PMCWLM	U	00000060	1	5712	
PMCWLMG	U	00000020	1	5713	
PMCWLML	U	00000040	1	5714	
PMCWLPM	X	00000008	1	5724	
PMCWLPUM	X	0000000A	1	5726	
PMCWM	U	00000004	1	5718	
PMCWMBI	H	0000000C	2	5728	
PMCWMM	U	00000018	1	5715	
PMCWMMC	U	00000008	1	5717	
PMCWMME	U	00000010	1	5716	
PMCWPAM	X	0000000F	1	5730	
PMCWPIM	X	0000000B	1	5727	
PMCWPNOM	X	00000009	1	5725	
PMCWPOM	X	0000000E	1	5729	
PMCWRES1	X	00000018	4	5739	
PMCWRES2	X	00000018	3	5740	
PMCWS	U	00000001	1	5744	
PMCWT	U	00000002	1	5719	
PMCWV	U	00000001	1	5720	4972
PMCWX	U	00000002	1	5743	
PRTLINE	C	000015B8	68	5075	4016 4354 4491 4630 4784 4785 5074
R0	U	00000000	1	5759	3537 4646 4655 4656 4679 4680 4687 4719 4720 4721 4726
R1	U	00000001	1	5760	3799 3826 3836 3844 3857 4688
R10	U	0000000A	1	5769	3670 3671 3679 3680 3689 3690 3700 3701 3709 3710 3718 3719 3728
					3729 3737 3738 3812 3861 3864 3897 3900 3901 3904 3905 3906 3907
					3908 3909 3910 3911 3912 3913 3914 3915 3916 3917 3918 3919 3920
					3921 3922 3923 3924 3925 3926 3927 3928 3929 3930 3931 3932 3933
					3934 3935 3936 3937 3938 3939 3940 3941 3942 3943 3944 3945 3946
					3947 3948 3949 3950 3951 3952 3953 3954 3955 3956 3957 3958 3959
					3960 3961 3962 3963 3964 3965 3966 3967 3968 3969 3970 3971 3972
					3973 3974 3975 3976 3977 3978 3979 3980 3981 3982 3983 3984 3985
					3986 3987 3988 3989 3990 3991 3992 3993 3994 3995 3996 3997 3998
					3999 4000 4001 4002 4003 4004 4005 4006 4007 4008 4010 4011 4012
					4035 4036 4037 4040 4041 4042 4043 4044 4045 4046 4047 4048 4049

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					4050 4051 4052 4053 4054 4055 4056 4057 4058 4059 4060 4061 4062
					4063 4064 4065 4066 4067 4068 4069 4070 4071 4072 4073 4074 4075
					4076 4077 4078 4079 4080 4081 4082 4083 4084 4085 4086 4087 4088
					4089 4090 4091 4092 4093 4094 4095 4096 4097 4098 4099 4100 4101
					4102 4103 4104 4105 4106 4107 4108 4109 4110 4111 4112 4113 4114
					4115 4116 4117 4118 4119 4120 4121 4122 4123 4124 4125 4126 4127
					4128 4129 4130 4131 4132 4133 4134 4136 4137 4148 4149 4150 4151
					4152 4153 4156 4157 4158 4159 4160 4161 4162 4163 4164 4165 4166
					4167 4168 4169 4170 4171 4172 4173 4174 4175 4176 4177 4178 4179
					4180 4181 4182 4183 4184 4185 4186 4187 4188 4189 4190 4191 4192
					4193 4194 4195 4196 4197 4198 4199 4200 4201 4202 4203 4204 4205
					4206 4207 4208 4209 4210 4211 4212 4213 4214 4215 4216 4217 4218
					4219 4220 4221 4222 4223 4224 4225 4226 4227 4228 4229 4230 4231
					4232 4233 4234 4235 4236 4237 4238 4239 4240 4241 4242 4243 4244
					4245 4246 4247 4248 4249 4250 4251 4252 4253 4254 4255 4256 4257
					4258 4259 4260 4261 4262 4263 4264 4265 4266 4267 4268 4269 4270
					4271 4272 4273 4274 4275 4276 4277 4278 4279 4280 4281 4282 4283
					4284 4285 4286 4287 4288 4289 4290 4291 4292 4293 4294 4295 4296
					4297 4298 4299 4300 4301 4302 4303 4304 4305 4306 4307 4308 4309
					4310 4311 4312 4313 4314 4315 4316 4317 4318 4319 4320 4321 4322
					4323 4324 4325 4326 4327 4328 4329 4330 4331 4332 4333 4334 4335
					4336 4337 4338 4339 4340 4341 4342 4343 4344 4345 4347 4348 4349
					4350 4380 4385 4386 4387 4390 4391 4392 4393 4394 4395 4396 4397
					4398 4399 4400 4401 4402 4403 4404 4405 4406 4407 4408 4409 4410
					4411 4412 4413 4414 4415 4416 4417 4418 4419 4420 4421 4422 4423
					4424 4425 4426 4427 4428 4429 4430 4431 4432 4433 4434 4435 4436
					4437 4438 4439 4440 4441 4442 4443 4444 4445 4446 4447 4448 4449
					4450 4451 4452 4453 4454 4455 4456 4457 4458 4459 4460 4461 4462
					4463 4464 4465 4466 4467 4468 4469 4470 4471 4472 4473 4474 4475
					4476 4477 4478 4479 4480 4481 4482 4483 4485 4486 4487 4517 4518
					4524 4525 4526 4529 4530 4531 4532 4533 4534 4535 4536 4537 4538
					4539 4540 4541 4542 4543 4544 4545 4546 4547 4548 4549 4550 4551
					4552 4553 4554 4555 4556 4557 4558 4559 4560 4561 4562 4563 4564
					4565 4566 4567 4568 4569 4570 4571 4572 4573 4574 4575 4576 4577
					4578 4579 4580 4581 4582 4583 4584 4585 4586 4587 4588 4589 4590
					4591 4592 4593 4594 4595 4596 4597 4598 4599 4600 4601 4602 4603
					4604 4605 4606 4607 4608 4609 4610 4611 4612 4613 4614 4615 4616
					4617 4618 4619 4620 4621 4622 4624 4625 4626 4643 4650 4651 4652
					4664 4665 4693 4733 4747 4751 4755 4869 4871 4876 4879 4902 4911
					4921 4922
R11	U	0000000B	1	5770	3832 3837 4385 4386 4387 4390 4391 4392 4393 4394 4395 4396 4397
					4398 4399 4400 4401 4402 4403 4404 4405 4406 4407 4408 4409 4410
					4411 4412 4413 4414 4415 4416 4417 4418 4419 4420 4421 4422 4423
					4424 4425 4426 4427 4428 4429 4430 4431 4432 4433 4434 4435 4436
					4437 4438 4439 4440 4441 4442 4443 4444 4445 4446 4447 4448 4449
					4450 4451 4452 4453 4454 4455 4456 4457 4458 4459 4460 4461 4462
					4463 4464 4465 4466 4467 4468 4469 4470 4471 4472 4473 4474 4475
					4476 4477 4478 4479 4480 4481 4482 4483 4485 4486 4487 4644 4660
					4739 4741 4756 4871 4873 4921
R12	U	0000000C	1	5771	3671 3680 3690 3701 3710 3719 3729 3738 3813 3862 3864 3900 3901
					3904 3905 3906 3907 3908 3909 3910 3911 3912 3913 3914 3915 3916
					3917 3918 3919 3920 3921 3922 3923 3924 3925 3926 3927 3928 3929

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					3930 3931 3932 3933 3934 3935 3936 3937 3938 3939 3940 3941 3942
					3943 3944 3945 3946 3947 3948 3949 3950 3951 3952 3953 3954 3955
					3956 3957 3958 3959 3960 3961 3962 3963 3964 3965 3966 3967 3968
					3969 3970 3971 3972 3973 3974 3975 3976 3977 3978 3979 3980 3981
					3982 3983 3984 3985 3986 3987 3988 3989 3990 3991 3992 3993 3994
					3995 3996 3997 3998 3999 4000 4001 4002 4003 4004 4005 4006 4007
					4008 4010 4011 4012 4149 4151 4153 4157 4159 4161 4163 4165 4167
					4169 4171 4173 4175 4177 4179 4181 4183 4185 4187 4189 4191 4193
					4195 4197 4199 4201 4203 4205 4207 4209 4211 4213 4215 4217 4219
					4221 4223 4225 4227 4229 4231 4233 4235 4237 4239 4241 4243 4245
					4247 4249 4251 4253 4255 4257 4259 4261 4263 4265 4267 4269 4271
					4273 4275 4277 4279 4281 4283 4285 4287 4289 4291 4293 4295 4297
					4299 4301 4303 4305 4307 4309 4311 4313 4315 4317 4319 4321 4323
					4325 4327 4329 4331 4333 4335 4337 4339 4341 4343 4345 4348 4350
					4519 4520 4524 4525 4526 4529 4530 4531 4532 4533 4534 4535 4536
					4537 4538 4539 4540 4541 4542 4543 4544 4545 4546 4547 4548 4549
					4550 4551 4552 4553 4554 4555 4556 4557 4558 4559 4560 4561 4562
					4563 4564 4565 4566 4567 4568 4569 4570 4571 4572 4573 4574 4575
					4576 4577 4578 4579 4580 4581 4582 4583 4584 4585 4586 4587 4588
					4589 4590 4591 4592 4593 4594 4595 4596 4597 4598 4599 4600 4601
					4602 4603 4604 4605 4606 4607 4608 4609 4610 4611 4612 4613 4614
					4615 4616 4617 4618 4619 4620 4621 4622 4624 4625 4626 4645 4650
					4655 4657 4693 4735 4774 4775 4777 4872 4875 4876 4877 4913 4914
					4915 4916
R13	U	0000000D	1	5772	3670 3679 3689 3700 3709 3718 3728 3737 3897 4035 4036 4037 4040
					4041 4042 4043 4044 4045 4046 4047 4048 4049 4050 4051 4052 4053
					4054 4055 4056 4057 4058 4059 4060 4061 4062 4063 4064 4065 4066
					4067 4068 4069 4070 4071 4072 4073 4074 4075 4076 4077 4078 4079
					4080 4081 4082 4083 4084 4085 4086 4087 4088 4089 4090 4091 4092
					4093 4094 4095 4096 4097 4098 4099 4100 4101 4102 4103 4104 4105
					4106 4107 4108 4109 4110 4111 4112 4113 4114 4115 4116 4117 4118
					4119 4120 4121 4122 4123 4124 4125 4126 4127 4128 4129 4130 4131
					4132 4133 4134 4136 4137 4148 4150 4152 4156 4158 4160 4162 4164
					4166 4168 4170 4172 4174 4176 4178 4180 4182 4184 4186 4188 4190
					4192 4194 4196 4198 4200 4202 4204 4206 4208 4210 4212 4214 4216
					4218 4220 4222 4224 4226 4228 4230 4232 4234 4236 4238 4240 4242
					4244 4246 4248 4250 4252 4254 4256 4258 4260 4262 4264 4266 4268
					4270 4272 4274 4276 4278 4280 4282 4284 4286 4288 4290 4292 4294
					4296 4298 4300 4302 4304 4306 4308 4310 4312 4314 4316 4318 4320
					4322 4324 4326 4328 4330 4332 4334 4336 4338 4340 4342 4344 4347
					4349 4380 4381 4654 4658 4664 4739 4743 4774 4778 4869 4872 4873
					4877 4879 4902 4911 4920
R14	U	0000000E	1	5773	3550 3554 3555 3556 3557 3559 3560 3561 3562 3564 3642 3743 3791
					3856 3859 3879 4018 4025 4356 4363 4493 4500 4632 4760 4895
R15	U	0000000F	1	5774	3674 3683 3693 3704 3713 3722 3732 3741 3754 3759 3764 3769 3774
					3779 3784 3789 3800 3803 3858 3871 3891 4017 4140 4355 4375 4492
					4512 4631 4766 4767 4772 4830 4831 4839 4855 4858 4859 4880 4893
					4894 4905 4918 4959 4991
R2	U	00000002	1	5761	3538 3543 3544 3545 3547 3800 3802 3827 3836 3848 3858 3872
R3	U	00000003	1	5762	3540 4890
R4	U	00000004	1	5763	
R5	U	00000005	1	5764	3576 3577 3578 3579 3580 3581 3588 3589 3595 3596 3602 3603 3609

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					3610 3617 3618 3624 3625 3631 3632 3638 3639 3652 3653 3654 3655
					3657 3658 3659 3660 3662 3663 3664 3665 3673 3682 3692 3703 3712
					3721 3731 3740 3753 3758 3763 3768 3773 3778 3783 3788 3805 3806
					3851 3852 3870 3886 3889 3896 4013 4032 4138 4145 4351 4370 4373
					4382 4488 4507 4510 4521 4627 4665 4666 4667 4668 4669 4672 4673
					4769 4840 4852 4857 4871 4903 4911
R6	U	00000006	1	5765	3582 3583 3588 3589 3595 3596 3602 3603 3609 3610 3617 3618 3624
					3625 3631 3632 3638 3639 3652 3653 3657 3658 3662 3663 3815 3819
					3841 3844 3861 3862 3888 3889 3899 4013 4034 4138 4147 4351 4372
					4373 4384 4488 4509 4510 4523 4627 4647 4652 4657 4667 4723 4724
					4726 4751 4757 4770 4842 4843 4844 4845 4847 4848 4849 4850 4853
					4872 4912 4913 4920
R7	U	00000007	1	5766	3816 3817 3820 3821 3831 3835 3841 3848 4648 4656 4755 4756 4757
					4771 4840 4842 4845 4847 4850 4854 4857 4877
R8	U	00000008	1	5767	3541 4891
R9	U	00000009	1	5768	3539 3547 3548
REG2LOW	U	000000DD	1	5167	5205 5210 5215
REG2PATT	U	AABBCCDD	1	5166	3827 5180 5185 5190 5195 5200 5205 5210 5215
RPTSAVE	F	00001328	4	4833	4766 4830
RPTSPEED	I	00001252	4	4766	4017 4355 4492 4631
RSTNPSW	F	00000000	8	5488	
RSTOPSW	F	00000008	8	5489	
SAVER1	F	000004A8	4	3867	3799 3857
SAVETRT	D	000004B0	8	3868	3836
SCANOUT	X	00000080	1	5526	5527
SCANOUTL	U	00000000	1	5527	
SCHIB	4	00000000	52	5703	5750 4968
SCHIBL	U	00000034	1	5750	
SCHMBA	A	00000028	8	5748	
SCHMDA1	X	00000030	4	5749	
SCHMDA3	X	00000028	12	5747	
SCHPMCW	X	00000000	28	5705	
SCHSCSW	X	0000001C	12	5746	
SCSW	4	00000000	12	5408	5470
SCSW0CC	U	00000004	1	5424	
SCSW1	X	00000002	1	5428	
SCSW2	X	00000003	1	5437	4819
SCSWACP	U	00000001	1	5436	
SCSWADA	U	00000040	1	5439	
SCSWAHP	U	00000002	1	5435	
SCSWALKC	U	00000010	1	5422	
SCSWARP	U	00000008	1	5433	
SCSWASA	U	00000080	1	5438	
SCSWASP	U	00000004	1	5434	
SCSWASUS	U	00000020	1	5440	
SCSWATTN	U	00000080	1	5450	
SCSWBUSY	U	00000010	1	5453	
SCSWCCTL	U	00000004	1	5465	
SCSWCCW	A	00000004	4	5447	4823
SCSWCCWF	U	00000080	1	5419	
SCSWCCWP	U	00000040	1	5420	
SCSWCDAT	U	00000008	1	5464	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
SCSWCE	U	00000008	1	5454	
SCSWCHNG	U	00000001	1	5467	
SCSWCNT	H	0000000A	2	5469	4824
SCSWCS	X	00000009	1	5459	
SCSWCTLS	X	00000001	1	5418	
SCSWCUE	U	00000020	1	5452	
SCSWDCC0	U	00000000	1	5414	
SCSWDCC1	U	00000001	1	5415	
SCSWDCC3	U	00000003	1	5416	
SCSWDCCM	U	00000003	1	5413	
SCSWDE	U	00000004	1	5455	
SCSWECWC	U	00000002	1	5425	
SCSWESWF	U	00000004	1	5412	
SCSWFC	U	00000010	1	5432	
SCSWFH	U	00000020	1	5431	
SCSWFLAG	X	00000000	1	5409	
SCSWFM	U	00000070	1	5429	
SCSWFS	U	00000040	1	5430	
SCSWICTL	U	00000002	1	5466	
SCSWIL	U	00000040	1	5461	
SCSWISIC	U	00000020	1	5421	
SCSWKEYM	U	000000F0	1	5410	
SCSWL	U	0000000C	1	5470	
SCSWPCI	U	00000080	1	5460	
SCSWPNOP	U	00000001	1	5426	
SCSWPRGM	U	00000020	1	5462	
SCSWPROT	U	00000010	1	5463	
SCSWSAS	U	00000010	1	5441	
SCSWSINT	U	00000008	1	5442	
SCSWSM	U	00000040	1	5451	
SCSWSPEN	U	00000001	1	5445	
SCSWSPRI	U	00000004	1	5443	4821
SCSWSSEC	U	00000002	1	5444	
SCSWSSIC	U	00000008	1	5423	
SCSWSUSC	U	00000008	1	5411	
SCSWUC	U	00000002	1	5456	
SCSWUS	X	00000008	1	5449	4820
SCSWUX	U	00000001	1	5457	
SEGLOOP	I	00001134	4	4650	4660
SEGTABLS	U	00003000	1	5058	5059 5304 4643 5061
SSARCHMD	X	000000A3	1	5558	
SSARS	F	00000120	4	5614	
SSCLKCMP	F	000000E0	8	5608	
SSCPUTIM	F	000000D8	8	5607	
SSCRS	F	000001C0	4	5617	
SSFPRS	D	00000160	8	5615	
SSGRS	F	00000180	4	5616	
SSMODEL	F	0000010C	4	5612	
SSPREFIX	F	00000108	4	5611	
SSPSW	F	00000100	8	5610	
SSXSAA	A	000000D4	4	5606	
STFLDATA	F	000000C8	4	5579	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
SUBDWORD	I	00001380	4	4869	4772 4855
SUBDWSAV	D	000013A8	8	4882	4869 4879
SUBTEST	X	000021FF	1	5302	3587 3594 3601 3608 3616 3623 3630 3637 3669 3678 3688 3699 3708 3717 3727 3736 3834 3843 3847 3882 4028 4366 4503 4639 4671 4677 4686 4706 4712 4718 4732 4738 4746 4750 4754
SVCICODE	H	0000008A	2	5538	
SVCIID	F	00000088	4	5534	
SVCIILC	X	00000089	1	5536	
SVCIILCM	U	0000000C	1	5537	
SVCNPSW	F	00000060	8	5521	
SVCOPSW	F	00000020	8	5493	5500
SVPGMNEW	D	000011B0	8	4696	4678 4702
TEST01	I	0000023A	4	3572	3554
TEST02	I	000002F0	4	3648	3555
TEST03	I	000003CA	4	3749	3556
TEST04	I	00000410	4	3797	3557
TEST91	I	000004B8	4	3878	3559
TEST92	I	00000794	4	4024	3560
TEST93	I	00000BC0	4	4362	3561
TEST94	I	00000E66	4	4499	3562
TEST95	I	00001116	4	4638	3564
TESTADDR	U	000021FE	1	5052	5053 5299
TESTNUM	X	000021FE	1	5301	3572 3648 3749 3797 3881 4027 4365 4502 4638
TICKSAAA	P	00001598	8	5070	4777 4780
TICKSBBB	P	000015A0	8	5071	4778 4782
TICKSTOT	P	000015A8	8	5072	4780 4781 4782 4785
TIMEADDR	U	000021FD	1	5053	5295
TIMEOPT	X	000021FD	1	5297	3878 4024 4362 4499
TIMER	F	00000050	4	5517	
TRT	I	0000049E	6	3864	3835
TRT1	A	000018C8	4	5177	
TRT2	A	000018F0	4	5182	
TRT256	A	00001968	4	5197	
TRT4	A	00001918	4	5187	
TRT8	A	00001940	4	5192	
TRTBC	I	000004A4	4	3865	3837
TRTBTH	A	00001990	4	5202	
TRTCTL	A	000018C8	4	5175	3805
TRTDONE	I	0000048A	4	3857	3854
TRTFAIL	I	00000486	4	3856	3845 3849 3865
TRTMVC1	I	00000492	6	3861	3817
TRTMVC2	I	00000498	6	3862	3821
TRTNEXT	U	00000028	1	5164	3851
TRTOP1	A	000019B8	4	5207	
TRTOP10	X	00001A0C	4	5223	4518 5177 5182 5187 5192 5197
TRTOP111	X	00001B0C	4	5225	5202 5212
TRTOP1F0	X	00001C0C	4	5227	5207
TRTOP2	A	000019E0	4	5212	
TRTOP20	X	00001D0C	1	5233	4520 5178 5183 5188 5193 5198
TRTOP211	X	00001E0C	1	5235	5203 5213
TRTOP2F0	X	00001F0C	1	5237	5208
TRTTEST	4	00000000	40	5149	3806

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
TST4LOOP	U	0000041E	1	3808	3853
TTDES	F	00000054	4	5518	
UA0	F	00000010	8	5490	
UA1	F	0000004C	4	5515	
UA2	F	000000A4	4	5560	
UA3	F	000000B4	4	5569	
UA4	X	000000B8	1	5570	
UA5	X	000000CC	8	5580	
UA6	X	000000EC	8	5586	
UA7	F	00000118	8	5597	
UA8	X	00000180	32	5626	
WPSW0008	3	000012C8	8	4804	4803
ZBRKADDR	A	00000110	8	5596	
ZEMONCNT	F	0000010C	4	5595	
ZEMONCTR	A	00000100	8	5593	
ZEMONSIZ	F	00000108	4	5594	
ZEXTNPSW	X	000001B0	16	5629	
ZEXTOPSW	X	00000130	16	5621	
ZIONPSW	X	000001F0	16	5633	
ZIOOPSW	X	00000170	16	5625	
ZMCKNPSW	X	000001E0	16	5632	
ZMCKOPSW	X	00000160	16	5624	
ZMKFAILA	F	000000F8	8	5588	
ZMONCODE	F	000000B0	8	5563	
ZPGMNPSW	X	000001D0	16	5631	
ZPGMOPSW	X	00000150	16	5623	
ZPGMTRX	F	000000A8	8	5562	
ZRSTNPSW	X	000001A0	16	5628	
ZRSTOPSW	X	00000120	16	5620	
ZSASDISP	U	000011C0	1	5634	
ZSVCNPSW	X	000001C0	16	5630	
ZSVCOPSW	X	00000140	16	5622	
=A(00+(5*K64))	A	0000152C	4	5033	4517
=A(MB+(5*K64))	A	00001530	4	5034	4519
=A(PAGE)	A	0000153C	4	5037	4648
=A(PAGETABS)	A	00001538	4	5036	4645 4672
=A(PFINSADR)	A	00001544	4	5039	4707
=A(PFPGBYTS)	A	00001540	4	5038	4666
=A(REG2PATT)	A	00001524	4	5031	3827
=A(SEGTABLS)	A	00001534	4	5035	4643
=CL5'CLC'	C	0000154C	5	5041	4016
=CL5'CLCL'	C	00001551	5	5042	4354
=CL5'MVCIN'	C	00001556	5	5043	4491
=CL5'TRT'	C	0000155B	5	5044	4630
=F'0'	F	00001528	4	5032	3852
=F'1'	F	00001548	4	5040	4875
=P'4294967296'	P	00001560	6	5045	4781

MACRO	DEFN	REFERENCES					
ANTR	109						
APROB	241						
ARCHIND	401	3431					
ARCHLVL	542	3430					
ASAIPL	668	3510					
ASALOAD	748	3493					
ASAREA	803	5480					
ASAZAREA	988						
CPUWAIT	1071	4800					
DSECTS	1397	5312	5344	5391	5406	5477	
DWAIT	1600	4929	4934	4939	4944		
DWAITEND	1657	4928					
ENADEV	1665	4965					
ESA390	1765						
IOCB	1776	4998					
IOCBDS	1952	5313					
IOFMT	1986	5345	5392	5407	5639	5657	5665	5702
IOINIT	2324	4953					
IOTRFR	2365						
ORB	2413	5017					
POINTER	2602						
PSWFMT	2630						
RAWAIT	2764						
RAWIO	2860	4787					
SIGCPU	3018						
SMMGR	3076						
SMMGRB	3176						
TRAP128	3225						
TRAP64	3202	3495	3498				
TRAPS	3238						
ZARCH	3312						
ZEROH	3324						
ZEROL	3352						
ZEROLH	3380						
ZEROLL	3403						

```
   DESC      SYMBOL     SIZE      POS         ADDR

Entry: 0

Image       IMAGE      12289  0000-3000  0000-3000
  Region    CODE       12289  0000-3000  0000-3000
    CSECT   CLCLETAL   12289  0000-3000  0000-3000
```

```
   STMT                                          FILE NAME

1     c:\Users\Fish\Documents\Visual Studio 2008\Projects\MyProjects\ASMA-0\CLCL-et-al\CLCL-et-al.asm
2     C:\Users\Fish\Documents\Visual Studio 2008\Projects\Hercules\_Git\_Harold\SATK-0\srcasm\satk.mac


** NO ERRORS FOUND **
```