```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                      2 ************************************************************************
                                                      3 *
                                                      4 *            CLC, CLCL, MVCIN and TRT instruction tests
                                                      5 *
                                                      6 ************************************************************************
                                                      7 *
                                                      8 *  This program tests proper functioning of the CLCL, MVCIN and TRT
                                                      9 *  instructions.  It also optionally times them.
                                                     10 *
                                                     11 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                     12 *  obvious coding errors.  None of the tests are thorough.  They are
                                                     13 *  NOT designed to test all aspects of any of the instructions.
                                                     14 *
                                                     15 ************************************************************************
                                                     16 *
                                                     17 *  Example Hercules Testcase:
                                                     18 *
                                                     19 *
                                                     20 *     *Testcase CLCL-et-al (Test CLCL, MVCIN and TRT instructions)
                                                     21 *
                                                     22 *     archlvl     390
                                                     23 *     mainsize    2
                                                     24 *     numcpu      1
                                                     25 *     sysclear
                                                     26 *
                                                     27 *     loadcore    "$(testpath)/CLCL-et-al.core"
                                                     28 *
                                                     29 *     runtest     2          # (NON-timing test duration)
                                                     30 *     ##r           21fd=ff    # (enable timing tests too!)
                                                     31 *     ##runtest     150        # (TIMING too test duration)
                                                     32 *
                                                     33 *     *Compare
                                                     34 *     r 21fe.2
                                                     35 *
                                                     36 *     *Want  "Ending test/subtest number"   9510
                                                     37 *
                                                     38 *     *Done
                                                     39 *
                                                     40 *
                                                     41 ************************************************************************
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                    43          PRINT OFF
                                                  3424          PRINT ON

                                                  3426 ********************************************************************************
                                                  3427 *        SATK prolog stuff...
                                                  3428 ********************************************************************************

                                                  3430          ARCHLVL  ZARCH=NO,MNOTE=NO
                                                  3432+$AL      OPSYN AL
                                                  3433+$ALR     OPSYN ALR
                                                  3434+$B       OPSYN B
                                                  3435+$BAS     OPSYN BAS
                                                  3436+$BASR    OPSYN BASR
                                                  3437+$BC      OPSYN BC
                                                  3438+$BCTR    OPSYN BCTR
                                                  3439+$BE      OPSYN BE
                                                  3440+$BH      OPSYN BH
                                                  3441+$BL      OPSYN BL
                                                  3442+$BM      OPSYN BM
                                                  3443+$BNE     OPSYN BNE
                                                  3444+$BNH     OPSYN BNH
                                                  3445+$BNL     OPSYN BNL
                                                  3446+$BNM     OPSYN BNM
                                                  3447+$BNO     OPSYN BNO
                                                  3448+$BNP     OPSYN BNP
                                                  3449+$BNZ     OPSYN BNZ
                                                  3450+$BO      OPSYN BO
                                                  3451+$BP      OPSYN BP
                                                  3452+$BXLE    OPSYN BXLE
                                                  3453+$BZ      OPSYN BZ
                                                  3454+$CH      OPSYN CH
                                                  3455+$L       OPSYN L
                                                  3456+$LH      OPSYN LH
                                                  3457+$LM      OPSYN LM
                                                  3458+$LPSW    OPSYN LPSW
                                                  3459+$LR      OPSYN LR
                                                  3460+$LTR     OPSYN LTR
                                                  3461+$NR      OPSYN NR
                                                  3462+$SL      OPSYN SL
                                                  3463+$SLR     OPSYN SLR
                                                  3464+$SR      OPSYN SR
                                                  3465+$ST      OPSYN ST
                                                  3466+$STM     OPSYN STM
                                                  3467+$X       OPSYN X
                                                  3468+$AHI     OPSYN AHI
                                                  3469+$B       OPSYN J
                                                  3470+$BC      OPSYN BRC
                                                  3471+$BE      OPSYN JE
                                                  3472+$BH      OPSYN JH
                                                  3473+$BL      OPSYN JL
                                                  3474+$BM      OPSYN JM
                                                  3475+$BNE     OPSYN JNE
```

```
 LOC         OBJECT CODE        ADDR1     ADDR2     STMT

                                                   3476+$BNH     OPSYN JNH
                                                   3477+$BNL     OPSYN JNL
                                                   3478+$BNM     OPSYN JNM
                                                   3479+$BNO     OPSYN JNO
                                                   3480+$BNP     OPSYN JNP
                                                   3481+$BNZ     OPSYN JNZ
                                                   3482+$BO      OPSYN JO
                                                   3483+$BP      OPSYN JP
                                                   3484+$BXLE    OPSYN JXLE
                                                   3485+$BZ      OPSYN JZ
                                                   3486+$CHI     OPSYN CHI
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  3488 ********************************************************************************
                                                  3489 *        Initiate the CLCLetal CSECT in the CODE region
                                                  3490 *        with the location counter at 0
                                                  3491 ********************************************************************************

                                                  3493 CLCLetal ASALOAD  REGION=CODE
                                 00000000  00003000 3494+CLCLetal START 0,CODE
00000000  000A0000 00000008                       3496+         PSW   0,0,2,0,X'008'      64-bit Restart ISR Trap New PSW
00000008                         00000008  00000058 3497+         ORG   CLCLetal+X'058'
00000058  000A0000 00000018                       3499+         PSW   0,0,2,0,X'018'      64-bit External ISR Trap New PSW
00000060  000A0000 00000020                       3500+         PSW   0,0,2,0,X'020'      64-bit Supervisor Call ISR Trap New PSW
00000068  000A0000 00000028                       3501+         PSW   0,0,2,0,X'028'      64-bit Program ISR Trap New PSW
00000070  000A0000 00000030                       3502+         PSW   0,0,2,0,X'030'      64-bit Machine Check Trap New PSW
00000078  000A0000 00000038                       3503+         PSW   0,0,2,0,X'038'      64-bit Input/Output Trap New PSW
00000080                         00000080  00000200 3504+         ORG   CLCLetal+512



                                                  3506 ********************************************************************************
                                                  3507 *        Create IPL (restart) PSW
                                                  3508 ********************************************************************************


                                                  3510          ASAIPL   IA=BEGIN
00000200                         00000200  00000000 3511+         ORG   CLCLetal
00000000  00080000 00000200                       3512+         PSW   0,0,0,0,BEGIN,24
00000008                         00000008  00000200 3513+         ORG   CLCLetal+512     Reset CSECT to end of assigned storage area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    3515 ********************************************************************************
                                                    3516 *                The actual "CLCLetal" program itself...
                                                    3517 ********************************************************************************
                                                    3518 *
                                                    3519 *  Architecture Mode: 390
                                                    3520 *  Addressing Mode:   31-bit
                                                    3521 *  Register Usage:
                                                    3522 *
                                                    3523 *   R0       (work)
                                                    3524 *   R1       I/O device used by ENADEV and RAWIO macros
                                                    3525 *   R2       First base register
                                                    3526 *   R3       IOCB pointer for ENADEV and RAWIO macros
                                                    3527 *   R4       IO work register used by ENADEV and RAWIO
                                                    3528 *   R5-R7    (work)
                                                    3529 *   R8       ORB pointer
                                                    3530 *   R9       Second base register
                                                    3531 *   R10-R13  (work)
                                                    3532 *   R14      Subroutine call
                                                    3533 *   R15      Secondary Subroutine call or work
                                                    3534 *
                                                    3535 ********************************************************************************


00000200                    00000000                3537          USING  ASA,R0          Low core addressability
00000200                    00000200                3538          USING  BEGIN,R2        FIRST Base Register
00000200                    00001200                3539          USING  BEGIN+4096,R9   SECOND Base Register
00000200                    00000000                3540          USING  IOCB,R3         SATK Device I/O Control Block
00000200                    00000000                3541          USING  ORB,R8          ESA/390 Operation Request Block


00000200  0520                                      3543 BEGIN    BALR  R2,0             Initalize FIRST base register
00000202  0620                                      3544          BCTR  R2,0             Initalize FIRST base register
00000204  0620                                      3545          BCTR  R2,0             Initalize FIRST base register

00000206  4190 2800                 00000800       3547          LA    R9,2048(,R2)     Initalize SECOND base register
0000020A  4190 9800                 00000800       3548          LA    R9,2048(,R9)     Initalize SECOND base register

0000020E  45E0 91D0                 000013D0       3550          BAL   R14,INIT         Initalize Program
                                                    3551 *
                                                    3552 **       Run the tests...
                                                    3553 *
00000212  45E0 203A                 0000023A       3554          BAL   R14,TEST01       Test CLC   instruction
00000216  45E0 20F0                 000002F0       3555          BAL   R14,TEST02       Test CLCL  instruction
0000021A  45E0 21CA                 000003CA       3556          BAL   R14,TEST03       Test MVCIN instruction
0000021E  45E0 2210                 00000410       3557          BAL   R14,TEST04       Test TRT   instruction
                                                    3558 *
00000222  45E0 22B8                 000004B8       3559          BAL   R14,TEST91       Time CLC   instruction  (speed test)
00000226  45E0 259A                 0000079A       3560          BAL   R14,TEST92       Time CLCL  instruction  (speed test)
0000022A  45E0 29D0                 00000BD0       3561          BAL   R14,TEST93       Time MVCIN instruction  (speed test)
0000022E  45E0 2C76                 00000E76       3562          BAL   R14,TEST94       Time TRT   instruction  (speed test)
                                                    3563 *
00000232  45E0 2F26                 00001126       3564          BAL   R14,TEST95       Test CLCL page fault handling
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                     3565 *
00000236  47F0 9220                       00001420  3566          B     EOJ               Normal completion
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  3568 ********************************************************************************
                                                  3569 *        TEST01                  Test CLC instruction
                                                  3570 ********************************************************************************

0000023A  9201 9FFE                      000021FE  3572 TEST01   MVI   TESTNUM,X'01'
                                                  3573 *
                                                  3574 **       Initialize test parameters...
                                                  3575 *
0000023E  5850 9440                      00001640  3576          L      R5,CLC4          Operand-1 address
00000242  92FF 5003                      00000003  3577          MVI    3(R5),X'FF'      Force unequal compare (op1 high)
00000246  5850 9450                      00001650  3578          L      R5,CLC256        (same thing for CLC256)
0000024A  92FF 50FF                      000000FF  3579          MVI    255(R5),X'FF'    (same thing for CLC256)
0000024E  5850 9458                      00001658  3580          L      R5,CLCOP1        (same thing for CLCOP1)
00000252  92FF 50FF                      000000FF  3581          MVI    255(R5),X'FF'    (same thing for CLCOP1)
00000256  5860 944C                      0000164C  3582          L      R6,CLC8+4        OPERAND-2(!) address
0000025A  92FF 6007                      00000007  3583          MVI    7(R6),X'FF'      Force OPERAND-2 to be high! (op1 LOW!)
                                                  3584 *
                                                  3585 **       Neither cross (one byte)
                                                  3586 *
0000025E  9201 9FFF                      000021FF  3587          MVI   SUBTEST,X'01'
00000262  9856 9420                      00001620  3588          LM    R5,R6,CLC1
00000266  D500 5000 6000      00000000   00000000  3589          CLC   0(1,R5),0(R6)
0000026C  4770 9250                      00001450  3590          BNE   FAILTEST
                                                  3591 *
                                                  3592 **       Neither cross (two bytes)
                                                  3593 *
00000270  9202 9FFF                      000021FF  3594          MVI   SUBTEST,X'02'
00000274  9856 9428                      00001628  3595          LM    R5,R6,CLC2
00000278  D501 5000 6000      00000000   00000000  3596          CLC   0(2,R5),0(R6)
0000027E  4770 9250                      00001450  3597          BNE   FAILTEST
                                                  3598 *
                                                  3599 **       Neither cross (four bytes)
                                                  3600 *
00000282  9204 9FFF                      000021FF  3601          MVI   SUBTEST,X'04'
00000286  9856 9440                      00001640  3602          LM    R5,R6,CLC4
0000028A  D503 5000 6000      00000000   00000000  3603          CLC   0(4,R5),0(R6)
00000290  47D0 9250                      00001450  3604          BNH   FAILTEST                 (see INIT; CLC4:    op1 > op2)
                                                  3605 *
                                                  3606 **       Neither cross (eight bytes)
                                                  3607 *
00000294  9208 9FFF                      000021FF  3608          MVI   SUBTEST,X'08'
00000298  9856 9448                      00001648  3609          LM    R5,R6,CLC8
0000029C  D507 5000 6000      00000000   00000000  3610          CLC   0(8,R5),0(R6)
000002A2  47B0 9250                      00001450  3611          BNL   FAILTEST                 (see INIT; CLC8:    op1 < op2)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3613 *
                                                  3614 **       Neither cross (256 bytes)
                                                  3615 *
000002A6  92FF 9FFF                     000021FF  3616          MVI   SUBTEST,X'FF'
000002AA  9856 9450                     00001650  3617          LM    R5,R6,CLC256
000002AE  D5FF 5000 6000      00000000  00000000  3618          CLC   0(256,R5),0(R6)
000002B4  47D0 9250                     00001450  3619          BNH   FAILTEST                (see INIT; CLC256:  op1 > op2)
                                                  3620 *
                                                  3621 **       Both cross
                                                  3622 *
000002B8  9222 9FFF                     000021FF  3623          MVI   SUBTEST,X'22'
000002BC  9856 9430                     00001630  3624          LM    R5,R6,CLCBOTH
000002C0  D5FF 5000 6000      00000000  00000000  3625          CLC   0(256,R5),0(R6)
000002C6  4770 9250                     00001450  3626          BNE   FAILTEST
                                                  3627 *
                                                  3628 **       Only op1 crosses
                                                  3629 *
000002CA  9210 9FFF                     000021FF  3630          MVI   SUBTEST,X'10'
000002CE  9856 9458                     00001658  3631          LM    R5,R6,CLCOP1
000002D2  D5FF 5000 6000      00000000  00000000  3632          CLC   0(256,R5),0(R6)
000002D8  47D0 9250                     00001450  3633          BNH   FAILTEST                (see INIT; CLCOP1:  op1 > op2)
                                                  3634 *
                                                  3635 **       Only op2 crosses
                                                  3636 *
000002DC  9220 9FFF                     000021FF  3637          MVI   SUBTEST,X'20'
000002E0  9856 9438                     00001638  3638          LM    R5,R6,CLCOP2
000002E4  D5FF 5000 6000      00000000  00000000  3639          CLC   0(256,R5),0(R6)
000002EA  4770 9250                     00001450  3640          BNE   FAILTEST
                                                  3641 *
000002EE  07FE                                    3642          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                          3644 ********************************************************************************
                                          3645 *        TEST02                    Test CLCL instruction
                                          3646 ********************************************************************************

000002F0  9202 9FFE                       000021FE  3648 TEST02   MVI   TESTNUM,X'02'
                                          3649 *
                                          3650 **       Initialize test parameters...
                                          3651 *
000002F4  9856 9E84                       00002084  3652          LM    R5,R6,CLCL4     CLCL4 test Op1 address and length
000002F8  1E56                                      3653          ALR   R5,R6           Point past last byte
000002FA  0650                                      3654          BCTR  R5,0            Backup to last byte
000002FC  92FF 5000                       00000000  3655          MVI   0(R5),X'FF'     Force unequal compare (op1 high)
                                          3656 *
00000300  9856 9EA4                       000020A4  3657          LM    R5,R6,CLCLOP1   (same thing for CLCLOP1 test)
00000304  1E56                                      3658          ALR   R5,R6                    "
00000306  0650                                      3659          BCTR  R5,0                     "
00000308  92FF 5000                       00000000  3660          MVI   0(R5),X'FF'              "
                                          3661 *
0000030C  9856 9E9C                       0000209C  3662          LM    R5,R6,CLCL8+8   CLCL8 test ===> OP2 <===
00000310  1E56                                      3663          ALR   R5,R6
00000312  0650                                      3664          BCTR  R5,0
00000314  92FF 5000                       00000000  3665          MVI   0(R5),X'FF'     ===> OPERAND-2 high (OP1 LOW) <===
                                          3666 *
                                          3667 **       Neither cross (one byte)
                                          3668 *
00000318  9201 9FFF                       000021FF  3669          MVI   SUBTEST,X'01'
0000031C  98AD 9E24                       00002024  3670          LM    R10,R13,CLCL1
00000320  0FAC                                      3671          CLCL  R10,R12
00000322  4770 9250                       00001450  3672          BNE   FAILTEST
00000326  4150 9EC4                       000020C4  3673          LA    R5,ECLCL1
0000032A  45F0 91E2                       000013E2  3674          BAL   R15,ENDCLCL
                                          3675 *
                                          3676 **       Neither cross (two bytes)
                                          3677 *
0000032E  9202 9FFF                       000021FF  3678          MVI   SUBTEST,X'02'
00000332  98AD 9E34                       00002034  3679          LM    R10,R13,CLCL2
00000336  0FAC                                      3680          CLCL  R10,R12
00000338  4770 9250                       00001450  3681          BNE   FAILTEST
0000033C  4150 9ED4                       000020D4  3682          LA    R5,ECLCL2
00000340  45F0 91E2                       000013E2  3683          BAL   R15,ENDCLCL
                                          3684 *
                                          3685 **       Neither cross (four bytes)
                                          3686 **       (inequality on last byte of op1)
                                          3687 *
00000344  9204 9FFF                       000021FF  3688          MVI   SUBTEST,X'04'
00000348  98AD 9E84                       00002084  3689          LM    R10,R13,CLCL4
0000034C  0FAC                                      3690          CLCL  R10,R12
0000034E  47D0 9250                       00001450  3691          BNH   FAILTEST                (see INIT; CLCL4:   op1 > op2)
00000352  4150 9F24                       00002124  3692          LA    R5,ECLCL4
00000356  45F0 91E2                       000013E2  3693          BAL   R15,ENDCLCL
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          3695 *
                                          3696 **       Neither cross (eight bytes)
                                          3697 **       (inequality on last byte of op2)
                                          3698 *
0000035A  9208 9FFF                       000021FF  3699          MVI   SUBTEST,X'08'
0000035E  98AD 9E94                       00002094  3700          LM    R10,R13,CLCL8
00000362  0FAC                                      3701          CLCL  R10,R12
00000364  47B0 9250                       00001450  3702          BNL   FAILTEST                  (see INIT; CLCL8:   op1 < op2)
00000368  4150 9F34                       00002134  3703          LA    R5,ECLCL8
0000036C  45F0 91E2                       000013E2  3704          BAL   R15,ENDCLCL
                                          3705 *
                                          3706 **       Neither cross (1K bytes)
                                          3707 *
00000370  9200 9FFF                       000021FF  3708          MVI   SUBTEST,X'00'
00000374  98AD 9E54                       00002054  3709          LM    R10,R13,CLCL1K
00000378  0FAC                                      3710          CLCL  R10,R12
0000037A  4770 9250                       00001450  3711          BNE   FAILTEST
0000037E  4150 9EF4                       000020F4  3712          LA    R5,ECLCL1K
00000382  45F0 91E2                       000013E2  3713          BAL   R15,ENDCLCL
                                          3714 *
                                          3715 **       Both cross
                                          3716 *
00000386  9222 9FFF                       000021FF  3717          MVI   SUBTEST,X'22'
0000038A  98AD 9E64                       00002064  3718          LM    R10,R13,CLCLBOTH
0000038E  0FAC                                      3719          CLCL  R10,R12
00000390  4770 9250                       00001450  3720          BNE   FAILTEST
00000394  4150 9F04                       00002104  3721          LA    R5,ECLCLBTH
00000398  45F0 91E2                       000013E2  3722          BAL   R15,ENDCLCL
                                          3723 *
                                          3724 **       Only op1 crosses
                                          3725 **       (inequality on last byte of op1)
                                          3726 *
0000039C  9210 9FFF                       000021FF  3727          MVI   SUBTEST,X'10'
000003A0  98AD 9EA4                       000020A4  3728          LM    R10,R13,CLCLOP1
000003A4  0FAC                                      3729          CLCL  R10,R12
000003A6  47D0 9250                       00001450  3730          BNH   FAILTEST                  (see INIT; CLCLOP1: op1 > op2)
000003AA  4150 9F44                       00002144  3731          LA    R5,ECLCLOP1
000003AE  45F0 91E2                       000013E2  3732          BAL   R15,ENDCLCL
                                          3733 *
                                          3734 **       Only op2 crosses
                                          3735 *
000003B2  9220 9FFF                       000021FF  3736          MVI   SUBTEST,X'20'
000003B6  98AD 9E74                       00002074  3737          LM    R10,R13,CLCLOP2
000003BA  0FAC                                      3738          CLCL  R10,R12
000003BC  4770 9250                       00001450  3739          BNE   FAILTEST
000003C0  4150 9F14                       00002114  3740          LA    R5,ECLCLOP2
000003C4  45F0 91E2                       000013E2  3741          BAL   R15,ENDCLCL
                                          3742 *
000003C8  07FE                                      3743          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3745 ********************************************************************************
                                                  3746 *        TEST03                    Test MVCIN instruction
                                                  3747 ********************************************************************************

000003CA  9203 9FFE                      000021FE  3749 TEST03   MVI   TESTNUM,X'03'
                                                  3750 *
                                                  3751 **       Neither cross (one byte)
                                                  3752 *
000003CE  4150 9460                      00001660  3753          LA    R5,INV1
000003D2  45F0 91F2                      000013F2  3754          BAL   R15,MVCINTST
                                                  3755 *
                                                  3756 **       Neither cross (two bytes)
                                                  3757 *
000003D6  4150 9470                      00001670  3758          LA    R5,INV2
000003DA  45F0 91F2                      000013F2  3759          BAL   R15,MVCINTST
                                                  3760 *
                                                  3761 **       Neither cross (four bytes)
                                                  3762 *
000003DE  4150 9480                      00001680  3763          LA    R5,INV4
000003E2  45F0 91F2                      000013F2  3764          BAL   R15,MVCINTST
                                                  3765 *
                                                  3766 **       Neither cross (eight bytes)
                                                  3767 *
000003E6  4150 9490                      00001690  3768          LA    R5,INV8
000003EA  45F0 91F2                      000013F2  3769          BAL   R15,MVCINTST
                                                  3770 *
                                                  3771 **       Neither cross (256 bytes)
                                                  3772 *
000003EE  4150 94A0                      000016A0  3773          LA    R5,INV256
000003F2  45F0 91F2                      000013F2  3774          BAL   R15,MVCINTST
                                                  3775 *
                                                  3776 **       Both cross
                                                  3777 *
000003F6  4150 94B0                      000016B0  3778          LA    R5,INVBOTH
000003FA  45F0 91F2                      000013F2  3779          BAL   R15,MVCINTST
                                                  3780 *
                                                  3781 **       Only op1 crosses
                                                  3782 *
000003FE  4150 94C0                      000016C0  3783          LA    R5,INVOP1
00000402  45F0 91F2                      000013F2  3784          BAL   R15,MVCINTST
                                                  3785 *
                                                  3786 **       Only op2 crosses
                                                  3787 *
00000406  4150 94D0                      000016D0  3788          LA    R5,INVOP2
0000040A  45F0 91F2                      000013F2  3789          BAL   R15,MVCINTST
                                                  3790 *
0000040E  07FE                                    3791          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3793 ********************************************************************************
                                                  3794 *        TEST04                    Test TRT instruction
                                                  3795 ********************************************************************************
00000410  9204 9FFE                      000021FE  3797 TEST04   MVI   TESTNUM,X'04'
                                                  3798
00000414  5010 22A8                      000004A8  3799          ST    R1,SAVER1          Save register 1
00000418  18F2                                     3800          LR    R15,R2             Save first base register
                                                  3801
0000041A                                          3802          DROP  R2                 Temporarily drop addressability
0000041A                  00000200                3803          USING BEGIN,R15          Establish temporary addressability
                                                  3804
0000041A  4150 96E0                      000018E0 3805          LA    R5,TRTCTL          Point R5 --> testing control table
0000041E                  00000000                3806          USING TRTTEST,R5         What each table entry looks like
                                                  3807
                          0000041E  00000001      3808 TST4LOOP EQU   *
                                                  3809 *
                                                  3810 **       Initialize operand data  (move data to testing address)
                                                  3811 *
0000041E  58A0 5008                      00000008 3812          L     R10,OP1WHERE       Where to move operand-1 data to
00000422  58C0 5014                      00000014 3813          L     R12,OP2WHERE       Where to move operand-2 data to
                                                  3814
00000426  5860 5000                      00000000 3815          L     R6,OP1DATA         Where op1 data is right now
0000042A  5870 5004                      00000004 3816          L     R7,OP1LEN          How much of it there is
0000042E  4470 F292                      00000492 3817          EX    R7,TRTMVC1         Move op1 data to testing location
                                                  3818
00000432  5860 500C                      0000000C 3819          L     R6,OP2DATA         Where op1 data is right now
00000436  5870 5010                      00000010 3820          L     R7,OP2LEN          How much of it there is
0000043A  4470 F298                      00000498 3821          EX    R7,TRTMVC2         Move op1 data to testing location
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    3823 *
                                                    3824 **       Initialize R1/R2...      (TRT non-zero CC updates R1/R2!)
                                                    3825 *
0000043E  1F11                                      3826          SLR   R1,R1               (known value)
00000440  5820 933C                         0000153C 3827          L     R2,=A(REG2PATT)    (known value)
                                                    3828 *
                                                    3829 **       Execute TRT instruction and check for expected condition code
                                                    3830 *
00000444  5870 5018                         00000018 3831          L     R7,EXLEN           (len-1)
00000448  58B0 501C                         0000001C 3832          L     R11,FAILMASK       (failure CC)
                                                    3833
0000044C  9200 9FFF                         000021FF 3834          MVI   SUBTEST,X'00'      (primary TRT)
00000450  4470 F29E                         0000049E 3835          EX    R7,TRT             TRT...
00000454  9012 F2B0                         000004B0 3836          STM   R1,R2,SAVETRT      (save R1/R2 results)
00000458  44B0 F2A4                         000004A4 3837          EX    R11,TRTBC          fail if...
                                                    3838 *
                                                    3839 **       Verify R1/R2 now contain (or still contain!) expected values
                                                    3840 *
0000045C  9867 5020                         00000020 3841          LM    R6,R7,ENDREGS
                                                    3842
00000460  9201 9FFF                         000021FF 3843          MVI   SUBTEST,X'01'      (R1 result)
00000464  1516                                      3844          CLR   R1,R6              R1 correct?
00000466  4770 F286                         00000486 3845          BNE   TRTFAIL            No, FAILTEST!
                                                    3846
0000046A  9202 9FFF                         000021FF 3847          MVI   SUBTEST,X'02'      (R2 result)
0000046E  1527                                      3848          CLR   R2,R7              R2 correct?
00000470  4770 F286                         00000486 3849          BNE   TRTFAIL            No, FAILTEST!
                                                    3850
00000474  4150 5028                         00000028 3851          LA    R5,TRTNEXT         Go on to next table entry
00000478  D503 9340 5000      00001540     00000000 3852          CLC   =F'0',0(R5)        End of table?
0000047E  4770 F21E                         0000041E 3853          BNE   TST4LOOP           No, loop...
00000482  47F0 F28A                         0000048A 3854          B     TRTDONE            Done! (success!)
                                                    3855
00000486  41E0 9250                         00001450 3856 TRTFAIL  LA    R14,FAILTEST       Unexpected results!
0000048A  5810 F2A8                         000004A8 3857 TRTDONE  L     R1,SAVER1          Restore register 1
0000048E  182F                                      3858          LR    R2,R15             Restore first base register
00000490  07FE                                      3859          BR    R14                Return to caller or FAILTEST
                                                    3860
00000492  D200 A000 6000      00000000     00000000 3861 TRTMVC1  MVC   0(0,R10),0(R6)     (move op1 to where it should be)
00000498  D200 C000 6000      00000000     00000000 3862 TRTMVC2  MVC   0(0,R12),0(R6)     (move op2 to where it should be)
                                                    3863
0000049E  DD00 A000 C000      00000000     00000000 3864 TRT      TRT   0(0,R10),0(R12)    (TRT op1,op2)
000004A4  4700 F286                         00000486 3865 TRTBC    BC    0,TRTFAIL          (fail if unexpected condition code)
                                                    3866
000004A8  00000000                                  3867 SAVER1   DC    F'0'
000004B0  00000000 00000000                         3868 SAVETRT  DC    D'0'               (saved R1/R2 from TRT results)
                                                    3869
000004B8                                            3870          DROP  R5
000004B8                                            3871          DROP  R15
000004B8                      00000200              3872          USING BEGIN,R2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3874 ********************************************************************************
                                                  3875 *        TEST91                  Time CLC instruction  (speed test)
                                                  3876 ********************************************************************************

000004B8  91FF 9FFD                     000021FD  3878 TEST91   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
000004BC  078E                                    3879           BZR   R14              No, skip timing tests

000004BE  9291 9FFE                     000021FE  3881           MVI   TESTNUM,X'91'
000004C2  9201 9FFF                     000021FF  3882           MVI   SUBTEST,X'01'
                                                  3883 *
                                                  3884 **       First, make sure we start clean!
                                                  3885 *
000004C6  98AD 9E44                     00002044  3886           LM    R10,R13,CLCL256        (Yes, "CLCL256", not "CLC256"!)
000004CA  D2FF A000 C000      00000000  00000000  3887           MVC   0(256,R10),0(R12)      (forces full equal comparison)
                                                  3888 *
                                                  3889 **       Next, time the overhead...
                                                  3890 *
000004D0  5850 9388                     00001588  3891           L     R5,NUMLOOPS
000004D4  B205 9390                     00001590  3892           STCK  BEGCLOCK
000004D8  0560                                    3893           BALR  R6,0
000004DA  0656                                    3894           BCTR  R5,R6
000004DC  B205 9398                     00001598  3895           STCK  ENDCLOCK
000004E0  45F0 9144                     00001344  3896           BAL   R15,CALCDUR
000004E4  D207 93A8 93A0      000015A8  000015A0  3897           MVC   OVERHEAD,DURATION
                                                  3898 *
                                                  3899 **       Now do the actual timing run...
                                                  3900 *
000004EA  5850 9388                     00001588  3901           L     R5,NUMLOOPS
000004EE  B205 9390                     00001590  3902           STCK  BEGCLOCK
000004F2  0560                                    3903           BALR  R6,0
000004F4  D5FF A000 C000      00000000  00000000  3904           CLC   0(256,R10),0(R12)
000004FA  D5FF A000 C000      00000000  00000000  3905           CLC   0(256,R10),0(R12)
                                                  3906 *         ..........ETC..........
                                                  3907           PRINT OFF
                                                  4013           PRINT ON
00000776  D5FF A000 C000      00000000  00000000  4014           CLC   0(256,R10),0(R12)
0000077C  D5FF A000 C000      00000000  00000000  4015           CLC   0(256,R10),0(R12)
00000782  D5FF A000 C000      00000000  00000000  4016           CLC   0(256,R10),0(R12)
00000788  0656                                    4017           BCTR  R5,R6
0000078A  B205 9398                     00001598  4018           STCK  ENDCLOCK
                                                  4019 *
0000078E  D204 93F1 9364      000015F1  00001564  4020           MVC   PRTLINE+33(5),=CL5'CLC'
00000794  45F0 906A                     0000126A  4021           BAL   R15,RPTSPEED
00000798  07FE                                    4022           BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4024 ********************************************************************************
                                          4025 *        TEST92                  Time CLCL instruction  (speed test)
                                          4026 ********************************************************************************

0000079A  91FF 9FFD                 000021FD  4028 TEST92   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
0000079E  078E                              4029          BZR   R14              No, skip timing tests

000007A0  9292 9FFE                 000021FE  4031          MVI   TESTNUM,X'92'
000007A4  9201 9FFF                 000021FF  4032          MVI   SUBTEST,X'01'
                                          4033 *
                                          4034 **       First, make sure we start clean!
                                          4035 *
000007A8  98AD 9E44                 00002044  4036          LM    R10,R13,CLCL256
000007AC  D2FF A000 C000      00000000  00000000  4037          MVC   0(256,R10),0(R12)          (forces full comparison)
                                          4038 *
                                          4039 **       Next, time the overhead...
                                          4040 *
000007B2  5850 9388                 00001588  4041          L     R5,NUMLOOPS
000007B6  B205 9390                 00001590  4042          STCK  BEGCLOCK
000007BA  0560                              4043          BALR  R6,0
000007BC  98AD 9E44                 00002044  4044          LM    R10,R13,CLCL256
000007C0  98AD 9E44                 00002044  4045          LM    R10,R13,CLCL256
                                          4046 *        .........ETC.........
                                          4047          PRINT OFF
                                          4144          PRINT ON
00000944  98AD 9E44                 00002044  4145          LM    R10,R13,CLCL256
00000948  98AD 9E44                 00002044  4146          LM    R10,R13,CLCL256
0000094C  0656                              4147          BCTR  R5,R6
0000094E  B205 9398                 00001598  4148          STCK  ENDCLOCK
00000952  45F0 9144                 00001344  4149          BAL   R15,CALCDUR
00000956  D207 93A8 93A0      000015A8  000015A0  4150          MVC   OVERHEAD,DURATION
                                          4151 *
                                          4152 **       Now do the actual timing run...
                                          4153 *
0000095C  5850 9388                 00001588  4154          L     R5,NUMLOOPS
00000960  B205 9390                 00001590  4155          STCK  BEGCLOCK
00000964  0560                              4156          BALR  R6,0
00000966  98AD 9E44                 00002044  4157          LM    R10,R13,CLCL256
0000096A  0FAC                              4158          CLCL  R10,R12
0000096C  98AD 9E44                 00002044  4159          LM    R10,R13,CLCL256
00000970  0FAC                              4160          CLCL  R10,R12
                                          4161 *        .........ETC.........
                                          4162          PRINT OFF
                                          4357          PRINT ON
00000BB8  98AD 9E44                 00002044  4358          LM    R10,R13,CLCL256
00000BBC  0FAC                              4359          CLCL  R10,R12
00000BBE  0656                              4360          BCTR  R5,R6
00000BC0  B205 9398                 00001598  4361          STCK  ENDCLOCK
                                          4362 *
00000BC4  D204 93F1 9369      000015F1  00001569  4363          MVC   PRTLINE+33(5),=CL5'CLCL'
00000BCA  45F0 906A                 0000126A  4364          BAL   R15,RPTSPEED
00000BCE  07FE                              4365          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   4367 ********************************************************************************
                                                   4368 *        TEST93                  Time MVCIN instruction  (speed test)
                                                   4369 ********************************************************************************

00000BD0  91FF 9FFD                     000021FD  4371 TEST93   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
00000BD4  078E                                    4372          BZR   R14              No, skip timing tests

00000BD6  9293 9FFE                     000021FE  4374          MVI   TESTNUM,X'93'
00000BDA  9201 9FFF                     000021FF  4375          MVI   SUBTEST,X'01'
                                                   4376 *
                                                   4377 **       First, make sure we start clean!
                                                   4378 *
00000BDE  98AD 94A0                     000016A0  4379          LM    R10,R13,INV256
00000BE2  D2FF D000 94E0      00000000  000016E0  4380          MVC   0(256,R13),MVCININ     (doesn't really matter, but...)
                                                   4381 *
                                                   4382 **       Next, time the overhead...
                                                   4383 *
00000BE8  5850 9388                     00001588  4384          L     R5,NUMLOOPS
00000BEC  B205 9390                     00001590  4385          STCK  BEGCLOCK
00000BF0  0560                                    4386          BALR  R6,0
00000BF2  0656                                    4387          BCTR  R5,R6
00000BF4  B205 9398                     00001598  4388          STCK  ENDCLOCK
00000BF8  45F0 9144                     00001344  4389          BAL   R15,CALCDUR
00000BFC  D207 93A8 93A0      000015A8  000015A0  4390          MVC   OVERHEAD,DURATION
                                                   4391 *
                                                   4392 **       Now do the actual timing run...
                                                   4393 *
00000C02  5850 9388                     00001588  4394          L     R5,NUMLOOPS
00000C06  B205 9390                     00001590  4395          STCK  BEGCLOCK
00000C0A  0560                                    4396          BALR  R6,0
00000C0C  E8FF A000 B000      00000000  00000000  4397          MVCIN 0(256,R10),0(R11)
00000C12  E8FF A000 B000      00000000  00000000  4398          MVCIN 0(256,R10),0(R11)
00000C18  E8FF A000 B000      00000000  00000000  4399          MVCIN 0(256,R10),0(R11)
                                                   4400 *        .........ETC.........
                                                   4401          PRINT OFF
                                                   4496          PRINT ON
00000E52  E8FF A000 B000      00000000  00000000  4497          MVCIN 0(256,R10),0(R11)
00000E58  E8FF A000 B000      00000000  00000000  4498          MVCIN 0(256,R10),0(R11)
00000E5E  E8FF A000 B000      00000000  00000000  4499          MVCIN 0(256,R10),0(R11)
00000E64  0656                                    4500          BCTR  R5,R6
00000E66  B205 9398                     00001598  4501          STCK  ENDCLOCK
                                                   4502 *
00000E6A  D204 93F1 936E      000015F1  0000156E  4503          MVC   PRTLINE+33(5),=CL5'MVCIN'
00000E70  45F0 906A                     0000126A  4504          BAL   R15,RPTSPEED
00000E74  07FE                                    4505          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4507 ********************************************************************************
                                          4508 *        TEST94                  Time TRT instruction  (speed test)
                                          4509 ********************************************************************************

00000E76  91FF 9FFD                 000021FD  4511 TEST94   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
00000E7A  078E                              4512          BZR   R14              No, skip timing tests

00000E7C  9294 9FFE                 000021FE  4514          MVI   TESTNUM,X'94'
00000E80  9201 9FFF                 000021FF  4515          MVI   SUBTEST,X'01'
                                          4516 *
                                          4517 **       First, make sure we start clean!
                                          4518 *
00000E84  58A0 9344                 00001544  4519          L     R10,=A(00+(5*K64))
00000E88  D2FF A000 9824      00000000  00001A24  4520          MVC   0(256,R10),TRTOP10
00000E8E  58C0 9348                 00001548  4521          L     R12,=A(MB+(5*K64))
00000E92  D2FF C000 9B24      00000000  00001D24  4522          MVC   0(256,R12),TRTOP20     (no stop = full op1 processing)
                                          4523 *
                                          4524 **       Next, time the overhead...
                                          4525 *
00000E98  5850 9388                 00001588  4526          L     R5,NUMLOOPS
00000E9C  B205 9390                 00001590  4527          STCK  BEGCLOCK
00000EA0  0560                              4528          BALR  R6,0
00000EA2  0656                              4529          BCTR  R5,R6
00000EA4  B205 9398                 00001598  4530          STCK  ENDCLOCK
00000EA8  45F0 9144                 00001344  4531          BAL   R15,CALCDUR
00000EAC  D207 93A8 93A0      000015A8  000015A0  4532          MVC   OVERHEAD,DURATION
                                          4533 *
                                          4534 **       Now do the actual timing run...
                                          4535 *
00000EB2  5850 9388                 00001588  4536          L     R5,NUMLOOPS
00000EB6  B205 9390                 00001590  4537          STCK  BEGCLOCK
00000EBA  0560                              4538          BALR  R6,0
00000EBC  DDFF A000 C000      00000000  00000000  4539          TRT   0(256,R10),0(R12)
00000EC2  DDFF A000 C000      00000000  00000000  4540          TRT   0(256,R10),0(R12)
00000EC8  DDFF A000 C000      00000000  00000000  4541          TRT   0(256,R10),0(R12)
                                          4542 *        .........ETC.........
                                          4543          PRINT OFF
                                          4638          PRINT ON
00001102  DDFF A000 C000      00000000  00000000  4639          TRT   0(256,R10),0(R12)
00001108  DDFF A000 C000      00000000  00000000  4640          TRT   0(256,R10),0(R12)
0000110E  DDFF A000 C000      00000000  00000000  4641          TRT   0(256,R10),0(R12)
00001114  0656                              4642          BCTR  R5,R6
00001116  B205 9398                 00001598  4643          STCK  ENDCLOCK
                                          4644 *
0000111A  D204 93F1 9373      000015F1  00001573  4645          MVC   PRTLINE+33(5),=CL5'TRT'
00001120  45F0 906A                 0000126A  4646          BAL   R15,RPTSPEED
00001124  07FE                              4647          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4649 ********************************************************************************
                                          4650 *        TEST95                    Test CLCL page fault handling
                                          4651 ********************************************************************************

00001126  9295 9FFE                     000021FE  4653 TEST95   MVI   TESTNUM,X'95'
0000112A  9200 9FFF                     000021FF  4654          MVI   SUBTEST,X'00'
                                          4655 *
                                          4656 **       First, make sure we start clean!
                                          4657 *
0000112E  98AD 9EB4                     000020B4  4658          LM    R10,R13,CLCLPF     Retrieve CLCL PF test parameters
00001132  0EAC                                    4659          MVCL  R10,R12            (forces full comparison)
                                          4660 *
                                          4661 **       Initialize Dynamic Address Translation tables...
                                          4662 *
00001134  58A0 934C                     0000154C  4663          L     R10,=A(SEGTABLS)   Segment Tables Origin
00001138  41B0 0020                     00000020  4664          LA    R11,NUMPGTBS       Number of Segment Table Entries
0000113C  58C0 9350                     00001550  4665          L     R12,=A(PAGETABS)   Page Tables Origin
00001140  1F00                                    4666          SLR   R0,R0              First Page Frame Address
00001142  4160 0004                     00000004  4667          LA    R6,4               Size of one table entry
00001146  5870 9354                     00001554  4668          L     R7,=A(PAGE)        Size of one Page Frame

0000114A  50C0 A000                     00000000  4670 SEGLOOP  ST    R12,0(,R10)        Seg Table Entry <= Page Table Origin
0000114E  960F A003                     00000003  4671          OI    3(R10),X'0F'       Seg Table Entry <= Page Table Length
00001152  1EA6                                    4672          ALR   R10,R6             Bump to next Segment Table Entry

00001154  41D0 0010                     00000010  4674          LA    R13,16             Page Table Entries per Page Table

00001158  5000 C000                     00000000  4675 PAGELOOP ST    R0,0(,R12)         Page Table Entry = Page Frame Address
0000115C  1E07                                    4676          ALR   R0,R7              Increment to next Page Frame Address
0000115E  1EC6                                    4677          ALR   R12,R6             Bump to next Page Table Entry
00001160  46D0 2F58                     00001158  4678          BCT   R13,PAGELOOP       Loop until Page table is complete

00001164  46B0 2F4A                     0000114A  4680          BCT   R11,SEGLOOP        Loop until all Segment Table Entries built
                                          4681 *
                                          4682 **       Update desired page table entry to cause page fault
                                          4683 *
00001168  98AD 9EB4                     000020B4  4684          LM    R10,R13,CLCLPF     Retrieve CLCL PF test parameters
0000116C  185A                                    4685          LR    R5,R10             R5 --> Operand-1
0000116E  5E50 9358                     00001558  4686          AL    R5,=A(PFPGBYTS)    R5 --> Operand-1 Page Fault address
00001172  1865                                    4687          LR    R6,R5              R6 --> Address where PF should occur
00001174  8850 000C                     0000000C  4688          SRL   R5,12              R5 = Page Frame number
00001178  8950 0002                     00000002  4689          SLL   R5,2               R5 = Page Table Entry number

0000117C  9204 9FFF                     000021FF  4691          MVI   SUBTEST,X'04'
00001180  5E50 9350                     00001550  4692          AL    R5,=A(PAGETABS)    R5 --> Page Table Entry
00001184  9604 5002                     00000002  4693          OI    2(R5),X'04'        Mark this page invalid
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4695 *
                                                  4696 **       Install program check routine to catch the page fault
                                                  4697 *
00001188  9202 9FFF                       000021FF 4698          MVI   SUBTEST,X'02'
0000118C  D207 2FC8 0068      000011C8   00000068 4699          MVC   SVPGMNEW,PGMNPSW   Save original Program New PSW
00001192  4100 2FD8                       000011D8 4700          LA    R0,MYPGMNEW        Point to temporary Pgm New routine
00001196  5000 006C                       0000006C 4701          ST    R0,PGMNPSW+4       Point Program New PSW to our routine
0000119A  9208 0069                       00000069 4702          MVI   PGMNPSW+1,X'08'    Make it a non-disabled-wait PSW!
                                                  4703 *
                                                  4704 **       Run the test: should cause a page fault
                                                  4705 *
0000119E  920F 9FFF                       000021FF 4706          MVI   SUBTEST,X'0F'
000011A2  B700 9380                       00001580 4707          LCTL  R0,R0,CRLREG0      Switch to DAT mode
000011A6  B711 9384                       00001584 4708          LCTL  R1,R1,CTLREG1      Switch to DAT mode
000011AA  8200 2FD0                       000011D0 4709          LPSW  DATONPSW           Switch to DAT mode
000011AE  4700 2FAE                       000011AE 4710 BEGDATON NOP   *                 (pad)
000011B2  4700 2FB2                       000011B2 4711          NOP   *                 (pad)
000011B6  B20D 0000                       00000000 4712          PTLB  ,                 Purge Translation Lookaside Buffer
000011BA  0FAC                                     4713 PFINSADR CLCL  R10,R12           Page Fault should occur on this instr
000011BC  07000700                                 4714          CNOP  0,8                    (align to doubleword)
000011C0  00000000 00000000                        4715 LOGICERR DC    D'0'                   We should never reach here!
000011C8  00000000 00000000                        4716 SVPGMNEW DC    D'0'                   Original Program New PSW
000011D0  04080000 000011AE                        4717 DATONPSW DC    XL4'04080000',A(BEGDATON)  Enable DAT PSW
                                                  4718 *
                                                  4719 **       Temporary Program New routine:
                                                  4720 **       Restore original Program New PSW
                                                  4721 *
000011D8  D207 0068 2FC8      00000068   000011C8 4722 MYPGMNEW MVC   PGMNPSW,SVPGMNEW   Restore original Program New PSW
                                                  4723 *
                                                  4724 **       Verify Program Check occurred on expected instruction
                                                  4725 *
000011DE  9268 9FFF                       000021FF 4726          MVI   SUBTEST,X'68'
000011E2  D503 935C 002C      0000155C   0000002C 4727          CLC   =A(PFINSADR),PGMOPSW+4   Program Check where expected?
000011E8  4770 9250                       00001450 4728          BNE   FAILTEST                 No?! Something is VERY WRONG!
                                                  4729 *
                                                  4730 **       Verify Program Check was indeed a page fault
                                                  4731 *
000011EC  9211 9FFF                       000021FF 4732          MVI   SUBTEST,X'11'
000011F0  9511 008F                       0000008F 4733          CLI   PGMICODE+1,X'11'   Verify it's a Page Fault interrupt
000011F4  4770 9250                       00001450 4734          BNE   FAILTEST           If not then something is VERY WRONG!
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4736 *
                                          4737 **       Verify Page Fault occurred on expected Page
                                          4738 *
000011F8  9205 9FFF                 000021FF  4739          MVI   SUBTEST,X'05'
000011FC  5800 0090                 00000090  4740          L     R0,PGMTRX           Get where Page Fault occurred
00001200  8800 000C                 0000000C  4741          SRL   R0,12
00001204  8900 000C                 0000000C  4742          SLL   R0,12

00001208  8860 000C                 0000000C  4744          SRL   R6,12               Where Page Fault is expected
0000120C  8960 000C                 0000000C  4745          SLL   R6,12

00001210  1506                              4747          CLR   R0,R6               Page Fault occur on expected Page?
00001212  4770 9250                 00001450  4748          BNE   FAILTEST            No? Then something is very wrong!
                                          4749 *
                                          4750 **       Verify CLCL instruction registers were updated as expected
                                          4751 *
00001216  9206 9FFF                 000021FF  4752          MVI   SUBTEST,X'06'
0000121A  55A0 9EB4                 000020B4  4753          CL    R10,CLCLPF          (op1 greater than starting value?)
0000121E  47D0 9250                 00001450  4754          BNH   FAILTEST
00001222  55C0 9EBC                 000020BC  4755          CL    R12,CLCLPF+4+4      (op2 greater than starting value?)
00001226  47D0 9250                 00001450  4756          BNH   FAILTEST

0000122A  9207 9FFF                 000021FF  4758          MVI   SUBTEST,X'07'
0000122E  15BD                              4759          CLR   R11,R13             (same remaining lengths?)
00001230  4770 9250                 00001450  4760          BNE   FAILTEST
00001234  55B0 9EB8                 000020B8  4761          CL    R11,CLCLPF+4        (op1 len less than starting value?)
00001238  47B0 9250                 00001450  4762          BNL   FAILTEST
0000123C  55D0 9EC0                 000020C0  4763          CL    R13,CLCLPF+4+4+4    (op2 len less than starting value?)
00001240  47B0 9250                 00001450  4764          BNL   FAILTEST

00001244  9208 9FFF                 000021FF  4766          MVI   SUBTEST,X'08'
00001248  55A0 9F54                 00002154  4767          CL    R10,ECLCLPF         (stop before end?)
0000124C  47B0 9250                 00001450  4768          BNL   FAILTEST

00001250  9209 9FFF                 000021FF  4770          MVI   SUBTEST,X'09'
00001254  15A6                              4771          CLR   R10,R6              (stop at or before expected page?)
00001256  4720 9250                 00001450  4772          BH    FAILTEST

0000125A  9210 9FFF                 000021FF  4774          MVI   SUBTEST,X'10'
0000125E  187A                              4775          LR    R7,R10              (op1 stopped address)
00001260  1E7B                              4776          ALR   R7,R11              (add remaining length)
00001262  1576                              4777          CLR   R7,R6               (would remainder reach PF page?)
00001264  47D0 9250                 00001450  4778          BNH   FAILTEST

00001268  07FE                              4780          BR    R14                 Success!
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4782 ********************************************************************************
                                          4783 *        RPTSPEED                  Report instruction speed
                                          4784 ********************************************************************************

0000126A  50F0 9140                 00001340  4786 RPTSPEED ST    R15,RPTSAVE        Save return address
0000126E  45F0 9144                 00001344  4787          BAL   R15,CALCDUR        Calculate duration
                                          4788 *
00001272  4150 93A8                 000015A8  4789          LA    R5,OVERHEAD        Subtract overhead
00001276  4160 93A0                 000015A0  4790          LA    R6,DURATION        From raw timing
0000127A  4170 93A0                 000015A0  4791          LA    R7,DURATION        Yielding true instruction timing
0000127E  45F0 9198                 00001398  4792          BAL   R15,SUBDWORD       Do it
                                          4793 *
00001282  98CD 93A0                 000015A0  4794          LM    R12,R13,DURATION   Convert to...
00001286  8CC0 000C                 0000000C  4795          SRDL  R12,12             ... microseconds
                                          4796 *
0000128A  4EC0 93B0                 000015B0  4797          CVD   R12,TICKSAAA       convert HIGH part to decimal
0000128E  4ED0 93B8                 000015B8  4798          CVD   R13,TICKSBBB       convert LOW  part to decimal
                                          4799 *
00001292  F877 93C0 93B0      000015C0  000015B0  4800          ZAP   TICKSTOT,TICKSAAA            Calculate...
00001298  FC75 93C0 9378      000015C0  00001578  4801          MP    TICKSTOT,=P'4294967296'      ...decimal...
0000129E  FA77 93C0 93B8      000015C0  000015B8  4802          AP    TICKSTOT,TICKSBBB            ...microseconds
                                          4803 *
000012A4  D20B 93FB 9414      000015FB  00001614  4804          MVC   PRTLINE+43(L'EDIT),EDIT          (edit into...
000012AA  DE0B 93FB 93C3      000015FB  000015C3  4805          ED    PRTLINE+43(L'EDIT),TICKSTOT+3     ...print line)
```

```
                                          4807          RAWIO 4,FAIL=FAILIO      Print elapsed time on console
000012B0  9200 300E                 0000000E  4808+         MVI   IOCBSC,X'00'          Clear SC information
000012B4  D201 300A 3006      0000000A  00000006  4809+         MVC   IOCBST,IOCBZERO       Clear accumulated status
000012BA  5810 3000                 00000000  4810+         L     1,IOCBDID             Remember the device ID with which I am working
                                          4811+* Initiate Subchannel-based input/output operation
000012BE  5840 3018                 00000018  4812+         $L    4,IOCBORB             Locate the ORB for the channel subsystem
000012C2  B233 4000                 00000000  4813+         SSCH  0(4)                  Initiate the I/O operation
000012C6  A774 00BD                 00001440  4814+         $BC   B'0111',FAILIO        ..Start function failed, report/handle the error
000012CA  5840 3020                 00000020  4815+         $L    4,IOCBIRB             Locate the IRB storage area
000012CE                      00000000  4816+         USING IRB,4                 Make it addressable

                                          4818+* Wait for I/O operation to present status via an interruption
000012CE                                  4819+IOWT0007 DS    0H  Wait for I/O to complete
000012CE  D207 90F0 0078      000012F0  00000078  4821+         MVC   IOS0008(8),120(0)               Save Input/Output new PSW
000012D4  D207 0078 90E8      00000078  000012E8  4822+         MVC   120(8,0),ION0008              Establish Input/Ouput new PSW
000012DA  8200 90E0                 000012E0  4823+         $LPSW WPSW0008                      Wait for event
000012E0  020A0000 00000000                   4824+WPSW0008 PSW   2,0,2,0,0                     Wait for event
000012E8  00082000 000012F8                   4825+ION0008  PSW   0,0,0,32,IRST0008,24              I/O New PSW: cc==2
000012F0  00000000 00000000                   4826+IOS0008  DC    XL8'00'
                                          4827+* Handle input/output interruption
000012F8                                  4828+IRST0008 DS    0H
000012F8  D207 0078 90F0      00000078  000012F0  4829+         MVC   120(8,0),IOS0008            Restore input/output new PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                         4830+* Process the interruption...
                                         4831+* Validate interruption is for the expected subchannel
000012FE  5510 00B8                 000000B8  4832+         CL    1,IOSSID              Is this the device for which I am waiting?
00001302  A774 FFE6                 000012CE  4833+         $BNE  IOWT0007              ..No, continue waiting for it
                                         4834+* Accumulate interruption information from IRB
00001306  B235 4000                 00000000  4835+         TSCH  0(4)                  Retrive interrupt information
0000130A  A744 FFE2                 000012CE  4836+         $BC   B'0100',IOWT0007      CC1 (not status pending), wait for it to arriv
0000130E  A714 0099                 00001440  4837+         $BC   B'0001',FAILIO        CC3 (not operational), an error then
                                         4838+*                                       CC0 (status was pending), accumulate the status
00001312  D600 300E 4003  0000000E  00000003  4839+         OC    IOCBSC,IRBSCSW+SCSW2  Accumulate status control
00001318  D601 300A 4008  0000000A  00000008  4840+         OC    IOCBST,IRBSCSW+SCSWUS Accumulate device and channel status
0000131E  9104 300E                 0000000E  4841+         TM    IOCBSC,SCSWSPRI       Primary subchannel status?
00001322  A7E4 FFD6                 000012CE  4842+         $BNO  IOWT0007              ..No, wait for primary status
00001326  D203 3010 4004  00000010  00000004  4843+         MVC   IOCBSCCW,IRBSCSW+SCSWCCW  CCW address
0000132C  D201 3016 400A  00000016  0000000A  4844+         MVC   IOCBRCNT,IRBSCSW+SCSWCNT  Residual count
                                         4845+* Test for errors as specified in the IOCB
00001332  910C 300A                 0000000A  4846+         TM    IOCBUS,CSWCE+CSWDE    Channel end and device end both accumulated?
00001336  A7E4 0085                 00001440  4847+         $BNO  FAILIO                Hunh? No CE and DE but do have primary status!
                                         4848+* Input/Output operation successful


0000133A  58F0 9140                 00001340  4850          L     R15,RPTSAVE           Restore return address
0000133E  07FF                               4851          BR    R15                   Return to caller

00001340  00000000                           4853 RPTSAVE  DC    F'0'                  R15 save area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                          4855 ********************************************************************************
                                          4856 *        CALCDUR                   Calculate DURATION
                                          4857 ********************************************************************************

00001344  50F0 9188                       00001388  4859 CALCDUR  ST    R15,CALCRET        Save return address
00001348  9057 918C                       0000138C  4860          STM   R5,R7,CALCWORK     Save work registers
                                          4861 *
0000134C  9867 9390                       00001590  4862          LM    R6,R7,BEGCLOCK     Remove CPU number from clock value
00001350  8C60 0006                       00000006  4863          SRDL  R6,6                       "
00001354  8D60 0006                       00000006  4864          SLDL  R6,6                       "
00001358  9067 9390                       00001590  4865          STM   R6,R7,BEGCLOCK             "
                                          4866 *
0000135C  9867 9398                       00001598  4867          LM    R6,R7,ENDCLOCK     Remove CPU number from clock value
00001360  8C60 0006                       00000006  4868          SRDL  R6,6                       "
00001364  8D60 0006                       00000006  4869          SLDL  R6,6                       "
00001368  9067 9398                       00001598  4870          STM   R6,R7,ENDCLOCK             "
                                          4871 *
0000136C  4150 9390                       00001590  4872          LA    R5,BEGCLOCK        Starting time
00001370  4160 9398                       00001598  4873          LA    R6,ENDCLOCK        Ending time
00001374  4170 93A0                       000015A0  4874          LA    R7,DURATION        Difference
00001378  45F0 9198                       00001398  4875          BAL   R15,SUBDWORD       Calculate duration
                                          4876 *
0000137C  9857 918C                       0000138C  4877          LM    R5,R7,CALCWORK     Restore work registers
00001380  58F0 9188                       00001388  4878          L     R15,CALCRET        Restore return address
00001384  07FF                            4879          BR    R15                Return to caller

00001388  00000000                        4881 CALCRET  DC    F'0'               R15 save area
0000138C  00000000 00000000               4882 CALCWORK DC    3F'0'              R5-R7 save area



                                          4884 ********************************************************************************
                                          4885 *        SUBDWORD                  Subtract two doublewords
                                          4886 *        R5 --> subtrahend, R6 --> minuend, R7 --> result
                                          4887 ********************************************************************************

00001398  90AD 91C0                       000013C0  4889 SUBDWORD STM   R10,R13,SUBDWSAV   Save registers
                                          4890 *
0000139C  98AB 5000                       00000000  4891          LM    R10,R11,0(R5)      Subtrahend  (value to subtract)
000013A0  98CD 6000                       00000000  4892          LM    R12,R13,0(R6)      Minuend     (what to subtract FROM)
000013A4  1FDB                            4893          SLR   R13,R11            Subtract LOW part
000013A6  47B0 91AE                       000013AE  4894          BNM   *+4+4              (branch if no borrow)
000013AA  5FC0 9360                       00001560  4895          SL    R12,=F'1'          (otherwise do borrow)
000013AE  1FCA                            4896          SLR   R12,R10            Subtract HIGH part
000013B0  90CD 7000                       00000000  4897          STM   R12,R13,0(R7)      Store results
                                          4898 *
000013B4  98AD 91C0                       000013C0  4899          LM    R10,R13,SUBDWSAV   Restore registers
000013B8  07FF                            4900          BR    R15                Return to caller

000013C0  00000000 00000000               4902 SUBDWSAV DC    2D'0'              R10-R13 save area
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                         4904 ********************************************************************************
                                         4905 *        Program Initialization
                                         4906 ********************************************************************************

000013D0                                 4908 INIT     DS     0H               Program Initialization

000013D0  4130 92C0                 000014C0  4910          LA     R3,IOCB_009      Point to IOCB
000013D4  5880 3018                 00000018  4911          L      R8,IOCBORB       Point to ORB

000013D8  45F0 9260                 00001460  4913          BAL    R15,IOINIT       Initialize the CPU for I/O operations
000013DC  45F0 926E                 0000146E  4914          BAL    R15,ENADEV       Enable our device making ready for use
000013E0  07FE                           4915          BR     R14              Return to caller




                                         4917 ********************************************************************************
                                         4918 *        Verify CLCL ending register values
                                         4919 * R10-R12 = actual ending values, R5 --> expected ending values
                                         4920 ********************************************************************************

000013E2  90AD 9F64                 00002164  4922 ENDCLCL  STM    R10,R13,CLCLEND     Save actual ending register values
000013E6  D50F 5000 9F64      00000000  00002164  4923          CLC    0(4*4,R5),CLCLEND   Do they have the expected values?
000013EC  4770 9250                 00001450  4924          BNE    FAILTEST            If not then the test has failed
000013F0  07FF                           4925          BR     R15                 Otherwise return to caller




                                         4927 ********************************************************************************
                                         4928 *        MVCINTST
                                         4929 ********************************************************************************

000013F2  98AD 5000                 00000000  4931 MVCINTST LM    R10,R13,0(R5)       a(dst),a(src+(len-1)),a(len-1),a(src)
000013F6  4160 95DF                 000017DF  4932          LA     R6,MVCININ+256-1    Point to end of source
000013FA  1F6C                           4933          SLR    R6,R12              Backup by length amount
000013FC  44C0 920E                 0000140E  4934          EX     R12,MVCINSRC        Initialize source data
00001400  44C0 9214                 00001414  4935          EX     R12,MVCINMVC        Do the Move Inverse
00001404  44C0 921A                 0000141A  4936          EX     R12,MVCINCLC        Compare with expected results
00001408  4770 9250                 00001450  4937          BNE    FAILTEST            FAIL if not the expected value
0000140C  07FF                           4938          BR     R15                 Otherwise return to caller


0000140E  D200 D000 6000      00000000  00000000  4940 MVCINSRC MVC   0(0,R13),0(R6)      Executed Instruction
00001414  E800 A000 B000      00000000  00000000  4941 MVCINMVC MVCIN 0(0,R10),0(R11)     Executed Instruction
0000141A  D500 A000 95E0      00000000  000017E0  4942 MVCINCLC CLC   0(0,R10),MVCINOUT   Executed Instruction
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4944 ************************************************************************
                                                  4945 *        Normal completion or Abnormal termination PSWs
                                                  4946 ************************************************************************


                                                  4948 EOJ      DWAITEND LOAD=YES          Normal completion
00001420                                          4950+EOJ      DS    0H
00001420  8200 9228                     00001428  4951+         LPSW  DWAT0010
00001428  000A0000 00000000                       4952+DWAT0010 PSW   0,0,2,0,X'000000'


                                                  4954 FAILDEV  DWAIT LOAD=YES,CODE=01     ENADEV failed
00001430                                          4955+FAILDEV  DS    0H
00001430  8200 9238                     00001438  4956+         LPSW  DWAT0011
00001438  000A0000 00010001                       4957+DWAT0011 PSW   0,0,2,0,X'010001'


                                                  4959 FAILIO   DWAIT LOAD=YES,CODE=02     RAWIO failed
00001440                                          4960+FAILIO   DS    0H
00001440  8200 9248                     00001448  4961+         LPSW  DWAT0012
00001448  000A0000 00010002                       4962+DWAT0012 PSW   0,0,2,0,X'010002'


                                                  4964 FAILTEST DWAIT LOAD=YES,CODE=BAD    Abnormal termination
00001450                                          4965+FAILTEST DS    0H
00001450  8200 9258                     00001458  4966+         LPSW  DWAT0013
00001458  000A0000 00010BAD                       4967+DWAT0013 PSW   0,0,2,0,X'010BAD'
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                 4969 ************************************************************************
                                                 4970 *        Initialize the CPU for I/O operations
                                                 4971 ************************************************************************

                                                 4973 IOINIT   IOINIT ,
00001460  B766 9268                   00001468  4974+IOINIT   LCTL  6,6,IOMK0014       Enable subchannel subclasses for interruptions
00001464  47F0 926C                   0000146C  4975+         B     IOMK0014+4
00001468                                        4976+IOMK0014 DS    0F
00001468  FF000000                              4977+         DC    XL4'FF000000'         All subchannel subclasses enabled

0000146C  07FF                                  4979          BR    R15                   Return to caller

                                                 4981 ************************************************************************
                                                 4982 *        Enable the device, making it ready for use
                                                 4983 ************************************************************************

                                                 4985 ENADEV   ENADEV ENAOKAY,FAILDEV,REG=4
0000146E  5810 92B4                   000014B4  4986+ENADEV   L     1,FIND0015
00001472  5840 3028                   00000028  4987+         $L    4,IOCBSIB             Locate where the SCHIB is to be stored
00001476                    00000000            4988+         USING SCHIB,4
00001476                                        4989+FINL0015 DS    0H   Retrieve Subchannel Information Block for desired device number
00001476  B234 4000                   00000000  4990+         STSCH 0(4)                  Store the SCHIB for first subchannel
0000147A  A774 FFDB                   00001430  4991+         $BC   B'0111',FAILDEV       Subchannel does not exist and device number not found
0000147E  9101 4005                   00000005  4992+         TM    PMCW1_8,PMCWV         Is the subchannel device number valid?
00001482  A784 0011                   000014A4  4993+         $BZ   FINN0015              ..No, check the next subchannel
00001486  D501 4006 3004      00000006  00000004  4994+         CLC   PMCWDNUM,IOCBDEV      Is this the device number being sought?
0000148C  A774 000C                   000014A4  4995+         $BNE  FINN0015              ..No, check the next subchannel
                                                 4996+* Subchannel found!
00001490  5010 3000                   00000000  4997+         ST    1,IOCBDID             Remember the subchannel so I/O can be done to it.
00001494  9680 4005                   00000005  4998+         OI    PMCW1_8,PMCWE         Make sure it is enabled so I/O requests accepted
00001498  B232 4000                   00000000  4999+         MSCH  0(4)                  Enable the subchannel to the channel sub-system
0000149C  A784 0010                   000014BC  5000+         $BC   B'1000',ENAOKAY       CC0 (SCHIB updated), device is ready.
000014A0  A7F4 FFC8                   00001430  5001+         $B    FAILDEV               CC1,CC2,CC3 (SCHIB update failed), quit
000014A4                                        5002+FINN0015 DS    0H  Advance to next subchannel
000014A4  4110 1001                   00000001  5003+         LA    1,1(0,1)              Advance to next subchannel
000014A8  5510 92B8                   000014B8  5004+         CL    1,FINM0015            Beyond maximum subchannel
000014AC  A7D4 FFE5                   00001476  5005+         $BNH  FINL0015              ..No, examine the next subchannel
000014B0  A724 FFC0                   00001430  5006+         $BH   FAILDEV               ..Yes, failed to enable the device
000014B4                                        5007+         DROP  4                     Forget SCHIB addressing
000014B4  00010000                              5008+FIND0015 DC    A(X'00010000')        First subchannel subsystem ID
000014B8  0001FFFF                              5009+FINM0015 DC    A(X'0001FFFF')        Last subchannel subsystem ID

000014BC  07FF                                  5011 ENAOKAY  BR    R15                   Return to caller
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5013 ********************************************************************************
                                                    5014 *         Structure used by RAWIO identifying
                                                    5015 *         the device and operation being performed
                                                    5016 ********************************************************************************


                                                    5018 IOCB_009 IOCB  X'009',CCW=CONPGM
000014C0  00000000                                  5019+IOCB_009 DC    A(0)            +0 Device Identifier (supplied by ENADEV macro)
000014C4  0009                                      5020+         DC    AL2(X'009')     +4 Device address or device number
000014C6  0000                                      5021+         DC    H'0'            +6 Must be zeros
000014C8  D3                                        5022+         DC    AL1(X'D3')      +8 Default detected unit errors
000014C9  3F                                        5023+         DC    AL1(X'3F')      +9 Default detected channel errors
000014CA  0000                                      5024+         DC    HL2'0'          +10 Accumulated unit and channel errors
000014CC  0000                                      5025+         DC    HL2'0'          +12 Tested unit and channel status
000014CE  00                                        5026+         DC    XL1'00'         +14 Accumulated subchannel status control from SCSW
000014CF  80                                        5027+         DC    XL1'80'         +15 Default unsoliticed wait condition
000014D0  00000000                                  5028+         DC    F'0'            +16 I/O status CCW address
000014D4  00000000                                  5029+         DC    F'0'            +20 residual count
000014D8  00001530                                  5030+         DC    A(IORB0016)     +24  Address where ORB is located
000014DC  00000000                                  5031+         DC    A(0)            +28  reserved
000014E0  000014F0                                  5032+         DC    A(IIRB0016)     +32 Address where IRB stored
000014E4  00000000                                  5033+         DC    A(0)            +36 reserved
000014E8  000014F0                                  5034+         DC    A(IIRB0016)     +40 Address where SCHIB stored
000014EC  00000000                                  5035+         DC    A(0)            +44 reserved
000014F0  00000000 00000000                         5036+IIRB0016 DC    16F'0'              Embedded shared IRB and SCHIB area
00001530                                            5038+IORB0016 DS    0XL12
00001530  00000000                                  5039+         DC    A(0)            Word 0 - Interruption Parameter
00001534  00                                        5040+         DC    AL1((0)*16+B'0000')  Word 1, bits 0-7
00001535  80                                        5041+         DC    BL1'10000000'   Word 1, bits 8-15
00001536  FF                                        5042+         DC    AL1(255)        Word 1, bits 16-23
00001537  00                                        5043+         DC    BL1'00000000'    Word 1, bits 24-31
00001538  000015C8                                  5044+         DC    AL4(CONPGM)     Word 2 - CCW address
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5046 ********************************************************************************
                                                    5047 *        Working Storage
                                                    5048 ********************************************************************************


0000153C                                            5050          LTORG ,                  Literals pool
0000153C  AABBCCDD                                  5051                =A(REG2PATT)
00001540  00000000                                  5052                =F'0'
00001544  00050000                                  5053                =A(00+(5*K64))
00001548  00150000                                  5054                =A(MB+(5*K64))
0000154C  00003000                                  5055                =A(SEGTABLS)
00001550  00003080                                  5056                =A(PAGETABS)
00001554  00001000                                  5057                =A(PAGE)
00001558  00005000                                  5058                =A(PFPGBYTS)
0000155C  000011BA                                  5059                =A(PFINSADR)
00001560  00000001                                  5060                =F'1'
00001564  C3D3C340 40                               5061                =CL5'CLC'
00001569  C3D3C3D3 40                               5062                =CL5'CLCL'
0000156E  D4E5C3C9 D5                               5063                =CL5'MVCIN'
00001573  E3D9E340 40                               5064                =CL5'TRT'
00001578  04294967 296C                             5065                =P'4294967296'

                            00000400  00000001  5067 K        EQU   1024             One KB
                            00001000  00000001  5068 PAGE     EQU   (4*K)            Size of one page
                            00010000  00000001  5069 K64      EQU   (64*K)           64 KB
                            00100000  00000001  5070 MB       EQU   (K*K)             1 MB

                            000021FE  00000001  5072 TESTADDR EQU   (2*PAGE+X'200'-2)  Where test/subtest numbers will go
                            000021FD  00000001  5073 TIMEADDR EQU   (TESTADDR-1)       Address of timing tests option flag

                            00200000  00000001  5075 MAINSIZE EQU   (2*MB)                   Minimum required storage size
                            00000020  00000001  5076 NUMPGTBS EQU   ((MAINSIZE+K64-1)/K64)   Number of Page Tables needed
                            00000002  00000001  5077 NUMSEGTB EQU   ((NUMPGTBS*4)/(16*4))    Number of Segment Tables
                            00003000  00000001  5078 SEGTABLS EQU   (3*PAGE)                 Segment Tables Origin
                            00003080  00000001  5079 PAGETABS EQU   (SEGTABLS+(NUMPGTBS*4))  Page Tables Origin
00001580  00B00060                                  5080 CRLREG0  DC    0A(0),XL4'00B00060'      Control Register 0
00001584  00003002                                  5081 CTLREG1  DC    A(SEGTABLS+NUMSEGTB)     Control Register 1

00001588  00002710                                  5083 NUMLOOPS DC    F'10000'         10,000 * 100 = 1,000,000

00001590  BBBBBBBB BBBBBBBB                        5085 BEGCLOCK DC    0D'0',8X'BB'     Begin
00001598  EEEEEEEE EEEEEEEE                        5086 ENDCLOCK DC    0D'0',8X'EE'     End
000015A0  DDDDDDDD DDDDDDDD                        5087 DURATION DC    0D'0',8X'DD'     Diff
000015A8  FFFFFFFF FFFFFFFF                        5088 OVERHEAD DC    0D'0',8X'FF'     Overhead

000015B0  00000000 0000000C                        5090 TICKSAAA DC    PL8'0'           Clock ticks high part
000015B8  00000000 0000000C                        5091 TICKSBBB DC    PL8'0'           Clock ticks low part
000015C0  00000000 0000000C                        5092 TICKSTOT DC    PL8'0'           Total clock ticks

000015C8  09000044 000015D0                        5094 CONPGM   CCW1  X'09',PRTLINE,0,L'PRTLINE
000015D0  40404040 40404040                        5095 PRTLINE  DC    C'         1,000,000 iterations of XXXXX took 999,999,999 microseconds'
00001614  40202020 6B202020                        5096 EDIT     DC    X'402020206B2020206B202120'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   5098 ************************************************************************
                                                   5099 *        CLC Test Parameters:   A(operand-1),A(operand-2)
                                                   5100 ************************************************************************

00001620  00010000 00110000                        5102 CLC1     DC    A(1*K64),A(MB+(1*K64))                          both equal
00001628  00010000 00110000                        5103 CLC2     DC    A(1*K64),A(MB+(1*K64))                          both equal
00001630  0000FFF4 0010FFDE                        5104 CLCBOTH  DC    A(1*K64-12),A(MB+(1*K64)-34)                    both equal
00001638  00010000 0010FFDE                        5105 CLCOP2   DC    A(1*K64),A(MB+(1*K64)-34)                       both equal

00001640  00020000 00120000                        5107 CLC4     DC    A(2*K64),A(MB+(2*K64))                            op1 HIGH
00001648  00030000 00130000                        5108 CLC8     DC    A(3*K64),A(MB+(3*K64))                            op1 LOW!
00001650  00040000 00140000                        5109 CLC256   DC    A(4*K64),A(MB+(4*K64))                            op1 HIGH
00001658  0004FFF4 00150000                        5110 CLCOP1   DC    A(5*K64-12),A(MB+(5*K64))                         op1 HIGH


                                                   5112 ************************************************************************
                                                   5113 *        MVCIN Test Parameters
                                                   5114 ************************************************************************
                                                   5115          PRINT DATA
00001660  00010000 00110000                        5116 INV1     DC    A(1*K64),A(MB+(1*K64)+1-1),A(1-1),A(MB+(1*K64))
00001668  00000000 00110000
00001670  00020000 00120001                        5117 INV2     DC    A(2*K64),A(MB+(2*K64)+2-1),A(2-1),A(MB+(2*K64))
00001678  00000001 00120000
00001680  00030000 00130003                        5118 INV4     DC    A(3*K64),A(MB+(3*K64)+4-1),A(4-1),A(MB+(3*K64))
00001688  00000003 00130000
00001690  00040000 00140007                        5119 INV8     DC    A(4*K64),A(MB+(4*K64)+8-1),A(8-1),A(MB+(4*K64))
00001698  00000007 00140000
000016A0  00050000 001500FF                        5120 INV256   DC    A(5*K64),A(MB+(5*K64)+256-1),A(256-1),A(MB+(5*K64))
000016A8  000000FF 00150000

000016B0  0005FFF4 001600DD                        5122 INVBOTH  DC    A(6*K64-12),A(MB+(6*K64)-34+256-1),A(256-1),A(MB+(6*K64)-34)
000016B8  000000FF 0015FFDE
000016C0  0006FFF4 001700FF                        5123 INVOP1   DC    A(7*K64-12),A(MB+(7*K64)+256-1),A(256-1),A(MB+(7*K64))
000016C8  000000FF 00170000
000016D0  00080000 001800DD                        5124 INVOP2   DC    A(8*K64),A(MB+(8*K64)-34+256-1),A(256-1),A(MB+(8*K64)-34)
000016D8  000000FF 0017FFDE
                                                   5125          PRINT NODATA
000016E0                                           5126 MVCININ  DC    0XL256'00'
000016E0  00010203 04050607                        5127          DC    XL16'000102030405060708090A0B0C0D0E0F'
000016F0  10111213 14151617                        5128          DC    XL16'101112131415161718191A1B1C1D1E1F'
00001700  20212223 24252627                        5129          DC    XL16'202122232425262728292A2B2C2D2E2F'
00001710  30313233 34353637                        5130          DC    XL16'303132333435363738393A3B3C3D3E3F'
                                                   5131          PRINT OFF
                                                   5144          PRINT ON
000017E0                                           5145 MVCINOUT DC    0XL256'00'
000017E0  FFFEFDFC FBFAF9F8                        5146          DC    XL16'FFFEFDFCFBFAF9F8F7F6F5F4F3F2F1F0'
000017F0  EFEEEDEC EBEAE9E8                        5147          DC    XL16'EFEEEDECEBEAE9E8E7E6E5E4E3E2E1E0'
00001800  DFDEDDDC DBDAD9D8                        5148          DC    XL16'DFDEDDDCDBDAD9D8D7D6D5D4D3D2D1D0'
00001810  CFCECDCC CBCAC9C8                        5149          DC    XL16'CFCECDCCCBCAC9C8C7C6C5C4C3C2C1C0'
                                                   5150          PRINT OFF
                                                   5163          PRINT ON
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    5165 ********************************************************************************
                                                    5166 *        TRTTEST DSECT
                                                    5167 ********************************************************************************


                                                    5169 TRTTEST  DSECT ,


00000000  00000000                                  5171 OP1DATA  DC    A(0)           Pointer to Operand-1 data
00000004  00000000                                  5172 OP1LEN   DC    F'0'           How much data is there - 1
00000008  00000000                                  5173 OP1WHERE DC    A(0)           Where Operand-1 data should be placed


0000000C  00000000                                  5175 OP2DATA  DC    A(0)           Pointer to Operand-2 data
00000010  00000000                                  5176 OP2LEN   DC    F'0'           How much data is there - 1
00000014  00000000                                  5177 OP2WHERE DC    A(0)           Where Operand-2 data should be placed


00000018  00000000                                  5179 EXLEN    DC    F'0'           Operand-1 test length (EX instruction)
0000001C  00000000                                  5180 FAILMASK DC    A(0)           Failure Branch on Condition mask


00000020  00000000 00000000                         5182 ENDREGS  DC    A(0),XL4'00'   Ending R1/R2 register values


                          00000028  00000001  5184 TRTNEXT  EQU   *              Start of next table entry...


                                                    


                          AABBCCDD  00000001  5186 REG2PATT EQU   X'AABBCCDD'    Register 2 starting/ending CC0 value
                          000000DD  00000001  5187 REG2LOW  EQU         X'DD'    (last byte above)


                                                    


                                                    


                          00000000  00003000  5189 CLCLetal CSECT ,


                                                    


                                                    


                                                    
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    5191 ************************************************************************
                                                    5192 *        TRT Testing Control tables   (ref: TRTDSECT)
                                                    5193 ************************************************************************
                                                    5194          PRINT DATA
000018E0                                            5195 TRTCTL   DC    0A(0)    start of table




000018E0  00001A24 00000000                         5197 TRT1     DC    A(TRTOP10),A(001-1),A(00+(1*K64))
000018E8  00010000
000018EC  00001D24 000000FF                         5198          DC    A(TRTOP20),A(256-1),A(MB+(1*K64))
000018F4  00110000
000018F8  00000000 00000007                         5199          DC               A(001-1),A(7) CC0
00001900  00000000 AABBCCDD                         5200          DC                        A(0),A(REG2PATT)



00001908  00001A24 00000000                         5202 TRT2     DC    A(TRTOP10),A(002-2),A(00+(2*K64))
00001910  00020000
00001914  00001D24 000000FF                         5203          DC    A(TRTOP20),A(256-1),A(MB+(2*K64))
0000191C  00120000
00001920  00000001 00000007                         5204          DC               A(002-1),A(7) CC0
00001928  00000000 AABBCCDD                         5205          DC                        A(0),A(REG2PATT)



00001930  00001A24 00000003                         5207 TRT4     DC    A(TRTOP10),A(004-1),A(00+(3*K64))
00001938  00030000
0000193C  00001D24 000000FF                         5208          DC    A(TRTOP20),A(256-1),A(MB+(3*K64))
00001944  00130000
00001948  00000003 00000007                         5209          DC               A(004-1),A(7) CC0
00001950  00000000 AABBCCDD                         5210          DC                        A(0),A(REG2PATT)



00001958  00001A24 00000007                         5212 TRT8     DC    A(TRTOP10),A(008-1),A(00+(4*K64))
00001960  00040000
00001964  00001D24 000000FF                         5213          DC    A(TRTOP20),A(256-1),A(MB+(4*K64))
0000196C  00140000
00001970  00000007 00000007                         5214          DC               A(008-1),A(7) CC0
00001978  00000000 AABBCCDD                         5215          DC                        A(0),A(REG2PATT)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001980  00001A24 000000FF                        5217 TRT256   DC    A(TRTOP10),A(256-1),A(00+(5*K64))
00001988  00050000
0000198C  00001D24 000000FF                        5218          DC    A(TRTOP20),A(256-1),A(MB+(5*K64))
00001994  00150000
00001998  000000FF 00000007                        5219          DC               A(256-1),A(7) CC0
000019A0  00000000 AABBCCDD                        5220          DC                    A(0),A(REG2PATT)



000019A8  00001B24 000000FF                        5222 TRTBTH   DC    A(TRTOP111),A(256-1),A(00+(6*K64)-12)  both cross page
000019B0  0005FFF4
000019B4  00001E24 000000FF                        5223          DC    A(TRTOP211),A(256-1),A(MB+(6*K64)-34)  both cross page
000019BC  0015FFDE
000019C0  000000FF 0000000B                        5224          DC               A(256-1),A(11) CC1 = stop, scan incomplete
000019C8  00060005 AABBCC11                        5225          DC                    A(00+(6*K64)-12+X'11'),A(REG2PATT-REG2LOW+X'11')



000019D0  00001C24 000000FF                        5227 TRTOP1   DC    A(TRTOP1F0),A(256-1),A(00+(7*K64)-12)  only op1 crosses
000019D8  0006FFF4
000019DC  00001F24 000000FF                        5228          DC    A(TRTOP2F0),A(256-1),A(MB+(7*K64))
000019E4  00170000
000019E8  000000FF 0000000D                        5229          DC               A(256-1),A(13) CC2 = stopped on last byte
000019F0  000700F3 AABBCCF0                        5230          DC                    A(00+(7*K64)-12+255),A(REG2PATT-REG2LOW+X'F0')



000019F8  00001B24 000000FF                        5232 TRTOP2   DC    A(TRTOP111),A(256-1),A(00+(8*K64))
00001A00  00080000
00001A04  00001E24 000000FF                        5233          DC    A(TRTOP211),A(256-1),A(MB+(8*K64)-34)  only op2 crosses
00001A0C  0017FFDE
00001A10  000000FF 0000000B                        5234          DC               A(256-1),A(11) CC1 = stop, scan incomplete
00001A18  00080011 AABBCC11                        5235          DC                    A(00+(8*K64)+X'11'),A(REG2PATT-REG2LOW+X'11')



00001A20  00000000                                 5237          DC    A(0)     end of table
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   5239 ********************************************************************************
                                                   5240 *        TRT op1 scan data...
                                                   5241 ********************************************************************************

00001A24  78125634 78125634                        5243 TRTOP10  DC    64XL4'78125634'    (CC0)
00001A2C  78125634 78125634
00001A34  78125634 78125634
00001A3C  78125634 78125634
00001A44  78125634 78125634
00001A4C  78125634 78125634
00001A54  78125634 78125634
00001A5C  78125634 78125634
00001A64  78125634 78125634
00001A6C  78125634 78125634
00001A74  78125634 78125634
00001A7C  78125634 78125634
00001A84  78125634 78125634
00001A8C  78125634 78125634
00001A94  78125634 78125634
00001A9C  78125634 78125634
00001AA4  78125634 78125634
00001AAC  78125634 78125634
00001AB4  78125634 78125634
00001ABC  78125634 78125634
00001AC4  78125634 78125634
00001ACC  78125634 78125634
00001AD4  78125634 78125634
00001ADC  78125634 78125634
00001AE4  78125634 78125634
00001AEC  78125634 78125634
00001AF4  78125634 78125634
00001AFC  78125634 78125634
00001B04  78125634 78125634
00001B0C  78125634 78125634
00001B14  78125634 78125634
00001B1C  78125634 78125634

00001B24  78125634 78125634                        5245 TRTOP111 DC    04XL4'78125634',X'00110000',59XL4'78125634'    (CC1)
00001B2C  78125634 78125634
00001B34  00110000 78125634
00001B3C  78125634 78125634
00001B44  78125634 78125634
00001B4C  78125634 78125634
00001B54  78125634 78125634
00001B5C  78125634 78125634
00001B64  78125634 78125634
00001B6C  78125634 78125634
00001B74  78125634 78125634
00001B7C  78125634 78125634
00001B84  78125634 78125634
00001B8C  78125634 78125634
00001B94  78125634 78125634
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00001B9C  78125634 78125634
00001BA4  78125634 78125634
00001BAC  78125634 78125634
00001BB4  78125634 78125634
00001BBC  78125634 78125634
00001BC4  78125634 78125634
00001BCC  78125634 78125634
00001BD4  78125634 78125634
00001BDC  78125634 78125634
00001BE4  78125634 78125634
00001BEC  78125634 78125634
00001BF4  78125634 78125634
00001BFC  78125634 78125634
00001C04  78125634 78125634
00001C0C  78125634 78125634
00001C14  78125634 78125634
00001C1C  78125634 78125634

00001C24  78125634 78125634                    5247 TRTOP1F0 DC    63XL4'78125634',X'000000F0'    (CC2)
00001C2C  78125634 78125634
00001C34  78125634 78125634
00001C3C  78125634 78125634
00001C44  78125634 78125634
00001C4C  78125634 78125634
00001C54  78125634 78125634
00001C5C  78125634 78125634
00001C64  78125634 78125634
00001C6C  78125634 78125634
00001C74  78125634 78125634
00001C7C  78125634 78125634
00001C84  78125634 78125634
00001C8C  78125634 78125634
00001C94  78125634 78125634
00001C9C  78125634 78125634
00001CA4  78125634 78125634
00001CAC  78125634 78125634
00001CB4  78125634 78125634
00001CBC  78125634 78125634
00001CC4  78125634 78125634
00001CCC  78125634 78125634
00001CD4  78125634 78125634
00001CDC  78125634 78125634
00001CE4  78125634 78125634
00001CEC  78125634 78125634
00001CF4  78125634 78125634
00001CFC  78125634 78125634
00001D04  78125634 78125634
00001D0C  78125634 78125634
00001D14  78125634 78125634
00001D1C  78125634 000000F0
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   5249 ********************************************************************************
                                                   5250 *        TRT op2 stop tables...
                                                   5251 ********************************************************************************

00001D24  00000000 00000000                        5253 TRTOP20  DC    256X'00'     no stop
00001D2C  00000000 00000000
00001D34  00000000 00000000
00001D3C  00000000 00000000
00001D44  00000000 00000000
00001D4C  00000000 00000000
00001D54  00000000 00000000
00001D5C  00000000 00000000
00001D64  00000000 00000000
00001D6C  00000000 00000000
00001D74  00000000 00000000
00001D7C  00000000 00000000
00001D84  00000000 00000000
00001D8C  00000000 00000000
00001D94  00000000 00000000
00001D9C  00000000 00000000
00001DA4  00000000 00000000
00001DAC  00000000 00000000
00001DB4  00000000 00000000
00001DBC  00000000 00000000
00001DC4  00000000 00000000
00001DCC  00000000 00000000
00001DD4  00000000 00000000
00001DDC  00000000 00000000
00001DE4  00000000 00000000
00001DEC  00000000 00000000
00001DF4  00000000 00000000
00001DFC  00000000 00000000
00001E04  00000000 00000000
00001E0C  00000000 00000000
00001E14  00000000 00000000
00001E1C  00000000 00000000

00001E24  00000000 00000000                        5255 TRTOP211 DC    17X'00',X'11',238X'00'     stop on X'11'
00001E2C  00000000 00000000
00001E34  00110000 00000000
00001E3C  00000000 00000000
00001E44  00000000 00000000
00001E4C  00000000 00000000
00001E54  00000000 00000000
00001E5C  00000000 00000000
00001E64  00000000 00000000
00001E6C  00000000 00000000
00001E74  00000000 00000000
00001E7C  00000000 00000000
00001E84  00000000 00000000
00001E8C  00000000 00000000
00001E94  00000000 00000000
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00001E9C  00000000 00000000
00001EA4  00000000 00000000
00001EAC  00000000 00000000
00001EB4  00000000 00000000
00001EBC  00000000 00000000
00001EC4  00000000 00000000
00001ECC  00000000 00000000
00001ED4  00000000 00000000
00001EDC  00000000 00000000
00001EE4  00000000 00000000
00001EEC  00000000 00000000
00001EF4  00000000 00000000
00001EFC  00000000 00000000
00001F04  00000000 00000000
00001F0C  00000000 00000000
00001F14  00000000 00000000
00001F1C  00000000 00000000

00001F24  00000000 00000000                    5257 TRTOP2F0 DC    240X'00',X'F0',15X'00'     stop on X'F0'
00001F2C  00000000 00000000
00001F34  00000000 00000000
00001F3C  00000000 00000000
00001F44  00000000 00000000
00001F4C  00000000 00000000
00001F54  00000000 00000000
00001F5C  00000000 00000000
00001F64  00000000 00000000
00001F6C  00000000 00000000
00001F74  00000000 00000000
00001F7C  00000000 00000000
00001F84  00000000 00000000
00001F8C  00000000 00000000
00001F94  00000000 00000000
00001F9C  00000000 00000000
00001FA4  00000000 00000000
00001FAC  00000000 00000000
00001FB4  00000000 00000000
00001FBC  00000000 00000000
00001FC4  00000000 00000000
00001FCC  00000000 00000000
00001FD4  00000000 00000000
00001FDC  00000000 00000000
00001FE4  00000000 00000000
00001FEC  00000000 00000000
00001FF4  00000000 00000000
00001FFC  00000000 00000000
00002004  00000000 00000000
0000200C  00000000 00000000
00002014  F0000000 00000000
0000201C  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    5259 ************************************************************************
                                                    5260 *        CLCL Test Parameters
                                                    5261 ************************************************************************

00002024  00060000 00000001                         5263 CLCL1    DC    A(6*K64),A(1),A(MB+(6*K64)),A(1)             both equal
0000202C  00160000 00000001

00002034  00060000 00000002                         5265 CLCL2    DC    A(6*K64),A(2),A(MB+(6*K64)),A(2)             both equal
0000203C  00160000 00000002

00002044  00060000 00000100                         5267 CLCL256  DC    A(6*K64),A(256),A(MB+(6*K64)),A(256)         both equal
0000204C  00160000 00000100

00002054  00060000 00000400                         5269 CLCL1K   DC    A(6*K64),A(K),A(MB+(6*K64)),A(K)             both equal
0000205C  00160000 00000400

00002064  0005FFF4 00010000                         5271 CLCLBOTH DC    A(6*K64-12),A(K64),A(MB+(6*K64)-34),A(K64)   both equal
0000206C  0015FFDE 00010000

00002074  00060000 00001000                         5273 CLCLOP2  DC    A(6*K64),A(PAGE),A(MB+(6*K64)-34),A(K64)     both equal
0000207C  0015FFDE 00010000

00002084  00070000 00000004                         5275 CLCL4    DC    A(7*K64),A(4),A(MB+(7*K64)),A(4)              op1 HIGH
0000208C  00170000 00000004

00002094  00080000 00000008                         5277 CLCL8    DC    A(8*K64),A(8),A(MB+(8*K64)),A(8)              op1 LOW!
0000209C  00180000 00000008

000020A4  0008FFF4 00010000                         5279 CLCLOP1  DC    A(9*K64-12),A(K64),A(MB+(9*K64)),A(PAGE)      op1 HIGH
000020AC  00190000 00001000

000020B4  000A0000 00010000                         5281 CLCLPF   DC    A(10*K64),A(K64),A(MB+(10*K64)),A(K64)      page fault
000020BC  001A0000 00010000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  5283 ********************************************************************
                                                  5284 *        CLCL Expected Ending Register Values
                                                  5285 ********************************************************************

000020C4  00060001 00000000                       5287 ECLCL1   DC    A(6*K64+1),A(0),A(MB+(6*K64)+1),A(0)         both equal
000020CC  00160001 00000000

000020D4  00060002 00000000                       5289 ECLCL2   DC    A(6*K64+2),A(0),A(MB+(6*K64)+2),A(0)         both equal
000020DC  00160002 00000000

000020E4  00060100 00000000                       5291 ECLCL256 DC    A(6*K64+256),A(0),A(MB+(6*K64)+256),A(0)     both equal
000020EC  00160100 00000000

000020F4  00060400 00000000                       5293 ECLCL1K  DC    A(6*K64+K),A(0),A(MB+(6*K64)+K),A(0)         both equal
000020FC  00160400 00000000

00002104  0006FFF4 00000000                       5295 ECLCLBTH DC    A(6*K64-12+K64),A(0),A(MB+(6*K64)-34+K64),A(0) bth equl
0000210C  0016FFDE 00000000

00002114  00061000 00000000                       5297 ECLCLOP2 DC    A(6*K64+PAGE),A(0),A(MB+(6*K64)-34+K64),A(0) both equal
0000211C  0016FFDE 00000000

00002124  00070003 00000001                       5299 ECLCL4   DC    A(7*K64+4-1),A(1),A(MB+(7*K64)+4-1),A(1)       op1 HIGH
0000212C  00170003 00000001

00002134  00080007 00000001                       5301 ECLCL8   DC    A(8*K64+8-1),A(1),A(MB+(8*K64)+8-1),A(1)       op1 LOW!
0000213C  00180007 00000001

00002144  0009FFF3 00000001                       5303 ECLCLOP1 DC    A(9*K64-12+K64-1),A(1),A(MB+(9*K64)+PAGE),A(0) op1 HIGH
0000214C  00191000 00000000

00002154  000B0000 00000000                       5305 ECLCLPF  DC    A(10*K64+K64),A(0),A(MB+(10*K64)+K64),A(0)   page fault
0000215C  001B0000 00000000

00002164  00000000 00000000                       5307 CLCLEND  DC    4F'0'          (actual ending register values)
0000216C  00000000 00000000
                            00000005  00000001    5308 PFPAGE   EQU   5              (page the Page Fault should occur on)
                            00005000  00000001    5309 PFPGBYTS EQU   (PFPAGE*PAGE)  (number of bytes into operand-1)
```

```
  LOC         OBJECT CODE        ADDR1     ADDR2     STMT

                                                     5311 ********************************************************************************
                                                     5312 *        Fixed storage locations
                                                     5313 ********************************************************************************


00002174                       00002174  000021FD  5315          ORG   CLCLetal+TIMEADDR      (s/b @ X'21FD')

000021FD  00                                       5317 TIMEOPT  DC    X'00'      Set to non-zero to run timing tests




000021FE                       000021FE  000021FE  5319          ORG   CLCLetal+TESTADDR      (s/b @ X'21FE', X'21FF')

000021FE  00                                       5321 TESTNUM  DC    X'00'      Test number of active test
000021FF  00                                       5322 SUBTEST  DC    X'00'      Active test sub-test number



00002200                       00002200  00003000  5324          ORG   CLCLetal+SEGTABLS      (s/b @ X'3000')
00003000  00                                       5326 DATTABS  DC    X'00'      Segment and Page Tables will go here...
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5328 ********************************************************************************
                                                    5329 *        IOCB DSECT
                                                    5330 ********************************************************************************

                                                    5332          DSECTS NAME=IOCB
                                                    5334+IOCB     DSECT
                                                    5335+*     Field usage by: CH SC Description (R->program read-only, X->program read/write)
00000000                                            5336+IOCBDID  DS    0F  +0     R  Device Identifier - Subsystem ID for channel subsystem
00000000  0000                                      5337+         DS    H   +0  R      reserved - must be zeros
00000002  0000                                      5338+IOCBDV   DS    H   +2  R      Channel Unit Device address of I/O operation
00000004  0000                                      5339+IOCBDEV  DS    H   +4  X  X  Device address or device number (R after ENADEV)
00000006  0000                                      5340+IOCBZERO DS    H   +6  R  R  Must be zeros
00000008  00                                        5341+IOCBUM   DS    X   +8  X  X  Unit status test mask
00000009  00                                        5342+IOCBCM   DS    X   +9  X  X  Channel status test mask
0000000A                                            5343+IOCBST   DS    0H  +10 X  X  Input/Output unit and channel status accumulation
0000000A  00                                        5344+IOCBUS   DS    X   +10 R  R  Accumulated unit status
0000000B  00                                        5345+IOCBCS   DS    X   +11 R  R  Accumulated channel status
0000000C  00                                        5346+IOCBUT   DS    X   +14 R  R  Used to test unit status
0000000D  00                                        5347+IOCBCT   DS    X   +13 R  R  Used to test channel status
0000000E  00                                        5348+IOCBSC   DS    X   +14    R  Accumulted subchanel status control
0000000F  00                                        5349+IOCBWAIT DS    X   +15 X  X  Recognized unsolicited interruption unit status events
00000010  00000000                                  5350+IOCBSCCW DS    A   +16 R  R  I/O status CCW address
00000014                                            5351+IOCBSCNT DS    0F  +20 R  R  I/O status residual count as a positive full word
00000014  0000                                      5352+         DS    H   +20 R     reserved must be zeros
00000016  0000                                      5353+IOCBRCNT DS    H   +22 R     I/O status residual count as an unsigned halfword
00000018                                            5354+IOCBCAW  DS    0A  +24 X     Channel Address word
00000018  00000000 00000000                         5355+IOCBORB  DS    AD  +24    X  Address of the ORB for channel subsystem I/O
00000020  00000000 00000000                         5356+IOCBIRB  DS    AD  +32    X  Channel subsystem IRB address
00000028  00000000 00000000                         5357+IOCBSIB  DS    AD  +40    X  Channel subsystem SCHIB address
                            00000030  00000001      5358+IOCBL    EQU   *-IOCB  Length of IOCB control block (48) without embedded structures
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   5360 ********************************************************************************
                                                   5361 *        ORB DSECT
                                                   5362 ********************************************************************************

                                                   5364          DSECTS NAME=ORB
                                                   5366+ORB      DSECT
00000000  00000000                                 5367+ORBPARM  DC    F'0'     Word 0, bits 0-31

00000004  00                                       5369+ORB1_0   DC    X'00'    Word 1, bits 0-7
                             000000F0  00000001    5370+ORBKEYM  EQU   X'F0'    Word 1, bits 0-3   - Storage Key Mask
                             00000008  00000001    5371+ORBS     EQU   X'08'    Word 1, bit 4      - Suspend Control
                             00000004  00000001    5372+ORBC     EQU   X'04'    Word 1, bit 5      - Streaming Mode Control
                             00000002  00000001    5373+ORBM     EQU   X'02'    Word 1, bit 6      - Modification Control
                             00000001  00000001    5374+ORBY     EQU   X'01'    Word 1, bit 7      - Synchronization Control

00000005  00                                       5376+ORB1_8   DC    X'00'    Word 1, bits 8-15
                             00000080  00000001    5377+ORBF     EQU   X'80'    Word 1, bit 8      - CCW Format-Control
                             00000040  00000001    5378+ORBP     EQU   X'40'    Word 1, bit 9      - Pre-fetch control
                             00000020  00000001    5379+ORBI     EQU   X'20'    Word 1, bit 10     - Initial-status Interruption Control
                             00000010  00000001    5380+ORBA     EQU   X'10'    Word 1, bit 11     - Address Limit Checking Control
                             00000008  00000001    5381+ORBU     EQU   X'08'    Word 1, bit 12     - Suppress-suspended-interruption control
                             00000004  00000001    5382+ORBB     EQU   X'04'    Word 1, bit 13     - Channel-Program-Type Control
                             00000002  00000001    5383+ORBH     EQU   X'02'    Word 1, bit 14     - Format 2-IDAW Control
                             00000001  00000001    5384+ORBT     EQU   X'01'    Word 1, bit 15     - 2K-IDAW control
00000006  00                                       5385+ORBLPM   DC    X'00'    Word 1, bits 16-23 - Logical Path Mask
00000007  00                                       5386+ORRB1_24 DC    X'00'    Word 1, bits 24-31
                             00000080  00000001    5387+ORBL     EQU   X'80'    Word 1, bit 24     - Incorrect Length Suppression Mode
                             0000007F  00000001    5388+ORBRSV3  EQU   X'7F'    Word 1, bits 25-31 - reserved must be zeros
                             00000040  00000001    5389+ORBD     EQU   X'40'    Word 1, bit 25     - MIDAW Addressing Control
                             0000003E  00000001    5390+ORBRSV26 EQU   X'3E'    Word 1, bits 26-30 - reserved must be zeros
                             0000007E  00000001    5391+ORBRSV25 EQU   X'7E'    Word 1, bits 25-30 - reserved must be zeros
                             00000001  00000001    5392+ORBX     EQU   X'01'    Word 1, bit 31     - ORB-extension control

00000008  00000000                                 5394+ORBCCW   DC    A(0)     Word 2, bits 1-31  - Channel Program Address
                             00000080  00000001    5395+ORBRSV4  EQU   X'80'    Word 2, bit 0      - reserved must be zero
                             0000000C  00000001    5396+ORBLEN   EQU   *-ORB Length of standard ORB
                                                   5397+* Extended ORB fields
0000000C  00                                       5398+ORBCSS   DC    X'00'    Word 3, bits 0-7   - Channel Subsystem Priority
0000000D  00                                       5399+ORBRSV5  DC    X'00'    Word 3, bits 8-15  - reserved must be zeros
0000000E                                           5400+ORBPGM   DC    0X'00'   Word 3, bits 16-23 - Transport mode reserves for program us
0000000E  00                                       5401+ORBCU    DC    X'00'    Word 3, bits 16-23 - Control Unit Priority
0000000F  00                                       5402+ORBRSV6  DC    X'00'    Word 3, bits 24-31 - reserved must be zeros
00000010  00000000 00000000                        5403+ORBRSV7  DC    XL16'00' Words 4-7          - reserved must be zeros
00000018  00000000 00000000
                             00000020  00000001    5404+ORBXLEN  EQU   *-ORB Length of extended ORB
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  5407 ********************************************************************************
                                                  5408 *        IRB DSECT
                                                  5409 ********************************************************************************

                                                  5411          DSECTS NAME=IRB
                                                  5413+IRB      DSECT Interruption          Response Block
00000000  00000000 00000000                       5414+IRBSCSW  DC    XL12'00' Words 0-2 - Subchannel Status Word (Defined by DSECT SCSW)
00000008  00000000
0000000C  00000000 00000000                       5415+IRBESW   DC    XL20'00' Words 3-7 - Extended Status Word
00000014  00000000 00000000
0000001C  00000000
00000020  00000000 00000000                       5416+IRBECW   DC    XL32'00' Words 8-15 - Extended Control Word
00000028  00000000 00000000
00000030  00000000 00000000
00000038  00000000 00000000
                             00000040  00000001  5417+IRBL     EQU   *-IRB    IRB Length
00000040  00000000 00000000                       5418+IRBEMW   DC    XL32'00' Words 16-23 - Extended Measurement Word
00000048  00000000 00000000
00000050  00000000 00000000
00000058  00000000 00000000
                             00000060  00000001  5419+IRBXL    EQU   *-IRB    Extended IRB Length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  5422 ********************************************************************************
                                                  5423 *        SCSW DSECT
                                                  5424 ********************************************************************************

                                                  5426          DSECTS NAME=SCSW
                                                  5428+SCSW     DSECT Subchannel          Status Word
00000000  00                                      5429+SCSWFLAG DC    X'00'    Flags
                          000000F0  00000001      5430+SCSWKEYM EQU   X'F0'    Storage Key Mask of subchannel storage key
                          00000008  00000001      5431+SCSWSUSC EQU   X'08'    Suspend Control
                          00000004  00000001      5432+SCSWESWF EQU   X'04'    Extended Status Word Format
                          00000003  00000001      5433+SCSWDCCM EQU   X'03'    Deferred condiont code mask
                          00000000  00000001      5434+SCSWDCC0 EQU   X'00'    Normal I/O interruption
                          00000001  00000001      5435+SCSWDCC1 EQU   X'01'    Deferred condition code is 1
                          00000003  00000001      5436+SCSWDCC3 EQU   X'03'    Deferred condition code is 3

00000001  00                                      5438+SCSWCTLS DC    X'00'    General Controls
                          00000080  00000001      5439+SCSWCCWF EQU   X'80'    CCW Format control when ...
                          00000040  00000001      5440+SCSWCCWP EQU   X'40'    CCW Prefetch Control
                          00000020  00000001      5441+SCSWISIC EQU   X'20'    Initial-Status-Interruption Control
                          00000010  00000001      5442+SCSWALKC EQU   X'10'    Address-Limit-Checking Control
                          00000008  00000001      5443+SCSWSSIC EQU   X'08'    Suppress suspended interruption
                          00000004  00000001      5444+SCSW0CC  EQU   X'04'    Zero-Condition Code
                          00000002  00000001      5445+SCSWECWC EQU   X'02'    Extended Control Word control
                          00000001  00000001      5446+SCSWPNOP EQU   X'01'    Path Not Operational

00000002  00                                      5448+SCSW1    DC    X'00'    Control Byte 1
                          00000070  00000001      5449+SCSWFM   EQU   X'70'    Functional Control Mask
                          00000040  00000001      5450+SCSWFS   EQU   X'40'    Function Control - Start Function
                          00000020  00000001      5451+SCSWFH   EQU   X'20'    Function Control - Halt Function
                          00000010  00000001      5452+SCSWFC   EQU   X'10'    Function Control - Clear Function
                          00000008  00000001      5453+SCSWARP  EQU   X'08'    Activity Control - Resume pending
                          00000004  00000001      5454+SCSWASP  EQU   X'04'    Activity Control - Start pending
                          00000002  00000001      5455+SCSWAHP  EQU   X'02'    Activity Control - Halt pending
                          00000001  00000001      5456+SCSWACP  EQU   X'01'    Activity Control - Clear pending
00000003  00                                      5457+SCSW2    DC    X'00'    Control Byte 2
                          00000080  00000001      5458+SCSWASA  EQU   X'80'    Activity Control - Subchannel Active
                          00000040  00000001      5459+SCSWADA  EQU   X'40'    Activity Control - Device Active
                          00000020  00000001      5460+SCSWASUS EQU   X'20'    Activity Control - Suspended
                          00000010  00000001      5461+SCSWSAS  EQU   X'10'    Status Control   - Alert Status
                          00000008  00000001      5462+SCSWSINT EQU   X'08'    Status Control   - Intermediate Status
                          00000004  00000001      5463+SCSWSPRI EQU   X'04'    Status Control   - Primary Status
                          00000002  00000001      5464+SCSWSSEC EQU   X'02'    Status Control   - Secondary Status
                          00000001  00000001      5465+SCSWSPEN EQU   X'01'    Status Control   - Status Pending

00000004  00000000                                5467+SCSWCCW  DC    A(0)     CCW Address

00000008  00                                      5469+SCSWUS   DC    X'00'    Unit Status
                          00000080  00000001      5470+SCSWATTN EQU   X'80'    Attention
                          00000040  00000001      5471+SCSWSM   EQU   X'40'    Status modifier
                          00000020  00000001      5472+SCSWCUE  EQU   X'20'    Control-unit end
                          00000010  00000001      5473+SCSWBUSY EQU   X'10'    Busy
                          00000008  00000001      5474+SCSWCE   EQU   X'08'    Channel end
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                               00000004  00000001 5475+SCSWDE   EQU   X'04'    Device end
                               00000002  00000001 5476+SCSWUC   EQU   X'02'    Unit check
                               00000001  00000001 5477+SCSWUX   EQU   X'01'    Unit exception

00000009  00                                      5479+SCSWCS   DC    X'00'    Channel Status
                               00000080  00000001 5480+SCSWPCI  EQU   X'80'    Program-controlled interruption
                               00000040  00000001 5481+SCSWIL   EQU   X'40'    Incorrect length
                               00000020  00000001 5482+SCSWPRGM EQU   X'20'    Program check
                               00000010  00000001 5483+SCSWPROT EQU   X'10'    Protection Check
                               00000008  00000001 5484+SCSWCDAT EQU   X'08'    Channel-data check
                               00000004  00000001 5485+SCSWCCTL EQU   X'04'    Channel-control check
                               00000002  00000001 5486+SCSWICTL EQU   X'02'    Interface-control check
                               00000001  00000001 5487+SCSWCHNG EQU   X'01'    Chaining check

0000000A  0000                                    5489+SCSWCNT  DC    H'0'     Residual CCW count
                               0000000C  00000001 5490+SCSWL    EQU   *-SCSW
```

```
  LOC         OBJECT CODE        ADDR1     ADDR2     STMT

                                                     5493 ************************************************************************
                                                     5494 *        (other DSECTS needed by SATK)
                                                     5495 ************************************************************************

                                                     5497          DSECTS PRINT=OFF,NAME=(ASA,SCHIB,CCW0,CCW1,CSW)

                                                     5773          PRINT ON

                                                     5775 ************************************************************************
                                                     5776 *        Register equates
                                                     5777 ************************************************************************

                                00000000  00000001   5779 R0       EQU   0
                                00000001  00000001   5780 R1       EQU   1
                                00000002  00000001   5781 R2       EQU   2
                                00000003  00000001   5782 R3       EQU   3
                                00000004  00000001   5783 R4       EQU   4
                                00000005  00000001   5784 R5       EQU   5
                                00000006  00000001   5785 R6       EQU   6
                                00000007  00000001   5786 R7       EQU   7
                                00000008  00000001   5787 R8       EQU   8
                                00000009  00000001   5788 R9       EQU   9
                                0000000A  00000001   5789 R10      EQU   10
                                0000000B  00000001   5790 R11      EQU   11
                                0000000C  00000001   5791 R12      EQU   12
                                0000000D  00000001   5792 R13      EQU   13
                                0000000E  00000001   5793 R14      EQU   14
                                0000000F  00000001   5794 R15      EQU   15

                                                     5796          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
ASA	4	00000000	512	5501	3537
ASBEGIN	U	00000000	1	5502	5507 5549 5585 5594 5612 5619 5625 5629 5633 5639 5656
ASEND	U	00000200	1	5655	5656
ASLENGTH	U	00000200	1	5656	
BCEXTCOD	H	0000001A	2	5519	
BCIOCOD	H	0000003A	2	5527	
BCMCKCOD	H	00000032	2	5525	
BCPGMCOD	H	0000002A	2	5523	
BCSVCCOD	H	00000022	2	5521	
BEGCLOCK	D	00001590	8	5085	3892 3902 4042 4155 4385 4395 4527 4537 4862 4865 4872
BEGDATON	I	000011AE	4	4710	4717
BEGIN	I	00000200	2	3543	3512 3538 3539 3803 3872
CALCDUR	I	00001344	4	4859	3896 4149 4389 4531 4787
CALCRET	F	00001388	4	4881	4859 4878
CALCWORK	F	0000138C	4	4882	4860 4877
CAW	F	00000048	4	5531	
CAWADDR	R	00000049	3	5534	
CAWKEY	X	00000048	1	5532	
CAWSUSP	U	00000008	1	5533	
CCW0	4	00000000	8	5660	5666
CCW0ADDR	R	00000001	3	5662	
CCW0CNT	H	00000006	2	5665	
CCW0CODE	X	00000000	1	5661	
CCW0FLGS	X	00000004	1	5663	
CCW0L	U	00000008	1	5666	
CCW1	4	00000000	8	5678	5683
CCW1ADDR	A	00000004	4	5682	
CCW1CNT	H	00000002	2	5681	
CCW1CODE	X	00000000	1	5679	
CCW1FLGS	X	00000001	1	5680	
CCW1L	U	00000008	1	5683	
CCWCC	U	00000040	1	5670	
CCWCD	U	00000080	1	5669	
CCWIDA	U	00000004	1	5674	
CCWPCI	U	00000008	1	5673	
CCWSKIP	U	00000010	1	5672	
CCWSLI	U	00000020	1	5671	
CCWSUSP	U	00000002	1	5675	
CHANID	F	000000A8	4	5586	
CLC1	A	00001620	4	5102	3588
CLC2	A	00001628	4	5103	3595
CLC256	A	00001650	4	5109	3578 3617
CLC4	A	00001640	4	5107	3576 3602
CLC8	A	00001648	4	5108	3582 3609
CLCBOTH	A	00001630	4	5104	3624
CLCL1	A	00002024	4	5263	3670
CLCL1K	A	00002054	4	5269	3709
CLCL2	A	00002034	4	5265	3679
CLCL256	A	00002044	4	5267	3886 4036 4044 4045 4048 4049 4050 4051 4052 4053 4054 4055 4056 4057 4058 4059 4060 4061 4062 4063 4064 4065 4066 4067 4068 4069 4070 4071 4072 4073 4074 4075 4076 4077 4078 4079 4080 4081 4082 4083 4084 4085 4086 4087 4088 4089 4090 4091 4092 4093 4094 4095

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     SYMBOL         TYPE    VALUE      LENGTH    DEFN  REFERENCES

                                                      4096  4097  4098  4099  4100  4101  4102  4103  4104  4105  4106  4107  4108
                                                      4109  4110  4111  4112  4113  4114  4115  4116  4117  4118  4119  4120  4121
                                                      4122  4123  4124  4125  4126  4127  4128  4129  4130  4131  4132  4133  4134
                                                      4135  4136  4137  4138  4139  4140  4141  4142  4143  4145  4146  4157  4159
                                                      4163  4165  4167  4169  4171  4173  4175  4177  4179  4181  4183  4185  4187
                                                      4189  4191  4193  4195  4197  4199  4201  4203  4205  4207  4209  4211  4213
                                                      4215  4217  4219  4221  4223  4225  4227  4229  4231  4233  4235  4237  4239
                                                      4241  4243  4245  4247  4249  4251  4253  4255  4257  4259  4261  4263  4265
                                                      4267  4269  4271  4273  4275  4277  4279  4281  4283  4285  4287  4289  4291
                                                      4293  4295  4297  4299  4301  4303  4305  4307  4309  4311  4313  4315  4317
                                                      4319  4321  4323  4325  4327  4329  4331  4333  4335  4337  4339  4341  4343
                                                      4345  4347  4349  4351  4353  4355  4358
CLCL4                A     00002084           4  5275  3652  3689
CLCL8                A     00002094           4  5277  3662  3700
CLCLBOTH             A     00002064           4  5271  3718
CLCLEND              F     00002164           4  5307  4922  4923
CLCLETAL             J     00000000       12289  3494  3497  3504  3511  3513  5315  5319  5324
CLCLOP1              A     000020A4           4  5279  3657  3728
CLCLOP2              A     00002074           4  5273  3737
CLCLPF               A     000020B4           4  5281  4658  4684  4753  4755  4761  4763
CLCOP1               A     00001658           4  5110  3580  3631
CLCOP2               A     00001638           4  5105  3638
CODE                 2     00000000       12289  3494
CONPGM               W     000015C8           8  5094  5044
CPUID                U     0000031B           1  5658
CRLREG0              A     00001580           4  5080  4707
CSW                  F     00000040           8  5530
CSWATTN              U     00000080           1  5700
CSWBUSY              U     00000010           1  5703
CSWCCTL              U     00000004           1  5715
CSWCCW               R     00000001           3  5697
CSWCDAT              U     00000008           1  5714
CSWCE                U     00000008           1  5704  4846
CSWCHNG              U     00000001           1  5717
CSWCNT               H     00000006           2  5719
CSWCS                X     00000005           1  5709
CSWCUE               U     00000020           1  5702
CSWDCC0              U     00000000           1  5693
CSWDCC1              U     00000001           1  5694
CSWDCC3              U     00000003           1  5695
CSWDCCM              U     00000003           1  5692
CSWDE                U     00000004           1  5705  4846
CSWFLAG              X     00000000           1  5687
CSWFMT               4     00000000           8  5686  5720
CSWFMTL              U     00000008           1  5720
CSWICTL              U     00000002           1  5716
CSWIL                U     00000040           1  5711
CSWKEYM              U     000000F0           1  5688
CSWLOG               U     00000004           1  5691
CSWPCI               U     00000080           1  5710
CSWPRGM              U     00000020           1  5712
CSWPROT              U     00000010           1  5713
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
CSWSM	U	00000040	1	5701	
CSWSUSP	U	00000008	1	5690	
CSWUC	U	00000002	1	5706	
CSWUS	X	00000004	1	5699	
CSWUX	U	00000001	1	5707	
CTLREG1	A	00001584	4	5081	4708
DATONPSW	X	000011D0	4	4717	4709
DATTABS	X	00003000	1	5326	
DURATION	D	000015A0	8	5087	3897 4150 4390 4532 4790 4791 4794 4874
DWAT0010	3	00001428	8	4952	4951
DWAT0011	3	00001438	8	4957	4956
DWAT0012	3	00001448	8	4962	4961
DWAT0013	3	00001458	8	4967	4966
ECLCL1	A	000020C4	4	5287	3673
ECLCL1K	A	000020F4	4	5293	3712
ECLCL2	A	000020D4	4	5289	3682
ECLCL256	A	000020E4	4	5291	
ECLCL4	A	00002124	4	5299	3692
ECLCL8	A	00002134	4	5301	3703
ECLCLBTH	A	00002104	4	5295	3721
ECLCLOP1	A	00002144	4	5303	3731
ECLCLOP2	A	00002114	4	5297	3740
ECLCLPF	A	00002154	4	5305	4767
EDIT	X	00001614	12	5096	4804 4805
ENADEV	I	0000146E	4	4986	4914
ENAOKAY	I	000014BC	2	5011	5000
ENDCLCL	I	000013E2	4	4922	3674 3683 3693 3704 3713 3722 3732 3741
ENDCLOCK	D	00001598	8	5086	3895 4018 4148 4361 4388 4501 4530 4643 4867 4870 4873
ENDREGS	A	00000020	4	5182	3841
EOJ	H	00001420	2	4950	3566
EXLEN	F	00000018	4	5179	3831
EXTCPUAD	H	00000084	2	5551	
EXTICODE	H	00000086	2	5552	
EXTIPARM	F	00000080	4	5550	
EXTNPSW	F	00000058	8	5540	
EXTOPSW	F	00000018	8	5512	5518
FAILDEV	H	00001430	2	4955	4991 5001 5006
FAILIO	H	00001440	2	4960	4814 4837 4847
FAILMASK	A	0000001C	4	5180	3832
FAILTEST	H	00001450	2	4965	3590 3597 3604 3611 3619 3626 3633 3640 3672 3681 3691 3702 3711 3720 3730 3739 3856 4728 4734 4748 4754 4756 4760 4762 4764 4768 4772 4778 4924 4937
FIND0015	A	000014B4	4	5008	4986
FINL0015	H	00001476	2	4989	5005
FINM0015	A	000014B8	4	5009	5004
FINN0015	H	000014A4	2	5002	4993 4995
IIRB0016	F	000014F0	4	5036	5032 5034
IMAGE	1	00000000	12289	0	
INIT	H	000013D0	2	4908	3550
INV1	A	00001660	4	5116	3753
INV2	A	00001670	4	5117	3758
INV256	A	000016A0	4	5120	3773 4379

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
INV4	A	00001680	4	5118	3763			
INV8	A	00001690	4	5119	3768			
INVBOTH	A	000016B0	4	5122	3778			
INVOP1	A	000016C0	4	5123	3783			
INVOP2	A	000016D0	4	5124	3788			
IOCB	4	00000000	48	5334	5358	3540		
IOCBCAW	A	00000018	4	5354				
IOCBCM	X	00000009	1	5342				
IOCBCS	X	0000000B	1	5345				
IOCBCT	X	0000000D	1	5347				
IOCBDEV	H	00000004	2	5339	4994			
IOCBDID	F	00000000	4	5336	4810	4997		
IOCBDV	H	00000002	2	5338				
IOCBIRB	A	00000020	8	5356	4815			
IOCBL	U	00000030	1	5358				
IOCBORB	A	00000018	8	5355	4812	4911		
IOCBRCNT	H	00000016	2	5353	4844			
IOCBSC	X	0000000E	1	5348	4808	4839	4841	
IOCBSCCW	A	00000010	4	5350	4843			
IOCBSCNT	F	00000014	4	5351				
IOCBSIB	A	00000028	8	5357	4987			
IOCBST	H	0000000A	2	5343	4809	4840		
IOCBUM	X	00000008	1	5341				
IOCBUS	X	0000000A	1	5344	4846			
IOCBUT	X	0000000C	1	5346				
IOCBWAIT	X	0000000F	1	5349				
IOCBZERO	H	00000006	2	5340	4809			
IOCB_009	A	000014C0	4	5019	4910			
IOELADDR	F	000000AC	4	5587				
IOICODE	H	000000BA	2	5592				
IOIID	F	000000C0	4	5597				
IOINIT	I	00001460	4	4974	4913			
IOIPARM	F	000000BC	4	5596				
IOMK0014	F	00001468	4	4976	4974	4975		
ION0008	3	000012E8	8	4825	4822			
IONPSW	F	00000078	8	5544				
IOOPSW	F	00000038	8	5516	5526			
IORB0016	X	00001530	12	5038	5030			
IOS0008	X	000012F0	8	4826	4821	4829		
IOSSID	F	000000B8	4	5595	4832			
IOWT0007	H	000012CE	2	4819	4833	4836	4842	
IPLCCW1	F	00000008	8	5504				
IPLCCW2	F	00000010	8	5505				
IPLPSW	F	00000000	8	5503				
IRB	4	00000000	96	5413	5417	5419	4816	
IRBECW	X	00000020	32	5416				
IRBEMW	X	00000040	32	5418				
IRBESW	X	0000000C	20	5415				
IRBL	U	00000040	1	5417				
IRBSCSW	X	00000000	12	5414	4839	4840	4843	4844
IRBXL	U	00000060	1	5419				
IRST0008	H	000012F8	2	4828	4825			

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
K	U	00000400	1	5067	5068 5069 5070 5269 5293
K64	U	00010000	1	5069	5076 4519 4521 5102 5103 5104 5105 5107 5108 5109 5110 5116 5117 5118 5119 5120 5122 5123 5124 5197 5198 5202 5203 5207 5208 5212 5213 5217 5218 5222 5223 5225 5227 5228 5230 5232 5233 5235 5263 5265 5267 5269 5271 5273 5275 5277 5279 5281 5287 5289 5291 5293 5295 5297 5299 5301 5303 5305
LCHANLOG	F	000000B0	4	5588	
LOGICERR	D	000011C0	8	4715	
MAINSIZE	U	00200000	1	5075	5076
MB	U	00100000	1	5070	5075 4521 5102 5103 5104 5105 5107 5108 5109 5110 5116 5117 5118 5119 5120 5122 5123 5124 5198 5203 5208 5213 5218 5223 5228 5233 5263 5265 5267 5269 5271 5273 5275 5277 5279 5281 5287 5289 5291 5293 5295 5297 5299 5301 5303 5305
MCKLOG	F	00000100	4	5620	
MCKNPSW	F	00000070	8	5543	
MCKOPSW	F	00000030	8	5515	5524
MEASUREB	X	000000B9	1	5591	
MKARCHMD	X	000000A3	1	5579	
MKARS	F	00000120	4	5618	
MKCLKCMP	F	000000E0	8	5604	
MKCPUTIM	F	000000D8	8	5603	
MKCRS	F	000001C0	4	5623	
MKDMGCOD	F	000000F4	4	5607	
MKFAILA	F	000000F8	4	5609	
MKFPRS	D	00000160	8	5621	
MKICODE	F	000000E8	4	5605	
MKLOGOUT	F	00000100	4	5611	
MKMODEL	F	000000FC	4	5610	
MKXSAA	F	000000D4	4	5602	
MONCLS	H	00000094	2	5567	
MONCODE	F	0000009C	4	5574	
MONNUMBR	X	00000095	1	5569	
MPGACCID	X	000000A2	1	5577	
MVCINCLC	I	0000141A	6	4942	4936
MVCININ	X	000016E0	256	5126	4380 4932
MVCINMVC	I	00001414	6	4941	4935
MVCINOUT	X	000017E0	256	5145	4942
MVCINSRC	I	0000140E	6	4940	4934
MVCINTST	I	000013F2	4	4931	3754 3759 3764 3769 3774 3779 3784 3789
MYPGMNEW	I	000011D8	6	4722	4700
NKGRS	F	00000180	4	5622	
NUMLOOPS	F	00001588	4	5083	3891 3901 4041 4154 4384 4394 4526 4536
NUMPGTBS	U	00000020	1	5076	5077 5079 4664
NUMSEGTB	U	00000002	1	5077	5081
OP1DATA	A	00000000	4	5171	3815
OP1LEN	F	00000004	4	5172	3816
OP1WHERE	A	00000008	4	5173	3812
OP2DATA	A	0000000C	4	5175	3819
OP2LEN	F	00000010	4	5176	3820
OP2WHERE	A	00000014	4	5177	3813
ORB	4	00000000	32	5366	5396 5404 3541
ORB1_0	X	00000004	1	5369	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
ORB1_8	X	00000005	1	5376	
ORBA	U	00000010	1	5380	
ORBB	U	00000004	1	5382	
ORBC	U	00000004	1	5372	
ORBCCW	A	00000008	4	5394	
ORBCSS	X	0000000C	1	5398	
ORBCU	X	0000000E	1	5401	
ORBD	U	00000040	1	5389	
ORBF	U	00000080	1	5377	
ORBH	U	00000002	1	5383	
ORBI	U	00000020	1	5379	
ORBKEYM	U	000000F0	1	5370	
ORBL	U	00000080	1	5387	
ORBLEN	U	0000000C	1	5396	
ORBLPM	X	00000006	1	5385	
ORBM	U	00000002	1	5373	
ORBP	U	00000040	1	5378	
ORBPARM	F	00000000	4	5367	
ORBPGM	X	0000000E	1	5400	
ORBRSV25	U	0000007E	1	5391	
ORBRSV26	U	0000003E	1	5390	
ORBRSV3	U	0000007F	1	5388	
ORBRSV4	U	00000080	1	5395	
ORBRSV5	X	0000000D	1	5399	
ORBRSV6	X	0000000F	1	5402	
ORBRSV7	X	00000010	16	5403	
ORBS	U	00000008	1	5371	
ORBT	U	00000001	1	5384	
ORBU	U	00000008	1	5381	
ORBX	U	00000001	1	5392	
ORBXLEN	U	00000020	1	5404	
ORBY	U	00000001	1	5374	
ORRB1_24	X	00000007	1	5386	
OVERHEAD	D	000015A8	8	5088	3897 4150 4390 4532 4789
PAGE	U	00001000	1	5068	5072 5078 5309 4668 5273 5279 5297 5303
PAGELOOP	I	00001158	4	4675	4678
PAGETABS	U	00003080	1	5079	4665
PCFETO	A	000000C4	4	5598	
PERACCID	X	000000A1	1	5576	
PERADDR	F	00000098	4	5573	
PERCODE	X	00000096	1	5570	
PERCODMK	U	000000F0	1	5571	
PFINSADR	I	000011BA	2	4713	4727
PFPAGE	U	00000005	1	5308	5309
PFPGBYTS	U	00005000	1	5309	4686
PGMACCID	X	000000A0	1	5575	
PGMDXC	F	00000090	4	5565	
PGMICODE	H	0000008E	2	5564	4733
PGMIID	F	0000008C	4	5560	
PGMIILC	X	0000008D	1	5562	
PGMIILCM	U	0000000C	1	5563	
PGMNPSW	F	00000068	8	5542	4699 4701 4702 4722

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
PGMOPSW	F	00000028	8	5514	5522 4727
PGMTRX	F	00000090	4	5566	4740
PMCW1_0	X	00000004	1	5727	
PMCW1_8	X	00000005	1	5730	4992 4998
PMCWB	U	00000004	1	5762	
PMCWCHP0	X	00000010	1	5751	
PMCWCHP1	X	00000011	1	5752	
PMCWCHP2	X	00000012	1	5753	
PMCWCHP3	X	00000013	1	5754	
PMCWCHP4	X	00000014	1	5755	
PMCWCHP5	X	00000015	1	5756	
PMCWCHP6	X	00000016	1	5757	
PMCWCHP7	X	00000017	1	5758	
PMCWDNUM	H	00000006	2	5742	4994
PMCWE	U	00000080	1	5731	4998
PMCWEXC	X	0000001B	1	5761	
PMCWIP	F	00000000	4	5726	
PMCWISCM	U	00000038	1	5728	
PMCWLM	U	00000060	1	5732	
PMCWLMG	U	00000020	1	5733	
PMCWLML	U	00000040	1	5734	
PMCWLPM	X	00000008	1	5744	
PMCWLPUM	X	0000000A	1	5746	
PMCWM	U	00000004	1	5738	
PMCWMBI	H	0000000C	2	5748	
PMCWMM	U	00000018	1	5735	
PMCWMMC	U	00000008	1	5737	
PMCWMME	U	00000010	1	5736	
PMCWPAM	X	0000000F	1	5750	
PMCWPIM	X	0000000B	1	5747	
PMCWPNOM	X	00000009	1	5745	
PMCWPOM	X	0000000E	1	5749	
PMCWRES1	X	00000018	4	5759	
PMCWRES2	X	00000018	3	5760	
PMCWS	U	00000001	1	5764	
PMCWT	U	00000002	1	5739	
PMCWV	U	00000001	1	5740	4992
PMCWX	U	00000002	1	5763	
PRTLINE	C	000015D0	68	5095	4020 4363 4503 4645 4804 4805 5094
R0	U	00000000	1	5779	3537 4666 4675 4676 4700 4701 4707 4740 4741 4742 4747
R1	U	00000001	1	5780	3799 3826 3836 3844 3857 4708
R10	U	0000000A	1	5789	3670 3671 3679 3680 3689 3690 3700 3701 3709 3710 3718 3719 3728
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SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
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R11	U	0000000B	1	5790	3832 3837 4397 4398 4399 4402 4403 4404 4405 4406 4407 4408 4409
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R12	U	0000000C	1	5791	3671 3680 3690 3701 3710 3719 3729 3738 3813 3862 3864 3887 3904
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     SYMBOL         TYPE    VALUE      LENGTH    DEFN  REFERENCES

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R13                    U     0000000D           1  5792  3670  3679  3689  3700  3709  3718  3728  3737  3886  4036  4044  4045  4048
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R15                    U     0000000F           1  5794  3674  3683  3693  3704  3713  3722  3732  3741  3754  3759  3764  3769  3774
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R2                     U     00000002           1  5781  3538  3543  3544  3545  3547  3800  3802  3827  3836  3848  3858  3872
R3                     U     00000003           1  5782  3540  4910
R4                     U     00000004           1  5783
R5                     U     00000005           1  5784  3576  3577  3578  3579  3580  3581  3588  3589  3595  3596  3602  3603  3609
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SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
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					4789 4860 4872 4877 4891 4923 4931
R6	U	00000006	1	5785	3582 3583 3588 3589 3595 3596 3602 3603 3609 3610 3617 3618 3624
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R7	U	00000007	1	5786	3816 3817 3820 3821 3831 3835 3841 3848 4668 4676 4775 4776 4777
					4791 4860 4862 4865 4867 4870 4874 4877 4897
R8	U	00000008	1	5787	3541 4911
R9	U	00000009	1	5788	3539 3547 3548
REG2LOW	U	000000DD	1	5187	5225 5230 5235
REG2PATT	U	AABBCCDD	1	5186	3827 5200 5205 5210 5215 5220 5225 5230 5235
RPTSAVE	F	00001340	4	4853	4786 4850
RPTSPEED	I	0000126A	4	4786	4021 4364 4504 4646
RSTNPSW	F	00000000	8	5508	
RSTOPSW	F	00000008	8	5509	
SAVER1	F	000004A8	4	3867	3799 3857
SAVETRT	D	000004B0	8	3868	3836
SCANOUT	X	00000080	1	5546	5547
SCANOUTL	U	00000000	1	5547	
SCHIB	4	00000000	52	5723	5770 4988
SCHIBL	U	00000034	1	5770	
SCHMBA	A	00000028	8	5768	
SCHMDA1	X	00000030	4	5769	
SCHMDA3	X	00000028	12	5767	
SCHPMCW	X	00000000	28	5725	
SCHSCSW	X	0000001C	12	5766	
SCSW	4	00000000	12	5428	5490
SCSW0CC	U	00000004	1	5444	
SCSW1	X	00000002	1	5448	
SCSW2	X	00000003	1	5457	4839
SCSWACP	U	00000001	1	5456	
SCSWADA	U	00000040	1	5459	
SCSWAHP	U	00000002	1	5455	
SCSWALKC	U	00000010	1	5442	
SCSWARP	U	00000008	1	5453	
SCSWASA	U	00000080	1	5458	
SCSWASP	U	00000004	1	5454	
SCSWASUS	U	00000020	1	5460	
SCSWATTN	U	00000080	1	5470	
SCSWBUSY	U	00000010	1	5473	
SCSWCCTL	U	00000004	1	5485	
SCSWCCW	A	00000004	4	5467	4843
SCSWCCWF	U	00000080	1	5439	
SCSWCCWP	U	00000040	1	5440	
SCSWCDAT	U	00000008	1	5484	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
SCSWCE	U	00000008	1	5474	
SCSWCHNG	U	00000001	1	5487	
SCSWCNT	H	0000000A	2	5489	4844
SCSWCS	X	00000009	1	5479	
SCSWCTLS	X	00000001	1	5438	
SCSWCUE	U	00000020	1	5472	
SCSWDCC0	U	00000000	1	5434	
SCSWDCC1	U	00000001	1	5435	
SCSWDCC3	U	00000003	1	5436	
SCSWDCCM	U	00000003	1	5433	
SCSWDE	U	00000004	1	5475	
SCSWECWC	U	00000002	1	5445	
SCSWESWF	U	00000004	1	5432	
SCSWFC	U	00000010	1	5452	
SCSWFH	U	00000020	1	5451	
SCSWFLAG	X	00000000	1	5429	
SCSWFM	U	00000070	1	5449	
SCSWFS	U	00000040	1	5450	
SCSWICTL	U	00000002	1	5486	
SCSWIL	U	00000040	1	5481	
SCSWISIC	U	00000020	1	5441	
SCSWKEYM	U	000000F0	1	5430	
SCSWL	U	0000000C	1	5490	
SCSWPCI	U	00000080	1	5480	
SCSWPNOP	U	00000001	1	5446	
SCSWPRGM	U	00000020	1	5482	
SCSWPROT	U	00000010	1	5483	
SCSWSAS	U	00000010	1	5461	
SCSWSINT	U	00000008	1	5462	
SCSWSM	U	00000040	1	5471	
SCSWSPEN	U	00000001	1	5465	
SCSWSPRI	U	00000004	1	5463	4841
SCSWSSEC	U	00000002	1	5464	
SCSWSSIC	U	00000008	1	5443	
SCSWSUSC	U	00000008	1	5431	
SCSWUC	U	00000002	1	5476	
SCSWUS	X	00000008	1	5469	4840
SCSWUX	U	00000001	1	5477	
SEGLOOP	I	0000114A	4	4670	4680
SEGTABLS	U	00003000	1	5078	5079 5324 4663 5081
SSARCHMD	X	000000A3	1	5578	
SSARS	F	00000120	4	5634	
SSCLKCMP	F	000000E0	8	5628	
SSCPUTIM	F	000000D8	8	5627	
SSCRS	F	000001C0	4	5637	
SSFPRS	D	00000160	8	5635	
SSGRS	F	00000180	4	5636	
SSMODEL	F	0000010C	4	5632	
SSPREFIX	F	00000108	4	5631	
SSPSW	F	00000100	8	5630	
SSXSAA	A	000000D4	4	5626	
STFLDATA	F	000000C8	4	5599	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
SUBDWORD	I	00001398	4	4889	4792 4875
SUBDWSAV	D	000013C0	8	4902	4889 4899
SUBTEST	X	000021FF	1	5322	3587 3594 3601 3608 3616 3623 3630 3637 3669 3678 3688 3699 3708 3717 3727 3736 3834 3843 3847 3882 4032 4375 4515 4654 4691 4698 4706 4726 4732 4739 4752 4758 4766 4770 4774
SVCICODE	H	0000008A	2	5558	
SVCIID	F	00000088	4	5554	
SVCIILC	X	00000089	1	5556	
SVCIILCM	U	0000000C	1	5557	
SVCNPSW	F	00000060	8	5541	
SVCOPSW	F	00000020	8	5513	5520
SVPGMNEW	D	000011C8	8	4716	4699 4722
TEST01	I	0000023A	4	3572	3554
TEST02	I	000002F0	4	3648	3555
TEST03	I	000003CA	4	3749	3556
TEST04	I	00000410	4	3797	3557
TEST91	I	000004B8	4	3878	3559
TEST92	I	0000079A	4	4028	3560
TEST93	I	00000BD0	4	4371	3561
TEST94	I	00000E76	4	4511	3562
TEST95	I	00001126	4	4653	3564
TESTADDR	U	000021FE	1	5072	5073 5319
TESTNUM	X	000021FE	1	5321	3572 3648 3749 3797 3881 4031 4374 4514 4653
TICKSAAA	P	000015B0	8	5090	4797 4800
TICKSBBB	P	000015B8	8	5091	4798 4802
TICKSTOT	P	000015C0	8	5092	4800 4801 4802 4805
TIMEADDR	U	000021FD	1	5073	5315
TIMEOPT	X	000021FD	1	5317	3878 4028 4371 4511
TIMER	F	00000050	4	5537	
TRT	I	0000049E	6	3864	3835
TRT1	A	000018E0	4	5197	
TRT2	A	00001908	4	5202	
TRT256	A	00001980	4	5217	
TRT4	A	00001930	4	5207	
TRT8	A	00001958	4	5212	
TRTBC	I	000004A4	4	3865	3837
TRTBTH	A	000019A8	4	5222	
TRTCTL	A	000018E0	4	5195	3805
TRTDONE	I	0000048A	4	3857	3854
TRTFAIL	I	00000486	4	3856	3845 3849 3865
TRTMVC1	I	00000492	6	3861	3817
TRTMVC2	I	00000498	6	3862	3821
TRTNEXT	U	00000028	1	5184	3851
TRTOP1	A	000019D0	4	5227	
TRTOP10	X	00001A24	4	5243	4520 5197 5202 5207 5212 5217
TRTOP111	X	00001B24	4	5245	5222 5232
TRTOP1F0	X	00001C24	4	5247	5227
TRTOP2	A	000019F8	4	5232	
TRTOP20	X	00001D24	1	5253	4522 5198 5203 5208 5213 5218
TRTOP211	X	00001E24	1	5255	5223 5233
TRTOP2F0	X	00001F24	1	5257	5228
TRTTEST	4	00000000	40	5169	3806

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
TST4LOOP	U	0000041E	1	3808	3853
TTDES	F	00000054	4	5538	
UA0	F	00000010	8	5510	
UA1	F	0000004C	4	5535	
UA2	F	000000A4	4	5580	
UA3	F	000000B4	4	5589	
UA4	X	000000B8	1	5590	
UA5	X	000000CC	8	5600	
UA6	X	000000EC	8	5606	
UA7	F	00000118	8	5617	
UA8	X	00000180	32	5646	
WPSW0008	3	000012E0	8	4824	4823
ZBRKADDR	A	00000110	8	5616	
ZEMONCNT	F	0000010C	4	5615	
ZEMONCTR	A	00000100	8	5613	
ZEMONSIZ	F	00000108	4	5614	
ZEXTNPSW	X	000001B0	16	5649	
ZEXTOPSW	X	00000130	16	5641	
ZIONPSW	X	000001F0	16	5653	
ZIOOPSW	X	00000170	16	5645	
ZMCKNPSW	X	000001E0	16	5652	
ZMCKOPSW	X	00000160	16	5644	
ZMKFAILA	F	000000F8	8	5608	
ZMONCODE	F	000000B0	8	5583	
ZPGMNPSW	X	000001D0	16	5651	
ZPGMOPSW	X	00000150	16	5643	
ZPGMTRX	F	000000A8	8	5582	
ZRSTNPSW	X	000001A0	16	5648	
ZRSTOPSW	X	00000120	16	5640	
ZSASDISP	U	000011C0	1	5654	
ZSVCNPSW	X	000001C0	16	5650	
ZSVCOPSW	X	00000140	16	5642	
=A(00+(5*K64))	A	00001544	4	5053	4519
=A(MB+(5*K64))	A	00001548	4	5054	4521
=A(PAGE)	A	00001554	4	5057	4668
=A(PAGETABS)	A	00001550	4	5056	4665 4692
=A(PFINSADR)	A	0000155C	4	5059	4727
=A(PFPGBYTS)	A	00001558	4	5058	4686
=A(REG2PATT)	A	0000153C	4	5051	3827
=A(SEGTABLS)	A	0000154C	4	5055	4663
=CL5'CLC'	C	00001564	5	5061	4020
=CL5'CLCL'	C	00001569	5	5062	4363
=CL5'MVCIN'	C	0000156E	5	5063	4503
=CL5'TRT'	C	00001573	5	5064	4645
=F'0'	F	00001540	4	5052	3852
=F'1'	F	00001560	4	5060	4895
=P'4294967296'	P	00001578	6	5065	4801

MACRO	DEFN	REFERENCES					
ANTR	109						
APROB	241						
ARCHIND	401	3431					
ARCHLVL	542	3430					
ASAIPL	668	3510					
ASALOAD	748	3493					
ASAREA	803	5500					
ASAZAREA	988						
CPUWAIT	1071	4820					
DSECTS	1397	5332	5364	5411	5426	5497	
DWAIT	1600	4949	4954	4959	4964		
DWAITEND	1657	4948					
ENADEV	1665	4985					
ESA390	1765						
IOCB	1776	5018					
IOCBDS	1952	5333					
IOFMT	1986	5365	5412	5427	5659	5677	5685	5722
IOINIT	2324	4973					
IOTRFR	2365						
ORB	2413	5037					
POINTER	2602						
PSWFMT	2630						
RAWAIT	2764						
RAWIO	2860	4807					
SIGCPU	3018						
SMMGR	3076						
SMMGRB	3176						
TRAP128	3225						
TRAP64	3202	3495	3498				
TRAPS	3238						
ZARCH	3312						
ZEROH	3324						
ZEROL	3352						
ZEROLH	3380						
ZEROLL	3403						

```
   DESC     SYMBOL    SIZE     POS        ADDR

Entry: 0

Image      IMAGE     12289  0000-3000  0000-3000
  Region   CODE      12289  0000-3000  0000-3000
    CSECT  CLCLETAL  12289  0000-3000  0000-3000
```

```
   STMT                                          FILE NAME

1     c:\Users\Fish\Documents\Visual Studio 2008\Projects\MyProjects\ASMA-0\CLCL-et-al\CLCL-et-al.asm
2     C:\Users\Fish\Documents\Visual Studio 2008\Projects\Hercules\_Git\_Harold\SATK-0\srcasm\satk.mac


** NO ERRORS FOUND **
```