```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                      2 ************************************************************************
                                                      3 *
                                                      4 *            CLC, CLCL, MVCIN and TRT instruction tests
                                                      5 *
                                                      6 ************************************************************************
                                                      7 *
                                                      8 *  This program tests proper functioning of the CLCL, MVCIN and TRT
                                                      9 *  instructions.  It also optionally times them.
                                                     10 *
                                                     11 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                     12 *  obvious coding errors.  None of the tests are thorough.  They are
                                                     13 *  NOT designed to test all aspects of any of the instructions.
                                                     14 *
                                                     15 ************************************************************************
                                                     16 *
                                                     17 *  Example Hercules Testcase:
                                                     18 *
                                                     19 *
                                                     20 *     *Testcase CLCL-et-al (Test CLCL, MVCIN and TRT instructions)
                                                     21 *
                                                     22 *     archlvl     390
                                                     23 *     mainsize    2
                                                     24 *     numcpu      1
                                                     25 *     sysclear
                                                     26 *
                                                     27 *     loadcore    "$(testpath)/CLCL-et-al.core"
                                                     28 *
                                                     29 *     runtest     2         # (NON-timing test duration)
                                                     30 *     ##r           1fff=ff   # (enable timing tests too!)
                                                     31 *     ##runtest     360       # (TIMING too test duration)
                                                     32 *
                                                     33 *     *Compare
                                                     34 *     r 2000.2
                                                     35 *
                                                     36 *     *Want  "Ending test/subtest number (NON-timing)"   0402
                                                     37 *     ##*Want  "Ending test/subtest number (TIMING too)"   9401
                                                     38 *
                                                     39 *     *Done
                                                     40 *
                                                     41 *
                                                     42 ************************************************************************
```

```
 LOC         OBJECT CODE        ADDR1     ADDR2     STMT

                                                      44           PRINT OFF
                                                    3425           PRINT ON

                                                    3427 ********************************************************************************
                                                    3428 *        SATK prolog stuff...
                                                    3429 ********************************************************************************

                                                    3431           ARCHLVL  ZARCH=NO,MNOTE=NO
                                                    3433+$AL       OPSYN AL
                                                    3434+$ALR      OPSYN ALR
                                                    3435+$B        OPSYN B
                                                    3436+$BAS      OPSYN BAS
                                                    3437+$BASR     OPSYN BASR
                                                    3438+$BC       OPSYN BC
                                                    3439+$BCTR     OPSYN BCTR
                                                    3440+$BE       OPSYN BE
                                                    3441+$BH       OPSYN BH
                                                    3442+$BL       OPSYN BL
                                                    3443+$BM       OPSYN BM
                                                    3444+$BNE      OPSYN BNE
                                                    3445+$BNH      OPSYN BNH
                                                    3446+$BNL      OPSYN BNL
                                                    3447+$BNM      OPSYN BNM
                                                    3448+$BNO      OPSYN BNO
                                                    3449+$BNP      OPSYN BNP
                                                    3450+$BNZ      OPSYN BNZ
                                                    3451+$BO       OPSYN BO
                                                    3452+$BP       OPSYN BP
                                                    3453+$BXLE     OPSYN BXLE
                                                    3454+$BZ       OPSYN BZ
                                                    3455+$CH       OPSYN CH
                                                    3456+$L        OPSYN L
                                                    3457+$LH       OPSYN LH
                                                    3458+$LM       OPSYN LM
                                                    3459+$LPSW     OPSYN LPSW
                                                    3460+$LR       OPSYN LR
                                                    3461+$LTR      OPSYN LTR
                                                    3462+$NR       OPSYN NR
                                                    3463+$SL       OPSYN SL
                                                    3464+$SLR      OPSYN SLR
                                                    3465+$SR       OPSYN SR
                                                    3466+$ST       OPSYN ST
                                                    3467+$STM      OPSYN STM
                                                    3468+$X        OPSYN X
                                                    3469+$AHI      OPSYN AHI
                                                    3470+$B        OPSYN J
                                                    3471+$BC       OPSYN BRC
                                                    3472+$BE       OPSYN JE
                                                    3473+$BH       OPSYN JH
                                                    3474+$BL       OPSYN JL
                                                    3475+$BM       OPSYN JM
                                                    3476+$BNE      OPSYN JNE
```

```
 LOC         OBJECT CODE        ADDR1     ADDR2     STMT

                                                   3477+$BNH     OPSYN JNH
                                                   3478+$BNL     OPSYN JNL
                                                   3479+$BNM     OPSYN JNM
                                                   3480+$BNO     OPSYN JNO
                                                   3481+$BNP     OPSYN JNP
                                                   3482+$BNZ     OPSYN JNZ
                                                   3483+$BO      OPSYN JO
                                                   3484+$BP      OPSYN JP
                                                   3485+$BXLE    OPSYN JXLE
                                                   3486+$BZ      OPSYN JZ
                                                   3487+$CHI     OPSYN CHI
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  3489 ********************************************************************************
                                                  3490 *        Initiate the CLCLetal CSECT in the CODE region
                                                  3491 *        with the location counter at 0
                                                  3492 ********************************************************************************

                                                  3494 CLCLetal ASALOAD  REGION=CODE
                                00000000  00003000  3495+CLCLetal START 0,CODE
00000000  000A0000 00000008                       3497+         PSW   0,0,2,0,X'008'      64-bit Restart ISR Trap New PSW
00000008                      00000008  00000058  3498+         ORG   CLCLetal+X'058'
00000058  000A0000 00000018                       3500+         PSW   0,0,2,0,X'018'      64-bit External ISR Trap New PSW
00000060  000A0000 00000020                       3501+         PSW   0,0,2,0,X'020'      64-bit Supervisor Call ISR Trap New PSW
00000068  000A0000 00000028                       3502+         PSW   0,0,2,0,X'028'      64-bit Program ISR Trap New PSW
00000070  000A0000 00000030                       3503+         PSW   0,0,2,0,X'030'      64-bit Machine Check Trap New PSW
00000078  000A0000 00000038                       3504+         PSW   0,0,2,0,X'038'      64-bit Input/Output Trap New PSW
00000080                      00000080  00000200  3505+         ORG   CLCLetal+512



                                                  3507 ********************************************************************************
                                                  3508 *        Create IPL (restart) PSW
                                                  3509 ********************************************************************************


                                                  3511          ASAIPL   IA=BEGIN
00000200                      00000200  00000000  3512+         ORG   CLCLetal
00000000  00080000 00000200                       3513+         PSW   0,0,0,0,BEGIN,24
00000008                      00000008  00000200  3514+         ORG   CLCLetal+512     Reset CSECT to end of assigned storage area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    3516 ********************************************************************************
                                                    3517 *                The actual "CLCLetal" program itself...
                                                    3518 ********************************************************************************
                                                    3519 *
                                                    3520 *  Architecture Mode: 390
                                                    3521 *  Addressing Mode:   31-bit
                                                    3522 *  Register Usage:
                                                    3523 *
                                                    3524 *   R0       (work)
                                                    3525 *   R1       I/O device used by ENADEV and RAWIO macros
                                                    3526 *   R2       First base register
                                                    3527 *   R3       IOCB pointer for ENADEV and RAWIO macros
                                                    3528 *   R4       IO work register used by ENADEV and RAWIO
                                                    3529 *   R5-R7    (work)
                                                    3530 *   R8       ORB pointer
                                                    3531 *   R9       Second base register
                                                    3532 *   R10-R13  (work)
                                                    3533 *   R14      Subroutine call
                                                    3534 *   R15      Secondary Subroutine call or work
                                                    3535 *
                                                    3536 ********************************************************************************


00000200                    00000000                3538          USING  ASA,R0          Low core addressability
00000200                    00000200                3539          USING  BEGIN,R2        FIRST Base Register
00000200                    00001200                3540          USING  BEGIN+4096,R9   SECOND Base Register
00000200                    00000000                3541          USING  IOCB,R3         SATK Device I/O Control Block
00000200                    00000000                3542          USING  ORB,R8          ESA/390 Operation Request Block


00000200  0520                                      3544 BEGIN    BALR   R2,0            Initalize FIRST base register
00000202  0620                                      3545          BCTR   R2,0            Initalize FIRST base register
00000204  0620                                      3546          BCTR   R2,0            Initalize FIRST base register

00000206  4190 2800                      00000800   3548          LA     R9,2048(,R2)    Initalize SECOND base register
0000020A  4190 9800                      00000800   3549          LA     R9,2048(,R9)    Initalize SECOND base register

0000020E  45E0 91B8                      000013B8   3551          BAL    R14,INIT        Initalize Program
                                                    3552 *
                                                    3553 **       Run the tests...
                                                    3554 *
00000212  45E0 203A                      0000023A   3555          BAL    R14,TEST01      Test CLC   instruction
00000216  45E0 20F0                      000002F0   3556          BAL    R14,TEST02      Test CLCL  instruction
0000021A  45E0 21CA                      000003CA   3557          BAL    R14,TEST03      Test MVCIN instruction
0000021E  45E0 2210                      00000410   3558          BAL    R14,TEST04      Test TRT   instruction
                                                    3559 *
00000222  45E0 22B8                      000004B8   3560          BAL    R14,TEST91      Time CLC   instruction  (speed test)
00000226  45E0 2594                      00000794   3561          BAL    R14,TEST92      Time CLCL  instruction  (speed test)
0000022A  45E0 29C0                      00000BC0   3562          BAL    R14,TEST93      Time MVCIN instruction  (speed test)
0000022E  45E0 2C66                      00000E66   3563          BAL    R14,TEST94      Time TRT   instruction  (speed test)
                                                    3564 *
00000232  45E0 2F16                      00001116   3565          BAL    R14,TEST95      Test CLCL page fault handling
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                     3566 *
00000236  47F0 9208                       00001408  3567          B     EOJ              Normal completion
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  3569 ********************************************************************************
                                                  3570 *        TEST01                  Test CLC instruction
                                                  3571 ********************************************************************************

0000023A  9201 9FFE                      000021FE  3573 TEST01   MVI   TESTNUM,X'01'
                                                  3574 *
                                                  3575 **       Initialize test parameters...
                                                  3576 *
0000023E  5850 9428                      00001628  3577          L      R5,CLC4          Operand-1 address
00000242  92FF 5003                      00000003  3578          MVI    3(R5),X'FF'      Force unequal compare (op1 high)
00000246  5850 9438                      00001638  3579          L      R5,CLC256        (same thing for CLC256)
0000024A  92FF 50FF                      000000FF  3580          MVI    255(R5),X'FF'    (same thing for CLC256)
0000024E  5850 9440                      00001640  3581          L      R5,CLCOP1        (same thing for CLCOP1)
00000252  92FF 50FF                      000000FF  3582          MVI    255(R5),X'FF'    (same thing for CLCOP1)
00000256  5860 9434                      00001634  3583          L      R6,CLC8+4        OPERAND-2(!) address
0000025A  92FF 6007                      00000007  3584          MVI    7(R6),X'FF'      Force OPERAND-2 to be high! (op1 LOW!)
                                                  3585 *
                                                  3586 **       Neither cross (one byte)
                                                  3587 *
0000025E  9201 9FFF                      000021FF  3588          MVI   SUBTEST,X'01'
00000262  9856 9408                      00001608  3589          LM    R5,R6,CLC1
00000266  D500 5000 6000      00000000   00000000  3590          CLC   0(1,R5),0(R6)
0000026C  4770 9238                      00001438  3591          BNE   FAILTEST
                                                  3592 *
                                                  3593 **       Neither cross (two bytes)
                                                  3594 *
00000270  9202 9FFF                      000021FF  3595          MVI   SUBTEST,X'02'
00000274  9856 9410                      00001610  3596          LM    R5,R6,CLC2
00000278  D501 5000 6000      00000000   00000000  3597          CLC   0(2,R5),0(R6)
0000027E  4770 9238                      00001438  3598          BNE   FAILTEST
                                                  3599 *
                                                  3600 **       Neither cross (four bytes)
                                                  3601 *
00000282  9204 9FFF                      000021FF  3602          MVI   SUBTEST,X'04'
00000286  9856 9428                      00001628  3603          LM    R5,R6,CLC4
0000028A  D503 5000 6000      00000000   00000000  3604          CLC   0(4,R5),0(R6)
00000290  47D0 9238                      00001438  3605          BNH   FAILTEST                 (see INIT; CLC4:    op1 > op2)
                                                  3606 *
                                                  3607 **       Neither cross (eight bytes)
                                                  3608 *
00000294  9208 9FFF                      000021FF  3609          MVI   SUBTEST,X'08'
00000298  9856 9430                      00001630  3610          LM    R5,R6,CLC8
0000029C  D507 5000 6000      00000000   00000000  3611          CLC   0(8,R5),0(R6)
000002A2  47B0 9238                      00001438  3612          BNL   FAILTEST                 (see INIT; CLC8:    op1 < op2)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          3614 *
                                          3615 **       Neither cross (256 bytes)
                                          3616 *
000002A6  92FF 9FFF                 000021FF  3617          MVI   SUBTEST,X'FF'
000002AA  9856 9438                 00001638  3618          LM    R5,R6,CLC256
000002AE  D5FF 5000 6000      00000000  00000000  3619          CLC   0(256,R5),0(R6)
000002B4  47D0 9238                 00001438  3620          BNH   FAILTEST                (see INIT; CLC256:  op1 > op2)
                                          3621 *
                                          3622 **       Both cross
                                          3623 *
000002B8  9222 9FFF                 000021FF  3624          MVI   SUBTEST,X'22'
000002BC  9856 9418                 00001618  3625          LM    R5,R6,CLCBOTH
000002C0  D5FF 5000 6000      00000000  00000000  3626          CLC   0(256,R5),0(R6)
000002C6  4770 9238                 00001438  3627          BNE   FAILTEST
                                          3628 *
                                          3629 **       Only op1 crosses
                                          3630 *
000002CA  9210 9FFF                 000021FF  3631          MVI   SUBTEST,X'10'
000002CE  9856 9440                 00001640  3632          LM    R5,R6,CLCOP1
000002D2  D5FF 5000 6000      00000000  00000000  3633          CLC   0(256,R5),0(R6)
000002D8  47D0 9238                 00001438  3634          BNH   FAILTEST                (see INIT; CLCOP1:  op1 > op2)
                                          3635 *
                                          3636 **       Only op2 crosses
                                          3637 *
000002DC  9220 9FFF                 000021FF  3638          MVI   SUBTEST,X'20'
000002E0  9856 9420                 00001620  3639          LM    R5,R6,CLCOP2
000002E4  D5FF 5000 6000      00000000  00000000  3640          CLC   0(256,R5),0(R6)
000002EA  4770 9238                 00001438  3641          BNE   FAILTEST
                                          3642 *
000002EE  07FE                            3643          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3645 ********************************************************************************
                                                  3646 *        TEST02                    Test CLCL instruction
                                                  3647 ********************************************************************************

000002F0  9202 9FFE                     000021FE  3649 TEST02   MVI   TESTNUM,X'02'
                                                  3650 *
                                                  3651 **       Initialize test parameters...
                                                  3652 *
000002F4  9856 9E6C                     0000206C  3653          LM    R5,R6,CLCL4     CLCL4 test Op1 address and length
000002F8  1E56                                    3654          ALR   R5,R6           Point past last byte
000002FA  0650                                    3655          BCTR  R5,0            Backup to last byte
000002FC  92FF 5000                     00000000  3656          MVI   0(R5),X'FF'     Force unequal compare (op1 high)
                                                  3657 *
00000300  9856 9E8C                     0000208C  3658          LM    R5,R6,CLCLOP1   (same thing for CLCLOP1 test)
00000304  1E56                                    3659          ALR   R5,R6                    "
00000306  0650                                    3660          BCTR  R5,0                     "
00000308  92FF 5000                     00000000  3661          MVI   0(R5),X'FF'              "
                                                  3662 *
0000030C  9856 9E84                     00002084  3663          LM    R5,R6,CLCL8+8   CLCL8 test ===> OP2 <===
00000310  1E56                                    3664          ALR   R5,R6
00000312  0650                                    3665          BCTR  R5,0
00000314  92FF 5000                     00000000  3666          MVI   0(R5),X'FF'     ===> OPERAND-2 high (OP1 LOW) <===
                                                  3667 *
                                                  3668 **       Neither cross (one byte)
                                                  3669 *
00000318  9201 9FFF                     000021FF  3670          MVI   SUBTEST,X'01'
0000031C  98AD 9E0C                     0000200C  3671          LM    R10,R13,CLCL1
00000320  0FAC                                    3672          CLCL  R10,R12
00000322  4770 9238                     00001438  3673          BNE   FAILTEST
00000326  4150 9EAC                     000020AC  3674          LA    R5,ECLCL1
0000032A  45F0 91CA                     000013CA  3675          BAL   R15,ENDCLCL
                                                  3676 *
                                                  3677 **       Neither cross (two bytes)
                                                  3678 *
0000032E  9202 9FFF                     000021FF  3679          MVI   SUBTEST,X'02'
00000332  98AD 9E1C                     0000201C  3680          LM    R10,R13,CLCL2
00000336  0FAC                                    3681          CLCL  R10,R12
00000338  4770 9238                     00001438  3682          BNE   FAILTEST
0000033C  4150 9EBC                     000020BC  3683          LA    R5,ECLCL2
00000340  45F0 91CA                     000013CA  3684          BAL   R15,ENDCLCL
                                                  3685 *
                                                  3686 **       Neither cross (four bytes)
                                                  3687 **       (inequality on last byte of op1)
                                                  3688 *
00000344  9204 9FFF                     000021FF  3689          MVI   SUBTEST,X'04'
00000348  98AD 9E6C                     0000206C  3690          LM    R10,R13,CLCL4
0000034C  0FAC                                    3691          CLCL  R10,R12
0000034E  47D0 9238                     00001438  3692          BNH   FAILTEST                (see INIT; CLCL4:   op1 > op2)
00000352  4150 9F0C                     0000210C  3693          LA    R5,ECLCL4
00000356  45F0 91CA                     000013CA  3694          BAL   R15,ENDCLCL
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3696 *
                                                  3697 **       Neither cross (eight bytes)
                                                  3698 **       (inequality on last byte of op2)
                                                  3699 *
0000035A  9208 9FFF                     000021FF  3700          MVI   SUBTEST,X'08'
0000035E  98AD 9E7C                     0000207C  3701          LM    R10,R13,CLCL8
00000362  0FAC                                    3702          CLCL  R10,R12
00000364  47B0 9238                     00001438  3703          BNL   FAILTEST                  (see INIT; CLCL8:   op1 < op2)
00000368  4150 9F1C                     0000211C  3704          LA    R5,ECLCL8
0000036C  45F0 91CA                     000013CA  3705          BAL   R15,ENDCLCL
                                                  3706 *
                                                  3707 **       Neither cross (1K bytes)
                                                  3708 *
00000370  9200 9FFF                     000021FF  3709          MVI   SUBTEST,X'00'
00000374  98AD 9E3C                     0000203C  3710          LM    R10,R13,CLCL1K
00000378  0FAC                                    3711          CLCL  R10,R12
0000037A  4770 9238                     00001438  3712          BNE   FAILTEST
0000037E  4150 9EDC                     000020DC  3713          LA    R5,ECLCL1K
00000382  45F0 91CA                     000013CA  3714          BAL   R15,ENDCLCL
                                                  3715 *
                                                  3716 **       Both cross
                                                  3717 *
00000386  9222 9FFF                     000021FF  3718          MVI   SUBTEST,X'22'
0000038A  98AD 9E4C                     0000204C  3719          LM    R10,R13,CLCLBOTH
0000038E  0FAC                                    3720          CLCL  R10,R12
00000390  4770 9238                     00001438  3721          BNE   FAILTEST
00000394  4150 9EEC                     000020EC  3722          LA    R5,ECLCLBTH
00000398  45F0 91CA                     000013CA  3723          BAL   R15,ENDCLCL
                                                  3724 *
                                                  3725 **       Only op1 crosses
                                                  3726 **       (inequality on last byte of op1)
                                                  3727 *
0000039C  9210 9FFF                     000021FF  3728          MVI   SUBTEST,X'10'
000003A0  98AD 9E8C                     0000208C  3729          LM    R10,R13,CLCLOP1
000003A4  0FAC                                    3730          CLCL  R10,R12
000003A6  47D0 9238                     00001438  3731          BNH   FAILTEST                  (see INIT; CLCLOP1: op1 > op2)
000003AA  4150 9F2C                     0000212C  3732          LA    R5,ECLCLOP1
000003AE  45F0 91CA                     000013CA  3733          BAL   R15,ENDCLCL
                                                  3734 *
                                                  3735 **       Only op2 crosses
                                                  3736 *
000003B2  9220 9FFF                     000021FF  3737          MVI   SUBTEST,X'20'
000003B6  98AD 9E5C                     0000205C  3738          LM    R10,R13,CLCLOP2
000003BA  0FAC                                    3739          CLCL  R10,R12
000003BC  4770 9238                     00001438  3740          BNE   FAILTEST
000003C0  4150 9EFC                     000020FC  3741          LA    R5,ECLCLOP2
000003C4  45F0 91CA                     000013CA  3742          BAL   R15,ENDCLCL
                                                  3743 *
000003C8  07FE                                    3744          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3746 ********************************************************************************
                                                  3747 *        TEST03                    Test MVCIN instruction
                                                  3748 ********************************************************************************

000003CA  9203 9FFE                      000021FE  3750 TEST03   MVI   TESTNUM,X'03'
                                                  3751 *
                                                  3752 **       Neither cross (one byte)
                                                  3753 *
000003CE  4150 9448                      00001648  3754          LA    R5,INV1
000003D2  45F0 91DA                      000013DA  3755          BAL   R15,MVCINTST
                                                  3756 *
                                                  3757 **       Neither cross (two bytes)
                                                  3758 *
000003D6  4150 9458                      00001658  3759          LA    R5,INV2
000003DA  45F0 91DA                      000013DA  3760          BAL   R15,MVCINTST
                                                  3761 *
                                                  3762 **       Neither cross (four bytes)
                                                  3763 *
000003DE  4150 9468                      00001668  3764          LA    R5,INV4
000003E2  45F0 91DA                      000013DA  3765          BAL   R15,MVCINTST
                                                  3766 *
                                                  3767 **       Neither cross (eight bytes)
                                                  3768 *
000003E6  4150 9478                      00001678  3769          LA    R5,INV8
000003EA  45F0 91DA                      000013DA  3770          BAL   R15,MVCINTST
                                                  3771 *
                                                  3772 **       Neither cross (256 bytes)
                                                  3773 *
000003EE  4150 9488                      00001688  3774          LA    R5,INV256
000003F2  45F0 91DA                      000013DA  3775          BAL   R15,MVCINTST
                                                  3776 *
                                                  3777 **       Both cross
                                                  3778 *
000003F6  4150 9498                      00001698  3779          LA    R5,INVBOTH
000003FA  45F0 91DA                      000013DA  3780          BAL   R15,MVCINTST
                                                  3781 *
                                                  3782 **       Only op1 crosses
                                                  3783 *
000003FE  4150 94A8                      000016A8  3784          LA    R5,INVOP1
00000402  45F0 91DA                      000013DA  3785          BAL   R15,MVCINTST
                                                  3786 *
                                                  3787 **       Only op2 crosses
                                                  3788 *
00000406  4150 94B8                      000016B8  3789          LA    R5,INVOP2
0000040A  45F0 91DA                      000013DA  3790          BAL   R15,MVCINTST
                                                  3791 *
0000040E  07FE                                    3792          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3794 ********************************************************************************
                                                  3795 *        TEST04                    Test TRT instruction
                                                  3796 ********************************************************************************

00000410  9204 9FFE                     000021FE  3798 TEST04   MVI   TESTNUM,X'04'
                                                  3799
00000414  5010 22A8                     000004A8  3800          ST    R1,SAVER1           Save register 1
00000418  18F2                                    3801          LR    R15,R2              Save first base register
                                                  3802
0000041A                                          3803          DROP  R2                  Temporarily drop addressability
0000041A                  00000200                3804          USING BEGIN,R15           Establish temporary addressability
                                                  3805
0000041A  4150 96C8                     000018C8  3806          LA    R5,TRTCTL           Point R5 --> testing control table
0000041E                  00000000                3807          USING TRTTEST,R5          What each table entry looks like
                                                  3808
                          0000041E  00000001      3809 TST4LOOP EQU   *
                                                  3810 *
                                                  3811 **       Initialize operand data  (move data to testing address)
                                                  3812 *
0000041E  58A0 5008                     00000008  3813          L     R10,OP1WHERE        Where to move operand-1 data to
00000422  58C0 5014                     00000014  3814          L     R12,OP2WHERE        Where to move operand-2 data to
                                                  3815
00000426  5860 5000                     00000000  3816          L     R6,OP1DATA          Where op1 data is right now
0000042A  5870 5004                     00000004  3817          L     R7,OP1LEN           How much of it there is
0000042E  4470 F292                     00000492  3818          EX    R7,TRTMVC1          Move op1 data to testing location
                                                  3819
00000432  5860 500C                     0000000C  3820          L     R6,OP2DATA          Where op1 data is right now
00000436  5870 5010                     00000010  3821          L     R7,OP2LEN           How much of it there is
0000043A  4470 F298                     00000498  3822          EX    R7,TRTMVC2          Move op1 data to testing location
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   3824 *
                                                   3825 **       Initialize R1/R2...      (TRT non-zero CC updates R1/R2!)
                                                   3826 *
0000043E  1F11                                     3827          SLR   R1,R1              (known value)
00000440  5820 9324                       00001524 3828          L     R2,=A(REG2PATT)    (known value)
                                                   3829 *
                                                   3830 **       Execute TRT instruction and check for expected condition code
                                                   3831 *
00000444  5870 5018                       00000018 3832          L     R7,EXLEN           (len-1)
00000448  58B0 501C                       0000001C 3833          L     R11,FAILMASK       (failure CC)
                                                   3834
0000044C  9200 9FFF                       000021FF 3835          MVI   SUBTEST,X'00'      (primary TRT)
00000450  4470 F29E                       0000049E 3836          EX    R7,TRT             TRT...
00000454  9012 F2B0                       000004B0 3837          STM   R1,R2,SAVETRT      (save R1/R2 results)
00000458  44B0 F2A4                       000004A4 3838          EX    R11,TRTBC          fail if...
                                                   3839 *
                                                   3840 **       Verify R1/R2 now contain (or still contain!) expected values
                                                   3841 *
0000045C  9867 5020                       00000020 3842          LM    R6,R7,ENDREGS
                                                   3843
00000460  9201 9FFF                       000021FF 3844          MVI   SUBTEST,X'01'      (R1 result)
00000464  1516                                     3845          CLR   R1,R6              R1 correct?
00000466  4770 F286                       00000486 3846          BNE   TRTFAIL            No, FAILTEST!
                                                   3847
0000046A  9202 9FFF                       000021FF 3848          MVI   SUBTEST,X'02'      (R2 result)
0000046E  1527                                     3849          CLR   R2,R7              R2 correct?
00000470  4770 F286                       00000486 3850          BNE   TRTFAIL            No, FAILTEST!
                                                   3851
00000474  4150 5028                       00000028 3852          LA    R5,TRTNEXT         Go on to next table entry
00000478  D503 9328 5000      00001528    00000000 3853          CLC   =F'0',0(R5)        End of table?
0000047E  4770 F21E                       0000041E 3854          BNE   TST4LOOP           No, loop...
00000482  47F0 F28A                       0000048A 3855          B     TRTDONE            Done! (success!)
                                                   3856
00000486  41E0 9238                       00001438 3857 TRTFAIL  LA    R14,FAILTEST       Unexpected results!
0000048A  5810 F2A8                       000004A8 3858 TRTDONE  L     R1,SAVER1          Restore register 1
0000048E  182F                                     3859          LR    R2,R15             Restore first base register
00000490  07FE                                     3860          BR    R14                Return to caller or FAILTEST
                                                   3861
00000492  D200 A000 6000      00000000    00000000 3862 TRTMVC1  MVC   0(0,R10),0(R6)     (move op1 to where it should be)
00000498  D200 C000 6000      00000000    00000000 3863 TRTMVC2  MVC   0(0,R12),0(R6)     (move op2 to where it should be)
                                                   3864
0000049E  DD00 A000 C000      00000000    00000000 3865 TRT      TRT   0(0,R10),0(R12)    (TRT op1,op2)
000004A4  4700 F286                       00000486 3866 TRTBC    BC    0,TRTFAIL          (fail if unexpected condition code)
                                                   3867
000004A8  00000000                                 3868 SAVER1   DC    F'0'
000004B0  00000000 00000000                        3869 SAVETRT  DC    D'0'               (saved R1/R2 from TRT results)
                                                   3870
000004B8                                           3871          DROP  R5
000004B8                                           3872          DROP  R15
000004B8                      00000200             3873          USING BEGIN,R2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3875 ********************************************************************************
                                                  3876 *        TEST91                  Time CLC instruction  (speed test)
                                                  3877 ********************************************************************************

000004B8  91FF 9FFD                     000021FD  3879 TEST91   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
000004BC  078E                                    3880          BZR   R14              No, skip timing tests

000004BE  9291 9FFE                     000021FE  3882          MVI   TESTNUM,X'91'
000004C2  9201 9FFF                     000021FF  3883          MVI   SUBTEST,X'01'
                                                  3884 *
                                                  3885 **       First, time the overhead...
                                                  3886 *
000004C6  5850 9370                     00001570  3887          L     R5,NUMLOOPS
000004CA  B205 9378                     00001578  3888          STCK  BEGCLOCK
000004CE  0560                                    3889          BALR  R6,0
000004D0  0656                                    3890          BCTR  R5,R6
000004D2  B205 9380                     00001580  3891          STCK  ENDCLOCK
000004D6  45F0 912C                     0000132C  3892          BAL   R15,CALCDUR
000004DA  D207 9390 9388      00001590  00001588  3893          MVC   OVERHEAD,DURATION
                                                  3894 *
                                                  3895 **       Now do the actual timing run...
                                                  3896 *
000004E0  5850 9370                     00001570  3897          L     R5,NUMLOOPS
000004E4  98AD 9E2C                     0000202C  3898          LM    R10,R13,CLCL256
000004E8  B205 9378                     00001578  3899          STCK  BEGCLOCK
000004EC  0560                                    3900          BALR  R6,0
000004EE  D5FF A000 C000      00000000  00000000  3901          CLC   0(256,R10),0(R12)
000004F4  D5FF A000 C000      00000000  00000000  3902          CLC   0(256,R10),0(R12)
                                                  3903 *        ..........ETC..........
                                                  3904          PRINT OFF
                                                  4010          PRINT ON
00000770  D5FF A000 C000      00000000  00000000  4011          CLC   0(256,R10),0(R12)
00000776  D5FF A000 C000      00000000  00000000  4012          CLC   0(256,R10),0(R12)
0000077C  D5FF A000 C000      00000000  00000000  4013          CLC   0(256,R10),0(R12)
00000782  0656                                    4014          BCTR  R5,R6
00000784  B205 9380                     00001580  4015          STCK  ENDCLOCK
                                                  4016 *
00000788  D204 93D9 934C      000015D9  0000154C  4017          MVC   PRTLINE+33(5),=CL5'CLC'
0000078E  45F0 9052                     00001252  4018          BAL   R15,RPTSPEED
00000792  07FE                                    4019          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4021 ********************************************************************************
                                          4022 *        TEST92                  Time CLCL instruction  (speed test)
                                          4023 ********************************************************************************

00000794  91FF 9FFD                 000021FD  4025 TEST92   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
00000798  078E                              4026          BZR   R14              No, skip timing tests

0000079A  9292 9FFE                 000021FE  4028          MVI   TESTNUM,X'92'
0000079E  9201 9FFF                 000021FF  4029          MVI   SUBTEST,X'01'
                                          4030 *
                                          4031 **       First, time the overhead...
                                          4032 *
000007A2  5850 9370                 00001570  4033          L     R5,NUMLOOPS
000007A6  B205 9378                 00001578  4034          STCK  BEGCLOCK
000007AA  0560                              4035          BALR  R6,0
000007AC  98AD 9E2C                 0000202C  4036          LM    R10,R13,CLCL256
000007B0  98AD 9E2C                 0000202C  4037          LM    R10,R13,CLCL256
000007B4  98AD 9E2C                 0000202C  4038          LM    R10,R13,CLCL256
                                          4039 *        .........ETC.........
                                          4040          PRINT OFF
                                          4136          PRINT ON
00000934  98AD 9E2C                 0000202C  4137          LM    R10,R13,CLCL256
00000938  98AD 9E2C                 0000202C  4138          LM    R10,R13,CLCL256
0000093C  0656                              4139          BCTR  R5,R6
0000093E  B205 9380                 00001580  4140          STCK  ENDCLOCK
00000942  45F0 912C                 0000132C  4141          BAL   R15,CALCDUR
00000946  D207 9390 9388      00001590  00001588  4142          MVC   OVERHEAD,DURATION
                                          4143 *
                                          4144 **       Now do the actual timing run...
                                          4145 *
0000094C  5850 9370                 00001570  4146          L     R5,NUMLOOPS
00000950  B205 9378                 00001578  4147          STCK  BEGCLOCK
00000954  0560                              4148          BALR  R6,0
00000956  98AD 9E2C                 0000202C  4149          LM    R10,R13,CLCL256
0000095A  0FAC                              4150          CLCL  R10,R12
0000095C  98AD 9E2C                 0000202C  4151          LM    R10,R13,CLCL256
00000960  0FAC                              4152          CLCL  R10,R12
00000962  98AD 9E2C                 0000202C  4153          LM    R10,R13,CLCL256
00000966  0FAC                              4154          CLCL  R10,R12
                                          4155 *        .........ETC.........
                                          4156          PRINT OFF
                                          4347          PRINT ON
00000BA2  98AD 9E2C                 0000202C  4348          LM    R10,R13,CLCL256
00000BA6  0FAC                              4349          CLCL  R10,R12
00000BA8  98AD 9E2C                 0000202C  4350          LM    R10,R13,CLCL256
00000BAC  0FAC                              4351          CLCL  R10,R12
00000BAE  0656                              4352          BCTR  R5,R6
00000BB0  B205 9380                 00001580  4353          STCK  ENDCLOCK
                                          4354 *
00000BB4  D204 93D9 9351      000015D9  00001551  4355          MVC   PRTLINE+33(5),=CL5'CLCL'
00000BBA  45F0 9052                 00001252  4356          BAL   R15,RPTSPEED
00000BBE  07FE                              4357          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4359 ********************************************************************************
                                                  4360 *        TEST93                  Time MVCIN instruction  (speed test)
                                                  4361 ********************************************************************************

00000BC0  91FF 9FFD                     000021FD  4363 TEST93   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
00000BC4  078E                                    4364           BZR   R14              No, skip timing tests

00000BC6  9293 9FFE                     000021FE  4366           MVI   TESTNUM,X'93'
00000BCA  9201 9FFF                     000021FF  4367           MVI   SUBTEST,X'01'
                                                  4368 *
                                                  4369 **       First, time the overhead...
                                                  4370 *
00000BCE  5850 9370                     00001570  4371           L     R5,NUMLOOPS
00000BD2  B205 9378                     00001578  4372           STCK  BEGCLOCK
00000BD6  0560                                    4373           BALR  R6,0
00000BD8  0656                                    4374           BCTR  R5,R6
00000BDA  B205 9380                     00001580  4375           STCK  ENDCLOCK
00000BDE  45F0 912C                     0000132C  4376           BAL   R15,CALCDUR
00000BE2  D207 9390 9388      00001590  00001588  4377           MVC   OVERHEAD,DURATION
                                                  4378 *
                                                  4379 **       Now do the actual timing run...
                                                  4380 *
00000BE8  98AD 9488                     00001688  4381           LM    R10,R13,INV256
00000BEC  D2FF D000 94C8      00000000  000016C8  4382           MVC   0(256,R13),MVCININ
00000BF2  5850 9370                     00001570  4383           L     R5,NUMLOOPS
00000BF6  B205 9378                     00001578  4384           STCK  BEGCLOCK
00000BFA  0560                                    4385           BALR  R6,0
00000BFC  E8FF A000 B000      00000000  00000000  4386           MVCIN 0(256,R10),0(R11)
00000C02  E8FF A000 B000      00000000  00000000  4387           MVCIN 0(256,R10),0(R11)
00000C08  E8FF A000 B000      00000000  00000000  4388           MVCIN 0(256,R10),0(R11)
                                                  4389 *         .........ETC.........
                                                  4390           PRINT OFF
                                                  4485           PRINT ON
00000E42  E8FF A000 B000      00000000  00000000  4486           MVCIN 0(256,R10),0(R11)
00000E48  E8FF A000 B000      00000000  00000000  4487           MVCIN 0(256,R10),0(R11)
00000E4E  E8FF A000 B000      00000000  00000000  4488           MVCIN 0(256,R10),0(R11)
00000E54  0656                                    4489           BCTR  R5,R6
00000E56  B205 9380                     00001580  4490           STCK  ENDCLOCK
                                                  4491 *
00000E5A  D204 93D9 9356      000015D9  00001556  4492           MVC   PRTLINE+33(5),=CL5'MVCIN'
00000E60  45F0 9052                     00001252  4493           BAL   R15,RPTSPEED
00000E64  07FE                                    4494           BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4496 ********************************************************************************
                                                  4497 *        TEST94                  Time TRT instruction  (speed test)
                                                  4498 ********************************************************************************

00000E66  91FF 9FFD                     000021FD  4500 TEST94   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
00000E6A  078E                                    4501          BZR   R14              No, skip timing tests

00000E6C  9294 9FFE                     000021FE  4503          MVI   TESTNUM,X'94'
00000E70  9201 9FFF                     000021FF  4504          MVI   SUBTEST,X'01'
                                                  4505 *
                                                  4506 **       First, time the overhead...
                                                  4507 *
00000E74  5850 9370                     00001570  4508          L     R5,NUMLOOPS
00000E78  B205 9378                     00001578  4509          STCK  BEGCLOCK
00000E7C  0560                                    4510          BALR  R6,0
00000E7E  0656                                    4511          BCTR  R5,R6
00000E80  B205 9380                     00001580  4512          STCK  ENDCLOCK
00000E84  45F0 912C                     0000132C  4513          BAL   R15,CALCDUR
00000E88  D207 9390 9388      00001590  00001588  4514          MVC   OVERHEAD,DURATION
                                                  4515 *
                                                  4516 **       Now do the actual timing run...
                                                  4517 *
00000E8E  58A0 932C                     0000152C  4518          L     R10,=A(00+(5*K64))
00000E92  D2FF A000 980C      00000000  00001A0C  4519          MVC   0(256,R10),TRTOP10
00000E98  58C0 9330                     00001530  4520          L     R12,=A(MB+(5*K64))
00000E9C  D2FF C000 9B0C      00000000  00001D0C  4521          MVC   0(256,R12),TRTOP20
00000EA2  5850 9370                     00001570  4522          L     R5,NUMLOOPS
00000EA6  B205 9378                     00001578  4523          STCK  BEGCLOCK
00000EAA  0560                                    4524          BALR  R6,0
00000EAC  DDFF A000 C000      00000000  00000000  4525          TRT   0(256,R10),0(R12)
00000EB2  DDFF A000 C000      00000000  00000000  4526          TRT   0(256,R10),0(R12)
00000EB8  DDFF A000 C000      00000000  00000000  4527          TRT   0(256,R10),0(R12)
                                                  4528 *        .........ETC.........
                                                  4529          PRINT OFF
                                                  4624          PRINT ON
000010F2  DDFF A000 C000      00000000  00000000  4625          TRT   0(256,R10),0(R12)
000010F8  DDFF A000 C000      00000000  00000000  4626          TRT   0(256,R10),0(R12)
000010FE  DDFF A000 C000      00000000  00000000  4627          TRT   0(256,R10),0(R12)
00001104  0656                                    4628          BCTR  R5,R6
00001106  B205 9380                     00001580  4629          STCK  ENDCLOCK
                                                  4630 *
0000110A  D204 93D9 935B      000015D9  0000155B  4631          MVC   PRTLINE+33(5),=CL5'TRT'
00001110  45F0 9052                     00001252  4632          BAL   R15,RPTSPEED
00001114  07FE                                    4633          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                          4635 ********************************************************************************
                                          4636 *        TEST95                    Test CLCL page fault handling
                                          4637 ********************************************************************************

00001116  9295 9FFE                  000021FE  4639 TEST95   MVI   TESTNUM,X'95'
0000111A  9200 9FFF                  000021FF  4640          MVI   SUBTEST,X'00'
                                          4641 *
                                          4642 **       Initialize Dynamic Address Translation tables...
                                          4643 *
0000111E  58A0 9334                  00001534  4644          L     R10,=A(SEGTABLS)   Segment Tables Origin
00001122  41B0 0020                  00000020  4645          LA    R11,NUMPGTBS       Number of Segment Table Entries
00001126  58C0 9338                  00001538  4646          L     R12,=A(PAGETABS)   Page Tables Origin
0000112A  1F00                               4647          SLR   R0,R0              First Page Frame Address
0000112C  4160 0004                  00000004  4648          LA    R6,4               Size of one table entry
00001130  5870 933C                  0000153C  4649          L     R7,=A(PAGE)        Size of one Page Frame

00001134  50C0 A000                  00000000  4651 SEGLOOP  ST    R12,0(,R10)        Seg Table Entry <= Page Table Origin
00001138  960F A003                  00000003  4652          OI    3(R10),X'0F'       Seg Table Entry <= Page Table Length
0000113C  1EA6                               4653          ALR   R10,R6             Bump to next Segment Table Entry

0000113E  41D0 0010                  00000010  4655          LA    R13,16             Page Table Entries per Page Table
00001142  5000 C000                  00000000  4656 PAGELOOP ST    R0,0(,R12)         Page Table Entry = Page Frame Address
00001146  1E07                               4657          ALR   R0,R7              Increment to next Page Frame Address
00001148  1EC6                               4658          ALR   R12,R6             Bump to next Page Table Entry
0000114A  46D0 2F42                  00001142  4659          BCT   R13,PAGELOOP       Loop until Page table is complete

0000114E  46B0 2F34                  00001134  4661          BCT   R11,SEGLOOP        Loop until all Segment Table Entries built
                                          4662 *
                                          4663 **       Update desired page table entry to cause page fault
                                          4664 *
00001152  98AD 9E9C                  0000209C  4665          LM    R10,R13,CLCLPF     Retrieve CLCL PF test parameters
00001156  185A                               4666          LR    R5,R10             R5 --> Operand-1
00001158  5E50 9340                  00001540  4667          AL    R5,=A(PFPGBYTS)    R5 --> Operand-1 Page Fault address
0000115C  1865                               4668          LR    R6,R5              R6 --> Address where PF should occur
0000115E  8850 000C                  0000000C  4669          SRL   R5,12              R5 = Page Frame number
00001162  8950 0002                  00000002  4670          SLL   R5,2               R5 = Page Table Entry number

00001166  9204 9FFF                  000021FF  4672          MVI   SUBTEST,X'04'
0000116A  5E50 9338                  00001538  4673          AL    R5,=A(PAGETABS)    R5 --> Page Table Entry
0000116E  9604 5002                  00000002  4674          OI    2(R5),X'04'        Mark this page invalid
                                          4675 *
                                          4676 **       Install program check routine to catch the page fault
                                          4677 *
00001172  9202 9FFF                  000021FF  4678          MVI   SUBTEST,X'02'
00001176  D207 2FB0 0068      000011B0  00000068  4679          MVC   SVPGMNEW,PGMNPSW   Save original Program New PSW
0000117C  4100 2FC0                  000011C0  4680          LA    R0,MYPGMNEW        Point to temporary Pgm New routine
00001180  5000 006C                  0000006C  4681          ST    R0,PGMNPSW+4       Point Program New PSW to our routine
00001184  9208 0069                  00000069  4682          MVI   PGMNPSW+1,X'08'    Make it a non-disabled-wait PSW!
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   4684 *
                                                   4685 **       Run the test: should cause a page fault
                                                   4686 *
00001188  920F 9FFF                     000021FF  4687          MVI   SUBTEST,X'0F'
0000118C  B700 9368                     00001568  4688          LCTL  R0,R0,CRLREG0      Switch to DAT mode
00001190  B711 936C                     0000156C  4689          LCTL  R1,R1,CTLREG1      Switch to DAT mode
00001194  8200 2FB8                     000011B8  4690          LPSW  DATONPSW           Switch to DAT mode
00001198  4700 2F98                     00001198  4691 BEGDATON NOP   *                  (pad)
0000119C  4700 2F9C                     0000119C  4692          NOP   *                  (pad)
000011A0  B20D 0000                     00000000  4693          PTLB  ,                  Purge Translation Lookaside Buffer
000011A4  0FAC                                    4694 PFINSADR CLCL  R10,R12            Page Fault should occur on this instr
000011A6  0700                                    4695          CNOP  0,8                  (align to doubleword)
000011A8  00000000 00000000                       4696 LOGICERR DC    D'0'                 We should never reach here!
000011B0  00000000 00000000                       4697 SVPGMNEW DC    D'0'                 Original Program New PSW
000011B8  04080000 00001198                       4698 DATONPSW DC    XL4'04080000',A(BEGDATON)  Enable DAT PSW
                                                   4699 *
                                                   4700 **       Temporary Program New routine:
                                                   4701 **       Restore original Program New PSW
                                                   4702 *
000011C0  D207 0068 2FB0  00000068  000011B0  4703 MYPGMNEW MVC   PGMNPSW,SVPGMNEW   Restore original Program New PSW
                                                   4704 *
                                                   4705 **       Verify Program Check occurred on expected instruction
                                                   4706 *
000011C6  9268 9FFF                     000021FF  4707          MVI   SUBTEST,X'68'
000011CA  D503 9344 002C  00001544  0000002C  4708          CLC   =A(PFINSADR),PGMOPSW+4   Program Check where expected?
000011D0  4770 9238                     00001438  4709          BNE   FAILTEST                 No?! Something is VERY WRONG!
                                                   4710 *
                                                   4711 **       Verify Program Check was indeed a page fault
                                                   4712 *
000011D4  9211 9FFF                     000021FF  4713          MVI   SUBTEST,X'11'
000011D8  9511 008F                     0000008F  4714          CLI   PGMICODE+1,X'11'   Verify it's a Page Fault interrupt
000011DC  4770 9238                     00001438  4715          BNE   FAILTEST          If not then something is VERY WRONG!
                                                   4716 *
                                                   4717 **       Verify Page Fault occurred on expected Page
                                                   4718 *
000011E0  9205 9FFF                     000021FF  4719          MVI   SUBTEST,X'05'
000011E4  5800 0090                     00000090  4720          L     R0,PGMTRX          Get where Page Fault occurred
000011E8  8800 000C                     0000000C  4721          SRL   R0,12
000011EC  8900 000C                     0000000C  4722          SLL   R0,12

000011F0  8860 000C                     0000000C  4724          SRL   R6,12              Where Page Fault is expected
000011F4  8960 000C                     0000000C  4725          SLL   R6,12

000011F8  1506                                    4727          CLR   R0,R6              Page Fault occur on expected Page?
000011FA  4770 9238                     00001438  4728          BNE   FAILTEST           No? Then something is very wrong!
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4730 *
                                                  4731 **       Verify CLCL instruction registers were updated as expected
                                                  4732 *
000011FE  9206 9FFF                     000021FF  4733          MVI   SUBTEST,X'06'
00001202  55A0 9E9C                     0000209C  4734          CL    R10,CLCLPF          (op1 greater than starting value?)
00001206  47D0 9238                     00001438  4735          BNH   FAILTEST
0000120A  55C0 9EA4                     000020A4  4736          CL    R12,CLCLPF+4+4      (op2 greater than starting value?)
0000120E  47D0 9238                     00001438  4737          BNH   FAILTEST

00001212  9207 9FFF                     000021FF  4739          MVI   SUBTEST,X'07'
00001216  15BD                                    4740          CLR   R11,R13             (same remaining lengths?)
00001218  4770 9238                     00001438  4741          BNE   FAILTEST
0000121C  55B0 9EA0                     000020A0  4742          CL    R11,CLCLPF+4        (op1 len less than starting value?)
00001220  47B0 9238                     00001438  4743          BNL   FAILTEST
00001224  55D0 9EA8                     000020A8  4744          CL    R13,CLCLPF+4+4+4    (op2 len less than starting value?)
00001228  47B0 9238                     00001438  4745          BNL   FAILTEST

0000122C  9208 9FFF                     000021FF  4747          MVI   SUBTEST,X'08'
00001230  55A0 9F3C                     0000213C  4748          CL    R10,ECLCLPF         (stop before end?)
00001234  47B0 9238                     00001438  4749          BNL   FAILTEST

00001238  9209 9FFF                     000021FF  4751          MVI   SUBTEST,X'09'
0000123C  15A6                                    4752          CLR   R10,R6              (stop at or before expected page?)
0000123E  4720 9238                     00001438  4753          BH    FAILTEST

00001242  9210 9FFF                     000021FF  4755          MVI   SUBTEST,X'10'
00001246  187A                                    4756          LR    R7,R10              (op1 stopped address)
00001248  1E7B                                    4757          ALR   R7,R11              (add remaining length)
0000124A  1576                                    4758          CLR   R7,R6               (would remainder reach PF page?)
0000124C  47D0 9238                     00001438  4759          BNH   FAILTEST

00001250  07FE                                    4761          BR    R14                 Success!
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4763 ********************************************************************************
                                          4764 *        RPTSPEED                  Report instruction speed
                                          4765 ********************************************************************************

00001252  50F0 9128                 00001328  4767 RPTSPEED ST    R15,RPTSAVE        Save return address
00001256  45F0 912C                 0000132C  4768          BAL   R15,CALCDUR        Calculate duration
                                          4769 *
0000125A  4150 9390                 00001590  4770          LA    R5,OVERHEAD        Subtract overhead
0000125E  4160 9388                 00001588  4771          LA    R6,DURATION        From raw timing
00001262  4170 9388                 00001588  4772          LA    R7,DURATION        Yielding true instruction timing
00001266  45F0 9180                 00001380  4773          BAL   R15,SUBDWORD       Do it
                                          4774 *
0000126A  98CD 9388                 00001588  4775          LM    R12,R13,DURATION   Convert to...
0000126E  8CC0 000C                 0000000C  4776          SRDL  R12,12             ... microseconds
                                          4777 *
00001272  4EC0 9398                 00001598  4778          CVD   R12,TICKSAAA       convert HIGH part to decimal
00001276  4ED0 93A0                 000015A0  4779          CVD   R13,TICKSBBB       convert LOW  part to decimal
                                          4780 *
0000127A  F877 93A8 9398      000015A8  00001598  4781          ZAP   TICKSTOT,TICKSAAA            Calculate...
00001280  FC75 93A8 9360      000015A8  00001560  4782          MP    TICKSTOT,=P'4294967296'      ...decimal...
00001286  FA77 93A8 93A0      000015A8  000015A0  4783          AP    TICKSTOT,TICKSBBB            ...microseconds
                                          4784 *
0000128C  D20B 93E3 93FC      000015E3  000015FC  4785          MVC   PRTLINE+43(L'EDIT),EDIT          (edit into...
00001292  DE0B 93E3 93AB      000015E3  000015AB  4786          ED    PRTLINE+43(L'EDIT),TICKSTOT+3     ...print line)
```

```
                                          4788          RAWIO 4,FAIL=FAILIO      Print elapsed time on console
00001298  9200 300E                 0000000E  4789+         MVI   IOCBSC,X'00'           Clear SC information
0000129C  D201 300A 3006      0000000A  00000006  4790+         MVC   IOCBST,IOCBZERO       Clear accumulated status
000012A2  5810 3000                 00000000  4791+         L     1,IOCBDID            Remember the device ID with which I am working
                                          4792+* Initiate Subchannel-based input/output operation
000012A6  5840 3018                 00000018  4793+         $L    4,IOCBORB            Locate the ORB for the channel subsystem
000012AA  B233 4000                 00000000  4794+         SSCH  0(4)                 Initiate the I/O operation
000012AE  A774 00BD                 00001428  4795+         $BC   B'0111',FAILIO       ..Start function failed, report/handle the error
000012B2  5840 3020                 00000020  4796+         $L    4,IOCBIRB            Locate the IRB storage area
000012B6                      00000000          4797+         USING IRB,4                Make it addressable

                                          4799+* Wait for I/O operation to present status via an interruption
000012B6                                  4800+IOWT0007 DS    0H  Wait for I/O to complete
000012B6  D207 90D8 0078      000012D8  00000078  4802+         MVC   IOS0008(8),120(0)               Save Input/Output new PSW
000012BC  D207 0078 90D0      00000078  000012D0  4803+         MVC   120(8,0),ION0008              Establish Input/Ouput new PSW
000012C2  8200 90C8                 000012C8  4804+         $LPSW WPSW0008                      Wait for event
000012C8  020A0000 00000000                   4805+WPSW0008 PSW   2,0,2,0,0                     Wait for event
000012D0  00082000 000012E0                   4806+ION0008  PSW   0,0,0,32,IRST0008,24              I/O New PSW: cc==2
000012D8  00000000 00000000                   4807+IOS0008  DC    XL8'00'
                                          4808+* Handle input/output interruption
000012E0                                  4809+IRST0008 DS    0H
000012E0  D207 0078 90D8      00000078  000012D8  4810+         MVC   120(8,0),IOS0008            Restore input/output new PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  4811+* Process the interruption...
                                                  4812+* Validate interruption is for the expected subchannel
000012E6  5510 00B8                     000000B8  4813+         CL    1,IOSSID              Is this the device for which I am waiting?
000012EA  A774 FFE6                     000012B6  4814+         $BNE  IOWT0007              ..No, continue waiting for it
                                                  4815+* Accumulate interruption information from IRB
000012EE  B235 4000                     00000000  4816+         TSCH  0(4)                  Retrive interrupt information
000012F2  A744 FFE2                     000012B6  4817+         $BC   B'0100',IOWT0007      CC1 (not status pending), wait for it to arriv
000012F6  A714 0099                     00001428  4818+         $BC   B'0001',FAILIO        CC3 (not operational), an error then
                                                  4819+*                                    CC0 (status was pending), accumulate the status
000012FA  D600 300E 4003      0000000E  00000003  4820+         OC    IOCBSC,IRBSCSW+SCSW2  Accumulate status control
00001300  D601 300A 4008      0000000A  00000008  4821+         OC    IOCBST,IRBSCSW+SCSWUS Accumulate device and channel status
00001306  9104 300E                     0000000E  4822+         TM    IOCBSC,SCSWSPRI       Primary subchannel status?
0000130A  A7E4 FFD6                     000012B6  4823+         $BNO  IOWT0007              ..No, wait for primary status
0000130E  D203 3010 4004      00000010  00000004  4824+         MVC   IOCBSCCW,IRBSCSW+SCSWCCW  CCW address
00001314  D201 3016 400A      00000016  0000000A  4825+         MVC   IOCBRCNT,IRBSCSW+SCSWCNT  Residual count
                                                  4826+* Test for errors as specified in the IOCB
0000131A  910C 300A                     0000000A  4827+         TM    IOCBUS,CSWCE+CSWDE    Channel end and device end both accumulated?
0000131E  A7E4 0085                     00001428  4828+         $BNO  FAILIO                Hunh? No CE and DE but do have primary status!
                                                  4829+* Input/Output operation successful


00001322  58F0 9128                     00001328  4831          L     R15,RPTSAVE           Restore return address
00001326  07FF                                    4832          BR    R15                   Return to caller

00001328  00000000                                4834 RPTSAVE  DC    F'0'                  R15 save area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4836 ********************************************************************************
                                          4837 *        CALCDUR                   Calculate DURATION
                                          4838 ********************************************************************************

0000132C  50F0 9170                  00001370  4840 CALCDUR  ST    R15,CALCRET        Save return address
00001330  9057 9174                  00001374  4841          STM   R5,R7,CALCWORK     Save work registers
                                          4842 *
00001334  9867 9378                  00001578  4843          LM    R6,R7,BEGCLOCK     Remove CPU number from clock value
00001338  8C60 0006                  00000006  4844          SRDL  R6,6                       "
0000133C  8D60 0006                  00000006  4845          SLDL  R6,6                       "
00001340  9067 9378                  00001578  4846          STM   R6,R7,BEGCLOCK             "
                                          4847 *
00001344  9867 9380                  00001580  4848          LM    R6,R7,ENDCLOCK     Remove CPU number from clock value
00001348  8C60 0006                  00000006  4849          SRDL  R6,6                       "
0000134C  8D60 0006                  00000006  4850          SLDL  R6,6                       "
00001350  9067 9380                  00001580  4851          STM   R6,R7,ENDCLOCK             "
                                          4852 *
00001354  4150 9378                  00001578  4853          LA    R5,BEGCLOCK        Starting time
00001358  4160 9380                  00001580  4854          LA    R6,ENDCLOCK        Ending time
0000135C  4170 9388                  00001588  4855          LA    R7,DURATION        Difference
00001360  45F0 9180                  00001380  4856          BAL   R15,SUBDWORD       Calculate duration
                                          4857 *
00001364  9857 9174                  00001374  4858          LM    R5,R7,CALCWORK     Restore work registers
00001368  58F0 9170                  00001370  4859          L     R15,CALCRET        Restore return address
0000136C  07FF                               4860          BR    R15                Return to caller

00001370  00000000                   4862 CALCRET  DC    F'0'               R15 save area
00001374  00000000 00000000          4863 CALCWORK DC    3F'0'              R5-R7 save area



                                          4865 ********************************************************************************
                                          4866 *        SUBDWORD                  Subtract two doublewords
                                          4867 *        R5 --> subtrahend, R6 --> minuend, R7 --> result
                                          4868 ********************************************************************************

00001380  90AD 91A8                  000013A8  4870 SUBDWORD STM   R10,R13,SUBDWSAV   Save registers
                                          4871 *
00001384  98AB 5000                  00000000  4872          LM    R10,R11,0(R5)      Subtrahend  (value to subtract)
00001388  98CD 6000                  00000000  4873          LM    R12,R13,0(R6)      Minuend     (what to subtract FROM)
0000138C  1FDB                               4874          SLR   R13,R11            Subtract LOW part
0000138E  47B0 9196                  00001396  4875          BNM   *+4+4              (branch if no borrow)
00001392  5FC0 9348                  00001548  4876          SL    R12,=F'1'          (otherwise do borrow)
00001396  1FCA                               4877          SLR   R12,R10            Subtract HIGH part
00001398  90CD 7000                  00000000  4878          STM   R12,R13,0(R7)      Store results
                                          4879 *
0000139C  98AD 91A8                  000013A8  4880          LM    R10,R13,SUBDWSAV   Restore registers
000013A0  07FF                               4881          BR    R15                Return to caller

000013A8  00000000 00000000          4883 SUBDWSAV DC    2D'0'              R10-R13 save area
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                    4885 ********************************************************************************
                                                    4886 *        Program Initialization
                                                    4887 ********************************************************************************

000013B8                                            4889 INIT     DS     0H               Program Initialization

000013B8  4130 92A8                    000014A8     4891          LA     R3,IOCB_009      Point to IOCB
000013BC  5880 3018                    00000018     4892          L      R8,IOCBORB       Point to ORB

000013C0  45F0 9248                    00001448     4894          BAL    R15,IOINIT       Initialize the CPU for I/O operations
000013C4  45F0 9256                    00001456     4895          BAL    R15,ENADEV       Enable our device making ready for use
000013C8  07FE                                      4896          BR     R14              Return to caller




                                                    4898 ********************************************************************************
                                                    4899 *        Verify CLCL ending register values
                                                    4900 * R10-R12 = actual ending values, R5 --> expected ending values
                                                    4901 ********************************************************************************

000013CA  90AD 9F4C                    0000214C     4903 ENDCLCL  STM    R10,R13,CLCLEND  Save actual ending register values
000013CE  D50F 5000 9F4C      00000000 0000214C     4904          CLC    0(4*4,R5),CLCLEND Do they have the expected values?
000013D4  4770 9238                    00001438     4905          BNE    FAILTEST         If not then the test has failed
000013D8  07FF                                      4906          BR     R15              Otherwise return to caller




                                                    4908 ********************************************************************************
                                                    4909 *        MVCINTST
                                                    4910 ********************************************************************************

000013DA  98AD 5000                    00000000     4912 MVCINTST LM     R10,R13,0(R5)    a(dst),a(src+(len-1)),a(len-1),a(src)
000013DE  4160 95C7                    000017C7     4913          LA     R6,MVCININ+256-1 Point to end of source
000013E2  1F6C                                      4914          SLR    R6,R12           Backup by length amount
000013E4  44C0 91F6                    000013F6     4915          EX     R12,MVCINSRC     Initialize source data
000013E8  44C0 91FC                    000013FC     4916          EX     R12,MVCINMVC     Do the Move Inverse
000013EC  44C0 9202                    00001402     4917          EX     R12,MVCINCLC     Compare with expected results
000013F0  4770 9238                    00001438     4918          BNE    FAILTEST         FAIL if not the expected value
000013F4  07FF                                      4919          BR     R15              Otherwise return to caller


000013F6  D200 D000 6000      00000000  00000000    4921 MVCINSRC MVC    0(0,R13),0(R6)   Executed Instruction
000013FC  E800 A000 B000      00000000  00000000    4922 MVCINMVC MVCIN  0(0,R10),0(R11)  Executed Instruction
00001402  D500 A000 95C8      00000000  000017C8    4923 MVCINCLC CLC    0(0,R10),MVCINOUT Executed Instruction
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4925 ************************************************************************
                                                  4926 *        Normal completion or Abnormal termination PSWs
                                                  4927 ************************************************************************


                                                  4929 EOJ      DWAITEND LOAD=YES          Normal completion
00001408                                          4931+EOJ      DS    0H
00001408  8200 9210                    00001410   4932+          LPSW  DWAT0010
00001410  000A0000 00000000                       4933+DWAT0010 PSW   0,0,2,0,X'000000'


                                                  4935 FAILDEV  DWAIT LOAD=YES,CODE=01     ENADEV failed
00001418                                          4936+FAILDEV  DS    0H
00001418  8200 9220                    00001420   4937+          LPSW  DWAT0011
00001420  000A0000 00010001                       4938+DWAT0011 PSW   0,0,2,0,X'010001'


                                                  4940 FAILIO   DWAIT LOAD=YES,CODE=02     RAWIO failed
00001428                                          4941+FAILIO   DS    0H
00001428  8200 9230                    00001430   4942+          LPSW  DWAT0012
00001430  000A0000 00010002                       4943+DWAT0012 PSW   0,0,2,0,X'010002'


                                                  4945 FAILTEST DWAIT LOAD=YES,CODE=BAD    Abnormal termination
00001438                                          4946+FAILTEST DS    0H
00001438  8200 9240                    00001440   4947+          LPSW  DWAT0013
00001440  000A0000 00010BAD                       4948+DWAT0013 PSW   0,0,2,0,X'010BAD'
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                 4950 ************************************************************************
                                                 4951 *        Initialize the CPU for I/O operations
                                                 4952 ************************************************************************

                                                 4954 IOINIT   IOINIT ,
00001448  B766 9250                   00001450  4955+IOINIT   LCTL  6,6,IOMK0014       Enable subchannel subclasses for interruptions
0000144C  47F0 9254                   00001454  4956+         B     IOMK0014+4
00001450                                        4957+IOMK0014 DS    0F
00001450  FF000000                              4958+         DC    XL4'FF000000'         All subchannel subclasses enabled

00001454  07FF                                  4960          BR    R15                   Return to caller

                                                 4962 ************************************************************************
                                                 4963 *        Enable the device, making it ready for use
                                                 4964 ************************************************************************

                                                 4966 ENADEV   ENADEV ENAOKAY,FAILDEV,REG=4
00001456  5810 929C                   0000149C  4967+ENADEV   L     1,FIND0015
0000145A  5840 3028                   00000028  4968+         $L    4,IOCBSIB             Locate where the SCHIB is to be stored
0000145E                    00000000            4969+         USING SCHIB,4
0000145E                                        4970+FINL0015 DS    0H   Retrieve Subchannel Information Block for desired device number
0000145E  B234 4000                   00000000  4971+         STSCH 0(4)                  Store the SCHIB for first subchannel
00001462  A774 FFDB                   00001418  4972+         $BC   B'0111',FAILDEV       Subchannel does not exist and device number not found
00001466  9101 4005                   00000005  4973+         TM    PMCW1_8,PMCWV         Is the subchannel device number valid?
0000146A  A784 0011                   0000148C  4974+         $BZ   FINN0015              ..No, check the next subchannel
0000146E  D501 4006 3004      00000006  00000004  4975+         CLC   PMCWDNUM,IOCBDEV      Is this the device number being sought?
00001474  A774 000C                   0000148C  4976+         $BNE  FINN0015              ..No, check the next subchannel
                                                 4977+* Subchannel found!
00001478  5010 3000                   00000000  4978+         ST    1,IOCBDID             Remember the subchannel so I/O can be done to it.
0000147C  9680 4005                   00000005  4979+         OI    PMCW1_8,PMCWE         Make sure it is enabled so I/O requests accepted
00001480  B232 4000                   00000000  4980+         MSCH  0(4)                  Enable the subchannel to the channel sub-system
00001484  A784 0010                   000014A4  4981+         $BC   B'1000',ENAOKAY       CC0 (SCHIB updated), device is ready.
00001488  A7F4 FFC8                   00001418  4982+         $B    FAILDEV               CC1,CC2,CC3 (SCHIB update failed), quit
0000148C                                        4983+FINN0015 DS    0H  Advance to next subchannel
0000148C  4110 1001                   00000001  4984+         LA    1,1(0,1)              Advance to next subchannel
00001490  5510 92A0                   000014A0  4985+         CL    1,FINM0015            Beyond maximum subchannel
00001494  A7D4 FFE5                   0000145E  4986+         $BNH  FINL0015              ..No, examine the next subchannel
00001498  A724 FFC0                   00001418  4987+         $BH   FAILDEV               ..Yes, failed to enable the device
0000149C                                        4988+         DROP  4                     Forget SCHIB addressing
0000149C  00010000                              4989+FIND0015 DC    A(X'00010000')        First subchannel subsystem ID
000014A0  0001FFFF                              4990+FINM0015 DC    A(X'0001FFFF')        Last subchannel subsystem ID

000014A4  07FF                                  4992 ENAOKAY  BR    R15                   Return to caller
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    4994 ********************************************************************************
                                                    4995 *         Structure used by RAWIO identifying
                                                    4996 *         the device and operation being performed
                                                    4997 ********************************************************************************


                                                    4999 IOCB_009 IOCB  X'009',CCW=CONPGM
000014A8  00000000                                  5000+IOCB_009 DC    A(0)            +0 Device Identifier (supplied by ENADEV macro)
000014AC  0009                                      5001+         DC    AL2(X'009')     +4 Device address or device number
000014AE  0000                                      5002+         DC    H'0'            +6 Must be zeros
000014B0  D3                                        5003+         DC    AL1(X'D3')      +8 Default detected unit errors
000014B1  3F                                        5004+         DC    AL1(X'3F')      +9 Default detected channel errors
000014B2  0000                                      5005+         DC    HL2'0'          +10 Accumulated unit and channel errors
000014B4  0000                                      5006+         DC    HL2'0'          +12 Tested unit and channel status
000014B6  00                                        5007+         DC    XL1'00'         +14 Accumulated subchannel status control from SCSW
000014B7  80                                        5008+         DC    XL1'80'         +15 Default unsoliticed wait condition
000014B8  00000000                                  5009+         DC    F'0'            +16 I/O status CCW address
000014BC  00000000                                  5010+         DC    F'0'            +20 residual count
000014C0  00001518                                  5011+         DC    A(IORB0016)     +24  Address where ORB is located
000014C4  00000000                                  5012+         DC    A(0)            +28  reserved
000014C8  000014D8                                  5013+         DC    A(IIRB0016)     +32 Address where IRB stored
000014CC  00000000                                  5014+         DC    A(0)            +36 reserved
000014D0  000014D8                                  5015+         DC    A(IIRB0016)     +40 Address where SCHIB stored
000014D4  00000000                                  5016+         DC    A(0)            +44 reserved
000014D8  00000000 00000000                         5017+IIRB0016 DC    16F'0'              Embedded shared IRB and SCHIB area
00001518                                            5019+IORB0016 DS    0XL12
00001518  00000000                                  5020+         DC    A(0)            Word 0 - Interruption Parameter
0000151C  00                                        5021+         DC    AL1((0)*16+B'0000')  Word 1, bits 0-7
0000151D  80                                        5022+         DC    BL1'10000000'   Word 1, bits 8-15
0000151E  FF                                        5023+         DC    AL1(255)        Word 1, bits 16-23
0000151F  00                                        5024+         DC    BL1'00000000'    Word 1, bits 24-31
00001520  000015B0                                  5025+         DC    AL4(CONPGM)     Word 2 - CCW address
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5027 ********************************************************************************
                                                    5028 *        Working Storage
                                                    5029 ********************************************************************************


00001524                                            5031          LTORG ,                  Literals pool
00001524  AABBCCDD                                  5032                =A(REG2PATT)
00001528  00000000                                  5033                =F'0'
0000152C  00050000                                  5034                =A(00+(5*K64))
00001530  00150000                                  5035                =A(MB+(5*K64))
00001534  00003000                                  5036                =A(SEGTABLS)
00001538  00003080                                  5037                =A(PAGETABS)
0000153C  00001000                                  5038                =A(PAGE)
00001540  00005000                                  5039                =A(PFPGBYTS)
00001544  000011A4                                  5040                =A(PFINSADR)
00001548  00000001                                  5041                =F'1'
0000154C  C3D3C340 40                               5042                =CL5'CLC'
00001551  C3D3C3D3 40                               5043                =CL5'CLCL'
00001556  D4E5C3C9 D5                               5044                =CL5'MVCIN'
0000155B  E3D9E340 40                               5045                =CL5'TRT'
00001560  04294967 296C                             5046                =P'4294967296'

                            00000400  00000001  5048 K        EQU   1024             One KB
                            00001000  00000001  5049 PAGE     EQU   (4*K)            Size of one page
                            00010000  00000001  5050 K64      EQU   (64*K)           64 KB
                            00100000  00000001  5051 MB       EQU   (K*K)             1 MB

                            000021FE  00000001  5053 TESTADDR EQU   (2*PAGE+X'200'-2)  Where test/subtest numbers will go
                            000021FD  00000001  5054 TIMEADDR EQU   (TESTADDR-1)       Address of timing tests option flag

                            00200000  00000001  5056 MAINSIZE EQU   (2*MB)                   Minimum required storage size
                            00000020  00000001  5057 NUMPGTBS EQU   ((MAINSIZE+K64-1)/K64)   Number of Page Tables needed
                            00000002  00000001  5058 NUMSEGTB EQU   ((NUMPGTBS*4)/(16*4))    Number of Segment Tables
                            00003000  00000001  5059 SEGTABLS EQU   (3*PAGE)                 Segment Tables Origin
                            00003080  00000001  5060 PAGETABS EQU   (SEGTABLS+(NUMPGTBS*4))  Page Tables Origin
00001568  00B00060                                  5061 CRLREG0  DC    0A(0),XL4'00B00060'      Control Register 0
0000156C  00003002                                  5062 CTLREG1  DC    A(SEGTABLS+NUMSEGTB)     Control Register 1

00001570  00002710                                  5064 NUMLOOPS DC    F'10000'         10,000 * 100 = 1,000,000

00001578  BBBBBBBB BBBBBBBB                         5066 BEGCLOCK DC    0D'0',8X'BB'     Begin
00001580  EEEEEEEE EEEEEEEE                         5067 ENDCLOCK DC    0D'0',8X'EE'     End
00001588  DDDDDDDD DDDDDDDD                         5068 DURATION DC    0D'0',8X'DD'     Diff
00001590  FFFFFFFF FFFFFFFF                         5069 OVERHEAD DC    0D'0',8X'FF'     Overhead

00001598  00000000 0000000C                         5071 TICKSAAA DC    PL8'0'           Clock ticks high part
000015A0  00000000 0000000C                         5072 TICKSBBB DC    PL8'0'           Clock ticks low part
000015A8  00000000 0000000C                         5073 TICKSTOT DC    PL8'0'           Total clock ticks

000015B0  09000044 000015B8                         5075 CONPGM   CCW1  X'09',PRTLINE,0,L'PRTLINE
000015B8  40404040 40404040                         5076 PRTLINE  DC    C'         1,000,000 iterations of XXXXX took 999,999,999 microseconds'
000015FC  40202020 6B202020                         5077 EDIT     DC    X'402020206B2020206B202120'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   5079 ************************************************************************
                                                   5080 *        CLC Test Parameters:   A(operand-1),A(operand-2)
                                                   5081 ************************************************************************

00001608  00010000 00110000                        5083 CLC1     DC    A(1*K64),A(MB+(1*K64))                          both equal
00001610  00010000 00110000                        5084 CLC2     DC    A(1*K64),A(MB+(1*K64))                          both equal
00001618  0000FFF4 0010FFDE                        5085 CLCBOTH  DC    A(1*K64-12),A(MB+(1*K64)-34)                    both equal
00001620  00010000 0010FFDE                        5086 CLCOP2   DC    A(1*K64),A(MB+(1*K64)-34)                       both equal

00001628  00020000 00120000                        5088 CLC4     DC    A(2*K64),A(MB+(2*K64))                            op1 HIGH
00001630  00030000 00130000                        5089 CLC8     DC    A(3*K64),A(MB+(3*K64))                            op1 LOW!
00001638  00040000 00140000                        5090 CLC256   DC    A(4*K64),A(MB+(4*K64))                            op1 HIGH
00001640  0004FFF4 00150000                        5091 CLCOP1   DC    A(5*K64-12),A(MB+(5*K64))                         op1 HIGH


                                                   5093 ************************************************************************
                                                   5094 *        MVCIN Test Parameters
                                                   5095 ************************************************************************
                                                   5096          PRINT DATA
00001648  00010000 00110000                        5097 INV1     DC    A(1*K64),A(MB+(1*K64)+1-1),A(1-1),A(MB+(1*K64))
00001650  00000000 00110000
00001658  00020000 00120001                        5098 INV2     DC    A(2*K64),A(MB+(2*K64)+2-1),A(2-1),A(MB+(2*K64))
00001660  00000001 00120000
00001668  00030000 00130003                        5099 INV4     DC    A(3*K64),A(MB+(3*K64)+4-1),A(4-1),A(MB+(3*K64))
00001670  00000003 00130000
00001678  00040000 00140007                        5100 INV8     DC    A(4*K64),A(MB+(4*K64)+8-1),A(8-1),A(MB+(4*K64))
00001680  00000007 00140000
00001688  00050000 001500FF                        5101 INV256   DC    A(5*K64),A(MB+(5*K64)+256-1),A(256-1),A(MB+(5*K64))
00001690  000000FF 00150000

00001698  0005FFF4 001600DD                        5103 INVBOTH  DC    A(6*K64-12),A(MB+(6*K64)-34+256-1),A(256-1),A(MB+(6*K64)-34)
000016A0  000000FF 0015FFDE
000016A8  0006FFF4 001700FF                        5104 INVOP1   DC    A(7*K64-12),A(MB+(7*K64)+256-1),A(256-1),A(MB+(7*K64))
000016B0  000000FF 00170000
000016B8  00080000 001800DD                        5105 INVOP2   DC    A(8*K64),A(MB+(8*K64)-34+256-1),A(256-1),A(MB+(8*K64)-34)
000016C0  000000FF 0017FFDE
                                                   5106          PRINT NODATA
000016C8                                           5107 MVCININ  DC    0XL256'00'
000016C8  00010203 04050607                        5108          DC    XL16'000102030405060708090A0B0C0D0E0F'
000016D8  10111213 14151617                        5109          DC    XL16'101112131415161718191A1B1C1D1E1F'
000016E8  20212223 24252627                        5110          DC    XL16'202122232425262728292A2B2C2D2E2F'
000016F8  30313233 34353637                        5111          DC    XL16'303132333435363738393A3B3C3D3E3F'
                                                   5112          PRINT OFF
                                                   5125          PRINT ON
000017C8                                           5126 MVCINOUT DC    0XL256'00'
000017C8  FFFEFDFC FBFAF9F8                        5127          DC    XL16'FFFEFDFCFBFAF9F8F7F6F5F4F3F2F1F0'
000017D8  EFEEEDEC EBEAE9E8                        5128          DC    XL16'EFEEEDECEBEAE9E8E7E6E5E4E3E2E1E0'
000017E8  DFDEDDDC DBDAD9D8                        5129          DC    XL16'DFDEDDDCDBDAD9D8D7D6D5D4D3D2D1D0'
000017F8  CFCECDCC CBCAC9C8                        5130          DC    XL16'CFCECDCCCBCAC9C8C7C6C5C4C3C2C1C0'
                                                   5131          PRINT OFF
                                                   5144          PRINT ON
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    5146 ********************************************************************************
                                                    5147 *        TRTTEST DSECT
                                                    5148 ********************************************************************************


                                                    5150 TRTTEST  DSECT ,


00000000  00000000                                  5152 OP1DATA  DC    A(0)           Pointer to Operand-1 data
00000004  00000000                                  5153 OP1LEN   DC    F'0'           How much data is there - 1
00000008  00000000                                  5154 OP1WHERE DC    A(0)           Where Operand-1 data should be placed


0000000C  00000000                                  5156 OP2DATA  DC    A(0)           Pointer to Operand-2 data
00000010  00000000                                  5157 OP2LEN   DC    F'0'           How much data is there - 1
00000014  00000000                                  5158 OP2WHERE DC    A(0)           Where Operand-2 data should be placed


00000018  00000000                                  5160 EXLEN    DC    F'0'           Operand-1 test length (EX instruction)
0000001C  00000000                                  5161 FAILMASK DC    A(0)           Failure Branch on Condition mask


00000020  00000000 00000000                         5163 ENDREGS  DC    A(0),XL4'00'   Ending R1/R2 register values


                    00000028  00000001  5165 TRTNEXT  EQU   *              Start of next table entry...


                    AABBCCDD  00000001  5167 REG2PATT EQU   X'AABBCCDD'    Register 2 starting/ending CC0 value
                    000000DD  00000001  5168 REG2LOW  EQU         X'DD'    (last byte above)


                    00000000  00003000  5170 CLCLetal CSECT ,
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    5172 ************************************************************************
                                                    5173 *        TRT Testing Control tables   (ref: TRTDSECT)
                                                    5174 ************************************************************************
                                                    5175          PRINT DATA
000018C8                                            5176 TRTCTL   DC    0A(0)    start of table




000018C8  00001A0C 00000000                         5178 TRT1     DC    A(TRTOP10),A(001-1),A(00+(1*K64))
000018D0  00010000
000018D4  00001D0C 000000FF                         5179          DC    A(TRTOP20),A(256-1),A(MB+(1*K64))
000018DC  00110000
000018E0  00000000 00000007                         5180          DC               A(001-1),A(7) CC0
000018E8  00000000 AABBCCDD                         5181          DC                        A(0),A(REG2PATT)



000018F0  00001A0C 00000000                         5183 TRT2     DC    A(TRTOP10),A(002-2),A(00+(2*K64))
000018F8  00020000
000018FC  00001D0C 000000FF                         5184          DC    A(TRTOP20),A(256-1),A(MB+(2*K64))
00001904  00120000
00001908  00000001 00000007                         5185          DC               A(002-1),A(7) CC0
00001910  00000000 AABBCCDD                         5186          DC                        A(0),A(REG2PATT)



00001918  00001A0C 00000003                         5188 TRT4     DC    A(TRTOP10),A(004-1),A(00+(3*K64))
00001920  00030000
00001924  00001D0C 000000FF                         5189          DC    A(TRTOP20),A(256-1),A(MB+(3*K64))
0000192C  00130000
00001930  00000003 00000007                         5190          DC               A(004-1),A(7) CC0
00001938  00000000 AABBCCDD                         5191          DC                        A(0),A(REG2PATT)




00001940  00001A0C 00000007                         5193 TRT8     DC    A(TRTOP10),A(008-1),A(00+(4*K64))
00001948  00040000
0000194C  00001D0C 000000FF                         5194          DC    A(TRTOP20),A(256-1),A(MB+(4*K64))
00001954  00140000
00001958  00000007 00000007                         5195          DC               A(008-1),A(7) CC0
00001960  00000000 AABBCCDD                         5196          DC                        A(0),A(REG2PATT)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001968  00001A0C 000000FF                        5198 TRT256   DC    A(TRTOP10),A(256-1),A(00+(5*K64))
00001970  00050000
00001974  00001D0C 000000FF                        5199          DC    A(TRTOP20),A(256-1),A(MB+(5*K64))
0000197C  00150000
00001980  000000FF 00000007                        5200          DC               A(256-1),A(7) CC0
00001988  00000000 AABBCCDD                        5201          DC                    A(0),A(REG2PATT)



00001990  00001B0C 000000FF                        5203 TRTBTH   DC    A(TRTOP111),A(256-1),A(00+(6*K64)-12)  both cross page
00001998  0005FFF4
0000199C  00001E0C 000000FF                        5204          DC    A(TRTOP211),A(256-1),A(MB+(6*K64)-34)  both cross page
000019A4  0015FFDE
000019A8  000000FF 0000000B                        5205          DC                A(256-1),A(11) CC1 = stop, scan incomplete
000019B0  00060005 AABBCC11                        5206          DC                     A(00+(6*K64)-12+X'11'),A(REG2PATT-REG2LOW+X'11')



000019B8  00001C0C 000000FF                        5208 TRTOP1   DC    A(TRTOP1F0),A(256-1),A(00+(7*K64)-12)  only op1 crosses
000019C0  0006FFF4
000019C4  00001F0C 000000FF                        5209          DC    A(TRTOP2F0),A(256-1),A(MB+(7*K64))
000019CC  00170000
000019D0  000000FF 0000000D                        5210          DC                A(256-1),A(13) CC2 = stopped on last byte
000019D8  000700F3 AABBCCF0                        5211          DC                     A(00+(7*K64)-12+255),A(REG2PATT-REG2LOW+X'F0')



000019E0  00001B0C 000000FF                        5213 TRTOP2   DC    A(TRTOP111),A(256-1),A(00+(8*K64))
000019E8  00080000
000019EC  00001E0C 000000FF                        5214          DC    A(TRTOP211),A(256-1),A(MB+(8*K64)-34)  only op2 crosses
000019F4  0017FFDE
000019F8  000000FF 0000000B                        5215          DC                A(256-1),A(11) CC1 = stop, scan incomplete
00001A00  00080011 AABBCC11                        5216          DC                     A(00+(8*K64)+X'11'),A(REG2PATT-REG2LOW+X'11')



00001A08  00000000                                 5218          DC    A(0)     end of table
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   5220 ********************************************************************************
                                                   5221 *        TRT op1 scan data...
                                                   5222 ********************************************************************************

00001A0C  78125634 78125634                        5224 TRTOP10  DC    64XL4'78125634'    (CC0)
00001A14  78125634 78125634
00001A1C  78125634 78125634
00001A24  78125634 78125634
00001A2C  78125634 78125634
00001A34  78125634 78125634
00001A3C  78125634 78125634
00001A44  78125634 78125634
00001A4C  78125634 78125634
00001A54  78125634 78125634
00001A5C  78125634 78125634
00001A64  78125634 78125634
00001A6C  78125634 78125634
00001A74  78125634 78125634
00001A7C  78125634 78125634
00001A84  78125634 78125634
00001A8C  78125634 78125634
00001A94  78125634 78125634
00001A9C  78125634 78125634
00001AA4  78125634 78125634
00001AAC  78125634 78125634
00001AB4  78125634 78125634
00001ABC  78125634 78125634
00001AC4  78125634 78125634
00001ACC  78125634 78125634
00001AD4  78125634 78125634
00001ADC  78125634 78125634
00001AE4  78125634 78125634
00001AEC  78125634 78125634
00001AF4  78125634 78125634
00001AFC  78125634 78125634
00001B04  78125634 78125634

00001B0C  78125634 78125634                        5226 TRTOP111 DC    04XL4'78125634',X'00110000',59XL4'78125634'    (CC1)
00001B14  78125634 78125634
00001B1C  00110000 78125634
00001B24  78125634 78125634
00001B2C  78125634 78125634
00001B34  78125634 78125634
00001B3C  78125634 78125634
00001B44  78125634 78125634
00001B4C  78125634 78125634
00001B54  78125634 78125634
00001B5C  78125634 78125634
00001B64  78125634 78125634
00001B6C  78125634 78125634
00001B74  78125634 78125634
00001B7C  78125634 78125634
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00001B84  78125634 78125634
00001B8C  78125634 78125634
00001B94  78125634 78125634
00001B9C  78125634 78125634
00001BA4  78125634 78125634
00001BAC  78125634 78125634
00001BB4  78125634 78125634
00001BBC  78125634 78125634
00001BC4  78125634 78125634
00001BCC  78125634 78125634
00001BD4  78125634 78125634
00001BDC  78125634 78125634
00001BE4  78125634 78125634
00001BEC  78125634 78125634
00001BF4  78125634 78125634
00001BFC  78125634 78125634
00001C04  78125634 78125634

00001C0C  78125634 78125634                    5228 TRTOP1F0 DC    63XL4'78125634',X'000000F0'    (CC2)
00001C14  78125634 78125634
00001C1C  78125634 78125634
00001C24  78125634 78125634
00001C2C  78125634 78125634
00001C34  78125634 78125634
00001C3C  78125634 78125634
00001C44  78125634 78125634
00001C4C  78125634 78125634
00001C54  78125634 78125634
00001C5C  78125634 78125634
00001C64  78125634 78125634
00001C6C  78125634 78125634
00001C74  78125634 78125634
00001C7C  78125634 78125634
00001C84  78125634 78125634
00001C8C  78125634 78125634
00001C94  78125634 78125634
00001C9C  78125634 78125634
00001CA4  78125634 78125634
00001CAC  78125634 78125634
00001CB4  78125634 78125634
00001CBC  78125634 78125634
00001CC4  78125634 78125634
00001CCC  78125634 78125634
00001CD4  78125634 78125634
00001CDC  78125634 78125634
00001CE4  78125634 78125634
00001CEC  78125634 78125634
00001CF4  78125634 78125634
00001CFC  78125634 78125634
00001D04  78125634 000000F0
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   5230 ********************************************************************************
                                                   5231 *        TRT op2 stop tables...
                                                   5232 ********************************************************************************

00001D0C  00000000 00000000                        5234 TRTOP20  DC    256X'00'     no stop
00001D14  00000000 00000000
00001D1C  00000000 00000000
00001D24  00000000 00000000
00001D2C  00000000 00000000
00001D34  00000000 00000000
00001D3C  00000000 00000000
00001D44  00000000 00000000
00001D4C  00000000 00000000
00001D54  00000000 00000000
00001D5C  00000000 00000000
00001D64  00000000 00000000
00001D6C  00000000 00000000
00001D74  00000000 00000000
00001D7C  00000000 00000000
00001D84  00000000 00000000
00001D8C  00000000 00000000
00001D94  00000000 00000000
00001D9C  00000000 00000000
00001DA4  00000000 00000000
00001DAC  00000000 00000000
00001DB4  00000000 00000000
00001DBC  00000000 00000000
00001DC4  00000000 00000000
00001DCC  00000000 00000000
00001DD4  00000000 00000000
00001DDC  00000000 00000000
00001DE4  00000000 00000000
00001DEC  00000000 00000000
00001DF4  00000000 00000000
00001DFC  00000000 00000000
00001E04  00000000 00000000

00001E0C  00000000 00000000                        5236 TRTOP211 DC    17X'00',X'11',238X'00'     stop on X'11'
00001E14  00000000 00000000
00001E1C  00110000 00000000
00001E24  00000000 00000000
00001E2C  00000000 00000000
00001E34  00000000 00000000
00001E3C  00000000 00000000
00001E44  00000000 00000000
00001E4C  00000000 00000000
00001E54  00000000 00000000
00001E5C  00000000 00000000
00001E64  00000000 00000000
00001E6C  00000000 00000000
00001E74  00000000 00000000
00001E7C  00000000 00000000
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00001E84  00000000 00000000
00001E8C  00000000 00000000
00001E94  00000000 00000000
00001E9C  00000000 00000000
00001EA4  00000000 00000000
00001EAC  00000000 00000000
00001EB4  00000000 00000000
00001EBC  00000000 00000000
00001EC4  00000000 00000000
00001ECC  00000000 00000000
00001ED4  00000000 00000000
00001EDC  00000000 00000000
00001EE4  00000000 00000000
00001EEC  00000000 00000000
00001EF4  00000000 00000000
00001EFC  00000000 00000000
00001F04  00000000 00000000

00001F0C  00000000 00000000                       5238 TRTOP2F0 DC    240X'00',X'F0',15X'00'     stop on X'F0'
00001F14  00000000 00000000
00001F1C  00000000 00000000
00001F24  00000000 00000000
00001F2C  00000000 00000000
00001F34  00000000 00000000
00001F3C  00000000 00000000
00001F44  00000000 00000000
00001F4C  00000000 00000000
00001F54  00000000 00000000
00001F5C  00000000 00000000
00001F64  00000000 00000000
00001F6C  00000000 00000000
00001F74  00000000 00000000
00001F7C  00000000 00000000
00001F84  00000000 00000000
00001F8C  00000000 00000000
00001F94  00000000 00000000
00001F9C  00000000 00000000
00001FA4  00000000 00000000
00001FAC  00000000 00000000
00001FB4  00000000 00000000
00001FBC  00000000 00000000
00001FC4  00000000 00000000
00001FCC  00000000 00000000
00001FD4  00000000 00000000
00001FDC  00000000 00000000
00001FE4  00000000 00000000
00001FEC  00000000 00000000
00001FF4  00000000 00000000
00001FFC  F0000000 00000000
00002004  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    5240 ********************************************************************************
                                                    5241 *        CLCL Test Parameters
                                                    5242 ********************************************************************************

0000200C  00060000 00000001                         5244 CLCL1    DC    A(6*K64),A(1),A(MB+(6*K64)),A(1)             both equal
00002014  00160000 00000001

0000201C  00060000 00000002                         5246 CLCL2    DC    A(6*K64),A(2),A(MB+(6*K64)),A(2)             both equal
00002024  00160000 00000002

0000202C  00060000 00000100                         5248 CLCL256  DC    A(6*K64),A(256),A(MB+(6*K64)),A(256)         both equal
00002034  00160000 00000100

0000203C  00060000 00000400                         5250 CLCL1K   DC    A(6*K64),A(K),A(MB+(6*K64)),A(K)             both equal
00002044  00160000 00000400

0000204C  0005FFF4 00010000                         5252 CLCLBOTH DC    A(6*K64-12),A(K64),A(MB+(6*K64)-34),A(K64)   both equal
00002054  0015FFDE 00010000

0000205C  00060000 00001000                         5254 CLCLOP2  DC    A(6*K64),A(PAGE),A(MB+(6*K64)-34),A(K64)     both equal
00002064  0015FFDE 00010000

0000206C  00070000 00000004                         5256 CLCL4    DC    A(7*K64),A(4),A(MB+(7*K64)),A(4)              op1 HIGH
00002074  00170000 00000004

0000207C  00080000 00000008                         5258 CLCL8    DC    A(8*K64),A(8),A(MB+(8*K64)),A(8)              op1 LOW!
00002084  00180000 00000008

0000208C  0008FFF4 00010000                         5260 CLCLOP1  DC    A(9*K64-12),A(K64),A(MB+(9*K64)),A(PAGE)      op1 HIGH
00002094  00190000 00001000

0000209C  000A0000 00010000                         5262 CLCLPF   DC    A(10*K64),A(K64),A(MB+(10*K64)),A(K64)      page fault
000020A4  001A0000 00010000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5264 ************************************************************************
                                                    5265 *        CLCL Expected Ending Register Values
                                                    5266 ************************************************************************

000020AC  00060001 00000000                         5268 ECLCL1   DC    A(6*K64+1),A(0),A(MB+(6*K64)+1),A(0)         both equal
000020B4  00160001 00000000

000020BC  00060002 00000000                         5270 ECLCL2   DC    A(6*K64+2),A(0),A(MB+(6*K64)+2),A(0)         both equal
000020C4  00160002 00000000

000020CC  00060100 00000000                         5272 ECLCL256 DC    A(6*K64+256),A(0),A(MB+(6*K64)+256),A(0)     both equal
000020D4  00160100 00000000

000020DC  00060400 00000000                         5274 ECLCL1K  DC    A(6*K64+K),A(0),A(MB+(6*K64)+K),A(0)         both equal
000020E4  00160400 00000000

000020EC  0006FFF4 00000000                         5276 ECLCLBTH DC    A(6*K64-12+K64),A(0),A(MB+(6*K64)-34+K64),A(0) bth equl
000020F4  0016FFDE 00000000

000020FC  00061000 00000000                         5278 ECLCLOP2 DC    A(6*K64+PAGE),A(0),A(MB+(6*K64)-34+K64),A(0) both equal
00002104  0016FFDE 00000000

0000210C  00070003 00000001                         5280 ECLCL4   DC    A(7*K64+4-1),A(1),A(MB+(7*K64)+4-1),A(1)       op1 HIGH
00002114  00170003 00000001

0000211C  00080007 00000001                         5282 ECLCL8   DC    A(8*K64+8-1),A(1),A(MB+(8*K64)+8-1),A(1)       op1 LOW!
00002124  00180007 00000001

0000212C  0009FFF3 00000001                         5284 ECLCLOP1 DC    A(9*K64-12+K64-1),A(1),A(MB+(9*K64)+PAGE),A(0) op1 HIGH
00002134  00191000 00000000

0000213C  000B0000 00000000                         5286 ECLCLPF  DC    A(10*K64+K64),A(0),A(MB+(10*K64)+K64),A(0)   page fault
00002144  001B0000 00000000

0000214C  00000000 00000000                         5288 CLCLEND  DC    4F'0'          (actual ending register values)
00002154  00000000 00000000
                            00000005  00000001    5289 PFPAGE   EQU   5              (page the Page Fault should occur on)
                            00005000  00000001    5290 PFPGBYTS EQU   (PFPAGE*PAGE)  (number of bytes into operand-1)
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5292 ********************************************************************************
                                                    5293 *        Fixed storage locations
                                                    5294 ********************************************************************************


0000215C                      0000215C  000021FD  5296          ORG   CLCLetal+TIMEADDR      (s/b @ X'21FD')

000021FD  00                                      5298 TIMEOPT  DC    X'00'      Set to non-zero to run timing tests




000021FE                      000021FE  000021FE  5300          ORG   CLCLetal+TESTADDR      (s/b @ X'21FE', X'21FF')

000021FE  00                                      5302 TESTNUM  DC    X'00'      Test number of active test
000021FF  00                                      5303 SUBTEST  DC    X'00'      Active test sub-test number


00002200                      00002200  00003000  5305          ORG   CLCLetal+SEGTABLS      (s/b @ X'3000')
00003000  00                                      5307 DATTABS  DC    X'00'      Segment and Page Tables will go here...
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5309 ********************************************************************************
                                                    5310 *        IOCB DSECT
                                                    5311 ********************************************************************************

                                                    5313          DSECTS NAME=IOCB
                                                    5315+IOCB     DSECT
                                                    5316+*     Field usage by: CH SC Description (R->program read-only, X->program read/writ
00000000                                            5317+IOCBDID  DS    0F  +0     R  Device Identifier - Subsystem ID for channel subsystem
00000000  0000                                      5318+         DS    H   +0  R      reserved - must be zeros
00000002  0000                                      5319+IOCBDV   DS    H   +2  R      Channel Unit Device address of I/O operation
00000004  0000                                      5320+IOCBDEV  DS    H   +4  X  X  Device address or device number (R after ENADEV)
00000006  0000                                      5321+IOCBZERO DS    H   +6  R  R  Must be zeros
00000008  00                                        5322+IOCBUM   DS    X   +8  X  X  Unit status test mask
00000009  00                                        5323+IOCBCM   DS    X   +9  X  X  Channel status test mask
0000000A                                            5324+IOCBST   DS    0H  +10 X  X  Input/Output unit and channel status accumulation
0000000A  00                                        5325+IOCBUS   DS    X   +10 R  R  Accumulated unit status
0000000B  00                                        5326+IOCBCS   DS    X   +11 R  R  Accumulated channel status
0000000C  00                                        5327+IOCBUT   DS    X   +14 R  R  Used to test unit status
0000000D  00                                        5328+IOCBCT   DS    X   +13 R  R  Used to test channel status
0000000E  00                                        5329+IOCBSC   DS    X   +14    R  Accumulted subchanel status control
0000000F  00                                        5330+IOCBWAIT DS    X   +15 X  X  Recognized unsolicited interruption unit status events
00000010  00000000                                  5331+IOCBSCCW DS    A   +16 R  R  I/O status CCW address
00000014                                            5332+IOCBSCNT DS    0F  +20 R  R  I/O status residual count as a positive full word
00000014  0000                                      5333+         DS    H   +20 R     reserved must be zeros
00000016  0000                                      5334+IOCBRCNT DS    H   +22 R     I/O status residual count as an unsigned halfword
00000018                                            5335+IOCBCAW  DS    0A  +24 X     Channel Address word
00000018  00000000 00000000                         5336+IOCBORB  DS    AD  +24    X  Address of the ORB for channel subsystem I/O
00000020  00000000 00000000                         5337+IOCBIRB  DS    AD  +32    X  Channel subsystem IRB address
00000028  00000000 00000000                         5338+IOCBSIB  DS    AD  +40    X  Channel subsystem SCHIB address
                            00000030  00000001      5339+IOCBL    EQU   *-IOCB  Length of IOCB control block (48) without embedded structures
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  5341 ********************************************************************************
                                                  5342 *        ORB DSECT
                                                  5343 ********************************************************************************

                                                  5345          DSECTS NAME=ORB
                                                  5347+ORB      DSECT
00000000  00000000                                5348+ORBPARM  DC    F'0'     Word 0, bits 0-31

00000004  00                                      5350+ORB1_0   DC    X'00'    Word 1, bits 0-7
                            000000F0  00000001    5351+ORBKEYM  EQU   X'F0'    Word 1, bits 0-3   - Storage Key Mask
                            00000008  00000001    5352+ORBS     EQU   X'08'    Word 1, bit 4      - Suspend Control
                            00000004  00000001    5353+ORBC     EQU   X'04'    Word 1, bit 5      - Streaming Mode Control
                            00000002  00000001    5354+ORBM     EQU   X'02'    Word 1, bit 6      - Modification Control
                            00000001  00000001    5355+ORBY     EQU   X'01'    Word 1, bit 7      - Synchronization Control

00000005  00                                      5357+ORB1_8   DC    X'00'    Word 1, bits 8-15
                            00000080  00000001    5358+ORBF     EQU   X'80'    Word 1, bit 8      - CCW Format-Control
                            00000040  00000001    5359+ORBP     EQU   X'40'    Word 1, bit 9      - Pre-fetch control
                            00000020  00000001    5360+ORBI     EQU   X'20'    Word 1, bit 10     - Initial-status Interruption Control
                            00000010  00000001    5361+ORBA     EQU   X'10'    Word 1, bit 11     - Address Limit Checking Control
                            00000008  00000001    5362+ORBU     EQU   X'08'    Word 1, bit 12     - Suppress-suspended-interruption control
                            00000004  00000001    5363+ORBB     EQU   X'04'    Word 1, bit 13     - Channel-Program-Type Control
                            00000002  00000001    5364+ORBH     EQU   X'02'    Word 1, bit 14     - Format 2-IDAW Control
                            00000001  00000001    5365+ORBT     EQU   X'01'    Word 1, bit 15     - 2K-IDAW control
00000006  00                                      5366+ORBLPM   DC    X'00'    Word 1, bits 16-23 - Logical Path Mask
00000007  00                                      5367+ORRB1_24 DC    X'00'    Word 1, bits 24-31
                            00000080  00000001    5368+ORBL     EQU   X'80'    Word 1, bit 24     - Incorrect Length Suppression Mode
                            0000007F  00000001    5369+ORBRSV3  EQU   X'7F'    Word 1, bits 25-31 - reserved must be zeros
                            00000040  00000001    5370+ORBD     EQU   X'40'    Word 1, bit 25     - MIDAW Addressing Control
                            0000003E  00000001    5371+ORBRSV26 EQU   X'3E'    Word 1, bits 26-30 - reserved must be zeros
                            0000007E  00000001    5372+ORBRSV25 EQU   X'7E'    Word 1, bits 25-30 - reserved must be zeros
                            00000001  00000001    5373+ORBX     EQU   X'01'    Word 1, bit 31     - ORB-extension control

00000008  00000000                                5375+ORBCCW   DC    A(0)     Word 2, bits 1-31  - Channel Program Address
                            00000080  00000001    5376+ORBRSV4  EQU   X'80'    Word 2, bit 0      - reserved must be zero
                            0000000C  00000001    5377+ORBLEN   EQU   *-ORB Length of standard ORB
                                                  5378+* Extended ORB fields
0000000C  00                                      5379+ORBCSS   DC    X'00'    Word 3, bits 0-7   - Channel Subsystem Priority
0000000D  00                                      5380+ORBRSV5  DC    X'00'    Word 3, bits 8-15  - reserved must be zeros
0000000E                                          5381+ORBPGM   DC    0X'00'   Word 3, bits 16-23 - Transport mode reserves for program us
0000000E  00                                      5382+ORBCU    DC    X'00'    Word 3, bits 16-23 - Control Unit Priority
0000000F  00                                      5383+ORBRSV6  DC    X'00'    Word 3, bits 24-31 - reserved must be zeros
00000010  00000000 00000000                       5384+ORBRSV7  DC    XL16'00' Words 4-7          - reserved must be zeros
00000018  00000000 00000000
                            00000020  00000001    5385+ORBXLEN  EQU   *-ORB Length of extended ORB
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  5388 ********************************************************************************
                                                  5389 *        IRB DSECT
                                                  5390 ********************************************************************************

                                                  5392          DSECTS NAME=IRB
                                                  5394+IRB      DSECT Interruption          Response Block
00000000  00000000 00000000                       5395+IRBSCSW  DC    XL12'00' Words 0-2 - Subchannel Status Word (Defined by DSECT SCSW)
00000008  00000000
0000000C  00000000 00000000                       5396+IRBESW   DC    XL20'00' Words 3-7 - Extended Status Word
00000014  00000000 00000000
0000001C  00000000
00000020  00000000 00000000                       5397+IRBECW   DC    XL32'00' Words 8-15 - Extended Control Word
00000028  00000000 00000000
00000030  00000000 00000000
00000038  00000000 00000000
                             00000040  00000001  5398+IRBL     EQU   *-IRB    IRB Length
00000040  00000000 00000000                       5399+IRBEMW   DC    XL32'00' Words 16-23 - Extended Measurement Word
00000048  00000000 00000000
00000050  00000000 00000000
00000058  00000000 00000000
                             00000060  00000001  5400+IRBXL    EQU   *-IRB    Extended IRB Length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   5403 ********************************************************************************
                                                   5404 *        SCSW DSECT
                                                   5405 ********************************************************************************

                                                   5407          DSECTS NAME=SCSW
                                                   5409+SCSW     DSECT Subchannel          Status Word
00000000  00                                       5410+SCSWFLAG DC    X'00'    Flags
                                00000F0  00000001  5411+SCSWKEYM EQU   X'F0'    Storage Key Mask of subchannel storage key
                                00000008 00000001  5412+SCSWSUSC EQU   X'08'    Suspend Control
                                00000004 00000001  5413+SCSWESWF EQU   X'04'    Extended Status Word Format
                                00000003 00000001  5414+SCSWDCCM EQU   X'03'    Deferred condiont code mask
                                00000000 00000001  5415+SCSWDCC0 EQU   X'00'    Normal I/O interruption
                                00000001 00000001  5416+SCSWDCC1 EQU   X'01'    Deferred condition code is 1
                                00000003 00000001  5417+SCSWDCC3 EQU   X'03'    Deferred condition code is 3

00000001  00                                       5419+SCSWCTLS DC    X'00'    General Controls
                                00000080 00000001  5420+SCSWCCWF EQU   X'80'    CCW Format control when ...
                                00000040 00000001  5421+SCSWCCWP EQU   X'40'    CCW Prefetch Control
                                00000020 00000001  5422+SCSWISIC EQU   X'20'    Initial-Status-Interruption Control
                                00000010 00000001  5423+SCSWALKC EQU   X'10'    Address-Limit-Checking Control
                                00000008 00000001  5424+SCSWSSIC EQU   X'08'    Suppress suspended interruption
                                00000004 00000001  5425+SCSW0CC  EQU   X'04'    Zero-Condition Code
                                00000002 00000001  5426+SCSWECWC EQU   X'02'    Extended Control Word control
                                00000001 00000001  5427+SCSWPNOP EQU   X'01'    Path Not Operational

00000002  00                                       5429+SCSW1    DC    X'00'    Control Byte 1
                                00000070 00000001  5430+SCSWFM   EQU   X'70'    Functional Control Mask
                                00000040 00000001  5431+SCSWFS   EQU   X'40'    Function Control - Start Function
                                00000020 00000001  5432+SCSWFH   EQU   X'20'    Function Control - Halt Function
                                00000010 00000001  5433+SCSWFC   EQU   X'10'    Function Control - Clear Function
                                00000008 00000001  5434+SCSWARP  EQU   X'08'    Activity Control - Resume pending
                                00000004 00000001  5435+SCSWASP  EQU   X'04'    Activity Control - Start pending
                                00000002 00000001  5436+SCSWAHP  EQU   X'02'    Activity Control - Halt pending
                                00000001 00000001  5437+SCSWACP  EQU   X'01'    Activity Control - Clear pending
00000003  00                                       5438+SCSW2    DC    X'00'    Control Byte 2
                                00000080 00000001  5439+SCSWASA  EQU   X'80'    Activity Control - Subchannel Active
                                00000040 00000001  5440+SCSWADA  EQU   X'40'    Activity Control - Device Active
                                00000020 00000001  5441+SCSWASUS EQU   X'20'    Activity Control - Suspended
                                00000010 00000001  5442+SCSWSAS  EQU   X'10'    Status Control   - Alert Status
                                00000008 00000001  5443+SCSWSINT EQU   X'08'    Status Control   - Intermediate Status
                                00000004 00000001  5444+SCSWSPRI EQU   X'04'    Status Control   - Primary Status
                                00000002 00000001  5445+SCSWSSEC EQU   X'02'    Status Control   - Secondary Status
                                00000001 00000001  5446+SCSWSPEN EQU   X'01'    Status Control   - Status Pending

00000004  00000000                                 5448+SCSWCCW  DC    A(0)     CCW Address

00000008  00                                       5450+SCSWUS   DC    X'00'    Unit Status
                                00000080 00000001  5451+SCSWATTN EQU   X'80'    Attention
                                00000040 00000001  5452+SCSWSM   EQU   X'40'    Status modifier
                                00000020 00000001  5453+SCSWCUE  EQU   X'20'    Control-unit end
                                00000010 00000001  5454+SCSWBUSY EQU   X'10'    Busy
                                00000008 00000001  5455+SCSWCE   EQU   X'08'    Channel end
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                               00000004  00000001 5456+SCSWDE   EQU   X'04'    Device end
                               00000002  00000001 5457+SCSWUC   EQU   X'02'    Unit check
                               00000001  00000001 5458+SCSWUX   EQU   X'01'    Unit exception

00000009  00                                      5460+SCSWCS   DC    X'00'    Channel Status
                               00000080  00000001 5461+SCSWPCI  EQU   X'80'    Program-controlled interruption
                               00000040  00000001 5462+SCSWIL   EQU   X'40'    Incorrect length
                               00000020  00000001 5463+SCSWPRGM EQU   X'20'    Program check
                               00000010  00000001 5464+SCSWPROT EQU   X'10'    Protection Check
                               00000008  00000001 5465+SCSWCDAT EQU   X'08'    Channel-data check
                               00000004  00000001 5466+SCSWCCTL EQU   X'04'    Channel-control check
                               00000002  00000001 5467+SCSWICTL EQU   X'02'    Interface-control check
                               00000001  00000001 5468+SCSWCHNG EQU   X'01'    Chaining check

0000000A  0000                                    5470+SCSWCNT  DC    H'0'     Residual CCW count
                               0000000C  00000001 5471+SCSWL    EQU   *-SCSW
```

```
  LOC         OBJECT CODE        ADDR1     ADDR2     STMT
                                                      5474 ************************************************************************
                                                      5475 *        (other DSECTS needed by SATK)
                                                      5476 ************************************************************************

                                                      5478          DSECTS PRINT=OFF,NAME=(ASA,SCHIB,CCW0,CCW1,CSW)
```

```
                                                      5754          PRINT ON

                                                      5756 ************************************************************************
                                                      5757 *        Register equates
                                                      5758 ************************************************************************

                            00000000  00000001  5760 R0        EQU   0
                            00000001  00000001  5761 R1        EQU   1
                            00000002  00000001  5762 R2        EQU   2
                            00000003  00000001  5763 R3        EQU   3
                            00000004  00000001  5764 R4        EQU   4
                            00000005  00000001  5765 R5        EQU   5
                            00000006  00000001  5766 R6        EQU   6
                            00000007  00000001  5767 R7        EQU   7
                            00000008  00000001  5768 R8        EQU   8
                            00000009  00000001  5769 R9        EQU   9
                            0000000A  00000001  5770 R10       EQU   10
                            0000000B  00000001  5771 R11       EQU   11
                            0000000C  00000001  5772 R12       EQU   12
                            0000000D  00000001  5773 R13       EQU   13
                            0000000E  00000001  5774 R14       EQU   14
                            0000000F  00000001  5775 R15       EQU   15
```

```
                                                      5777          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
ASA	4	00000000	512	5482	3538
ASBEGIN	U	00000000	1	5483	5488 5530 5566 5575 5593 5600 5606 5610 5614 5620 5637
ASEND	U	00000200	1	5636	5637
ASLENGTH	U	00000200	1	5637	
BCEXTCOD	H	0000001A	2	5500	
BCIOCOD	H	0000003A	2	5508	
BCMCKCOD	H	00000032	2	5506	
BCPGMCOD	H	0000002A	2	5504	
BCSVCCOD	H	00000022	2	5502	
BEGCLOCK	D	00001578	8	5066	3888 3899 4034 4147 4372 4384 4509 4523 4843 4846 4853
BEGDATON	I	00001198	4	4691	4698
BEGIN	I	00000200	2	3544	3513 3539 3540 3804 3873
CALCDUR	I	0000132C	4	4840	3892 4141 4376 4513 4768
CALCRET	F	00001370	4	4862	4840 4859
CALCWORK	F	00001374	4	4863	4841 4858
CAW	F	00000048	4	5512	
CAWADDR	R	00000049	3	5515	
CAWKEY	X	00000048	1	5513	
CAWSUSP	U	00000008	1	5514	
CCW0	4	00000000	8	5641	5647
CCW0ADDR	R	00000001	3	5643	
CCW0CNT	H	00000006	2	5646	
CCW0CODE	X	00000000	1	5642	
CCW0FLGS	X	00000004	1	5644	
CCW0L	U	00000008	1	5647	
CCW1	4	00000000	8	5659	5664
CCW1ADDR	A	00000004	4	5663	
CCW1CNT	H	00000002	2	5662	
CCW1CODE	X	00000000	1	5660	
CCW1FLGS	X	00000001	1	5661	
CCW1L	U	00000008	1	5664	
CCWCC	U	00000040	1	5651	
CCWCD	U	00000080	1	5650	
CCWIDA	U	00000004	1	5655	
CCWPCI	U	00000008	1	5654	
CCWSKIP	U	00000010	1	5653	
CCWSLI	U	00000020	1	5652	
CCWSUSP	U	00000002	1	5656	
CHANID	F	000000A8	4	5567	
CLC1	A	00001608	4	5083	3589
CLC2	A	00001610	4	5084	3596
CLC256	A	00001638	4	5090	3579 3618
CLC4	A	00001628	4	5088	3577 3603
CLC8	A	00001630	4	5089	3583 3610
CLCBOTH	A	00001618	4	5085	3625
CLCL1	A	0000200C	4	5244	3671
CLCL1K	A	0000203C	4	5250	3710
CLCL2	A	0000201C	4	5246	3680
CLCL256	A	0000202C	4	5248	3898 4036 4037 4038 4041 4042 4043 4044 4045 4046 4047 4048 4049 4050 4051 4052 4053 4054 4055 4056 4057 4058 4059 4060 4061 4062 4063 4064 4065 4066 4067 4068 4069 4070 4071 4072 4073 4074 4075 4076 4077 4078 4079 4080 4081 4082 4083 4084 4085 4086 4087 4088

```
     SYMBOL         TYPE    VALUE      LENGTH    DEFN  REFERENCES

                                                      4089  4090  4091  4092  4093  4094  4095  4096  4097  4098  4099  4100  4101
                                                      4102  4103  4104  4105  4106  4107  4108  4109  4110  4111  4112  4113  4114
                                                      4115  4116  4117  4118  4119  4120  4121  4122  4123  4124  4125  4126  4127
                                                      4128  4129  4130  4131  4132  4133  4134  4135  4137  4138  4149  4151  4153
                                                      4157  4159  4161  4163  4165  4167  4169  4171  4173  4175  4177  4179  4181
                                                      4183  4185  4187  4189  4191  4193  4195  4197  4199  4201  4203  4205  4207
                                                      4209  4211  4213  4215  4217  4219  4221  4223  4225  4227  4229  4231  4233
                                                      4235  4237  4239  4241  4243  4245  4247  4249  4251  4253  4255  4257  4259
                                                      4261  4263  4265  4267  4269  4271  4273  4275  4277  4279  4281  4283  4285
                                                      4287  4289  4291  4293  4295  4297  4299  4301  4303  4305  4307  4309  4311
                                                      4313  4315  4317  4319  4321  4323  4325  4327  4329  4331  4333  4335  4337
                                                      4339  4341  4343  4345  4348  4350
CLCL4                A     0000206C           4  5256  3653  3690
CLCL8                A     0000207C           4  5258  3663  3701
CLCLBOTH             A     0000204C           4  5252  3719
CLCLEND              F     0000214C           4  5288  4903  4904
CLCLETAL             J     00000000       12289  3495  3498  3505  3512  3514  5296  5300  5305
CLCLOP1              A     0000208C           4  5260  3658  3729
CLCLOP2              A     0000205C           4  5254  3738
CLCLPF               A     0000209C           4  5262  4665  4734  4736  4742  4744
CLCOP1               A     00001640           4  5091  3581  3632
CLCOP2               A     00001620           4  5086  3639
CODE                 2     00000000       12289  3495
CONPGM               W     000015B0           8  5075  5025
CPUID                U     0000031B           1  5639
CRLREG0              A     00001568           4  5061  4688
CSW                  F     00000040           8  5511
CSWATTN              U     00000080           1  5681
CSWBUSY              U     00000010           1  5684
CSWCCTL              U     00000004           1  5696
CSWCCW               R     00000001           3  5678
CSWCDAT              U     00000008           1  5695
CSWCE                U     00000008           1  5685  4827
CSWCHNG              U     00000001           1  5698
CSWCNT               H     00000006           2  5700
CSWCS                X     00000005           1  5690
CSWCUE               U     00000020           1  5683
CSWDCC0              U     00000000           1  5674
CSWDCC1              U     00000001           1  5675
CSWDCC3              U     00000003           1  5676
CSWDCCM              U     00000003           1  5673
CSWDE                U     00000004           1  5686  4827
CSWFLAG              X     00000000           1  5668
CSWFMT               4     00000000           8  5667  5701
CSWFMTL              U     00000008           1  5701
CSWICTL              U     00000002           1  5697
CSWIL                U     00000040           1  5692
CSWKEYM              U     000000F0           1  5669
CSWLOG               U     00000004           1  5672
CSWPCI               U     00000080           1  5691
CSWPRGM              U     00000020           1  5693
CSWPROT              U     00000010           1  5694
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
CSWSM	U	00000040	1	5682	
CSWSUSP	U	00000008	1	5671	
CSWUC	U	00000002	1	5687	
CSWUS	X	00000004	1	5680	
CSWUX	U	00000001	1	5688	
CTLREG1	A	0000156C	4	5062	4689
DATONPSW	X	000011B8	4	4698	4690
DATTABS	X	00003000	1	5307	
DURATION	D	00001588	8	5068	3893 4142 4377 4514 4771 4772 4775 4855
DWAT0010	3	00001410	8	4933	4932
DWAT0011	3	00001420	8	4938	4937
DWAT0012	3	00001430	8	4943	4942
DWAT0013	3	00001440	8	4948	4947
ECLCL1	A	000020AC	4	5268	3674
ECLCL1K	A	000020DC	4	5274	3713
ECLCL2	A	000020BC	4	5270	3683
ECLCL256	A	000020CC	4	5272	
ECLCL4	A	0000210C	4	5280	3693
ECLCL8	A	0000211C	4	5282	3704
ECLCLBTH	A	000020EC	4	5276	3722
ECLCLOP1	A	0000212C	4	5284	3732
ECLCLOP2	A	000020FC	4	5278	3741
ECLCLPF	A	0000213C	4	5286	4748
EDIT	X	000015FC	12	5077	4785 4786
ENADEV	I	00001456	4	4967	4895
ENAOKAY	I	000014A4	2	4992	4981
ENDCLCL	I	000013CA	4	4903	3675 3684 3694 3705 3714 3723 3733 3742
ENDCLOCK	D	00001580	8	5067	3891 4015 4140 4353 4375 4490 4512 4629 4848 4851 4854
ENDREGS	A	00000020	4	5163	3842
EOJ	H	00001408	2	4931	3567
EXLEN	F	00000018	4	5160	3832
EXTCPUAD	H	00000084	2	5532	
EXTICODE	H	00000086	2	5533	
EXTIPARM	F	00000080	4	5531	
EXTNPSW	F	00000058	8	5521	
EXTOPSW	F	00000018	8	5493	5499
FAILDEV	H	00001418	2	4936	4972 4982 4987
FAILIO	H	00001428	2	4941	4795 4818 4828
FAILMASK	A	0000001C	4	5161	3833
FAILTEST	H	00001438	2	4946	3591 3598 3605 3612 3620 3627 3634 3641 3673 3682 3692 3703 3712 3721 3731 3740 3857 4709 4715 4728 4735 4737 4741 4743 4745 4749 4753 4759 4905 4918
FIND0015	A	0000149C	4	4989	4967
FINL0015	H	0000145E	2	4970	4986
FINM0015	A	000014A0	4	4990	4985
FINN0015	H	0000148C	2	4983	4974 4976
IIRB0016	F	000014D8	4	5017	5013 5015
IMAGE	1	00000000	12289	0	
INIT	H	000013B8	2	4889	3551
INV1	A	00001648	4	5097	3754
INV2	A	00001658	4	5098	3759
INV256	A	00001688	4	5101	3774 4381

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
INV4	A	00001668	4	5099	3764
INV8	A	00001678	4	5100	3769
INVBOTH	A	00001698	4	5103	3779
INVOP1	A	000016A8	4	5104	3784
INVOP2	A	000016B8	4	5105	3789
IOCB	4	00000000	48	5315	5339 3541
IOCBCAW	A	00000018	4	5335	
IOCBCM	X	00000009	1	5323	
IOCBCS	X	0000000B	1	5326	
IOCBCT	X	0000000D	1	5328	
IOCBDEV	H	00000004	2	5320	4975
IOCBDID	F	00000000	4	5317	4791 4978
IOCBDV	H	00000002	2	5319	
IOCBIRB	A	00000020	8	5337	4796
IOCBL	U	00000030	1	5339	
IOCBORB	A	00000018	8	5336	4793 4892
IOCBRCNT	H	00000016	2	5334	4825
IOCBSC	X	0000000E	1	5329	4789 4820 4822
IOCBSCCW	A	00000010	4	5331	4824
IOCBSCNT	F	00000014	4	5332	
IOCBSIB	A	00000028	8	5338	4968
IOCBST	H	0000000A	2	5324	4790 4821
IOCBUM	X	00000008	1	5322	
IOCBUS	X	0000000A	1	5325	4827
IOCBUT	X	0000000C	1	5327	
IOCBWAIT	X	0000000F	1	5330	
IOCBZERO	H	00000006	2	5321	4790
IOCB_009	A	000014A8	4	5000	4891
IOELADDR	F	000000AC	4	5568	
IOICODE	H	000000BA	2	5573	
IOIID	F	000000C0	4	5578	
IOINIT	I	00001448	4	4955	4894
IOIPARM	F	000000BC	4	5577	
IOMK0014	F	00001450	4	4957	4955 4956
ION0008	3	000012D0	8	4806	4803
IONPSW	F	00000078	8	5525	
IOOPSW	F	00000038	8	5497	5507
IORB0016	X	00001518	12	5019	5011
IOS0008	X	000012D8	8	4807	4802 4810
IOSSID	F	000000B8	4	5576	4813
IOWT0007	H	000012B6	2	4800	4814 4817 4823
IPLCCW1	F	00000008	8	5485	
IPLCCW2	F	00000010	8	5486	
IPLPSW	F	00000000	8	5484	
IRB	4	00000000	96	5394	5398 5400 4797
IRBECW	X	00000020	32	5397	
IRBEMW	X	00000040	32	5399	
IRBESW	X	0000000C	20	5396	
IRBL	U	00000040	1	5398	
IRBSCSW	X	00000000	12	5395	4820 4821 4824 4825
IRBXL	U	00000060	1	5400	
IRST0008	H	000012E0	2	4809	4806

```
     SYMBOL         TYPE    VALUE      LENGTH    DEFN  REFERENCES

K                    U     00000400          1  5048  5049  5050  5051  5250  5274
K64                  U     00010000          1  5050  5057  4518  4520  5083  5084  5085  5086  5088  5089  5090  5091  5097  5098
                                                     5099  5100  5101  5103  5104  5105  5178  5179  5183  5184  5188  5189  5193
                                                     5194  5198  5199  5203  5204  5206  5208  5209  5211  5213  5214  5216  5244
                                                     5246  5248  5250  5252  5254  5256  5258  5260  5262  5268  5270  5272  5274
                                                     5276  5278  5280  5282  5284  5286
LCHANLOG             F     000000B0          4  5569
LOGICERR             D     000011A8          8  4696
MAINSIZE             U     00200000          1  5056  5057
MB                   U     00100000          1  5051  5056  4520  5083  5084  5085  5086  5088  5089  5090  5091  5097  5098  5099
                                                     5100  5101  5103  5104  5105  5179  5184  5189  5194  5199  5204  5209  5214
                                                     5244  5246  5248  5250  5252  5254  5256  5258  5260  5262  5268  5270  5272
                                                     5274  5276  5278  5280  5282  5284  5286
MCKLOG               F     00000100          4  5601
MCKNPSW              F     00000070          8  5524
MCKOPSW              F     00000030          8  5496  5505
MEASUREB             X     000000B9          1  5572
MKARCHMD             X     000000A3          1  5560
MKARS                F     00000120          4  5599
MKCLKCMP             F     000000E0          8  5585
MKCPUTIM             F     000000D8          8  5584
MKCRS                F     000001C0          4  5604
MKDMGCOD             F     000000F4          4  5588
MKFAILA              F     000000F8          4  5590
MKFPRS               D     00000160          8  5602
MKICODE              F     000000E8          4  5586
MKLOGOUT             F     00000100          4  5592
MKMODEL              F     000000FC          4  5591
MKXSAA               F     000000D4          4  5583
MONCLS               H     00000094          2  5548
MONCODE              F     0000009C          4  5555
MONNUMBR             X     00000095          1  5550
MPGACCID             X     000000A2          1  5558
MVCINCLC             I     00001402          6  4923  4917
MVCININ              X     000016C8        256  5107  4382  4913
MVCINMVC             I     000013FC          6  4922  4916
MVCINOUT             X     000017C8        256  5126  4923
MVCINSRC             I     000013F6          6  4921  4915
MVCINTST             I     000013DA          4  4912  3755  3760  3765  3770  3775  3780  3785  3790
MYPGMNEW             I     000011C0          6  4703  4680
NKGRS                F     00000180          4  5603
NUMLOOPS             F     00001570          4  5064  3887  3897  4033  4146  4371  4383  4508  4522
NUMPGTBS             U     00000020          1  5057  5058  5060  4645
NUMSEGTB             U     00000002          1  5058  5062
OP1DATA              A     00000000          4  5152  3816
OP1LEN               F     00000004          4  5153  3817
OP1WHERE             A     00000008          4  5154  3813
OP2DATA              A     0000000C          4  5156  3820
OP2LEN               F     00000010          4  5157  3821
OP2WHERE             A     00000014          4  5158  3814
ORB                  4     00000000         32  5347  5377  5385  3542
ORB1_0               X     00000004          1  5350
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
ORB1_8	X	00000005	1	5357	
ORBA	U	00000010	1	5361	
ORBB	U	00000004	1	5363	
ORBC	U	00000004	1	5353	
ORBCCW	A	00000008	4	5375	
ORBCSS	X	0000000C	1	5379	
ORBCU	X	0000000E	1	5382	
ORBD	U	00000040	1	5370	
ORBF	U	00000080	1	5358	
ORBH	U	00000002	1	5364	
ORBI	U	00000020	1	5360	
ORBKEYM	U	000000F0	1	5351	
ORBL	U	00000080	1	5368	
ORBLEN	U	0000000C	1	5377	
ORBLPM	X	00000006	1	5366	
ORBM	U	00000002	1	5354	
ORBP	U	00000040	1	5359	
ORBPARM	F	00000000	4	5348	
ORBPGM	X	0000000E	1	5381	
ORBRSV25	U	0000007E	1	5372	
ORBRSV26	U	0000003E	1	5371	
ORBRSV3	U	0000007F	1	5369	
ORBRSV4	U	00000080	1	5376	
ORBRSV5	X	0000000D	1	5380	
ORBRSV6	X	0000000F	1	5383	
ORBRSV7	X	00000010	16	5384	
ORBS	U	00000008	1	5352	
ORBT	U	00000001	1	5365	
ORBU	U	00000008	1	5362	
ORBX	U	00000001	1	5373	
ORBXLEN	U	00000020	1	5385	
ORBY	U	00000001	1	5355	
ORRB1_24	X	00000007	1	5367	
OVERHEAD	D	00001590	8	5069	3893 4142 4377 4514 4770
PAGE	U	00001000	1	5049	5053 5059 5290 4649 5254 5260 5278 5284
PAGELOOP	I	00001142	4	4656	4659
PAGETABS	U	00003080	1	5060	4646
PCFETO	A	000000C4	4	5579	
PERACCID	X	000000A1	1	5557	
PERADDR	F	00000098	4	5554	
PERCODE	X	00000096	1	5551	
PERCODMK	U	000000F0	1	5552	
PFINSADR	I	000011A4	2	4694	4708
PFPAGE	U	00000005	1	5289	5290
PFPGBYTS	U	00005000	1	5290	4667
PGMACCID	X	000000A0	1	5556	
PGMDXC	F	00000090	4	5546	
PGMICODE	H	0000008E	2	5545	4714
PGMIID	F	0000008C	4	5541	
PGMIILC	X	0000008D	1	5543	
PGMIILCM	U	0000000C	1	5544	
PGMNPSW	F	00000068	8	5523	4679 4681 4682 4703

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
PGMOPSW	F	00000028	8	5495	5503 4708
PGMTRX	F	00000090	4	5547	4720
PMCW1_0	X	00000004	1	5708	
PMCW1_8	X	00000005	1	5711	4973 4979
PMCWB	U	00000004	1	5743	
PMCWCHP0	X	00000010	1	5732	
PMCWCHP1	X	00000011	1	5733	
PMCWCHP2	X	00000012	1	5734	
PMCWCHP3	X	00000013	1	5735	
PMCWCHP4	X	00000014	1	5736	
PMCWCHP5	X	00000015	1	5737	
PMCWCHP6	X	00000016	1	5738	
PMCWCHP7	X	00000017	1	5739	
PMCWDNUM	H	00000006	2	5723	4975
PMCWE	U	00000080	1	5712	4979
PMCWEXC	X	0000001B	1	5742	
PMCWIP	F	00000000	4	5707	
PMCWISCM	U	00000038	1	5709	
PMCWLM	U	00000060	1	5713	
PMCWLMG	U	00000020	1	5714	
PMCWLML	U	00000040	1	5715	
PMCWLPM	X	00000008	1	5725	
PMCWLPUM	X	0000000A	1	5727	
PMCWM	U	00000004	1	5719	
PMCWMBI	H	0000000C	2	5729	
PMCWMM	U	00000018	1	5716	
PMCWMMC	U	00000008	1	5718	
PMCWMME	U	00000010	1	5717	
PMCWPAM	X	0000000F	1	5731	
PMCWPIM	X	0000000B	1	5728	
PMCWPNOM	X	00000009	1	5726	
PMCWPOM	X	0000000E	1	5730	
PMCWRES1	X	00000018	4	5740	
PMCWRES2	X	00000018	3	5741	
PMCWS	U	00000001	1	5745	
PMCWT	U	00000002	1	5720	
PMCWV	U	00000001	1	5721	4973
PMCWX	U	00000002	1	5744	
PRTLINE	C	000015B8	68	5076	4017 4355 4492 4631 4785 4786 5075
R0	U	00000000	1	5760	3538 4647 4656 4657 4680 4681 4688 4720 4721 4722 4727
R1	U	00000001	1	5761	3800 3827 3837 3845 3858 4689
R10	U	0000000A	1	5770	3671 3672 3680 3681 3690 3691 3701 3702 3710 3711 3719 3720 3729
					3730 3738 3739 3813 3862 3865 3898 3901 3902 3905 3906 3907 3908
					3909 3910 3911 3912 3913 3914 3915 3916 3917 3918 3919 3920 3921
					3922 3923 3924 3925 3926 3927 3928 3929 3930 3931 3932 3933 3934
					3935 3936 3937 3938 3939 3940 3941 3942 3943 3944 3945 3946 3947
					3948 3949 3950 3951 3952 3953 3954 3955 3956 3957 3958 3959 3960
					3961 3962 3963 3964 3965 3966 3967 3968 3969 3970 3971 3972 3973
					3974 3975 3976 3977 3978 3979 3980 3981 3982 3983 3984 3985 3986
					3987 3988 3989 3990 3991 3992 3993 3994 3995 3996 3997 3998 3999
					4000 4001 4002 4003 4004 4005 4006 4007 4008 4009 4011 4012 4013
					4036 4037 4038 4041 4042 4043 4044 4045 4046 4047 4048 4049 4050

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					4051 4052 4053 4054 4055 4056 4057 4058 4059 4060 4061 4062 4063
					4064 4065 4066 4067 4068 4069 4070 4071 4072 4073 4074 4075 4076
					4077 4078 4079 4080 4081 4082 4083 4084 4085 4086 4087 4088 4089
					4090 4091 4092 4093 4094 4095 4096 4097 4098 4099 4100 4101 4102
					4103 4104 4105 4106 4107 4108 4109 4110 4111 4112 4113 4114 4115
					4116 4117 4118 4119 4120 4121 4122 4123 4124 4125 4126 4127 4128
					4129 4130 4131 4132 4133 4134 4135 4137 4138 4149 4150 4151 4152
					4153 4154 4157 4158 4159 4160 4161 4162 4163 4164 4165 4166 4167
					4168 4169 4170 4171 4172 4173 4174 4175 4176 4177 4178 4179 4180
					4181 4182 4183 4184 4185 4186 4187 4188 4189 4190 4191 4192 4193
					4194 4195 4196 4197 4198 4199 4200 4201 4202 4203 4204 4205 4206
					4207 4208 4209 4210 4211 4212 4213 4214 4215 4216 4217 4218 4219
					4220 4221 4222 4223 4224 4225 4226 4227 4228 4229 4230 4231 4232
					4233 4234 4235 4236 4237 4238 4239 4240 4241 4242 4243 4244 4245
					4246 4247 4248 4249 4250 4251 4252 4253 4254 4255 4256 4257 4258
					4259 4260 4261 4262 4263 4264 4265 4266 4267 4268 4269 4270 4271
					4272 4273 4274 4275 4276 4277 4278 4279 4280 4281 4282 4283 4284
					4285 4286 4287 4288 4289 4290 4291 4292 4293 4294 4295 4296 4297
					4298 4299 4300 4301 4302 4303 4304 4305 4306 4307 4308 4309 4310
					4311 4312 4313 4314 4315 4316 4317 4318 4319 4320 4321 4322 4323
					4324 4325 4326 4327 4328 4329 4330 4331 4332 4333 4334 4335 4336
					4337 4338 4339 4340 4341 4342 4343 4344 4345 4346 4348 4349 4350
					4351 4381 4386 4387 4388 4391 4392 4393 4394 4395 4396 4397 4398
					4399 4400 4401 4402 4403 4404 4405 4406 4407 4408 4409 4410 4411
					4412 4413 4414 4415 4416 4417 4418 4419 4420 4421 4422 4423 4424
					4425 4426 4427 4428 4429 4430 4431 4432 4433 4434 4435 4436 4437
					4438 4439 4440 4441 4442 4443 4444 4445 4446 4447 4448 4449 4450
					4451 4452 4453 4454 4455 4456 4457 4458 4459 4460 4461 4462 4463
					4464 4465 4466 4467 4468 4469 4470 4471 4472 4473 4474 4475 4476
					4477 4478 4479 4480 4481 4482 4483 4484 4486 4487 4488 4518 4519
					4525 4526 4527 4530 4531 4532 4533 4534 4535 4536 4537 4538 4539
					4540 4541 4542 4543 4544 4545 4546 4547 4548 4549 4550 4551 4552
					4553 4554 4555 4556 4557 4558 4559 4560 4561 4562 4563 4564 4565
					4566 4567 4568 4569 4570 4571 4572 4573 4574 4575 4576 4577 4578
					4579 4580 4581 4582 4583 4584 4585 4586 4587 4588 4589 4590 4591
					4592 4593 4594 4595 4596 4597 4598 4599 4600 4601 4602 4603 4604
					4605 4606 4607 4608 4609 4610 4611 4612 4613 4614 4615 4616 4617
					4618 4619 4620 4621 4622 4623 4625 4626 4627 4644 4651 4652 4653
					4665 4666 4694 4734 4748 4752 4756 4870 4872 4877 4880 4903 4912
					4922 4923
R11	U	0000000B	1	5771	3833 3838 4386 4387 4388 4391 4392 4393 4394 4395 4396 4397 4398
					4399 4400 4401 4402 4403 4404 4405 4406 4407 4408 4409 4410 4411
					4412 4413 4414 4415 4416 4417 4418 4419 4420 4421 4422 4423 4424
					4425 4426 4427 4428 4429 4430 4431 4432 4433 4434 4435 4436 4437
					4438 4439 4440 4441 4442 4443 4444 4445 4446 4447 4448 4449 4450
					4451 4452 4453 4454 4455 4456 4457 4458 4459 4460 4461 4462 4463
					4464 4465 4466 4467 4468 4469 4470 4471 4472 4473 4474 4475 4476
					4477 4478 4479 4480 4481 4482 4483 4484 4486 4487 4488 4645 4661
					4740 4742 4757 4872 4874 4922
R12	U	0000000C	1	5772	3672 3681 3691 3702 3711 3720 3730 3739 3814 3863 3865 3901 3902
					3905 3906 3907 3908 3909 3910 3911 3912 3913 3914 3915 3916 3917
					3918 3919 3920 3921 3922 3923 3924 3925 3926 3927 3928 3929 3930

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					3931 3932 3933 3934 3935 3936 3937 3938 3939 3940 3941 3942 3943
					3944 3945 3946 3947 3948 3949 3950 3951 3952 3953 3954 3955 3956
					3957 3958 3959 3960 3961 3962 3963 3964 3965 3966 3967 3968 3969
					3970 3971 3972 3973 3974 3975 3976 3977 3978 3979 3980 3981 3982
					3983 3984 3985 3986 3987 3988 3989 3990 3991 3992 3993 3994 3995
					3996 3997 3998 3999 4000 4001 4002 4003 4004 4005 4006 4007 4008
					4009 4011 4012 4013 4150 4152 4154 4158 4160 4162 4164 4166 4168
					4170 4172 4174 4176 4178 4180 4182 4184 4186 4188 4190 4192 4194
					4196 4198 4200 4202 4204 4206 4208 4210 4212 4214 4216 4218 4220
					4222 4224 4226 4228 4230 4232 4234 4236 4238 4240 4242 4244 4246
					4248 4250 4252 4254 4256 4258 4260 4262 4264 4266 4268 4270 4272
					4274 4276 4278 4280 4282 4284 4286 4288 4290 4292 4294 4296 4298
					4300 4302 4304 4306 4308 4310 4312 4314 4316 4318 4320 4322 4324
					4326 4328 4330 4332 4334 4336 4338 4340 4342 4344 4346 4349 4351
					4520 4521 4525 4526 4527 4530 4531 4532 4533 4534 4535 4536 4537
					4538 4539 4540 4541 4542 4543 4544 4545 4546 4547 4548 4549 4550
					4551 4552 4553 4554 4555 4556 4557 4558 4559 4560 4561 4562 4563
					4564 4565 4566 4567 4568 4569 4570 4571 4572 4573 4574 4575 4576
					4577 4578 4579 4580 4581 4582 4583 4584 4585 4586 4587 4588 4589
					4590 4591 4592 4593 4594 4595 4596 4597 4598 4599 4600 4601 4602
					4603 4604 4605 4606 4607 4608 4609 4610 4611 4612 4613 4614 4615
					4616 4617 4618 4619 4620 4621 4622 4623 4625 4626 4627 4646 4651
					4656 4658 4694 4736 4775 4776 4778 4873 4876 4877 4878 4914 4915
					4916 4917
R13	U	0000000D	1	5773	3671 3680 3690 3701 3710 3719 3729 3738 3898 4036 4037 4038 4041
					4042 4043 4044 4045 4046 4047 4048 4049 4050 4051 4052 4053 4054
					4055 4056 4057 4058 4059 4060 4061 4062 4063 4064 4065 4066 4067
					4068 4069 4070 4071 4072 4073 4074 4075 4076 4077 4078 4079 4080
					4081 4082 4083 4084 4085 4086 4087 4088 4089 4090 4091 4092 4093
					4094 4095 4096 4097 4098 4099 4100 4101 4102 4103 4104 4105 4106
					4107 4108 4109 4110 4111 4112 4113 4114 4115 4116 4117 4118 4119
					4120 4121 4122 4123 4124 4125 4126 4127 4128 4129 4130 4131 4132
					4133 4134 4135 4137 4138 4149 4151 4153 4157 4159 4161 4163 4165
					4167 4169 4171 4173 4175 4177 4179 4181 4183 4185 4187 4189 4191
					4193 4195 4197 4199 4201 4203 4205 4207 4209 4211 4213 4215 4217
					4219 4221 4223 4225 4227 4229 4231 4233 4235 4237 4239 4241 4243
					4245 4247 4249 4251 4253 4255 4257 4259 4261 4263 4265 4267 4269
					4271 4273 4275 4277 4279 4281 4283 4285 4287 4289 4291 4293 4295
					4297 4299 4301 4303 4305 4307 4309 4311 4313 4315 4317 4319 4321
					4323 4325 4327 4329 4331 4333 4335 4337 4339 4341 4343 4345 4348
					4350 4381 4382 4655 4659 4665 4740 4744 4775 4779 4870 4873 4874
					4878 4880 4903 4912 4921
R14	U	0000000E	1	5774	3551 3555 3556 3557 3558 3560 3561 3562 3563 3565 3643 3744 3792
					3857 3860 3880 4019 4026 4357 4364 4494 4501 4633 4761 4896
R15	U	0000000F	1	5775	3675 3684 3694 3705 3714 3723 3733 3742 3755 3760 3765 3770 3775
					3780 3785 3790 3801 3804 3859 3872 3892 4018 4141 4356 4376 4493
					4513 4632 4767 4768 4773 4831 4832 4840 4856 4859 4860 4881 4894
					4895 4906 4919 4960 4992
R2	U	00000002	1	5762	3539 3544 3545 3546 3548 3801 3803 3828 3837 3849 3859 3873
R3	U	00000003	1	5763	3541 4891
R4	U	00000004	1	5764	
R5	U	00000005	1	5765	3577 3578 3579 3580 3581 3582 3589 3590 3596 3597 3603 3604 3610

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					3611 3618 3619 3625 3626 3632 3633 3639 3640 3653 3654 3655 3656
					3658 3659 3660 3661 3663 3664 3665 3666 3674 3683 3693 3704 3713
					3722 3732 3741 3754 3759 3764 3769 3774 3779 3784 3789 3806 3807
					3852 3853 3871 3887 3890 3897 4014 4033 4139 4146 4352 4371 4374
					4383 4489 4508 4511 4522 4628 4666 4667 4668 4669 4670 4673 4674
					4770 4841 4853 4858 4872 4904 4912
R6	U	00000006	1	5766	3583 3584 3589 3590 3596 3597 3603 3604 3610 3611 3618 3619 3625
					3626 3632 3633 3639 3640 3653 3654 3658 3659 3663 3664 3816 3820
					3842 3845 3862 3863 3889 3890 3900 4014 4035 4139 4148 4352 4373
					4374 4385 4489 4510 4511 4524 4628 4648 4653 4658 4668 4724 4725
					4727 4752 4758 4771 4843 4844 4845 4846 4848 4849 4850 4851 4854
					4873 4913 4914 4921
R7	U	00000007	1	5767	3817 3818 3821 3822 3832 3836 3842 3849 4649 4657 4756 4757 4758
					4772 4841 4843 4846 4848 4851 4855 4858 4878
R8	U	00000008	1	5768	3542 4892
R9	U	00000009	1	5769	3540 3548 3549
REG2LOW	U	000000DD	1	5168	5206 5211 5216
REG2PATT	U	AABBCCDD	1	5167	3828 5181 5186 5191 5196 5201 5206 5211 5216
RPTSAVE	F	00001328	4	4834	4767 4831
RPTSPEED	I	00001252	4	4767	4018 4356 4493 4632
RSTNPSW	F	00000000	8	5489	
RSTOPSW	F	00000008	8	5490	
SAVER1	F	000004A8	4	3868	3800 3858
SAVETRT	D	000004B0	8	3869	3837
SCANOUT	X	00000080	1	5527	5528
SCANOUTL	U	00000000	1	5528	
SCHIB	4	00000000	52	5704	5751 4969
SCHIBL	U	00000034	1	5751	
SCHMBA	A	00000028	8	5749	
SCHMDA1	X	00000030	4	5750	
SCHMDA3	X	00000028	12	5748	
SCHPMCW	X	00000000	28	5706	
SCHSCSW	X	0000001C	12	5747	
SCSW	4	00000000	12	5409	5471
SCSW0CC	U	00000004	1	5425	
SCSW1	X	00000002	1	5429	
SCSW2	X	00000003	1	5438	4820
SCSWACP	U	00000001	1	5437	
SCSWADA	U	00000040	1	5440	
SCSWAHP	U	00000002	1	5436	
SCSWALKC	U	00000010	1	5423	
SCSWARP	U	00000008	1	5434	
SCSWASA	U	00000080	1	5439	
SCSWASP	U	00000004	1	5435	
SCSWASUS	U	00000020	1	5441	
SCSWATTN	U	00000080	1	5451	
SCSWBUSY	U	00000010	1	5454	
SCSWCCTL	U	00000004	1	5466	
SCSWCCW	A	00000004	4	5448	4824
SCSWCCWF	U	00000080	1	5420	
SCSWCCWP	U	00000040	1	5421	
SCSWCDAT	U	00000008	1	5465	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
SCSWCE	U	00000008	1	5455	
SCSWCHNG	U	00000001	1	5468	
SCSWCNT	H	0000000A	2	5470	4825
SCSWCS	X	00000009	1	5460	
SCSWCTLS	X	00000001	1	5419	
SCSWCUE	U	00000020	1	5453	
SCSWDCC0	U	00000000	1	5415	
SCSWDCC1	U	00000001	1	5416	
SCSWDCC3	U	00000003	1	5417	
SCSWDCCM	U	00000003	1	5414	
SCSWDE	U	00000004	1	5456	
SCSWECWC	U	00000002	1	5426	
SCSWESWF	U	00000004	1	5413	
SCSWFC	U	00000010	1	5433	
SCSWFH	U	00000020	1	5432	
SCSWFLAG	X	00000000	1	5410	
SCSWFM	U	00000070	1	5430	
SCSWFS	U	00000040	1	5431	
SCSWICTL	U	00000002	1	5467	
SCSWIL	U	00000040	1	5462	
SCSWISIC	U	00000020	1	5422	
SCSWKEYM	U	000000F0	1	5411	
SCSWL	U	0000000C	1	5471	
SCSWPCI	U	00000080	1	5461	
SCSWPNOP	U	00000001	1	5427	
SCSWPRGM	U	00000020	1	5463	
SCSWPROT	U	00000010	1	5464	
SCSWSAS	U	00000010	1	5442	
SCSWSINT	U	00000008	1	5443	
SCSWSM	U	00000040	1	5452	
SCSWSPEN	U	00000001	1	5446	
SCSWSPRI	U	00000004	1	5444	4822
SCSWSSEC	U	00000002	1	5445	
SCSWSSIC	U	00000008	1	5424	
SCSWSUSC	U	00000008	1	5412	
SCSWUC	U	00000002	1	5457	
SCSWUS	X	00000008	1	5450	4821
SCSWUX	U	00000001	1	5458	
SEGLOOP	I	00001134	4	4651	4661
SEGTABLS	U	00003000	1	5059	5060 5305 4644 5062
SSARCHMD	X	000000A3	1	5559	
SSARS	F	00000120	4	5615	
SSCLKCMP	F	000000E0	8	5609	
SSCPUTIM	F	000000D8	8	5608	
SSCRS	F	000001C0	4	5618	
SSFPRS	D	00000160	8	5616	
SSGRS	F	00000180	4	5617	
SSMODEL	F	0000010C	4	5613	
SSPREFIX	F	00000108	4	5612	
SSPSW	F	00000100	8	5611	
SSXSAA	A	000000D4	4	5607	
STFLDATA	F	000000C8	4	5580	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
SUBDWORD	I	00001380	4	4870	4773 4856
SUBDWSAV	D	000013A8	8	4883	4870 4880
SUBTEST	X	000021FF	1	5303	3588 3595 3602 3609 3617 3624 3631 3638 3670 3679 3689 3700 3709 3718 3728 3737 3835 3844 3848 3883 4029 4367 4504 4640 4672 4678 4687 4707 4713 4719 4733 4739 4747 4751 4755
SVCICODE	H	0000008A	2	5539	
SVCIID	F	00000088	4	5535	
SVCIILC	X	00000089	1	5537	
SVCIILCM	U	0000000C	1	5538	
SVCNPSW	F	00000060	8	5522	
SVCOPSW	F	00000020	8	5494	5501
SVPGMNEW	D	000011B0	8	4697	4679 4703
TEST01	I	0000023A	4	3573	3555
TEST02	I	000002F0	4	3649	3556
TEST03	I	000003CA	4	3750	3557
TEST04	I	00000410	4	3798	3558
TEST91	I	000004B8	4	3879	3560
TEST92	I	00000794	4	4025	3561
TEST93	I	00000BC0	4	4363	3562
TEST94	I	00000E66	4	4500	3563
TEST95	I	00001116	4	4639	3565
TESTADDR	U	000021FE	1	5053	5054 5300
TESTNUM	X	000021FE	1	5302	3573 3649 3750 3798 3882 4028 4366 4503 4639
TICKSAAA	P	00001598	8	5071	4778 4781
TICKSBBB	P	000015A0	8	5072	4779 4783
TICKSTOT	P	000015A8	8	5073	4781 4782 4783 4786
TIMEADDR	U	000021FD	1	5054	5296
TIMEOPT	X	000021FD	1	5298	3879 4025 4363 4500
TIMER	F	00000050	4	5518	
TRT	I	0000049E	6	3865	3836
TRT1	A	000018C8	4	5178	
TRT2	A	000018F0	4	5183	
TRT256	A	00001968	4	5198	
TRT4	A	00001918	4	5188	
TRT8	A	00001940	4	5193	
TRTBC	I	000004A4	4	3866	3838
TRTBTH	A	00001990	4	5203	
TRTCTL	A	000018C8	4	5176	3806
TRTDONE	I	0000048A	4	3858	3855
TRTFAIL	I	00000486	4	3857	3846 3850 3866
TRTMVC1	I	00000492	6	3862	3818
TRTMVC2	I	00000498	6	3863	3822
TRTNEXT	U	00000028	1	5165	3852
TRTOP1	A	000019B8	4	5208	
TRTOP10	X	00001A0C	4	5224	4519 5178 5183 5188 5193 5198
TRTOP111	X	00001B0C	4	5226	5203 5213
TRTOP1F0	X	00001C0C	4	5228	5208
TRTOP2	A	000019E0	4	5213	
TRTOP20	X	00001D0C	1	5234	4521 5179 5184 5189 5194 5199
TRTOP211	X	00001E0C	1	5236	5204 5214
TRTOP2F0	X	00001F0C	1	5238	5209
TRTTEST	4	00000000	40	5150	3807

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
TST4LOOP	U	0000041E	1	3809	3854
TTDES	F	00000054	4	5519	
UA0	F	00000010	8	5491	
UA1	F	0000004C	4	5516	
UA2	F	000000A4	4	5561	
UA3	F	000000B4	4	5570	
UA4	X	000000B8	1	5571	
UA5	X	000000CC	8	5581	
UA6	X	000000EC	8	5587	
UA7	F	00000118	8	5598	
UA8	X	00000180	32	5627	
WPSW0008	3	000012C8	8	4805	4804
ZBRKADDR	A	00000110	8	5597	
ZEMONCNT	F	0000010C	4	5596	
ZEMONCTR	A	00000100	8	5594	
ZEMONSIZ	F	00000108	4	5595	
ZEXTNPSW	X	000001B0	16	5630	
ZEXTOPSW	X	00000130	16	5622	
ZIONPSW	X	000001F0	16	5634	
ZIOOPSW	X	00000170	16	5626	
ZMCKNPSW	X	000001E0	16	5633	
ZMCKOPSW	X	00000160	16	5625	
ZMKFAILA	F	000000F8	8	5589	
ZMONCODE	F	000000B0	8	5564	
ZPGMNPSW	X	000001D0	16	5632	
ZPGMOPSW	X	00000150	16	5624	
ZPGMTRX	F	000000A8	8	5563	
ZRSTNPSW	X	000001A0	16	5629	
ZRSTOPSW	X	00000120	16	5621	
ZSASDISP	U	000011C0	1	5635	
ZSVCNPSW	X	000001C0	16	5631	
ZSVCOPSW	X	00000140	16	5623	
=A(00+(5*K64))	A	0000152C	4	5034	4518
=A(MB+(5*K64))	A	00001530	4	5035	4520
=A(PAGE)	A	0000153C	4	5038	4649
=A(PAGETABS)	A	00001538	4	5037	4646 4673
=A(PFINSADR)	A	00001544	4	5040	4708
=A(PFPGBYTS)	A	00001540	4	5039	4667
=A(REG2PATT)	A	00001524	4	5032	3828
=A(SEGTABLS)	A	00001534	4	5036	4644
=CL5'CLC'	C	0000154C	5	5042	4017
=CL5'CLCL'	C	00001551	5	5043	4355
=CL5'MVCIN'	C	00001556	5	5044	4492
=CL5'TRT'	C	0000155B	5	5045	4631
=F'0'	F	00001528	4	5033	3853
=F'1'	F	00001548	4	5041	4876
=P'4294967296'	P	00001560	6	5046	4782

```
 MACRO     DEFN  REFERENCES

ANTR        110
APROB       242
ARCHIND     402   3432
ARCHLVL     543   3431
ASAIPL      669   3511
ASALOAD     749   3494
ASAREA      804   5481
ASAZAREA    989
CPUWAIT    1072   4801
DSECTS     1398   5313   5345   5392   5407   5478
DWAIT      1601   4930   4935   4940   4945
DWAITEND   1658   4929
ENADEV     1666   4966
ESA390     1766
IOCB       1777   4999
IOCBDS     1953   5314
IOFMT      1987   5346   5393   5408   5640   5658   5666   5703
IOINIT     2325   4954
IOTRFR     2366
ORB        2414   5018
POINTER    2603
PSWFMT     2631
RAWAIT     2765
RAWIO      2861   4788
SIGCPU     3019
SMMGR      3077
SMMGRB     3177
TRAP128    3226
TRAP64     3203   3496   3499
TRAPS      3239
ZARCH      3313
ZEROH      3325
ZEROL      3353
ZEROLH     3381
ZEROLL     3404
```

```
   DESC     SYMBOL    SIZE     POS        ADDR

Entry: 0

Image      IMAGE     12289  0000-3000  0000-3000
  Region   CODE      12289  0000-3000  0000-3000
    CSECT  CLCLETAL  12289  0000-3000  0000-3000
```

```
   STMT                                          FILE NAME

1     c:\Users\Fish\Documents\Visual Studio 2008\Projects\MyProjects\ASMA-0\CLCL-et-al\CLCL-et-al.asm
2     C:\Users\Fish\Documents\Visual Studio 2008\Projects\Hercules\_Git\_Harold\SATK-0\srcasm\satk.mac


** NO ERRORS FOUND **
```