```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    2 ********************************************************************************
                                                    3 *                                FLOAT
                                                    4 ********************************************************************************
                                                    5 *
                                                    6 *   This program performs a few EXTREMELY simple Floating Point
                                                    7 *   tests based on the instruction-use examples in Appendix A.
                                                    8 *   "Number Representation and Instruction-Use Examples" of the
                                                    9 *   SA22-7200-00 "ESA/370 Principles of Operation" manual.
                                                   10 *
                                                   11 *   Unlike other S/370 tests, this test runs in BC mode not EC mode
                                                   12 *   for no other reason than that's the mode that MVT runs in, and
                                                   13 *   at the time, there was some concern as to whether floating point
                                                   14 *   instructions were being executed properly (GitHub Issue #546).
                                                   15 *
                                                   16 ********************************************************************************
                                                   18 ********************************************************************************
                                                   19 *                                LOW CORE
                                                   20 ********************************************************************************
                           00000000  00000601    22 TEST     START 0
00000000                   00000000              23          USING TEST,0                Use absolute addressing

00000000                   00000000  00000000    25          ORG   TEST+X'00'           S/370 Restart new PSW
00000000  00000000                               26          DC    XL4'00000000'         S/370 Restart new PSW
00000004  00000200                               27          DC    A(BEGIN)              S/370 Restart new PSW

00000008                   00000008  00000068    29          ORG   TEST+X'68'           S/370 Program new PSW
00000068  00020000                               30          DC    XL4'00020000'         S/370 Program new PSW
0000006C  0000DEAD                               31          DC    A(X'DEAD')            S/370 Program new PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    33 ********************************************************************************
                                                    34 *                              MAINLINE
                                                    35 ********************************************************************************

00000070                      00000070  00000200    37          ORG   TEST+X'200'             Start of test program
00000200                                            38 BEGIN    DS    0H


00000200  45E0 0250                     00000250    40          BAL   R14,TEST1
00000204  45E0 0274                     00000274    41          BAL   R14,TEST2
00000208  45E0 0298                     00000298    42          BAL   R14,TEST3
0000020C  45E0 02D8                     000002D8    43          BAL   R14,TEST4
00000210  45E0 030A                     0000030A    44          BAL   R14,TEST5
00000214  45E0 0328                     00000328    45          BAL   R14,TEST6


00000218  9200 0600                     00000600    47          MVI   TESTNUM,0               No test has failed
0000021C  9200 0601                     00000601    48          MVI   SUBTEST,0               No sub-test has failed either

00000220  8200 0228                     00000228    50 SUCCESS  LPSW  GOODPSW                 Load  SUCCESS disabled wait PSW
00000228  00020000                                  51 GOODPSW  DC    0D'0',XL4'00020000'     S/370 SUCCESS disabled wait PSW
0000022C  00000000                                  52          DC    A(0)                    S/370 SUCCESS disabled wait PSW


00000230  8200 0238                     00000238    54 BADCC    LPSW  BADCCPSW                Load  FAILURE disabled wait PSW
00000238  00020000                                  55 BADCCPSW DC    0D'0',XL4'00020000'     S/370 FAILURE disabled wait PSW
0000023C  000BADCC                                  56          DC    A(X'BADCC')             S/370 FAILURE disabled wait PSW

00000240  8200 0248                     00000248    58 BADGOT   LPSW  FAILPSW                Load  FAILURE disabled wait PSW
00000248  00020000                                  59 FAILPSW  DC    0D'0',XL4'00020000'     S/370 FAILURE disabled wait PSW
0000024C  00BADBAD                                  60          DC    A(X'BADBAD')            S/370 FAILURE disabled wait PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                     62 ************************************************************************
                                                     63 *                 TEST 1:  AE/AD  (Add Normalized)
                                                     64 ************************************************************************

00000250  92F1 0600                         00000600    66 TEST1    MVI   TESTNUM,X'F1'
00000254  9200 0601                         00000601    67          MVI   SUBTEST,0
                                                        68 *
                                                        69 *  Add Normalized (AD, ADR, AE, AER, AXR)
                                                        70 *
                                                        71 *    FPR6 contains
                                                        72 *    C3 08 21 00 00 00 00 00
                                                        73 *
                                                        74 *    Storage location contains
                                                        75 *    41 12 34 56 00 00 00 00
                                                        76 *
                                                        77 *
                                                        78 *    Machine Format
                                                        79 *
                                                        80 *      Op Code R1 X2 B2 D2
                                                        81 *        7A     6  0  D 000
                                                        82 *
                                                        83 *
                                                        84 *    Assembler Format
                                                        85 *
                                                        86 *      Op Code R1,D2(X2,B2)
                                                        87 *        AE    6,0(0,13)
                                                        88 *
                                                        89 *
                                                        90 *  the result (left half of FPR6) is
                                                        91 *  C2 80 EC BB.
                                                        92 *
                                                        93 *  The right half of FPR6 is unchanged.
                                                        94 *
                                                        95 *  Condition code 1 is set (result less than zero).
                                                        96 *
                                                        97 *  If the long-precision instruction 'AD' were used,
                                                        98 *  the result in FPR6 would be
                                                        99 *  C2 80 BC BA A0 00 00 00.
                                                       100 *
00000258  6860 0350                         00000350   101          LD    FPR6,T1_FPR6
0000025C  7A60 0358                         00000358   102          AE    FPR6,T1_STRG
00000260  47B0 0230                         00000230   103          BC    B'1011',BADCC  (not CC1)
00000264  6060 0360                         00000360   104          STD   FPR6,T1_GOT
00000268  D507 0360 0368      00000360      00000368   105          CLC   T1_GOT,T1_WANT
0000026E  4770 0240                         00000240   106          BNE   BADGOT
00000272  07FE                                         107          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                    109 ********************************************************************************
                                                    110 *                  TEST 2:  AU  (Add Unnormalized)
                                                    111 ********************************************************************************

00000274  92F2 0600                         00000600   113 TEST2    MVI   TESTNUM,X'F2'
00000278  9200 0601                         00000601   114          MVI   SUBTEST,0
                                                    115 *
                                                    116 *  Add Unnormalized (AU, AUR, AW, AWR)
                                                    117 *
                                                    118 *  using the the same operands as in the
                                                    119 *  previous ADD NORMALIZED example:
                                                    120 *
                                                    121 *  FPR6 contains
                                                    122 *  C3 08 21 00 00 00 00 00
                                                    123 *
                                                    124 *  Storage location contains
                                                    125 *  41 12 34 56 00 00 00 00
                                                    126 *
                                                    127 *
                                                    128 *    Machine Format
                                                    129 *
                                                    130 *      Op Code R1 X2 B2 D2
                                                    131 *        7E     6  0  D 0000
                                                    132 *
                                                    133 *
                                                    134 *    Assembler Format
                                                    135 *
                                                    136 *      Op Code R1,D2(X2,B2)
                                                    137 *        AU    6,0(0,13)
                                                    138 *
                                                    139 *
                                                    140 *  result in FPR6
                                                    141 *  C3 08 0E CB 00 00 00 00
                                                    142 *
                                                    143 *  Condition code 1 is set (result less than zero).
                                                    144 *
0000027C  6860 0370                         00000370   145          LD    FPR6,T2_FPR6
00000280  7E60 0378                         00000378   146          AU    FPR6,T2_STRG
00000284  47B0 0230                         00000230   147          BC    B'1011',BADCC  (not CC1)
00000288  6060 0380                         00000380   148          STD   FPR6,T2_GOT
0000028C  D507 0380 0388      00000380     00000388   149          CLC   T2_GOT,T2_WANT
00000292  4770 0240                         00000240   150          BNE   BADGOT
00000296  07FE                                         151          BR    R14
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   153 ********************************************************************************
                                                   154 *                    TEST 3:  CDR  (Compare)
                                                   155 ********************************************************************************

00000298  92F3 0600                      00000600   157 TEST3    MVI   TESTNUM,X'F3'
0000029C  9200 0601                      00000601   158          MVI   SUBTEST,0
                                                   159 *
                                                   160 *  Compare (CD, CDR, CE, CER)
                                                   161 *
                                                   162 *  FPR4 contains
                                                   163 *  43 00 00 00 00 00 00 00 (zero)
                                                   164 *
                                                   165 *  FPR6 contains
                                                   166 *  35 12 34 56 78 9A BC DE (positive number).
                                                   167 *
                                                   168 *
                                                   169 *    Machine Format
                                                   170 *
                                                   171 *      Op Code R1 R2
                                                   172 *        29     4  6
                                                   173 *
                                                   174 *
                                                   175 *    Assembler Format
                                                   176 *
                                                   177 *      Op Code R1,R2
                                                   178 *       CDR     4,6
                                                   179 *
                                                   180 *
                                                   181 *  Condition code 1 is set (FPR4 less than FPR6).
                                                   182 *
                                                   183 *  If FPR6 instead contained
                                                   184 *  34 12 34 56 78 9A BC DE
                                                   185 *
                                                   186 *  Condition code 0 (equal) would instead be set.
                                                   187 *
                                                   188 *  As another example
                                                   189 *  41 00 12 34 56 78 9A BC
                                                   190 *
                                                   191 *  compares equal to all numbers of the form:
                                                   192 *  3F 12 34 56 78 9A BC 0X
                                                   193 *
                                                   194 *  where X represents any hexadecimal digit.
                                                   195 *
000002A0  6840 0390                      00000390   196          LD    FPR4,T3_FPR4
000002A4  6860 0398                      00000398   197          LD    FPR6,T3_FPR6
000002A8  2946                                      198          CDR   FPR4,FPR6
000002AA  47B0 0230                      00000230   199          BC    B'1011',BADCC  (not CC1)
000002AE  6860 03A0                      000003A0   200          LD    FPR6,T3_FPR6A
000002B2  2946                                      201          CDR   FPR4,FPR6
000002B4  4770 0230                      00000230   202          BC    B'0111',BADCC  (not CC0)
000002B8  6840 03A8                      000003A8   203          LD    FPR4,T3_FPR4A
000002BC  4110 03B0                      000003B0   204          LA    R1,T3_FPR6X
000002C0  4120 0010                      00000010   205          LA    R2,T3_NUMX
000002C4  6860 1000                      00000000   206 T3_XLOOP LD    FPR6,0(,R1)
000002C8  2946                                      207          CDR   FPR4,FPR6
000002CA  4770 0230                      00000230   208          BC    B'0111',BADCC  (not CC0)
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

000002CE  4110 1008                       00000008   209          LA    R1,8(,R1)
000002D2  4620 02C4                       000002C4   210          BCT   R2,T3_XLOOP
000002D6  07FE                            00000000   211          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                     213 ********************************************************************************
                                                     214 *                    TEST 4:  DER  (Divide)
                                                     215 ********************************************************************************

000002D8  92F4 0600                        00000600  217 TEST4    MVI   TESTNUM,X'F4'
000002DC  9200 0601                        00000601  218          MVI   SUBTEST,0
                                                     219 *
                                                     220 *  Divide (DD, DDR, DE, DER)
                                                     221 *
                                                     222 *  first operand  = dividend
                                                     223 *  second operand = divisor
                                                     224 *  resulting quotient = replaces first operand
                                                     225 *
                                                     226 *
                                                     227 *    Machine Format
                                                     228 *
                                                     229 *      Op Code R1 R2
                                                     230 *        3D     2  0
                                                     231 *
                                                     232 *
                                                     233 *    Assembler Format
                                                     234 *
                                                     235 *      Op Code R1,R2
                                                     236 *       DER     2,0
                                                     237 *
                                                     238 *
                                                     239 *          FPR2 Before  FPR0          FPR2 After
                                                     240 *  Case    (Dividend)   (Divisor)     (Quotient)
                                                     241 *
                                                     242 *   A      -43 082100   +43 001234    -42 72522F
                                                     243 *   B      +42 101010   +45 111111    +3D F0F0F0
                                                     244 *   C      +48 30000F   +41 400000    +47 C0003C
                                                     245 *   D      +48 30000F   +41 200000    +48 180007
                                                     246 *   E      +48 180007   +41 200000    +47 C00038
                                                     247 *
000002E0  4110 0430                        00000430  248          LA    R1,T4_A
000002E4  4120 0005                        00000005  249          LA    R2,T4_NUMT
000002E8  7820 1000                        00000000  250 T4_LOOP  LE    FPR2,0(,R1)
000002EC  7800 1004                        00000004  251          LE    FPR0,4(,R1)
000002F0  3D20                                       252          DER   FPR2,FPR0
000002F2  7020 046C                        0000046C  253          STE   FPR2,T4_GOT
000002F6  D503 046C 1008      0000046C    00000008  254          CLC   T4_GOT,8(R1)
000002FC  4770 0240                        00000240  255          BNE   BADGOT
00000300  4110 100C                        0000000C  256          LA    R1,3*4(,R1)
00000304  4620 02E8                        000002E8  257          BCT   R2,T4_LOOP
00000308  07FE                                       258          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                    260 ********************************************************************************
                                                    261 *                    TEST 5:  HDR  (Halve)
                                                    262 ********************************************************************************

0000030A  92F5 0600                        00000600   264 TEST5    MVI   TESTNUM,X'F5'
0000030E  9200 0601                        00000601   265          MVI   SUBTEST,0
                                                    266
                                                    267 *
                                                    268 *  Halve (HDR, HER)
                                                    269 *
                                                    270 *  HALVE produces the same result as floating-point
                                                    271 *  DIVIDE with a divisor of 2.0.
                                                    272 *
                                                    273 *  FPR2 contains
                                                    274 *  + 48 30 00 00 00 00 00 0F
                                                    275 *
                                                    276 *  FPR2 result
                                                    277 *  + 48 18 00 00 00 00 00 07
                                                    278 *
                                                    279 *
                                                    280 *    Machine Format
                                                    281 *
                                                    282 *      Op Code R1 R2
                                                    283 *        24     2  2
                                                    284 *
                                                    285 *    Assembler Format
                                                    286 *
                                                    287 *       Op Code R1,R2
                                                    288 *        HDR     2,2
                                                    289 *
00000312  6820 0470                        00000470   290          LD    FPR2,T5_FPR2
00000316  2422                                      291          HDR   FPR2,FPR2
00000318  6020 0478                        00000478   292          STD   FPR2,T5_GOT
0000031C  D507 0478 0480      00000478     00000480   293          CLC   T5_GOT,T5_WANT
00000322  4770 0240                        00000240   294          BNE   BADGOT
00000326  07FE                                      295          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    297 ********************************************************************************
                                                    298 *                    TEST 6:  MDR  (Multiply)
                                                    299 ********************************************************************************

00000328  92F6 0600                         00000600   301 TEST6    MVI   TESTNUM,X'F6'
0000032C  9200 0601                         00000601   302          MVI   SUBTEST,0
                                                    303 *
                                                    304 *  Multiply (MD, MDR, ME, MER, MXD, MXDR, MXR)
                                                    305 *
                                                    306 *  FPR0: -33 606060 60606060
                                                    307 *  FPR2: -5A 200000 20000020
                                                    308 *
                                                    309 *
                                                    310 *    Machine Format
                                                    311 *
                                                    312 *      Op Code R1 R2
                                                    313 *        2C     0  2
                                                    314 *
                                                    315 *    Assembler Format
                                                    316 *
                                                    317 *      Op Code R1,R2
                                                    318 *        MDR    0,2
                                                    319 *
                                                    320 *
                                                    321 *  Final FPR0 result:
                                                    322 *  +4C C0C0C1 81818241
                                                    323 *
00000330  6800 0488                         00000488   324          LD    FPR0,T6_FPR0
00000334  6820 0490                         00000490   325          LD    FPR2,T6_FPR2
00000338  2C02                                         326          MDR   FPR0,FPR2
0000033A  6000 0498                         00000498   327          STD   FPR0,T6_GOT
0000033E  D507 0498 04A0          00000498  000004A0   328          CLC   T6_GOT,T6_WANT
00000344  4770 0240                         00000240   329          BNE   BADGOT
00000348  07FE                                         330          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     332 ********************************************************************************
                                                     333 *                          Working storage
                                                     334 ********************************************************************************

0000034A                                             336          LTORG ,                            Literals Pool


00000350                                             338          DC    0D'0'
00000350  C3082100 00000000                         339 T1_FPR6  DC    XL8'C3 08 21 00 00 00 00 00'
00000358  41123456 00000000                         340 T1_STRG  DC    XL8'41 12 34 56 00 00 00 00'
00000360  00000000 00000000                         341 T1_GOT   DC    XL8'00'
00000368  C280ECBB 00000000                         342 T1_WANT  DC    XL8'C2 80 EC BB 00 00 00 00'


00000370  C3082100 00000000                         344 T2_FPR6  DC    XL8'C3 08 21 00 00 00 00 00'
00000378  41123456 00000000                         345 T2_STRG  DC    XL8'41 12 34 56 00 00 00 00'
00000380  00000000 00000000                         346 T2_GOT   DC    XL8'00'
00000388  C3080ECB 00000000                         347 T2_WANT  DC    XL8'C3 08 0E CB 00 00 00 00'


00000390  43000000 00000000                         349 T3_FPR4  DC    XL8'43 00 00 00 00 00 00 00'
00000398  35123456 789ABCDE                         350 T3_FPR6  DC    XL8'35 12 34 56 78 9A BC DE'
000003A0  34123456 789ABCDE                         351 T3_FPR6A DC    XL8'34 12 34 56 78 9A BC DE'
000003A8  41001234 56789ABC                         352 T3_FPR4A DC    XL8'41 00 12 34 56 78 9A BC'
000003B0  3F123456 789ABC00                         353 T3_FPR6X DC    XL8'3F 12 34 56 78 9A BC 00'
000003B8  3F123456 789ABC01                         354          DC    XL8'3F 12 34 56 78 9A BC 01'
000003C0  3F123456 789ABC02                         355          DC    XL8'3F 12 34 56 78 9A BC 02'
000003C8  3F123456 789ABC03                         356          DC    XL8'3F 12 34 56 78 9A BC 03'
000003D0  3F123456 789ABC04                         357          DC    XL8'3F 12 34 56 78 9A BC 04'
000003D8  3F123456 789ABC05                         358          DC    XL8'3F 12 34 56 78 9A BC 05'
000003E0  3F123456 789ABC06                         359          DC    XL8'3F 12 34 56 78 9A BC 06'
000003E8  3F123456 789ABC07                         360          DC    XL8'3F 12 34 56 78 9A BC 07'
000003F0  3F123456 789ABC08                         361          DC    XL8'3F 12 34 56 78 9A BC 08'
000003F8  3F123456 789ABC09                         362          DC    XL8'3F 12 34 56 78 9A BC 09'
00000400  3F123456 789ABC0A                         363          DC    XL8'3F 12 34 56 78 9A BC 0A'
00000408  3F123456 789ABC0B                         364          DC    XL8'3F 12 34 56 78 9A BC 0B'
00000410  3F123456 789ABC0C                         365          DC    XL8'3F 12 34 56 78 9A BC 0C'
00000418  3F123456 789ABC0D                         366          DC    XL8'3F 12 34 56 78 9A BC 0D'
00000420  3F123456 789ABC0E                         367          DC    XL8'3F 12 34 56 78 9A BC 0E'
00000428  3F123456 789ABC0F                         368          DC    XL8'3F 12 34 56 78 9A BC 0F'
                           00000010  00000001       369 T3_NUMX  EQU   (*-T3_FPR6X)/8
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    371          PRINT DATA
00000430  C3082100 43001234                         372 T4_A     DC    XL4'C3 082100',XL4'43 001234',XL4'C2 72522F'
00000438  C272522F
0000043C  42101010 45111111                         373 T4_B     DC    XL4'42 101010',XL4'45 111111',XL4'3D F0F0F0'
00000444  3DF0F0F0
00000448  4830000F 41400000                         374 T4_C     DC    XL4'48 30000F',XL4'41 400000',XL4'47 C0003C'
00000450  47C0003C
00000454  4830000F 41200000                         375 T4_D     DC    XL4'48 30000F',XL4'41 200000',XL4'48 180007'
0000045C  48180007
00000460  48180007 41200000                         376 T4_E     DC    XL4'48 180007',XL4'41 200000',XL4'47 C00038'
00000468  47C00038
                             00000005  00000001     377 T4_NUMT  EQU   (*-T4_A)/(3*4)
0000046C  00000000                                  378 T4_GOT   DC    XL4'00'
                                                    379          PRINT NODATA
00000470                                            380          DC    0D'0'    (alignment)


00000470  48300000 0000000F                         382 T5_FPR2  DC    XL8'48 30 00 00 00 00 00 0F'
00000478  00000000 00000000                         383 T5_GOT   DC    XL8'00'
00000480  48180000 00000007                         384 T5_WANT  DC    XL8'48 18 00 00 00 00 00 07'


00000488  B3606060 60606060                         386 T6_FPR0  DC    XL8'B3 606060 60606060'
00000490  DA200000 20000020                         387 T6_FPR2  DC    XL8'DA 200000 20000020'
00000498  00000000 00000000                         388 T6_GOT   DC    XL8'00'
000004A0  4CC0C0C1 81818241                         389 T6_WANT  DC    XL8'4C C0C0C1 81818241'



000004A8                     000004A8  00000600     391          ORG   TEST+X'600'              Test flags

00000600  00                                        393 TESTNUM  DC    X'00'                    Test number that failed
00000601  00                                        394 SUBTEST  DC    X'00'                    Sub-test number that failed
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                          396 ********************************************************************************
                                          397 *                          Register equates
                                          398 ********************************************************************************

                                00000000  00000001   400 R0       EQU   0
                                00000001  00000001   401 R1       EQU   1
                                00000002  00000001   402 R2       EQU   2
                                00000003  00000001   403 R3       EQU   3
                                00000004  00000001   404 R4       EQU   4
                                00000005  00000001   405 R5       EQU   5
                                00000006  00000001   406 R6       EQU   6
                                00000007  00000001   407 R7       EQU   7
                                00000008  00000001   408 R8       EQU   8
                                00000009  00000001   409 R9       EQU   9
                                0000000A  00000001   410 R10      EQU   10
                                0000000B  00000001   411 R11      EQU   11
                                0000000C  00000001   412 R12      EQU   12
                                0000000D  00000001   413 R13      EQU   13
                                0000000E  00000001   414 R14      EQU   14
                                0000000F  00000001   415 R15      EQU   15

                                00000000  00000001   417 FPR0     EQU   0
                                00000002  00000001   418 FPR2     EQU   2
                                00000004  00000001   419 FPR4     EQU   4
                                00000006  00000001   420 FPR6     EQU   6

                                          00000000   422          END   TEST
```

```
     SYMBOL         TYPE  VALUE   LENGTH  DEFN  REFERENCES

BADCC                I    000230       4    54  103  147  199  202  208
BADCCPSW             D    000238       8    55   54
BADGOT               I    000240       4    58  106  150  255  294  329
BEGIN                H    000200       2    38   27
FAILPSW              D    000248       8    59   58
FPR0                 U    000000       1   417  251  252  324  326  327
FPR2                 U    000002       1   418  250  252  253  290  291  292  325  326
FPR4                 U    000004       1   419  196  198  201  203  207
FPR6                 U    000006       1   420  101  102  104  145  146  148  197  198  200  201  206  207
GOODPSW              D    000228       8    51   50
IMAGE                1    000000    1538     0
R0                   U    000000       1   400
R1                   U    000001       1   401  204  206  209  248  250  251  254  256
R10                  U    00000A       1   410
R11                  U    00000B       1   411
R12                  U    00000C       1   412
R13                  U    00000D       1   413
R14                  U    00000E       1   414   40   41   42   43   44   45  107  151  211  258  295  330
R15                  U    00000F       1   415
R2                   U    000002       1   402  205  210  249  257
R3                   U    000003       1   403
R4                   U    000004       1   404
R5                   U    000005       1   405
R6                   U    000006       1   406
R7                   U    000007       1   407
R8                   U    000008       1   408
R9                   U    000009       1   409
SUBTEST              X    000601       1   394   48   67  114  158  218  265  302
SUCCESS              I    000220       4    50
T1_FPR6              X    000350       8   339  101
T1_GOT               X    000360       8   341  104  105
T1_STRG              X    000358       8   340  102
T1_WANT              X    000368       8   342  105
T2_FPR6              X    000370       8   344  145
T2_GOT               X    000380       8   346  148  149
T2_STRG              X    000378       8   345  146
T2_WANT              X    000388       8   347  149
T3_FPR4              X    000390       8   349  196
T3_FPR4A             X    0003A8       8   352  203
T3_FPR6              X    000398       8   350  197
T3_FPR6A             X    0003A0       8   351  200
T3_FPR6X             X    0003B0       8   353  369  204
T3_NUMX              U    000010       1   369  205
T3_XLOOP             I    0002C4       4   206  210
T4_A                 X    000430       4   372  377  248
T4_B                 X    00043C       4   373
T4_C                 X    000448       4   374
T4_D                 X    000454       4   375
T4_E                 X    000460       4   376
T4_GOT               X    00046C       4   378  253  254
T4_LOOP              I    0002E8       4   250  257
T4_NUMT              U    000005       1   377  249
T5_FPR2              X    000470       8   382  290
T5_GOT               X    000478       8   383  292  293
T5_WANT              X    000480       8   384  293
T6_FPR0              X    000488       8   386  324
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T6_FPR2	X	000490	8	387	325
T6_GOT	X	000498	8	388	327 328
T6_WANT	X	0004A0	8	389	328
TEST	J	000000	1538	22	25 29 37 391 23 422
TEST1	I	000250	4	66	40
TEST2	I	000274	4	113	41
TEST3	I	000298	4	157	42
TEST4	I	0002D8	4	217	43
TEST5	I	00030A	4	264	44
TEST6	I	000328	4	301	45
TESTNUM	X	000600	1	393	47 66 113 157 217 264 301

MACRO DEFN REFERENCES

No defined macros

```
   DESC     SYMBOL   SIZE     POS       ADDR

Entry: 0

Image       IMAGE    1538   000-601   000-601
  Region             1538   000-601   000-601
    CSECT   TEST     1538   000-601   000-601
```

STMT FILE NAME

1 c:\Users\Fish\Documents\Visual Studio 2008\Projects\MyProjects\ASMA-0\float\float.asm

** NO ERRORS FOUND **