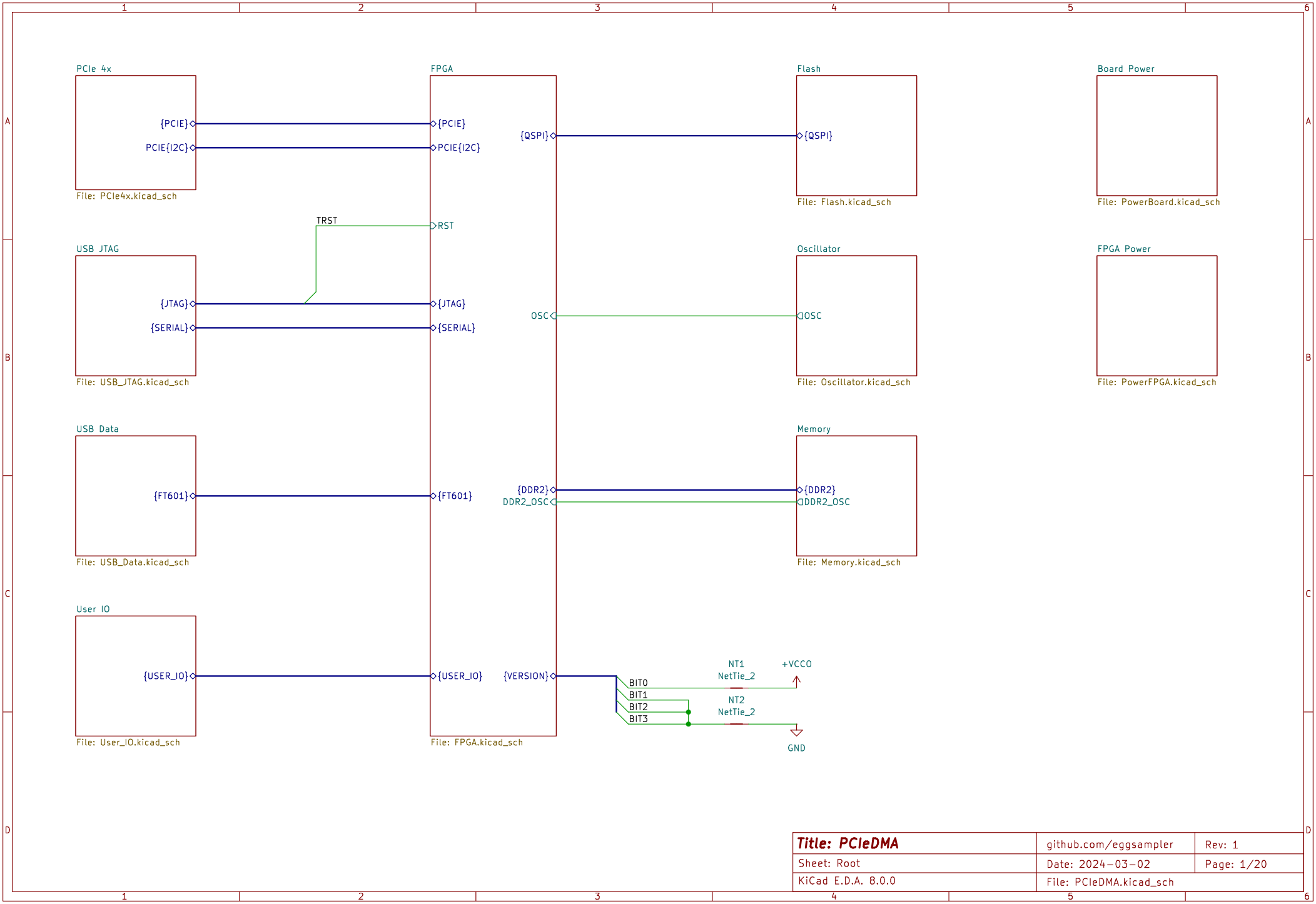
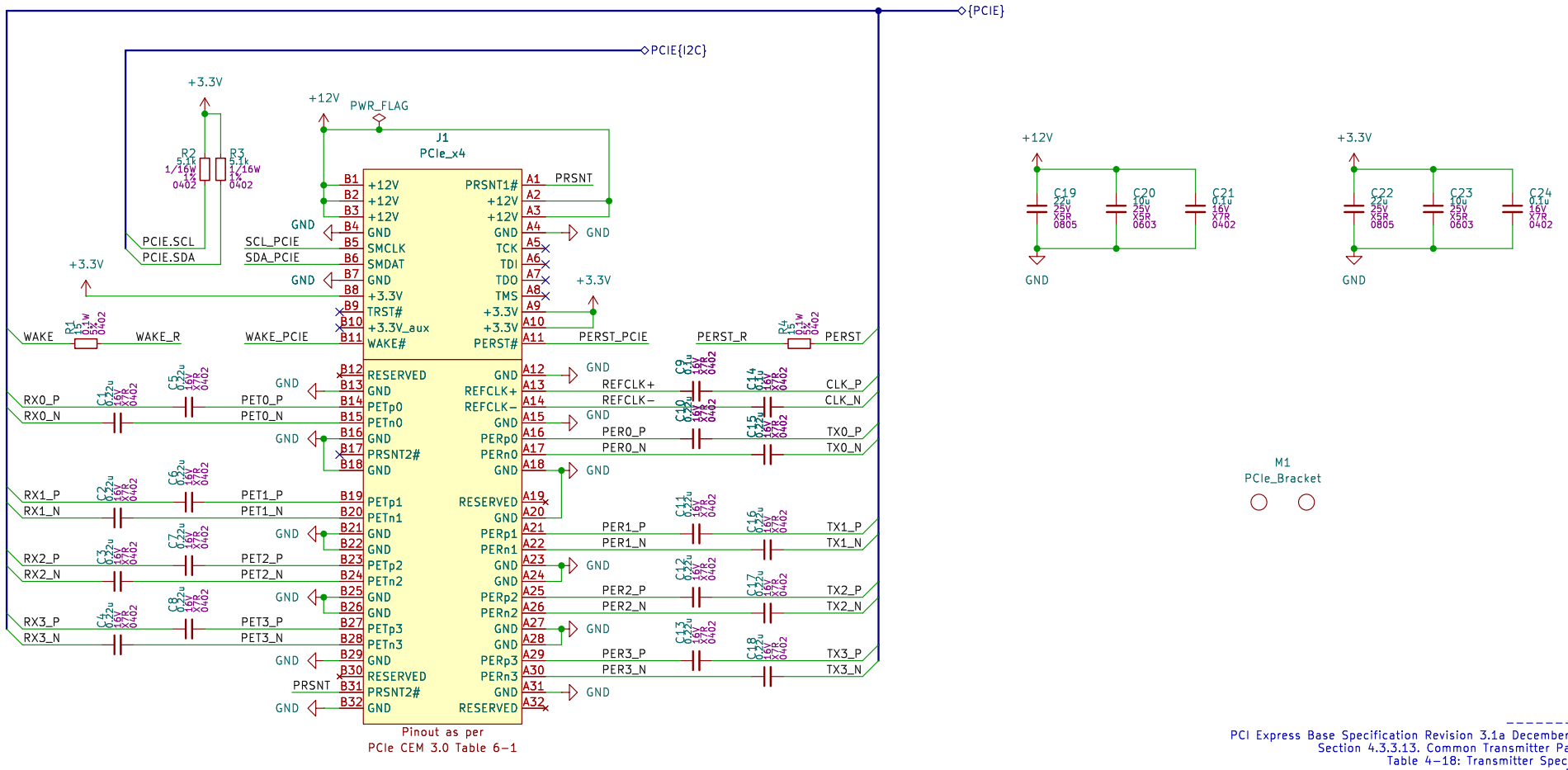
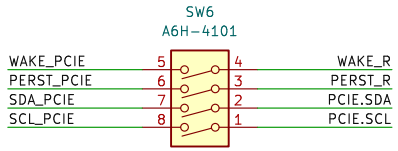

PCIe 4x
{PCIE}
PCIE{I2C}
File: PCIe4x.kicad_sch
FPGA
{PCIE}
PCIE{I2C}
RST
{JTAG}
{SERIAL}
{QSPI}
OSC
{DDR2}
DDR2_OSC
{FT601}
{USER_IO}
{VERSION}
BIT0
BIT1
BIT2
BIT3
NT1
NetTie_2
NT2
NetTie_2
+VCCO
GND
File: FPGA.kicad_sch
Flash
{QSPI}
File: Flash.kicad_sch
Board Power
File: PowerBoard.kicad_sch
TRST
USB JTAG
{JTAG}
{SERIAL}
File: USB_JTAG.kicad_sch
Oscillator
OSC
File: Oscillator.kicad_sch
FPGA Power
File: PowerFPGA.kicad_sch
USB Data
{FT601}
File: USB_Data.kicad_sch
Memory
{DDR2}
DDR2_OSC
File: Memory.kicad_sch
User IO
{USER_IO}
File: User_IO.kicad_sch
Title: PCIeDMA
github.com/eggsampler
Rev: 1
Sheet: Root
Date: 2024-03-02
Page: 1/20
KiCad E.D.A. 8.0.0
File: PCIeDMA.kicad_sch





Notes:

DIP Switches for enabling/disabling hardware lines

Notes:

PCI Express Base Specification Revision 3.1a December 7 2015,
Section 4.3.3.13. Common Transmitter Parameters
Table 4-18: Transmitter Specifications
Page 376

Lists AC Coupling Capacitor values of 75-265nF for 2.5GT/s, 75-265nF for 5.0 GT/s and 176 to 265nF for 8 GT/s
Note 14: All platforms that have transmitters supporting 8.0 GT/s must implement the 176-265 nF CTX value.
Platforms operating at 2.5 or 5.0 GT/s only may implement over a range of 75 to 265 nF.

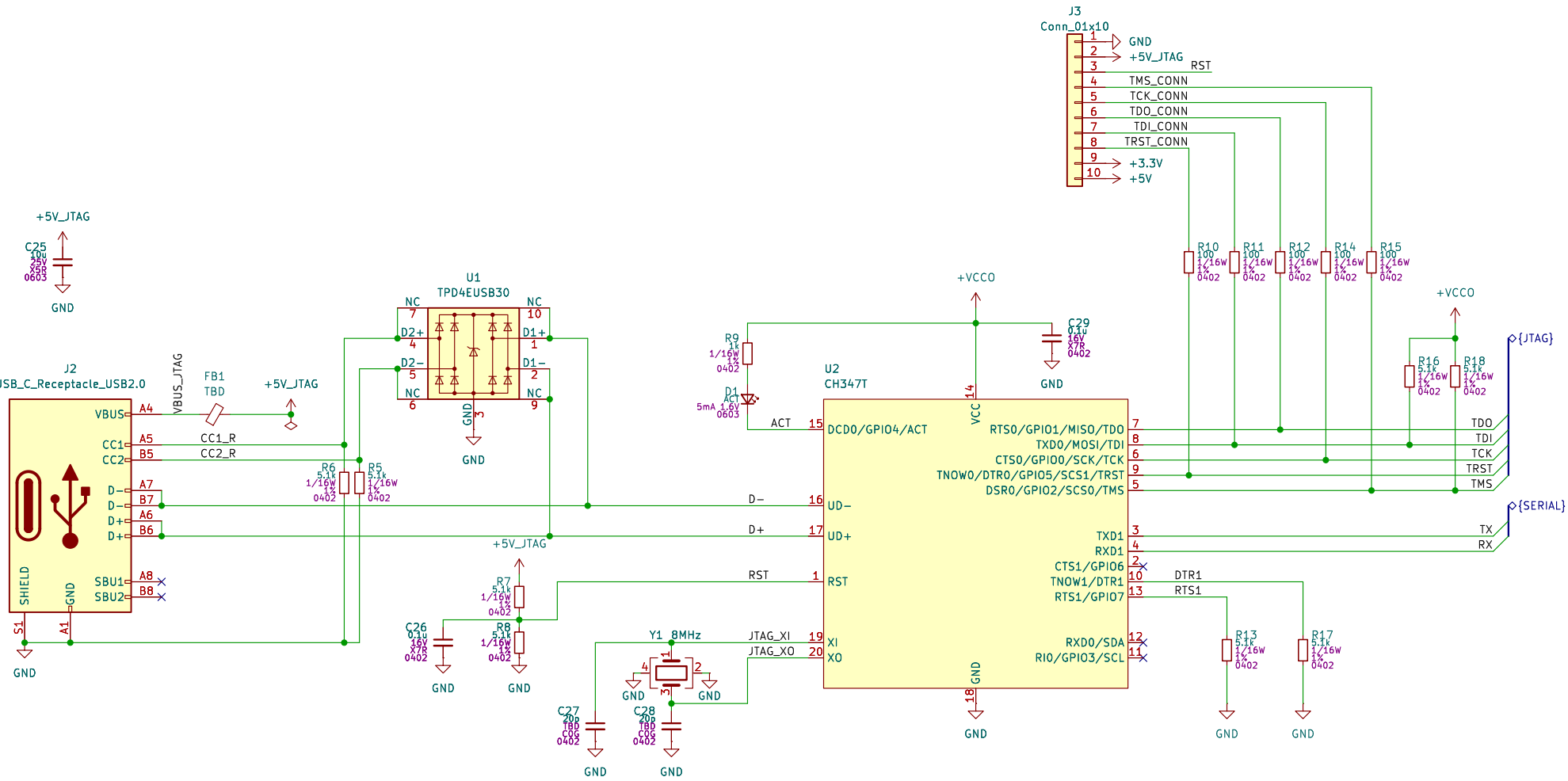
The REFCLK coupling is not a PCIe spec, but a Xilinx recommendation. 100nF for LVDS
(even though the REFCLK is HSCL).
AC701 uses 10nF caps, shouldn't matter too much.

PCI Express Card Electromechanical Specification Revision 3.0 July 21, 2013
Section 3.2. Presence Detect
Page 41
tldr used for hotplugging and isolation, connect PRSNT1# to longest supported PRSNT2# pin
---
PCIe 3.3V supply is used, but electromechanical spec table 4-1 page 44 gives +/- 9% which is a little too close to
Artix-7 DS181 absolute max V_CCO of 3.6V (and above recommended max of 3.465V)

Solder jumpers on SMBUS, WAKE and PERST lines for detection/customisation purposes

Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: PCIe 4x	Date: 2024-01-01	Page: 2/20
KiCad E.D.A. 8.0.0	File: PCIe4x.kicad_sch	

JTAG

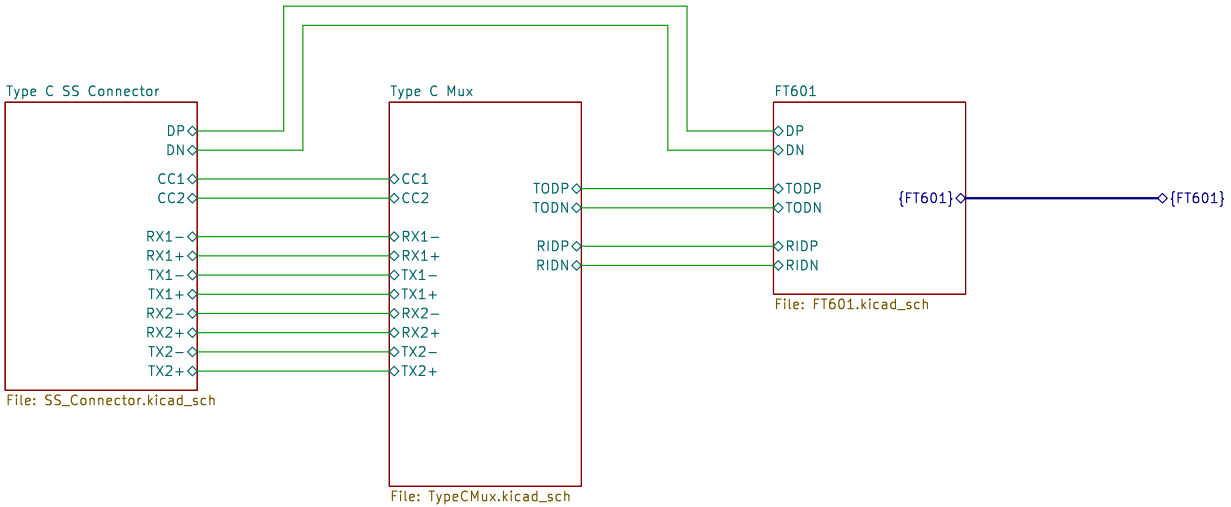


Notes:

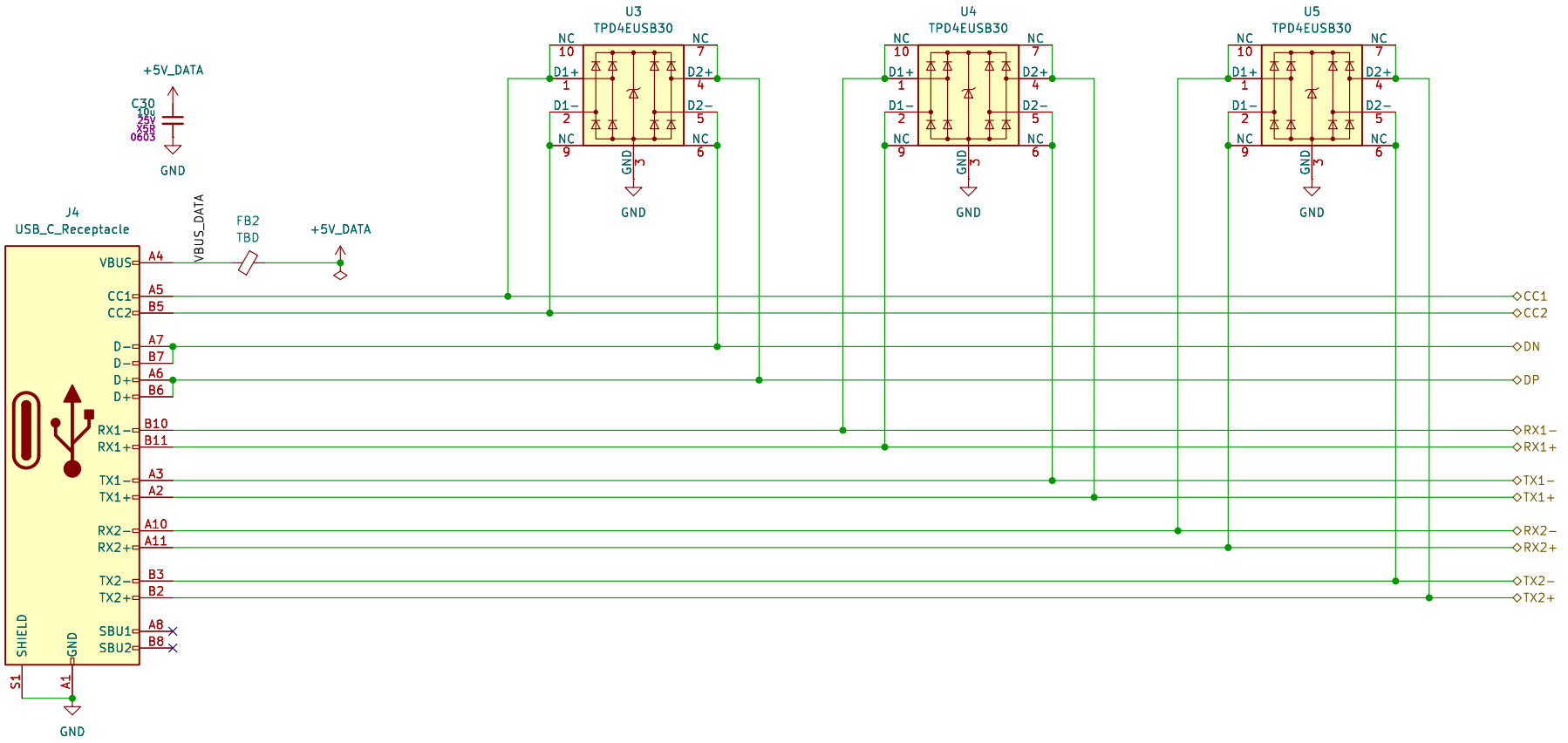
TODO: Calculate crystal load capacitors based on crystal part selection

RST pin pulled to 2.5V above VIH3 of 2.0V when +5V_JTAG USB is connected via voltage divider. Pulled low by divider when no +5_JTAG

Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: USB JTAG	Date: 2024-01-01	Page: 3/20
KiCad E.D.A. 8.0.0	File: USB_JTAG.kicad_sch	



Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: USB Data	Date: 2024−01−01	Page: 4/20
KiCad E.D.A. 8.0.0	File: USB_Data.kicad_sch	

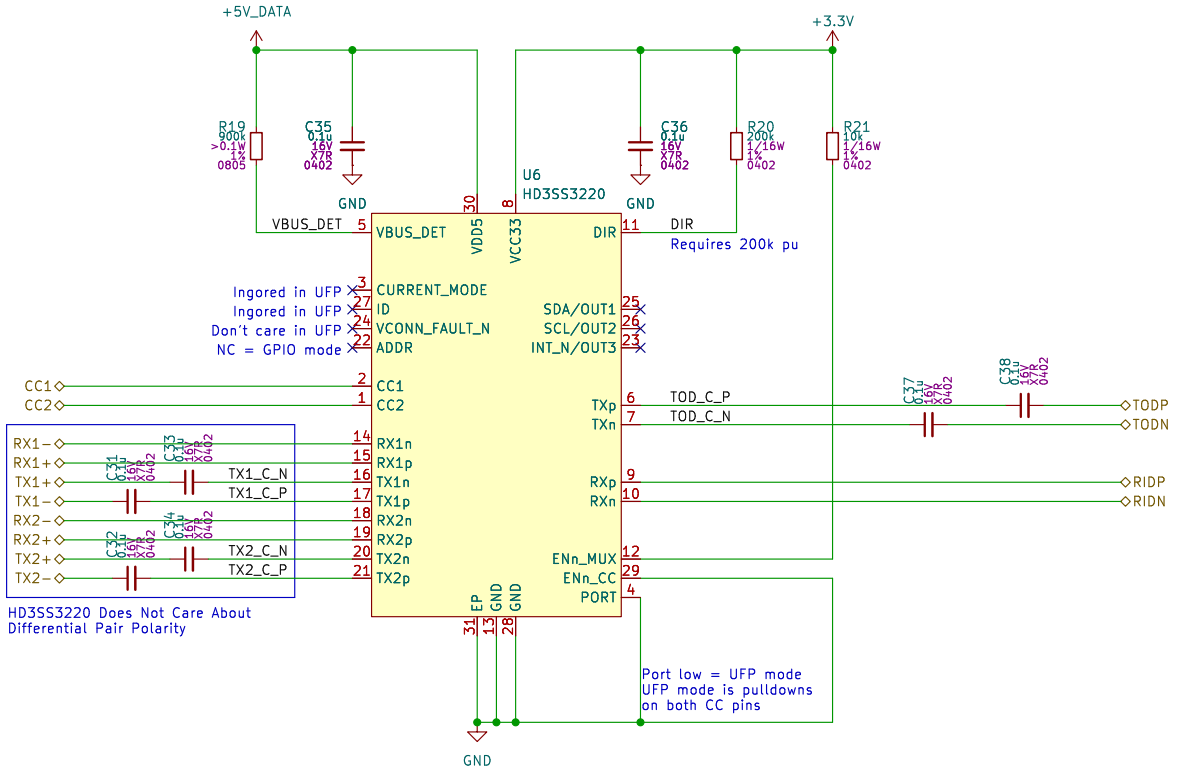


Notes:

+5V_Data is used for the mux and FT601

TPD4EUSB30 is used instead of a single part to simplify the BOM, as this can be used for the jtag interface too.

Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: Type C SS Connector	Date: 2024−01−01	Page: 5/20
KiCad E.D.A. 8.0.0	File: SS_Connector.kicad_sch	



Notes:

7.3.12 VDD5 and VCC33 Power−On Requirements

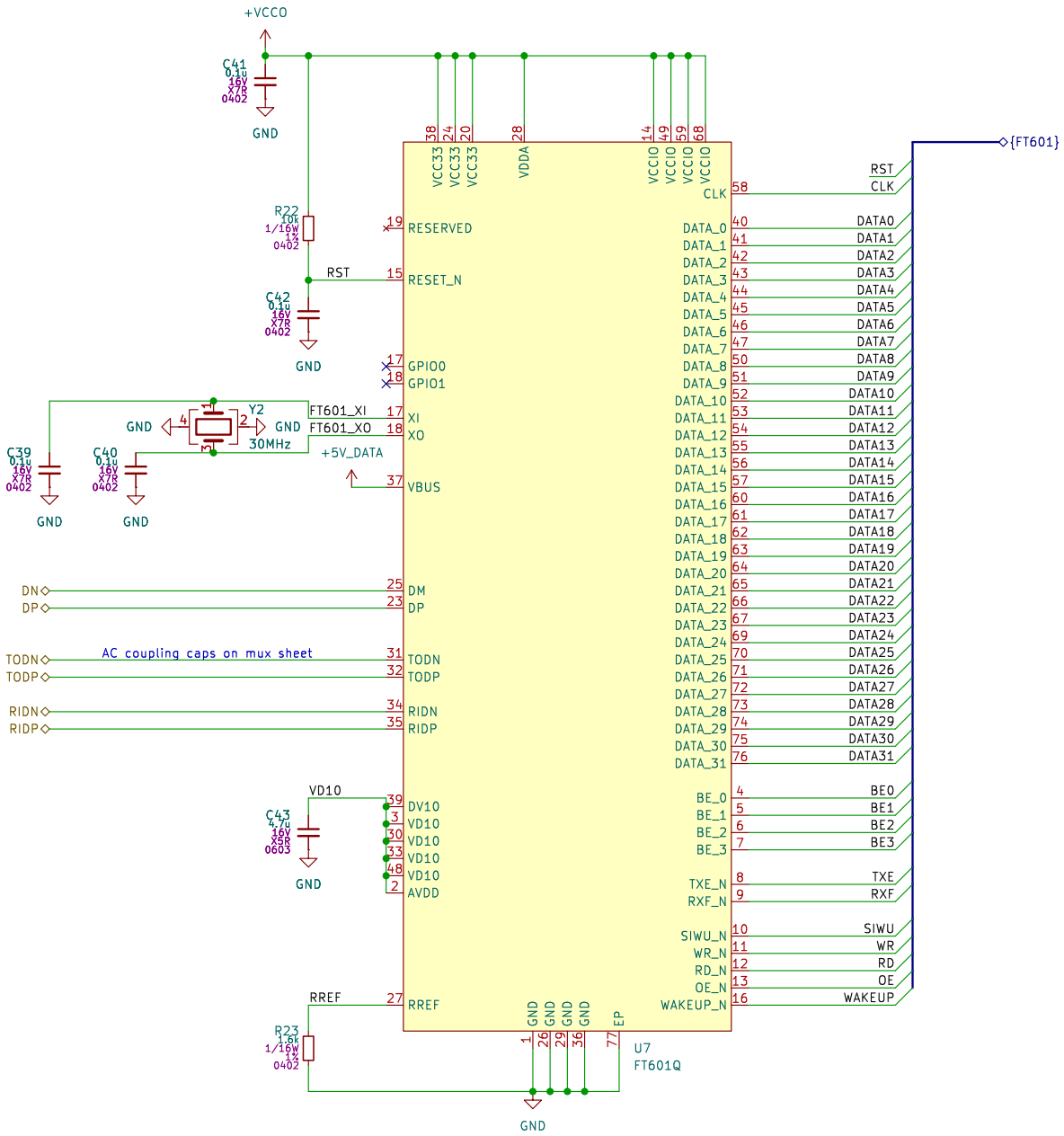
The HD3SS3220 has two power supplies: VDD5 and VCC33. The VDD5 supply powers the internal CC controller and also provides VCONN to either CC1 or CC2. The VCC33 powers the 2:1 MUX.

The HD3SS3220 non−failsafe pins are the following: PORT, ADDR, SDA/OUT1, SCL/OUT2, INT_IN/OUT3, VCONN_FAULT_N, and DIR. If any of these non−failsafe pins are pulled−up to a supply other than VDD5, then VDD5 supply must be powered up before the VCC33 supply. If it is not possible to power up VDD5 before VCC33, then the ENn_CC pin must be held high while both supplies are ramping and then asserted low after both supplies are stable

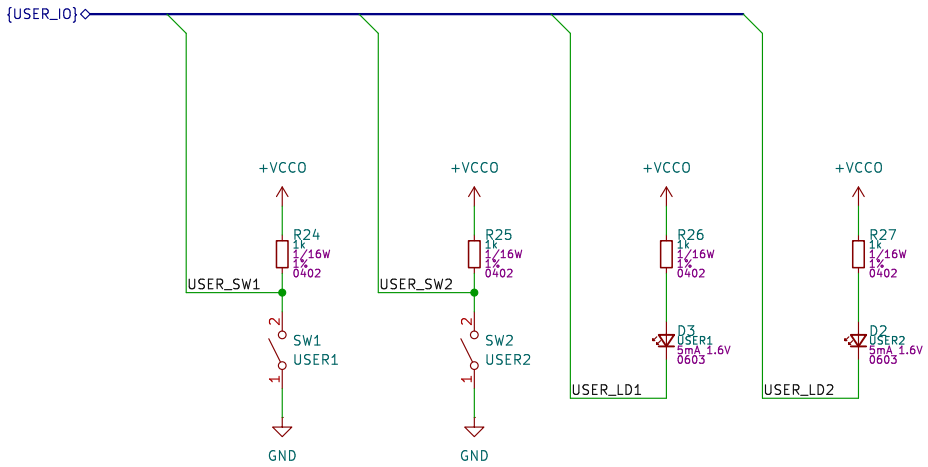
Notes:

Schematic based on datasheet 8.2.4 UFP port

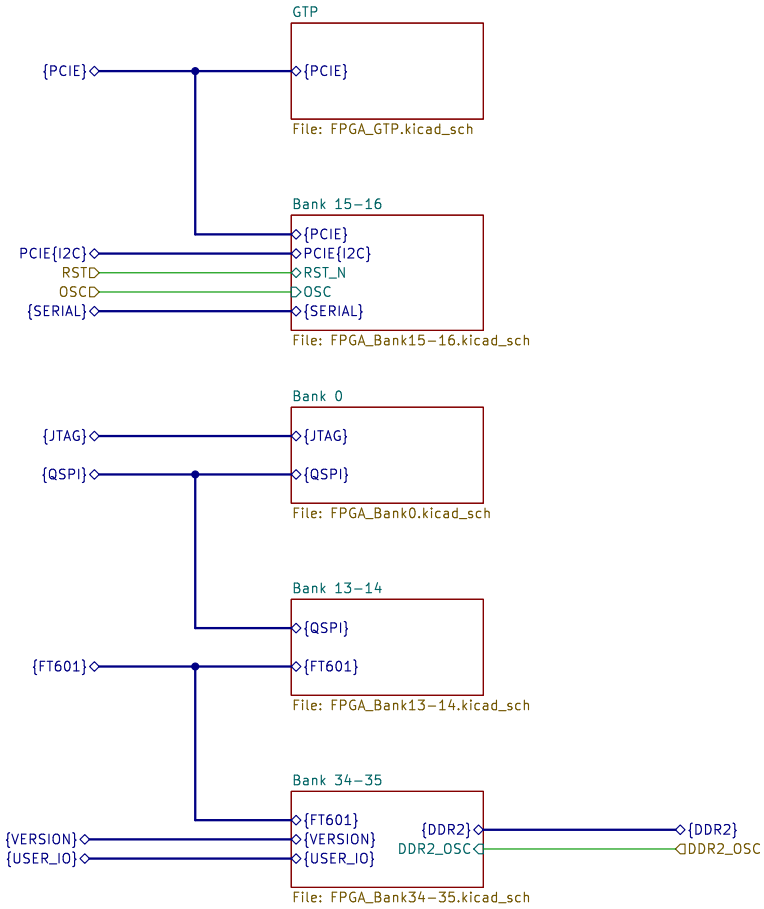
Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: Type C Mux	Date: 2024−01−01	Page: 6/20
KiCad E.D.A. 8.0.0	File: TypeCMux.kicad_sch	



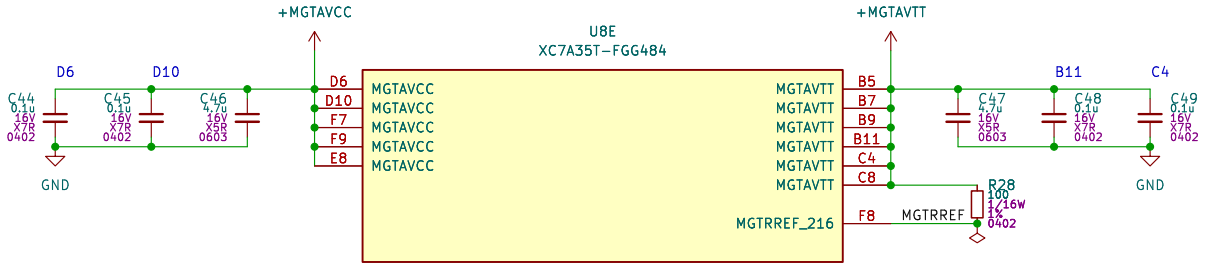
Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: FT601	Date: 2024-01-01	Page: 7/20
KiCad E.D.A. 8.0.0	File: FT601.kicad_sch	

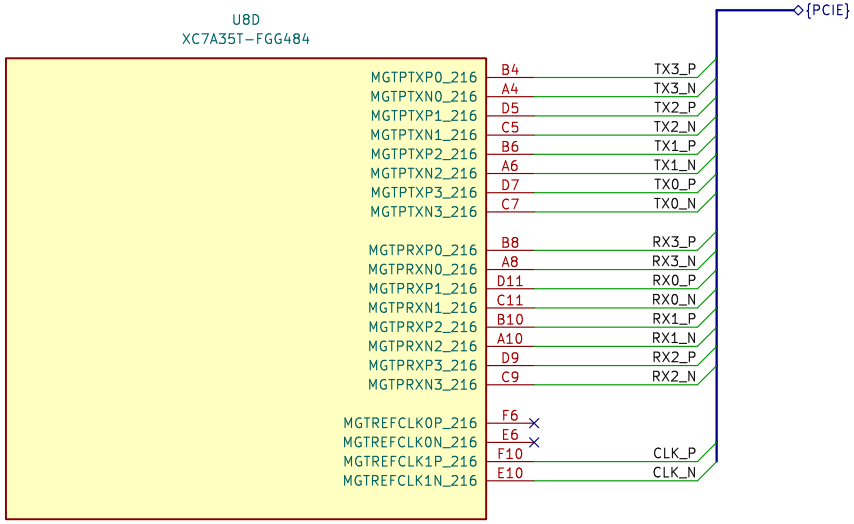


Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: User IO	Date: 2024-01-01	Page: 8/20
KiCad E.D.A. 8.0.0	File: User_IO.kicad_sch	



Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: FPGA	Date: 2024–01–01	Page: 9/20
KiCad E.D.A. 8.0.0	File: FPGA.kicad_sch	





Notes:

DS181 Page 2, Table 2: Recommended Operating Conditions
VMGTAVCC: Typical 1.0V
VMGTAVTT: Typical 1.2V

UG482 Table 5-14: MGTRREF – Connect to a 100Ω resistor that is also connected to MGTAVTT
Termination Resistor Calibration Circuit: The MGTRREF pin should be connected to the MGTAVTT supply through a 100Ω precision external resistor.

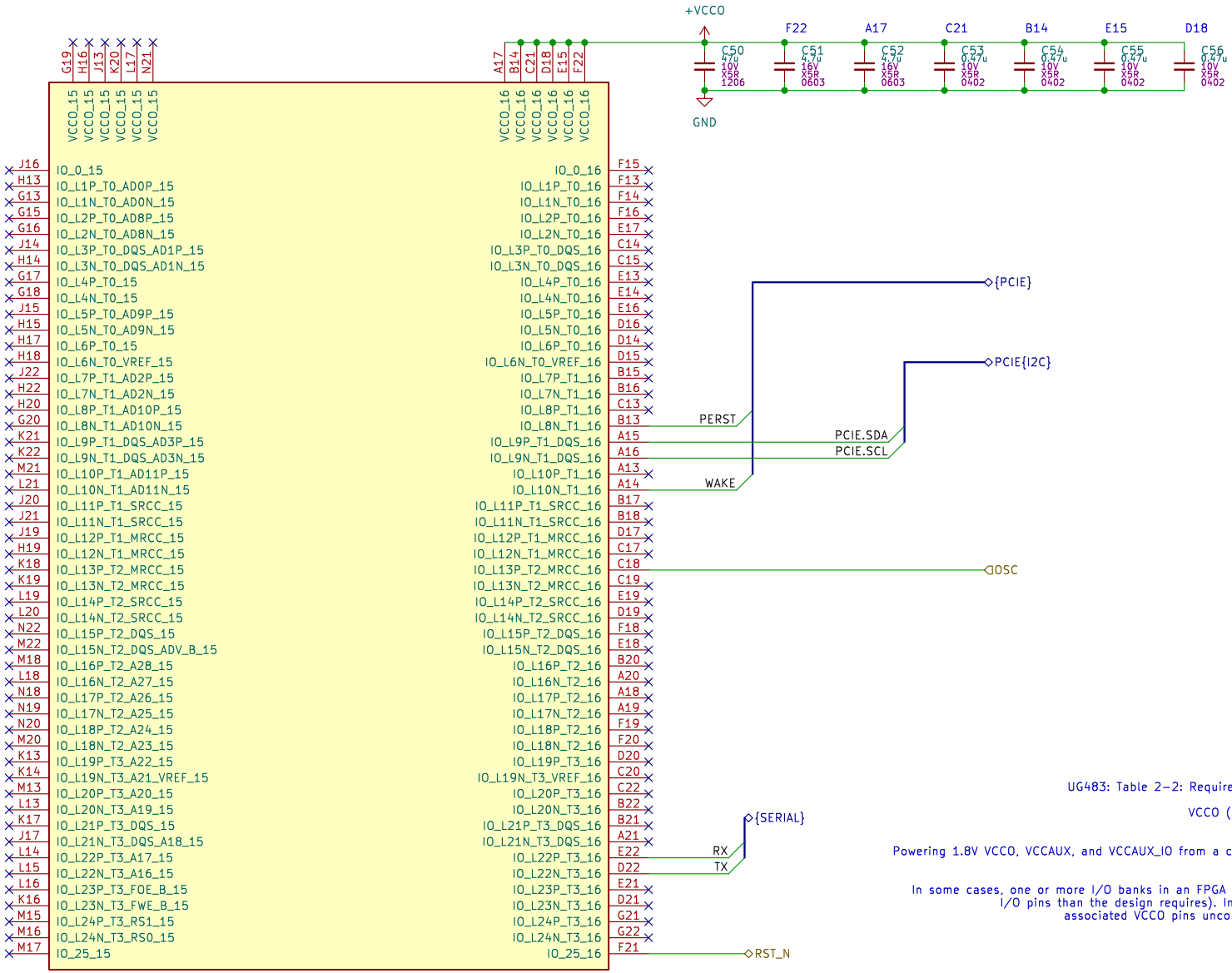
UG482: Unused Reference Clocks
It is recommended to leave the unused differential input pin clock pair floating (both MGTREFCLKP and MGTREFCLKN)

UG482: Power Supply Decoupling Capacitors
One 4.7uF 10% Ceramic capacitor per MGTAVCC group
Two 0.1uF 10% Ceramic capacitor per MGTAVTT power supply group
The larger 4.7 µF capacitors should be placed in close proximity and outside the perimeter of the FPGA pin field.
The 0.1µF capacitors on the other hand must be placed as close to the GTP Quad power supply pins as possible.
(See this section for 0.1uF capacitor pin placement)

UG482 Page 236
(For both MGTAVCC_G[N] and MGTAVTT_G[N])
The power supply regulator for this voltage should not be shared with non-transceiver loads.

AC coupling capacitors for RX and TX differential pairs are on PCIe connector sheet

Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: GTP	Date: 2024-01-01	Page: 10/20
KiCad E.D.A. 8.0.0	File: FPGA_GTP.kicad_sch	



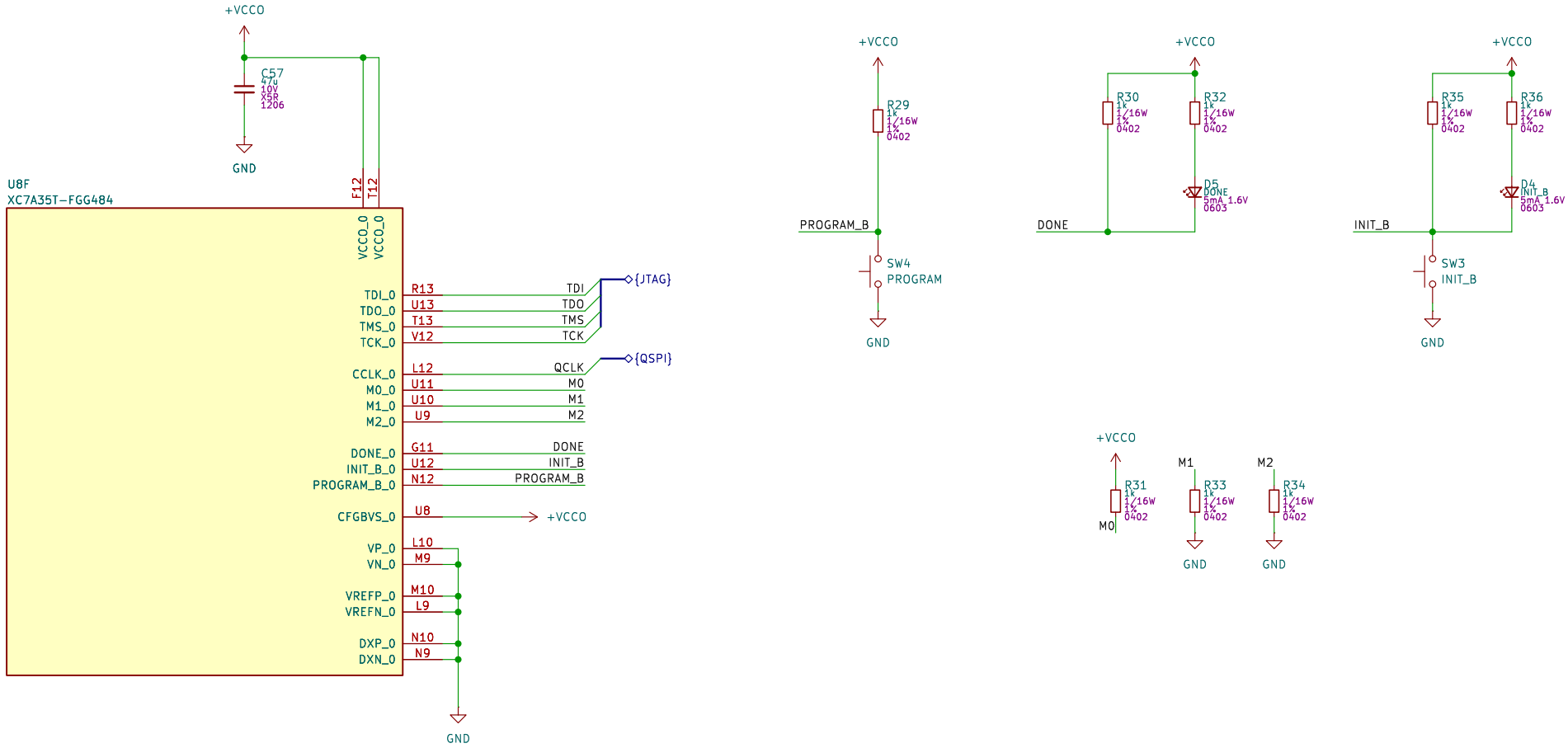
Notes:

UG483: Table 2-2: Required PCB Capacitor Quantities per Device: Artix-7 Devices
Page 16, row FGG484 XC7A35T
VCCO (all other Banks, per Bank): 1x47uF, 2x4.7uF, 4x0.47uF

UG483: Page 36 Power Supply Consolidation
Powering 1.8V VCCO, VCCAUX, and VCCAUX_IO from a common PCB plane is allowed in 7 series FPGA designs.

UG483: Page 36 Unconnected VCCO Pins
In some cases, one or more I/O banks in an FPGA are not used (for example, when an FPGA has far more I/O pins than the design requires). In these cases, it might be desirable to leave the bank's associated VCCO pins unconnected, as it can free up some PCB layout constraints

Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: Bank 15-16	Date: 2024-01-01	Page: 11/20
KiCad E.D.A. 8.0.0	File: FPGA_Bank15-16.kicad_sch	



Notes:

UG483: Table 2-2: Required PCB Capacitor Quantities per Device: Artix-7 Devices
Page 16, row FGG484 XC7A35T
VCCO (bank 0): 1x47uF

UG470: Page 28 Configuration Banks Voltage Select
CFGVBS pulled low for 1.8V or 1.5V JTAG operation

UG470 Page 7
The specific configuration mode is selected by setting the appropriate level on the dedicated mode input pins M[2:0]. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors (≤ 1 kΩ), or tied directly to ground or VCCO_0. The mode pins should not be toggled during
Table 2-1: 7 Series FPGA Configuration Modes
Configuration Mode – M[2:0]
Master SPI – 001
(ie, M2 low, M1 low, M0 high)

Notes:

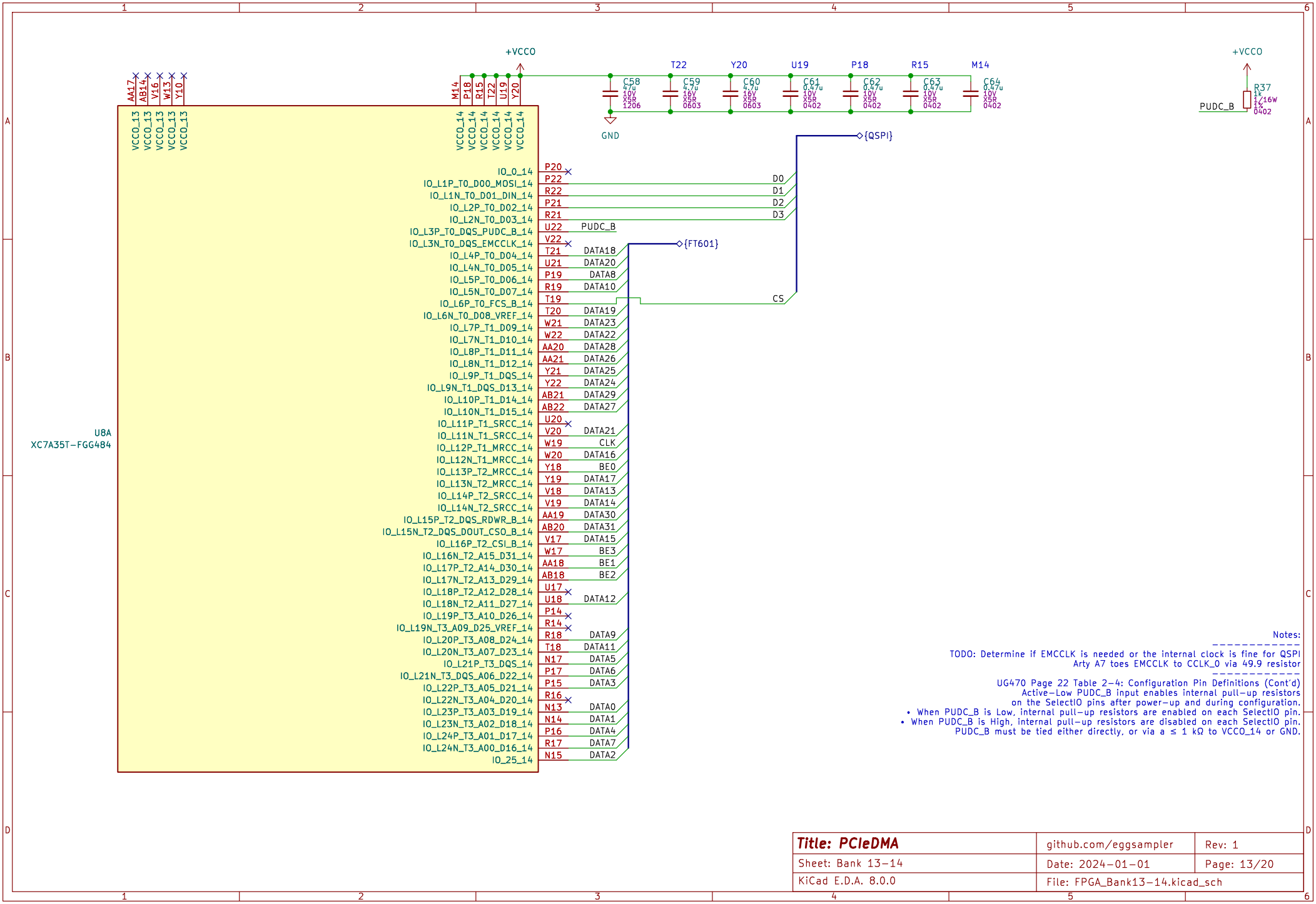
UG470 Page 21 Table 2-4: Configuration Pin Definitions (Cont'd)
Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to VCCO_0 to ensure a stable High input, and recommend push-button to GND to enable manual configuration reset.

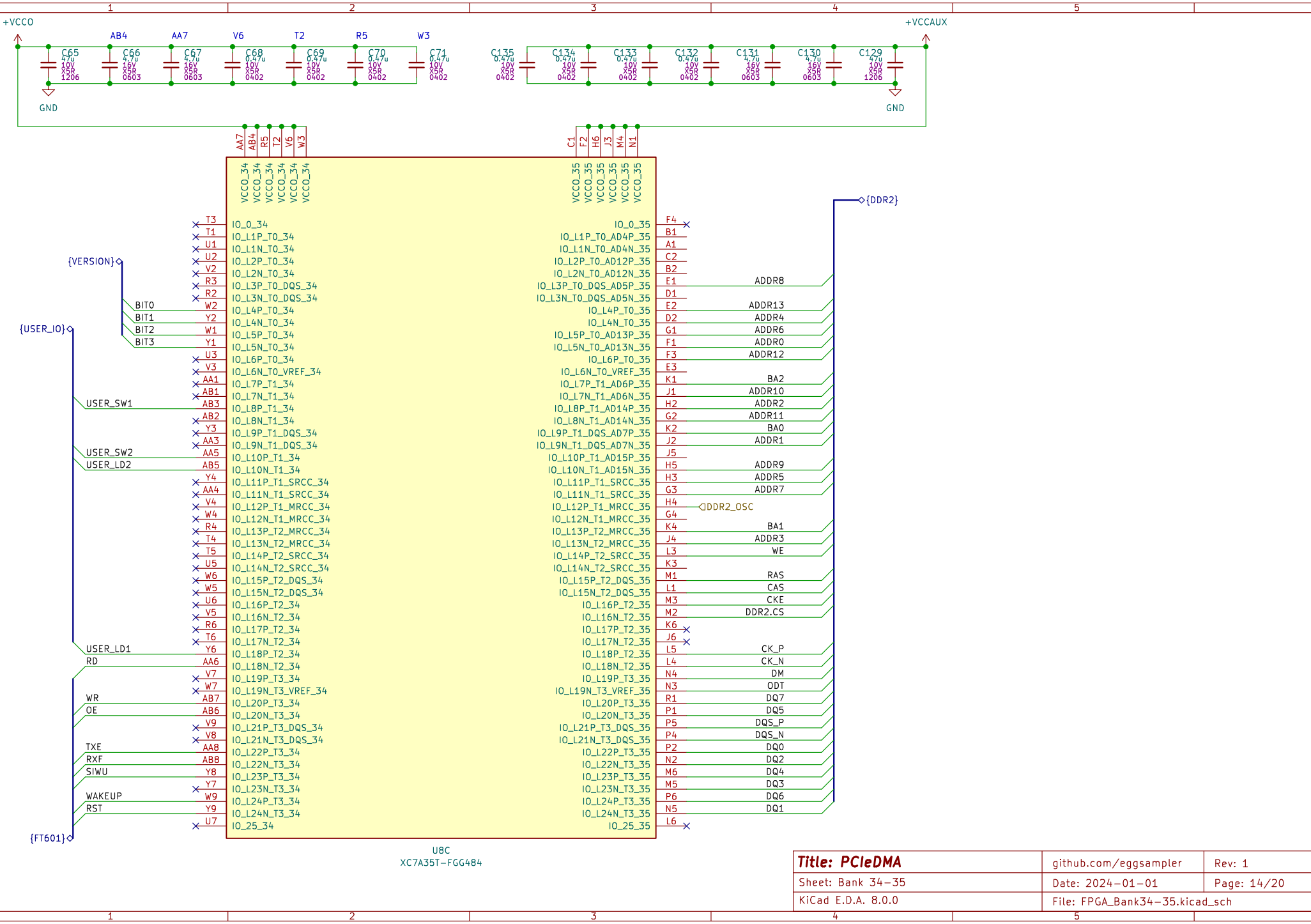
UG470 Page 21 Table 2-4: Configuration Pin Definitions (Cont'd)
INIT_B can externally be held Low during power-up to stall the power-on configuration sequence at the end of the initialization process.
Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to VCCO_0 to ensure clean Low-to-High transitions.

UG470 Page 22 Table 2-4: Configuration Pin Definitions (Cont'd)
A High signal on the DONE pin indicates completion of the configuration sequence.
The DONE output is an open-drain output by default.
Note: DONE has an internal pull-up resistor of approximately 10 kΩ.

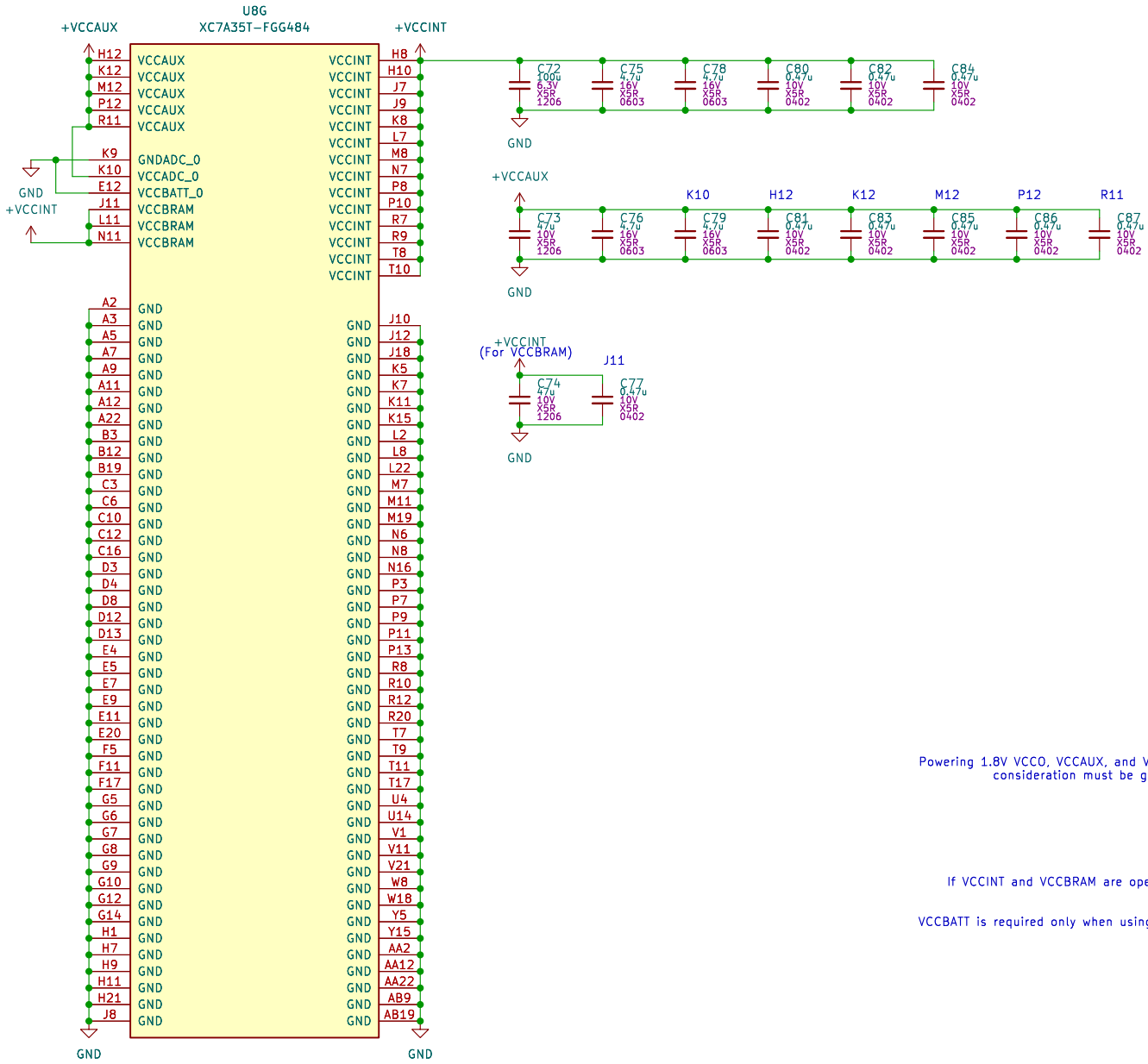
UG470 Page 15 Configuration Debugging
The two most important configuration signals, INIT_B and DONE, should be connected to LED drivers. The pulsing of INIT_B from Low to High indicates the completion of initialization at power-up.

Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: Bank 0	Date: 2024-01-01	Page: 12/20
KiCad E.D.A. 8.0.0	File: FPGA_Bank0.kicad_sch	


+VCCO
AA17
AB14
V16
W13
Y10
VCCO_13
M14
P18
R15
T22
U19
Y20
VCCO_14
C58 47u 10V X5R 1206
C59 4.7u 16V X5R 0603
C60 4.7u 16V X5R 0603
C61 0.47u 10V X5R 0402
C62 0.47u 10V X5R 0402
C63 0.47u 10V X5R 0402
C64 0.47u 10V X5R 0402
GND
+VCCO
R37 1k 1/16W 1% 0402
PUDC_B
{QSPI}
D0
D1
D2
D3
CS
{FT601}
U8A
XC7A35T-FGG484
IO_0_14
IO_L1P_T0_D00_MOSI_14
IO_L1N_T0_D01_DIN_14
IO_L2P_T0_D02_14
IO_L2N_T0_D03_14
IO_L3P_T0_DQS_PUDC_B_14
IO_L3N_T0_DQS_EMCCLK_14
IO_L4P_T0_D04_14
IO_L4N_T0_D05_14
IO_L5P_T0_D06_14
IO_L5N_T0_D07_14
IO_L6P_T0_FCS_B_14
IO_L6N_T0_D08_VREF_14
IO_L7P_T1_D09_14
IO_L7N_T1_D10_14
IO_L8P_T1_D11_14
IO_L8N_T1_D12_14
IO_L9P_T1_DQS_14
IO_L9N_T1_DQS_D13_14
IO_L10P_T1_D14_14
IO_L10N_T1_D15_14
IO_L11P_T1_SRCC_14
IO_L11N_T1_SRCC_14
IO_L12P_T1_MRCC_14
IO_L12N_T1_MRCC_14
IO_L13P_T2_MRCC_14
IO_L13N_T2_MRCC_14
IO_L14P_T2_SRCC_14
IO_L14N_T2_SRCC_14
IO_L15P_T2_DQS_RDWR_B_14
IO_L15N_T2_DQS_DOUT_CSO_B_14
IO_L16P_T2_CSI_B_14
IO_L16N_T2_A15_D31_14
IO_L17P_T2_A14_D30_14
IO_L17N_T2_A13_D29_14
IO_L18P_T2_A12_D28_14
IO_L18N_T2_A11_D27_14
IO_L19P_T3_A10_D26_14
IO_L19N_T3_A09_D25_VREF_14
IO_L20P_T3_A08_D24_14
IO_L20N_T3_A07_D23_14
IO_L21P_T3_DQS_14
IO_L21N_T3_DQS_A06_D22_14
IO_L22P_T3_A05_D21_14
IO_L22N_T3_A04_D20_14
IO_L23P_T3_A03_D19_14
IO_L23N_T3_A02_D18_14
IO_L24P_T3_A01_D17_14
IO_L24N_T3_A00_D16_14
IO_25_14
P20
P22
R22
P21
R21
U22
V22
T21
U21
P19
R19
T19
T20
W21
W22
AA20
AA21
Y21
Y22
AB21
AB22
U20
V20
W19
W20
Y18
Y19
V18
V19
AA19
AB20
V17
W17
AA18
AB18
U17
U18
P14
R14
R18
T18
N17
P17
P15
R16
N13
N14
P16
R17
N15
PUDC_B
DATA18
DATA20
DATA8
DATA10
DATA19
DATA23
DATA22
DATA28
DATA26
DATA25
DATA24
DATA29
DATA27
DATA21
CLK
DATA16
BE0
DATA17
DATA13
DATA14
DATA30
DATA31
DATA15
BE3
BE1
BE2
DATA12
DATA9
DATA11
DATA5
DATA6
DATA3
DATA0
DATA1
DATA4
DATA7
DATA2
Notes:
TODO: Determine if EMCCLK is needed or the internal clock is fine for QSPI
Arty A7 toes EMCCLK to CCLK_0 via 49.9 resistor
UG470 Page 22 Table 2-4: Configuration Pin Definitions (Cont'd)
Active-Low PUDC_B input enables internal pull-up resistors
on the SelectIO pins after power-up and during configuration.
• When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin.
• When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin.
PUDC_B must be tied either directly, or via a ≤ 1 kΩ to VCCO_14 or GND.
Title: PCIeDMA
github.com/eggsampler
Rev: 1
Sheet: Bank 13-14
Date: 2024-01-01
Page: 13/20
KiCad E.D.A. 8.0.0
File: FPGA_Bank13-14.kicad_sch



Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: Bank 34-35	Date: 2024-01-01	Page: 14/20
KiCad E.D.A. 8.0.0	File: FPGA_Bank34-35.kicad_sch	



Notes:

UG483: Table 2-2: Required PCB Capacitor Quantities per Device: Artix-7 Devices
Page 16, row FGG484 XC7A35T
VCCINT: 1x100uF, 2x4.7uF, 3x0.47uF
VCCBRAM: 1x47uF, 1x0.47uF
VCCAUX: 1x47uF, 2x4.7uF, 5x0.47uF

UG483: Page 19: Table 2-5: PCB Capacitor Specifications
100uF: < 1210, Ceramic X7R or X5R, 1nH ESL Max, 5mΩ < ESR < 40mΩ, > 2.5V
47uF: < 1210, Ceramic X7R or X5R, 1nH ESL Max, 5mΩ < ESR < 40mΩ, > 6.3V
4.7uF: < 0805, Ceramic X7R or X5R, 1nH ESL Max, 5mΩ < ESR < 20mΩ, > 6.3V
0.47uF: < 0603, Ceramic X7R or X5R, 0.5nH ESL Max, 5mΩ < ESR < 20mΩ, > 6.3V

UG483: Page 36 Power Supply Consolidation
Powering 1.8V VCCO, VCCAUX, and VCCAUX_IO from a common PCB plane is allowed in 7 series FPGA designs. However, careful consideration must be given to power supply noise-in particular, any noise on the VCCO rail should not violate the recommended operating condition range for the VCCAUX supply.

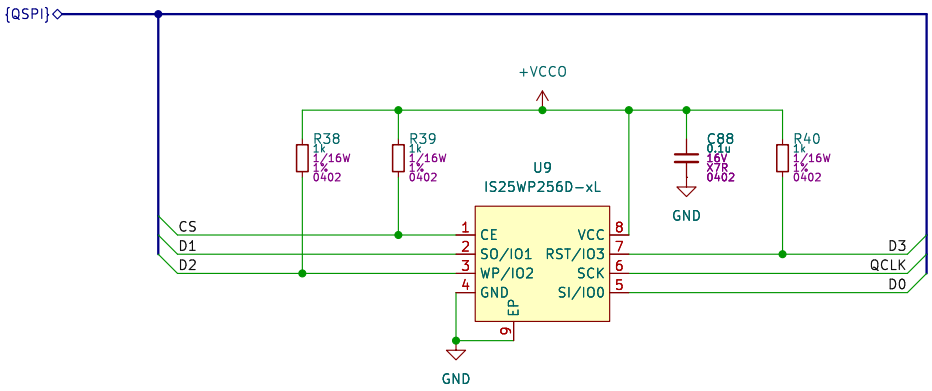
DS181: Page 2 Table 2: Recommended Operating Conditions
VCCAUX Min 1.71, Typ 1.8, Max 1.89
(so +/- 5%)

DS181: Page 3, Note 3
If VCCINT and VCCBRAM are operating at the same voltage, VCCINT and VCCBRAM should be connected to the same supply.

DS181 Page 3,
VCCBATT is required only when using bitstream encryption. If battery is not used, connect VCCBATT to either ground or VCCAUX.

TODO: Confirm if VCCADC tied to VCCAUX if unused is fine

Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: Bank VCC	Date: 2024-01-01	Page: 15/20
KiCad E.D.A. 8.0.0	File: FPGA_BankVCC.kicad_sch	

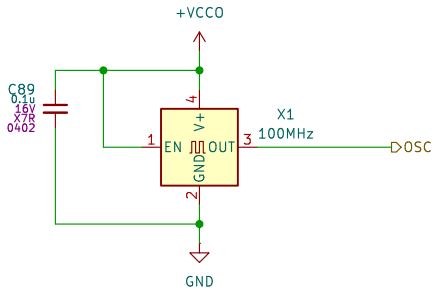


Notes:

Datasheet Rev.A 06/29/2017 Page 9
The Chip Enable (CE#) pin enables and disables the devices operation.
When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the devices non-critical internal circuitry power down to allow minimal levels of power consumption while in a standby state

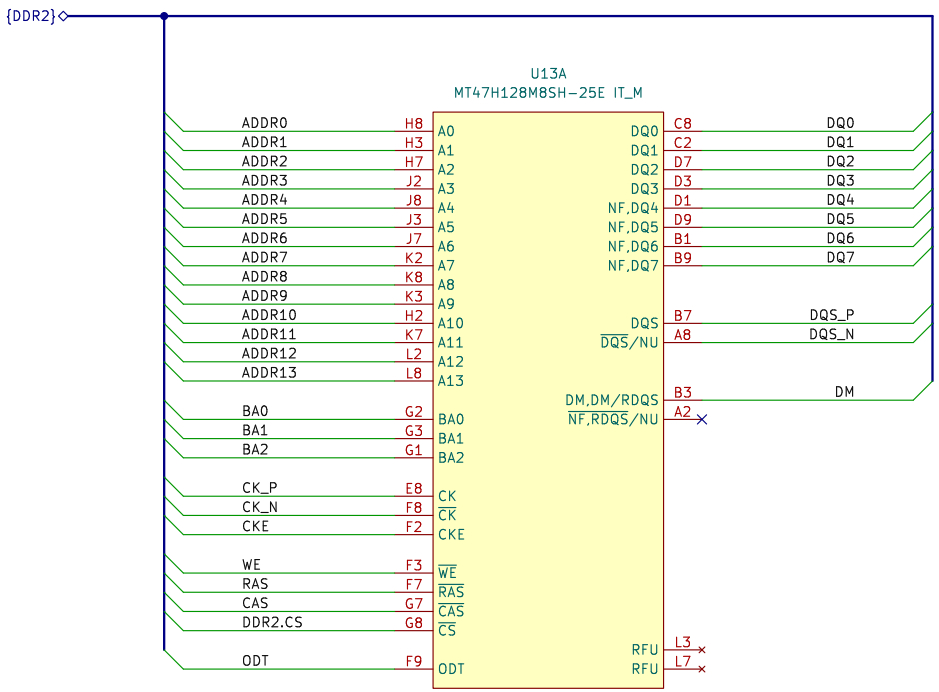
Datasheet Rev.A 06/29/2017 Page 166
9.8 POWER-UP AND POWER-DOWN
At Power-up and Power-down, the device must be NOT SELECTED until Vcc reaches at the right level.
(Adding a simple pull-up resistor on CE# is recommended.)
(also added pullups on dual mode pins)
TODO: is 1k pullup too strong?

Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: Flash	Date: 2024-01-01	Page: 16/20
KiCad E.D.A. 8.0.0	File: Flash.kicad_sch	

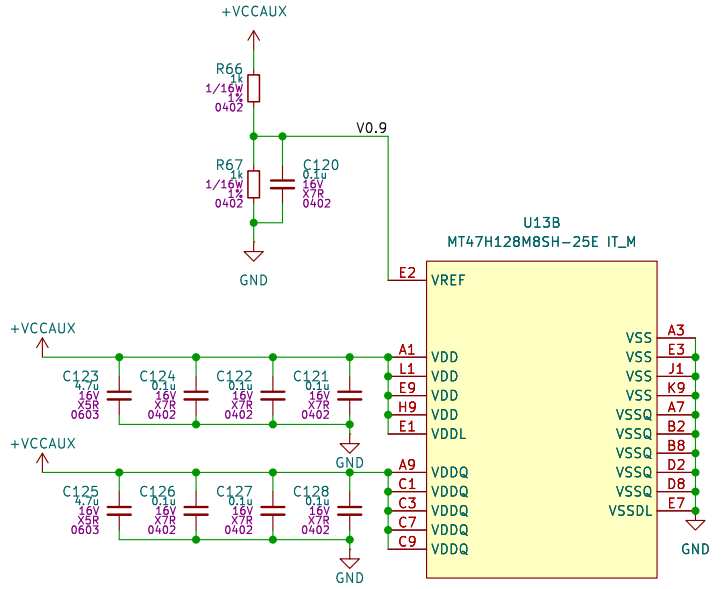


Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: Oscillator	Date: 2024-01-01	Page: 17/20
KiCad E.D.A. 8.0.0	File: Oscillator.kicad_sch	

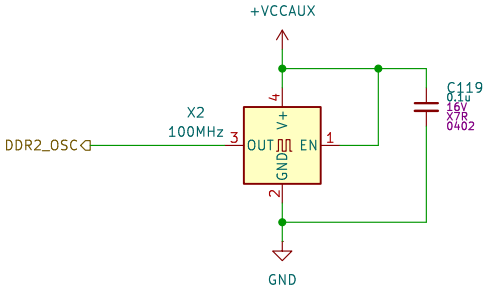
DDR2 Memory Lines



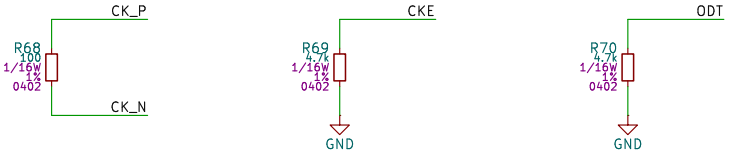
DDR2 Memory Power



DDR2 Memory Clock

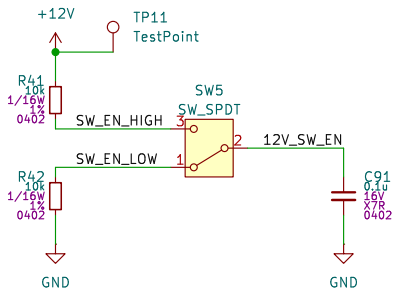


Termination & Pull-downs



Title: PCIeDMA	github.com/eggsampler	Rev: 1
Sheet: Memory	Date: 2024-01-01	Page: 18/20
KiCad E.D.A. 8.0.0	File: Memory.kicad_sch	

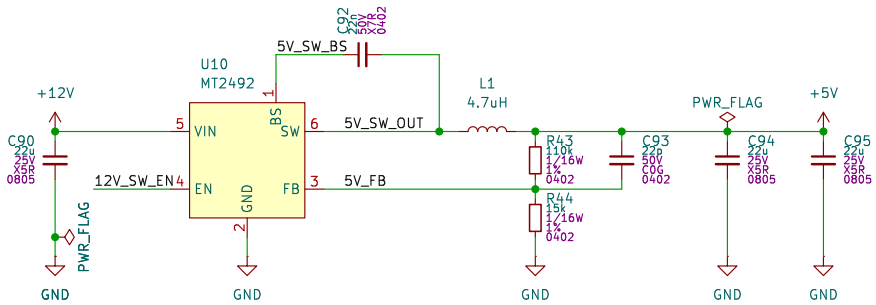
Main Power Switch



Notes:

Switch enables/disables 5v supply for rest of the board
FPGA voltages derived from this 5v
TODO: should there be another switch for this?
Maybe an input for the FPGA?

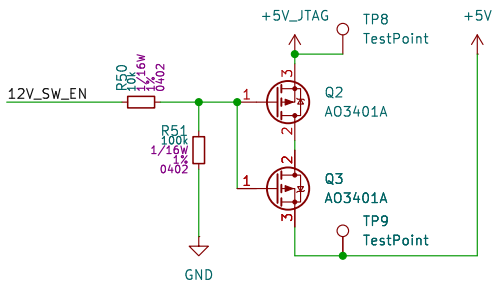
PCIe 12v to 5v Supply



Notes:

From typical application on MT2492 V2.1

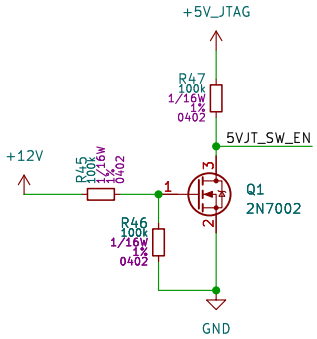
JTAG 5v Power Select



Notes:

This should allow the board 5v to be powered from the jtag supply if the 12v isn't present ie card not plugged in, or the switch is off, and provide some reverse polarity protection.
TODO: Size some mosfets, maybe dual package so8?

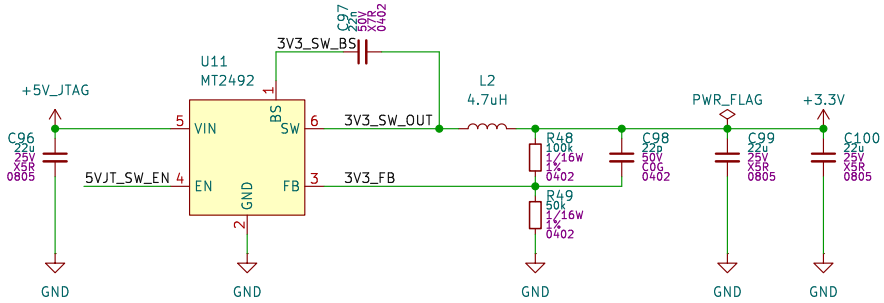
JTAG 3v3 Power Enable



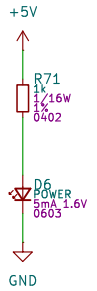
Notes:

This will enable the 3v3 JTAG peripheral supply if the card is not powered or plugged in.
Otherwise if powered and plugged in, the 3v3 supply from the PCIe bus is used.

JTAG 3v3 Power Supply



Power LED



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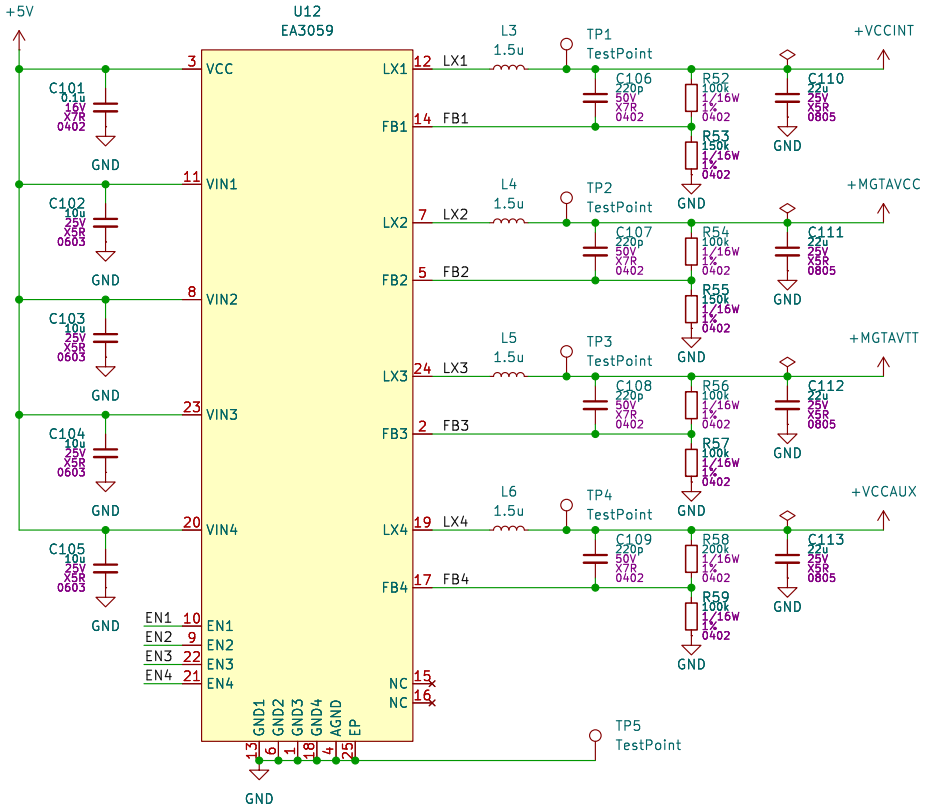
FPGA Power Supply



Notes:

Input voltages
PCIe: 12V, 3.3V, 3.3V_aux
USB: 5V

Output voltages
VCCO: 3.3V
VCCINT: 1.0V
VCCBRAM: Use VCCINT
VCCAUX: 1.8V
MGTAVCC: 1.0V
MGTAVTT: 1.2V
5V: Leds
3.3V: FT601, CH347

V_OUT=0.6 * R1/R2 + 0.6
1.0=0.6*(100/150)+0.6
1.2=0.6*(100/100)+0.6
1.8=0.6*(200/100)+0.6

General concept is to power everything from the pcie 12v -> 5v buck if possible,
physical switch on that 5v line to turn fpga off

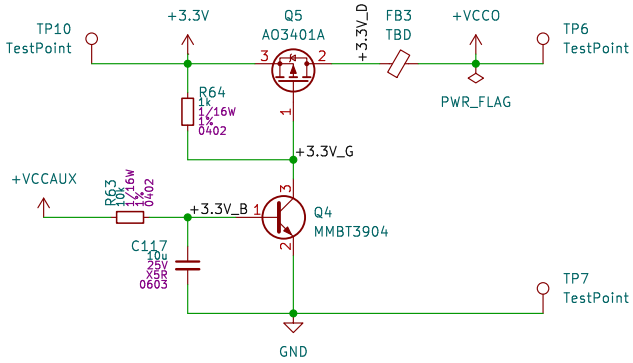
Notes:

DS181 Page 8 Power-On/Off Power Supply Sequencing
The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on.

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers
is VCCINT, VMGTAVCC, VMGTAVTT OR VMGTAVCC, VCCINT, VMGTAVTT.
Both VMGTAVCC and VCCINT can be ramped simultaneously.

VCCINT (& VCCBRAM) & VMGTAVCC -> VMGTAVTT & VCCAUX -> VCCO

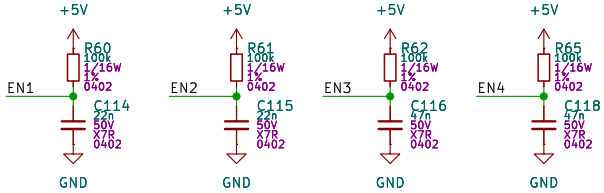
VCCO Power Sequence



Notes:

This circuit powers VCCO after VCCAUX is up
10kOhm * 10uF = a few 10s of ms until the npn conducts
Ferrite bead for filtering
TODO: Consider filter specifically for pcie 3v3 ripple

FPGA Power Sequence



Notes:

Min ramp time for all supplies on FPGA is 0.2ms (DS181 Table 7)

EA3059 datasheet gives values 100k and 10n to 100n for power sequencing on EN pins
and a minimum voltage for Enable Pin Input High Voltage of 2V

At 100kR at 22nF,
2=5(1-e^(-t/((100*10^3)*(22*10^-9))))
gives a time of approx 0.0011238, or 1.1238ms

At 100kR and 47nF
2=5(1-e^(-t/((100*10^3)*(47*10^-9))))
gives a time of approx 0.0024009, or 2.4009ms

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KiCad E.D.A. 8.0.0	File: PowerFPGA.kicad_sch	