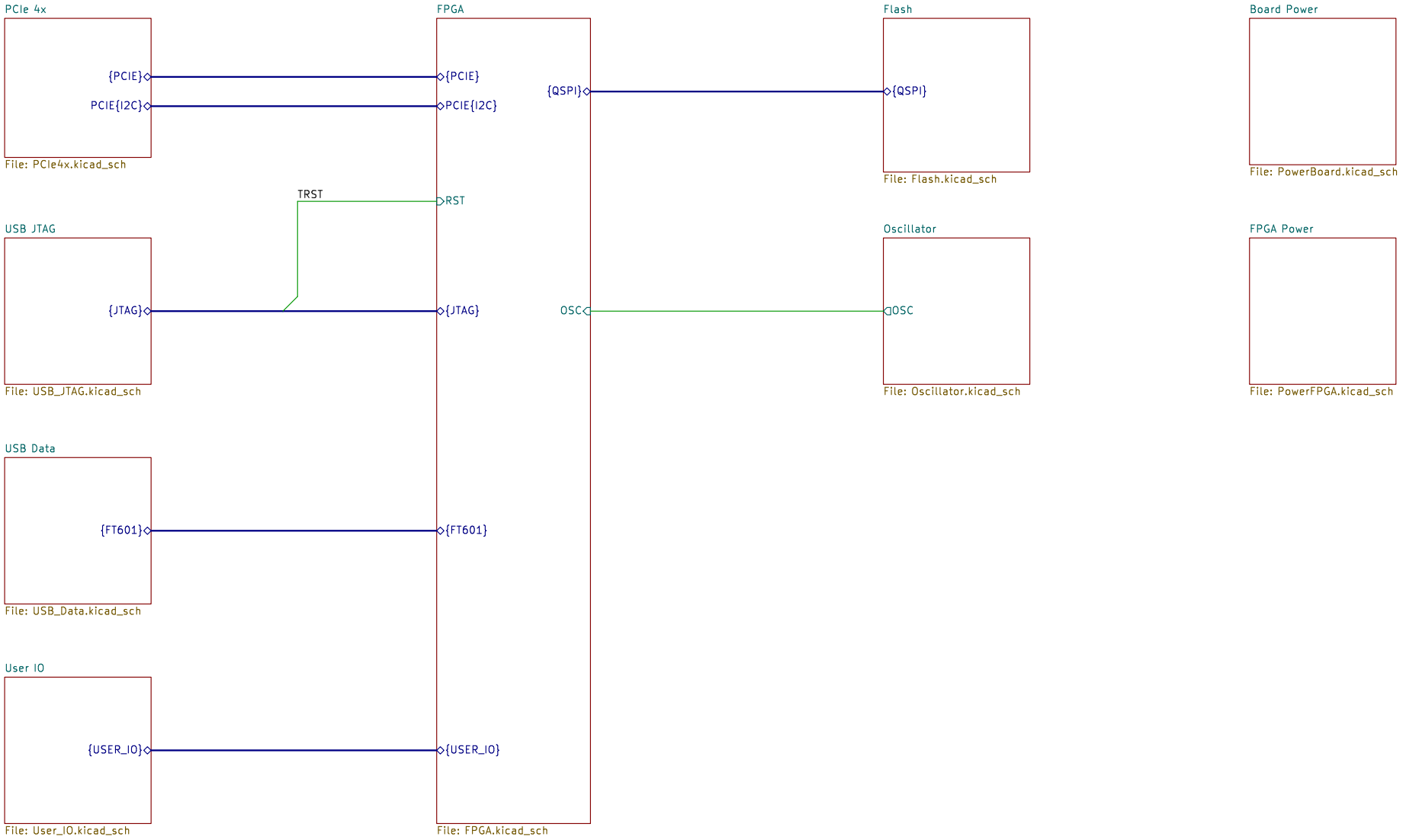
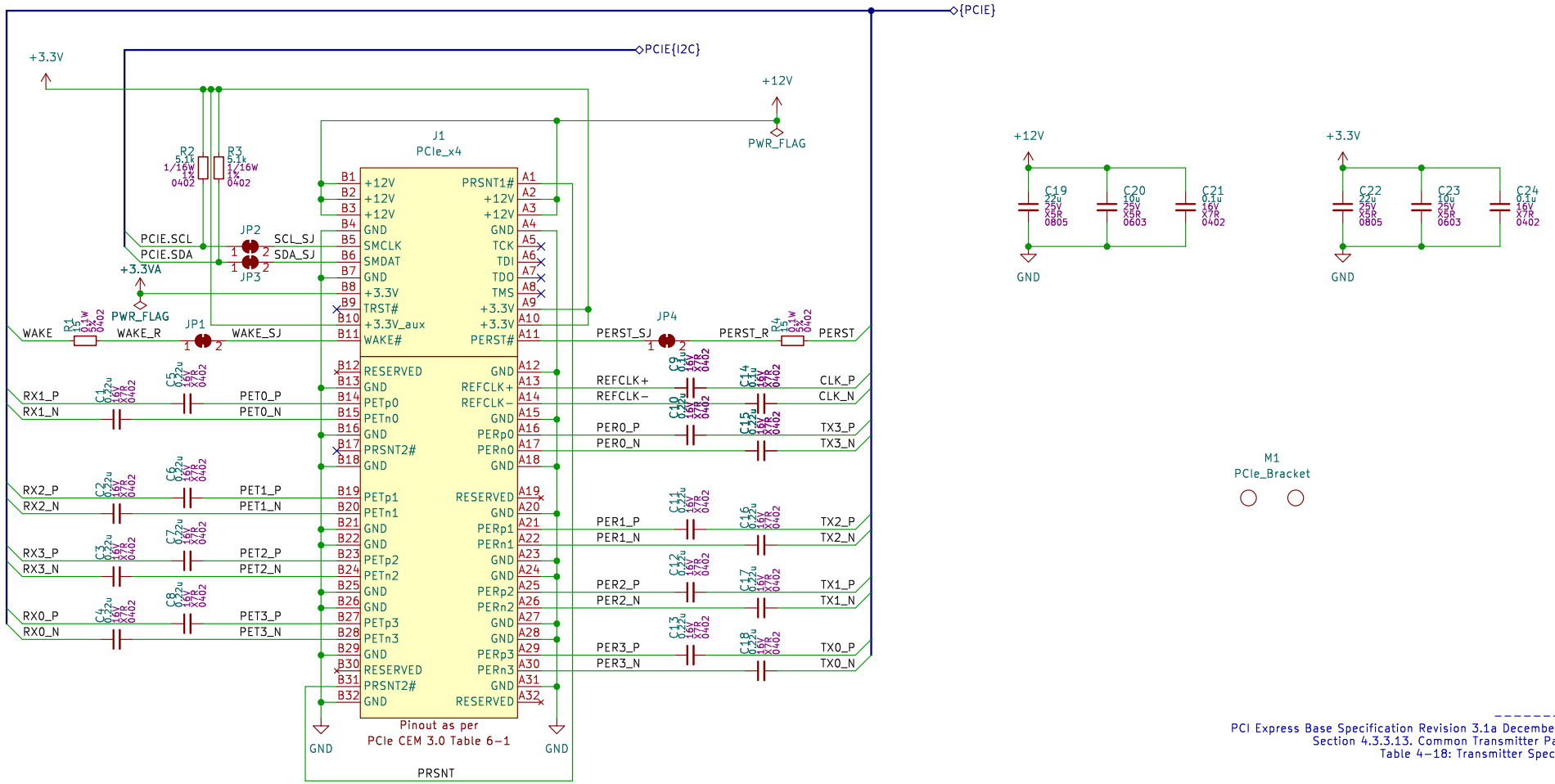



| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: | File: PCIeDMA.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 1/19 |




Notes:

PCI Express Base Specification Revision 3.1a December 7 2015,
Section 4.3.3.13. Common Transmitter Parameters
Table 4−18: Transmitter Specifications
Page 376

Lists AC Coupling Capacitor values of 75−265nF for 2.5GT/s, 75−265nF for 5.0 GT/s and 176 to 265nF for 8 GT/s
Note 14: All platforms that have transmitters supporting 8.0 GT/s must implement the 176−265 nF CTX value.
Platforms operating at 2.5 or 5.0 GT/s only may implement over a range of 75 to 265 nF.

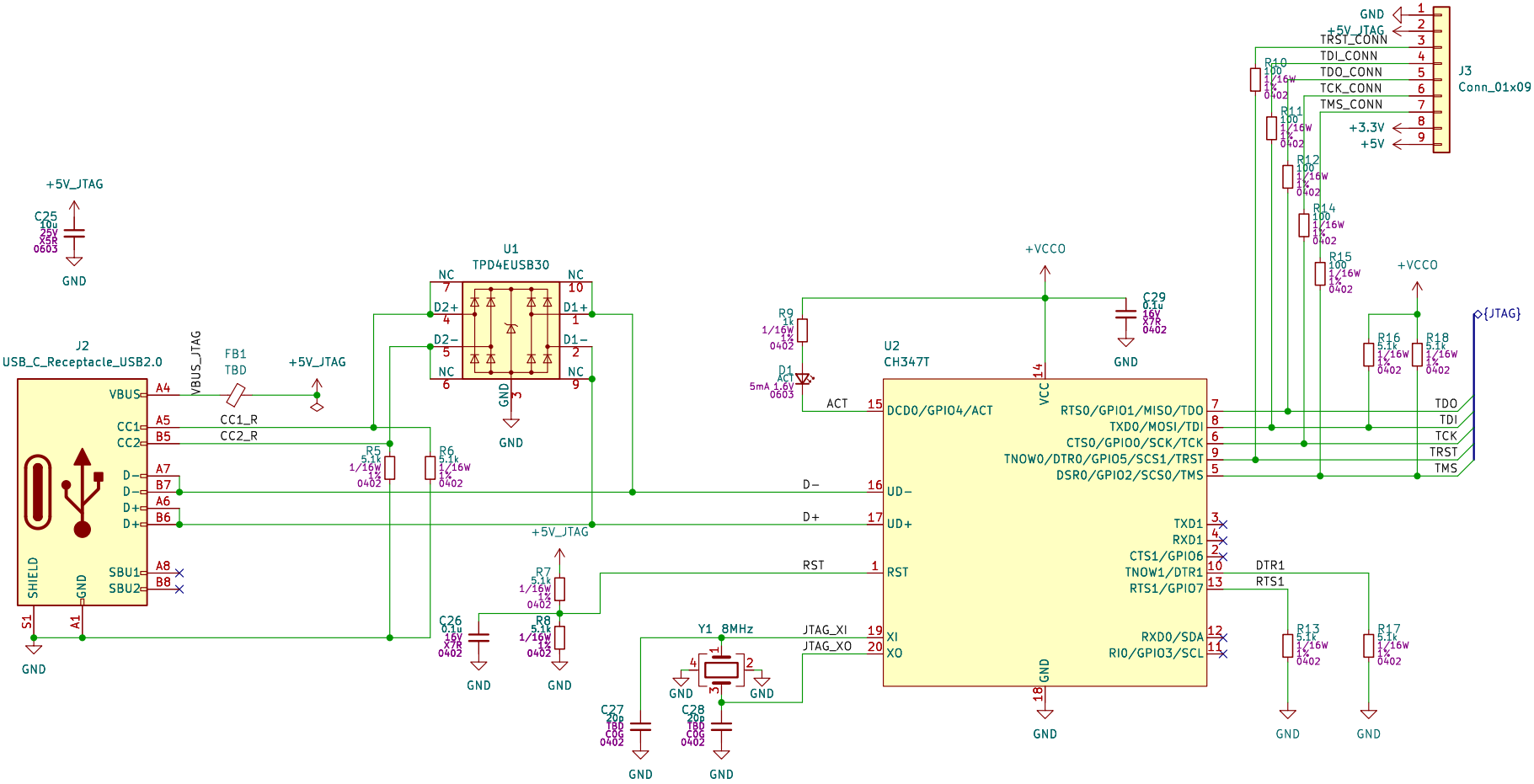
The REFCLK coupling is not a PCIe spec, but a Xilinx recommendation. 100nF for LVDS
(even though the REFCLK is HSCL).
AC701 uses 10nF caps, shouldn't matter too much.

PCI Express Card Electromechanical Specification Revision 3.0 July 21, 2013
Section 3.2. Presence Detect
Page 41
tldr used for hotplugging and isolation, connect PRSNT1# to longest supported PRSNT2# pin

PCIe 3.3V supply is used, but electromechanical spec table 4−1 page 44 gives +/− 9% which is a little too close to
Artix−7 DS181 absolute max V_CCO of 3.6V (and above recommended max of 3.465V)

Solder jumpers on SMBUS, WAKE and PERST lines for detection/customisation purposes

| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: PCIe 4x | File: PCIe4x.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023−02−14 | Id: 2/19 |

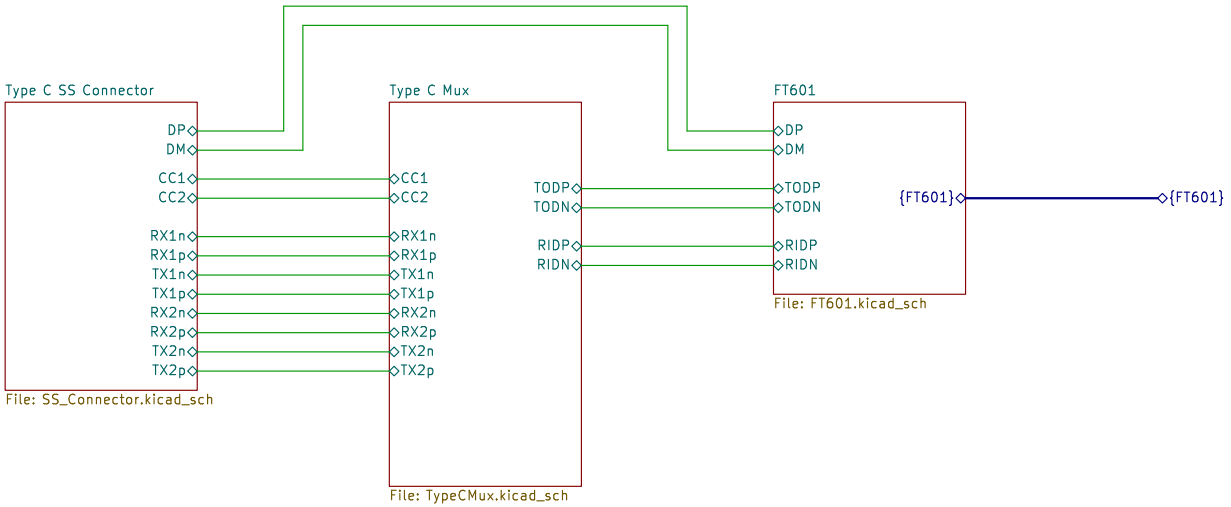



Notes:

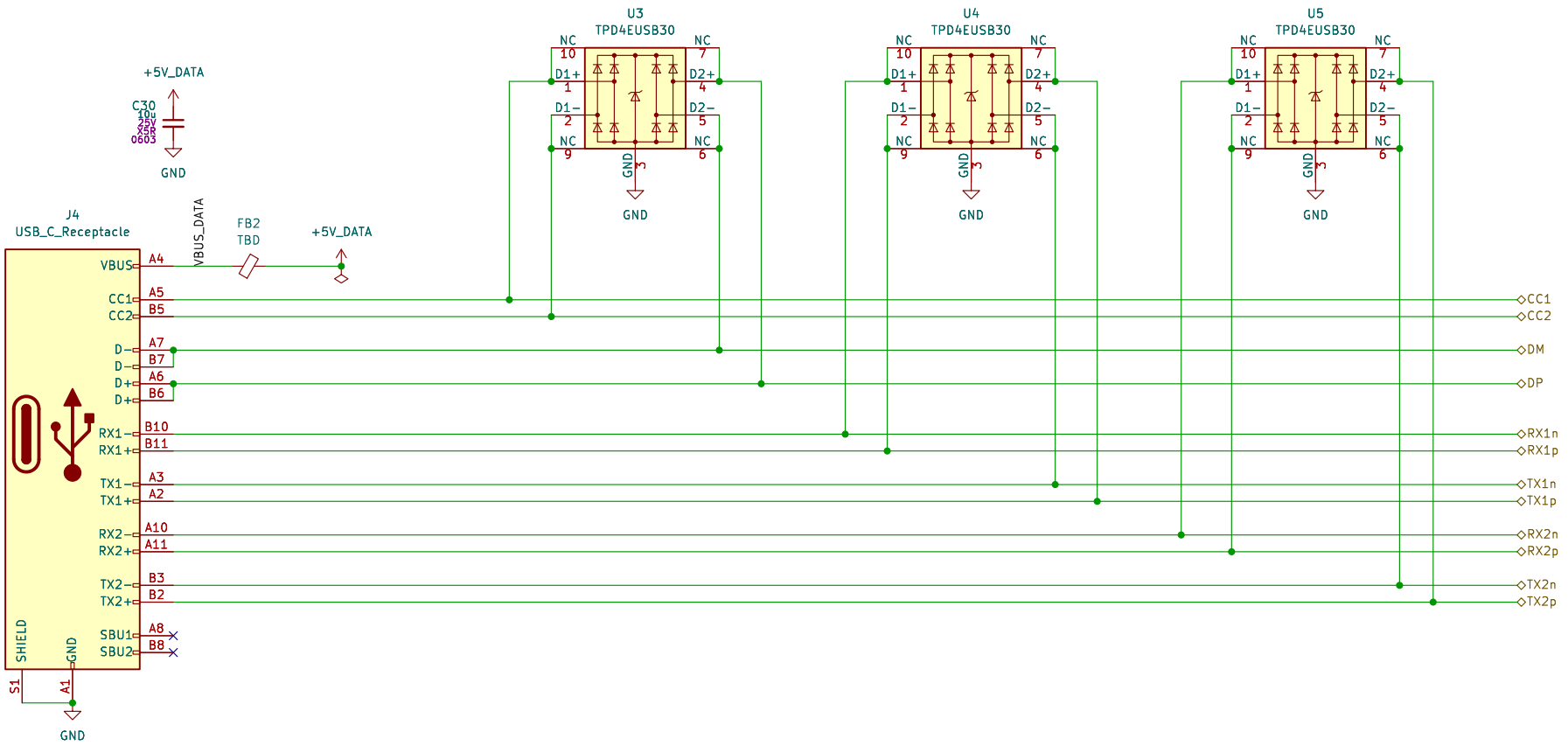
TODO: Calculate crystal load capacitors based on crystal part selection

RST pin pulled to 2.5V above VIH3 of 2.0V when +5V_JTAG USB is connected via voltage divider. Pulled low by divider when no +5_JTAG

| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: USB JTAG | File: USB_JTAG.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 3/19 |




| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: USB Data | File: USB_Data.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 4/19 |

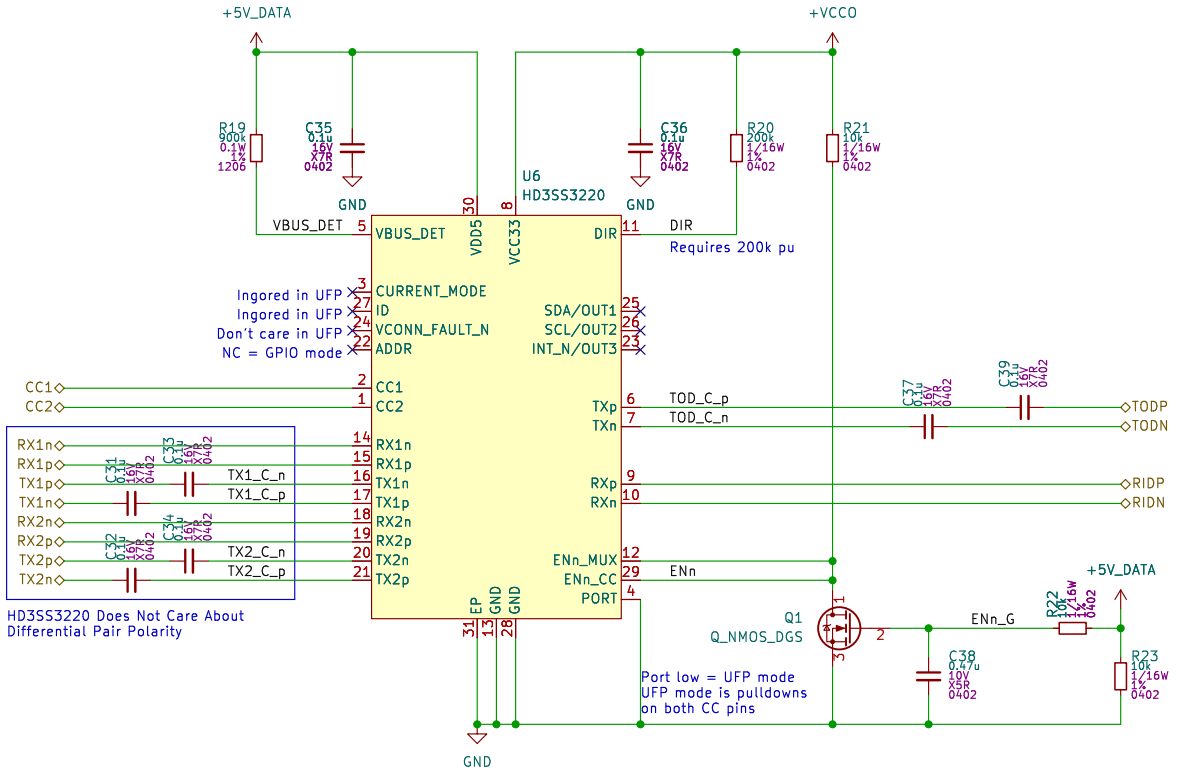



Notes:

+5V_Data is used for the mux and FT601

TPD4EUSB30 is used instead of a single part to simplify the BOM, as this can be used for the jtag interface too.

| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: Type C SS Connector | File: SS_Connector.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 5/19 |




Notes:

7.3.12 VDD5 and VCC33 Power–On Requirements

The HD3SS3220 has two power supplies: VDD5 and VCC33. The VDD5 supply powers the internal CC controller and also provides VCONN to either CC1 or CC2. The VCC33 powers the 2:1 MUX.

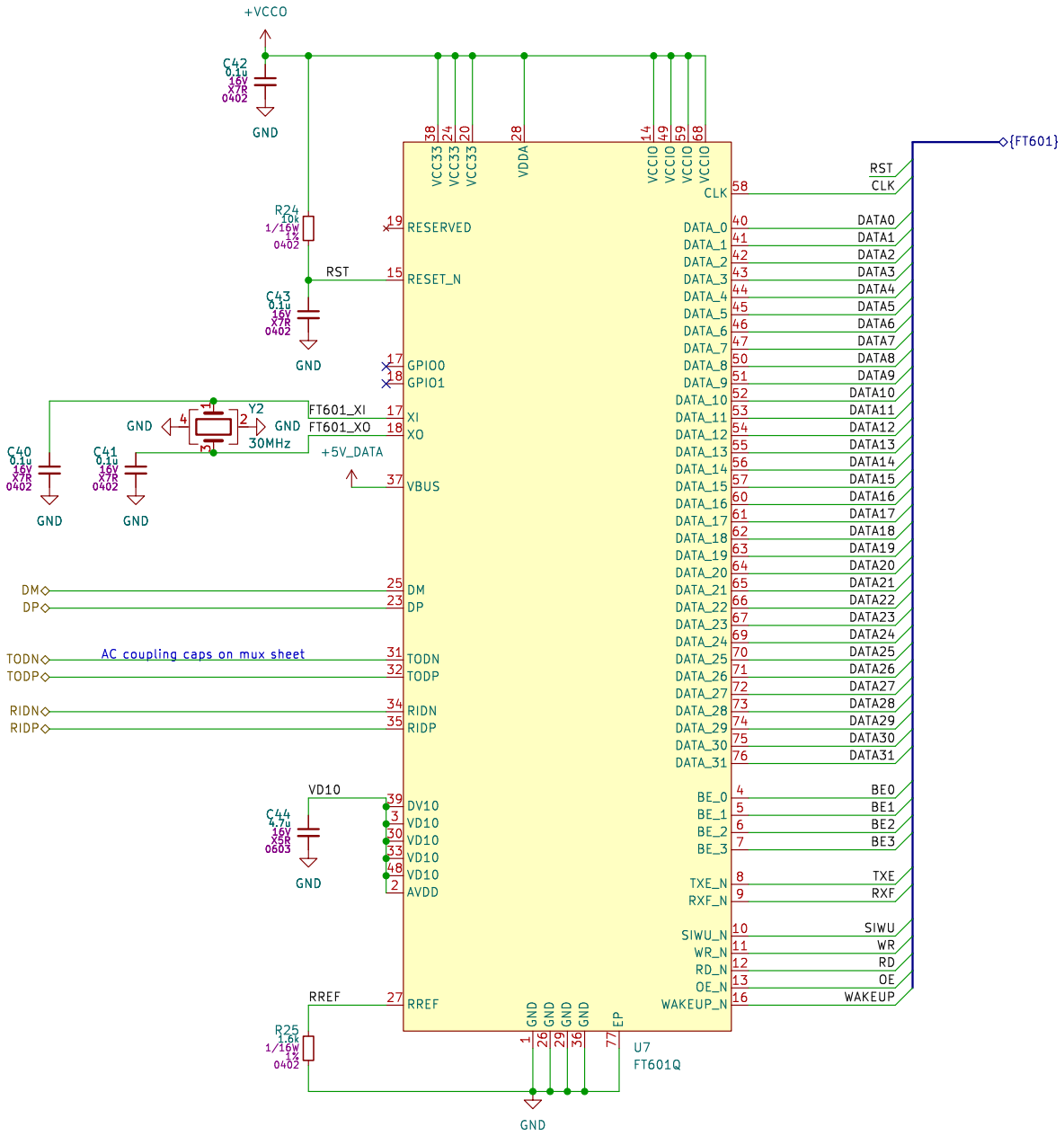
The HD3SS3220 non–failsafe pins are the following: PORT, ADDR, SDA/OUT1, SCL/OUT2, INT_IN/OUT3, VCONN_FAULT_N, and DIR. If any of these non–failsafe pins are pulled–up to a supply other than VDD5, then VDD5 supply must be powered up before the VCC33 supply. If it is not possible to power up VDD5 before VCC33, then the ENn_CC pin must be held high while both supplies are ramping and then asserted low after both supplies are stable

3.3v should always be on first when plugged into pcie slot and not plugged into usb
nmos will hold the pin high to 3.3v until turned off by 5v data
t_ENnCC_HI = 2ms
ENn_CC VIH = VDD5–0.3
10k * 0.47u should give about 10ms to 4.5v

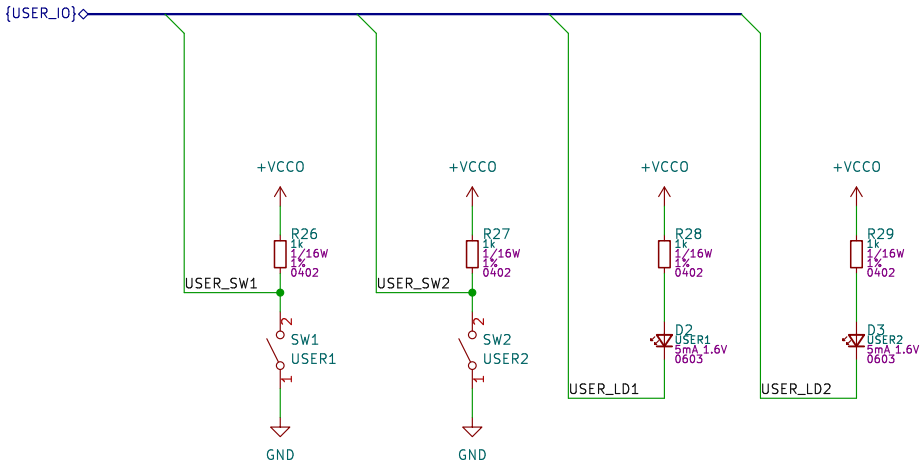
Notes:

Schematic based on datasheet 8.2.4 UFP port

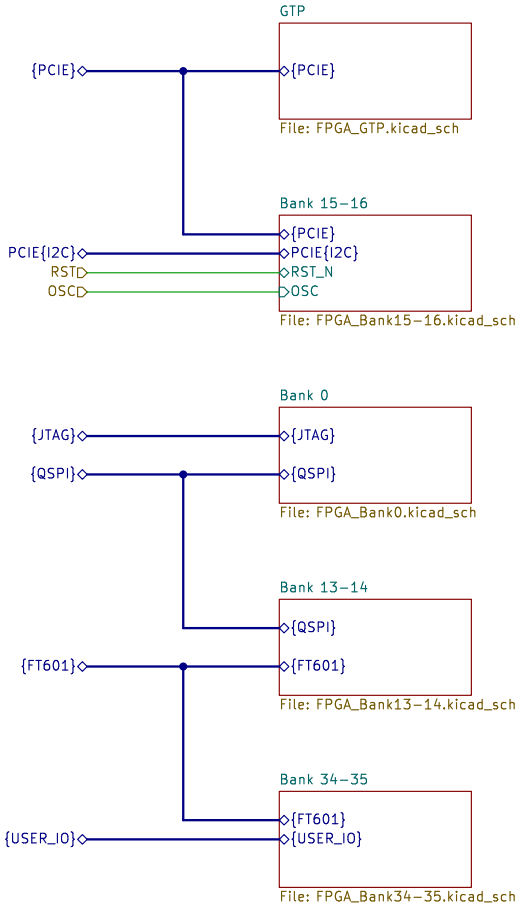
| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: Type C Mux | File: TypeCMux.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023–02–14 | Id: 6/19 |

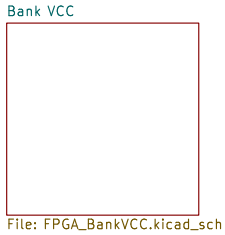



| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: FT601 | File: FT601.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 7/19 |

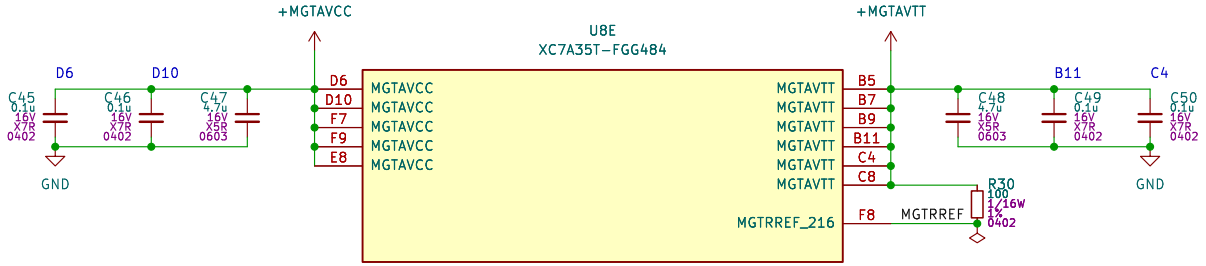


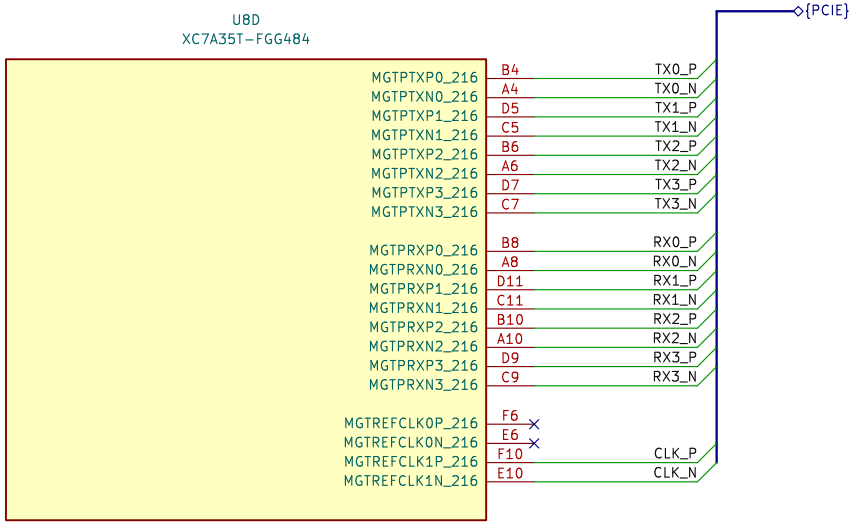

| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: User IO | File: User_IO.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 8/19 |




| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: FPGA | File: FPGA.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023–02–14 | Id: 9/19 |




Notes:

DS181 Page 2, Table 2: Recommended Operating Conditions
VMGTAVCC: Typical 1.0V
VMGTAVTT: Typical 1.2V

UG482 Table 5-14: MGTRREF – Connect to a 100Ω resistor that is also connected to MGTAVTT
Termination Resistor Calibration Circuit: The MGTRREF pin should be connected to the MGTAVTT supply through a 100Ω precision external resistor.

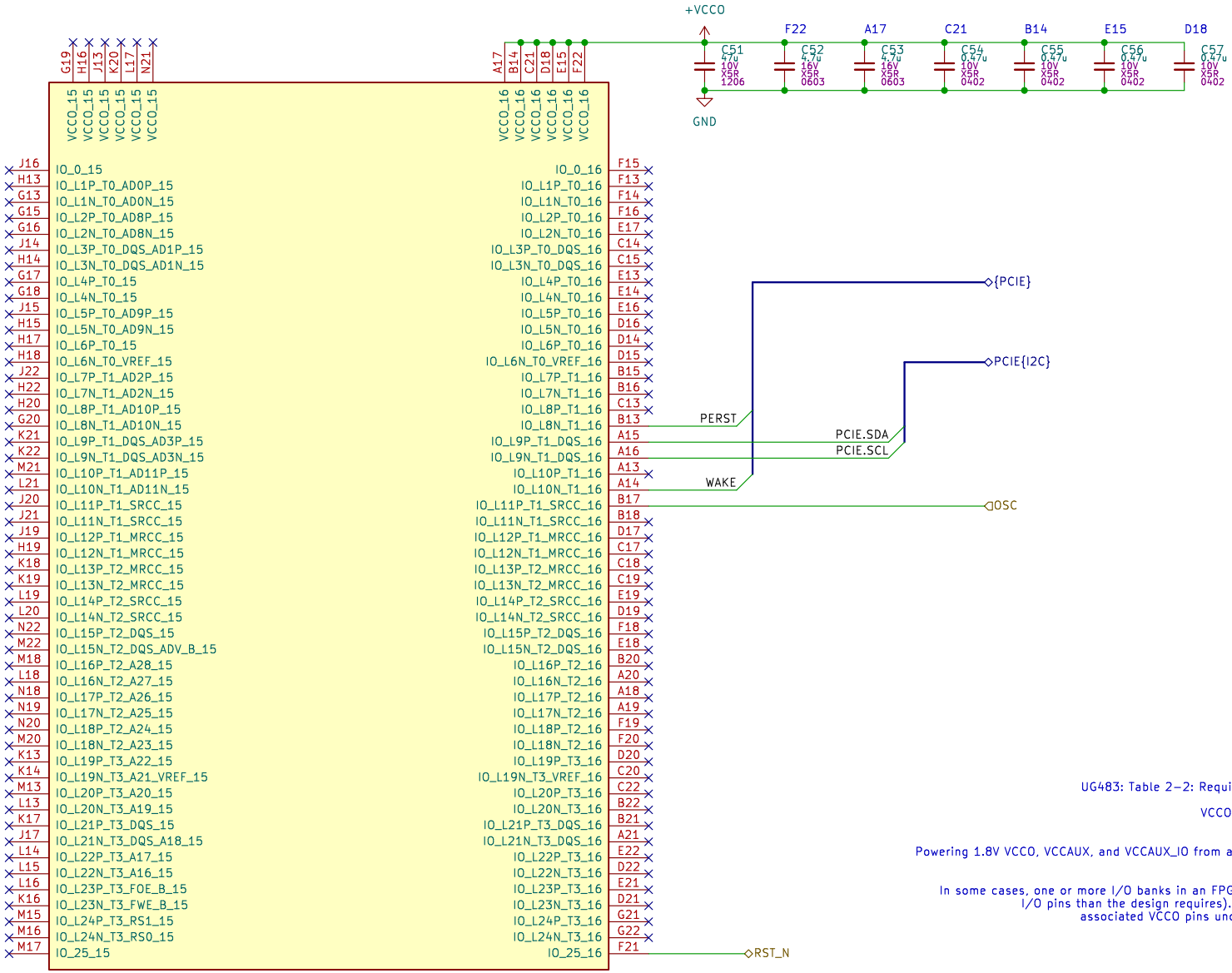
UG482: Unused Reference Clocks
It is recommended to leave the unused differential input pin clock pair floating (both MGTREFCLKP and MGTREFCLKN)

UG482: Power Supply Decoupling Capacitors
One 4.7uF 10% Ceramic capacitor per MGTAVCC group
Two 0.1uF 10% Ceramic capacitor per MGTAVTT power supply group
The larger 4.7 µF capacitors should be placed in close proximity and outside the perimeter of the FPGA pin field.
The 0.1µF capacitors on the other hand must be placed as close to the GTP Quad power supply pins as possible.
(See this section for 0.1uF capacitor pin placement)

UG482 Page 236
(For both MGTAVCC_G[N] and MGTAVTT_G[N])
The power supply regulator for this voltage should not be shared with non-transceiver loads.

AC coupling capacitors for RX and TX differential pairs are on PCIe connector sheet

| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: GTP | File: FPGA_GTP.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 10/19 |



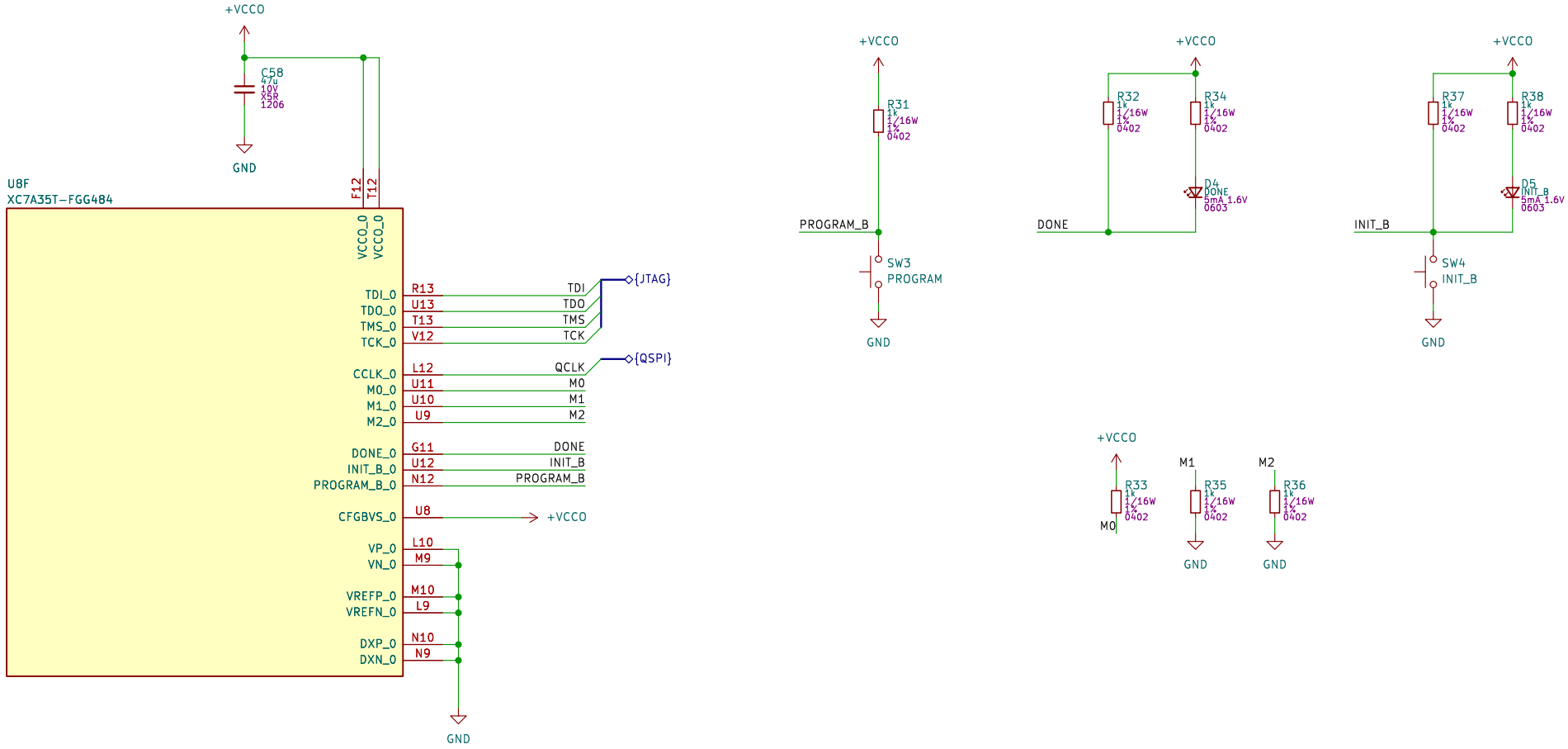

Notes:

UG483: Table 2-2: Required PCB Capacitor Quantities per Device: Artix-7 Devices
Page 16, row FGG484 XC7A35T
VCCO (all other Banks, per Bank): 1x47uF, 2x4.7uF, 4x0.47uF

UG483: Page 36 Power Supply Consolidation
Powering 1.8V VCCO, VCCAUX, and VCCAUX_IO from a common PCB plane is allowed in 7 series FPGA designs.

UG483: Page 36 Unconnected VCCO Pins
In some cases, one or more I/O banks in an FPGA are not used (for example, when an FPGA has far more I/O pins than the design requires). In these cases, it might be desirable to leave the bank's associated VCCO pins unconnected, as it can free up some PCB layout constraints

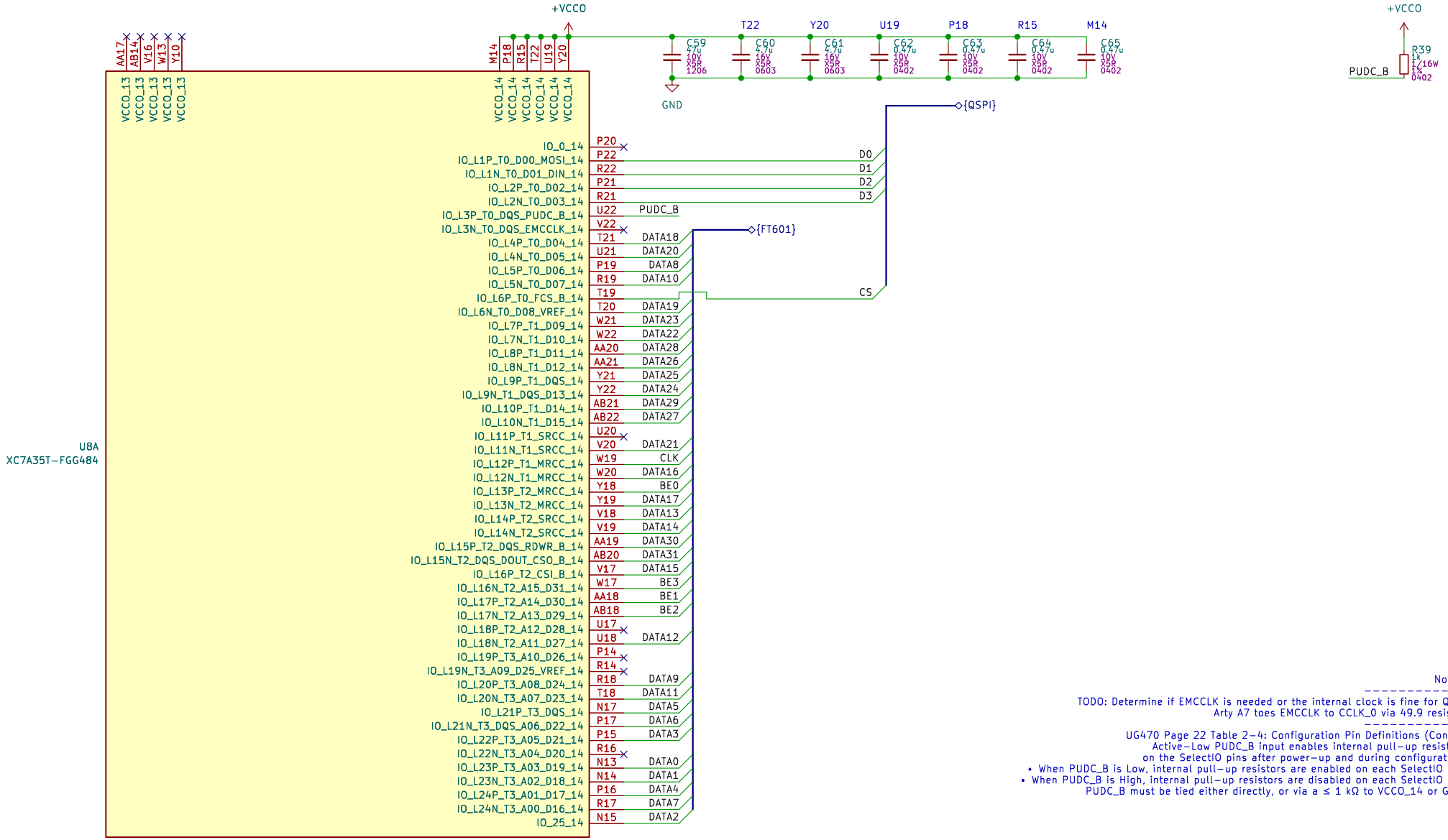
| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: Bank 15-16 | File: FPGA_Bank15-16.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 11/19 |




Notes:
---
UG483: Table 2-2: Required PCB Capacitor Quantities per Device: Artix-7 Devices
Page 16, row FGG484 XC7A35T
VCCO (bank 0): 1x47uF
---
UG470: Page 28 Configuration Banks Voltage Select
CFGVBS pulled low for 1.8V or 1.5V JTAG operation
---
UG470 Page 7
The specific configuration mode is selected by setting the appropriate level on the dedicated mode input pins M[2:0]. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors (≤ 1 kΩ), or tied directly to ground or VCCO_0. The mode pins should not be toggled during
Table 2-1: 7 Series FPGA Configuration Modes
Configuration Mode – M[2:0]
Master SPI – 001
(ie, M2 low, M1 low, M0 high)

Notes:
---
UG470 Page 21 Table 2-4: Configuration Pin Definitions (Cont'd)
Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to VCCO_0 to ensure a stable High input, and recommend push-button to GND to enable manual configuration reset.
---
UG470 Page 21 Table 2-4: Configuration Pin Definitions (Cont'd)
INIT_B can externally be held Low during power-up to stall the power-on configuration sequence at the end of the initialization process.
Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to VCCO_0 to ensure clean Low-to-High transitions.
---
UG470 Page 22 Table 2-4: Configuration Pin Definitions (Cont'd)
A High signal on the DONE pin indicates completion of the configuration sequence.
The DONE output is an open-drain output by default.
Note: DONE has an internal pull-up resistor of approximately 10 kΩ.
---
UG470 Page 15 Configuration Debugging
The two most important configuration signals, INIT_B and DONE, should be connected to LED drivers. The pulsing of INIT_B from Low to High indicates the completion of initialization at power-up.

| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: Bank 0 | File: FPGA_Bank0.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 12/19 |




Notes:

TODO: Determine if EMCCLK is needed or the internal clock is fine for QSPI
Arty A7 toes EMCCLK to CCLK_0 via 49.9 resistor

UG470 Page 22 Table 2-4: Configuration Pin Definitions (Cont'd)
Active-Low PUDC_B input enables internal pull-up resistors
on the SelectIO pins after power-up and during configuration.
- When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin.
- When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin.

PUDC_B must be tied either directly, or via a ≤ 1 kΩ to VCCO_14 or GND.

| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: Bank 13-14 | File: FPGA_Bank13-14.kicad_sch | |
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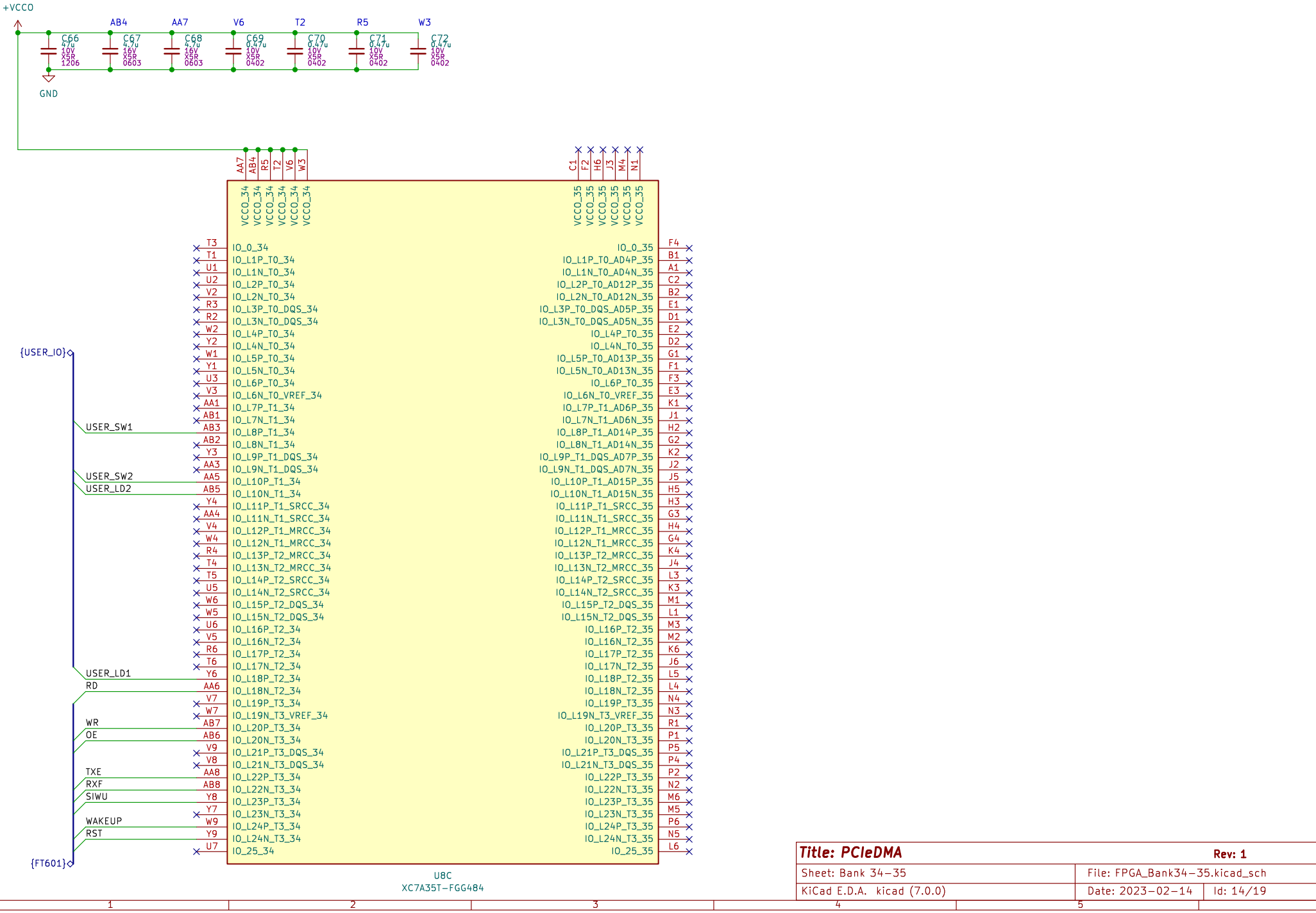
+VCCO
AB4
AA7
V6
T2
R5
W3
C66 47u 10V X5R 1206
C67 4.7u 16V X5R 0603
C68 4.7u 16V X5R 0603
C69 0.47u 10V X5R 0402
C70 0.47u 10V X5R 0402
C71 0.47u 10V X5R 0402
C72 0.47u 10V X5R 0402
GND
AA7 AB4 R5 T2 V6 W3
C1 F2 H6 J3 M4 N1
VCCO_34
VCCO_35
IO_0_34 T3
IO_L1P_T0_34 T1
IO_L1N_T0_34 U1
IO_L2P_T0_34 U2
IO_L2N_T0_34 V2
IO_L3P_T0_DQS_34 R3
IO_L3N_T0_DQS_34 R2
IO_L4P_T0_34 W2
IO_L4N_T0_34 Y2
IO_L5P_T0_34 W1
IO_L5N_T0_34 Y1
IO_L6P_T0_34 U3
IO_L6N_T0_VREF_34 V3
IO_L7P_T1_34 AA1
IO_L7N_T1_34 AB1
IO_L8P_T1_34 AB3
IO_L8N_T1_34 AB2
IO_L9P_T1_DQS_34 Y3
IO_L9N_T1_DQS_34 AA3
IO_L10P_T1_34 AA5
IO_L10N_T1_34 AB5
IO_L11P_T1_SRCC_34 Y4
IO_L11N_T1_SRCC_34 AA4
IO_L12P_T1_MRCC_34 V4
IO_L12N_T1_MRCC_34 W4
IO_L13P_T2_MRCC_34 R4
IO_L13N_T2_MRCC_34 T4
IO_L14P_T2_SRCC_34 T5
IO_L14N_T2_SRCC_34 U5
IO_L15P_T2_DQS_34 W6
IO_L15N_T2_DQS_34 W5
IO_L16P_T2_34 U6
IO_L16N_T2_34 V5
IO_L17P_T2_34 R6
IO_L17N_T2_34 T6
IO_L18P_T2_34 Y6
IO_L18N_T2_34 AA6
IO_L19P_T3_34 V7
IO_L19N_T3_VREF_34 W7
IO_L20P_T3_34 AB7
IO_L20N_T3_34 AB6
IO_L21P_T3_DQS_34 V9
IO_L21N_T3_DQS_34 V8
IO_L22P_T3_34 AA8
IO_L22N_T3_34 AB8
IO_L23P_T3_34 Y8
IO_L23N_T3_34 Y7
IO_L24P_T3_34 W9
IO_L24N_T3_34 Y9
IO_25_34 U7
IO_0_35 F4
IO_L1P_T0_AD4P_35 B1
IO_L1N_T0_AD4N_35 A1
IO_L2P_T0_AD12P_35 C2
IO_L2N_T0_AD12N_35 B2
IO_L3P_T0_DQS_AD5P_35 E1
IO_L3N_T0_DQS_AD5N_35 D1
IO_L4P_T0_35 E2
IO_L4N_T0_35 D2
IO_L5P_T0_AD13P_35 G1
IO_L5N_T0_AD13N_35 F1
IO_L6P_T0_35 F3
IO_L6N_T0_VREF_35 E3
IO_L7P_T1_AD6P_35 K1
IO_L7N_T1_AD6N_35 J1
IO_L8P_T1_AD14P_35 H2
IO_L8N_T1_AD14N_35 G2
IO_L9P_T1_DQS_AD7P_35 K2
IO_L9N_T1_DQS_AD7N_35 J2
IO_L10P_T1_AD15P_35 J5
IO_L10N_T1_AD15N_35 H5
IO_L11P_T1_SRCC_35 H3
IO_L11N_T1_SRCC_35 G3
IO_L12P_T1_MRCC_35 H4
IO_L12N_T1_MRCC_35 G4
IO_L13P_T2_MRCC_35 K4
IO_L13N_T2_MRCC_35 J4
IO_L14P_T2_SRCC_35 L3
IO_L14N_T2_SRCC_35 K3
IO_L15P_T2_DQS_35 M1
IO_L15N_T2_DQS_35 L1
IO_L16P_T2_35 M3
IO_L16N_T2_35 M2
IO_L17P_T2_35 K6
IO_L17N_T2_35 J6
IO_L18P_T2_35 L5
IO_L18N_T2_35 L4
IO_L19P_T3_35 N4
IO_L19N_T3_VREF_35 N3
IO_L20P_T3_35 R1
IO_L20N_T3_35 P1
IO_L21P_T3_DQS_35 P5
IO_L21N_T3_DQS_35 P4
IO_L22P_T3_35 P2
IO_L22N_T3_35 N2
IO_L23P_T3_35 M6
IO_L23N_T3_35 M5
IO_L24P_T3_35 P6
IO_L24N_T3_35 N5
IO_25_35 L6
{USER_IO}
USER_SW1
USER_SW2
USER_LD2
USER_LD1
RD
WR
OE
TXE
RXF
SIWU
WAKEUP
RST
{FT601}
U8C
XC7A35T-FGG484
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Rev: 1
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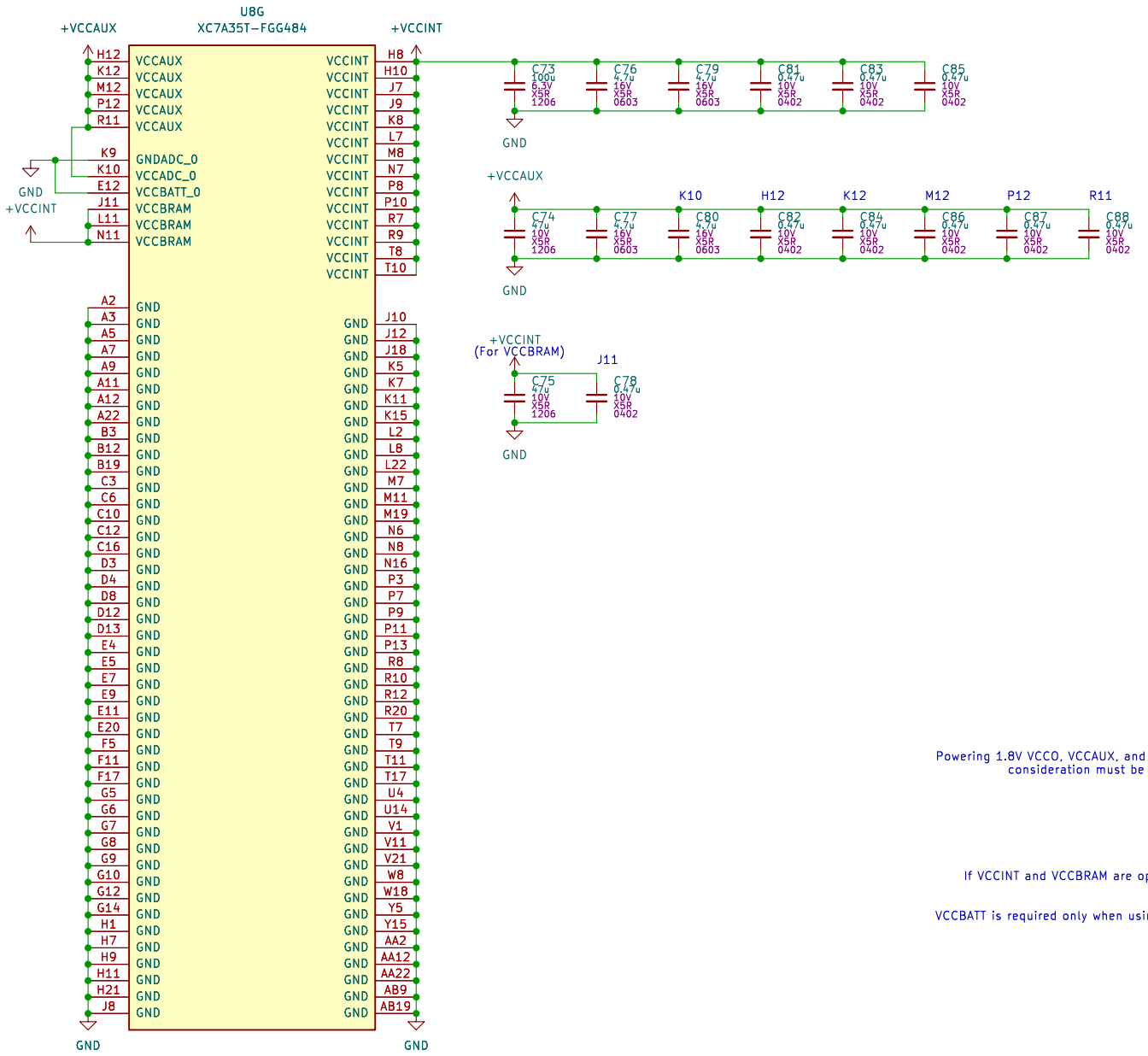
Date: 2023-02-14
Id: 14/19




Notes:

UG483: Table 2–2: Required PCB Capacitor Quantities per Device: Artix–7 Devices
Page 16, row FGG484 XC7A35T
VCCINT: 1x100uF, 2x4.7uF, 3x0.47uF
VCCBRAM: 1x47uF, 1x0.47uF
VCCAUX: 1x47uF, 2x4.7uF, 5x0.47uF

UG483: Page 19: Table 2–5: PCB Capacitor Specifications
100uF: < 1210, Ceramic X7R or X5R, 1nH ESL Max, 5mΩ < ESR < 40mΩ, > 2.5V
47uF: < 1210, Ceramic X7R or X5R, 1nH ESL Max, 5mΩ < ESR < 40mΩ, > 6.3V
4.7uF: < 0805, Ceramic X7R or X5R, 1nH ESL Max, 5mΩ < ESR < 20mΩ, > 6.3V
0.47uF: < 0603, Ceramic X7R or X5R, 0.5nH ESL Max, 5mΩ < ESR < 20mΩ, > 6.3V

UG483: Page 36 Power Supply Consolidation
Powering 1.8V VCCO, VCCAUX, and VCCAUX_IO from a common PCB plane is allowed in 7 series FPGA designs. However, careful consideration must be given to power supply noise–in particular, any noise on the VCCO rail should not violate the recommended operating condition range for the VCCAUX supply.

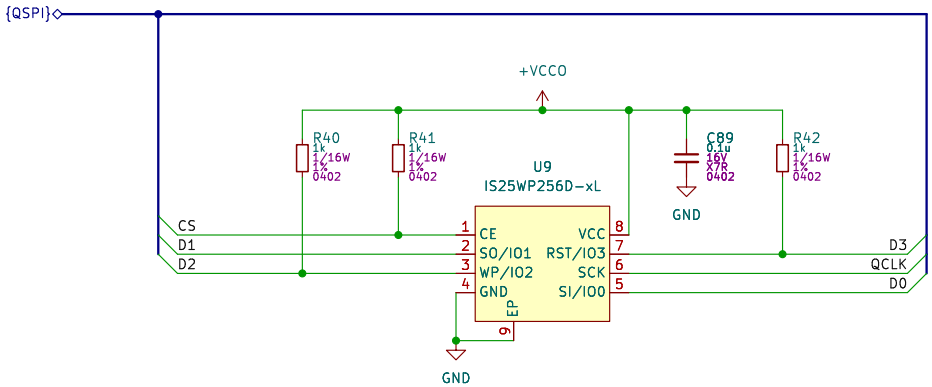
DS181: Page 2 Table 2: Recommended Operating Conditions
VCCAUX Min 1.71, Typ 1.8, Max 1.89
(so +/– 5%)

DS181: Page 3, Note 3
If VCCINT and VCCBRAM are operating at the same voltage, VCCINT and VCCBRAM should be connected to the same supply.

DS181 Page 3,
VCCBATT is required only when using bitstream encryption. If battery is not used, connect VCCBATT to either ground or VCCAUX.

TODO: Confirm if VCCADC tied to VCCAUX if unused is fine

| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: Bank VCC | File: FPGA_BankVCC.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 15/19 |

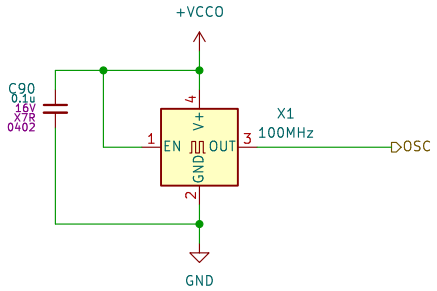



Notes:

Datasheet Rev.A 06/29/2017 Page 9
The Chip Enable (CE#) pin enables and disables the devices operation.
When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the devices non-critical internal circuitry power down to allow minimal levels of power consumption while in a standby state

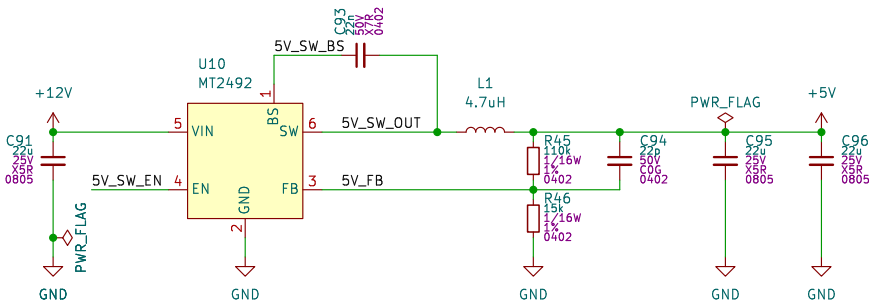
Datasheet Rev.A 06/29/2017 Page 166
9.8 POWER-UP AND POWER-DOWN
At Power-up and Power-down, the device must be NOT SELECTED until Vcc reaches at the right level.
(Adding a simple pull-up resistor on CE# is recommended.)
(also added pullups on dual mode pins)
TODO: is 1k pullup too strong?

| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: Flash | File: Flash.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 16/19 |

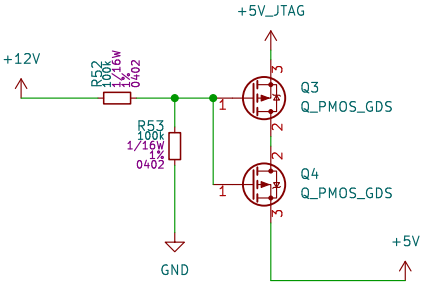


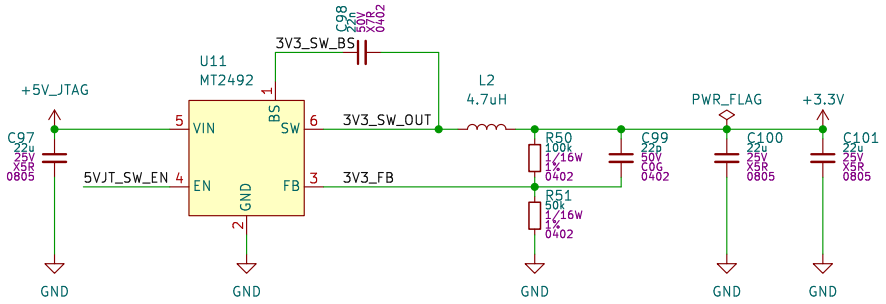

| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: Oscillator | File: Oscillator.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 17/19 |

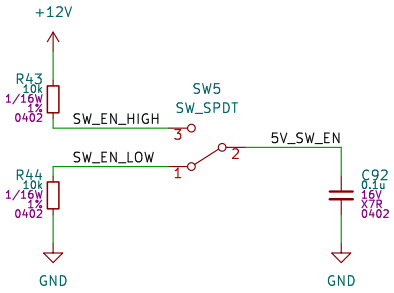
Notes:
From typical application on MT2492 V2.1

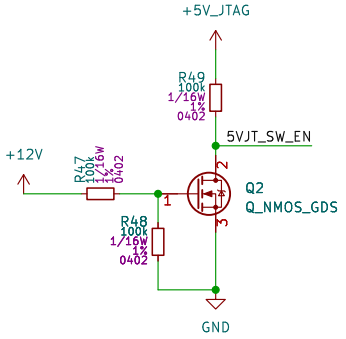



Notes:
This should allow the board to be powered from the jtag supply,
and provide some reverse polarity protection.
TODO: Size some mosfets, maybe dual package so8?



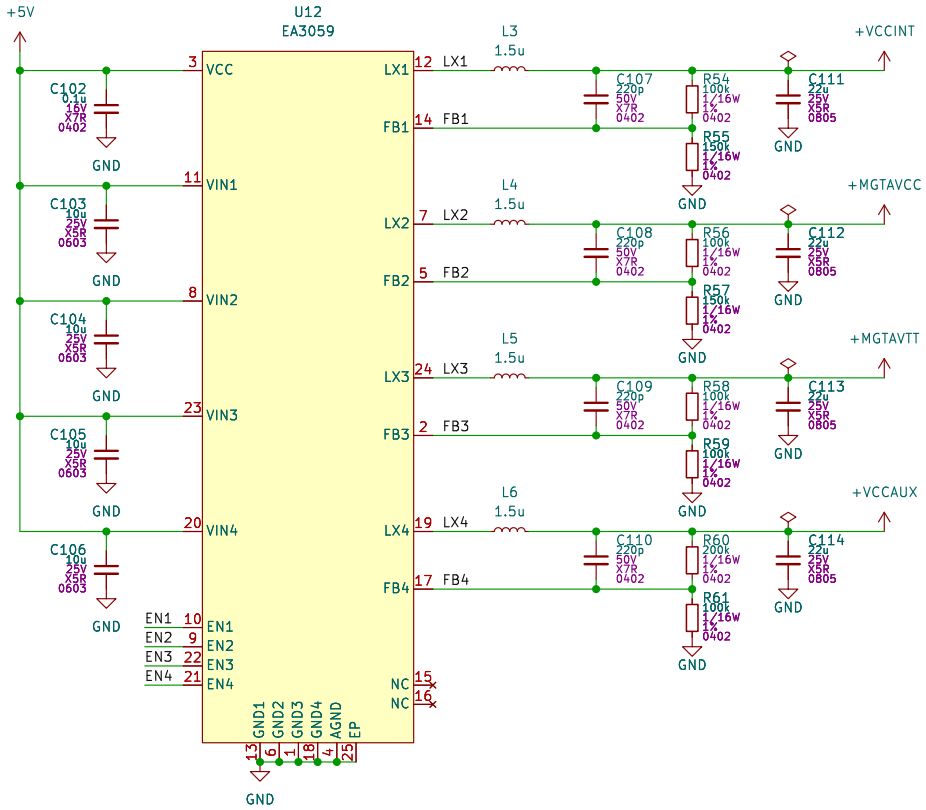




Notes:
Switch enables/disables 5v supply for rest of the board
FPGA voltages derived from this 5v
TODO: should there be another switch for this? Maybe an input for the FPGA?

| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: Board Power | File: PowerBoard.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 18/19 |

Notes:
---
General concept is to power everything from the pcie 12v -> 5v buck if possible,
physical switch on that 5v line to turn fpga off




Notes:
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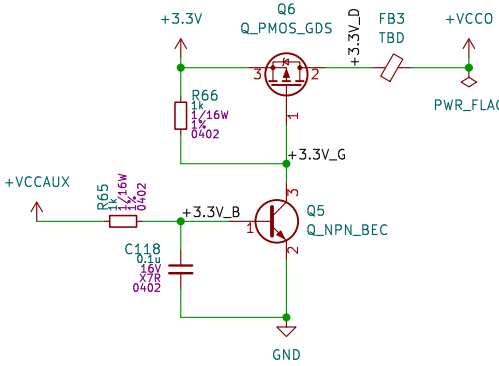
1kOhm * 4.7uF = a few ms until the npn conducts
Ferrite bead for filtering
TODO: Consider filter specifically for pcie 3v3 ripple

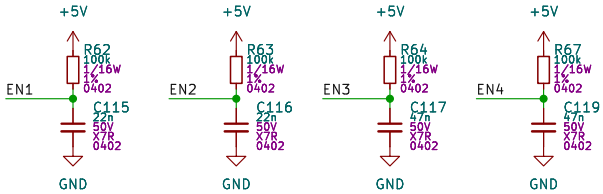



Notes:
---
Min ramp time for all supplies on FPGA is 0.2ms (DS181 Table 7)

EA3059 datasheet gives values 100k and 10n to 100n for power sequencing on EN pins
and a minimum voltage for Enable Pin Input High Voltage of 2V

At 100kR at 22nF,
2=5(1-e^(-t/((100*10^3)*(22*10^-9))))
gives a time of approx 0.0011238, or 1.1238ms

At 100kR and 47nF
2=5(1-e^(-t/((100*10^3)*(47*10^-9))))
gives a time of approx 0.0024009, or 2.4009ms




Notes:
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DS181 Page 8 Power-On/Off Power Supply Sequencing
The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on.

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers
is VCCINT, VMGTAVCC, VMGTAVTT OR VMGTAVCC, VCCINT, VMGTAVTT.
Both VMGTAVCC and VCCINT can be ramped simultaneously.

VCCINT (& VCCBRAM) & VMGTAVCC -> VMGTAVTT & VCCAUX -> VCCO

Notes:
---
V_OUT=0.6 * R1/R2 + 0.6
1.0=0.6*(100/150)+0.6
1.2=0.6*(100/100)+0.6
1.8=0.6*(200/100)+0.6

Notes:
---
Input voltages
PCIe: 12V, 3.3V, 3.3V_aux
USB: 5V
---
Output voltages
VCCO: 3.3V
VCCINT: 1.0V
VCCBRAM: Use VCCINT
VCCAUX: 1.8V
MGTAVCC: 1.0V
MGTAVTT: 1.2V
5V: Leds
3.3V: FT601, CH347

| | | |
|---|---|---|
| **Title: PCIeDMA** | | **Rev: 1** |
| Sheet: FPGA Power | File: PowerFPGA.kicad_sch | |
| KiCad E.D.A. kicad (7.0.0) | Date: 2023-02-14 | Id: 19/19 |