

YADRO ! " # \$ % & '

() * + , , - * . / * . 01234 452- * 3155- 32.

! " # \$ % & ' () # # # " # & + , - , . . # * # / + # 0 , " " # + % / # - 1 - # & 2 3 1 " " 1 \$, ' 4 . 2 5 6 7 , + & 5 # 7 1 \$ - . # 8 , " \$ & # / , + 1 9 , + 1 : . 2 5) ' # ; # & . < % / + 1 - , + , ; \$ % ; 1 -) ' # ; % - # \$. # " 6 \$ " 6 + % = ' 1 3 . 2 , ; # . \$ + # ' ' , + 2 & . , > . 1 5 1 . \$, + 9 , : " # & , ; # . \$ + # ' ' , + / + , + 2 & % . 1 : 1 " / , 0 1 % ' 1 = 1 + # & % . . 2 , & 2 3 1 " " 1 \$, ' 1 . ! " , ? \$ 1 @ " \$ + # : " \$ & % / # 7 ; ' (3 , . 2 ; / + # 0 , " " # + @ " / # - # A 4 (" 1 " \$, - . # : > 1 . 2 . B ' # ; , . , / # " + , 7 " \$ & , . . # + , % ' 1 = @ (A 1 : 9 @ . ; 0 1 1 " 1 " \$, - . # : > 1 . 2 , . % = 2 & % , \$ " 6 1 . \$, + ; # . . , ; \$ # - : # . - % + > + @ \$ 1 = 1 + @ , \$ = % / + # " 2 # \$ & 2 3 1 " " 1 \$, ' 4 . 2 5 6 7 , + ; 7 + @ * 1 - @ " \$ + # : " \$ & % - , 1 & # = & + % A % , \$ #) + % \$. # 1 5 # \$ & , \$ 2 . C + # 1 = & # 7 1 \$, ' 4 . # " \$ 4 1 . \$, + ; # . . , ; \$ % . , / # " + , 7 " \$ & , . . # & ' 1 6 , \$. % / + # 1 = & # 7 1 \$, ' 4 . # " \$ 4 & , : " 1 " \$, - 2 . < % > % ; # - % . 7 % = % . 1 - % , \$ " 6 + % = + %) # \$; # : 1 / # 7 7 , + 8 ; # : 1 . \$, + ; # . . , ; # & 7 ' 6 3 1 / # & , + % = + %) % \$ 2 & % , - 2 5 ; # - % . 7 # : YADRO.

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D' 6 \$ # * # , 3 \$ #) 2 / + # 7 @ ; \$ 1 & . # " \$ % 8 1 + # & % \$ 4 " 6 & . % > , : * + @ / / , , . . , #) 5 # 7 1 - " " , 7 @ (A 1 : - 1 . 1 - % ' 4 . 2 : . %) # + = . % . 1 : 1 . % & 2 ; # & :

¥ B % = # & 2 , = . % . 1 6 0 1 9 + # & # : " 5 , - # \$, 5 . 1 ; 1

¥ < % 3 % ' 4 . 2 : # / 2 \$ + % = + %) # \$; 1 RTL . % Verilog/SystemVerilog 1 . % & 2 ; 1 + %) # \$ 2 " " 1 - @ ' 6 \$ # + # -

D # / # ' . 1 \$, ' 4 . 2 - 1 / ' (" % - 1) @ 7 @ \$:

¥ E / 2 \$ + %) # \$ 2 " CFGH

¥ C + # 3 1 \$ % ' ; . 1 * @ " I 1 9 + # & % 6 " 5 , - # \$, 5 . 1 ; % 1 % + 5 1 \$, ; \$ @ + % ; # - / 4 (\$, + % , D ? & 1 7 J % + + 1 " 1 H % + % J % + + 1 " "

: - ; 2181- /. < . 54-

EO , . 1 \$ 4 & % > 1 = . % . 1 6 1 . % & 2 ; 1 / # - # 8 , \$ \$, " \$ & # , = % 7 % . 1 , . ! 2 - # 8 , \$, & 2) + % \$ 4 ' () # : 1 = / , + , 3 1 " " , . . 2 5 . 1 8 , & % + 1 % . \$ # & .

NOTE

H' # 8 . # " \$ 4 = % 7 % . 1 : # \$ ' 1 3 % , \$ " 6 . D' 6 " #) , " , 7 # & % . 1 6 7 # " \$ % \$ # 3 . # + , > 1 \$ 4 # 7 1 . 1 = & % + 1 % . \$ # & . K 2 # 0 , . 1 - , , " " 1 & 2 + , > 1 \$,) # ' , , " ' # 8 . 2 : & % + 1 % . \$.

NOTE

L % = + %) # \$ % . . 2 :) ' # ; - # 8 , \$ 1 - , \$ 4 = % 7 , + 8 ; @ (latency) , % - # 8 , \$ 1 . , 1 - , \$ 4 - + , > % \$ 4 & % -

NOTE

K 2 # 0 , . 1 - , , " " 1 & 2 " 7 , ' % , \$,) ' # ; , #) ' % 7 % (A 1 : - 1 . 1 - % ' 4 . 2 - latency 1 - % ; " 1 - % ' 4 . # : / + # / @ " ; . # : " / # " #) . # " \$ 4 (. < #) @ 7 , \$ 7 # " \$ % \$ # 3 . # , , " " 1 # . / + # " \$ #) @ 7 , \$ + %) # \$ % \$ 4 . M & 2 # \$ 7 , ' 4 . # (& README) / , + , 3 1 " " 1 \$, # * + % . 1 3 , . 1 6 & % > , : + , % ' 1 = % 0 1 1 1 & # = - # 8 . 2 , " / # " #) 2 1 5 @ " \$ + % . . . 1 6 .

! " # \$ % & % \$ ' () *) + , - # . #) + ,

1. C + # , ; \$ 1 + # & % . 1 , . L , = @ ' 4 \$ % \$ # - ? \$ % / % 6 & ' 6 , \$ " 6 README , & ; ' (3 % (A 1 : :

N # / 1 " % . 1 , / + 1 . 6 \$ 2 5 / + 1 / + # , ; \$ 1 + # & % . 1 1 + , > , . 1 : ;

N (# / O 1 # . % ' 4 . #) - 1 ; + # % + 5 1 \$, ; \$ @ + . 2 , 7 1 % * + % - - 2 @ " \$ + # : " \$ & % ;

N # / 1 " % . 1 , + %) # \$ 2 " / + # , ; \$ 1 + # & % . . 2 5 - # 7 @ ' , : ;

< % - & % 8 , . & / , + & @ (# 3 , + , 7 4 5 # 7 & % > 1 5 - 2 " ' , : / + 1 / + # , ; \$ 1 + # & % . 1 1) ' # ; % .

2. O # 7 1 + # & % . 1 , 1 bring-up \$, " \$. L , = @ ' 4 \$ % \$ # - 7 % . . # * # ? \$ % / % 6 & ' 6 , \$ " 6 :

N ; # 7 . % Verilog 1 ' 1 System Verilog

N testbench 1 . %) # + \$, " \$ # & 2 5 & , ; \$ # + # & 7 ' 6 " + , 7 2 ModelSim

N (# / O 1 # . % ' 4 . #) " ; + 1 / \$ 7 ' 6 = % / @ " ; % " 1 - @ ' 6 \$ # + % (Makefile 1 ' 1 bash)

=. *4. 52 1. #*- 10*. /18. 2->? valid/credit
452- *@- A; . 8 valid/ready 452- *@- A;

Figure 1. /" 012" 10) #, 34*5# 5'. 1(, vc_vr_converter

6) " *07*83 5'. 1(,

```
module vc_vr_converter #(
    È parameter DATA_WIDTH = 8,
    È           CREDIT_NUM = 2
)(
    È input logic          clk,
    È input logic          rst_n,

    È //valid/credit interface
    È input logic [DATA_WIDTH-1:0] s_data_i,
    È input logic                  s_valid_i,
    È output logic                  s_credit_o,

    È //valid/ready interface
    È output logic [DATA_WIDTH-1:0] m_data_o,
    È output logic                  m_valid_o,
    È input logic                  m_ready_i
);
```

(, 4; . 54-

<, #) 5#71- # +%=+%) #\$\$\$4 /+, #) +%=#&\$\$, ' 4 valid/credit 1. \$, +9, : "% & valid/ready 1. \$, +9, : ".

90' " ' 2' (\$0+: 5# . #)) %4

1. <% &5#7 - #7@' 6 /#" \$@/(\$ 7%. . 2, /# > 1. , s_data_i > 1+1. #: DATA_WIDTH.D%. . 2, s_data_i /, +, 7%(\$"6 \$#' 4; # & \$#- "' @3%, , , "' 1 s_valid_i +%&, . , 71. 10, .
2. K#7@' 4 1- , , \$; #' 13, "\$&# 7#" \$@/. 25 ; +, 71\$#& +%&. #, CREDIT_NUM. C#7 ; +, 71\$%- 1 =7, "4 /#7+%=@- , &%, \$"6 ; #' 13, "\$&# 7%. . 25 s_data_i , ; # \$#+, , "/"#") , . /+1. 6\$4 - #7@' 4 /# "1*. %' @ s_valid_i. ! \$#- "' @3%, , , "' 1 \$, ; @A, , ; #' 13, "\$&# ; +, 71\$#& & - #7@' , +%&. #. @' (, \$# /#' @3, . . 2, & \$, ; @A, - \$%; \$, 7%. . 2, s_data_i /# "1*. %' @ s_valid_i)@7@\$ /#\$, +6. 2. C#7+%=@- , &%, \$"6, 3\$# /#" , . 6\$16 ") +#" " - #7@' 6 \$, ; @A, , ; #' 13, "\$&# 7#" \$@/. 25 ; +, 71\$#& +%&. # /%+%- , \$+@ CREDIT_NUM.
3. P, +, = /#+\$ s_credit_o /, +, 7%Q\$"6 1. 9#+- %016 # 7#" \$@/. 25 ; +, 71\$%5. G- /@' 4" . % 1 \$%; \$

```
. % s_cred_i t_o /#; %=2&%, $ master-@"$+#: "$&@, 3$# "$%' 7#"$/,. , A Q 1 ; +, 71$. C+1 ?$#-
master-@"$+#: "$&# . , 7#' 8. # @"$%. %&' 1&%"$4 "1*. %' s_val_i d_i & , 71. 10@ /+1 # $"@"$&11
7#"$/ . 25 ; +, 71$#&. G=. %3%' 4. #, /+1 %; $1&. #- ") +#", - #7@' 6 vc_vr_converter, master-
@"$+#: "$&# "31$%, $, 3$# 7#"$/ . 2, ; +, 71$2 # $"@"$&@ ( $. C+1 ". 6$11 ") +#" % - #7@' 4
vc_vr_converter 7#' 8, . &, +. @$4 master-@"$+#: "$&@ CREDIT_NUM ; +, 71$#& 3, +, = /#+$
s_cred_i t_o.
```

90' " ' 2' (\$*0*. #; +. #)) %4

1. <% &25#7 /#+\$ m_data_o /, +, 7% (\$"6 /#' @3, . . 2, 7%. . 2, 3, +, = &5#7. #: /#+\$ s_data_i.
C+1 ?\$#- 7%. . 2, . % m_data_o "31\$% (\$"6 ; #++ , ; \$. 2- 1 \$#' 4; # & \$#- "' @3%, , , "' 1 m_val_i d_o
+&%, . , 71. 10, .
2. D%. . 2, m_data_o "31\$% (\$"6 /, +, 7%. . 2- 1, , , "' 1 m_val_i d_o 1 m_ready_i #7. #&+, - , . . #
@"\$%. #&' , . 2 & , 71. 10@. % \$, ; @A, - \$%; \$, .
3. R"' 1 "1*. %' m_val_i d_o @"\$%. #&' , . & 1, \$# m_data_o . , - #8, \$ - , . 6\$4 "&#, =. %3, . 1, , /#; % . ,
)@7, \$ /#7\$&, +87, . 16 3, +, = m_ready_i.
4. D%. . 2, . % &25#7 7#' 8. 2 /, +, 7%&%"\$4"6 & \$#- 8, /#67; , , & ; %; #- #. 1 /#"\$/1' 1 . %
&5#7.

<18, /+1&, 7, . /+1- , + /+, #) +%=#&%. 16 1. \$, +9, : "#& 7' 6 ; #. 91* @+ %011:

```
DATA_WIDTH = 8
CREDIT_NUM = 2
```

Figure 2. 90+5*0 \$0*' <0#-' &#) +, +) " *07*83' &

=. *4. 52 2. #1213189A *- 1*<- *-0+@- *

Figure 3. /" 012" 10) #, 34*5# 5'. 1(, reorder_buffer

6) " *07*83 5'. 1(,

```
module reorder_buffer #(
    È parameter DATA_WIDTH = 8
)(
    È input logic          clk,
    È input logic          rst_n,

    È //AR slave interface
    È input logic          [3:0] s_arid_i,
    È input logic          s_arvalid_i,
    È output logic         s_arready_o,

    È //R slave interface
    È output logic [DATA_WIDTH-1:0] s_rdata_o,
    È output logic          [3:0] s_rid_o,
    È output logic         s_rvalid_o,
    È input logic          s_rready_i,

    È //AR master interface
    È output logic          [3:0] m_arid_o,
    È output logic         m_arvalid_o,
    È input logic          m_arready_i,

    È //R master interface
    È input logic [DATA_WIDTH-1:0] m_rdata_i,
    È input logic          [3:0] m_rid_i,
    È input logic         m_rvalid_i,
    È output logic         m_rready_o
);
```

(, 4; . 54-

<, #) 5#71- # +%=%) #\$\$\$4 /#\$\$; #&2: +, #+7, +-)@9, +, ; #\$\$+2: :

¥ C+1. 1- %, \$ /#\$\$; 1= 16 @. 1; %' 4. 25 ID & 71%/=#. , # \$ 0 7# 15 3, +, = AR slave 1. \$, +9, : ".
C#+67#; ID & /#\$\$; , - #8, \$) 2\$4 /+#1=&#' 4. 2- .

¥ C, +, 7%Q\$ /#\$\$; ID), = 1=- , . . 1: & \$#- 8, /#+67; , 1= AR slave 1. \$, +9, : "% & AR master
1. \$, +9, : ".

¥ D' 6 ; %87## / , +, 7%. . ## ID . % AR master 1. \$, +9, : " , /+1. 1- %, \$ 7%. . 2, 3, +, = R master
1. \$, +9, : ". 0%87#, "' #&# 7%. . 25 \$%; 8, /#- , 3, . # ID, . # /#+67#; /+1Q- % 7%. . 25 . % R
master 1. \$, +9, : " , - #8, \$, , "#&/%7%\$4 " /#+67; #- / , +, 7%31 ID . % AR master 1. \$, +9, : " , .

¥ ! 27%, \$ 7%. . 2, . % R slave 1. \$, +9, : " , / , +, @/#+67#31&%6 15 \$%; 1- #) +%=#- , 3\$#) 2 ID
/#\$\$; % 7%. . 25 "##\$&, \$"\$&#&%' 1 /#+67; @ ID 1= /#\$\$; % ID . % AR slave 1. \$, +9, : " , .

90' " ' 2' (\$0+: 5# ID

1. <% &5#7 1. \$, +9, : "% AR slave . % > 1. @ s_arid_i - #7@' 6 reorder_buffer /#"\$/%(\$ ID &
71%/=#. , # \$ 0 7# 15. C+1 ?\$#- ID . % > 1. , s_arid_i "31\$('\$6 ; #++ , ; \$. 2- 1 \$#' 4; # & \$#-
"' @3%, , , "' 1 s_arvalid_i +%&, . , 71. 10, .
2. ID . % > 1. , s_arid_i "31\$('\$6 /+1. 6\$2- , , "' 1 s_arvalid_i 1 s_arready_o #7. #&+ , - , . . #
@"\$%. #&' , . 2 & , 71. 10@. % \$, ; @A, - \$%; \$, .
3. R"' 1 "1*. %' s_arvalid_i @"\$%. #&' , . & 1, \$# s_arid_i . , - #8, \$ - , . 6\$4 "&# , = . %3, . 1, , /#; %
 , ,)@7, \$ /#7\$&, +87, . 16 3, +, = s_arready_o.

90' " ' 2' (\$*0*. #; + ID

1. <% &25#7 1. \$, +9, : "% AR master . % > 1. @ m_arid_o - #7@' 6 reorder_buffer), = 1=- , . . 1: 1 &
\$#- 8, /#+67; , / , +, 7%('\$6 ID, /#' @3, . . 2, /# 1. \$, +9, : "@ AR slave. C+1 ?\$#- ID . % > 1. ,
m_arid_o "31\$('\$6 ; #++ , ; \$. 2- 1 \$#' 4; # & \$#- "' @3%, , , "' 1 m_arvalid_o +%&, . , 71. 10, .
2. ID . % > 1. , m_arid_o "31\$('\$6 /+1. 6\$2- , , "' 1 m_arvalid_o 1 m_arready_i #7. #&+ , - , . . #
@"\$%. #&' , . 2 & , 71. 10@. % \$, ; @A, - \$%; \$, .
3. R"' 1 "1*. %' m_arvalid_o @"\$%. #&' , . & 1, \$# m_arid_o . , - #8, \$ - , . 6\$4 "&# , = . %3, . 1, , /#; %
 , ,)@7, \$ /#7\$&, +87, . 16 3, +, = m_arready_i.

90' " ' 2' (\$0+: 5# . #)) %4

1. D' 6 ; %87## / , +, 7%. . ## ID 3, +, = 1. \$, +9, : " AR master . % &5#7 1. \$, +9, : "% R master . %
> 1. @ m_rid_i &#=&+%A%, '\$6 \$#\$ 8, ID &- , "\$, " 7%. . 2- 1 . % > 1. , m_rdata_i > 1+1. #:
DATA_WIDTH. C+1 ?\$#- 7%. . 2, &- , "\$, " ID - #*\$ \$ /+15#71\$4 " /+#1=&#' 4. #: =%7, +8; #:
1 /#+67#; ID . % > 1. , m_rid_i & #) A, - "' @3%, - #8, \$, , "##\$&, \$"\$&#&%'4 /#+67; @
/ , +, 7%31 ID /# 1. \$, +9, : "@ AR master. D%. . 2, . % m_rdata_i 1 ID . % m_rid_i "31\$('\$6
; #++ , ; \$. 2- 1 \$#' 4; # & \$#- "' @3%, , , "' 1 m_rvalid_i +%&, . , 71. 10, .
2. D%. . 2, m_rdata_i 1 ID m_rid_i "31\$('\$6 /+1. 6\$2- 1, , "' 1 m_rvalid_i 1 m_rready_o
#7. #&+ , - , . . # @"\$%. #&' , . 2 & , 71. 10@. % \$, ; @A, - \$%; \$, .
3. R"' 1 "1*. %' m_rvalid_i @"\$%. #&' , . & 1, \$# m_rdata_i 1 m_rid_i . , - #*\$ \$ - , . 6\$4 "&# ,
= . %3, . 1, , /#; % , ,)@7, \$ /#7\$&, +87, . 16 3, +, = m_rready_o.

90' " ' 2' (\$*0*. #; + . #)) %4

1. R"" 1 . % 1. \$, +9, : ", R master) 2' 1 /# ' @3, . 2 7%. . 2, " ID, ; # \$ # + 2:) 2' / + 1. 6\$ +%. 4> ,
 & ", 5 . % 1. \$, +9, : ", AR slave, \$# ?\$ 1 7%. . 2, / , +, 7%(\$" 6 . % & 25# 7 /# + \$ % s_rdata_o, % . %
 & 25# 7 s_rid_o / , +, 7% Q \$" 6 ID, ; # \$ # + 2: " ## \$ & , \$ " \$ & @, \$?\$ 1 - 7%. . 2 - . E "\$ % ' 4. 2, 7%. . 2,
 & - , " , " ID 7# ' 8. 2 / , +, 7% & % \$ 4 " 6 %. % ' # * 13. # & /# + 67; , " ' , 7# & %. 16 ID . % 1. \$, +9, : ", AR
 slave. C + 1 ?\$ # - 7%. . 2, . % s_rdata_o 1 ID . % s_rid_o " 31\$ % (\$" 6 ; # + + , ; \$. 2 - 1 \$ # ' 4; # & \$ # -
 " ' @ 3%, , , " ' 1 s_rvalid_o + % & , . , 71. 10, .

2. D%. . 2, s_rdata_o 1 ID s_rid_o " 31\$ % (\$" 6 / , +, 7%. . 2 - 1, , " ' 1 s_rvalid_o 1 s_rready_i
 # 7. # & +, - , . . # @ "\$ % . # & ' , . 2 & , 71. 10 @ . % \$, ; @ A, - \$ % ; \$, .

3. R"" 1 " 1*. % ' s_rvalid_o @ "\$ % . # & ' , . & 1, \$ # s_rdata_o 1 s_rid_o . , - # * @ \$ - , . 6\$ 4 " & #,
 =. % 3, . 1, , /# ; % . ,) @ 7, \$ /# 7\$ & , + 87, . 16 3, +, = s_rready_i.

< 18, / + 1 & , 7, . / + 1 - , + + , # + 7, + 1. * % 7' 6 3, \$ 2 +, 5 ID # \$ 0 7# 3 7' 6 ; #. 91 * @ + % 0 1 1:

DATA_WIDTH = 8

Figure 4. 90+5*0 0*' 0. *0+) =#