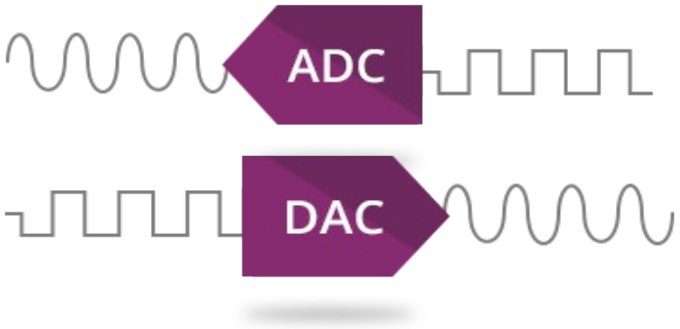
The Many Dimensions of SDR Hardware

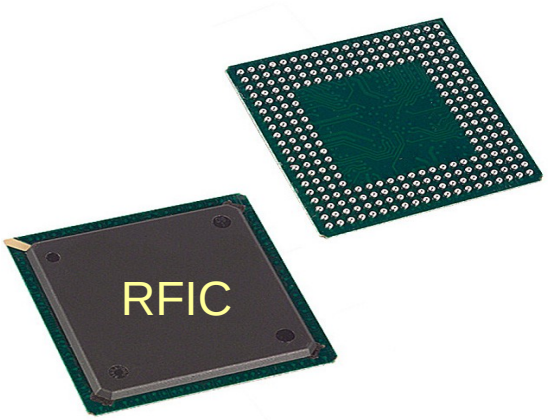
Plotting a Course for the Hardware Behind the Software

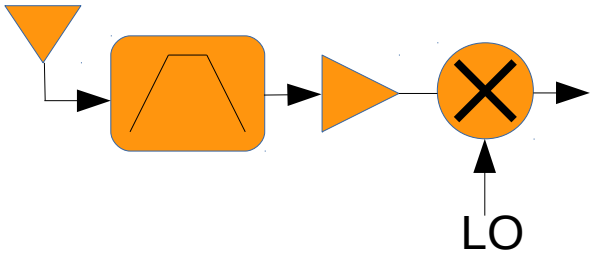
Sept 2017



John Orlando

Epiq Solutions





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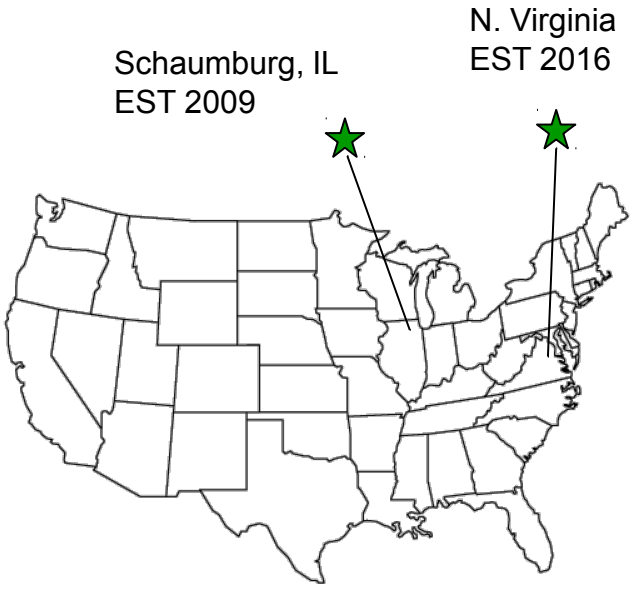
Epiq Solutions in a Nutshell

- **How we help our customers**
  - Develop and deliver <u>SDR transceiver building blocks</u> that radically reduce our customer's SWaP and time to market
  - Develop and deliver <u>turnkey wireless sensing solutions</u> to provide detailed insight into wireless networks and devices operating in areas of interest



Sidekiq

Matchstiq

4G LTE

Wi Fi

EPIQ SOLUTIONS

Trying to understand SDR specs is like...

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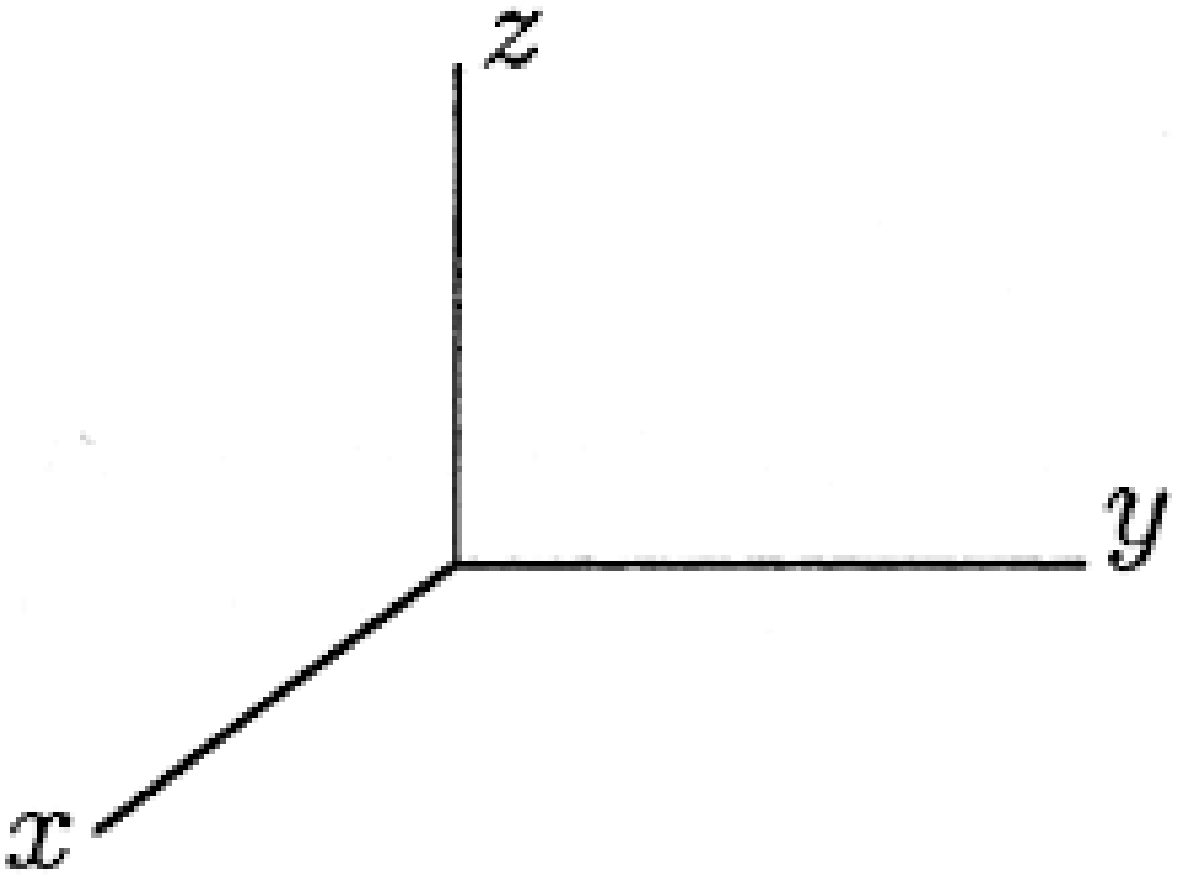
Many-Dimensional Space of SDR



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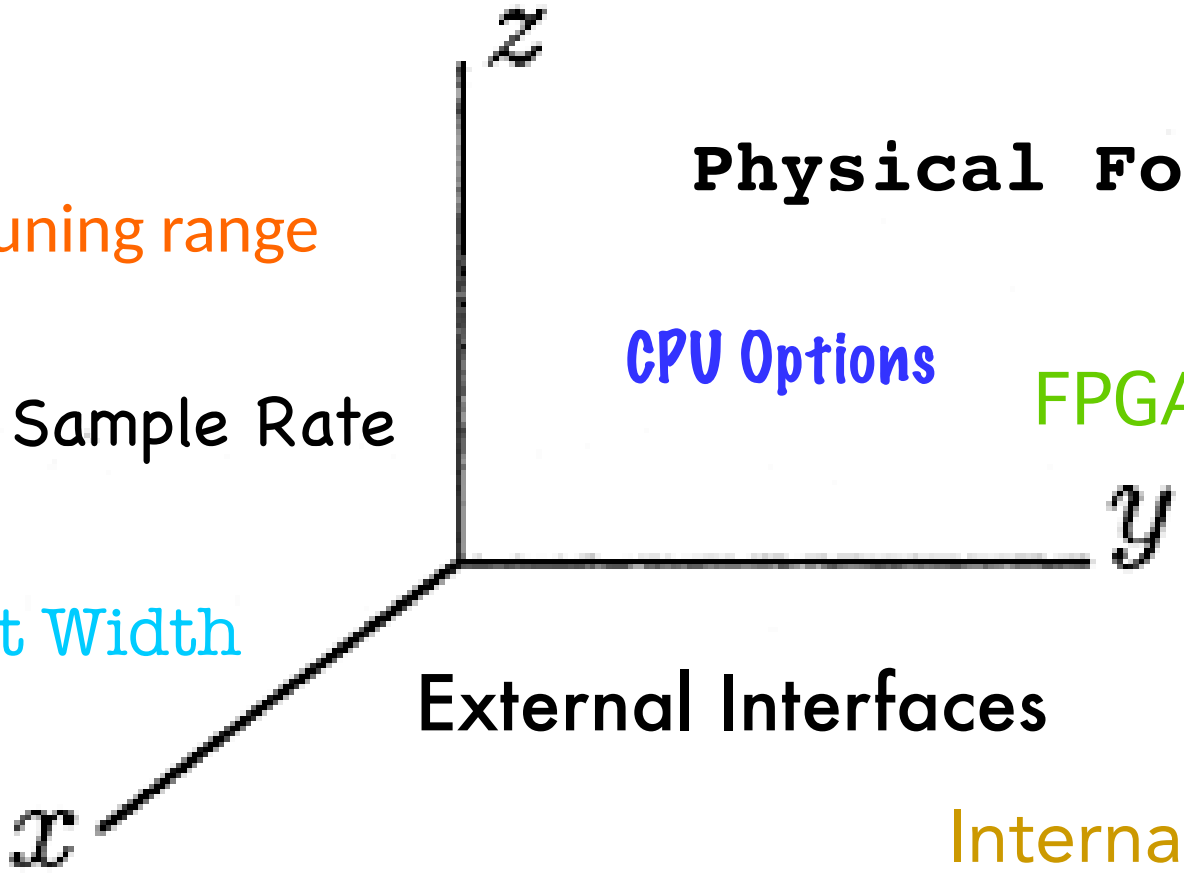
Many-Dimensional Space of SDR



Physical Form Factor

RF tuning range

CPU Options

FPGA Options

Sample Rate

Sample Bit Width

External Interfaces

Internal Interfaces

Instantaneous Bandwidth

Software APIs

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Outline for Today

Five Key SDR Hardware Parameters:

1) Form Factor
2) RF Tuning Range
3) Data Converters
4) Interface
5) CPU Class

- What are the options available today?
- What you should be thinking about when developing a system?
- What is coming down the pike tomorrow?

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Form Factor

Form Factor

RACK MOUNTED

Quadratiq

USRP X310

Maveriq

CUSTOM

Matchstiq S10

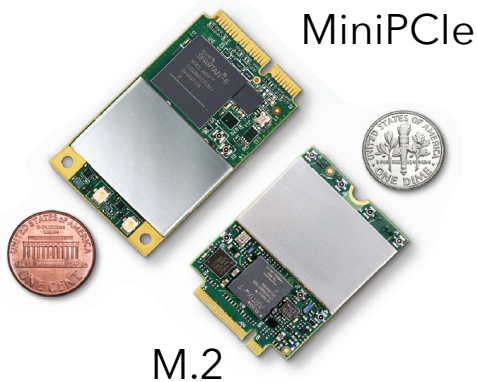
USRP E310

HackRF

LimeSDR

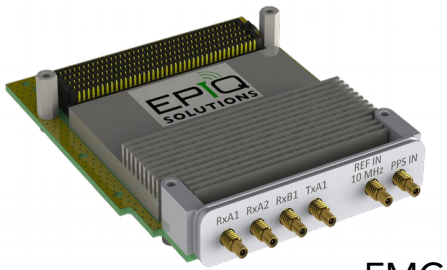
STANDARD CARD

MiniPCIe



M.2

Sidekiq Family



FMC (VITA 57.1)

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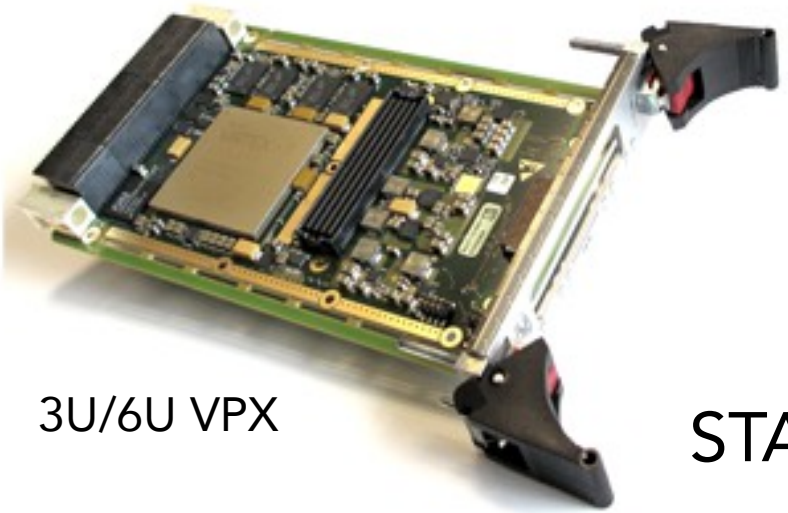
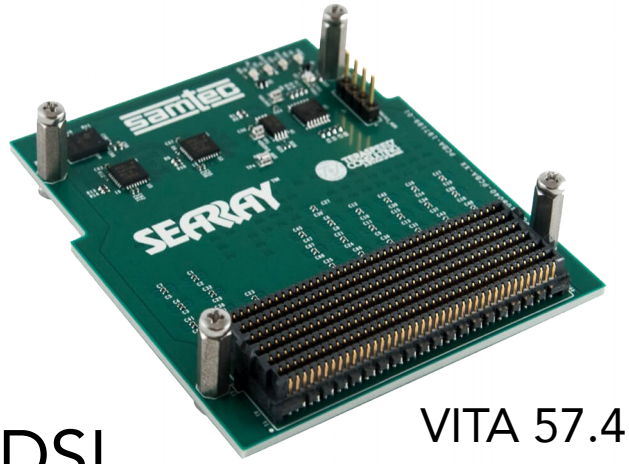
Form Factor – Industry Trends



3U/6U VPX

STANDARDS!



VITA 57.4 (FMC+)

M.2 2280

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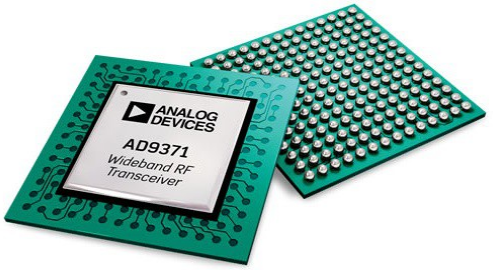
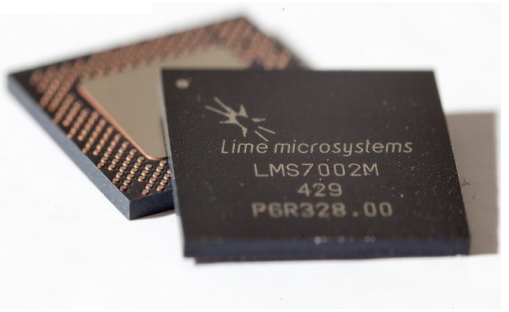
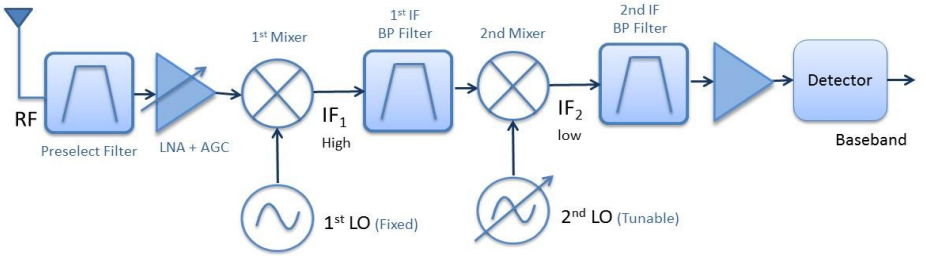
RF Tuning Range

- RFIC based
  - Analog Devices AD9361: 70 MHz to 6 GHz
  - Analog Devices AD9371: 300 MHz to 6 GHz
  - Lime Micro LMS7002: 100 KHz to 3.8 GHz
- Discrete designs
  - Superheterodyne covering 2 MHz to 6 GHz
- Direct RF Sampling
  - DC to 2 GHz (with caveats)
- Block up/down converter + RFIC
  - Best of both worlds
  - 1 MHz to 6 GHz







Matchstiq S12

Sidekiq X2

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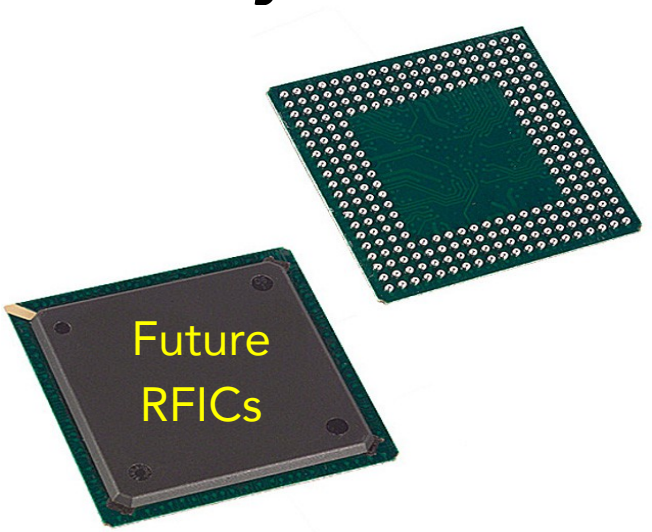
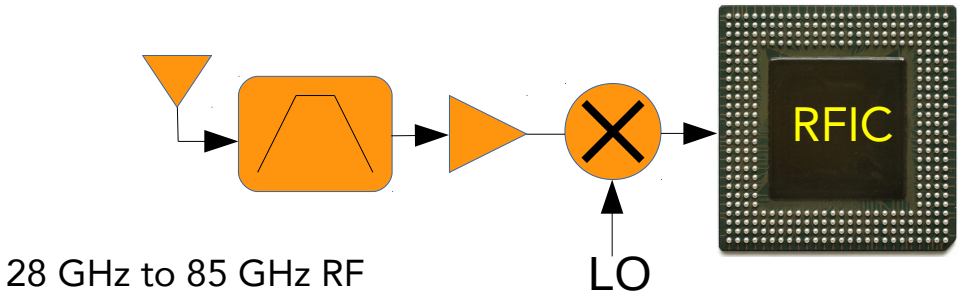
RF Tuning Range – Industry Trends

- RFIC based
  - DC to 6-12 GHz
- What about higher?
  - 28+ GHz for 5G
  - Hybrid block up/down converter + RFIC
- What about higher-er?
  - 60 GHz to 85 GHz
  - Hybrid block up/down converter + RFIC





Data Converters

- Current RFICs have integrated data converters
  - AD9361: Up to 61.44 Msps, 12-bit A/D, 12-bit D/A, parallel interface
  - LMS7002: Up to 61.44 Msps, 12-bit A/D, 12-bit D/A, parallel interface
  - AD9371: Up to 122.88 Msps, 16-bit A/D, 14-bit D/A, serial interface (JESD204b)
- Discrete A/D and D/A converters
  - 16-bit for IF sampling (up to 100s of Msps)
  - 12-bit for direct RF sampling (up to 4 Gsps)
  - JESD204b most common interface these days

ENOB!

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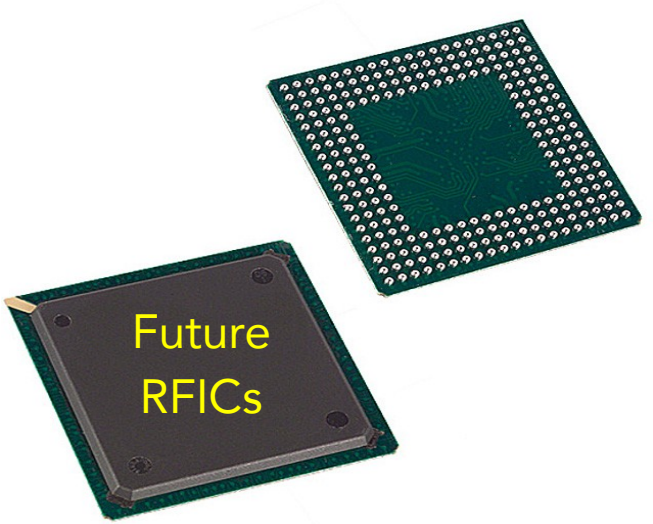
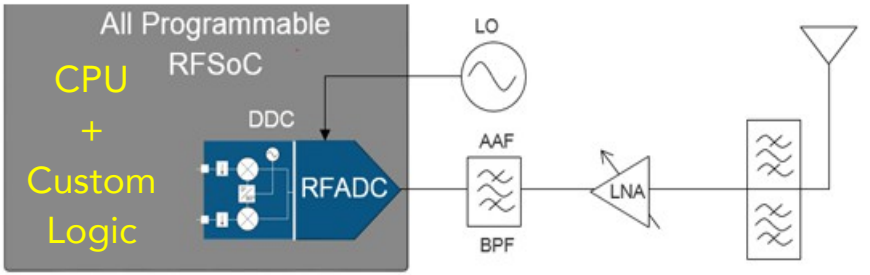
Data Converters – Industry Trends

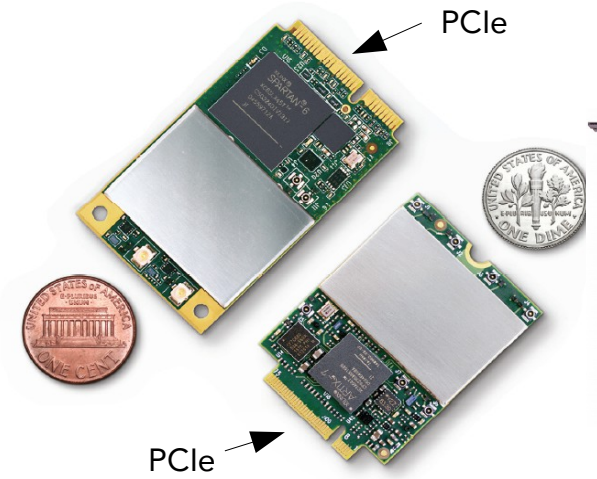
- RFICs
  - 100s of Msps
  - Topping out at 16-bits
  - Serial interface (JESD204b)
- Fully integrated into FPGA
  - Xilinx RFSoC
  - FPGA fabric + multi-Gsps A/D and D/A converters in single chip
  - 2/4/8/16 channels
  - No JESD204b to worry about
  - Same challenges as any direct RF sampling solution

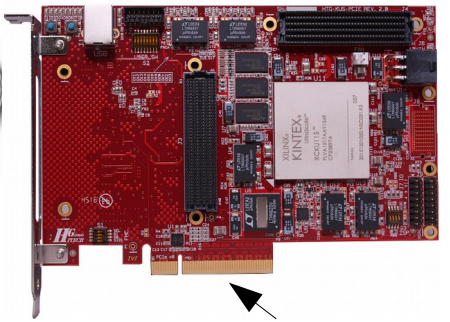




Interfaces

- PCIe
  - Fast (up to 16 Gbps per lane), low latency, scalable
  - Optimized/efficient transport
  - Typically an edge connector interface
  - Focused on generic data transport
- Ethernet
  - Fast (10 Gbps), medium latency, scalable
  - Bulky connectors + cables (SFP+)
  - Focused on networking use-case
- USB 3.0/3.1
  - Fast (5/10 Gbps), higher latency, difficult to scale
  - Typically a cable interface
  - Focused on consumer use-cases and peripherals (cameras, data storage, etc)





10 GbE

USB 3.0

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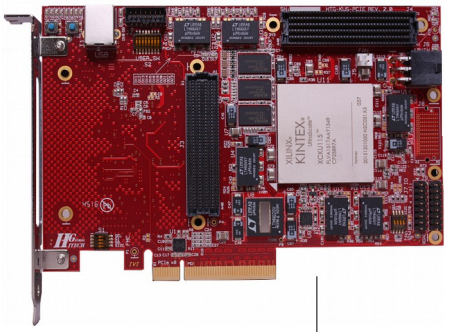
Interfaces – Industry Trends

- PCIe all day long
  - Gen5 hits 32 Gbps per lane (2019)
- Thunderbolt 3
  - Cabled PCIe for the masses!
  - Baked into USB-C connector
  - Up to 40 Gbps (well, 32 Gbps for PCIe... 4 lanes x 8 Gbps)
  - Daisy-chain multiple devices with single host
- Ethernet
  - 10 GbE over RJ45
  - Laptops need to catch up
  - 40G/100G

+



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CPU Classes

- Key architectural questions for SDR usage
  - Core CPU processing capability (SIMD options?)
  - I/O options to move data in/out of the CPU
  - Memory architecture (cache, RAM, and non-volatile)
  - Lots of others, but these are the big ones
- ARM
  - Single/dual/quad/octo core solutions
  - 1W – 10W typical power consumption
  - Ex: NXP (formerly Freescale) i.MX6 and i.MX7
  - Ex: Xilinx Zynq and Zynq Ultrascale System on Chip
- Intel x86
  - Solutions from 1 to 24 cores
  - 4W to 70W+
  - Better support for GPU usage
  - Ex: Atom "Apollo Lake" (1-4 cores) family very power efficient with familiar x86 SIMD extensions

Dual-core ARM (Zynq)

Quad core ARM (i.MX6)

Quad core x86

12 core x86

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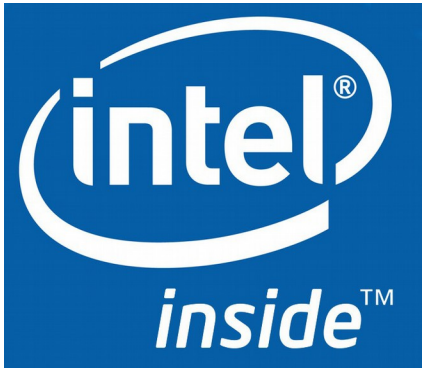
CPU Classes – Industry Trends

- Companies continue to experiment with massive multi-core
  - Ex: Adapteva Epiphany CPU, Ceva DSP, others
  - Still no formidable traction
- Same old same old?
  - ARM and x86 will continue to lead the charge
  - 4-8 cores seems to be the sweet spot
  - AMD Ryzen Threadripper (8/12/16 core x86)
  - GPU additions continue to improve
  - Intel recently shuttered their really interesting low power integrated CPU module business (Joule, Galileo, Edison)



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Summary

- SDR world offers more variables now than ever before
- Platform variables/options are numerous, making objective comparisons challenging
- This is just the tip of the iceberg, but it is a start...

- Let's look at some concrete examples

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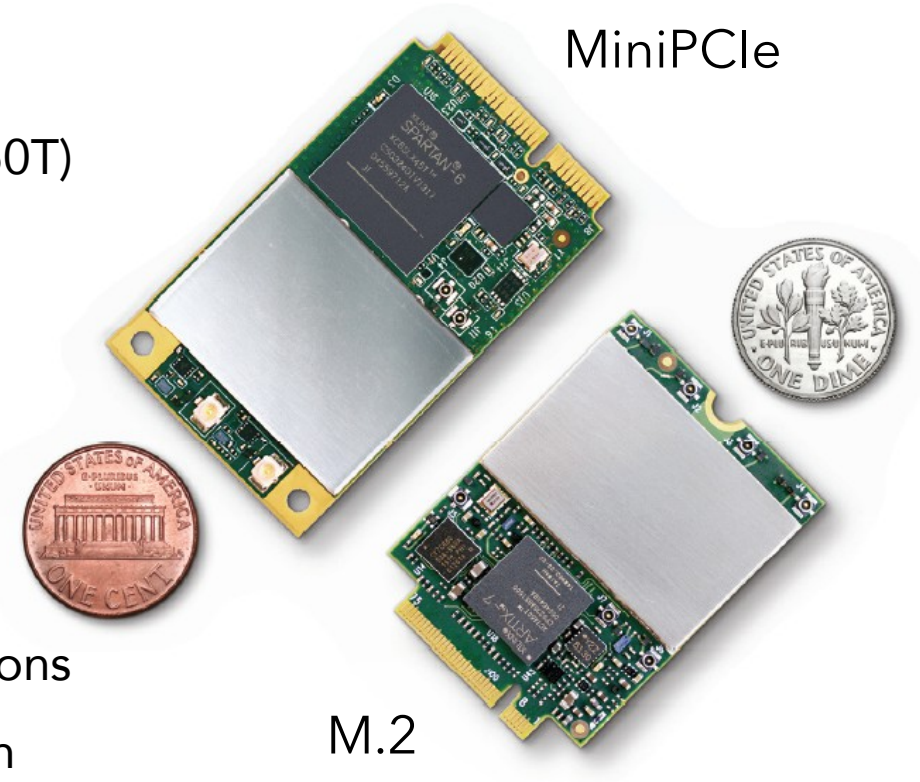
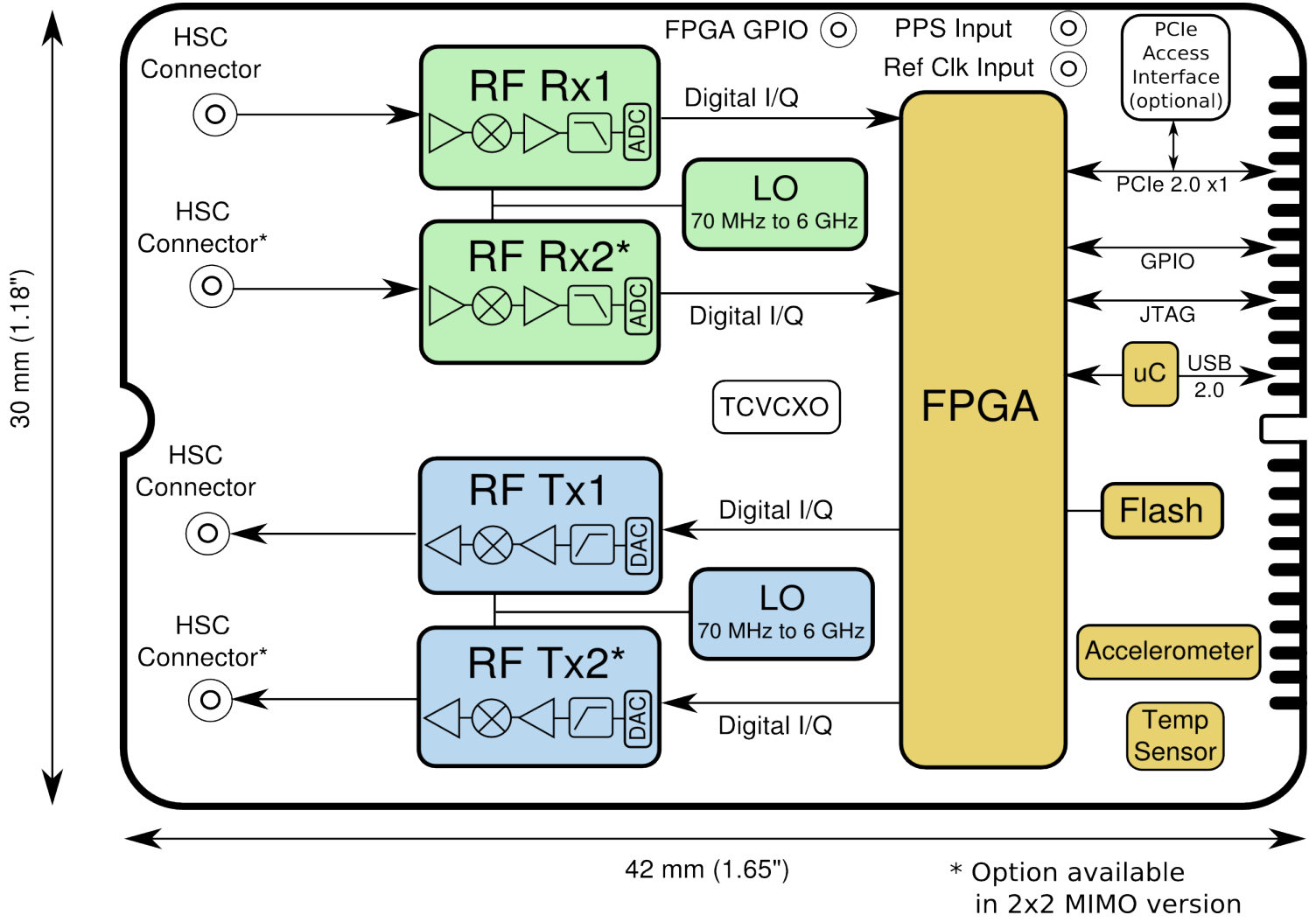
Sidekiq M.2

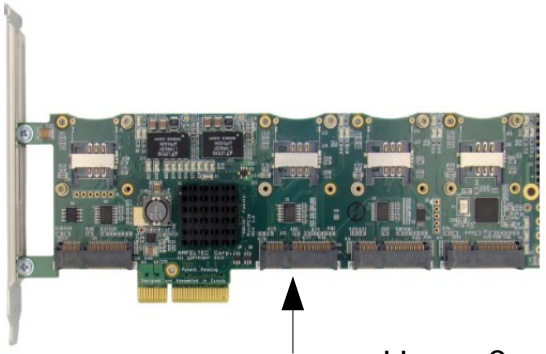
- Form Factor: Standard M.2 3042 card
- 30mm x42mm x 4mm
- AD9361 RFIC + Xilinx Artix 7 FPGA (XC7A50T)
- RF Tuning Range: 70 MHz – 6 GHz
- 2x2 MIMO capable transceiver
- Data Converters: Between 200 Ksps and 61.44 Msps
- Interface: Gen2 PCIe x1 interface to host
- External PPS and reference clock input options
- Typical power consumption: 2W (application dependent)
- Supported by libsidekiq API and gr-sidekiq



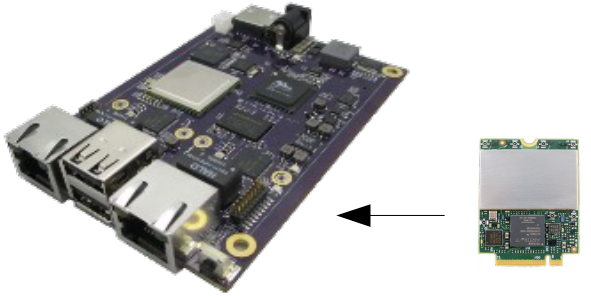
Sidekiq M.2 block diagram



Sidekiq Deployment Options



Up to 8 cards

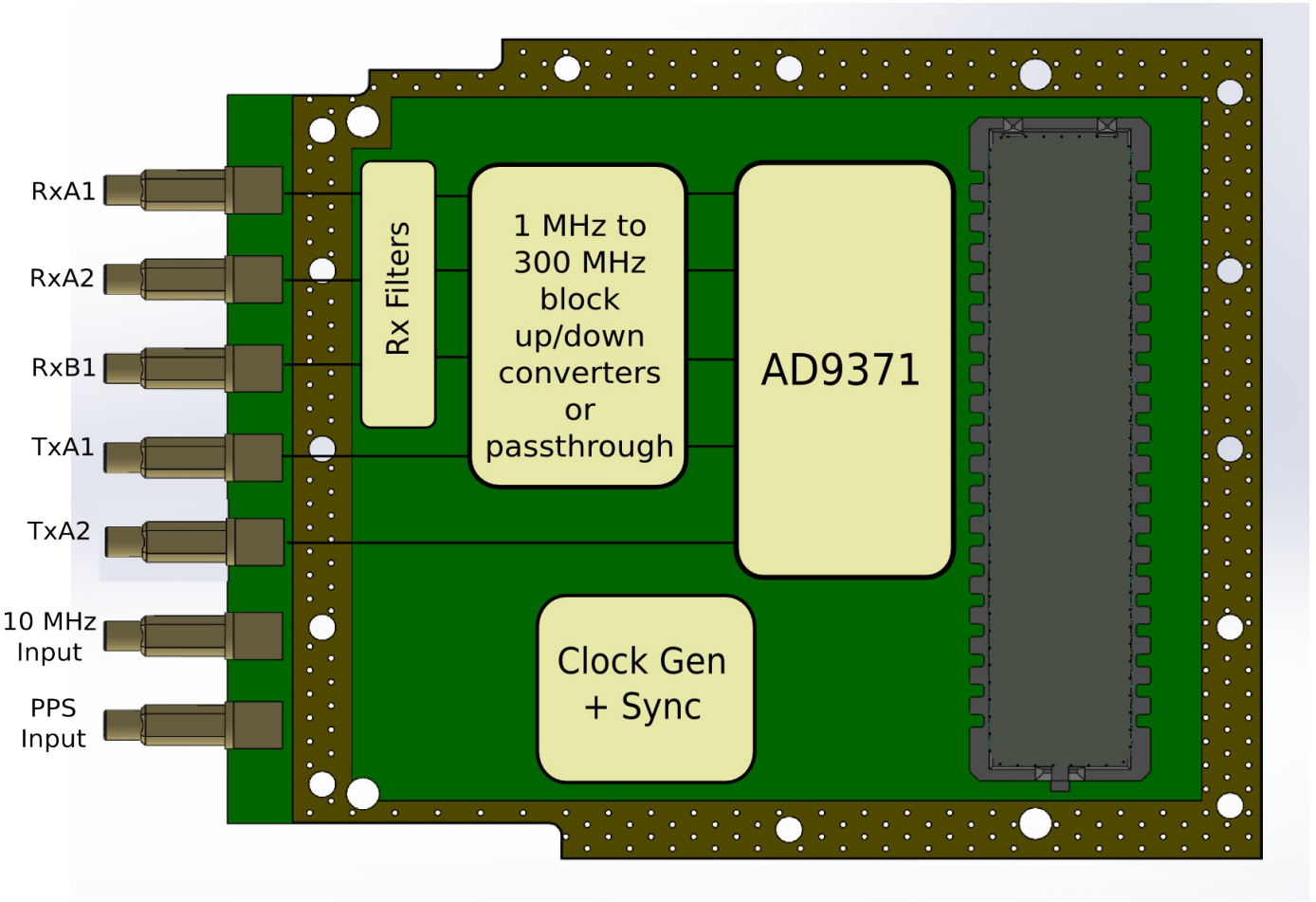


Up to 6 cards

Sidekiq X2

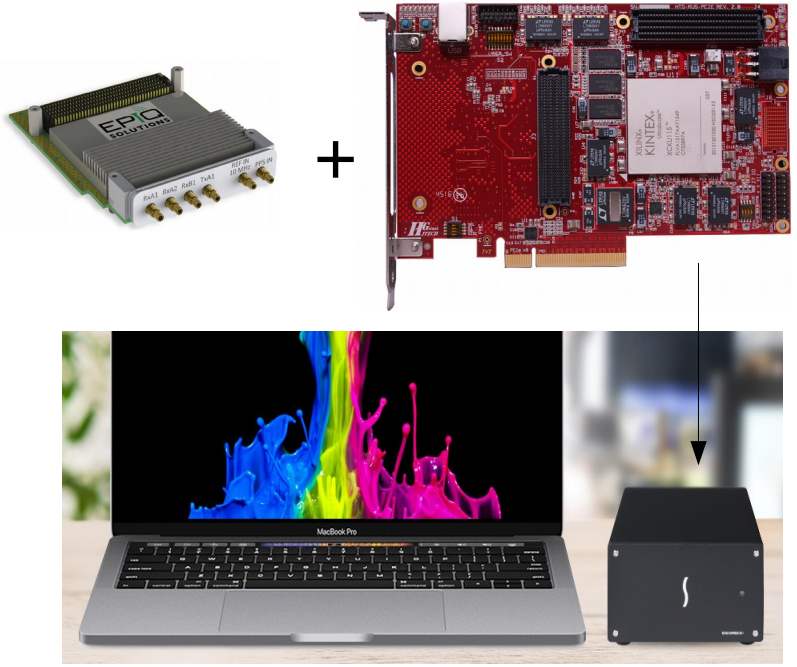
- Form Factor: VITA 57.1 FMC card form factor
- 84mm x 69mm x 8.5mm
- Based on Analog Devices' AD9371 RFIC
- RF Tuning Range: 1 MHz to 6 GHz
- Multiple RF interfaces
  - Phase coherent Rx pair (common LO)
  - Third independently tunable Rx
  - Phase coherent Tx pair
- Data Converters: 16-bit A/D, 14-bit D/A
- Up to 100 MHz RF bandwidth per channe
- Integrated Rx pre-select filters
- 10 MHz + PPS input on front panel
- Power consumption: 4W – 10W (application dependent)
- Supported by libsidekiq API and gr-sidekiq

Sidekiq X2 Block Diagram

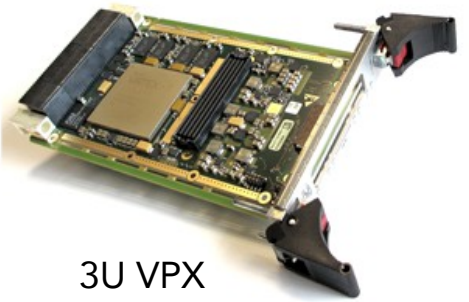


Sidekiq X2 Deployment Options

- Sidekiq X2 Thunderbolt 3 Platform
  - Interface: FMC PCIe carrier card with Xilinx Kintex Ultrascale KCU060 FPGA
    - 726K LEs, 2760 DSP slices, 38 Mb BRAM
  - Thunderbolt3 Chassis for PCIe carrier
  - PCIe Gen3 x4 interface to host laptop/NUC/desktop PC replaces 10 GbE
    - Low latency PCIe
    - DMA directly to host system memory
    - 122.88 Msamples/sec * 4 bytes/sample * 3 Rx channels = ~1500 MB/sec (12 Gbits/sec)
- 3U VPX carrier card
  - Xilinx Zynq Ultrascale+ ZU9EG (quad-core ARM + FPGA)
    - 600K LEs, 2520 DSP slices, 32 Mb BRAM
  - 4 GB DDR4 RAM
  - Supports conduction and convection cooled options



Thunderbolt 3



3U VPX

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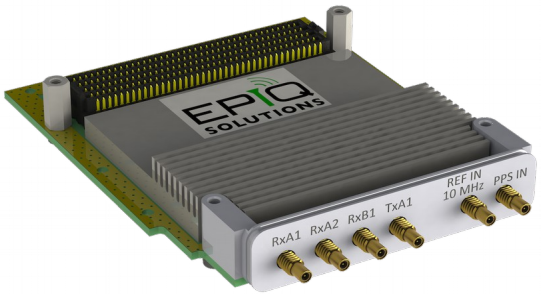
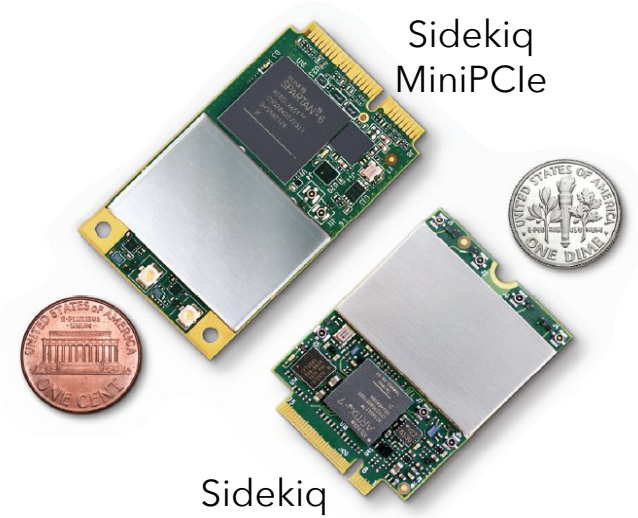


Sidekiq X2

Questions?

THANK YOU!



Sidekiq MiniPCIe

Sidekiq M2

Maveriq

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Matchstiq Sx0

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