RF System Synchronization – Baseband

- Daniel Jepson – SDR Group Manager, National Instruments

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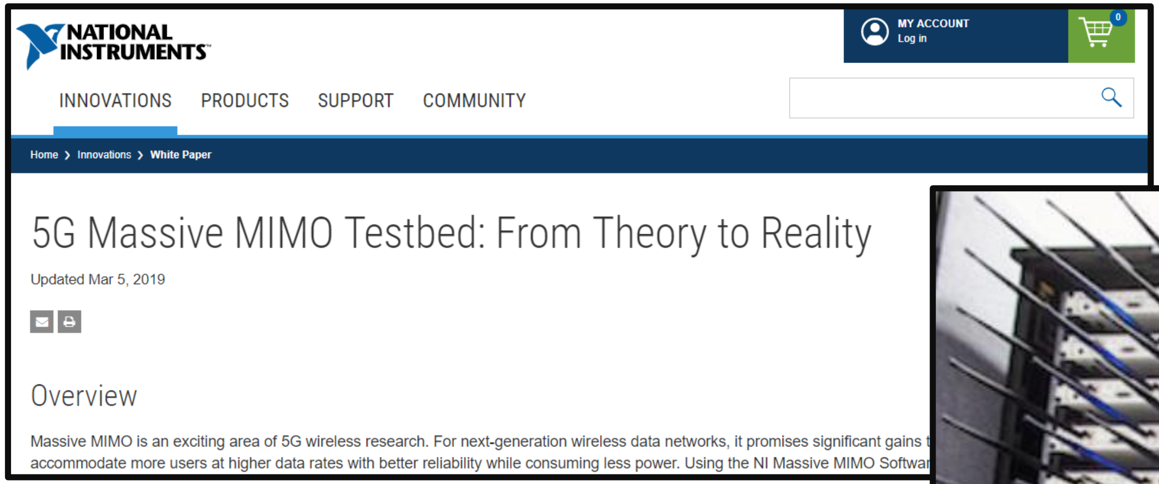
RF Systems: Baseband

Application for Baseband Synchronization



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5G Massive MIMO Testbed: From Theory to Reality

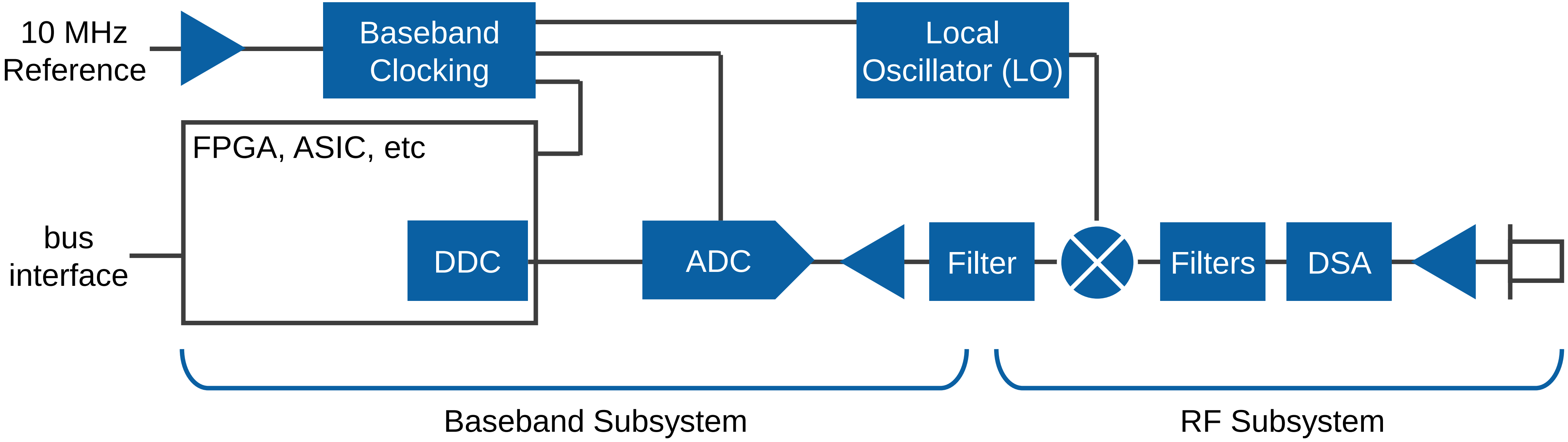
Updated Mar 5, 2019

Overview

Massive MIMO is an exciting area of 5G wireless research. For next-generation wireless data networks, it promises significant gains t
accommodate more users at higher data rates with better reliability while consuming less power. Using the NI Massive MIMO Softwar

http://www.ni.com/en-us/innovations/white-papers/14/5g-massive-mimo-testbed--from-theory-to-reality--.html

Typical SDR Device



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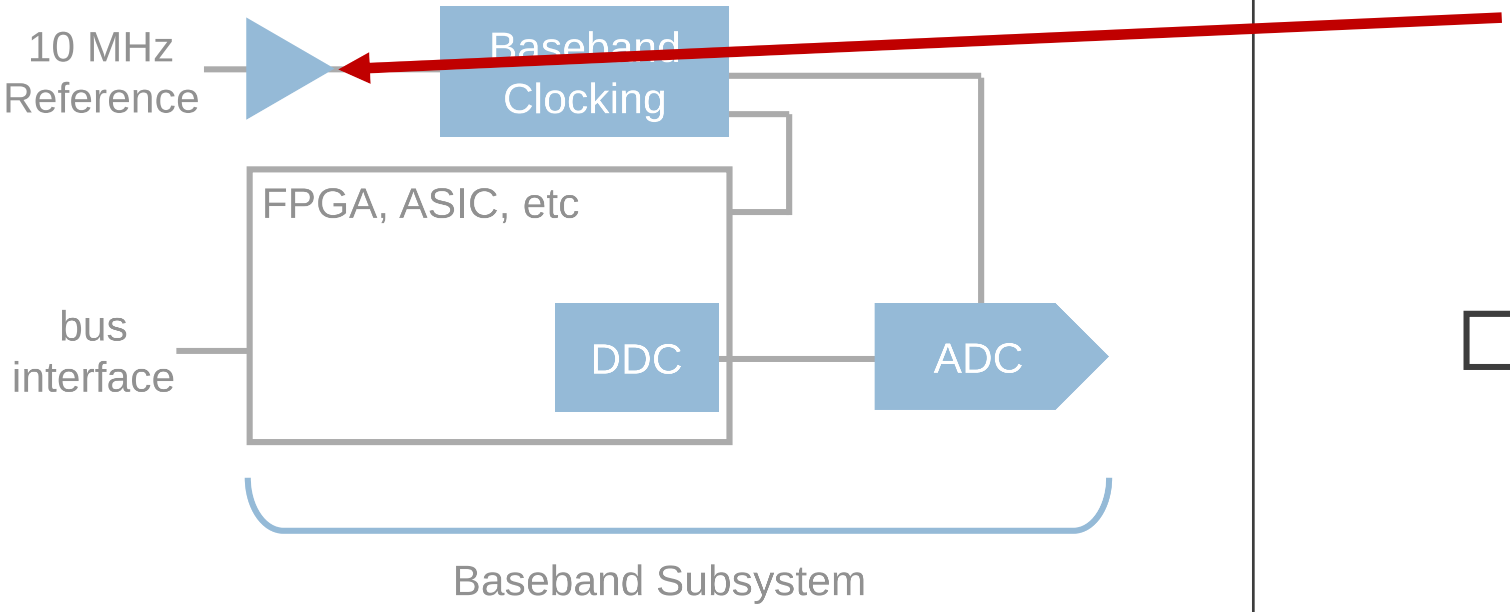
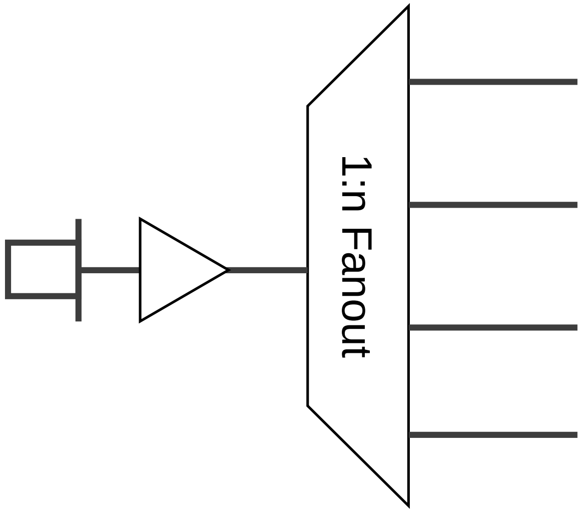


Reference Clock
Input & Fanout



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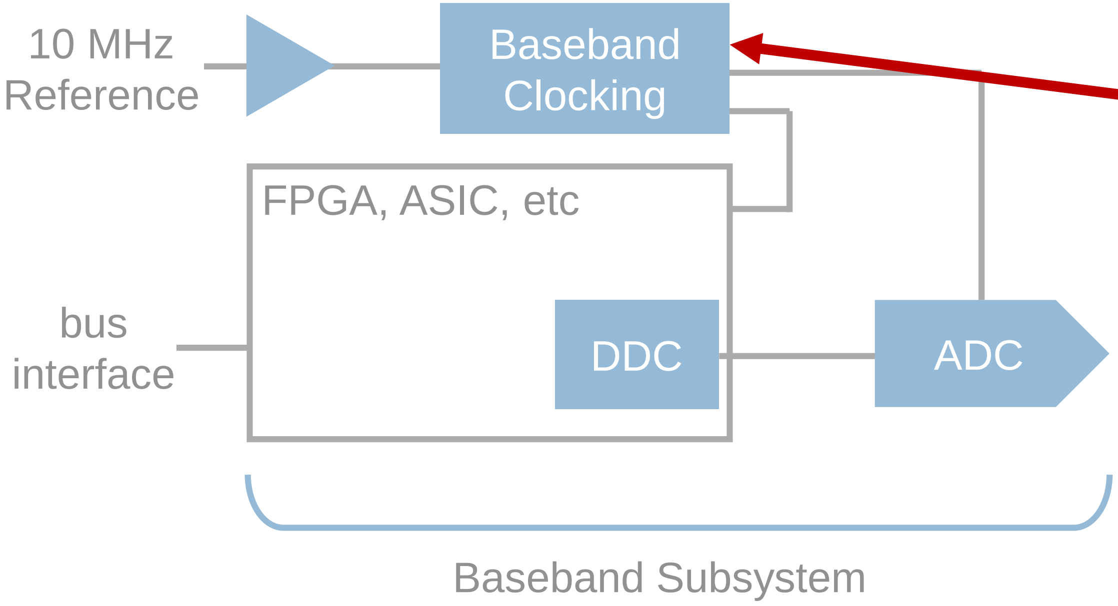
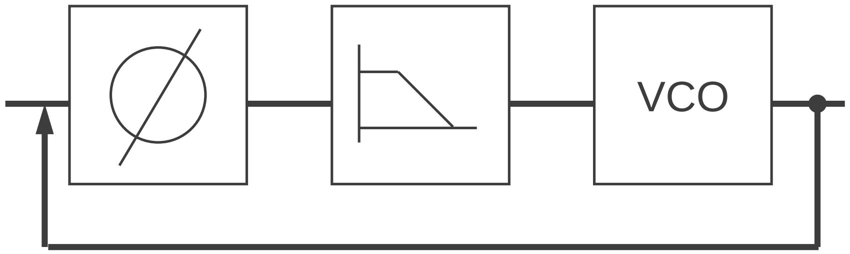


Converter Clock PLL



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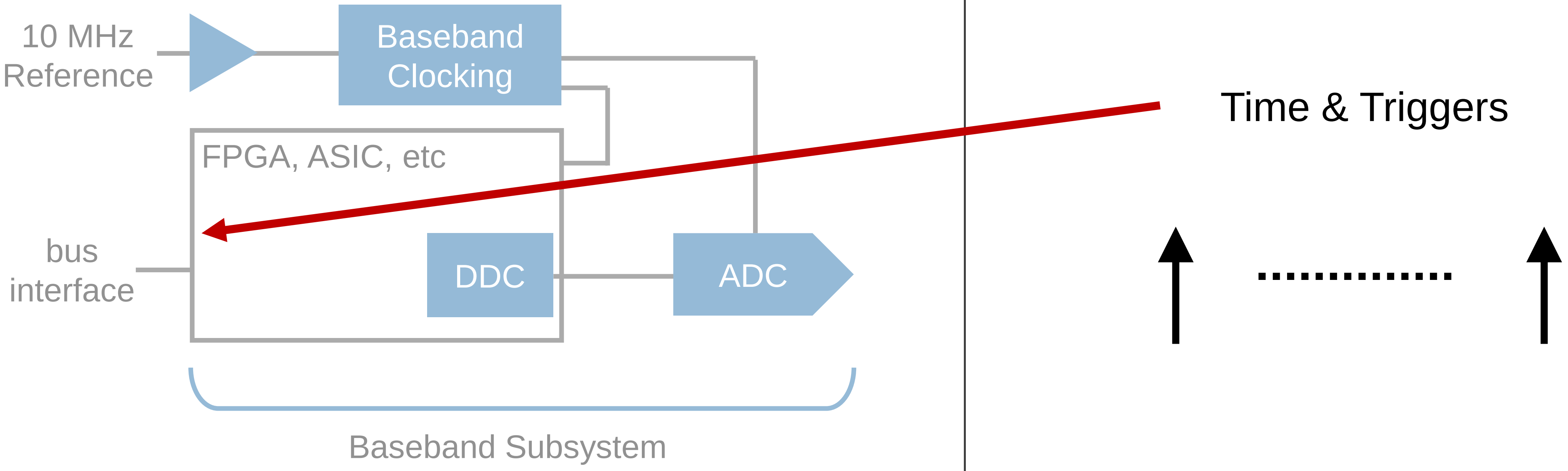


Building a Synchronized System

The Basics

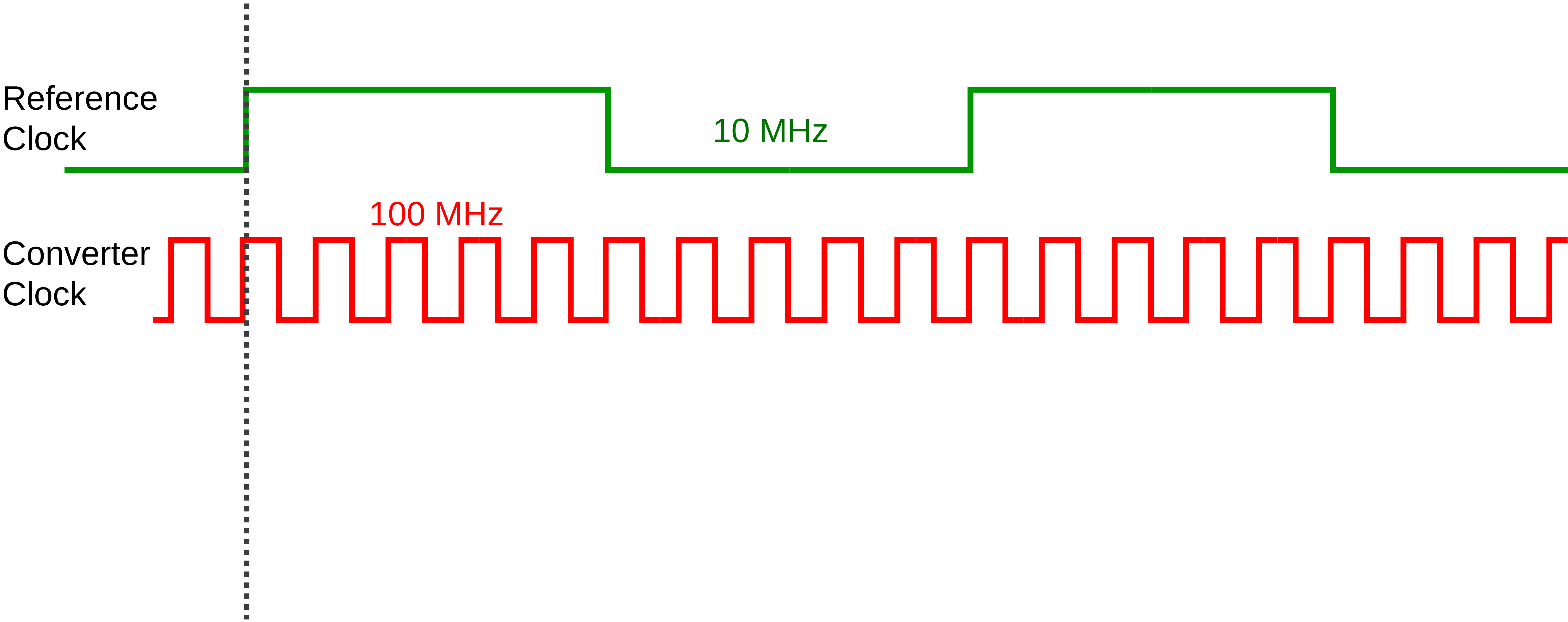
- Start with a single device and maybe even a single channel

Reference Clock

Host Computer

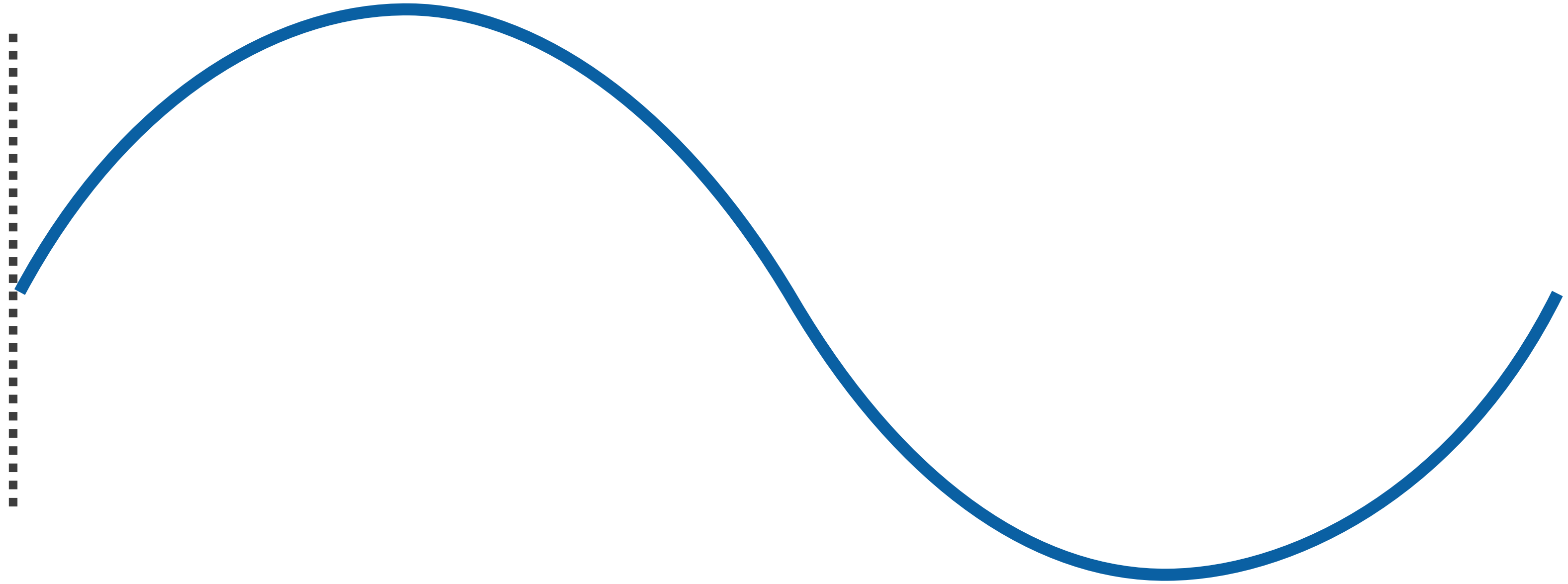
RF Signal

“Viewing” Synchronization: the Clocks

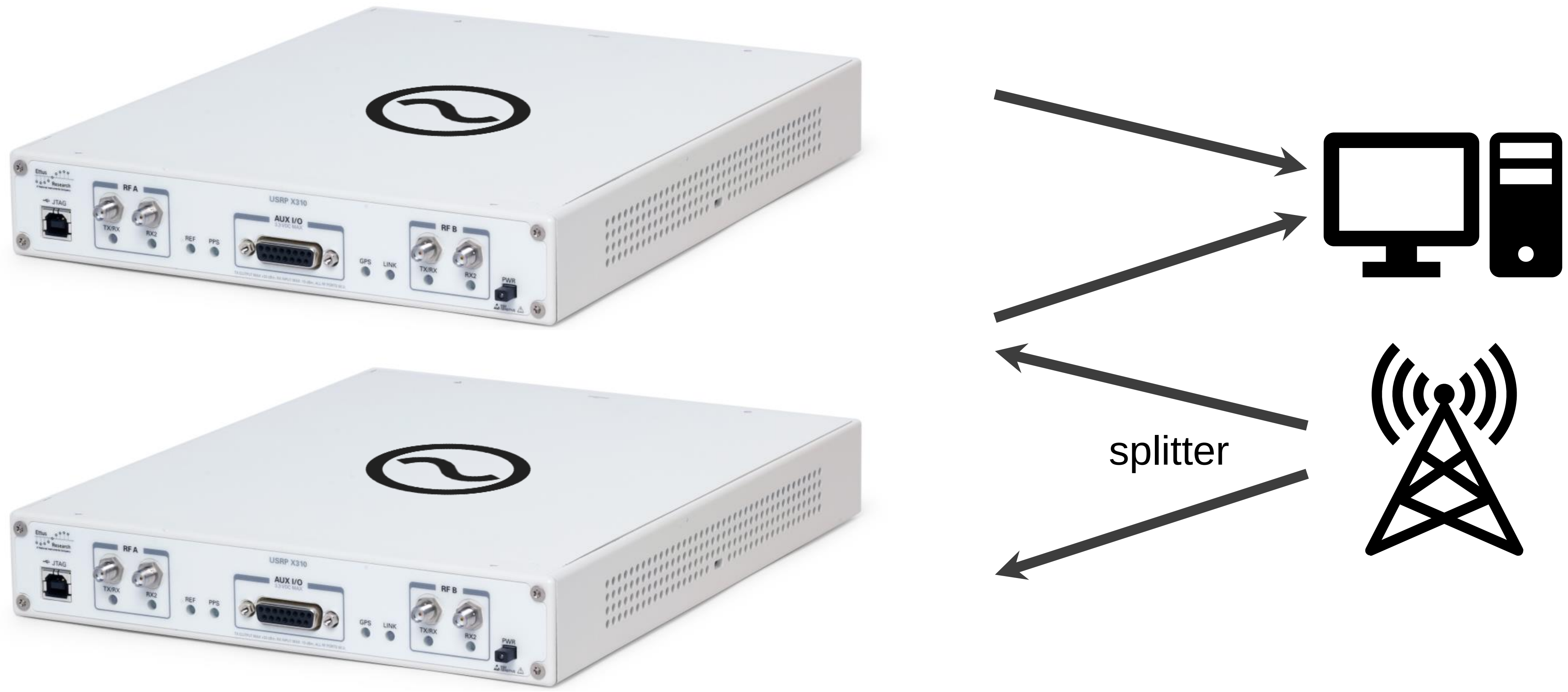


“Viewing” Synchronization: the Data

Baseband
RF Signal



Increasing Device Count



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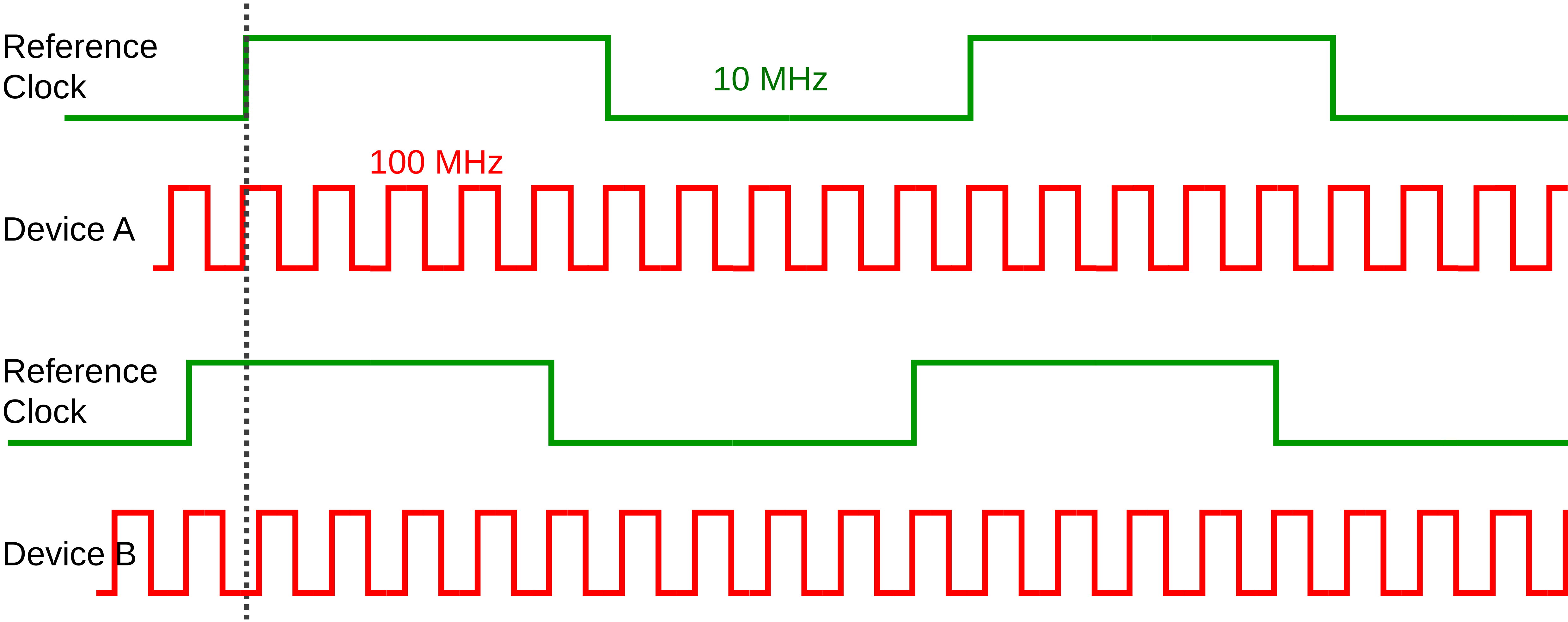
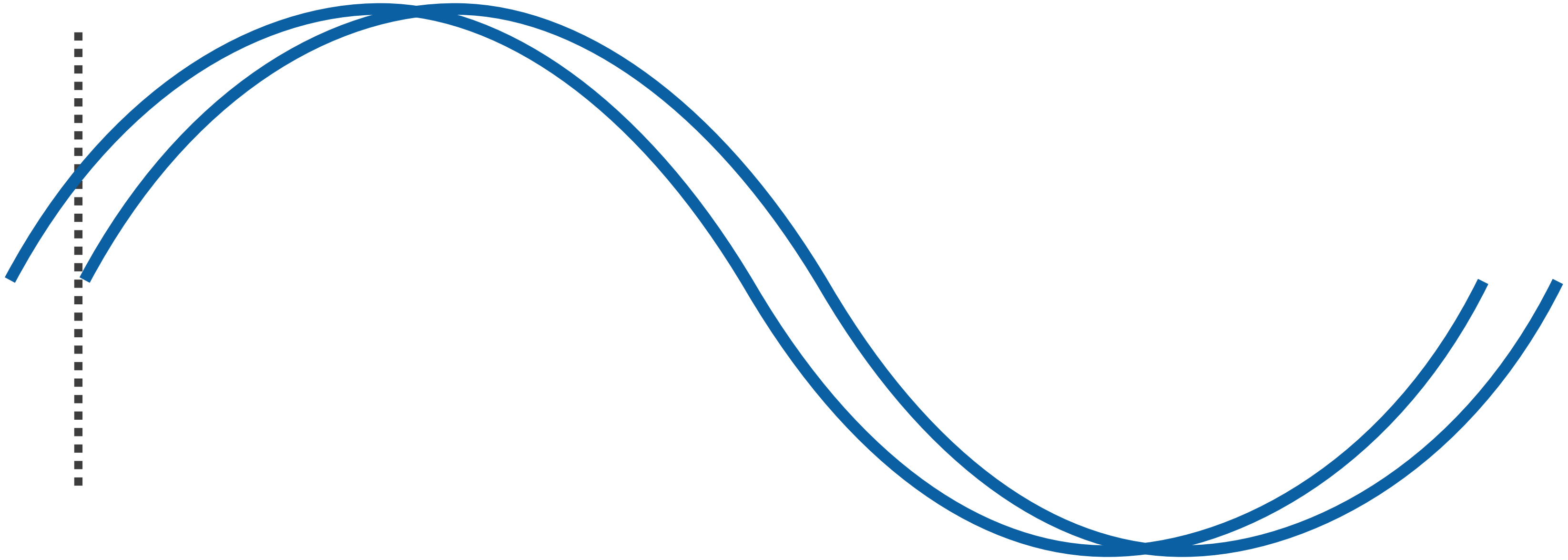
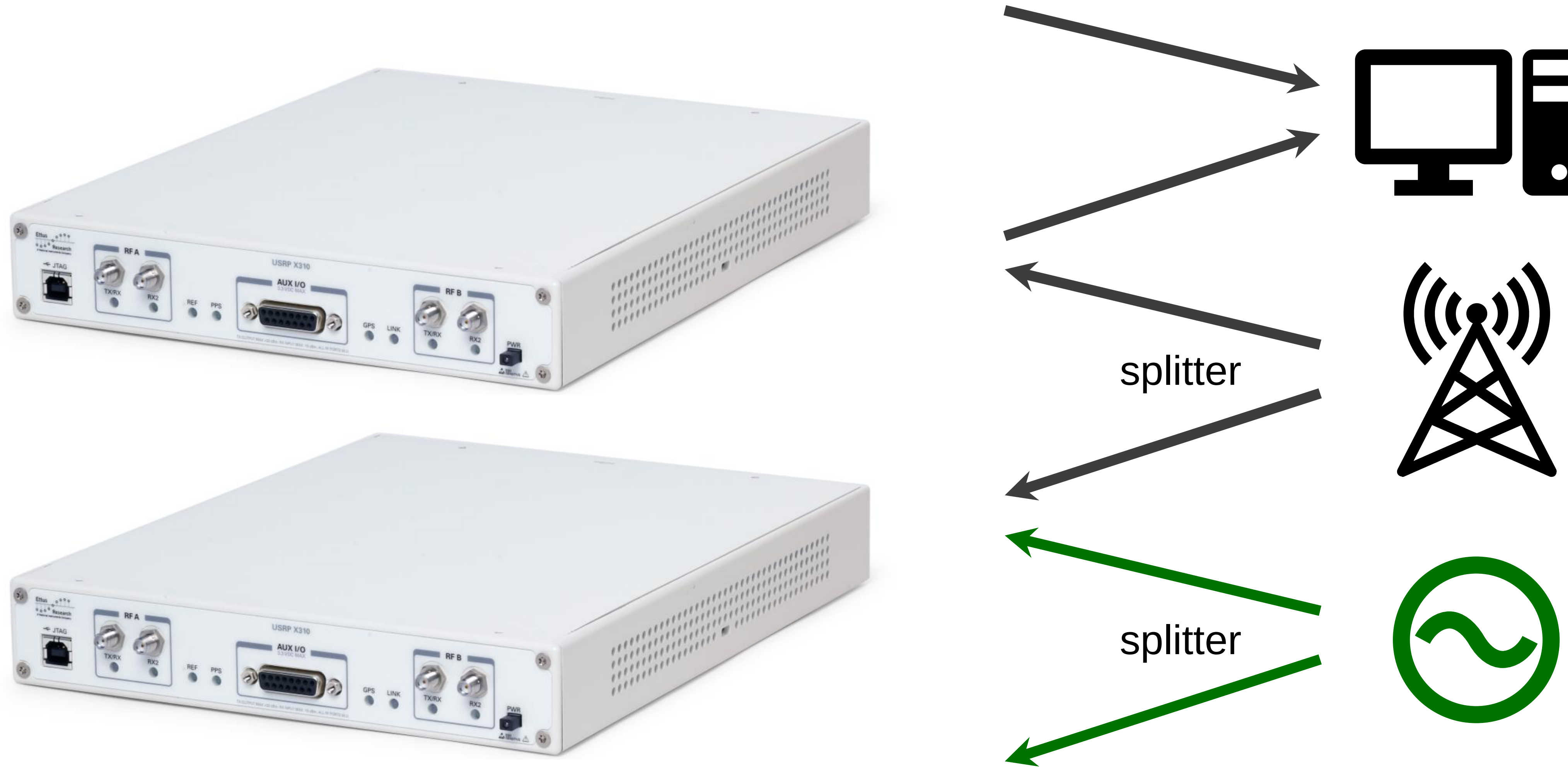


Increasing Device Count

Baseband
RF Signals



Shared Reference Clocks



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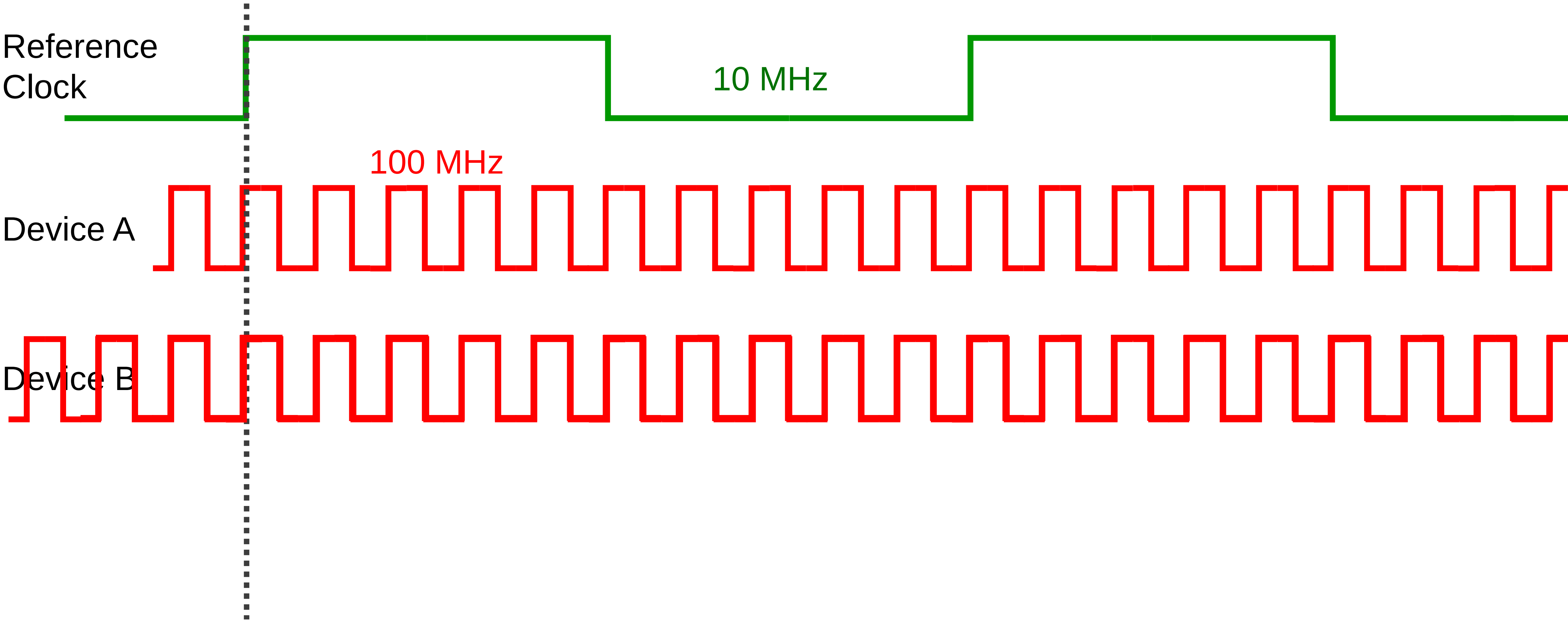
Shared Reference Clocks



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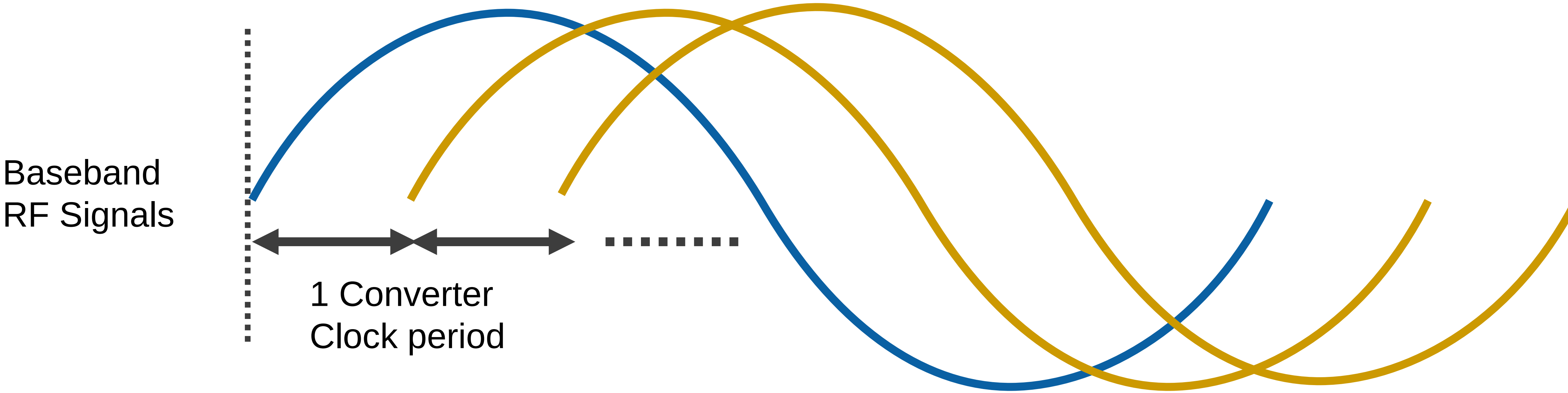
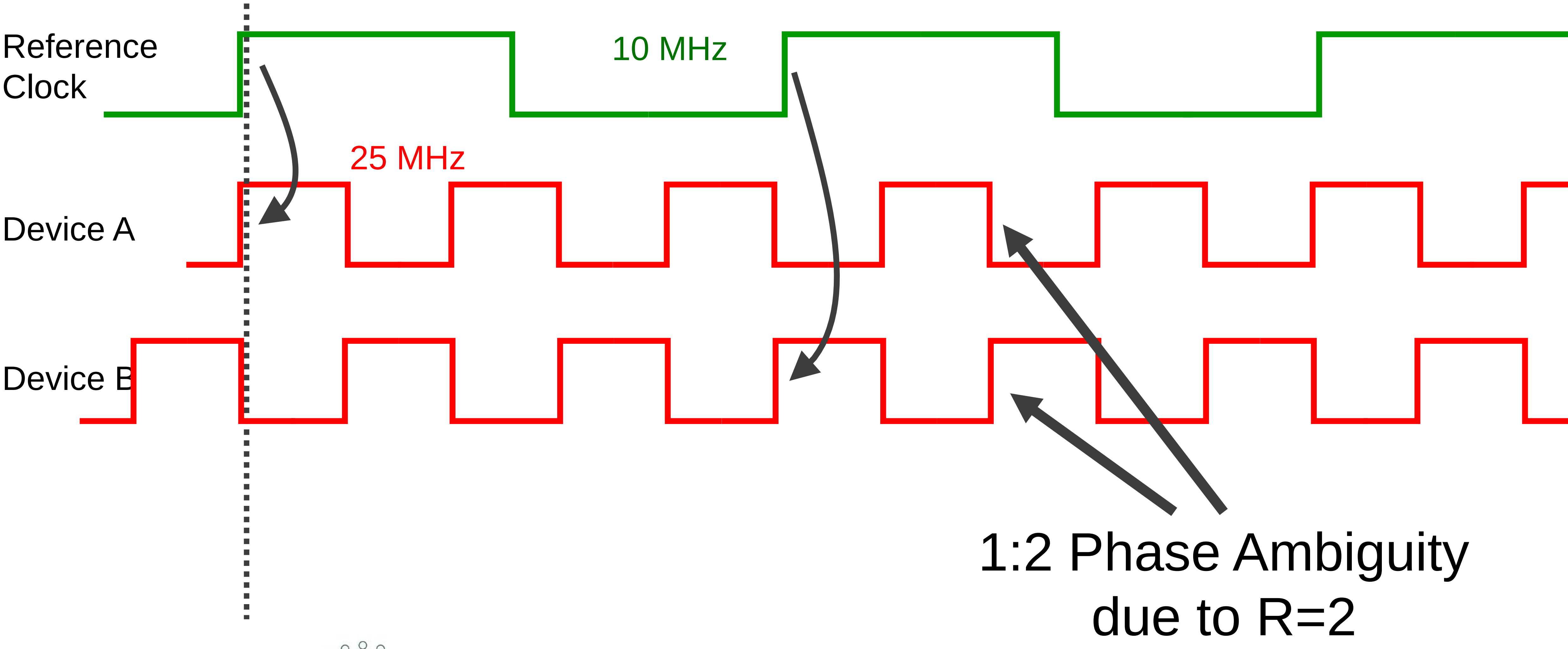


Unrelated Clock Rates



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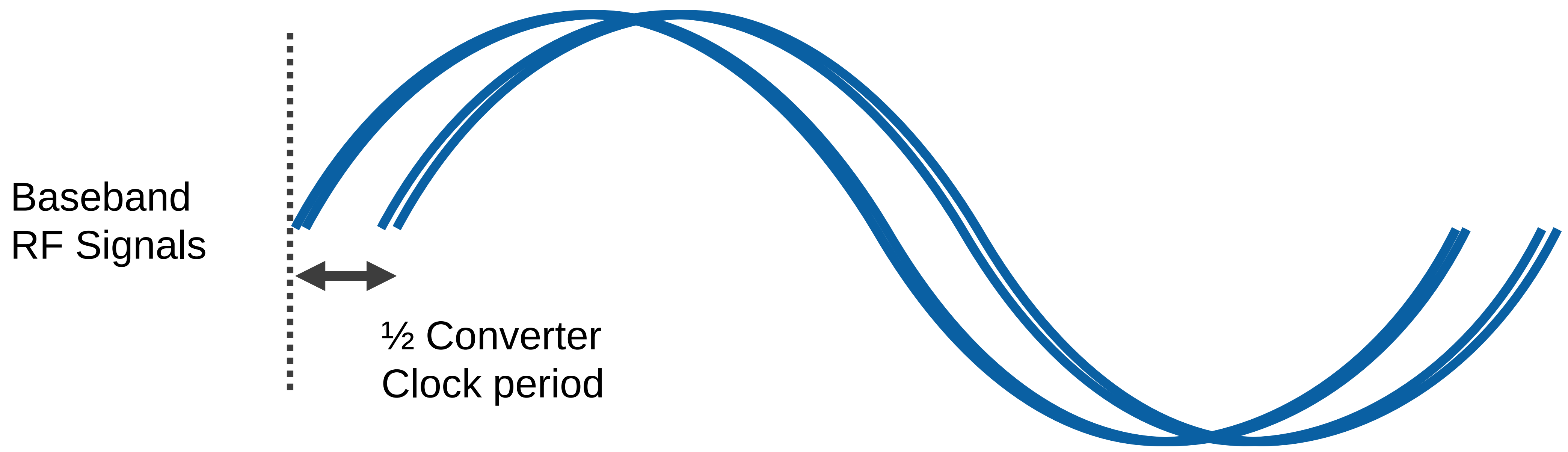


Number of Quantization Steps = R divider value

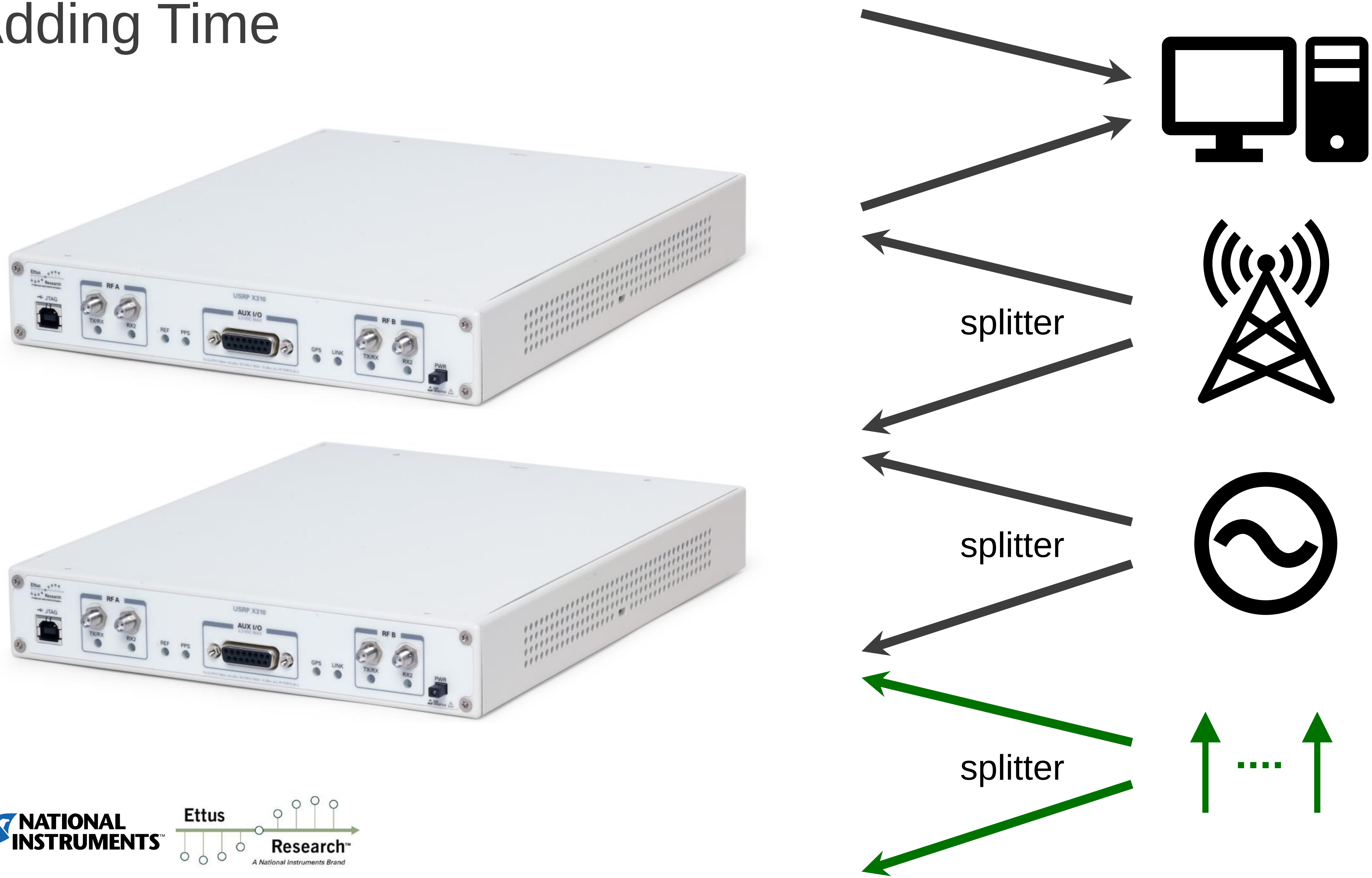
PPS for Time Coherence

- Pulse per Second: identifies a single Reference Clock edge on all devices

- Allows multiple devices using the same Reference Clock to align themselves to a common “timebase”.

- Used for PLL resets, timekeeper alignment, and acquisition start/stop.

Adding Time



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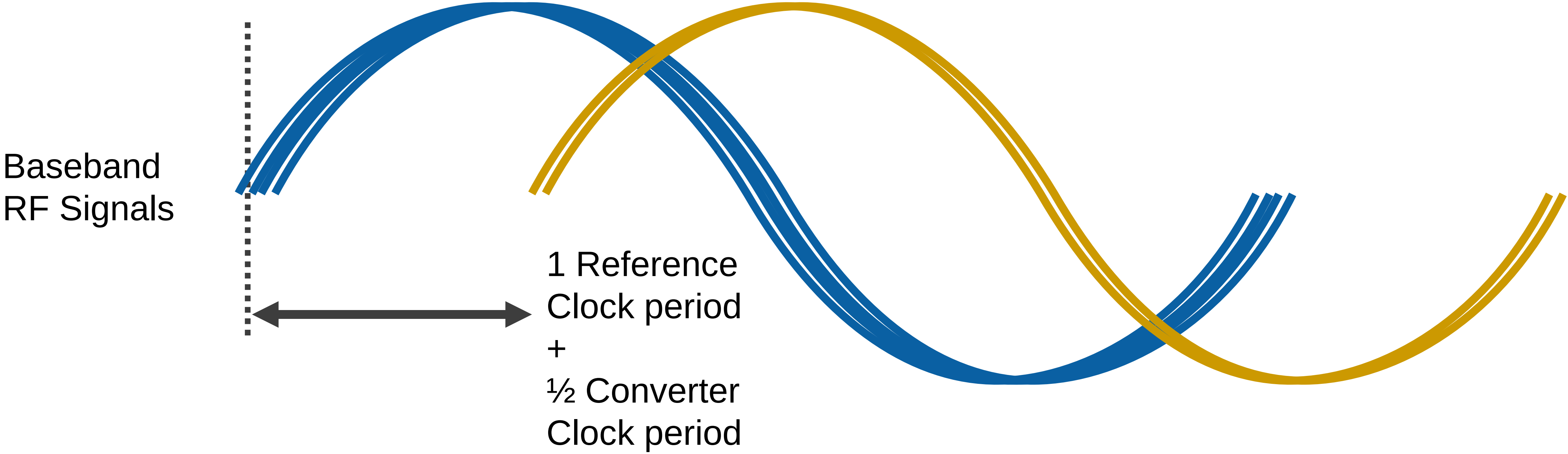
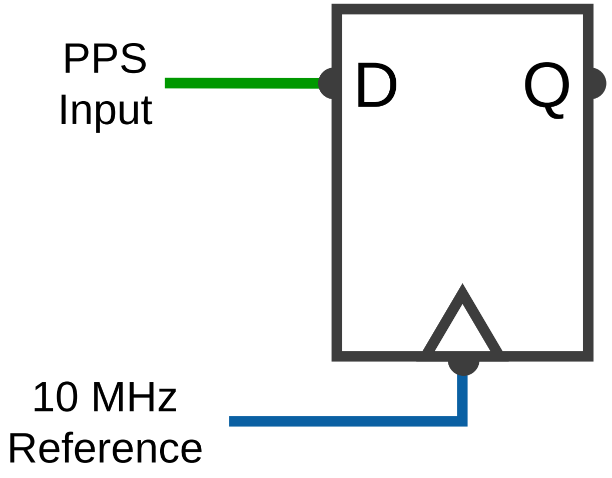
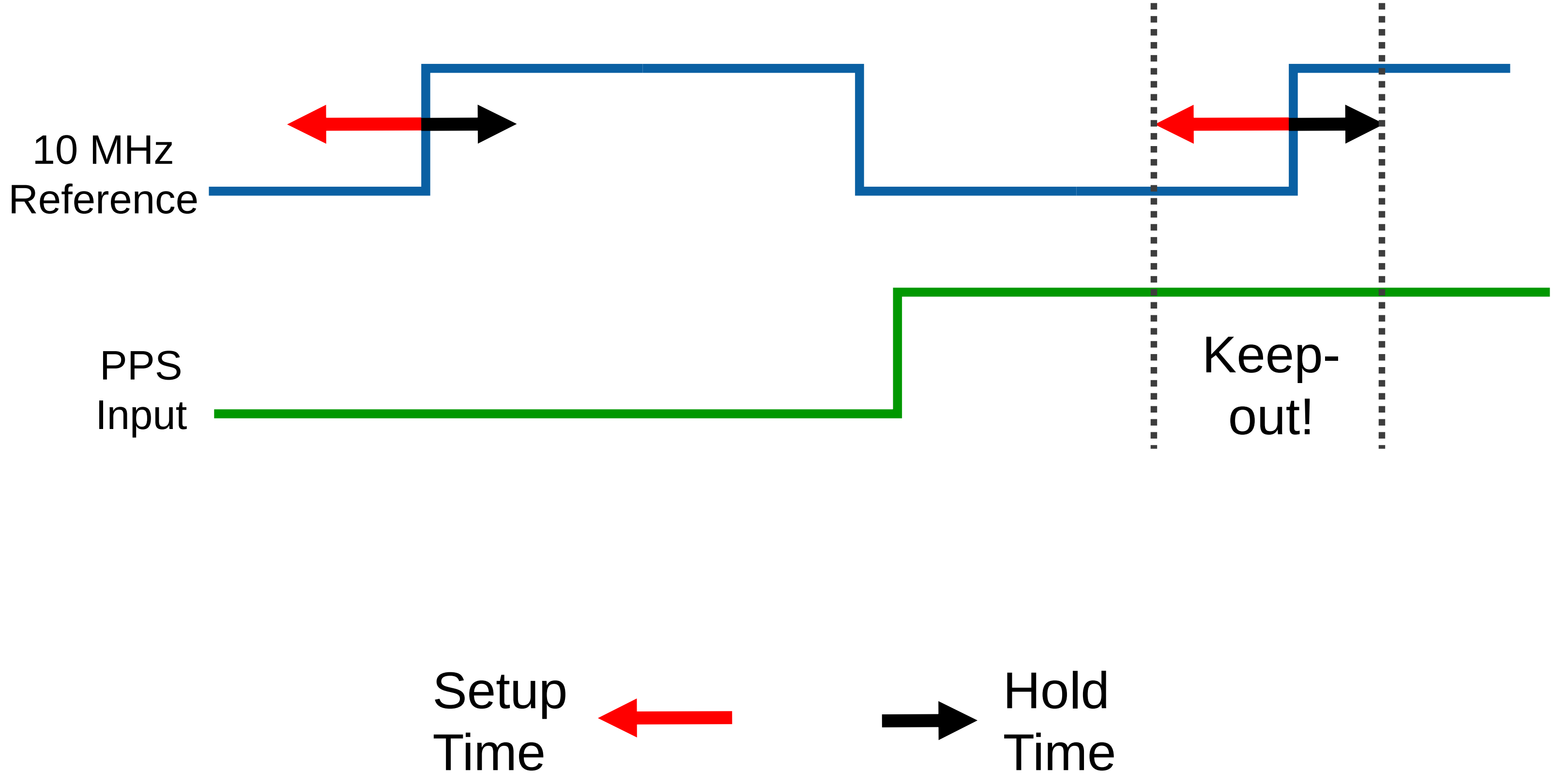
Adding Time

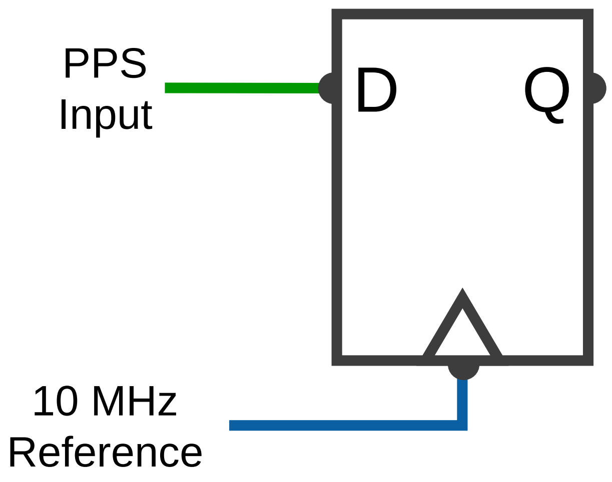

Baseband
RF Signals
1 Reference
Clock period
+
½ Converter
Clock period

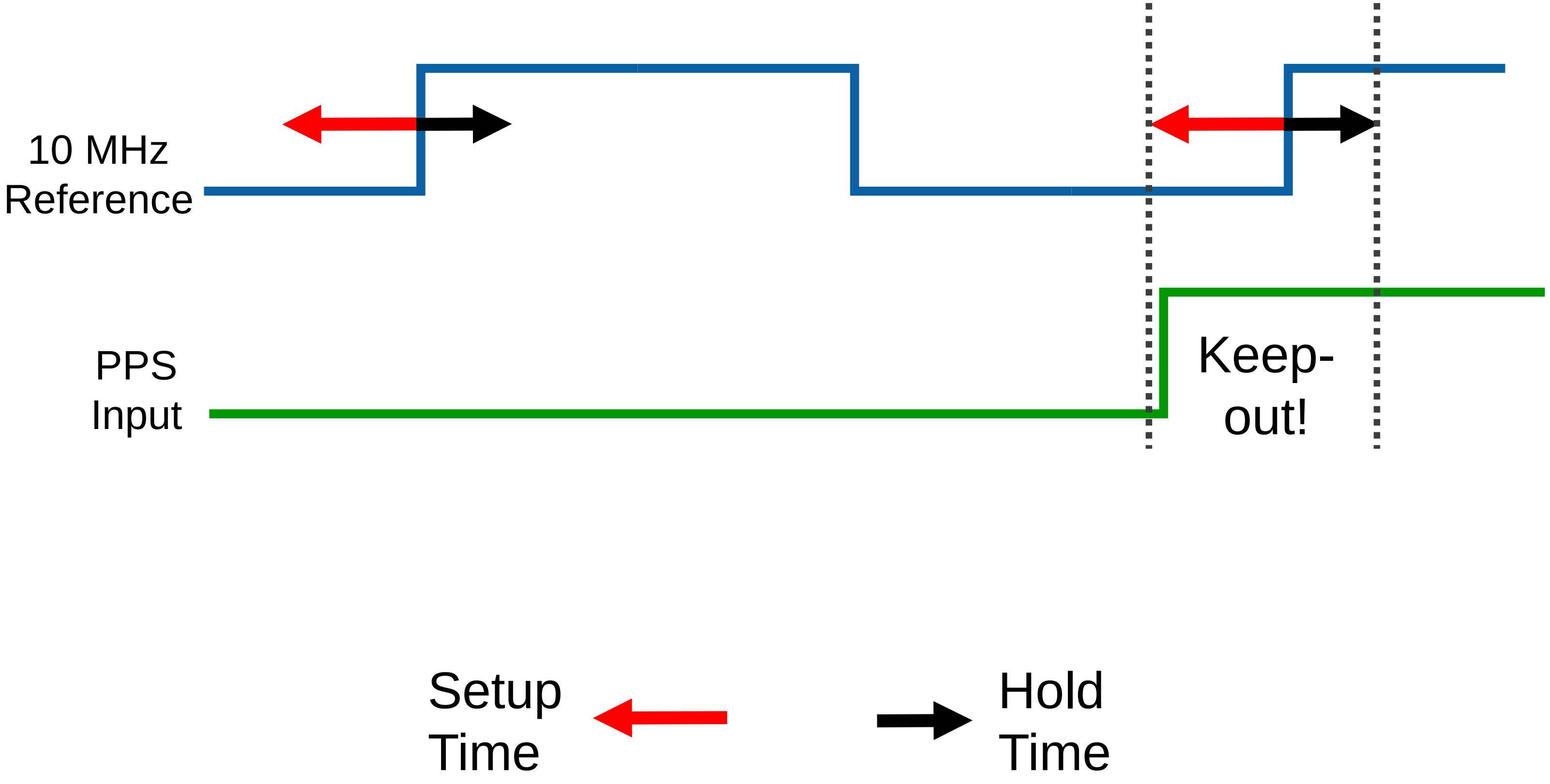
Closing Timing





Closing Timing





Timing with the PPS

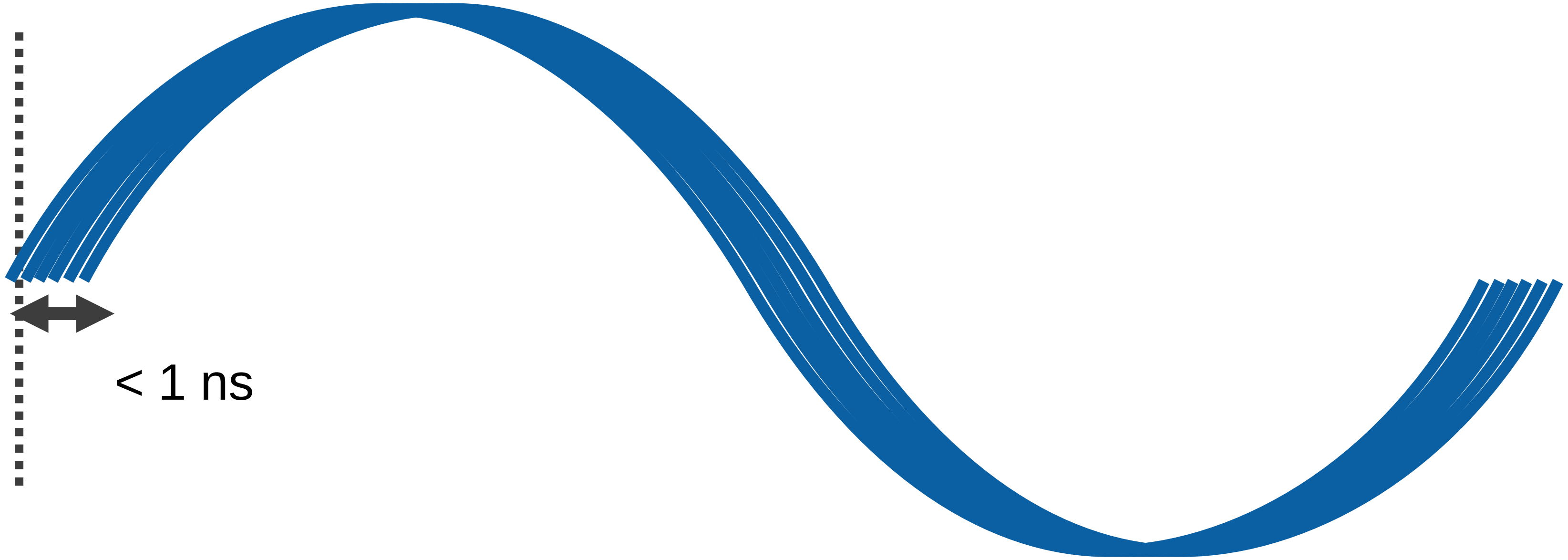
- Timing between PPS and the Reference Clock must be closed at the FPGA or ASIC used to control the device

- Published numbers may exist on the setup and hold time required for the PPS with respect to the Reference Clock at the ports of the SDR equipment

- Practical Implementation Pitfalls:
  - PPS should be driven from the same clock domain that receives it
  - Match the cable lengths of the clock and PPS to each SDR device as closely as possible
  - Use the same topology (star or daisy-chained) for all devices

Cleaning Up

Baseband
RF Signals



Further Considerations

- Devices should be at a constant (or identical) temperature
  - Buffers and board traces have different propagation delays
  - PLLs (for the converters and LOs) tend to drift

- Close timing between PPS & Reference Clock into the device, but also close timing at your PLL for the reset pulse

- Remember to account for variations in your Reference Clock distribution and generation device, which directly contributes to your overall uncertainty

Geographically Distributed Systems

Very, Very Long Cables

- Practically only work up to a few meters long
- Changes in temperature and bend radius of the cable affect the time delay through it
- All devices must have length-matched cables

GPS

- Once locked to a satellite, the reference clocks will align world-wide
- Alignment is typically poor compared to cabled synchronization; expect 10s of nanoseconds
- Local clocks inherit the accuracy of the satellite's oscillator

White Rabbit

- Ethernet-based synchronization protocol using optical cables and specialized transceivers up to 10 km
- Extension of the IEEE 1588 PTP for time references
- Synchronous Ethernet (SyncE) is used for distributing clock references
- Typical performance is better than 1 ns!

Using Ethernet-Based Synchronization on the USRP™ N3xx Devices

Contents [hide]

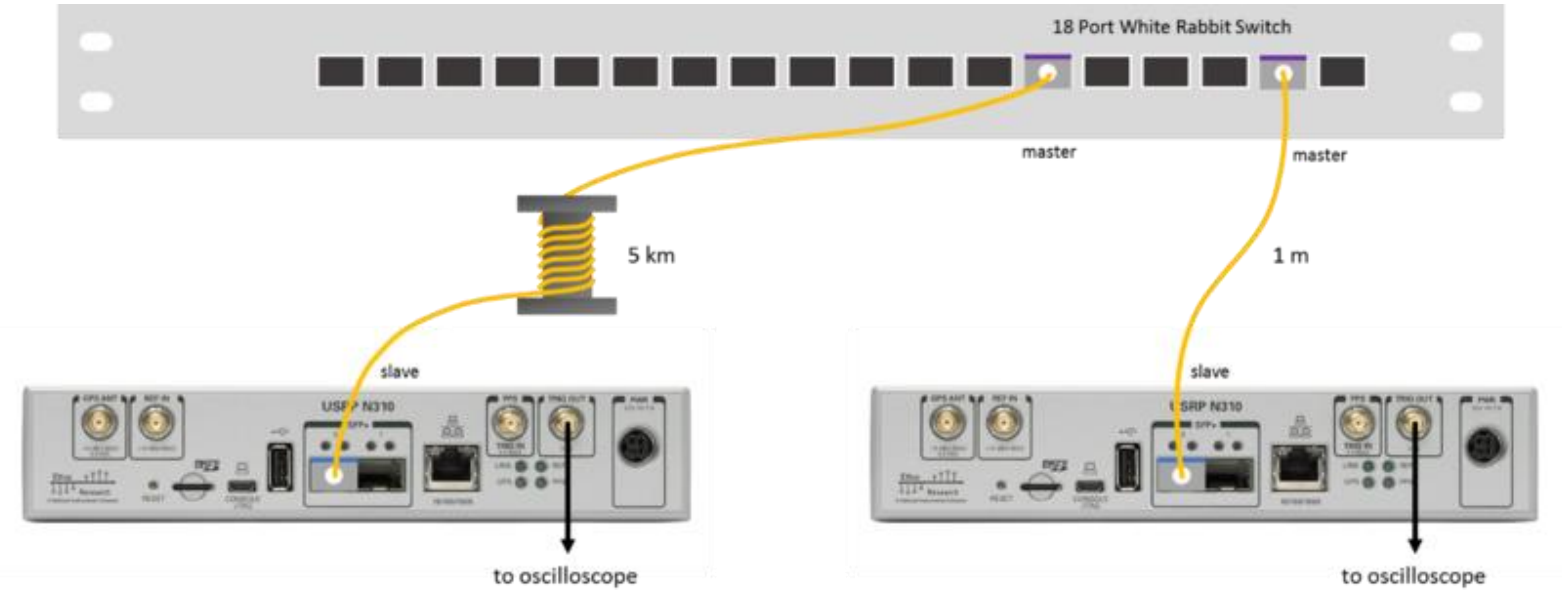
Application Note Number

AN-158

Revision History

Date	Author	Details
2018-05-01	Dan Baker, Wan Liu	Initial creation

White Rabbit System Setup



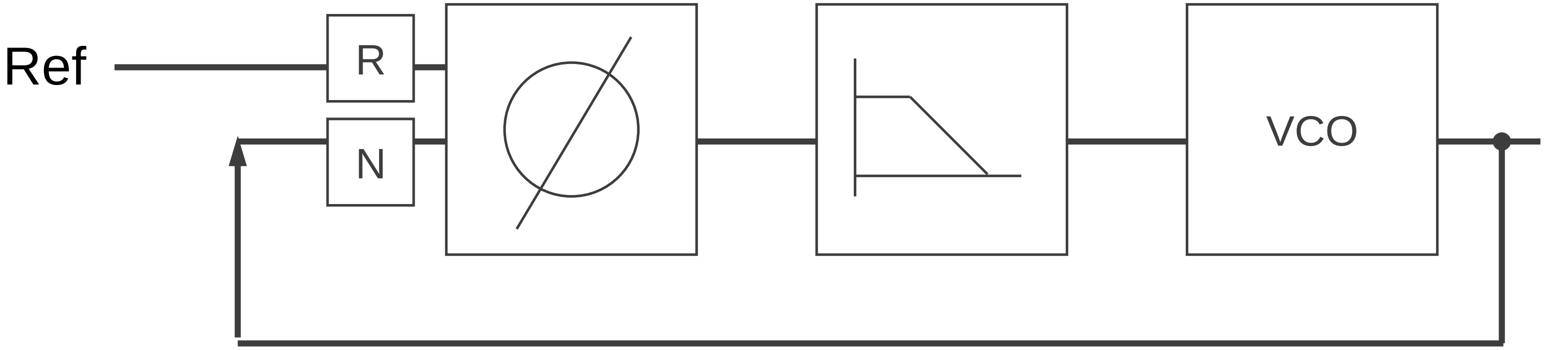
200ms alignment!

Advanced Alignment

For PLLs without an R-reset

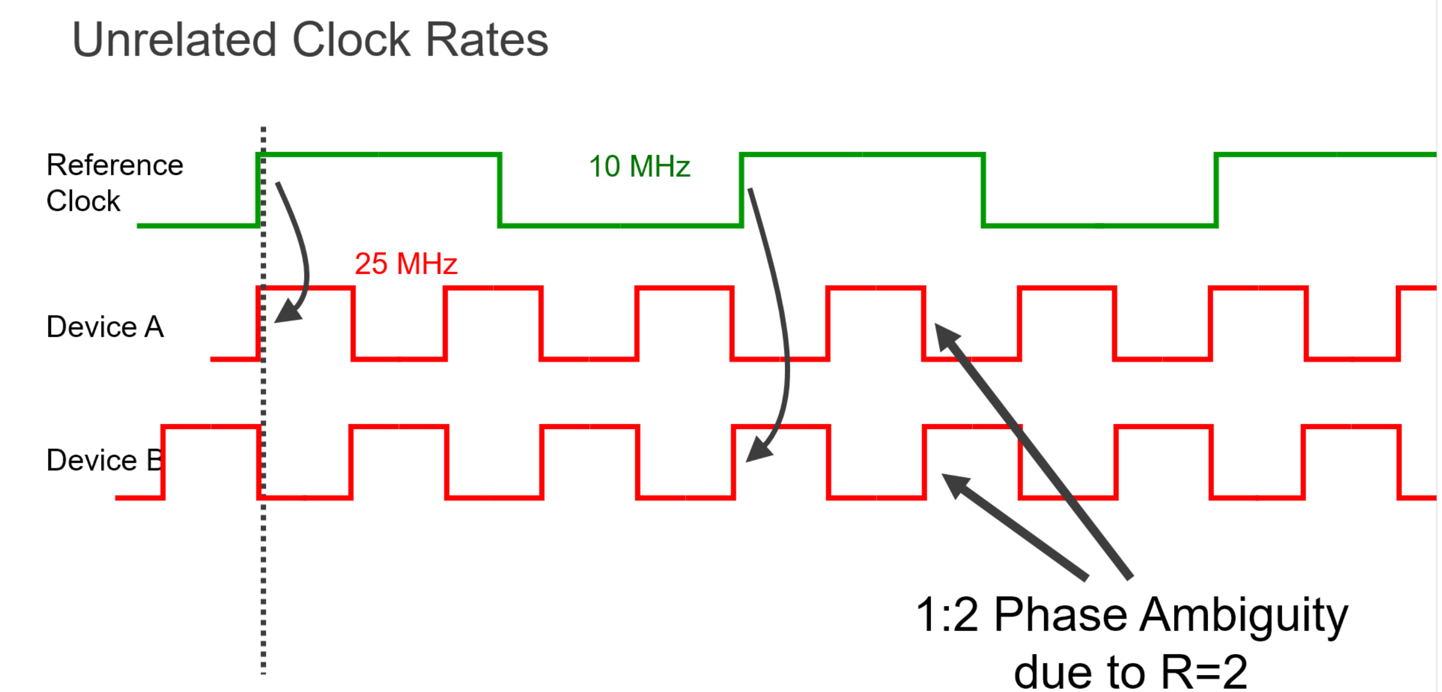
- R-divider resets allow alignment of unrelated Reference and Converter Clock rates

- Without the reset, the Converter Clock offset must be measured and compensated for externally



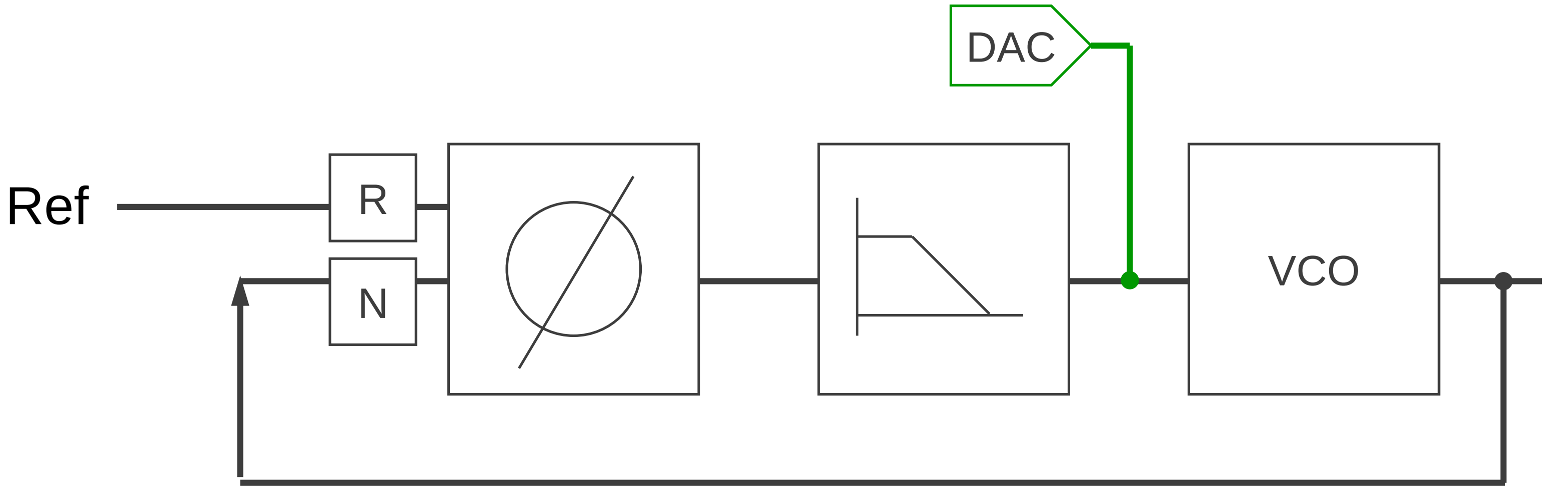
Measuring Phase Offset

- Time-to-Digital Converter
  - Create pulses in the Reference Clock and Converter clock domains
  - Measure the time between the pulses using analog or digital circuitry



Compensation Techniques

- Digitally with DSP in the signal processing chain
  - FIR filters with programmable taps based on the measured delay
- Digital clock shifting within the PLL
  - Typically VCO or ½ VCO steps
- Injecting a phase compensation offset to the VCO input
  - Allows fine resolution shifting, often at the cost of requiring calibration



Summary

Share your Reference Clock

Share a trigger (PPS) signal based on the Reference Clock

Recognize environment, equipment, and topology variables

RF System Synchronization – Baseband

- Thank you!