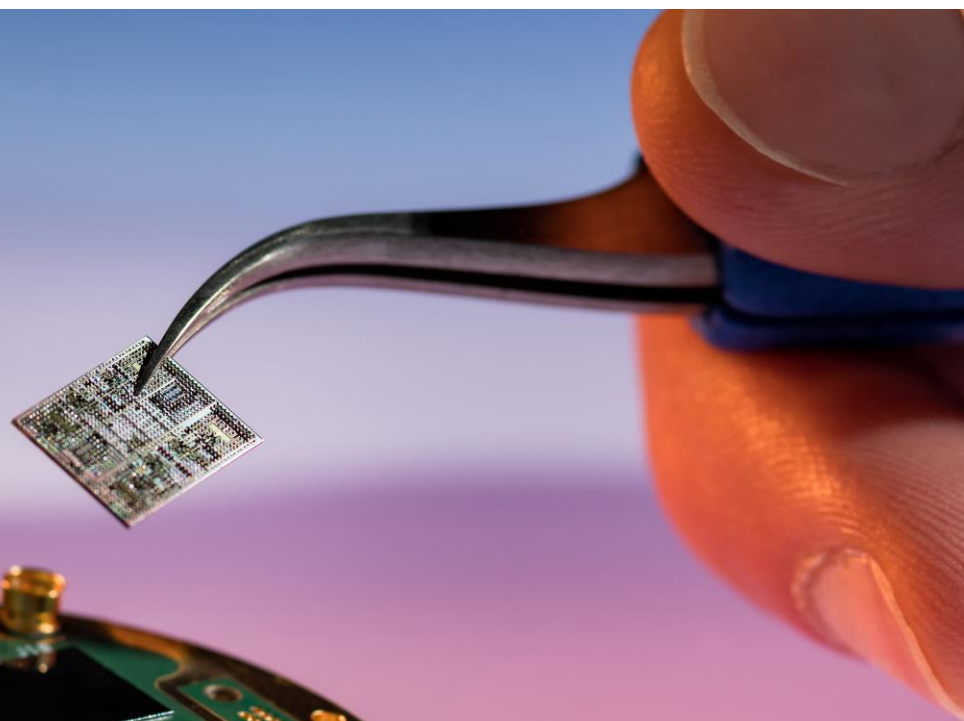


# Introduction to GNURadio on the Hedgehog SDR

*Christopher Maxey*  
BAE Systems – FAST Labs



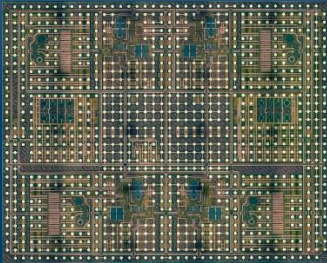
The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

09-19-2018

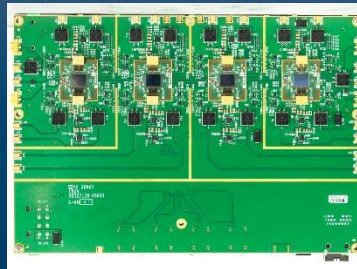
# Agenda

Intro

MATRICs RF-FPGA



Hedgehog Module



GnuRadio on  
Hedgehog



Wrap-Up





# The MATRICS RF-FPGA

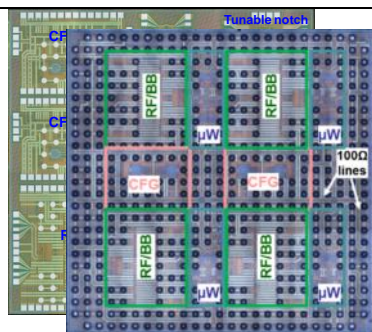
## Why use a MATRICs RF-FPGA?

- Analogous to Digital FPGA:
  - Save time and money (vs. custom RF ASIC) in low-volume applications
  - **Rapid prototyping**
  - In-field upgrades
  - On-the-fly response to environment

# MATRICs RF-FPGA IC progress

## MATRICs V1

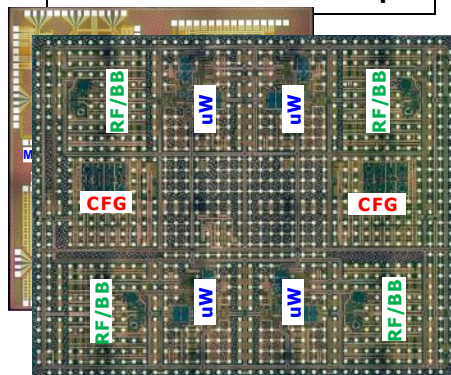
Tape-out: May 2013  
Demo Full Chip



- 1<sup>st</sup>-generation RF-FPGA
  - 10 functional blocks
  - Microwave switch fabric
  - LO distribution
- Coarse-grained reconfigurability
- DC-to-20 GHz operation
- > 80 dB RF isolation
- Tile-able layout

## MATRICs V2

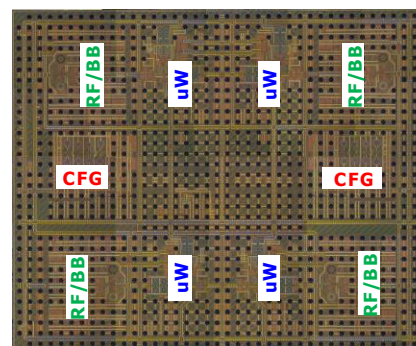
Tape-out: July 2014  
Demo Full Chip



- 2<sup>nd</sup>-generation RF-FPGA
  - Improved architecture
  - T/R switch
- Lower Phase-noise CFG
- Higher-linearity RF/BB
- Full-functioned MW block
  - Up/down-conversion
  - "MIXORAMP" reconfigurable mixer/amplifier/4-way active switch
- Phase-coherent Fractional-N CFG

## MATRICs V3

Tape-out: Jan 2016  
Full Chip



- 3<sup>rd</sup>-generation RF-FPGA
  - More configurability
  - Improved Performance
- Lower Noise Figure RF/BB
- Reconfigurable Microwave Block
  - Tunable Gain
  - Tunable BW
  - Tunable Dynamic Range
- Improved CFG with lock-detect and calibration circuit
  - VCO overlaps optimized
  - New on-chip VCO calibration algorithm

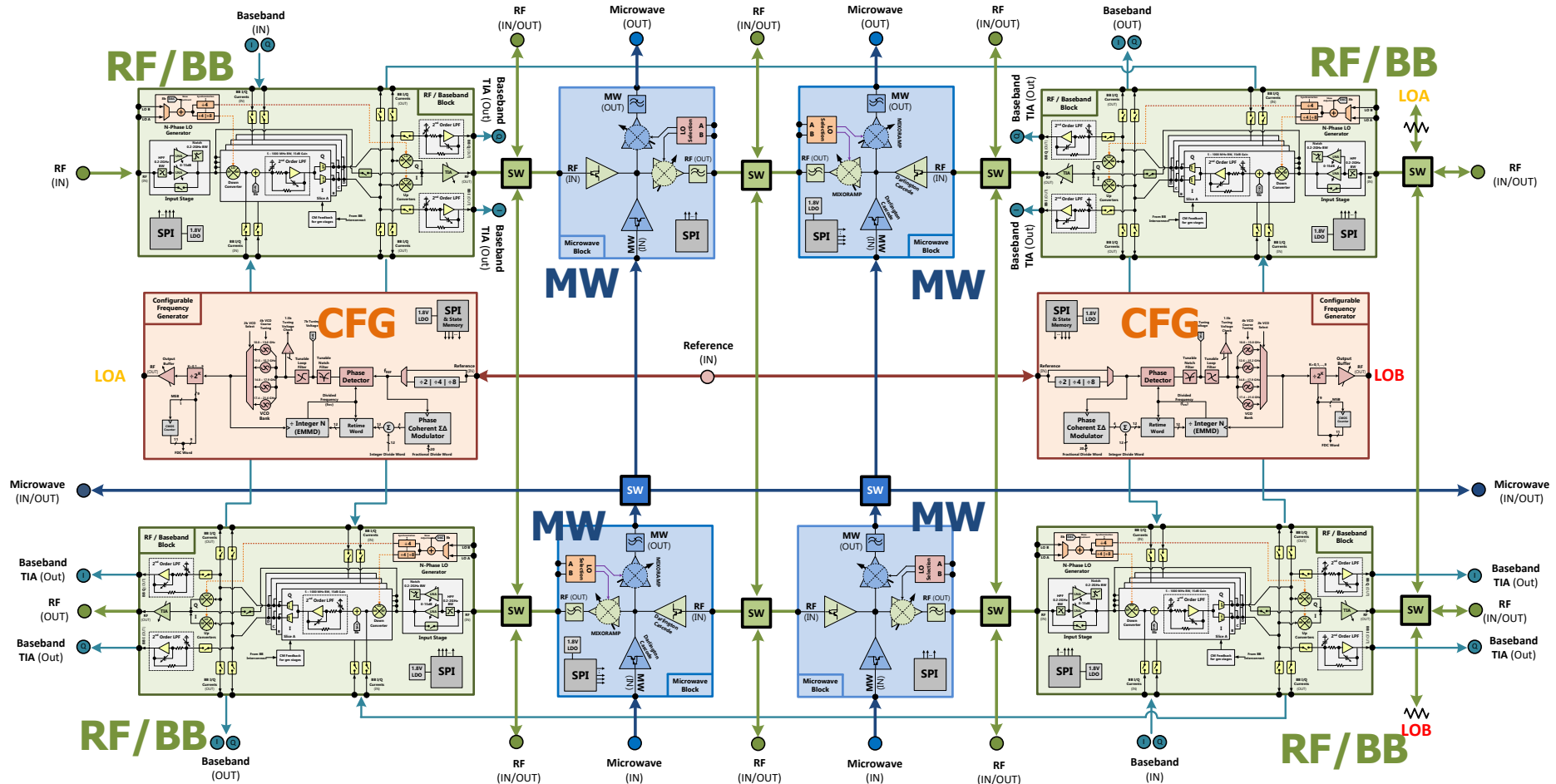
## MATRICs V4

Tape-out: Summer 2018  
Full Chip



- 4<sup>th</sup>-generation RF-FPGA
  - 40 GHz
  - 4 CFGs
  - Improved Performance in new process (SCB13S4B)
- Wider IBW RF/BB Block
  - 4GHz IBW
  - Stretch goal of 10GHz operating frequency
- mmW Microwave Block
  - Extended to 40GHz
- Improved CFGs
  - Extended to 40GHz Support
  - Improved phase noise from new process

# MATRICs V3 architecture



RF/Baseband (RF/BB):

Microwave (MW):

Configurable Frequency Generator (CFG):

DC to 6 GHz

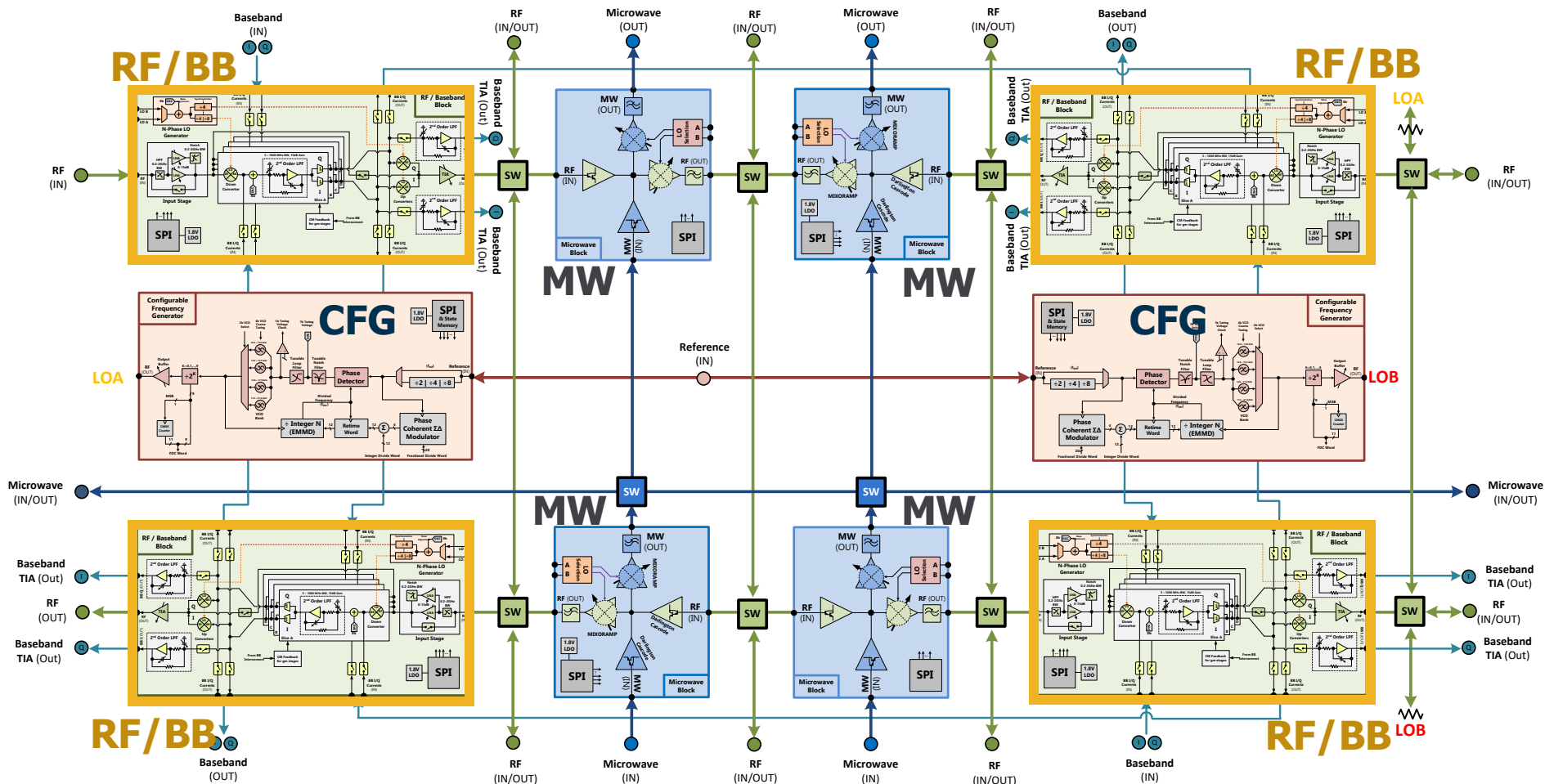
0.5 GHz to 20 GHz

10 MHz to 20 GHz



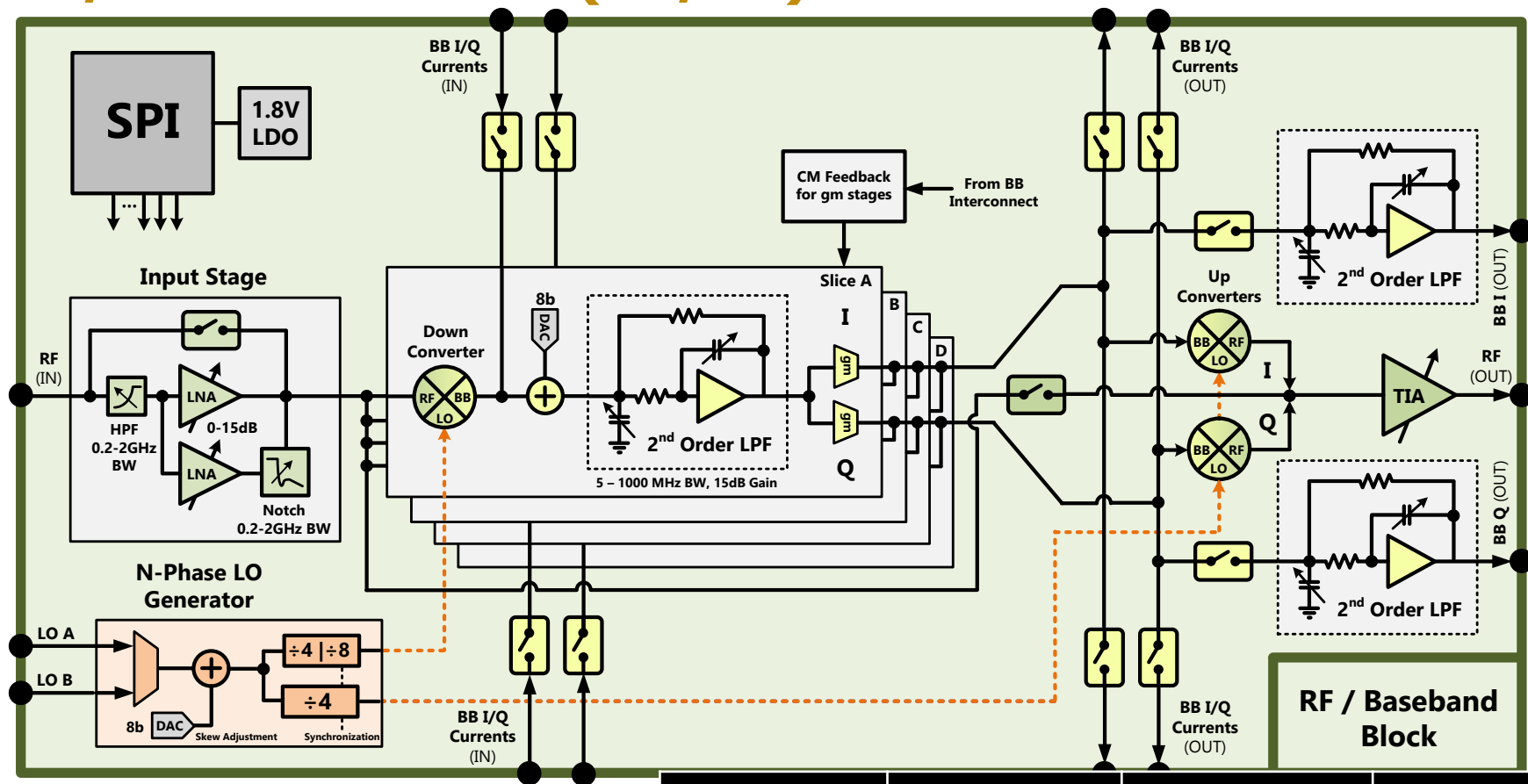
-

# RF/Baseband Block (RF/BB): DC-to-6 GHz





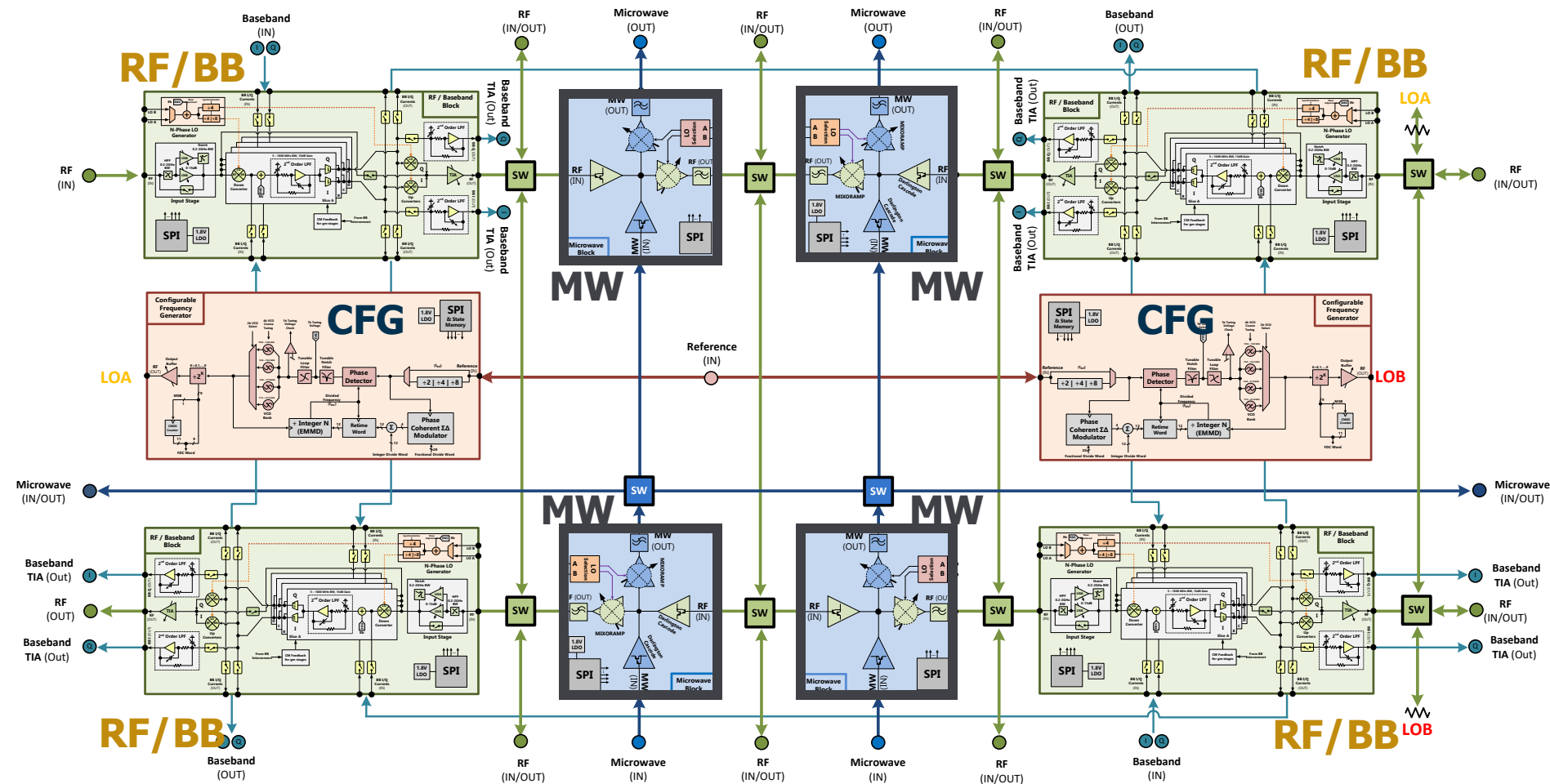
# RF/Baseband Block (RF/BB): DC-to-6 GHz



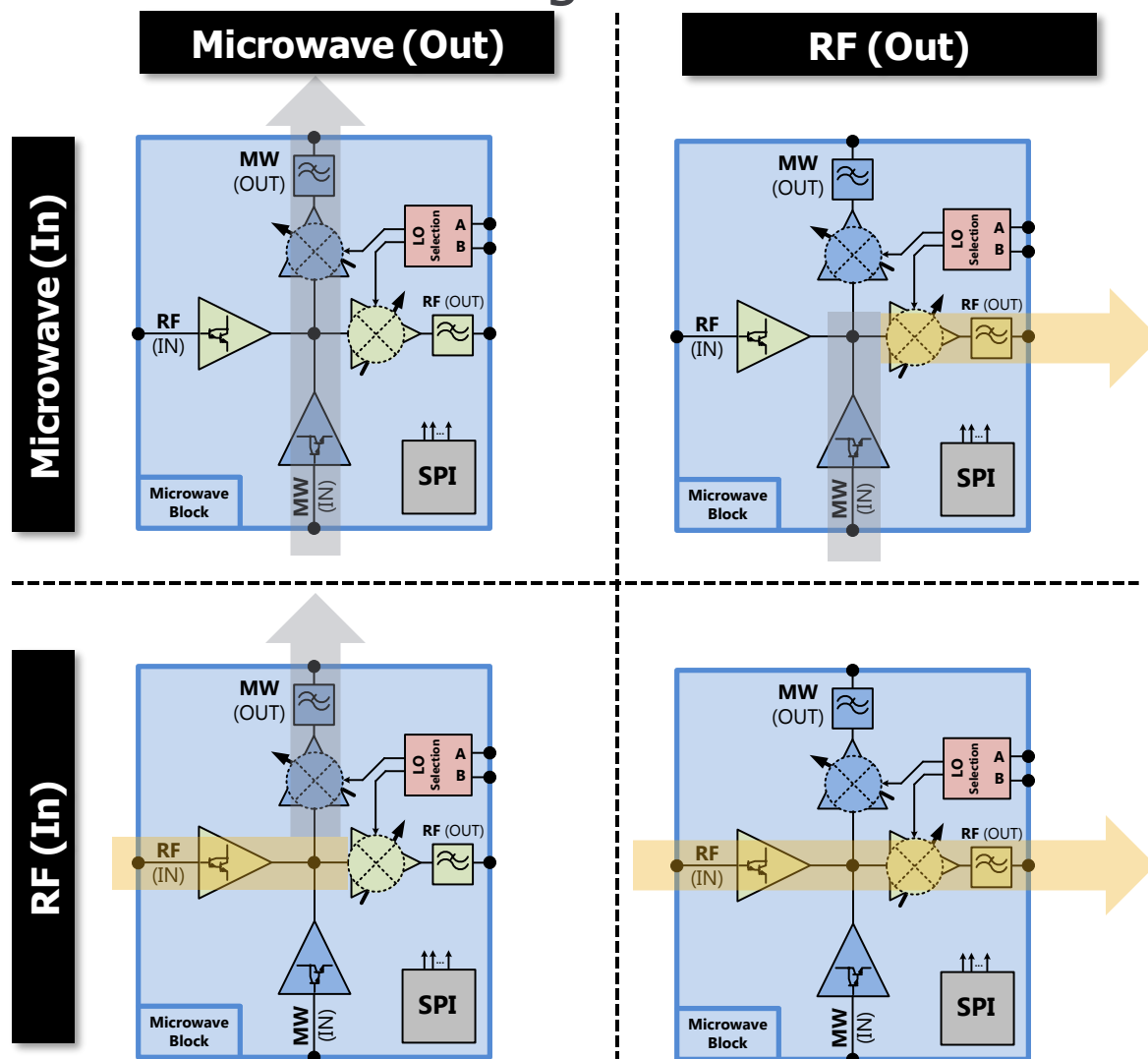
- 4- and 8-path direct-conversion Rx
- I/Q upconverter

Front-end	IB IIP3	OOB IIP3	NF
LNA-1 <sup>st</sup>	> +5 dBm	> +12 dBm	< 10 dB
Mixer-1 <sup>st</sup>	> +15 dBm	> +30 dBm	< 14 dB

# Microwave Block (MW): 0.5 to 20 GHz



# Microwave block usage



- Amplification
- Frequency conversion
- Signal routing

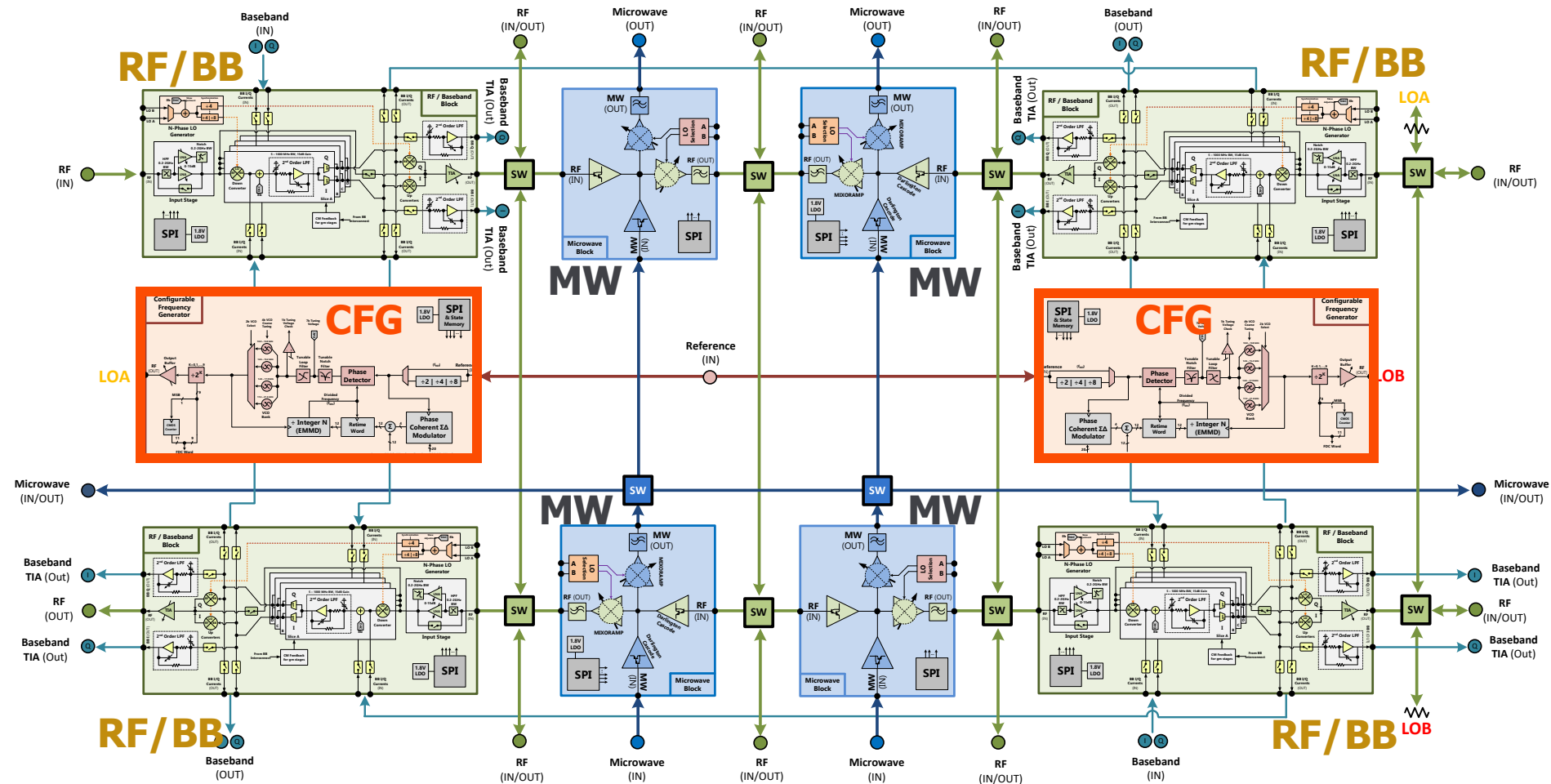
RF: DC to 6 GHz



MW: 0.5 to 20 GHz

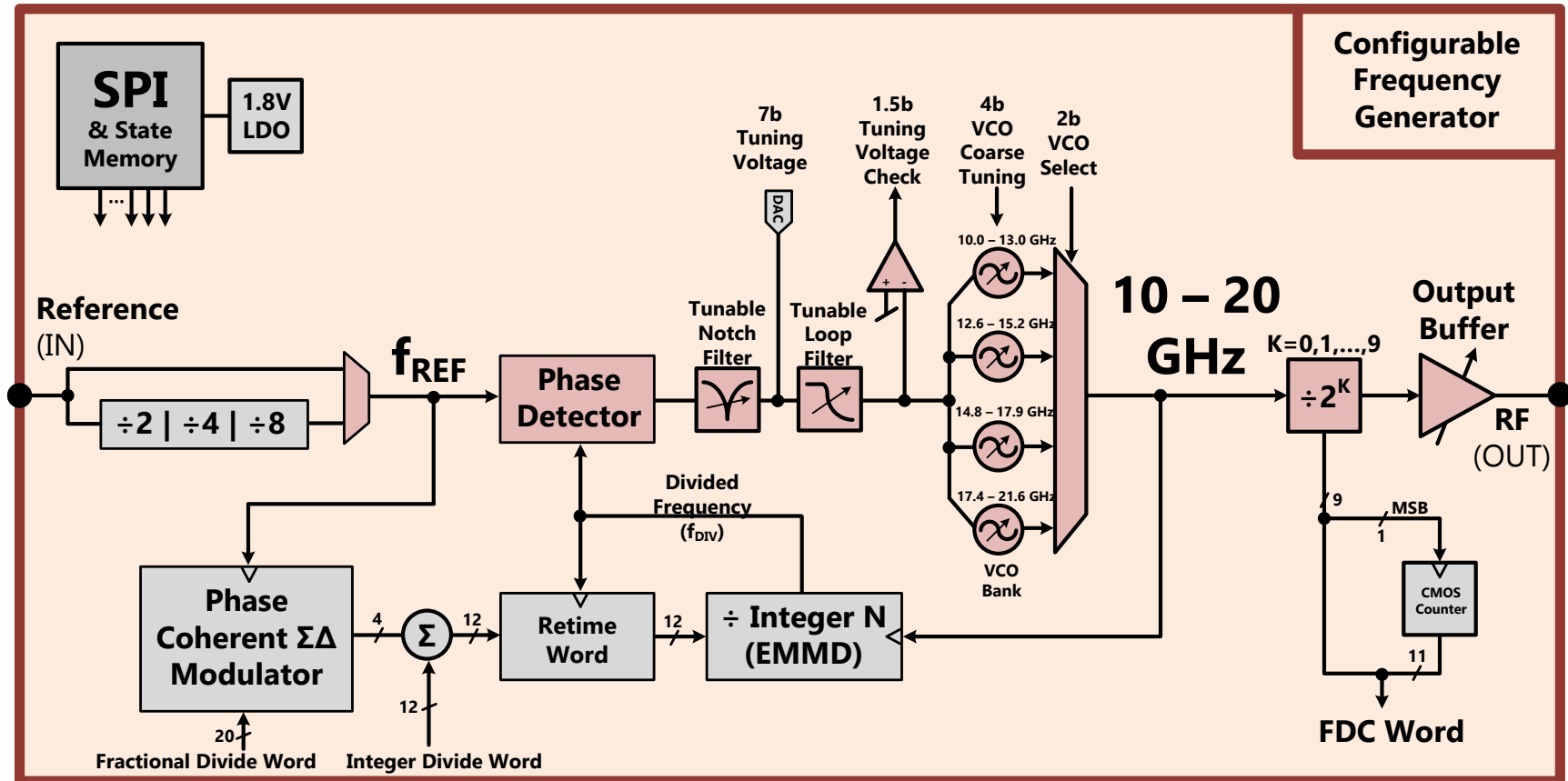


# Configurable Frequency Generator (CFG)

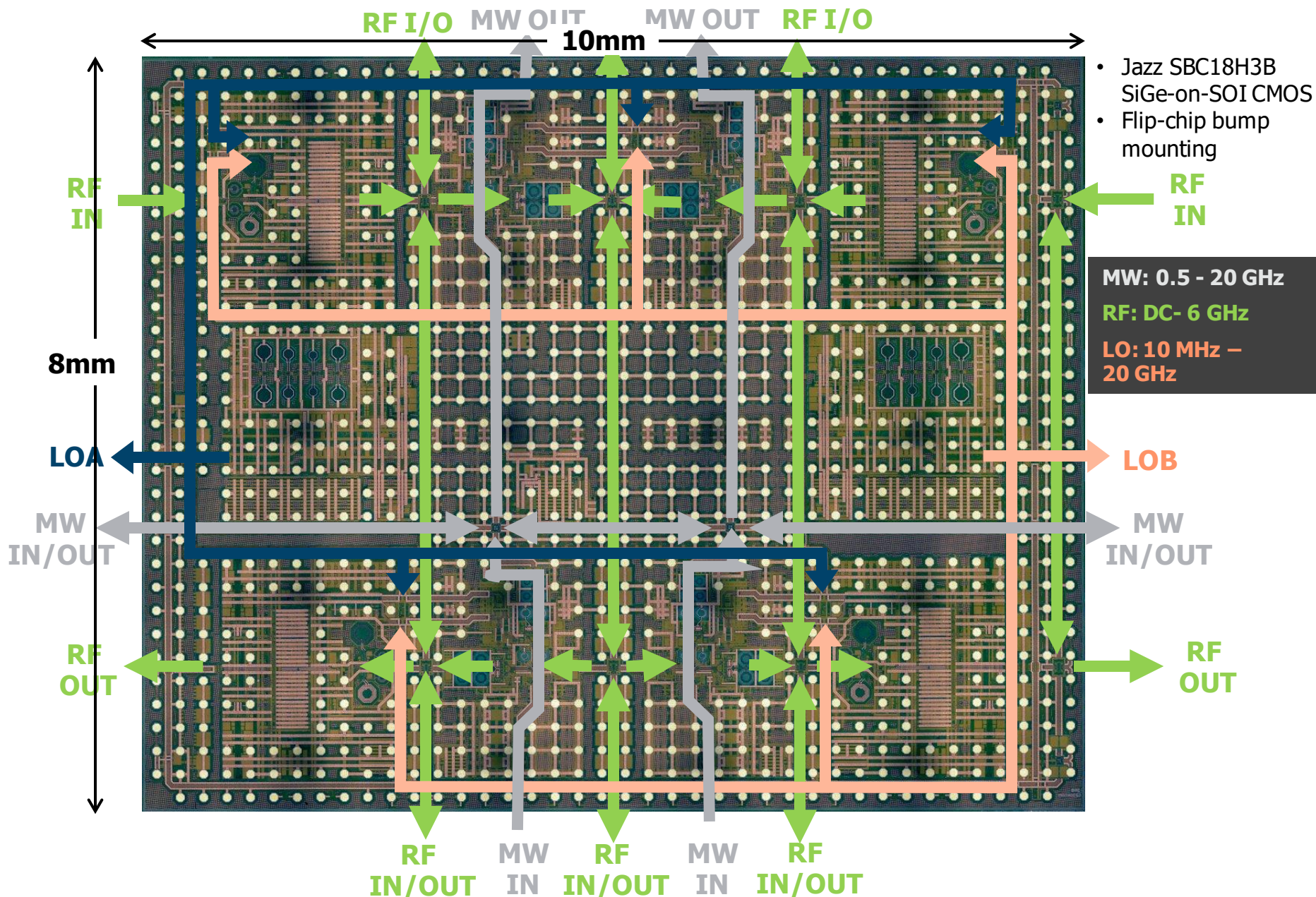




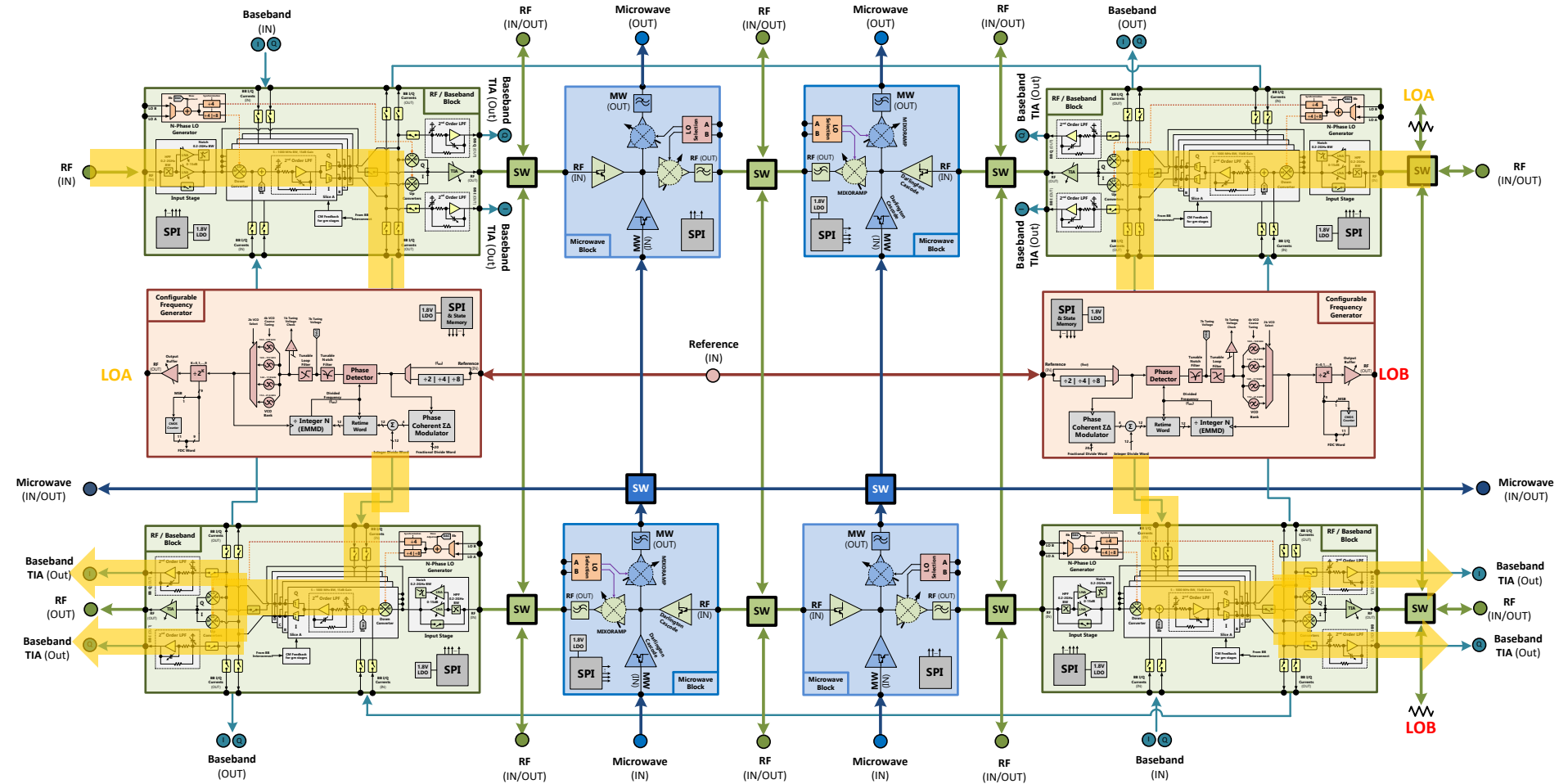
# MATRICs V3 Configurable Frequency Generator (CFG)



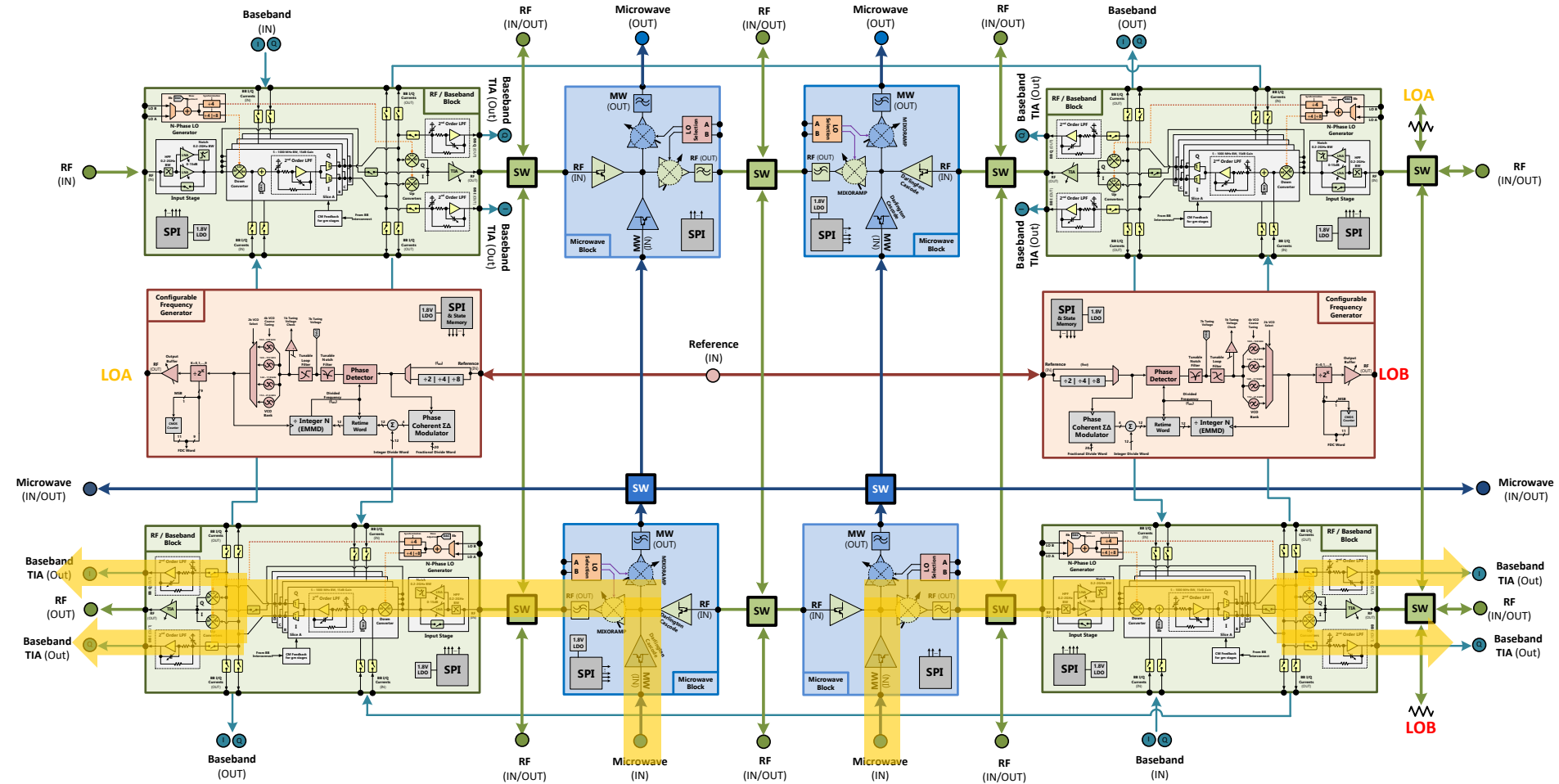
- Integer-N and  $\Sigma\Delta$  fractional-N modes
- Octave-BW PLL (10 to 20 GHz) followed by binary divider
- Quad SiGe VCOs, each with 16 coarse-tuning sub-bands



# 2-channel DC-to-6 GHz direct conversion Rx

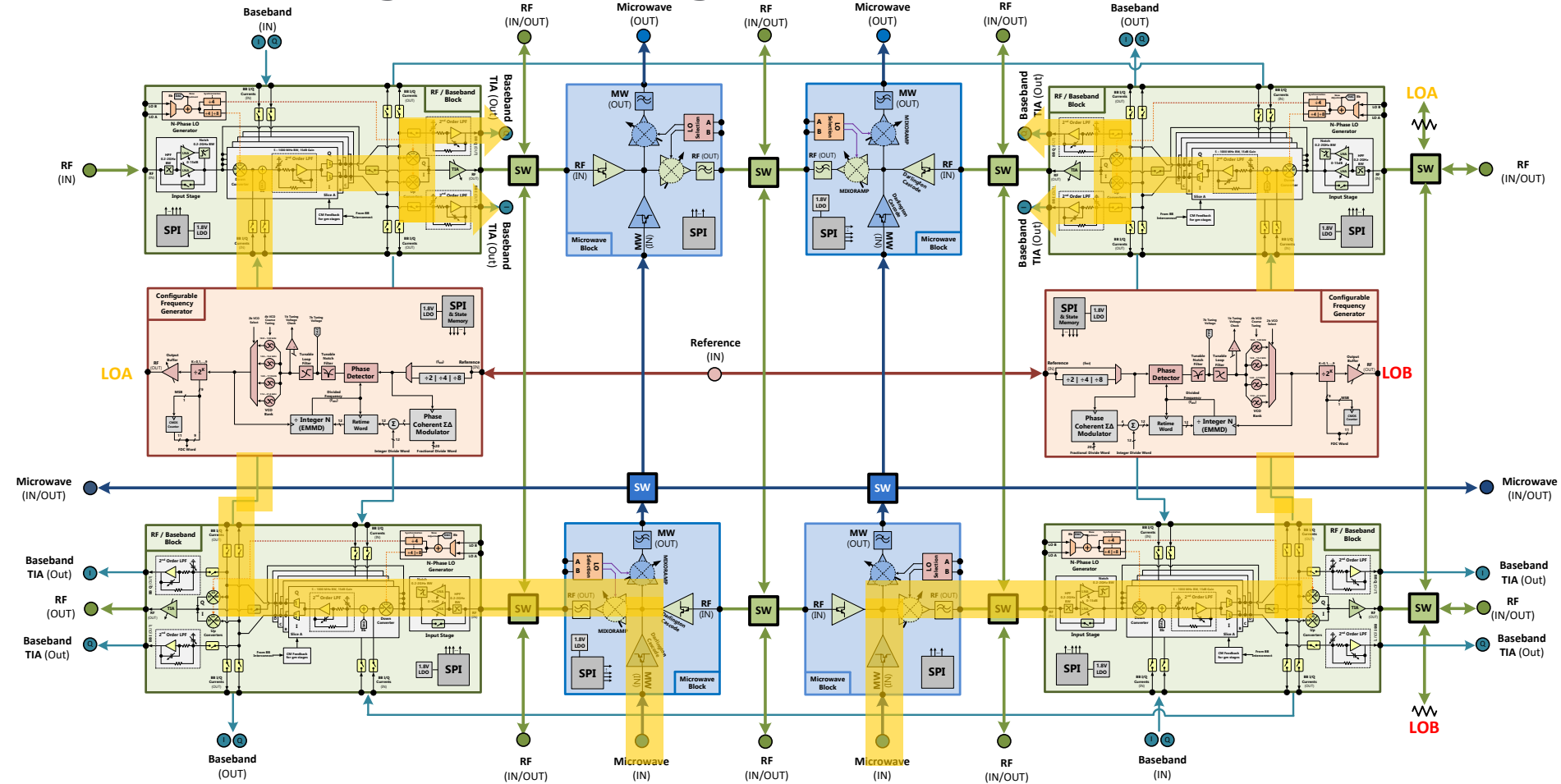


# 2-channel 0.5-to-20 GHz super-heterodyne Rx

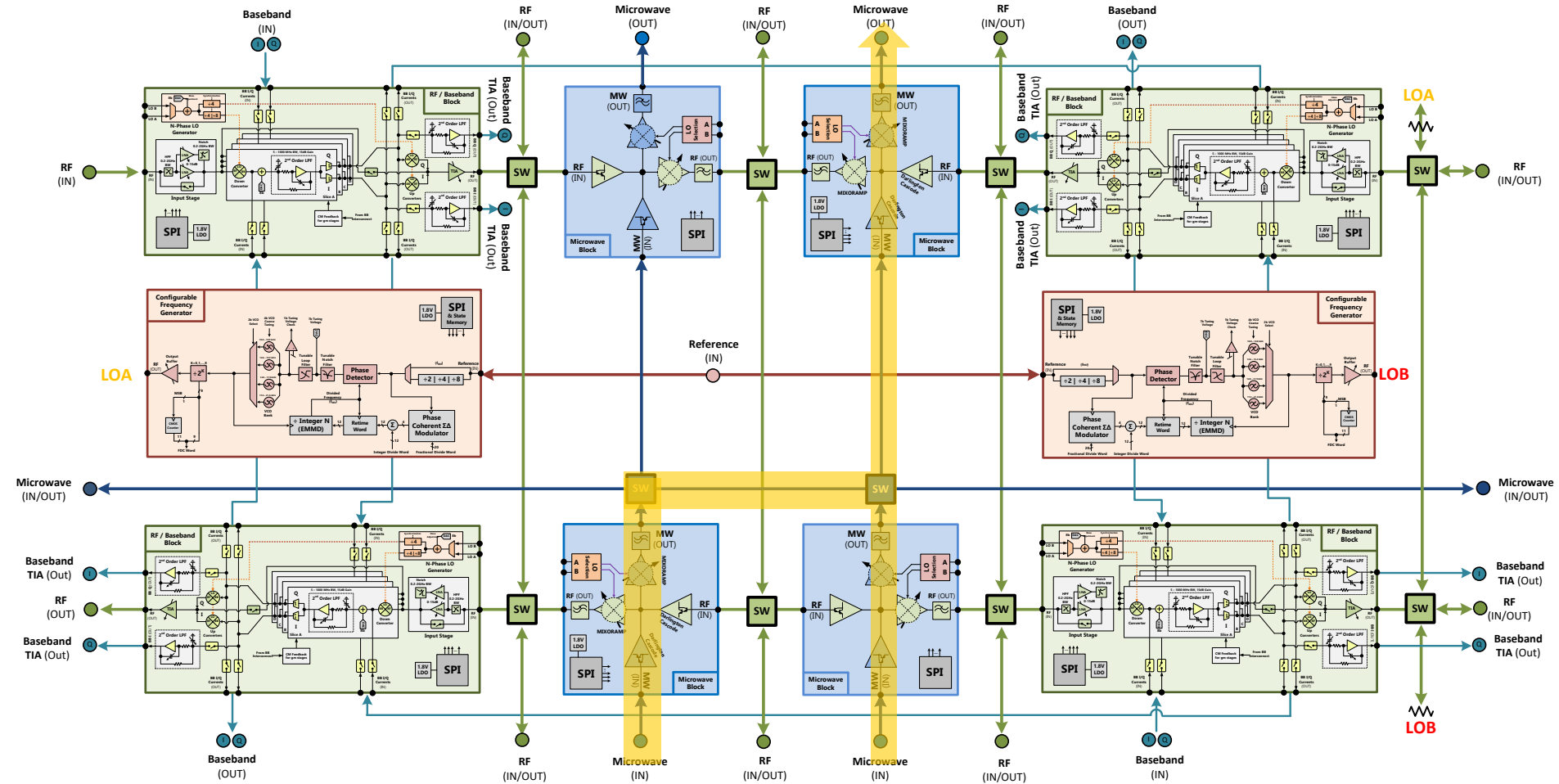




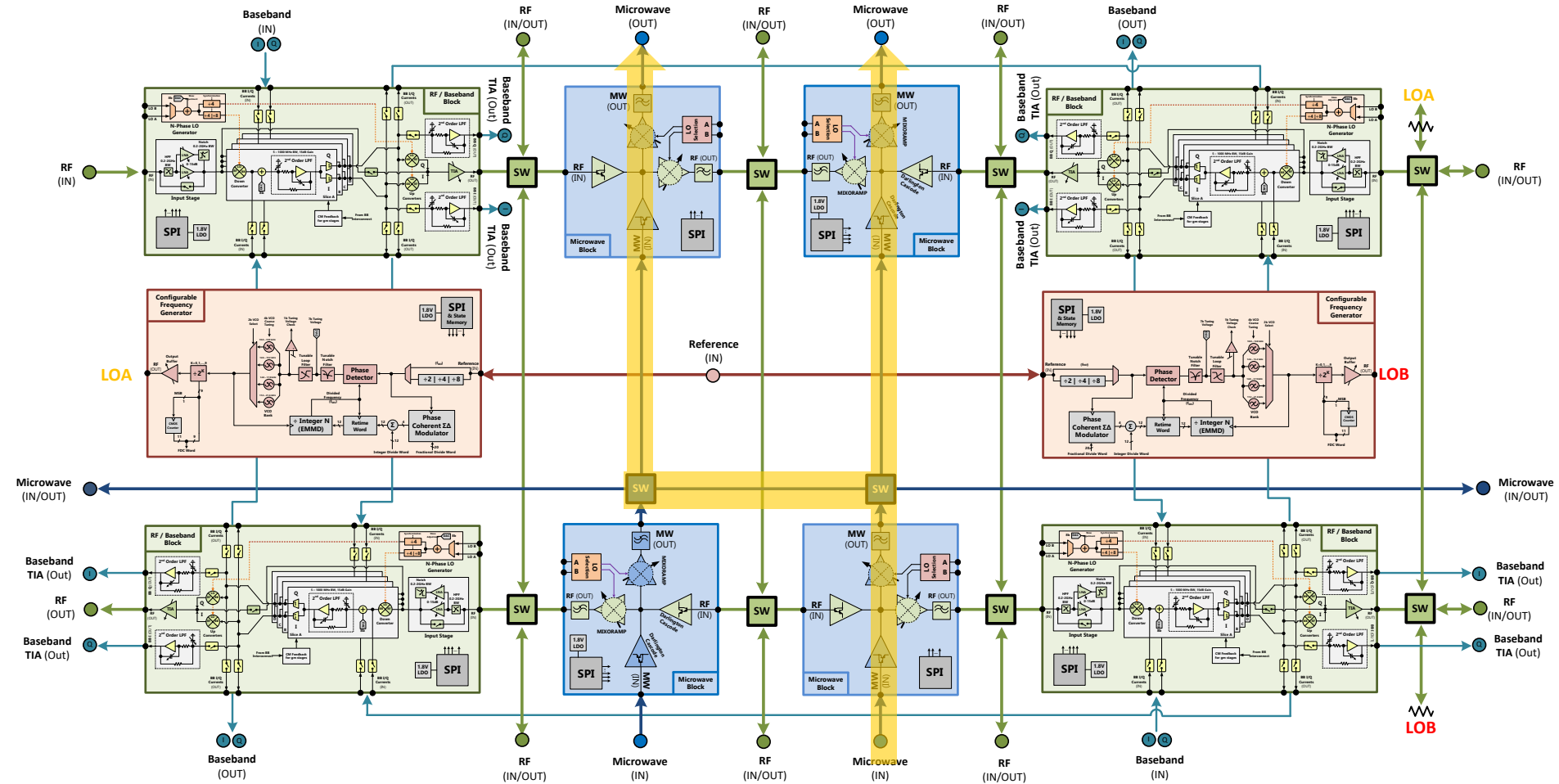
# 2-channel 0.5-to-20 GHz super-heterodyne Rx with increased gain and filtering



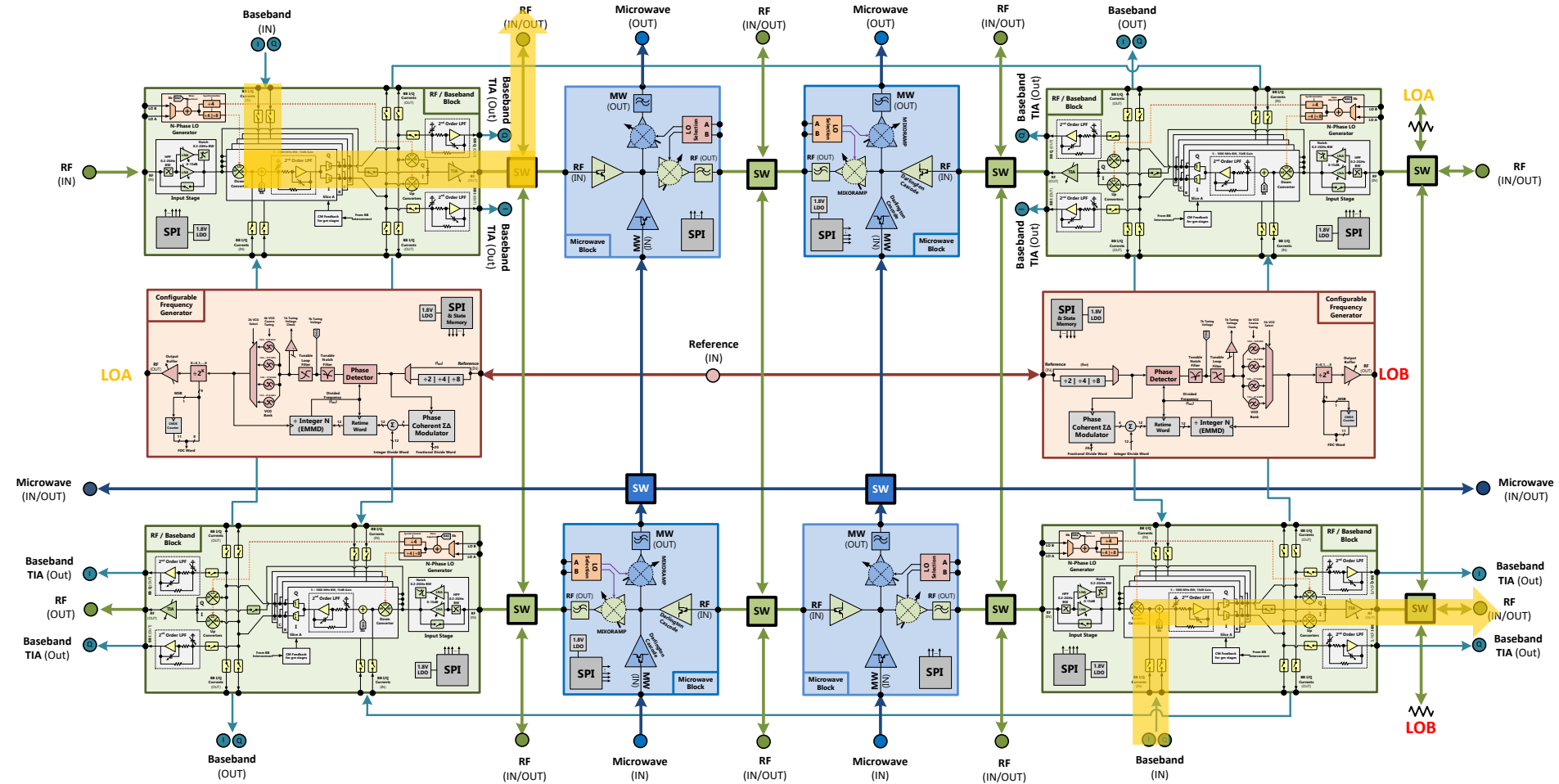
# 2:1 microwave MUX/ amplifier / down-/up-converter



# Microwave amplifier / down-/up-converter / 1:2 router

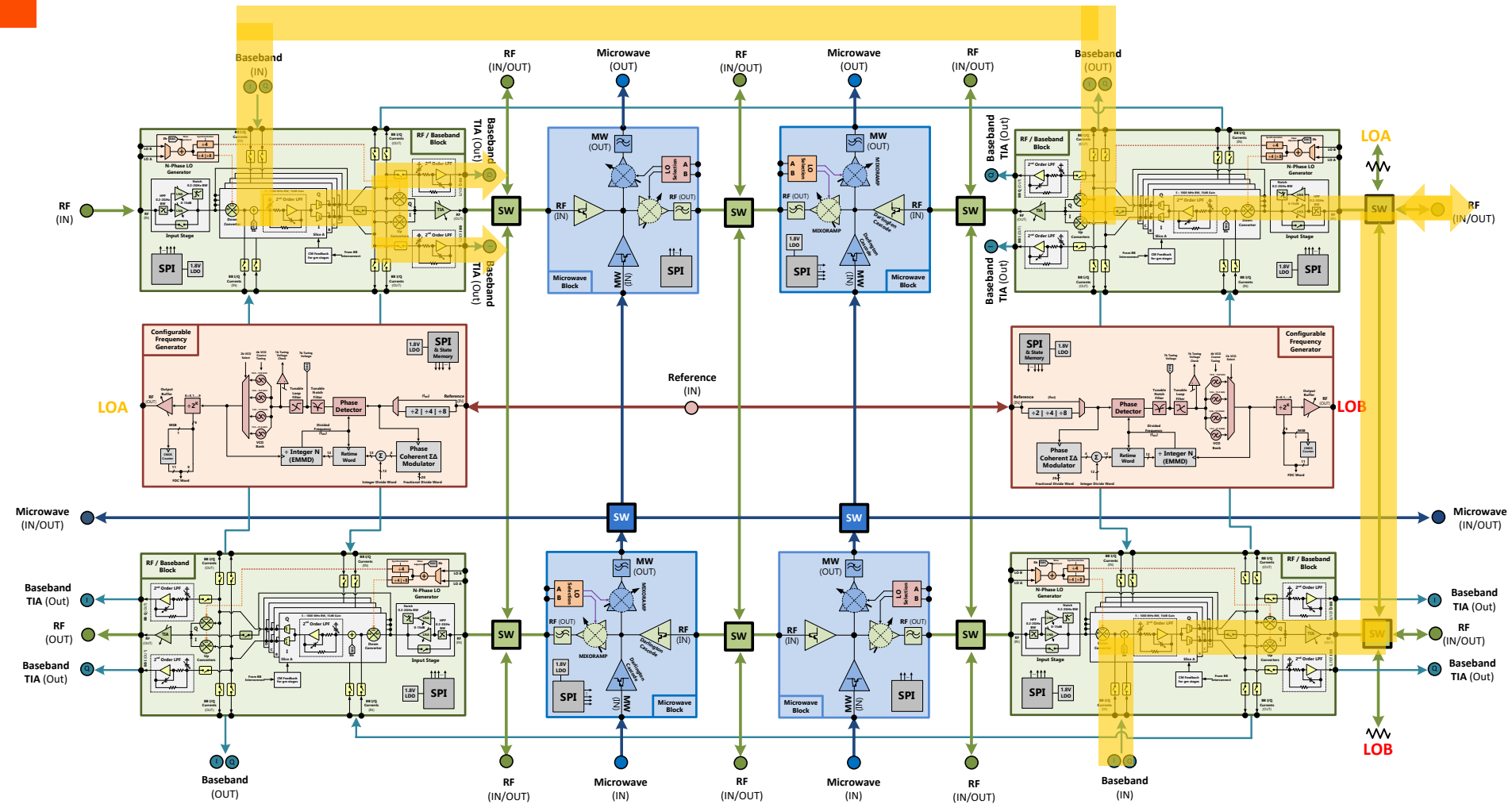


# Dual I/Q up-converters

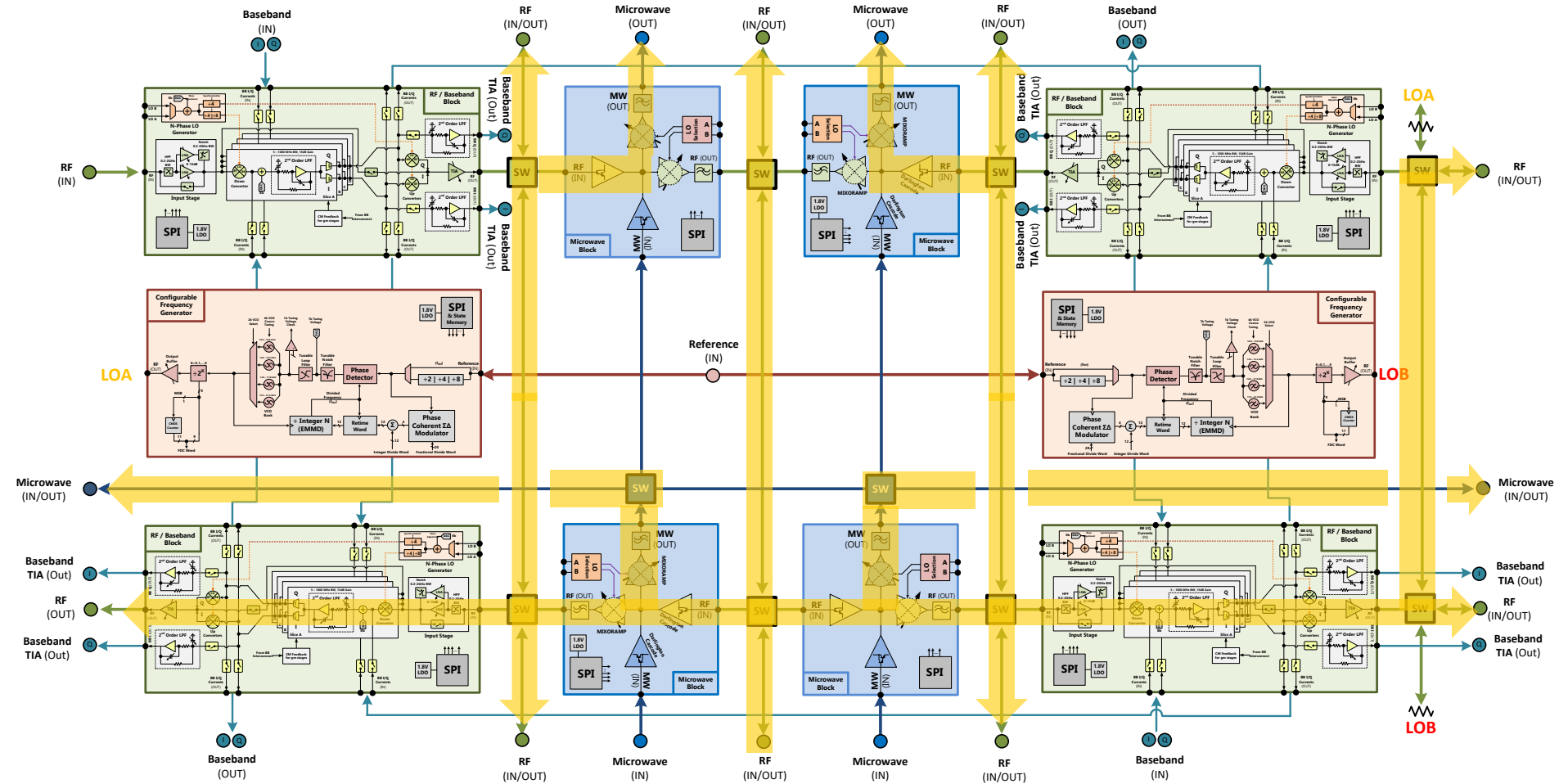




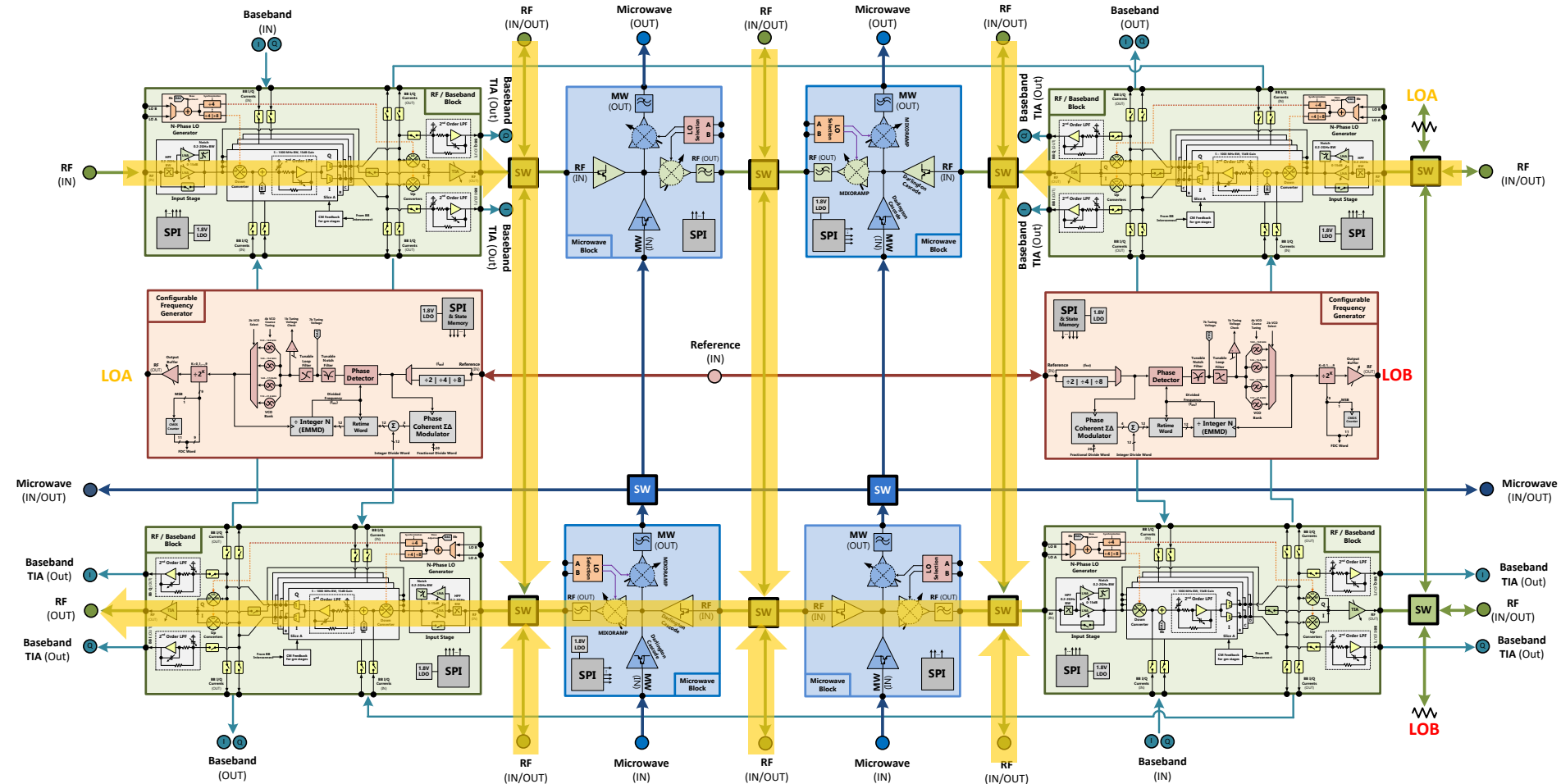
# DC-to-6 GHz RF transceiver



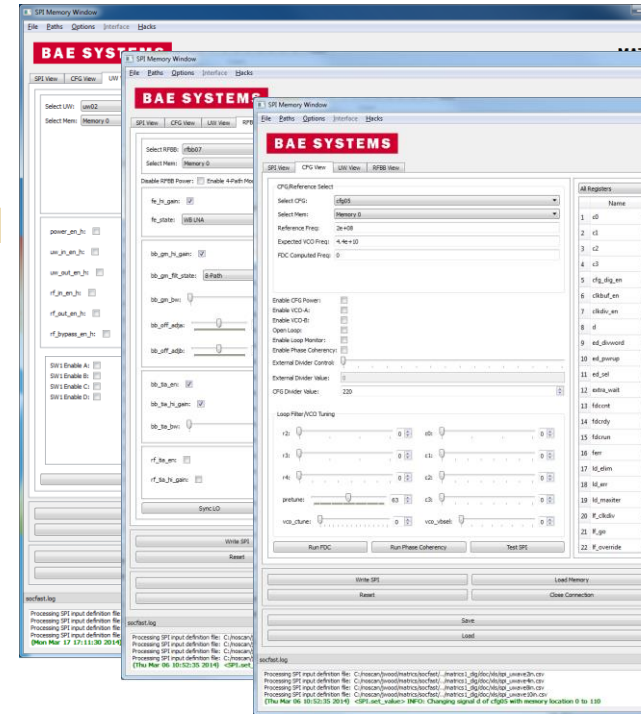
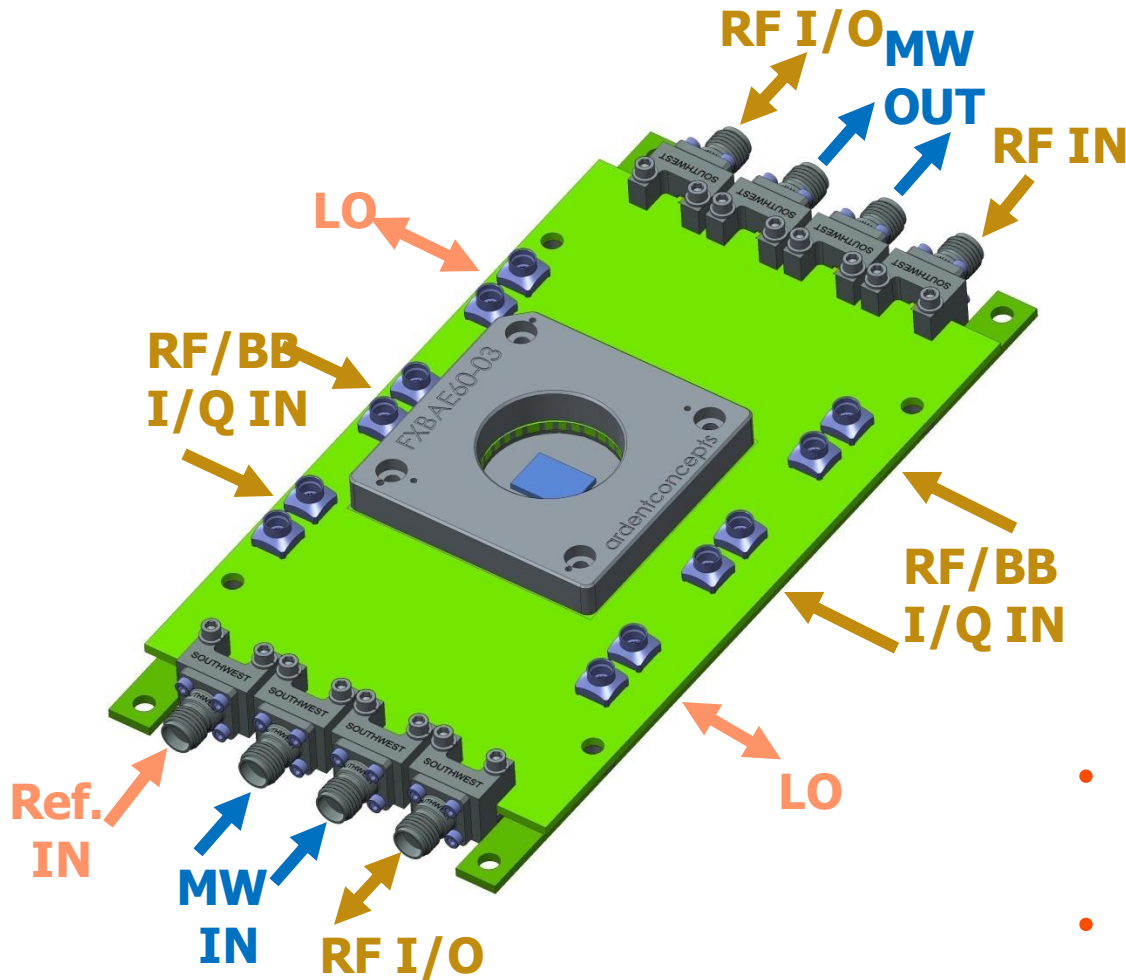
# 1:12 DC-to-6 GHz RF signal router



# 8:1 DC-to-6 GHz RF MUX



# MATRICs Evaluation Board (top view)

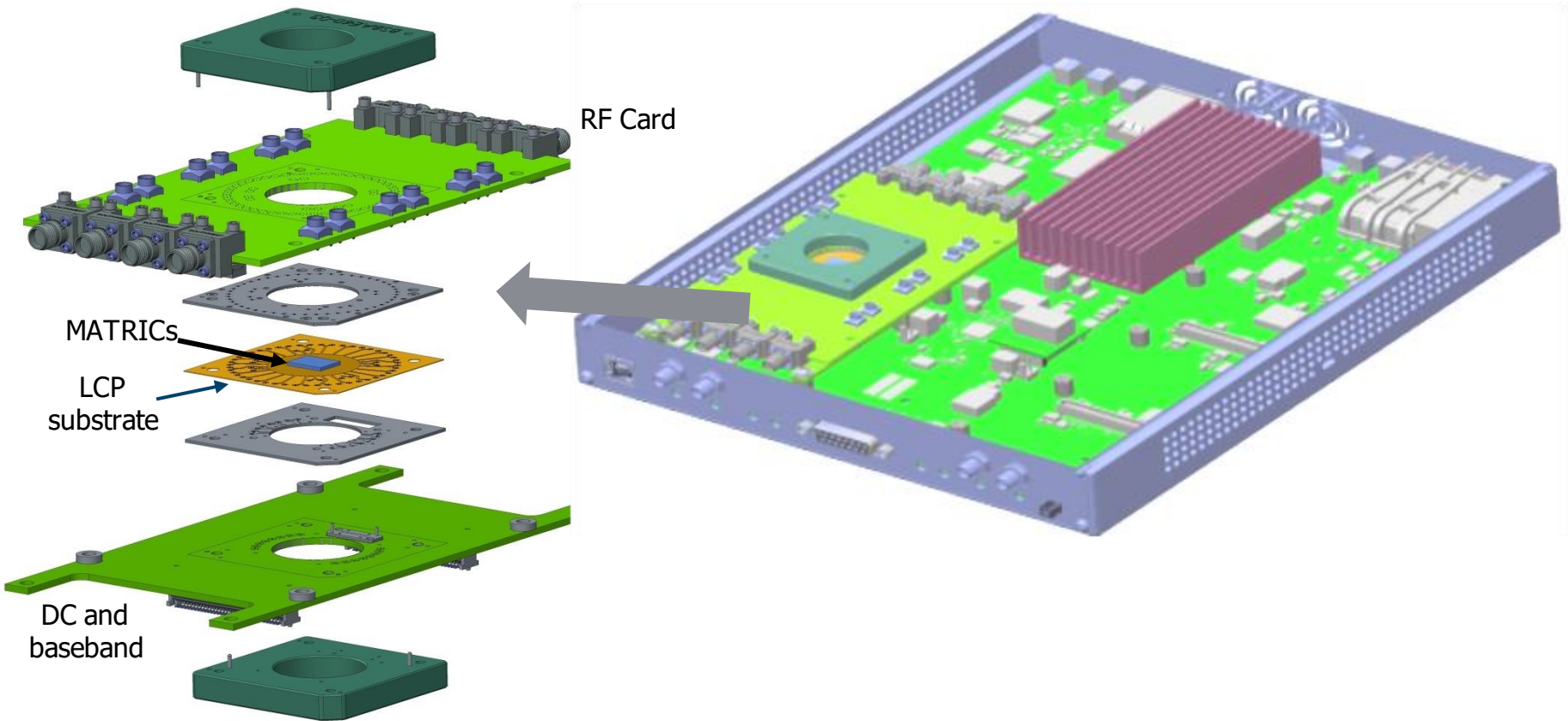


## GUIs for $\mu$ W , RF/BB, & CFG Configuration

- High-isolation socket holds MATRICs IC on LCP substrate
- On-board broadband baluns



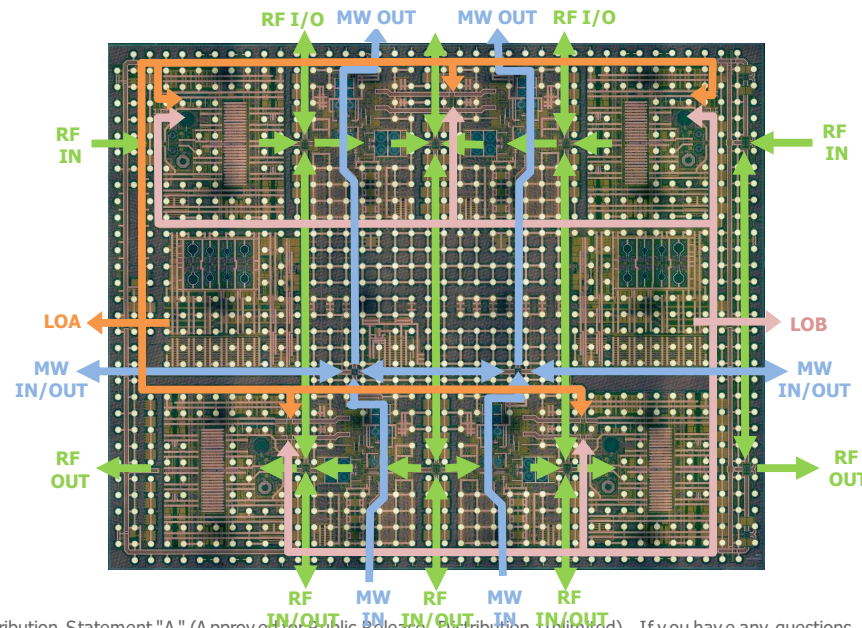
## Ettus X310 / NI USRP-294x SDR compatibility



Leverage NI/Ettus SDR hardware (ADCs, DACs, FPGAs, and power supplies) and open-source software

# MATRICs RF-FPGA Summary

- Save time and \$\$ vs. custom RF ASIC development
- Enables rapid reconfiguration and on-the-fly adaptation
  - Rapid prototyping
  - In-field upgrades
  - Dynamic frequency planning
  - Performance on demand
- Ettus-compatible evaluation board available

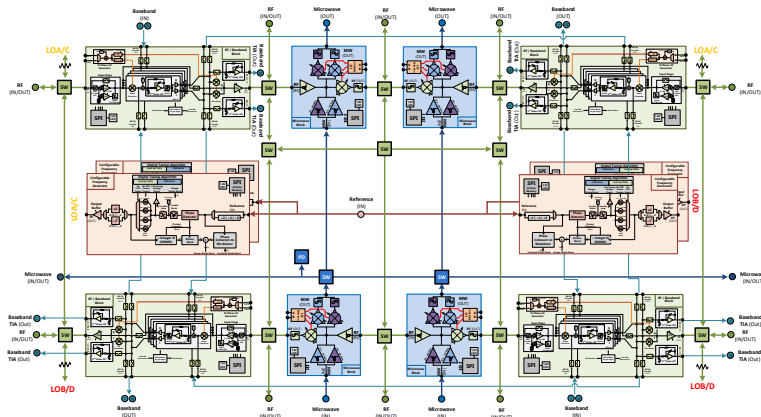




# The Hedgehog Module

# Two transcendent RF SoCs

## MATRICs V4



World's first mm-wave multi-function monolithic transceiver

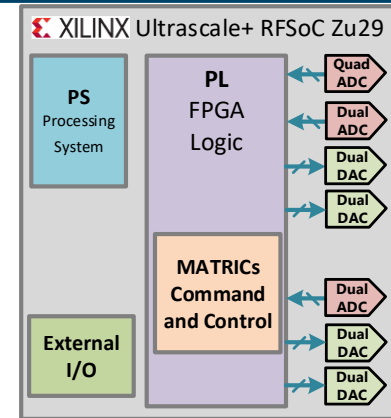
Arbitrarily switchable fabric made possible by 130 nm BiCMOS-on-SOI

82% component count reduction compared to discrete implementations

High channel density for scalable, integrated array applications

Integrated software/firmware for rapid development of custom radios

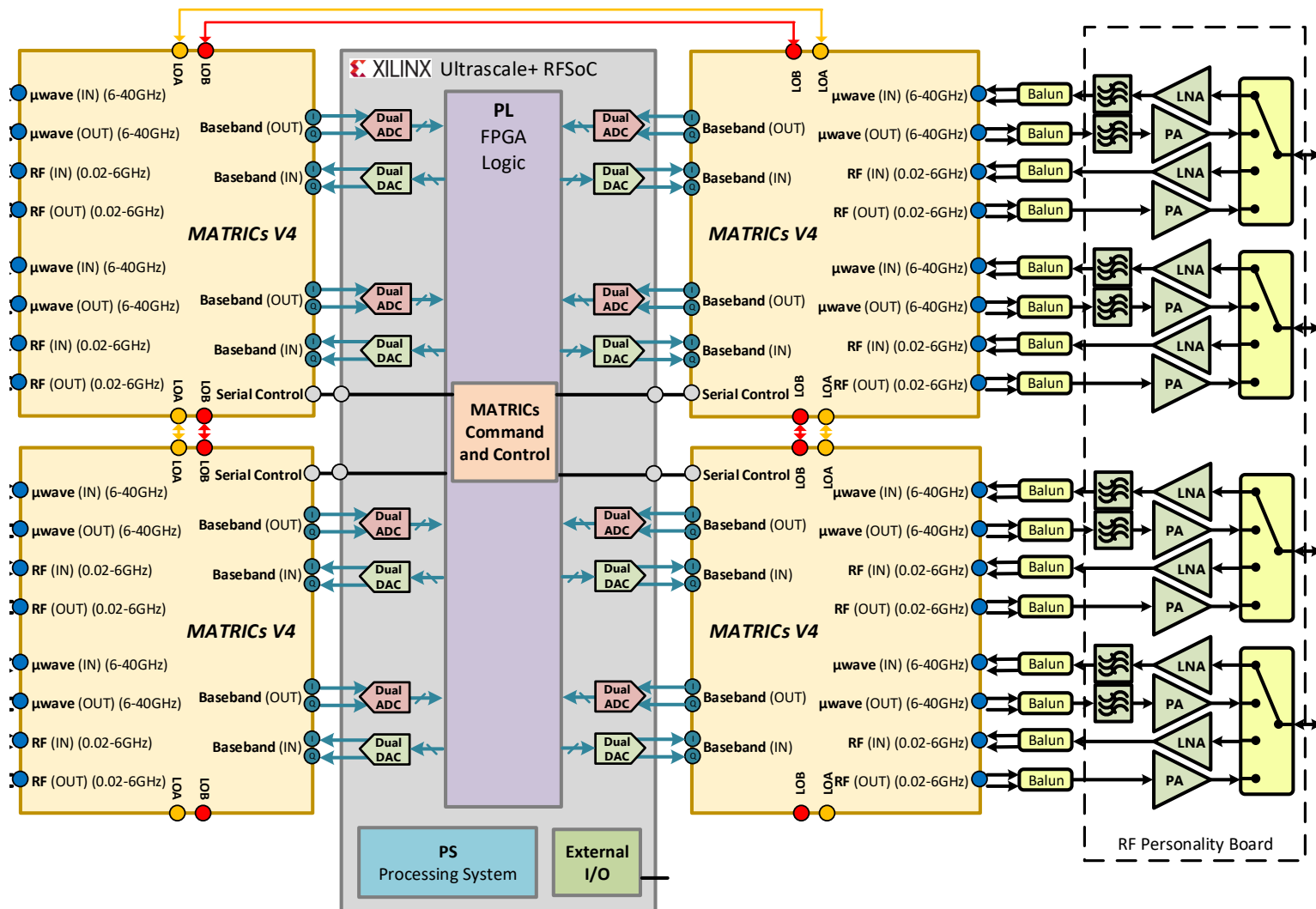
## Ultrascale+ RFSoc



World's first integrated multi-processor, multi-converter FPGA

Eliminates JESD204B/C analog interface, dramatically saving power and latency

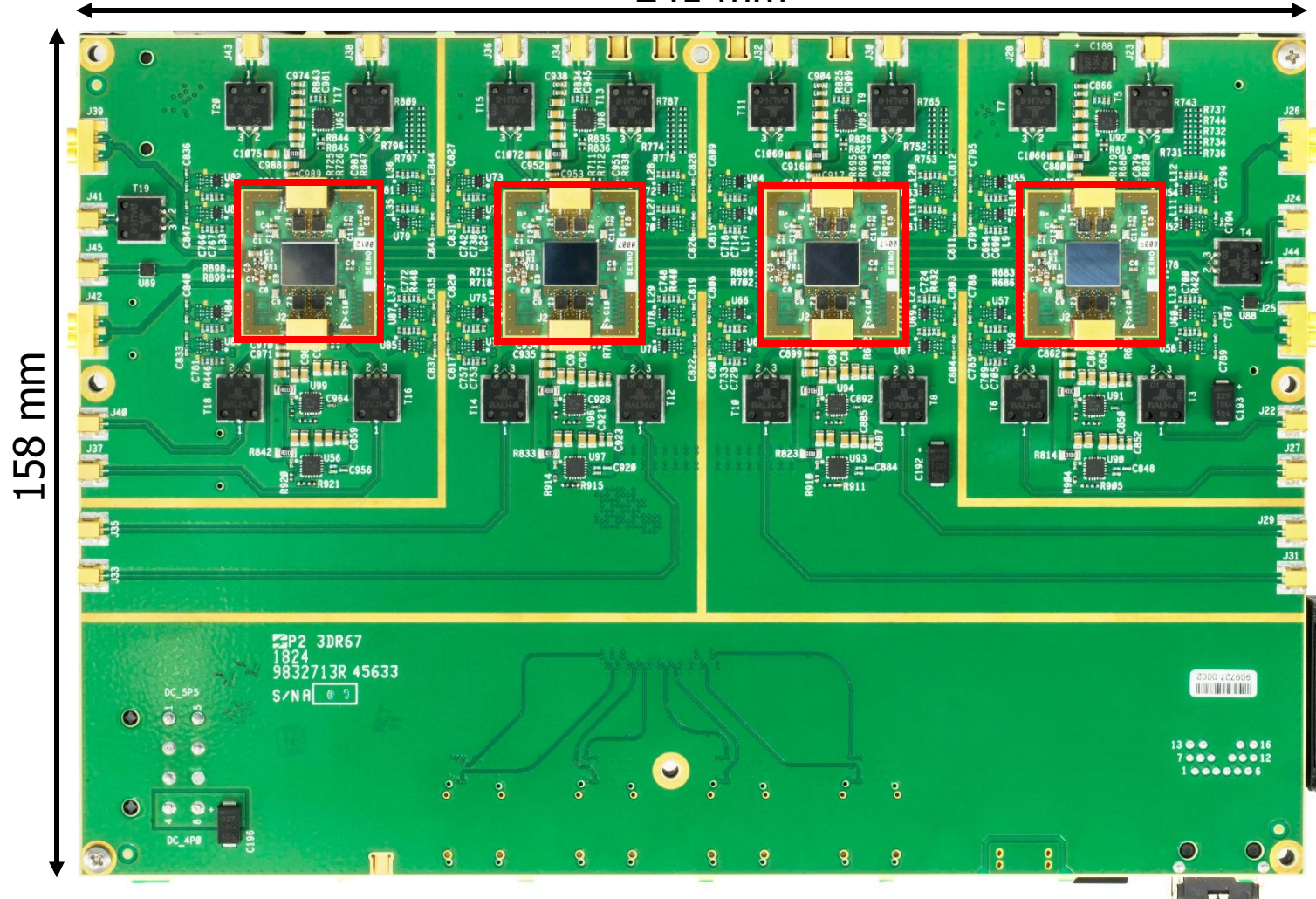
# Hedgehog Block Diagram





# Alpha Hedgehog Module (RF Side)

241 mm

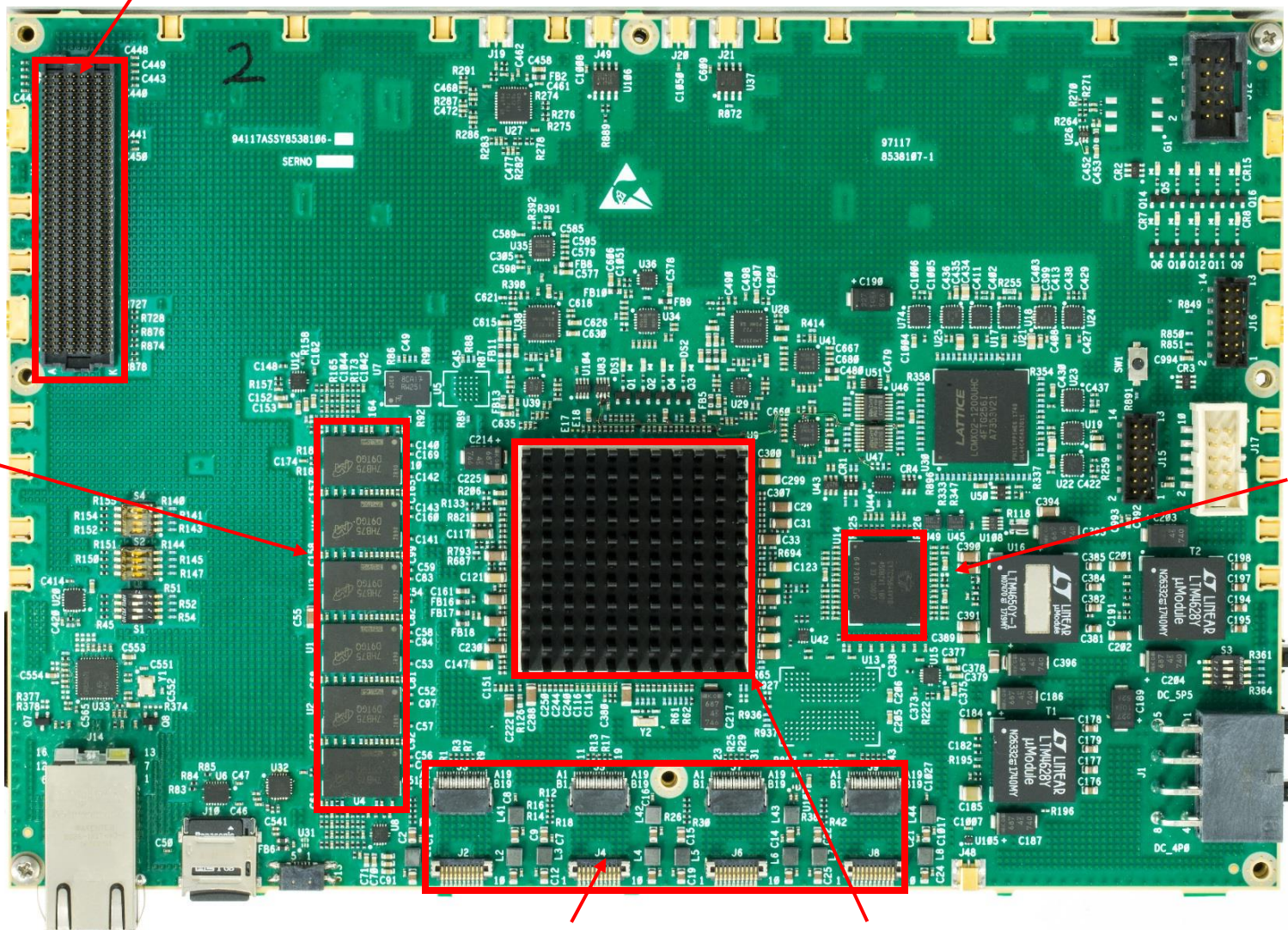




## Personality Connector

DRAM

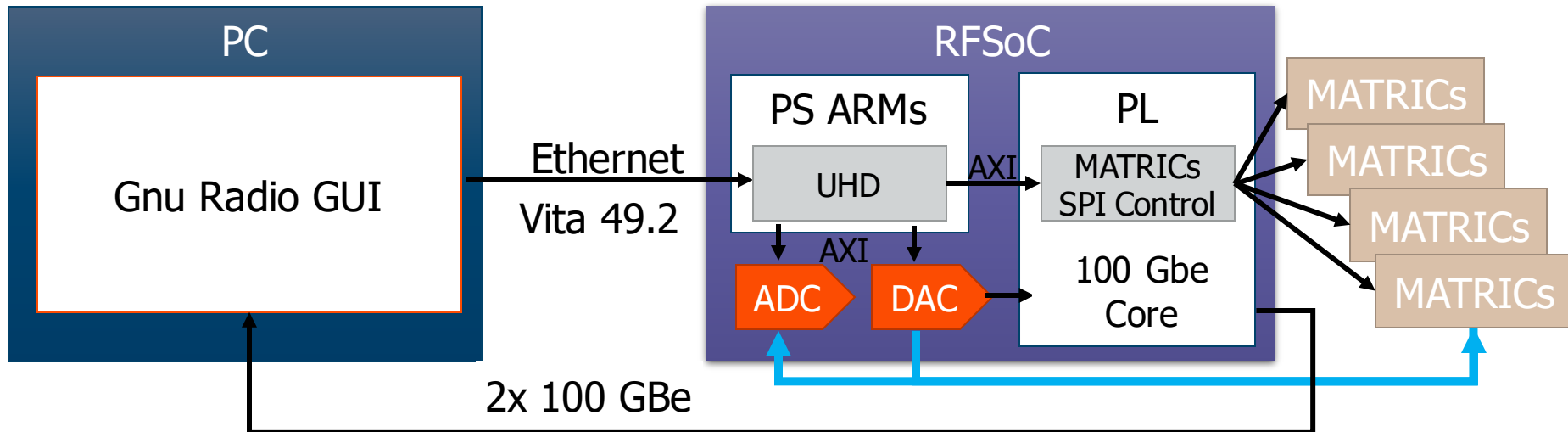
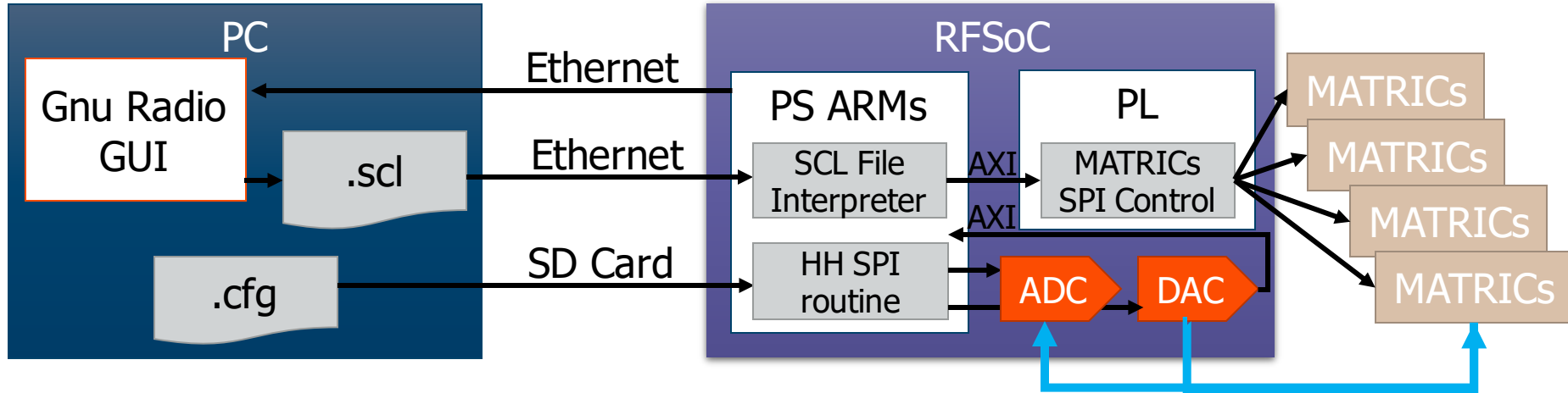
QDR



Firefly Connectors

Xilinx Zu29DR RFSoc

## Programming on Hedgehog





# Demonstration Walkthrough



# Demo Part 1

The screenshot displays a software interface with a central block diagram and several configuration panels.

**Block Diagram:**

- Options:** EDs: top\_block, Generate Options: QT GUI
- Variable:** EDs: samp\_rate, Value: 20
- File Source:** File: .../srcan/abram/n0\_1.bin, Repeat: Yes, Add begin tag: ()
- Int To Float:** Scale: 1
- QT GUI Frequency Sink:** FFT Size: 4096, Center Frequency (Hz): 0, Bandwidth (Hz): 20

**MATRICS Configuration:**

- Interface Select: Socket
- Socket Port Number: 8080
- Socket IP Address: 15...10.5
- Reference Frequency (MHz): 100
- CFG A Output Frequency (MHz): 2k
- CFG B Output Frequency (MHz): 8...8k
- CFG A Output Enable: Enabled
- CFG B Output Enable: Enabled
- TX CH1 Type: Homodyne
- TX CH1 LO1: CFG A
- TX CH1 Divider: Divide By 2
- TX CH1 LO2: CFG A
- TX CH1 Gain: 0
- TX CH2 Type: Homodyne
- TX CH2 LO1: CFG A
- TX CH2 Divider: Divide By 2
- TX CH2 LO2: CFG A
- TX CH2 Gain: 0
- RX CH1 Type: Homodyne
- RX CH1 LO1: CFG A
- RX CH1 Divider: Divide By 2
- RX CH1 LO2: CFG A
- RX CH1 Gain: 0
- RX CH2 Type: Homodyne
- RX CH2 LO1: CFG A
- RX CH2 Divider: Divide By 2
- RX CH2 LO2: CFG A
- RX CH2 Gain: 0

**Right Panel (Module List):**

- (no module specified)
- acars2
- ADSB
- ais
- AX.25
- burst
- cdma
- es
- EVENTSTREAM
- GSM
- Instrumentation
- IQ Balance
- lte
- mapper
- MATRICS
- MATRICS
- HAQI
- RADAR
- Sinks
- Sources
- Spectrum Estimation
- Stream Conversions
- UQComs
- Core
- Audio
- Boolean Operators
- Byte Operators
- Channel Models
- Channelizers
- Coding
- Control Port
- Debug Tools
- Deprecated
- Digital Television
- Equalizers
- Error Coding
- FCD
- File Operators

**Bottom Left Console:**

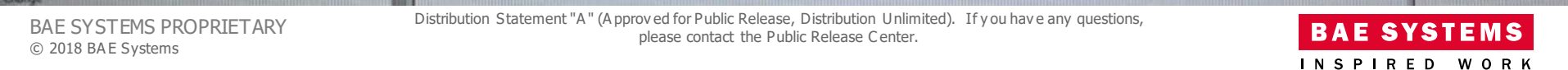
```

interface> Transmission Data length: 22
interface> Received 22 bytes of data.
interface> ACK: Message Received.
interface> Sending 106 bytes of data.
interface> Blocking to receive data length...
interface> Transmission Data length: 22
interface> Received 22 bytes of data.
interface> ACK: Message Received.
Change
  
```

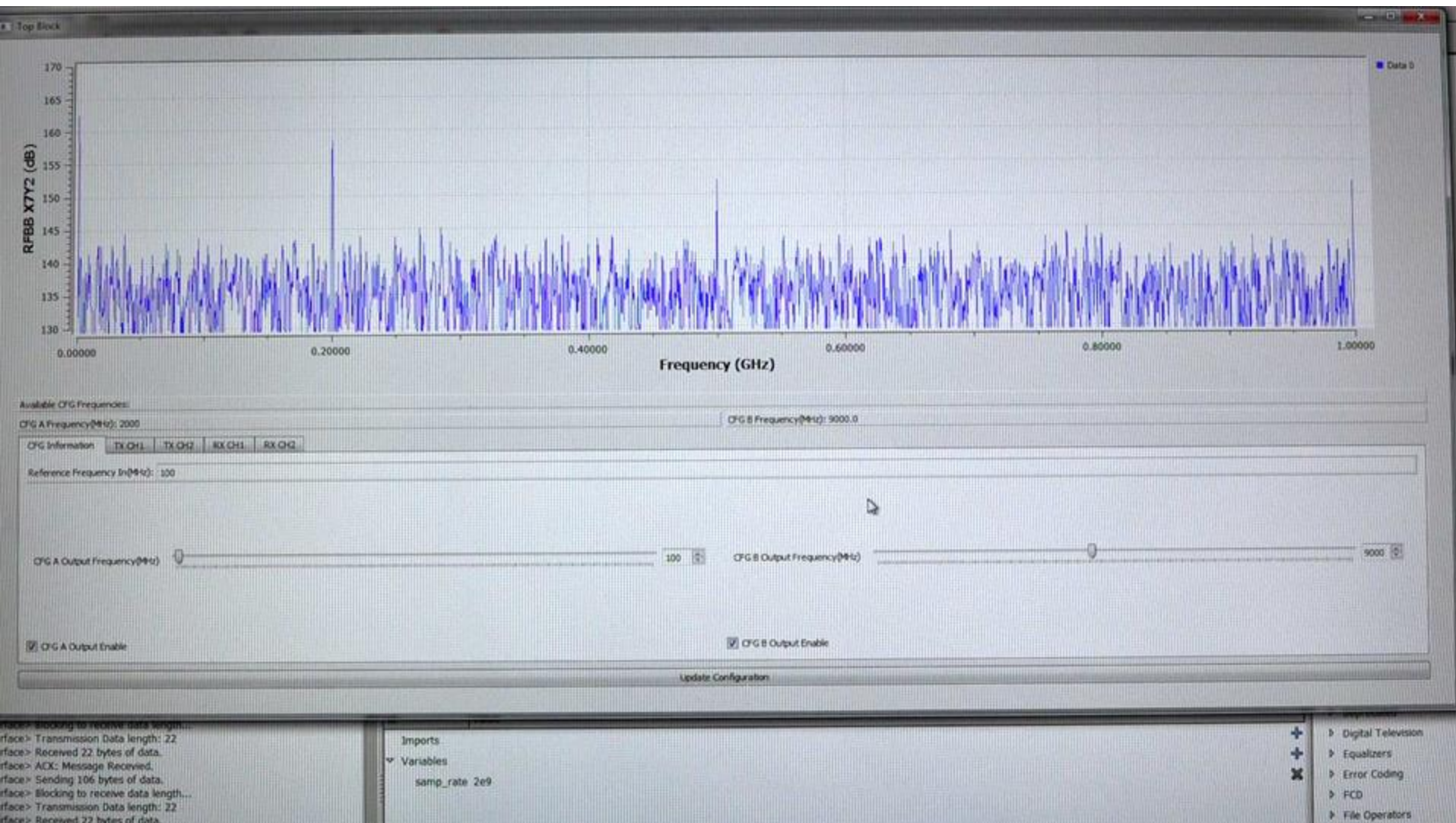
**Bottom Right Table:**

Id	Value
Imports	
Variables	
samp_rate	2e9





# Demo Part 3



## Acknowledgments

- Tom Rondeau, Janet Liu, David Kirkwood, and the rest of the government team under DARPA/MTO Hedgehog Program, Contract No. FA8650-17-C-7709
- Steve Hary & Brandon Mathieu, AFRL
- Mike Scott, Dave Howard, Ed Priesler, Jazz Semiconductor
- Manuel Uhm, Doug Johnson, Dan Baker NI/Ettus Research