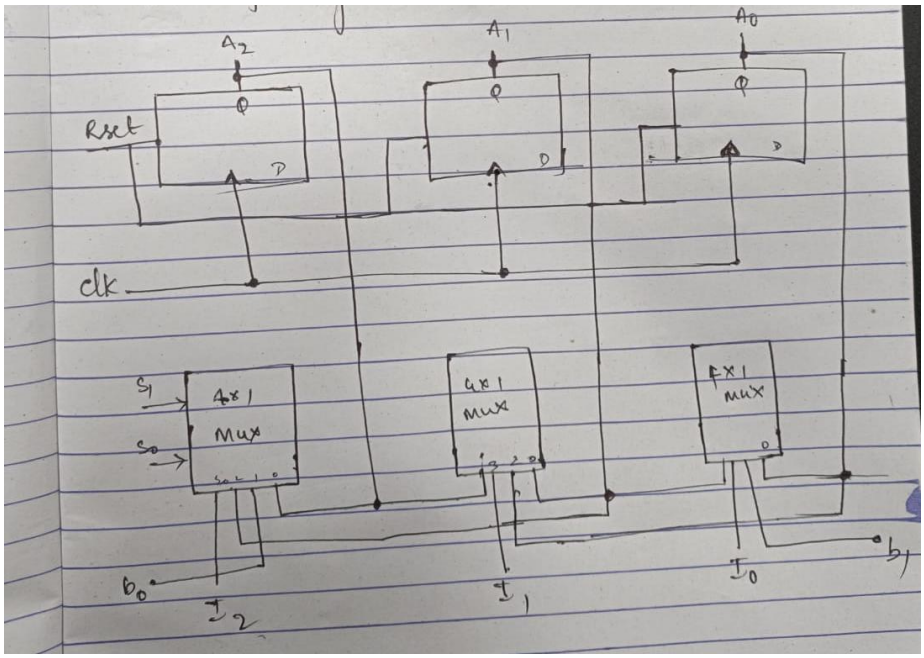
VHDL CODE DEVELOPMENT AND CPLD BOARD OPERATING

Aim: The purpose is to create VHDL code, feed it to a CPLD board, and test the board's operation.

Summary Of the Experiment: Creating structural VHDL code for a 3-bit universal shift register using behavioral VHDL code for a D flip flop and MUX, then putting it into a CPLD board to test its functionality.

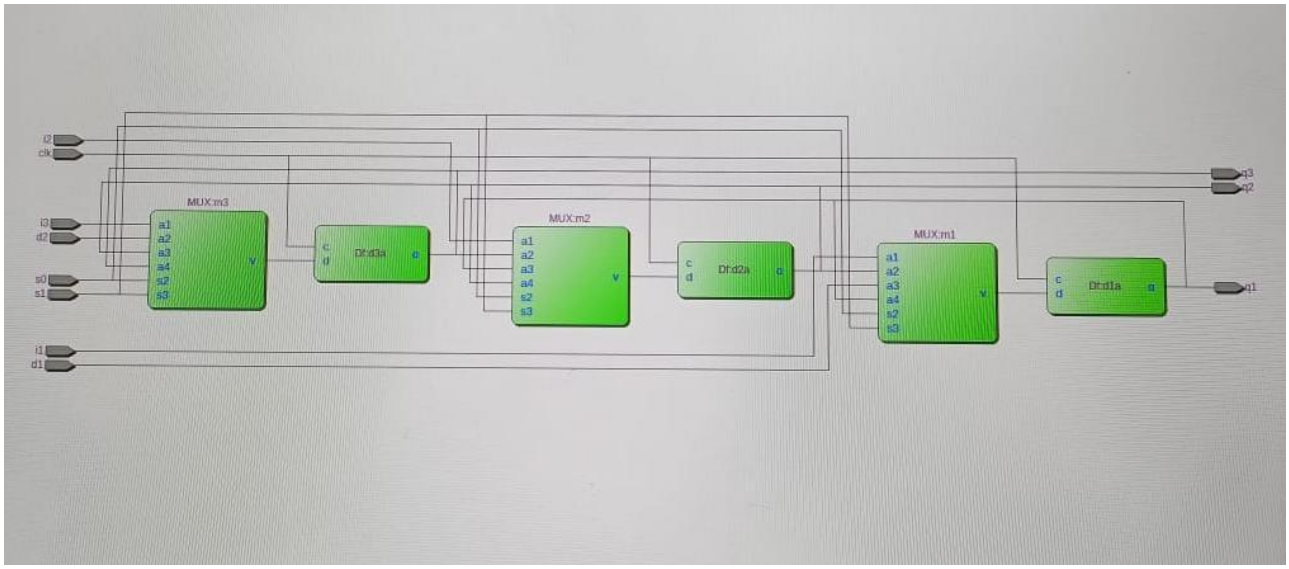
Components Used: CPLD MAX3000A Board, JTAG port, Type-B USB cable, ALTERA BUS Blaster cable, and Bus Blaster HDL code were the components utilized (for CPLD).

Circuit Diagram: 3-bit Universal Shift Register



Snapshots Of Gate-level Netlist:

3-bit Universal Shift Register in structural modeling style



VHDL Code:

3-bit Universal Shift Register in structural modeling style

```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.ALL;
3
4   entity shift_register is
5   port(s1,s0,i1,i2,i3,d1,d2,clk:in std_logic;
6        q1,q2,q3:out std_logic);
7   end shift_register;
8
9   architecture structure of shift_register is
10  component Df
11  port(d,c: in std_logic;
12  q: out std_logic);
13  end component;
14  component MUX
15  port(s2,s3,a1,a2,a3,a4: in std_logic;
16  y:out std_logic);
17  end component;
18   signal c1,c2,c3,c4,y1,y2,y3 : std_logic;
19   begin
20   m1:MUX port map(s0,s1,i1,c1,d1,c2,y1);
21   m2:MUX port map(s0,s1,i2,c4,c2,c1,y2);
22   m3:MUX port map(s0,s1,i3,d2,c1,c4,y3);
23   d1a: Df port map(y1,clk,c2);
24   d2a: Df port map(y2,clk,c1);
25   d3a: Df port map(y3,clk,c4);
26   q1<=c2;
27   q2<=c1;
28   q3<=c4;
29   end structure;
30
31   library IEEE;
32   use IEEE.STD_LOGIC_1164.ALL;
33
34  entity Df is
35  port(d,c,rst:in std_logic;
36       q:out std_logic);
37  end Df;
38
39  architecture Behavioral of Df is
40  begin
41  process(rst,c)
42   begin
43
44  if(rst='1') then
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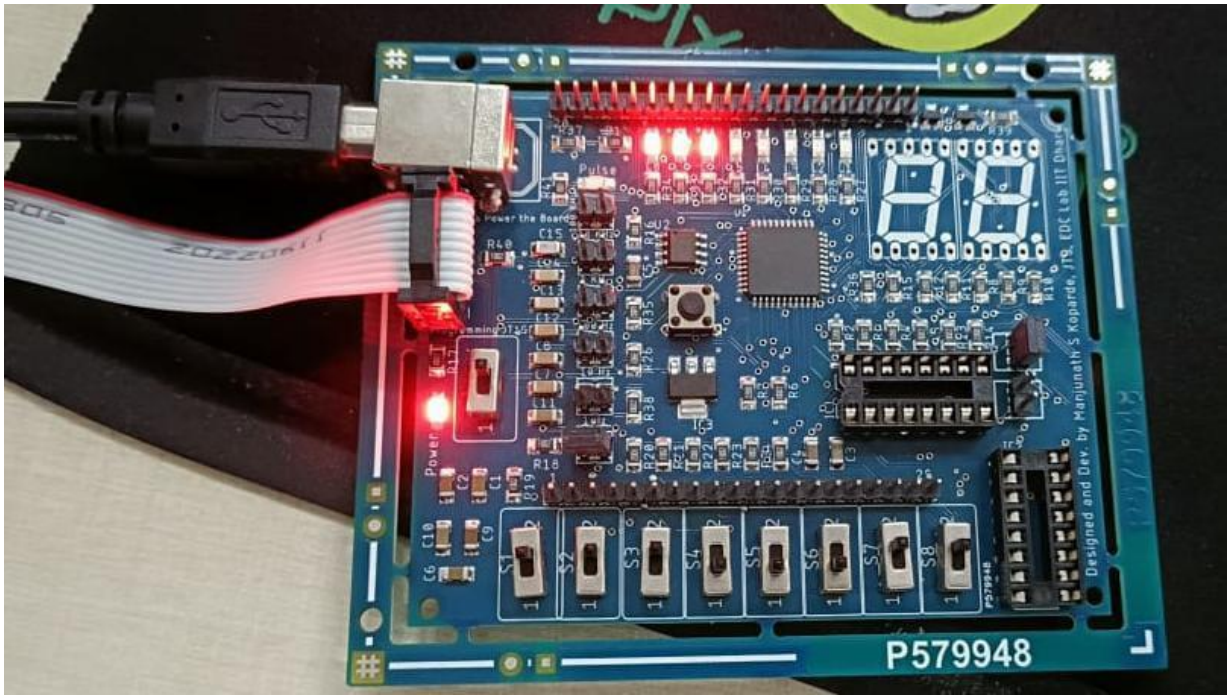
```
46      q<='0';
47    elsif(c'event and c='1') then
48
49      q<=d;
50    end if;
51    end process;
52    end Behavioral;
53
54    library IEEE;
55    use IEEE.STD_LOGIC_1164.ALL;
56  entity MUX is
57  port(s2,s3,a1,a2,a3,a4: in std_logic;
58    y:out std_logic);
59    end MUX;
60  architecture behavioral of MUX is
61  begin
62  process(s2,s3)
63    begin
64  if(s2='0' and s3='0') then
65    y<=a1;
66  elsif(s2='1' and s3='0') then
67    y<=a2;
68  elsif(s2='0' and s3='1') then
69    y<=a3;
70  elsif(s2='1' and s3='1') then
71    y<=a4;
72    end if;
73    end process;
74    end behavioral;
```

CPLD Board Image:



Results and Conclusion: Acquired a thorough understanding of how to create VHDL code using the circuit's logic. By loading the code onto a CPLD board, the 3-bit Universal Shift Register's functioning was tested using this information to construct the code.