

# LAB 5 - REPORT

## Designing & Implementation Of Adders & Subtractors

**Aim:** *Implementing the circuit for a given question using the ICs and constructing adders & subtractors*

1. Design and implement a half subtractor circuit using a minimum number of two (2) input NAND gates.
2. Familiarize 74LS83 IC and implement a controlled 3-bit adder/subtractor circuit which is controlled by signal CTRL using 74LS83 and a minimum number of 2-input gates.

**Summary of the Experiment:** *Solving the given circuit problem using the appropriate minimum number of NAND gates and also implementing the controlled 3-bit adder/subtractor by using 74LS83 IC by considering the given conditions such as the minimum number of 2-input gates*

**Components Used::** *IC 7400, IC 7486, IC 74LS83, 2Kohm resistor array -2, DIP switches, LED displays, breadboard, multi-meter, and power supply.*

**Circuit Diagrams & Snapshots :**

9/02/23

## Lab - 5

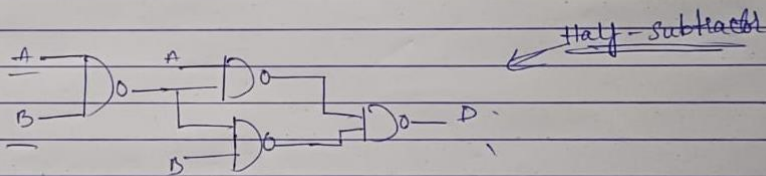
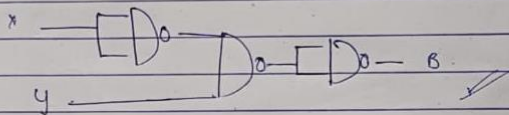
2-bit subtractor is

1)

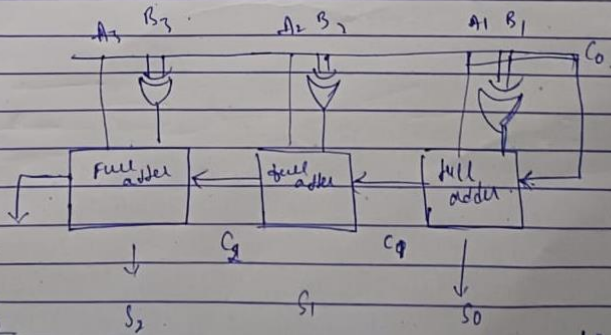
x	y	D	B
0	0	0	0
0	1	1	1
1	0	0	0
1	1	0	0

$$D = x \oplus y$$

$$B = \bar{x}y$$



2)



$$\begin{array}{r} 5 \\ -4 \\ \hline 1 \end{array}$$

1103

$$\begin{array}{r} A_3 \ A_2 \ A_1 \\ 1 \ 0 \ 0 \\ 1 \ 0 \ 1 \\ \hline 1 \ 0 \ 0 \ 1 \end{array}$$

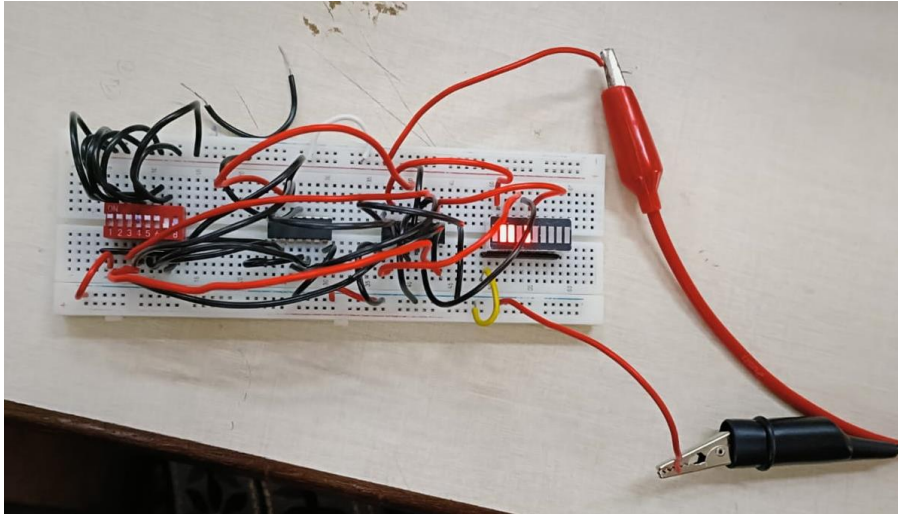
MSS  $\rightarrow$  1001  $\rightarrow$  255

$$\begin{array}{r} 7 \ 7 \\ 7 \ 7 \\ \hline 1 \ 1 \ 1 \end{array}$$

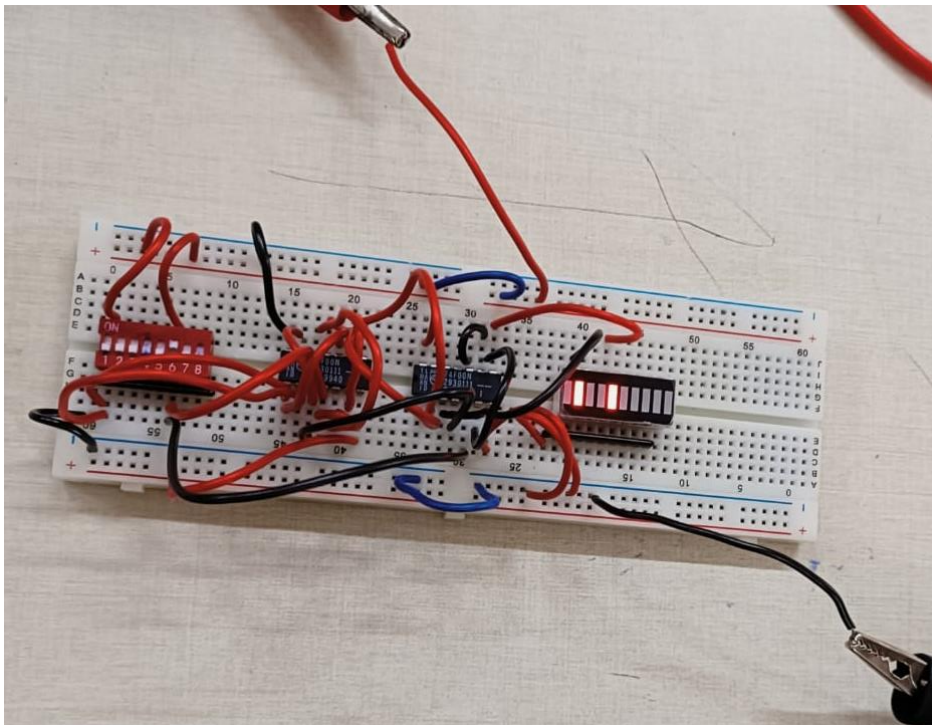
$$\begin{array}{r} 1 \ 1 \ 1 \\ 1 \ 1 \ 0 \\ \hline 1 \ 1 \ 1 \end{array}$$

MSB  $\rightarrow$  1110  $\rightarrow$  LSB

## Half Subtractor



## 3-Bit Adder/Subtractor



## Results and Discussions :

- *X and Y are inputs, and D and B are the difference and borrow.*

- $D = XY' + X'Y$   $B = X'Y$
- Here 3 NAND gates are required to get B as output and 4 to get D as output.
- So we require a minimum of 7 NAND gates to design half subtractor.
- To implement a 3-bit adder/subtractor we need 74LS83 IC, and 3 XOR gates i.e., one 7486 IC.
- If CTRL=0 then the circuit acts as an adder and for 1 it acts as a subtractor. We use XOR gates to get the 2's complement.
- We use (A1 B1) (A2 B2) and (A3 B3) of 74LS83 IC.

### **Conclusion:**

- ❖ Half subtractor is implemented using a minimum of 7 NAND gates.
- ❖ A 3-bit adder/subtractor is implemented using 74LS83 IC which is controlled by signal CTRL using 74LS83 and 3 XOR gates of.
- ❖ For CTRL=0 adder is implemented and for 1 subtractor is implemented.