LAB 8 - REPORT

Aim:

Forming VHDL code into CPLD and checking the code functionality.

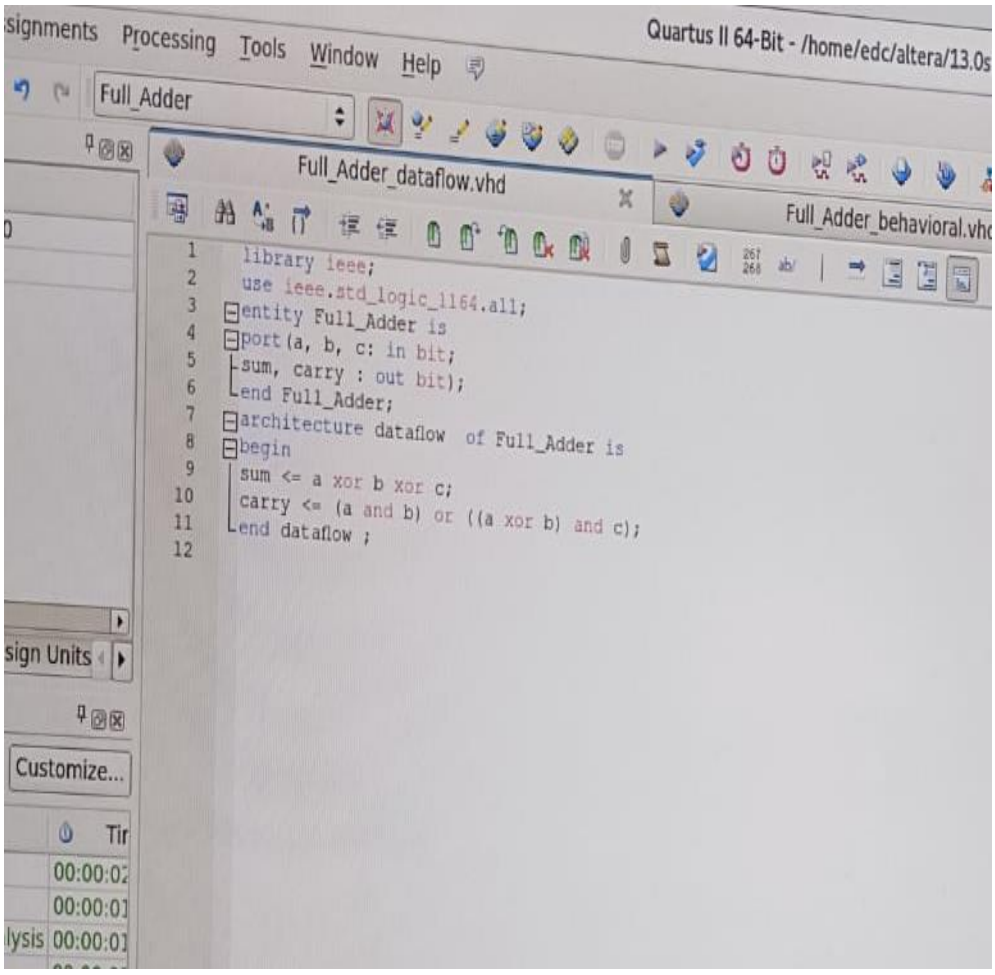
Summary of the experiment:

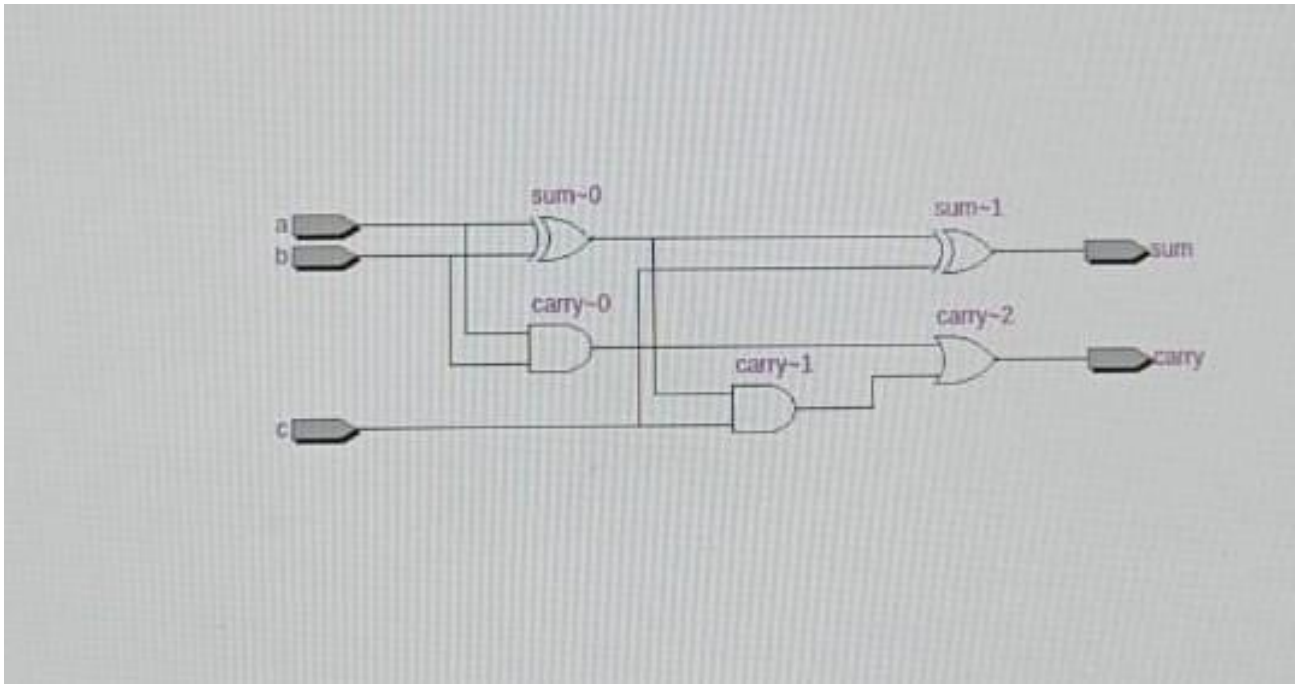
Conversion of VHDL code to CPLD and verifying the code functionality. It is supported by 3 different modelling styles: Dataflow, Behavioural, and Structural.

Components used:

CPLD MAX3000A Board, JTAG port, Type-B USB cable, ALTERA BUS Blaster cable, Bus blaster HDL code (for CPLD).

1.FULL ADDER WITH DATA FLOW MODELLING

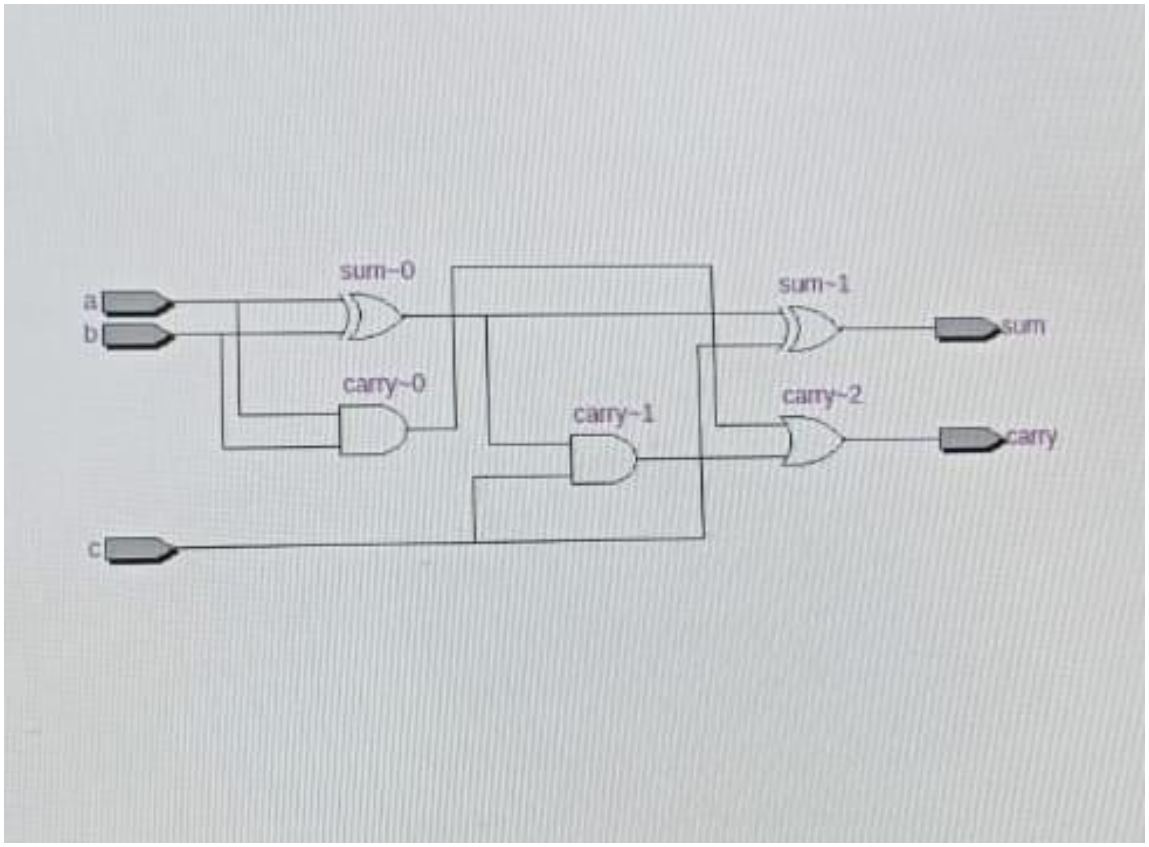




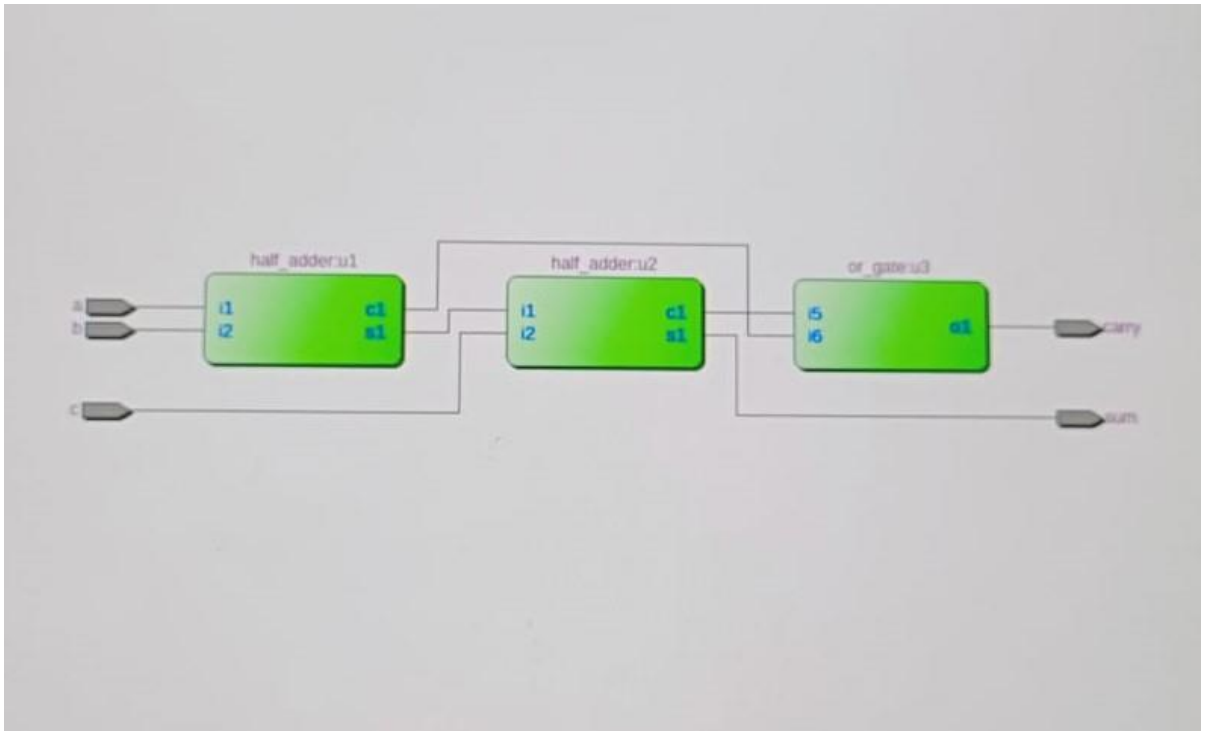
2. FULL ADDER WITH BEHAVIORAL MODELLING

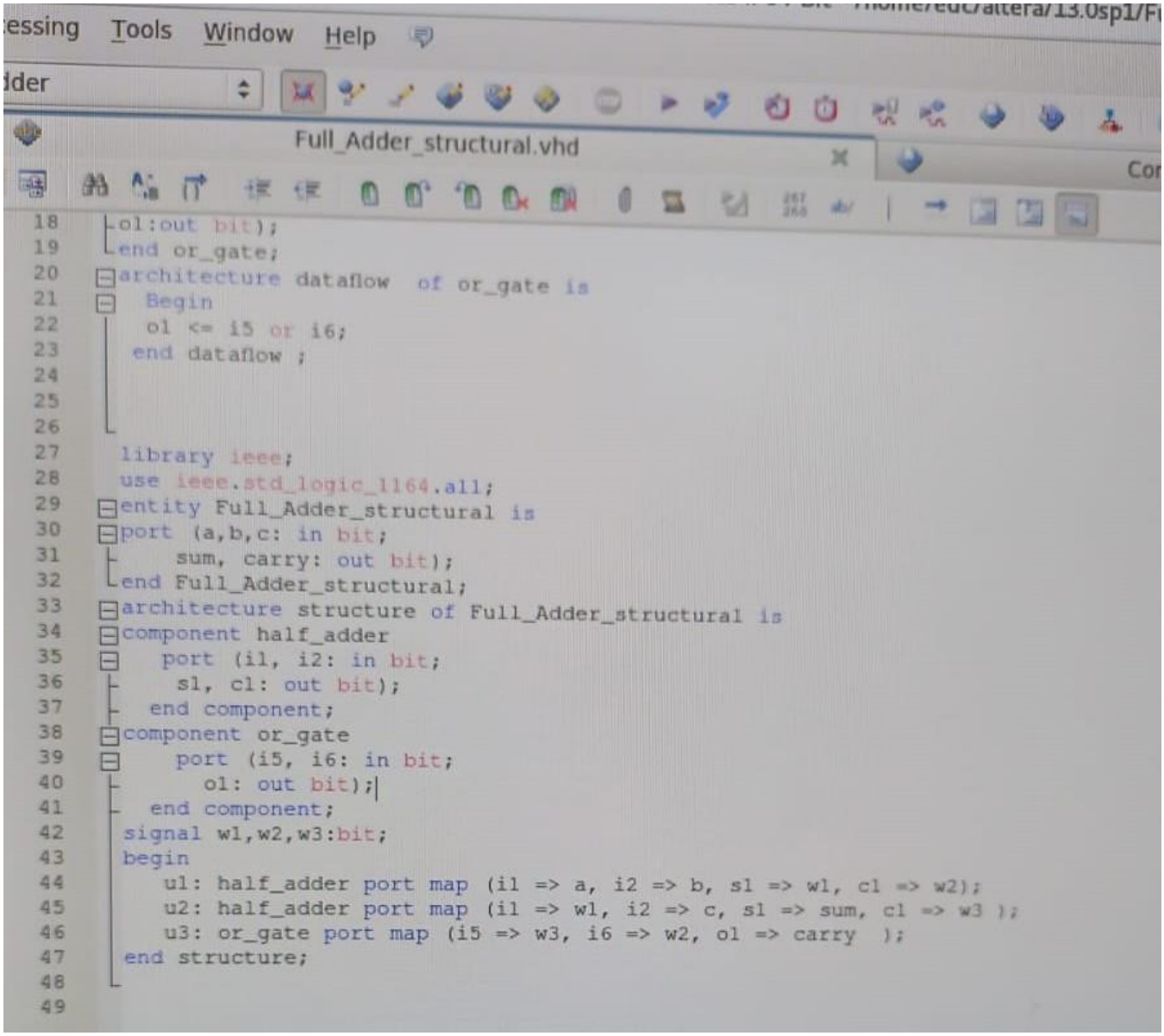
Full_Adder_dataflow.vhd | Full_Adder_behavioral.vhd

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   entity Full_Adder_behavioral is
4      port(a,b,c: in bit;
5           sum, carry: out bit);
6      end Full_Adder_behavioral;
7   architecture behavior of Full_Adder_behavioral is
8   begin
9      c1: process (a,b,c)
10        begin
11        if a='1' then
12           sum <= b xnor c ;
13           carry <= b or c ;
14        else
15           sum <= b xor c ;
16           carry <= b and c ;
17        end if ;
18     end process c1 ;
19  end behavior;
```

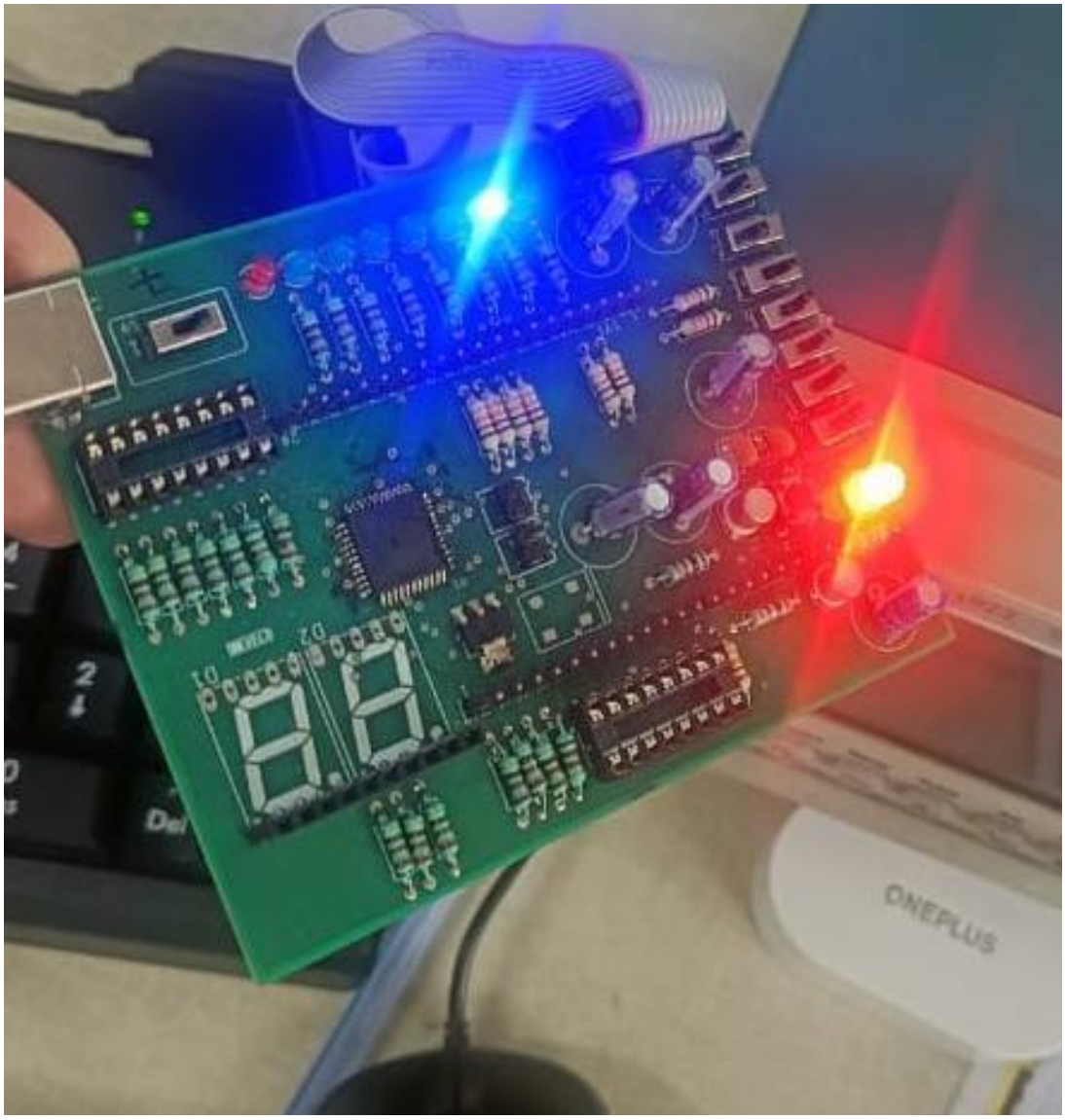


3. FULL ADDER WITH STRUCTURAL MODELLING





Snapshots of Circuit :



Results and Conclusion:

1. We got to know about dataflow, behavioural and structural modelling. We have converted VHDL to CPLD.
2. We knew about VHDL and CPLD.
3. We have also checked the code function correctly. We have made a full adder circuit using that knowledge and modelling