

LAB 8 - REPORT

Aim:

Forming VHDL code into CPLD and checking the code functionality.

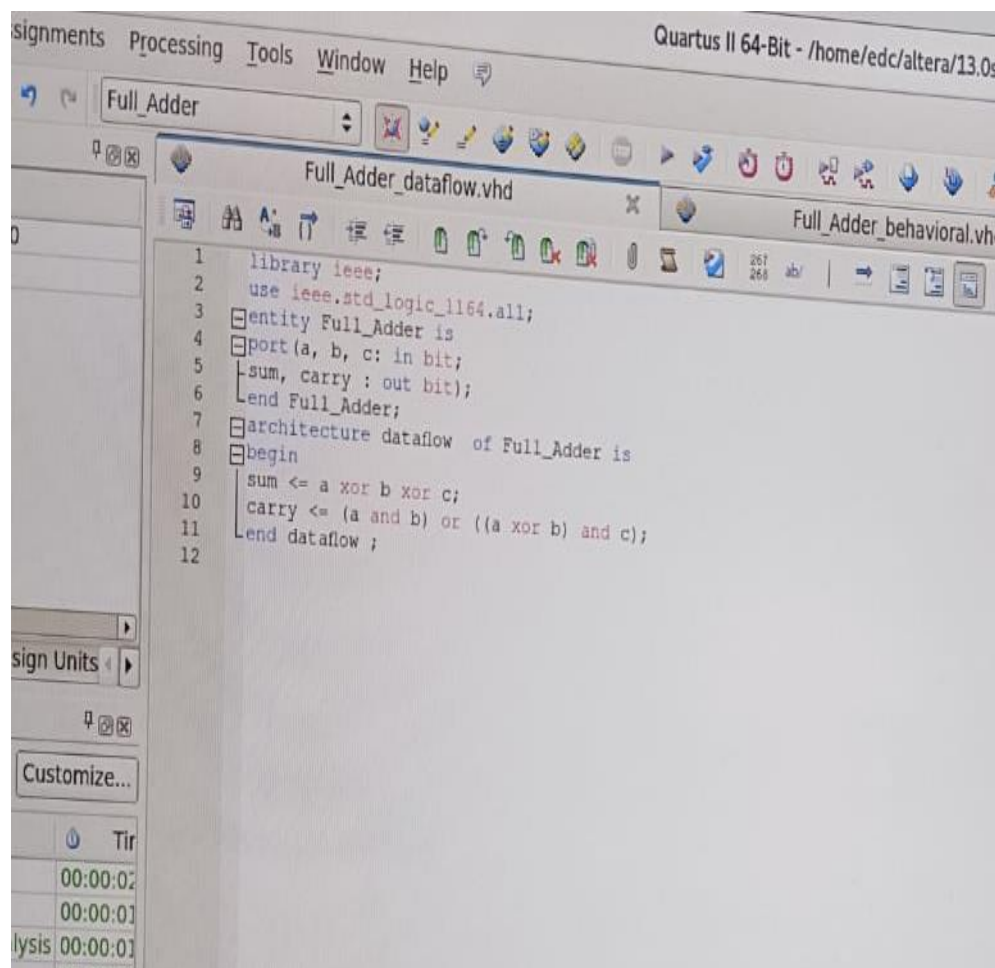
Summary of the experiment:

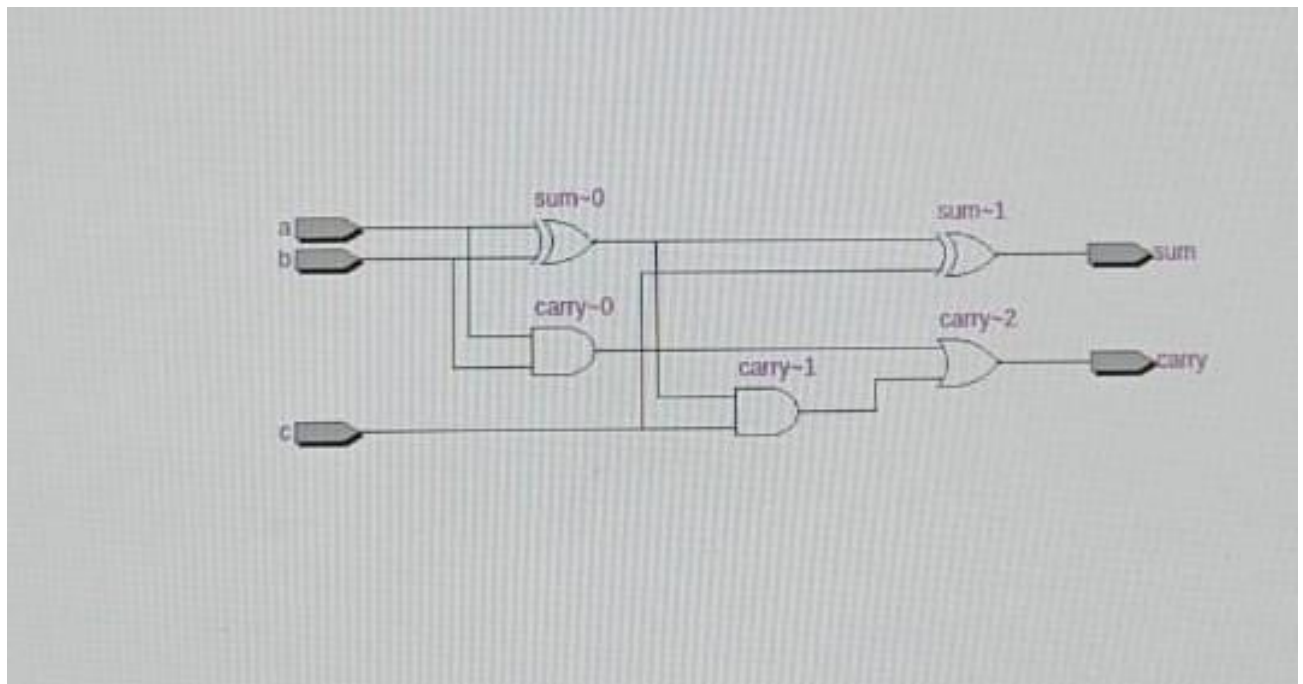
Conversion of VHDL code to CPLD and verifying the code functionality. It is supported by 3 different modelling styles: Dataflow, Behavioural, and Structural.

Components used:

CPLD MAX3000A Board, JTAG port, Type-B USB cable, ALTERA BUS Blaster cable, Bus blaster HDL code (for CPLD).

1. FULL ADDER WITH DATA FLOW MODELLING



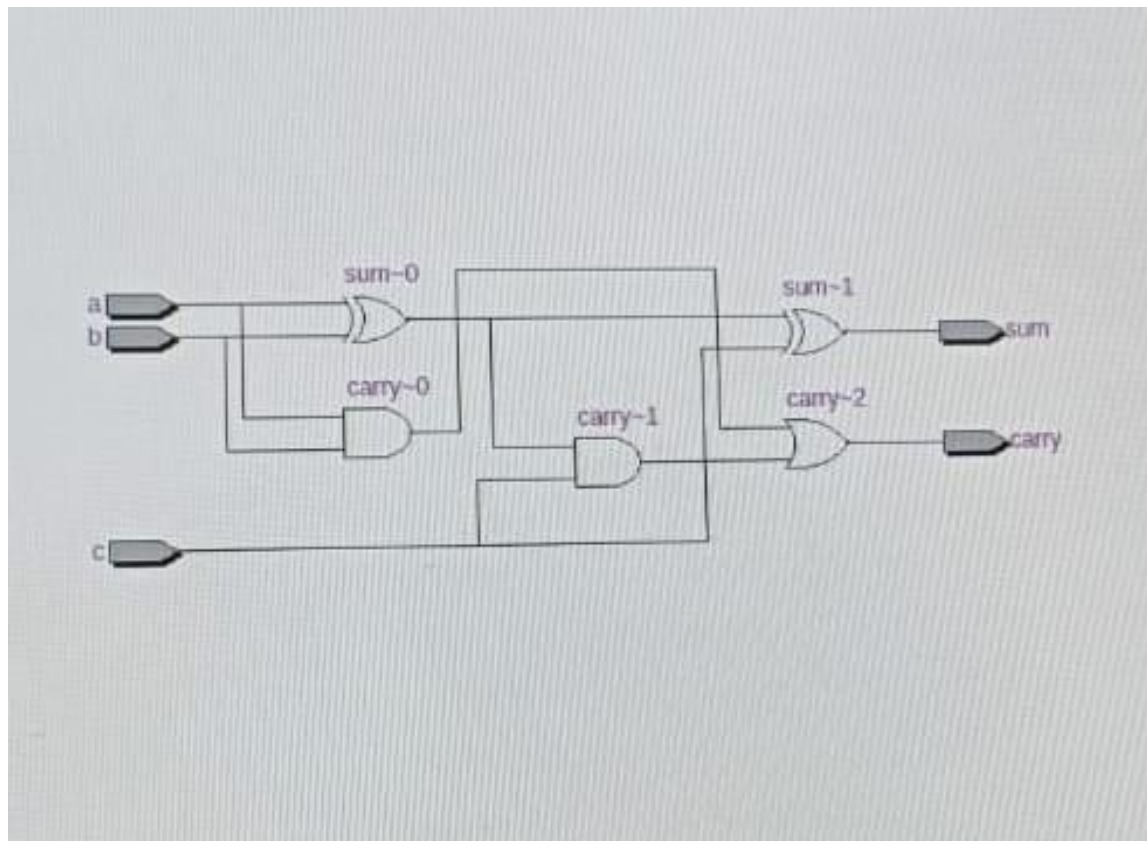


2. FULL ADDER WITH BEHAVIORAL MODELLING

```

1  library ieee;
2  use ieee.std_logic_1164.all;
3  entity Full_Adder_behavioral is
4  port (a,b,c: in bit;
5        sum, carry: out bit);
6  end Full_Adder_behavioral;
7  architecture behavior of Full_Adder_behavioral is
8  begin
9  cl: process (a,b,c)
10     begin
11         if a='1' then
12             sum <= b xnor c ;
13             carry <= b or c ;
14         else
15             sum <= b xor c ;
16             carry <= b and c ;
17         end if ;
18     end process cl ;
19 end behavior;

```

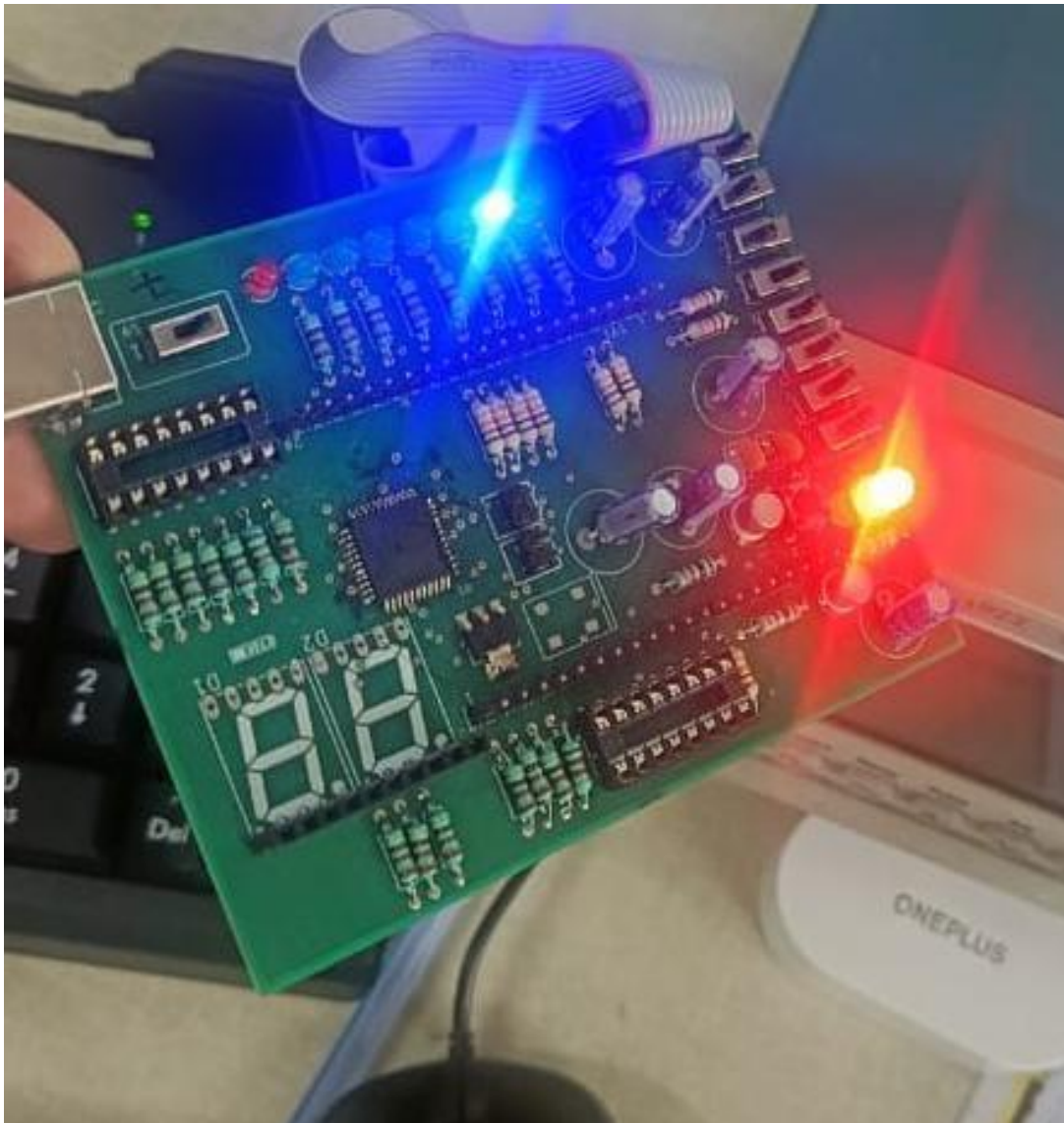


3. FULL ADDER WITH STRUCTURAL MODELLING



```
Processing Tools Window Help
Full_Adder_structural.vhd
18 ol:out bit);
19 end or_gate;
20 architecture dataflow of or_gate is
21 begin
22     ol <= i5 or i6;
23 end dataflow ;
24
25
26
27 library ieee;
28 use ieee.std_logic_1164.all;
29 entity Full_Adder_structural is
30 port (a,b,c: in bit;
31       sum, carry: out bit);
32 end Full_Adder_structural;
33 architecture structure of Full_Adder_structural is
34 component half_adder
35 port (i1, i2: in bit;
36       s1, c1: out bit);
37 end component;
38 component or_gate
39 port (i5, i6: in bit;
40       o1: out bit);
41 end component;
42 signal w1,w2,w3:bit;
43 begin
44     u1: half_adder port map (i1 => a, i2 => b, s1 => w1, c1 => w2);
45     u2: half_adder port map (i1 => w1, i2 => c, s1 => sum, c1 => w3 );
46     u3: or_gate port map (i5 => w3, i6 => w2, o1 => carry );
47 end structure;
48
49
```

Snapshots of Circuit :



Results and Conclusion:

1. We got to know about dataflow, behavioural and structural modelling. We have converted VHDL to CPLD.
2. We knew about VHDL and CPLD.
3. We have also checked the code function correctly. We have made a full adder circuit using that knowledge and modelling