DESCRIPTION

PT6324 is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/8 to 1/16 duty factor housed in 52-pin plastic LQFP. 24 segment output lines, 16 grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to PT6324 via a three-line serial interface.

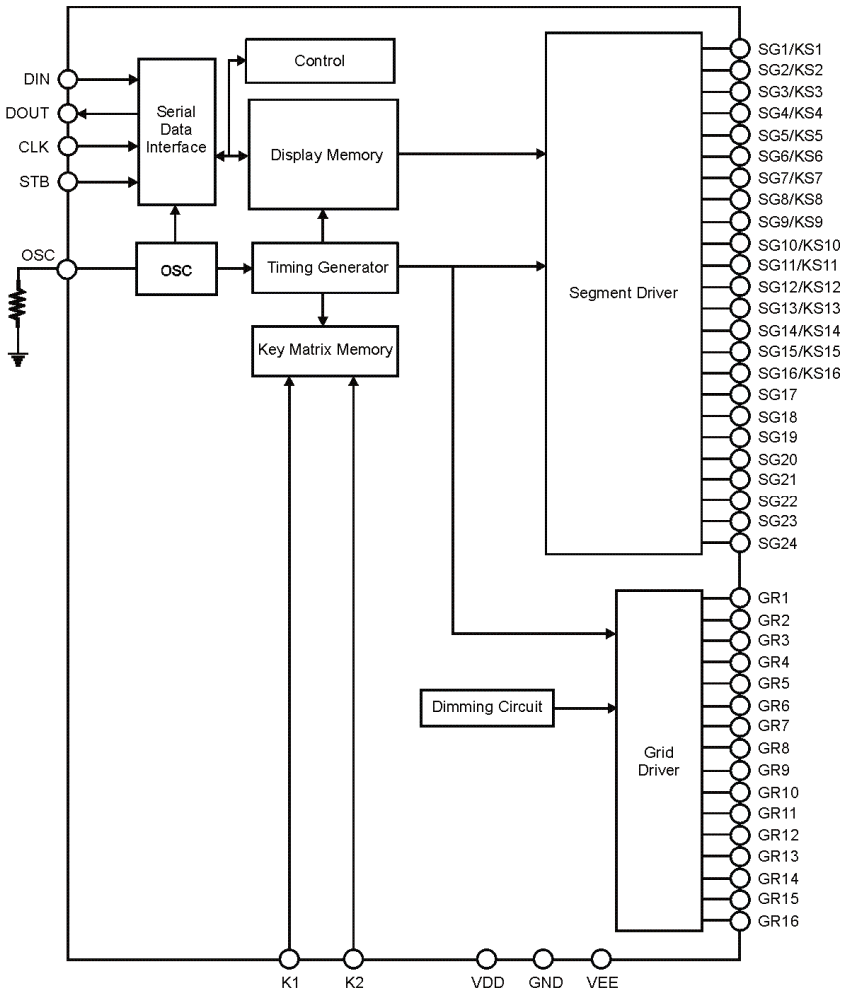
APPLICATIONS

- Microcomputer peripheral devices
- Digital Audio/Video system: CD/MD/VCD/DVD players
- Car audio
- VCR
- Electric scale meter
- P.O.S.
- Electronic equipment with instructional display

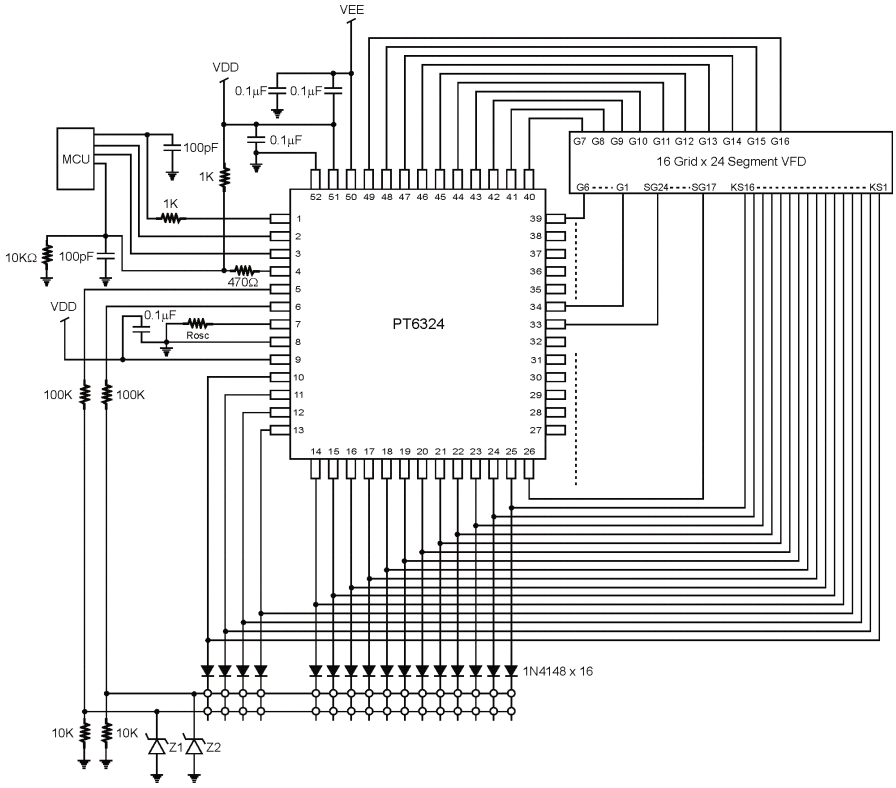
FEATURES

- CMOS technology
- Low power consumption
- Wide operating voltage VDD=2.7V~5.5V
- Key scanning (16 x 2 matrix)
- Display modes: (24 segments, 8 digits to 24 segments, 16 digits)
- 8-Step dimming circuitry
- Serial interface for Clock, Data Input, Data Output, Strobe pins
- No external resistors needed for driver outputs

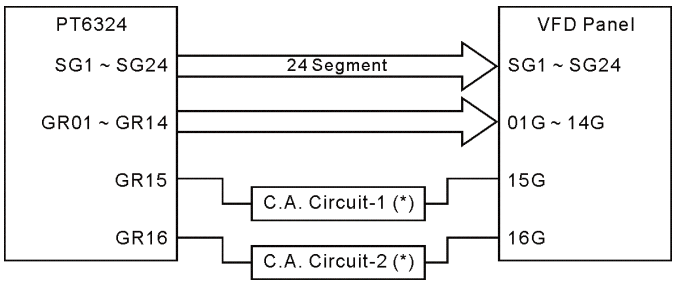
BLOCK DIAGRAM



16-GRID X 24-SEGMENT VFD APPLICATION CIRCUIT

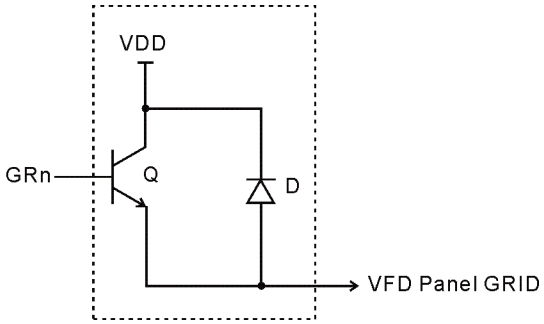


Notes:
1. The value of Rosc is depend on PT6324 IC chip supply voltage of V_{DD} (Rosc=82KΩ, when V_{DD}=5V; Rosc=100KΩ, when V_{DD}=3.3V).
2. Z1, Z2=Zener diode 5.1V
3. Please adding the current amplifying circuit as following figure when I_{OHGR}>15mA on VFD panel for high brightness issue.



*=C.A. Circuit=Current amplifying circuit

C.A. Circuit-1 & C.A. Circuit-2 Ex.:

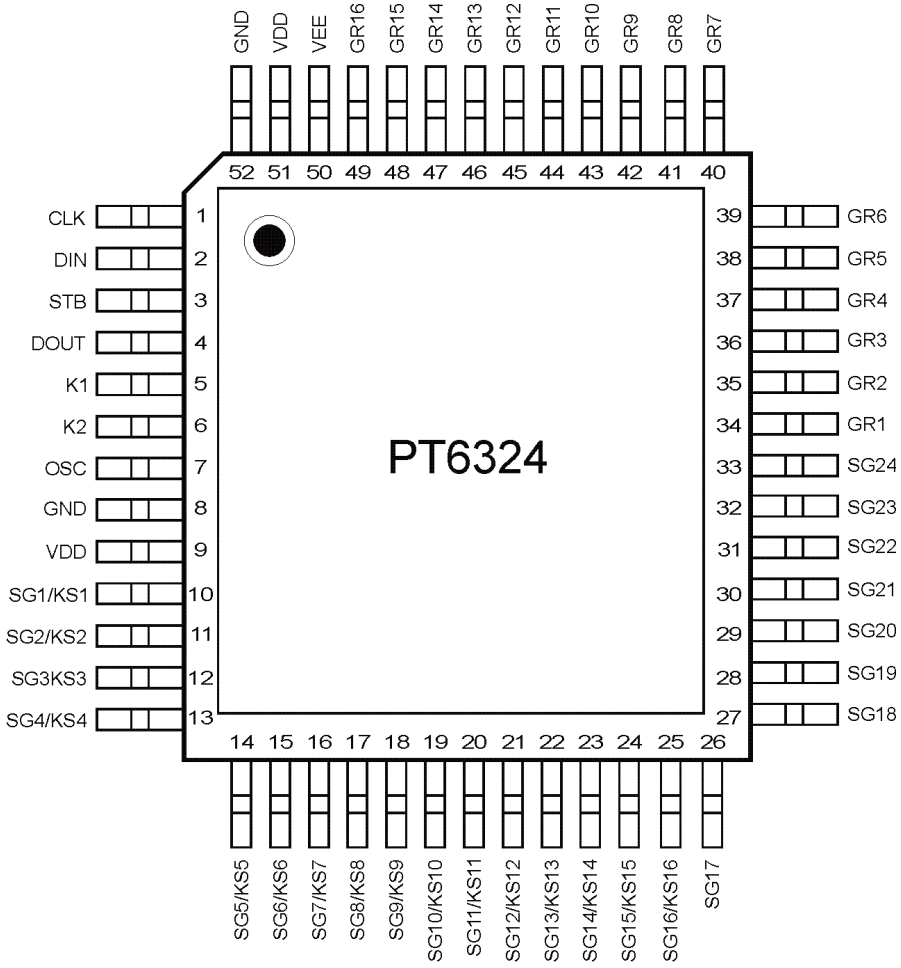


Parts recommended:
- Q=SAMSUNG-KSR1105 (General fast switching transistor)
- D=HITACHI-HSM221C (General fast recovery diode)

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6324-LQ	52-Pin, LQFP	PT6324-LQ

PIN CONFIGURATION



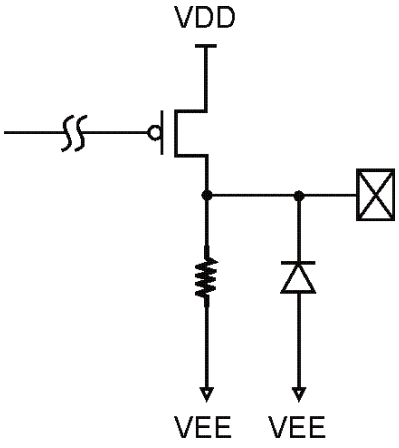
PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
CLK	I	Clock input pin This pin reads serial data at the rising edge and outputs data at the falling edge.	1
DIN	I	Data input pin When this pin acts as input pin, serial data is inputted at the rising edge of the shift clock (starting from the lower bit)	2
STB	I	Serial interface strobe pin The data input after the STB has fallen is processed as a command. When this in is “HIGH”, CLK is ignored.	3
DOUT	O	Data output pin (N-channel, Open-drain) When this pin acts as output pin, serial data is outputted at the falling edge of the shift clock (starting from the lower bit)	4
K1 to K2	I	Key data input pins The data inputted to these pins is latched at the end of the display cycle.	5, 6
OSC	I	Oscillator input pin A resistor is connected to this pin to determine the oscillation frequency.	7
GND	-	Ground pin	8, 52
VDD	-	Logic power supply	9, 51
SG1/KS1 to SG16/KS16	O	High-voltage segment output pins Also acts as the key source	10 to 25
SG17 to SG24	O	High-voltage segment output pins	26 to 33
GR1 to GR16	O	High-voltage grid output pins	34 to 49
VEE	-	Pull-down level	50

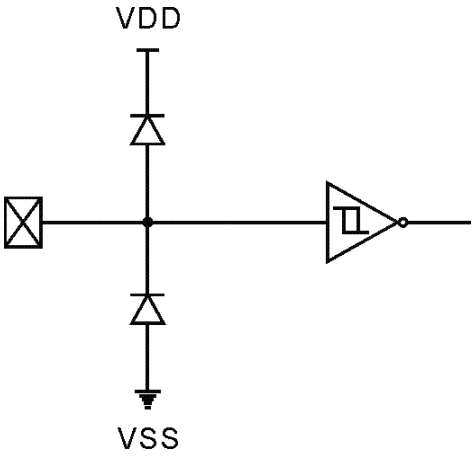
INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below:

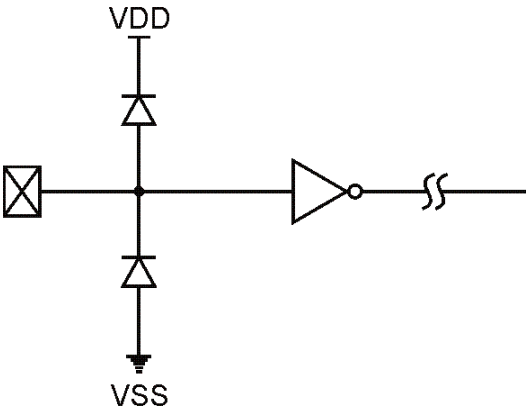
Output Pins: SGn/GRn



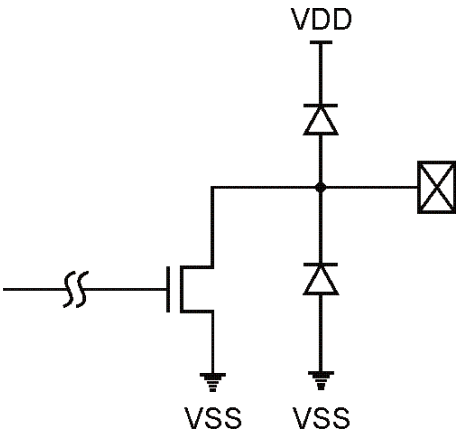
Input Pins: DIN, CLK, STB



Input Pins: K1, K2



Output Pin: DOUT



FUNCTION DESCRIPTION

COMMANDS

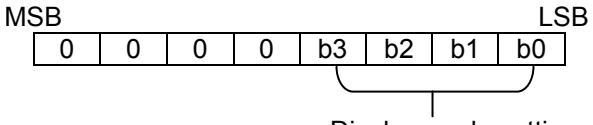
Commands determine the display mode and status of PT6324. A command is the first byte (b0 to b7) inputted to PT6324 via the DIN Pin after STB Pin has changed from “HIGH” to “LOW” State. If for some reason the STB Pin is set to “HIGH” while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DISPLAY MODE SETTING COMMANDS

PT6324 provides 8 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6324 via the DIN Pin when STB is “LOW”. However, for these commands, the bits 5 to 8 (b4 to b7) are given a value of “0”.

The Display Mode Setting Commands determine the number of segments and grids to be used (1/8 to 1/16 duty, 24 segments). When these commands are executed, the display is forcibly turned off. A display command “ON” must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned “ON”, the 16-digit, 24-segment modes is selected.



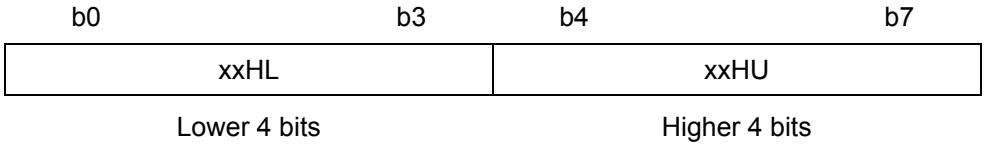
Display mode settings:

0000: 8 digits, 24 segments
1000: 9 digits, 24 segments
1001: 10 digits, 24 segments
1010: 11 digits, 24 segments
1011: 12 digits, 24 segments
1100: 13 digits, 24 segments
1101: 14 digits, 24 segments
1110: 15 digits, 24 segments
1111: 16 digits, 24 segments

DISPLAY MODE AND RAM ADDRESS

Data transmitted from an external device to PT6324 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6324 are given below in 8 bits unit.

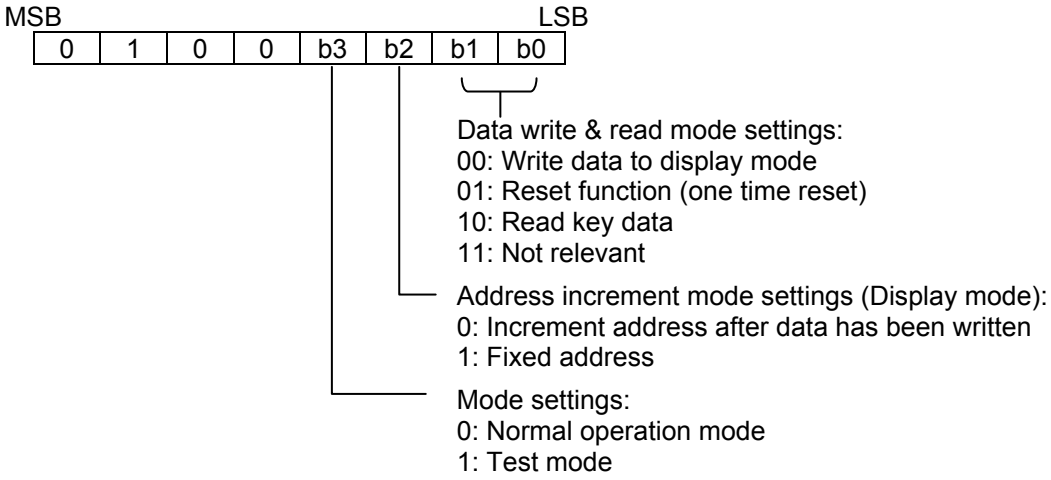
SG1 SG4	SG5 SG8	SG9 SG12	SG13 SG16	SG17 SG20	SG21 SG24	
00HL	00HU	01HL	01HU	02HL	02HU	DIG1
03HL	03HU	04HL	04HU	05HL	05HU	DIG2
06HL	06HU	07HL	07HU	08HL	08HU	DIG3
09HL	09HU	0AHL	0AHU	0BHL	0BHU	DIG4
0CHL	0CHU	0DHL	0DHU	0EHL	0EHU	DIG5
0FHL	0FHU	10HL	10HU	11HL	11HU	DIG6
12HL	12HU	13HL	13HU	14HL	14HU	DIG7
15HL	15HU	16HL	16HU	17HL	17HU	DIG8
18HL	18HU	19HL	19HU	1AHL	1AHU	DIG9
1BHL	1BHU	1CHL	1CHU	1DHL	1DHU	DIG10
1EHL	1EHU	1FHL	1FHU	20HL	20HU	DIG11
21HL	21HU	22HL	22HU	23HL	23HU	DIG12
24HL	24HU	25HL	25HU	26HL	26HU	DIG13
27HL	27HU	28HL	28HU	29HL	29HU	DIG14
2AHL	2AHU	2BHL	2BHU	2CHL	2CHU	DIG15
2DHL	2DHU	2EHL	2EHU	2FHL	2FHU	DIG16



COMMAND 2: DATA SETTING COMMANDS

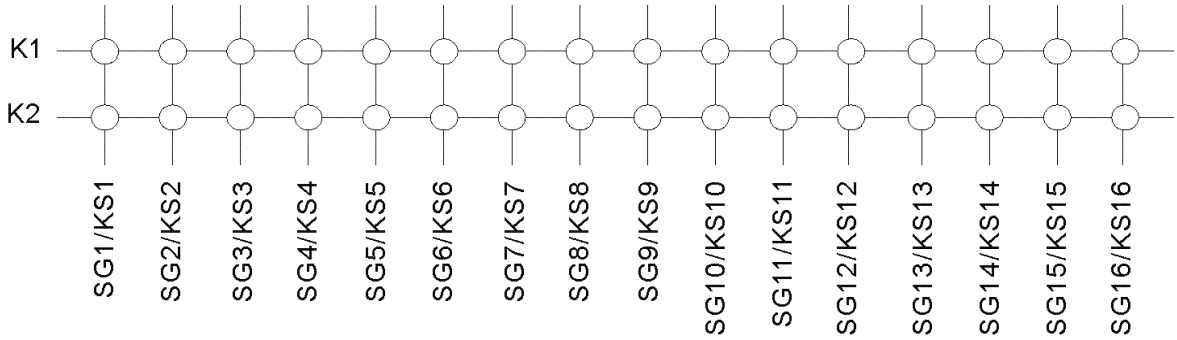
The Data Setting Commands executes the Data Write or Data Read Modes for PT6324. The data Setting Command, the bits 5 and 6 (b4, b5) are given the value of “0”, bit 7 (b6) is given the value of “1” while bit 8 (b7) is given the value of “0”. Please refer to the diagram below.

When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of “0”.



PT6324 KEY MATRIX & KEY INPUT DATA STORAGE RAM

PT6324 Key Matrix consists of 16 x 2 array as shown below:



Each data inputted by each key are stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG16, b7) has been read, the least significant bit of the next data (SG1, b0) is read.

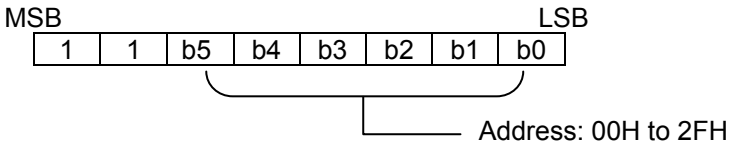
K1……K2	K1……K2	K1……K2	K1……K2
SG1/KS1	SG2/KS2	SG3/KS3	SG4/KS4
SG5/KS5	SG6/KS6	SG7/KS7	SG8/KS8
SG9/KS9	SG10/KS10	SG11/KS11	SG12/KS12
SG13/KS13	SG14/KS14	SG15/KS15	SG16/KS16
b0……..b1	b2……b3	b4……..b5	b6……..b7

Reading Sequence

COMMAND 3: ADDRESS SETTING COMMANDS

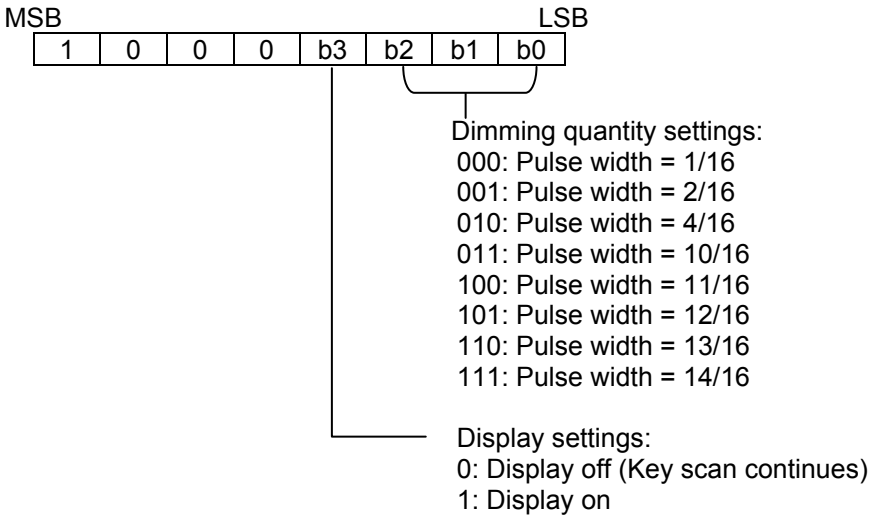
Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of “00H” to “2FH”. If the address is set to 30H or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at “00H”.

Please refer to the diagram below.



COMMAND 4: DISPLAY CONTROL COMMANDS

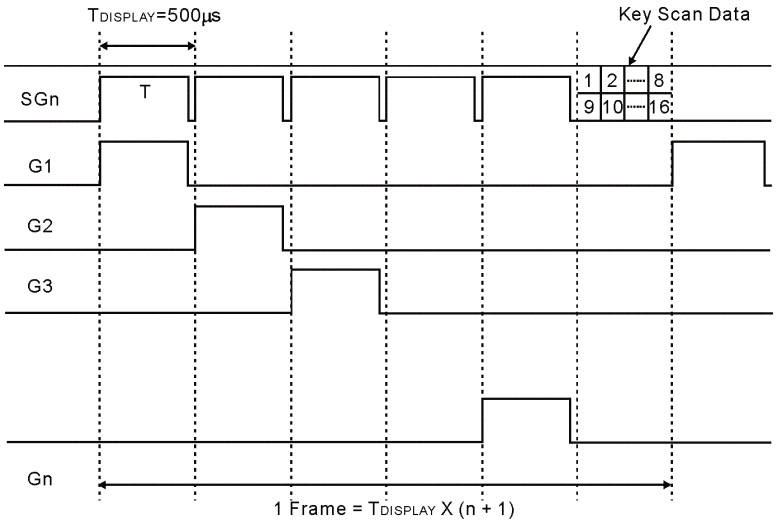
The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF.



DISPLAY TIMING

The Key Scanning and display timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the 16 x 2 matrix is stored in the RAM.

Internal Operating Frequency (fosc) = 224/T

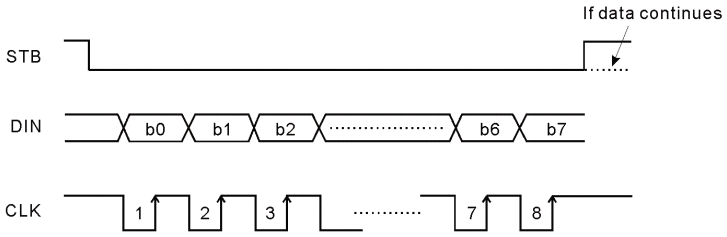


Note: T is the width of Segment only

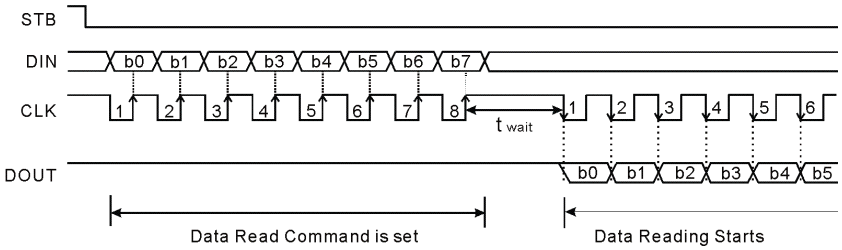
SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6324 serial communication format. The DIN/DOUT Pin is an Schmitt trigger circuit and N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1KΩ to 10KΩ) must be connected to DIN/DOUT when using key scan function.

Reception (Data/Command Write)



Transmission (Data Read)

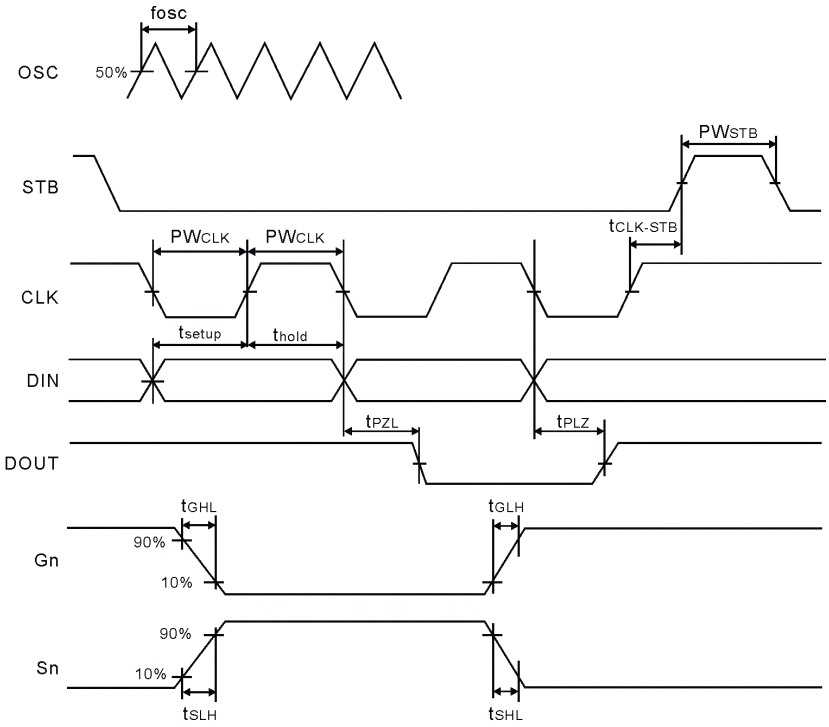


where: twait (waiting time) ≥ 1μs

It must be noted that when the data is read, the waiting time (twait) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1μs.

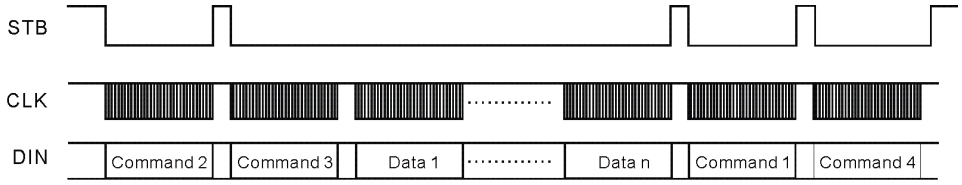
SWITCHING CHARACTERISTIC WAVEFORM

PT6324 Switching Characteristics Waveform is given below.



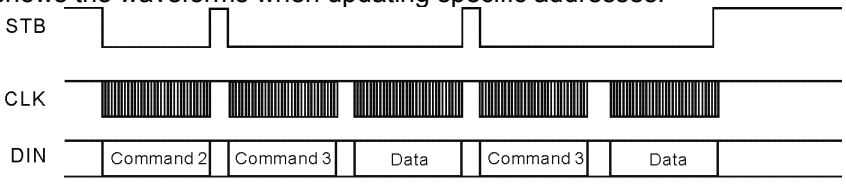
APPLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.



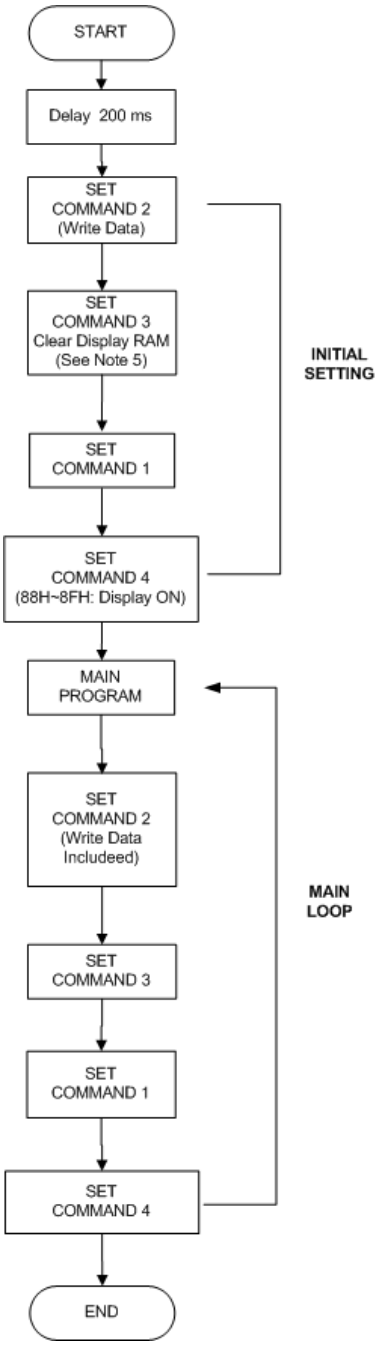
where: Command 1: Display Mode Setting Command
Command 2: Data Setting Command
Command 3: Address Setting Command
Data 1 to n : Transfer Display Data (48 Bytes max.)
Command 4: Display Control Command

The following diagram shows the waveforms when updating specific addresses.



where: Command 2: Data Setting Command
Command 3: Address Setting Command
Data: Display Data

RECOMMENDED SOFTWARE FLOWCHART



Notes:
1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V_{DD}	-0.3 to +7	V
Driver supply voltage	V_{EE}	V_{DD} +0.3 to V_{DD} -40	V
Logic input voltage	V_I	-0.3 to V_{DD} +0.3	V
VFD driver output voltage	V_O	V_{EE} -0.3 to V_{DD} +0.3	V
VFD driver output current	I_{OVFD}	-40 (Grid); -15 (Segment)	mA
Operating temperature	Topr	-40 to +85	℃
Storage temperature	Tstg	-65 to +150	℃

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	V_{DD}	2.7	5	5.5	V
High-level input voltage (VDD=5V)	V_{IH}	0.75V_{DD}	-	V_{DD}	V
Low-level input voltage (VDD=5V)	V_{IL}	0	-	0.25V_{DD}	V
High-level input voltage (VDD=3.3V)	V_{IH}	0.8V_{DD}	-	V_{DD}	V
Low-level input voltage (VDD=3.3V)	V_{IL}	0	-	0.2V_{DD}	V
Driver supply voltage	V_{EE}	V_{DD} -35	-	0	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, V_{DD}=5V, GND=0V, V_{EE}=V_{DD}-35 V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Low-level output voltage	V_{OLDOUT}	D_{OUT} I_{OLDOUT}=4mA	-	-	0.4	V
High-level output current	I_{OHSG}	V_O=V_{DD} -2V, SG1 to SG24	-3	-	-	mA
High-level output current	I_{OHGR}	V_O=V_{DD} -2V, GR1 to GR16	-15	-	-	mA
High-level input voltage	V_{IH}	-	0.75V_{DD}	-	-	V
Low-level input voltage	V_{IL}	-	-	-	0.25V_{DD}	V
Input current	I_I	V_{DD} or GND	-	-	±1	μA
Dynamic current consumption	I_{DDdyn}	Under no load, Display OFF	-	-	5	mA

(Unless otherwise stated, V_{DD}=3.3V, GND=0V, V_{EE}=V_{DD}-35 V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Low-level output voltage	V_{OLDOUT}	D_{OUT} I_{OLDOUT}=4mA	-	-	0.4	V
High-level output current	I_{OHSG}	V_O=V_{DD} -2V, SG1 to SG24	-1.5	-	-	mA
High-level output current	I_{OHGR}	V_O=V_{DD} -2V, GR1 to GR16	-6	-	-	mA
High-level input voltage	V_{IH}	-	0.8V_{DD}	-	-	V
Low-level input voltage	V_{IL}	-	-	-	0.2V_{DD}	V
Input current	I_I	V_{DD} or GND	-	-	±1	μA
Dynamic current consumption	I_{DDdyn}	Under no load, Display OFF	-	-	3	mA

TIMING CHARACTERISTICS

(Unless otherwise specified, V_{DD}=5V, GND=0V, V_{EE}=V_{DD}-35V, Ta=25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse width	PW_{CLK}		400	-	-	ns
Strobe pulse width	PW_{STB}		1000	-	-	ns
Data setup time	t_{setup}		100	-	-	ns
Data hold time	t_{hold}		100	-	-	ns
Clock-strobe time	$t_{CLK-STB}$	CLK↑ → STB↑	1000	-	-	ns
Propagation delay time	t_{PZL}	R_L=10KΩ, C_L=15pF	-	-	100	ns
	t_{PLZ}		-	-	400	ns

(Unless otherwise specified, V_{DD}=3.3V, GND=0V, V_{EE}=V_{DD}-35V, Ta=25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse width	PW_{CLK}		400	-	-	ns
Strobe pulse width	PW_{STB}		1000	-	-	ns
Data setup time	t_{setup}		100	-	-	ns
Data hold time	t_{hold}		100	-	-	ns
Clock-strobe time	$t_{CLK-STB}$	CLK↑ → STB↑	1000	-	-	ns
Propagation delay time	t_{PZL}	R_L=10KΩ, C_L=15pF	-	-	100	ns
	t_{PLZ}		-	-	600	ns

SWITCHING CHARACTERISTICS

(Unless otherwise specified, V_{DD}=5V, GND=0V, V_{EE}=V_{DD}-35V, Ta=25℃)

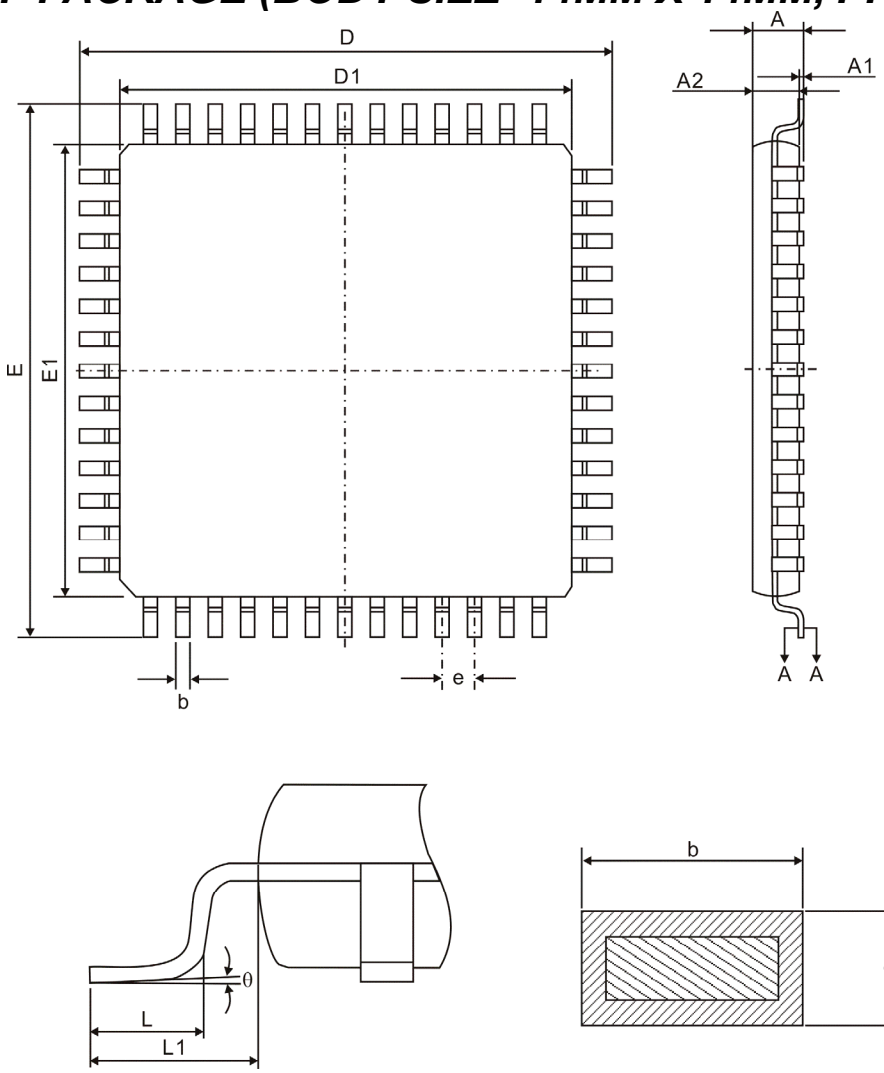
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Grid rise time	t_{GLH}	C_L=300pF	-	-	0.5	μs
Segment rise time	t_{SLH}		-	-	2.0	μs
Grid fall time	t_{GHL}		-	-	150	μs
Segment fall time	t_{SHL}		-	-	150	μs
Oscillation frequency	f_{OSC}	R=82KΩ	350	500	650	KHz

(Unless otherwise specified, V_{DD}=3.3V, GND=0V, V_{EE}=V_{DD}-35V, Ta=25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Grid rise time	t_{GLH}	C_L=300pF	-	-	1.2	μs
Segment rise time	t_{SLH}		-	-	4.0	μs
Grid fall time	t_{GHL}		-	-	150	μs
Segment fall time	t_{SHL}		-	-	150	μs
Oscillation frequency	f_{OSC}	R=100KΩ	350	500	650	KHz

PACKAGE INFORMATION

52-PIN, LQFP PACKAGE (BODY SIZE=14MM X 14MM, PITCH=1.00MM)



Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.35	-	0.50
c	0.09	-	0.20
D	16.60 BSC		
D1	14.00 BSC		
E	16.60 BSC		
E1	14.00 BSC		
e	1.00 BSC		
θ	0°	3.5°	7°
L	0.70	0.85	1.00
L1	1.30 REF		

Note: Refer to JEDEC MS-026

IMPORTANT NOTICE

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