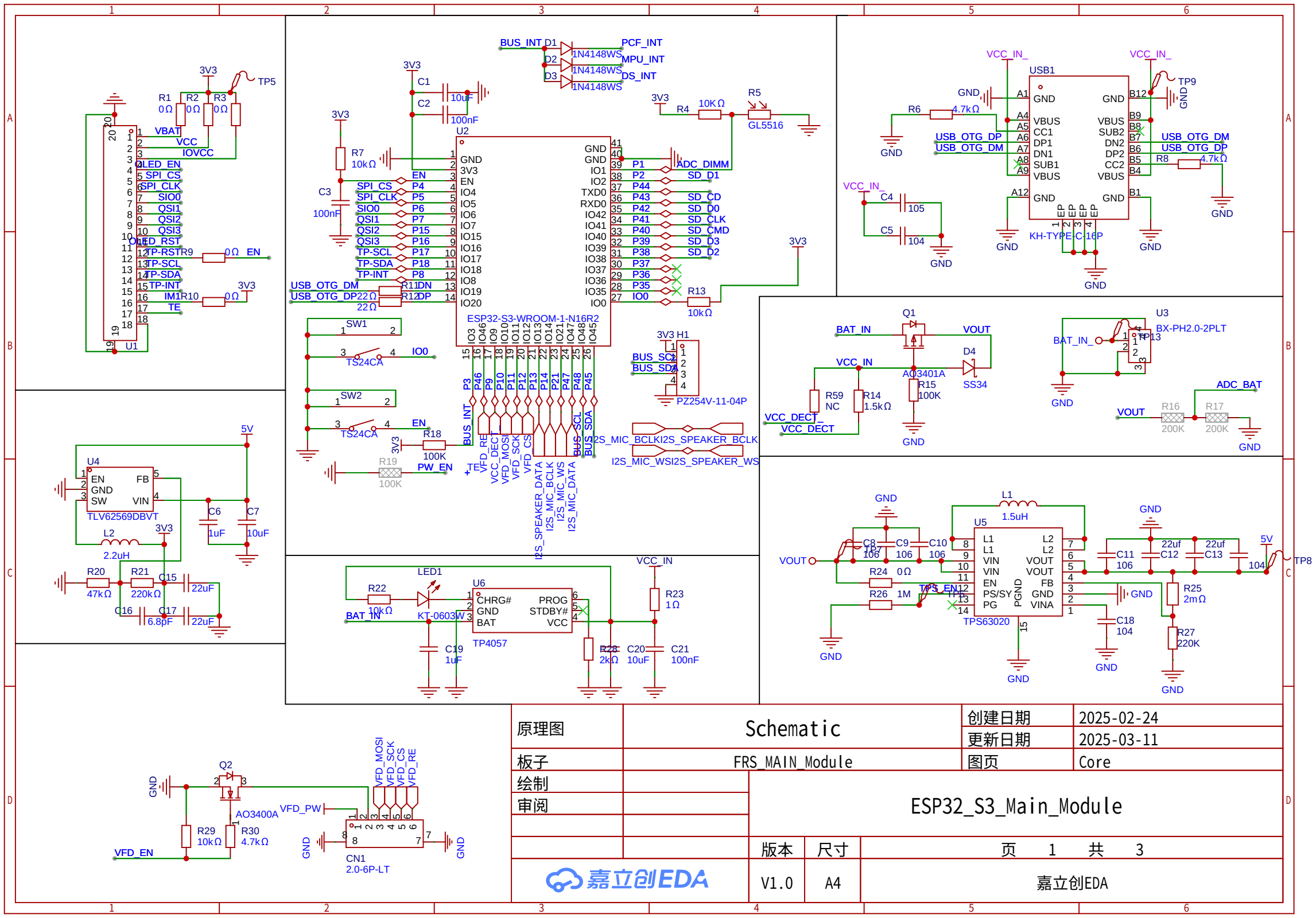
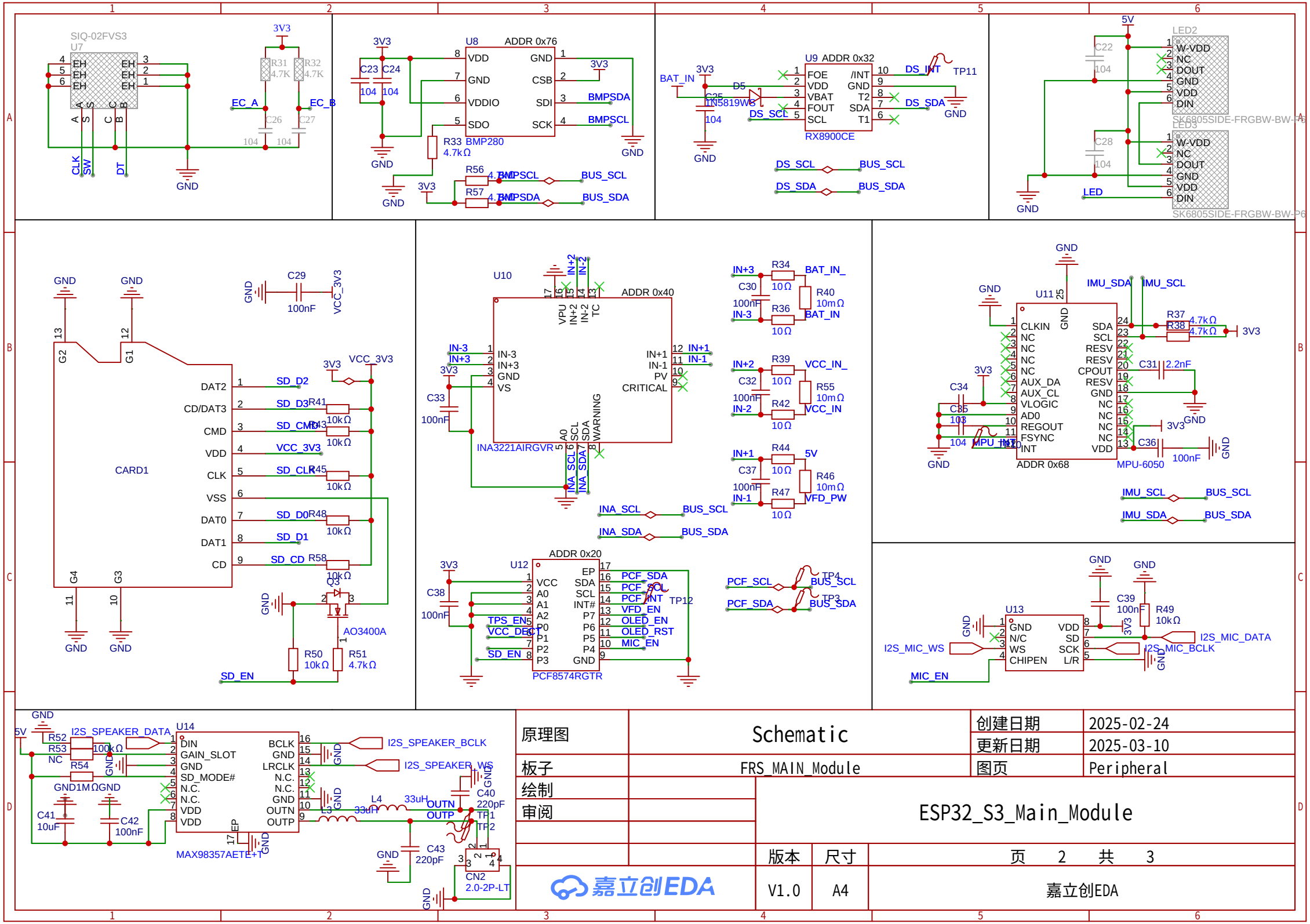


原理图	Schematic	创建日期	2025-02-24
		更新日期	2025-03-11
板子	FRS_MAIN_Module	图页	Core
绘制			
审阅			
	ESP32_S3_Main_Module		
		版本	尺寸
		V1.0	A4
		页 1 共 3	
嘉立创EDA		嘉立创EDA	

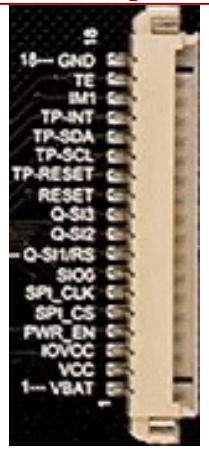


原理图	Schematic	创建日期	2025-02-24
		更新日期	2025-03-10
板子	FRS_MAIN_Module	图页	Peripheral
绘制			
审阅			
	ESP32_S3_Main_Module		
		版本	尺寸
		V1.0	A4
		页 2 共 3	
嘉立创EDA		嘉立创EDA	

DWO LIMITED

PIN DESCRIPTION

NO.	Pin Name	I/O	Description
1	VBAT	P	Battery Voltage 3.8V TYP. (2.9-4.5V)
2	VCC	P	Power supply for display driver IC analog system.
3	IOVCC	P	Power supply for display driver IC interface and logic system
4	PWR_EN	I	Power IC enable control pin. Unused, please open this pin.
5	SPI_CS	I	Chip select input pin ("Low" enable)
6	SPI_CLK	I	SCL: A synchronous clock signal in SPI I/F.
7	SIO0	I/O	Serial Data Input input & output in QSPI,data Lane 0
8	DCX /Q-SI1	I	Serial Data Input in QSPI,data Lane 1; Display data / command selection in 4-wire SPI I/F. D/CX = "0" : Command D/CX = "1" : Display data or Parameter If not used, please connect to VSSI.
9	Q-SI2	I	Serial Data Input in QSPI,data Lane 2
10	Q-SI3	I	Serial Data Input in QSPI,data Lane 3
11	SPI_RESET	I	Display driver reset, must be applied to properly initialize the chip. Signal is active low.
12	TP_RESET	I	TP driver reset. Signal is active low.
13	TP-SCL	I	Touch Panel Clock Input. Communication Voltage follow IOVCC If not used, please open this pin.
14	TP_SDA	I/O	Touch Panel Data Input and output. Communication Voltage follow IOVCC If not used, , please open this pin.
15	TP-INT	O	Touch Panel Interrupt Output. If not used, please open this pin.
16	IM1	I	Dsipaly Interface type selection;
17	TE	O	Tearing Effect
18	GND	P	Ground



GAIN_SLOT = GND through 100kΩ	14.4	15	15.6	dB
GAIN_SLOT = GND	11.4	12	12.6	
GAIN_SLOT = unconnected	8.4	9	9.6	
GAIN_SLOT = V_{DD}	5.4	6	6.6	
GAIN_SLOT = V_{DD} through 100kΩ	2.4	3	3.6	

ESP32-S3 集成了两个 12 位 SAR（逐次逼近寄存器） ADC，ADC1 和 ADC2，支持20 个模拟通道输入。这 20个模拟通道输入对应着具体的 IO。

ADC1型：

10 通道：GPIO1 - GPIO10 只有两个spi，因此，要把sd卡改成sdmc
ADC2型： 唤醒源必须是RTC脚

10 通道：GPIO11 - GPIO20

表 3. Summary of Register Set

POINTER ADDRESS (Hex)	REGISTER NAME	DESCRIPTION	POWER-ON RESET BINARY	POWER-ON RESET HEX	TYPE(1)
0	Configuration	All-register reset, shunt and bus voltage ADC conversion times and averaging, operating mode.	01110001 00100111	7127	R/W
1	Channel-1 Shunt Voltage	Averaged shunt voltage value.	00000000 00000000	0000	R
2	Channel-1 Bus Voltage	Averaged bus voltage value.	00000000 00000000	0000	R
3	Channel-2 Shunt Voltage	Averaged shunt voltage value.	00000000 00000000	0000	R
4	Channel-2 Bus Voltage	Averaged bus voltage value.	00000000 00000000	0000	R
5	Channel-3 Shunt Voltage	Averaged shunt voltage value.	00000000 00000000	0000	R
6	Channel-3 Bus Voltage	Averaged bus voltage value.	00000000 00000000	0000	R
7	Channel-1 Critical Alert Limit	Contains limit value to compare each conversion value to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/W
8	Channel-1 Warning Alert Limit	Contains limit value to compare to averaged measurement to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/W
9	Channel-2 Critical Alert Limit	Contains limit value to compare each conversion value to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/W
A	Channel-2 Warning Alert Limit	Contains limit value to compare to averaged measurement to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/W
B	Channel-3 Critical Alert Limit	Contains limit value to compare each conversion value to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/W
C	Channel-3 Warning Alert Limit	Contains limit value to compare to averaged measurement to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/W
D	Shunt-Voltage Sum	Contains the summed value of the each of the selected shunt voltage conversions.	00000000 00000000	0000	R
E	Shunt-Voltage Sum Limit	Contains limit value to compare to the Shunt Voltage Sum register to determine if the corresponding limit has been exceeded.	01111111 11111110	7FFE	R/W
F	Mask/Enable	Alert configuration, alert status indication, summation control and status.	00000000 00000010	0002	R/W
10	Power-Valid Upper Limit	Contains limit value to compare all bus voltage conversions to determine if the Power Valid level has been reached.	00100111 00010000	2710	R/W
11	Power-Valid Lower Limit	Contains limit value to compare all bus voltage conversions to determine if the any voltage rail has dropped below the Power Valid range.	00100011 00101000	2328	R/W
FE	Manufacturer ID	Contains unique manufacturer identification number.	01010100 01001001	5449	R
FF	Die ID	Contains unique die identification number.	00110010 00100000	3220	R

原理图	Schematic	创建日期	2025-03-03
		更新日期	2025-03-11
板子	FRS_MAIN_Module	图页	Description
绘制		ESP32_S3_Main_Module	
审阅			
		版本	尺寸	页 3 共 3
嘉立创EDA		V1.0	A4	嘉立创EDA