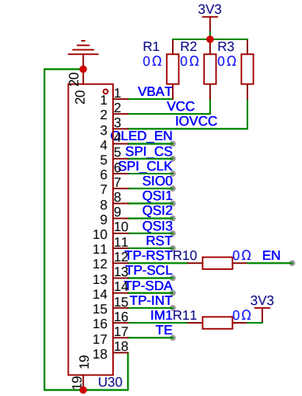
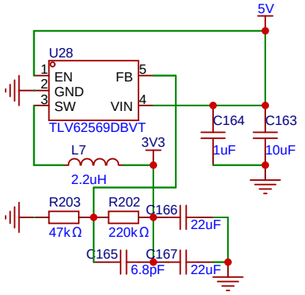
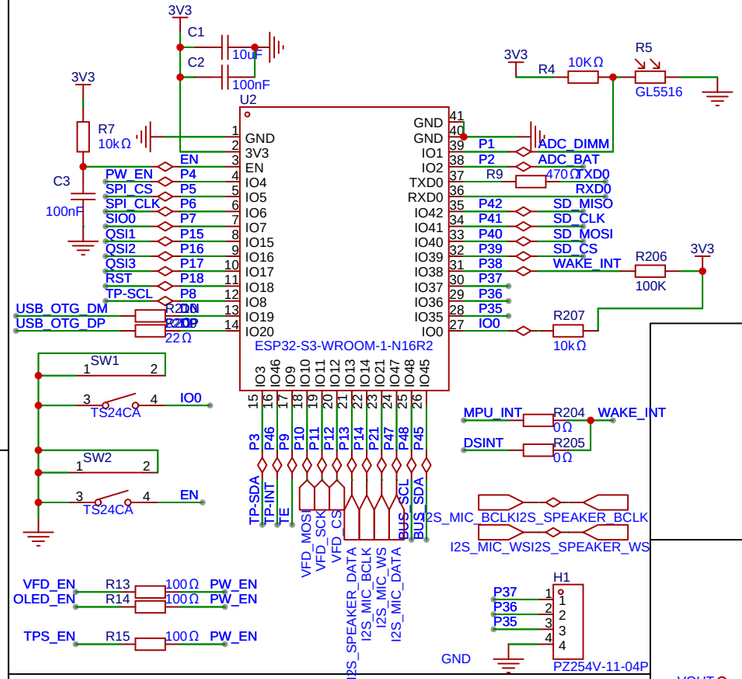
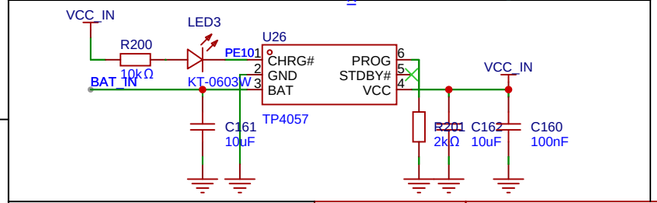
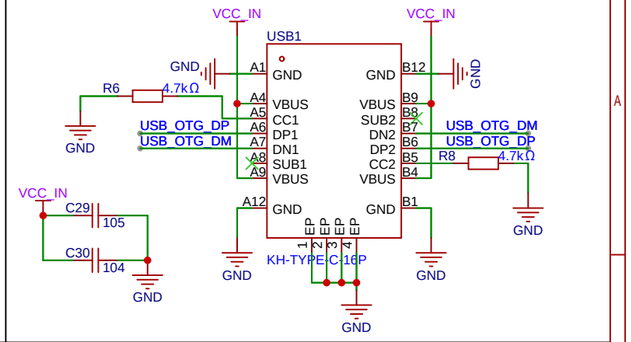
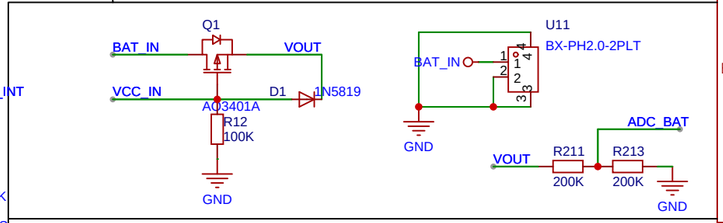


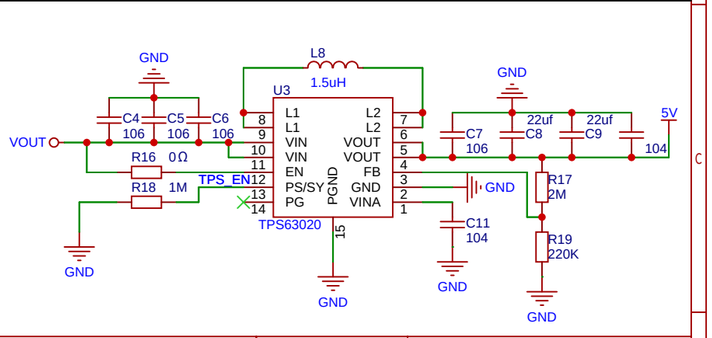


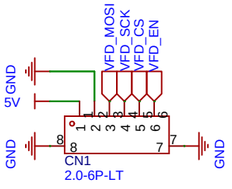










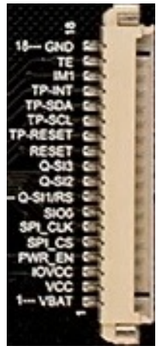


原理图	Schematic	创建日期	2025-02-24
		更新日期	2025-02-24
板子	FRS_MAIN_Module	图页	Core
绘制			
审阅			
	ESP32_S3_Main_Module		
	版本	尺寸	页 1 共 2
嘉立创EDA	V1.0	A4	嘉立创EDA

DWO LIMITED

PIN DESCRIPTION

NO.	Pin Name	I/O	Description
1	VBAT	P	Battery Voltage 3.8V TYP. (2.9-4.5V)
2	VCC	P	Power supply for display driver IC analog system.
3	IOVCC	P	Power supply for display driver IC interface and logic system
4	PWR_EN	I	Power IC enable control pin. Unused, please open this pin.
5	SPI_CS	I	Chip select input pin ("Low" enable)
6	SPI_CLK	I	SCL: A synchronous clock signal in SPI I/F.
7	SIO0	I/O	Serial Data Input input & output in QSPI,data Lane 0
8	DCX /SI-SI1	I	Serial Data Input in QSPI,data Lane 1; Display data / command selection in 4-wire SPI I/F. D/CX = "0" : Command D/CX = "1" : Display data or Parameter if not used, please connect to VSSI.
9	QI-SI2	I	Serial Data Input in QSPI,data Lane 2
10	QI-SI3	I	Serial Data Input in QSPI,data Lane 3
11	SPI_RESET	I	Display driver reset, must be applied to properly initialize the chip. Signal is active low.
12	TP_RESET	I	TP driver reset. Signal is active low.
13	TP-SCL	I	Touch Panel Clock Input. Communication Voltage follow IOVCC If not used, please open this pin.
14	TP_SDA	I/O	Touch Panel Data Input and output. Communication Voltage follow IOVCC If not used, please open this pin.
15	TP-INT	O	Touch Panel Interrupt Output. If not used, please open this pin.
16	IM1	I	Dispaly Interface type selection;
17	TE	O	Tearing Effect
18	GND	P	Ground

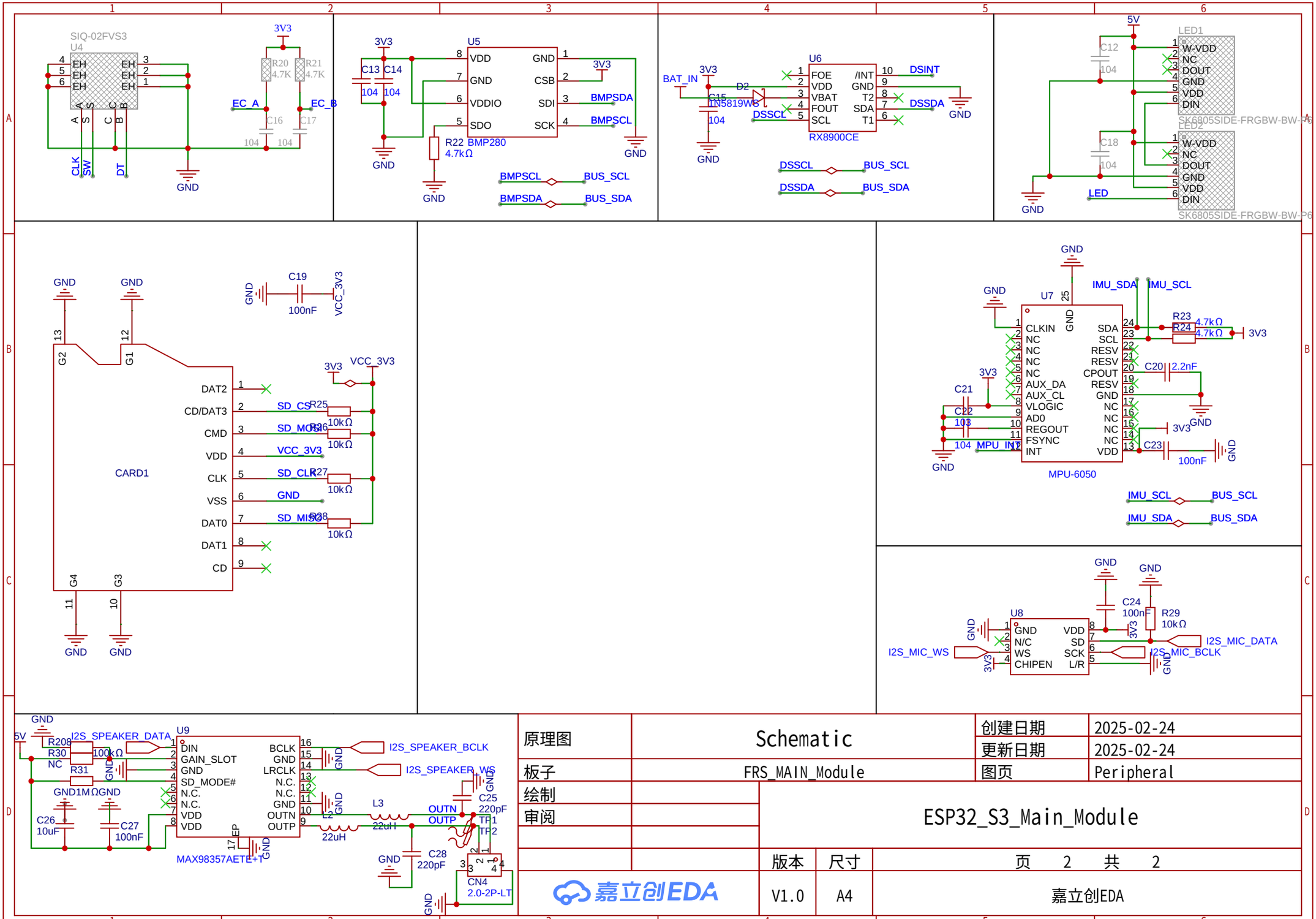


ESP32-S3 集成了两个 12 位 SAR（逐次逼近寄存器） ADC，ADC1 和 ADC2，支持20 个模拟通道输入。这 20个模拟通道输入对应着具体

ADC1型：

10 通道：GPIO1 - GPIO10
ADC2型：

10 通道：GPIO11 - GPIO20



原理图	Schematic	创建日期	2025-02-24
		更新日期	2025-02-24
板子	FRS_MAIN_Module	图页	Peripheral
绘制		ESP32_S3_Main_Module	
审阅			
		版本	尺寸	页 2 共 2
嘉立创EDA		V1.0	A4	嘉立创EDA

GAIN_SLOT = GND through 100kΩ	14.4	15	15.6
GAIN_SLOT = GND	11.4	12	12.6
GAIN_SLOT = unconnected	8.4	9	9.6
GAIN_SLOT = V_{DD}	5.4	6	6.6
GAIN_SLOT = V_{DD} through 100kΩ	2.4	3	3.6

dB