原件
VFD开发

DAEWOO

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SPECIFICATION

MWO

VACUUM FLUORESCENT DISPLAY

HCM-09MS33T

	Date	Descriptions	Approved by
1	2012.06.05	Refer to REVISION RECORD	
2	2013.9.13		
3			
4			
5			
6			
7			
8			
9			
10			

Designed by	Checked by	Approved by
2012.06.05	2012.06.05	

Customer's Approval

REVISION RECORD

MODEL	HCM-09MS33T

REV.	REVISION RECORD	REVISION DETAILS	ISSUED DATE
1	▸ ORIGINAL --- rev 1		05-Jun-2012
2	▸ ELECTRICAL CHARACTERISTICS --- rev 2 ▸ OPTICAL CHARACTERISTICS --- rev2 ▸ SWITCHING WAVEFORM --- rev 2 ▸ BLOCK DIAGRAM --- rev 2	IC change	13-Sep-2013

1. ELECTRICAL CHARACTERISTICS(HCM-09MS33T,Rev2,13-Sep-2013)

ABSOLUTE MAXIMUM RATINGS(Ta=25℃, GND = 0V)

ITEMS	SYMBOL	VALUE	UNIT
Logic Supply Voltage	VDD1	-0.3 ~ +7.0	Vdc
Logic Input Voltage	VI	-0.3 ~ VDD1+0.3	Vdc
Driver Supply Voltage	VDD2	-0.3 ~ +88.0	Vdc
Operating Temperature	Topr	-40 ~ +85	℃
Storage Temperature	Tstg	-55~+85	℃

NOTE 1. Top and Tstg are a temperature surrounding the panel. (1cm approx.)

RECOMMENDABLE OPERATING CONDITIONS(Duty=1/10)

ITEMS	SYMBOL	Condition	MIN.	TYP.	MAX.	UNIT
Filament Voltage	Ef	-	2.34	2.6	2.86	Vac
Logic Supply Voltage	VDD1	-	4.5	5.0	5.5	Vdc
Driver Supply Voltage	VDD2	-	24.3	27.0	29.7	Vdc
High Level Input Voltage	VIH	Logic	0.8VDD1	-	VDD1	Vdc
Low Level Input Voltage	VIL	Logic	0	-	0.2VDD1	Vdc
Cut-off Voltage	Ek	-	3.8	-	4.8	Vdc

DC CHARACTERISTICS

Filament Current	If	-	225	250	275	mA
Logic Supply Current	IDD1	No load,Data input all H	-	-	5	mA
Driver Supply Current(AVERAGE)	IDD2(AVE)	-	-	12	24	mA
Driver Supply Current(PEAK)	IDD2(PEAK)	-	-	31	62	mA
High Level Input Current	IIH	VIN = VDD1	-	0.1	1	μA
Low Level Input Current	IIL	VIN = VSS; DI, CLK, STB	-2	-	2	μA
		VIN = VSS; BLK,DIR	-220	-	-45	μA

AC CHARACTERISTICS

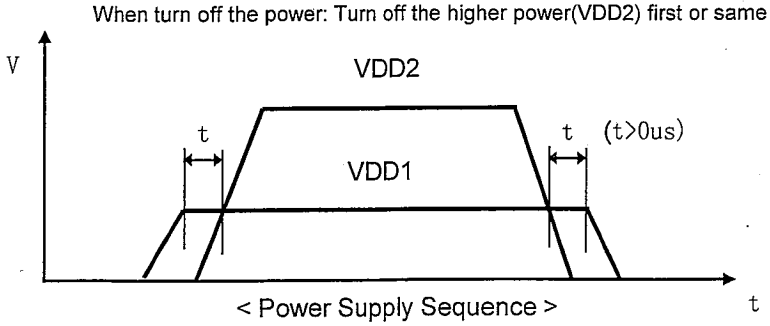
Frame Frequency	-	-	100	-	-	Hz
Clock Frequency	fCLK	Duty=45~55%	-	-	12	MHz
Data Setup Time	tSU(D)	-	10	-	-	ns
Data Hold Time	tHO(D)	-	10	-	-	ns
Clock to Latch Time	tCL	CLK↑→STB↑	30	-	-	ns
Latch Pulse Width	tw(L)	-	30	-	-	ns
Latch to Clock Time	tLC	STB↓→CLK↓	30	-	-	ns
Blanking to Latch Time	tBL	BLK↑→STB↑	600	-	-	ns
Latch to Blanking Time	tLB	STB↓→BLK↓	60	-	-	ns
Clock to Data Output Time	tPHL(L)	CL = 15pF	-	40	50	ns
	tPLH(L)		-	40	50	ns
Driver Output Transfer Time	tPLH(Q)	CL=50pF, RL=220KΩ	-	900	1200	ns
	tPHL(Q)		-	900	1200	ns
Driver Output Rising Edge Time	tr(Q)		-	150	250	ns
Driver Output Falling Edge Time	tf(Q)		-	300	500	ns

NOTE 2. Exceeding these values may damage this panel.

NOTE 3. Panel may be demaged under the scan stop.

NOTE 4. When turn on the power : Turn on the lower power(VDD1) first or same time

When turn off the power: Turn off the higher power(VDD2) first or same time

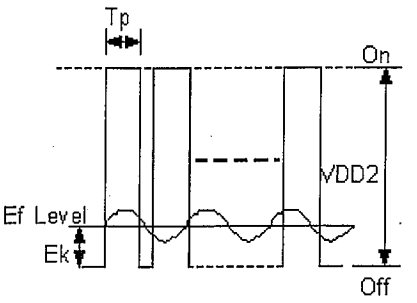


< Power Supply Sequence >

NOTE 5. Do not pull down the lower power(VDD1) under 4.5V,because the Logic HIGH level is unstable

NOTE 6. Quality can be assured only within above rated value and this value is most optimized condition for the Brightness & life time.

2. OPTICAL CHARACTERISTICS(HCM-09MS33T,Rev2,13-Sep-2013)

ITEMS	TEST CONDITION	Color	MIN.	TYP.	MAX.	UNIT
Brightness	Ef=2.6Vac, VDD1=5.0Vdc VDD2=27.0Vdc (Ek=3.8Vdc) Tp=100μs ,Tb=0μs, Duty=1/10  	GREEN	102	204	—	ft-L
		Cd-free Rsh.O.	20	41	—	
Brightness Ratio Between Digits		$\frac{L(MAX)}{L(MIN)}$	-	-	2	
Color Coordinate		GREEN (G. :x=0.250,y=0.439) Cd-free REDDISH ORANGE (Cd-free Rsh.O. :x=0.62,y=0.37)				

NOTE7. All phosphor is Cd-free phosphor.

3. TRUTH TABLE

TRUTH TABLE 1. (SHIFT REGISTER)

CLK	
	One(1) bit data shift
H or L	Data hold

NOTE 8. Input data for shift-register is DI.

TRUTH TABLE 2. (STB, DRIVER)

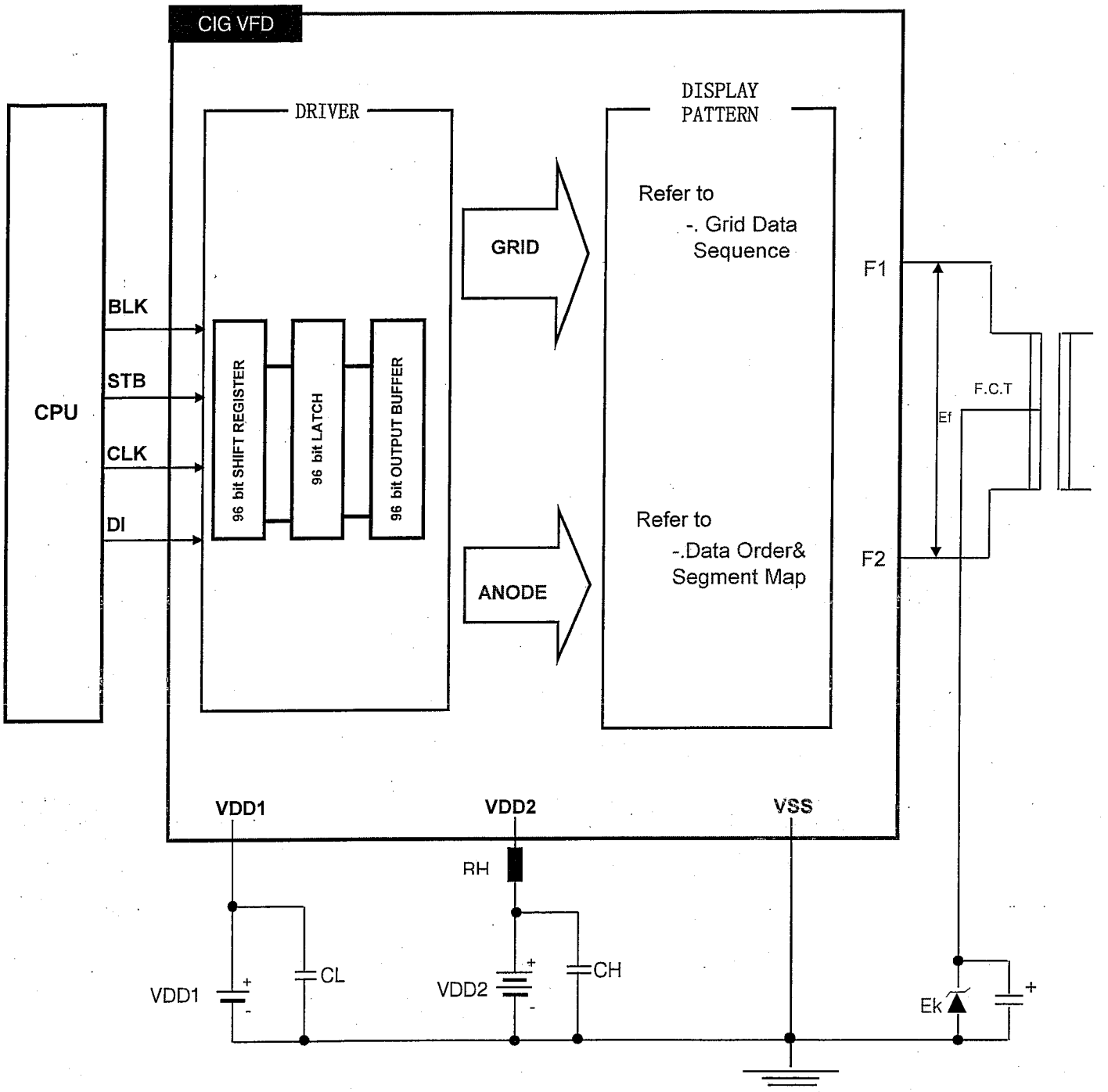
DI	STB	BLK	DRIVER OUTPUT
X	X	H	L
L	H	L	L
H	H	L	H
X	L	L	output data is latched

NOTE 9. X = H or L , H = High level , L = Low level

PIN DESCRIPTION

pin name	description	I/O
VDD1	Logic power supply	-
VDD2	High voltage power supply for driving VFD	-
VSS	Ground	-
CLK	Shift register clock input	I
DI	Serial data input	I
STB	Latch strobe Input Pin. Shift register data is outputted at LAT high level and latched at fallingedge of LAT.	I
BLK	Blanking Input Pin. When this pin is set to high level or floating, the driver pins are set to low level.	I

4.BLOCK DIAGRAM (HCM-09MS33T,Rev2,13-Sep-2013)



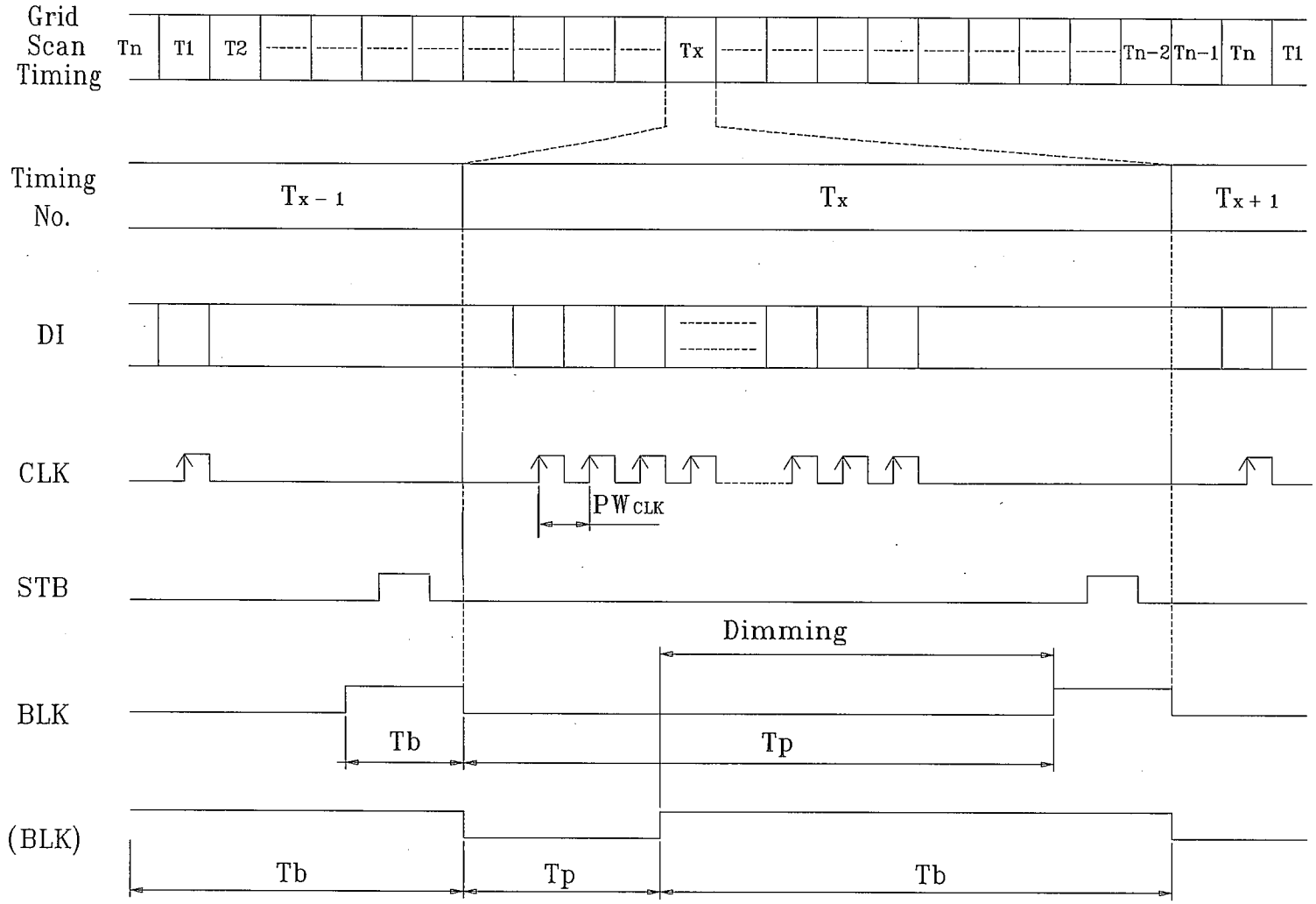
NOTE

RH:22Ω. Current limit resistor for protecting IC.

CH,CL: 0.1μF. Low pass filter for noise filtering.

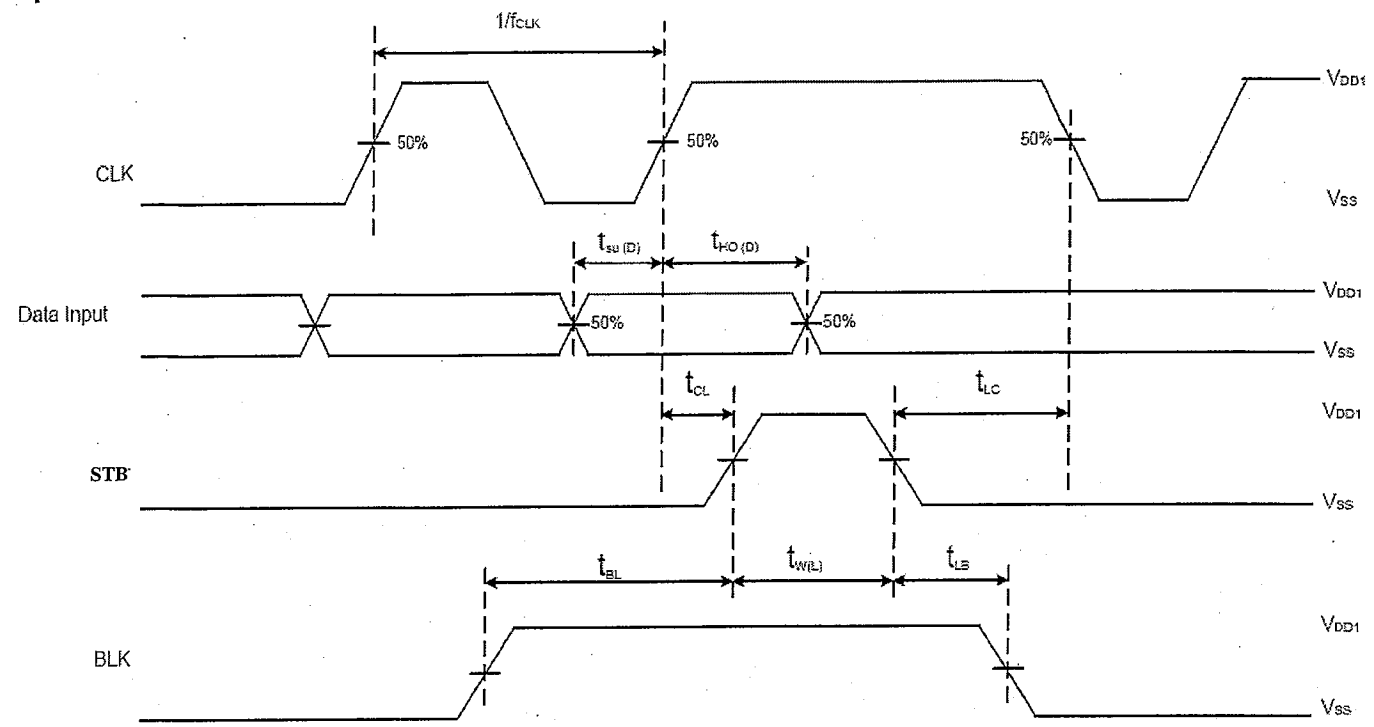
FCT: Filament is center-tab grounded.

5.TIMING CHART (HCM-09MS33T,Rev1,05-Jun-2012)



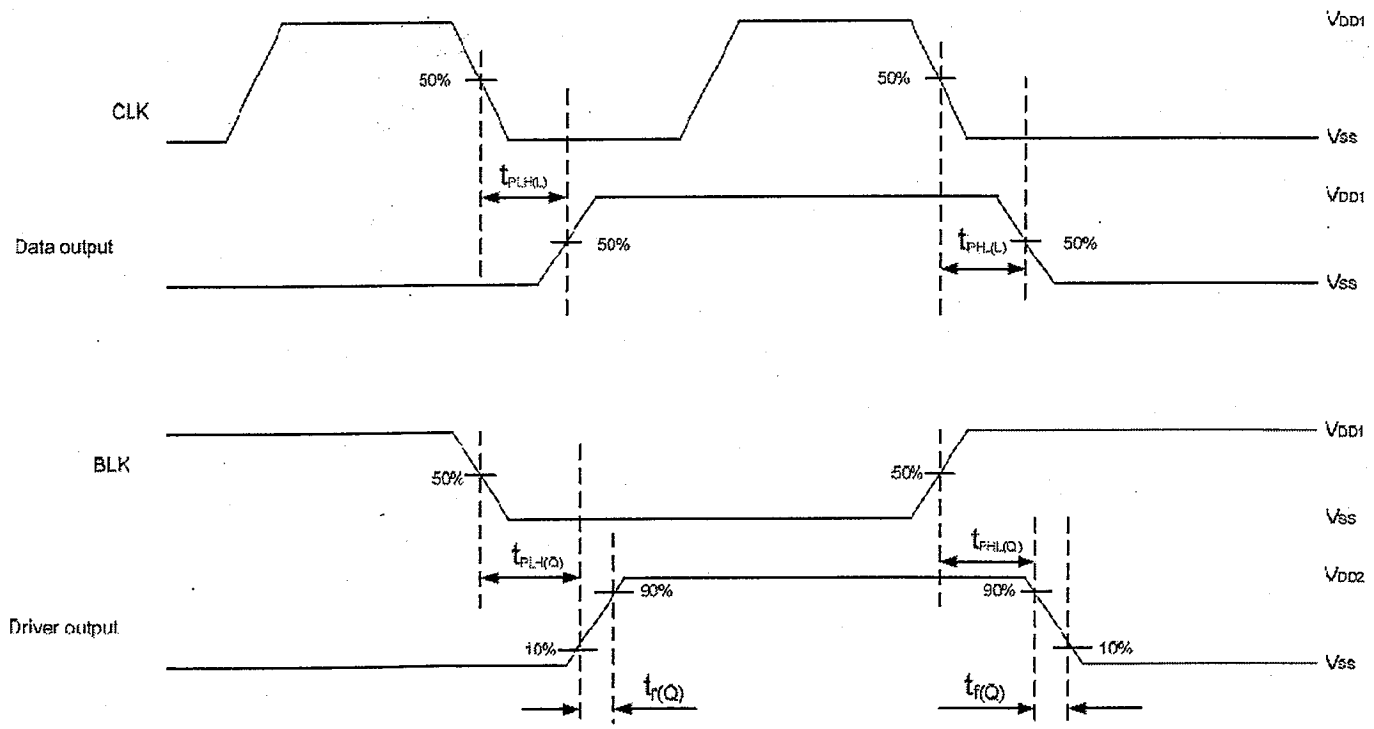
6.SWITCHING WAVEFORM (HCM-09MS33T,Rev2,13-Sep-2013)

Input

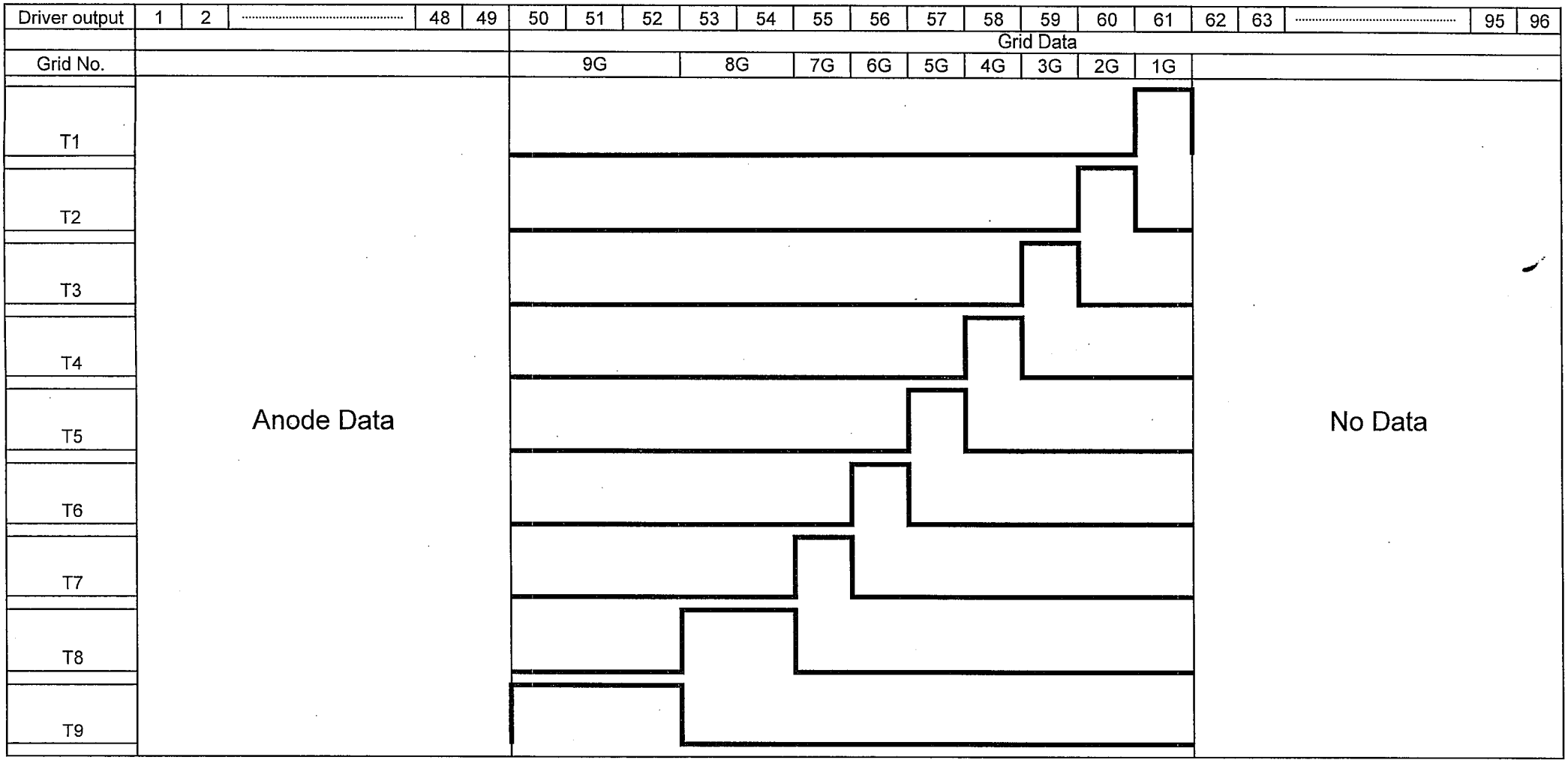


Note: LAT signal can be active only when BLK signal is high level.

Output



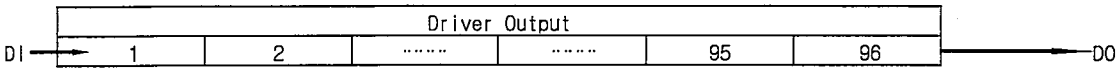
7.GRID DATA SEQUENCE (HCM-09MS33T,Rev1,05-Jun-2012)



8.SEGMENT MAP (HCM-09MS33T,Rev1,05-Jun-2012)

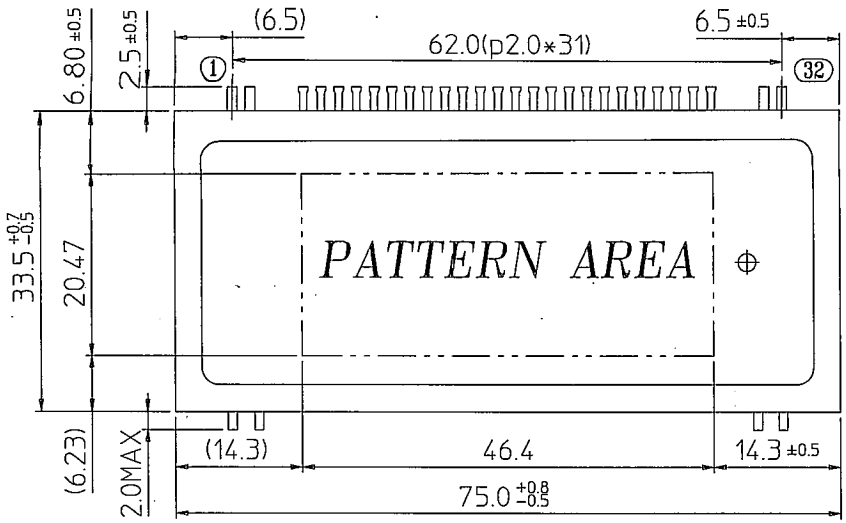
	SEGMENT								
DRIVER OUTPUT	9G	8G	7G	6G	5G	4G	3G	2G	1G
1		49							
2		48							
3		47							
4		46							
5		45							
6		44							
7		43							
8		42							
9		41							
10		40							
11		39							
12		38							
13		37							
14		36							
15		35							
16		34							
17		33							
18		32							
19		31							
20		30							
21		29							
22		28							
23		27							
24		26							
25		25							
26		24							
27		23							
28		22							
29		31							
30		20							
31		19							
32		18							
33		17							
34		16					col2		
35		15					col1	s1	
36	MICROWAVE	14	a	a	a	a	a	a	a
37	REHEAT	13	f	f	f	f	f	f	f
38	SENSOR	12	h	h	h	h	h	h	h
39	DEFROST	11	j	j	j	j	j	j	j
40	CONVECTION	10	k	k	k	k	k	k	k
41	2(GRILL)	9	b	b	b	b	b	b	b
42	1(GRILL)	8	g	g	g	g	g	g	g
43	GRILL	7	m	m	m	m	m	m	m
44	LBS	6	e	e	e	e	e	e	e
45	OZ	5	r	r	r	r	r	r	r
46	CUPS	4	p	p	p	p	p	p	p
47	2(STAGE)	3	n	n	n	n	n	n	n
48	1(STAGE)	2	c	c	c	c	c	c	c
49	STAGE	1	d	d	d	d	d	d	d
50	Grid Scan Data								
51									
52									
53									
54									
55									
56									
57									
58									
59									
60									
61									
62	NO Data								
63									
95									
96									

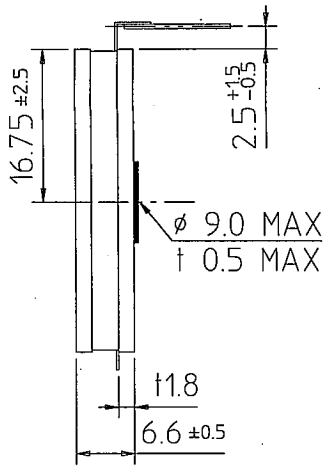
■ DATA SHIFTING DIRECTION

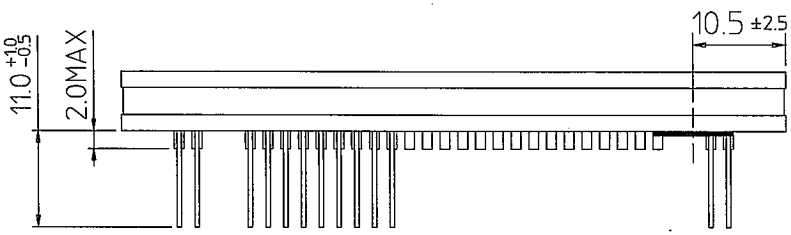


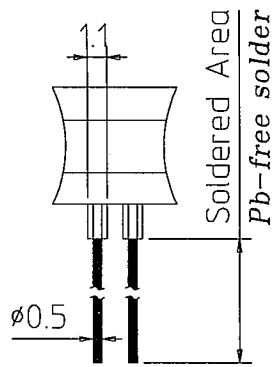
☞ GRID and ANODE is the same data shifting direction

OUTER DIMENSIONS









LEAD DETAIL

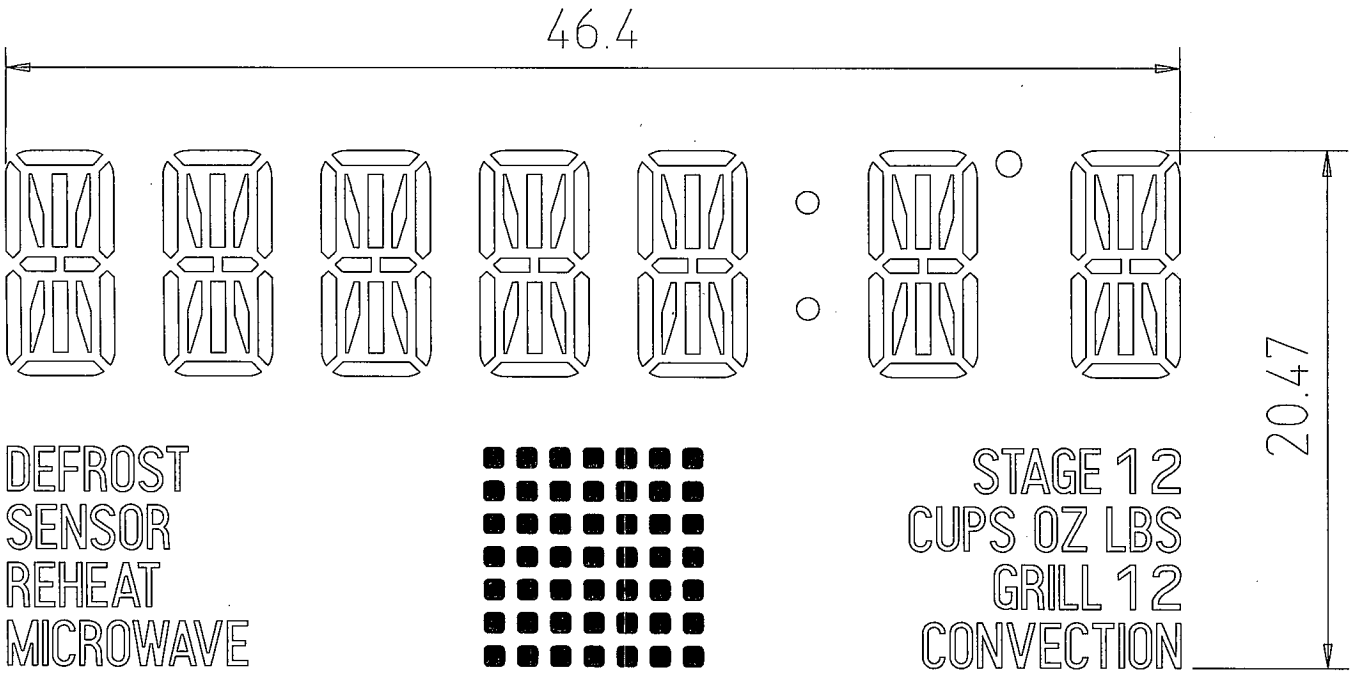
PIN CONNECTION

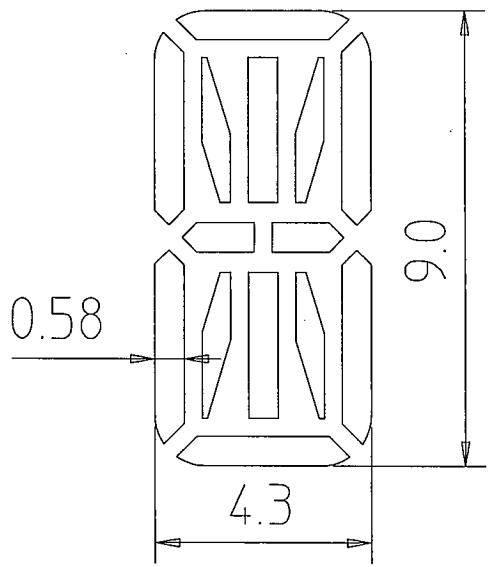
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14-27	28	29	30	31	32
CONNECTION	F1	F1	NP	NP	VDD2	VSS	VSS	VDD1	BLK	STB	DO	CLK	DI	NX	NX(IC)	NP	NP	F2	F2

◉ Note ◉
1) Fn : Filament pin
2) NP : No pin
3) NX : No extended pin
4) NX(IC) : Pins are internally connected, and should be electrically opened on the PCB

MODEL : HCM-09MS33T
OUTER DIMENSIONS
Rev. ① 05-Jun-2012

PATTERN DETAILS



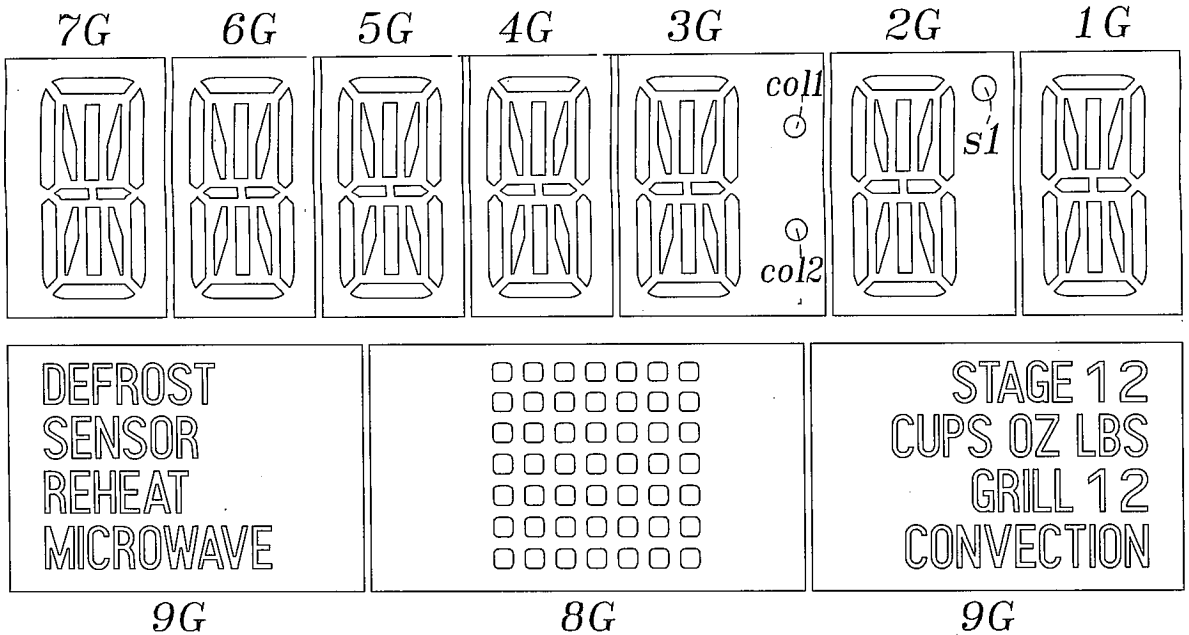


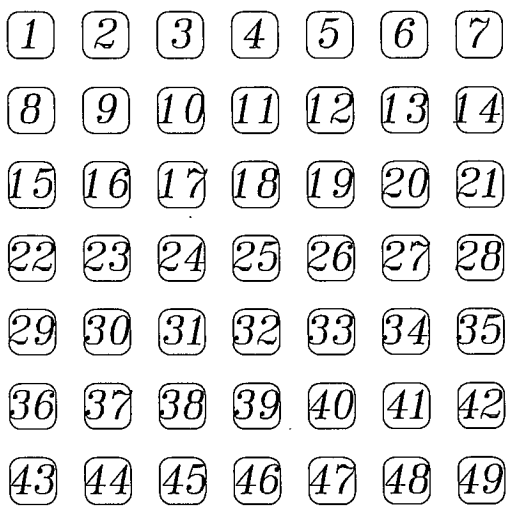
◎ Color of Illumination ◎

- cd-free Reddish Orange (cd-free Rsh.0. x=0.62, y=0.37) ----- Hatched patterns.
- Green (G. x=0.250, y=0.439) ----- Others.

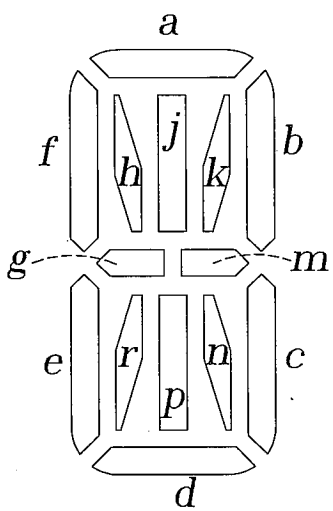
MODEL : HCM-09MS33T
PATTERN DETAILS
Rev. ① 05-Jun-2012

GRID ASSIGNMENT





(8G)



(1G~7G)

MODEL : HCM-09MS33T
GRID ASSIGNMENT
Rev. ① 05-Jun-2012